# Verilog HW#1: Matrix-Vector Computations


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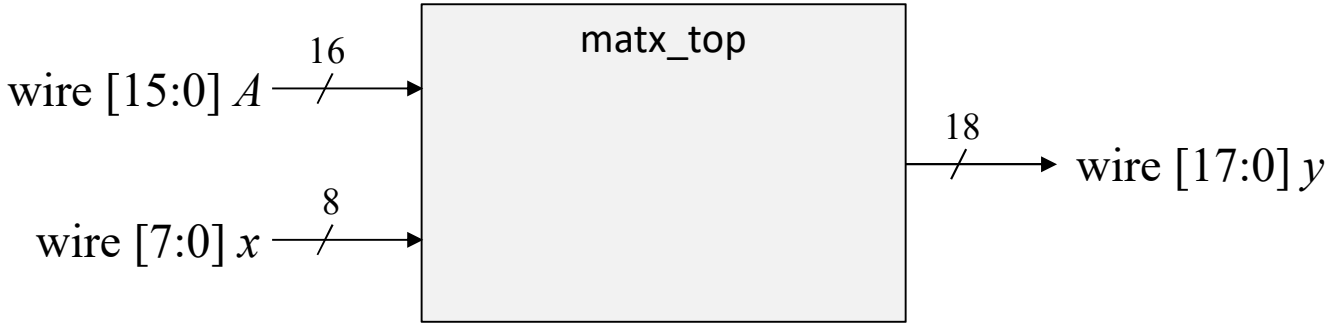
# Verilog HW#1

- Goal: Design a combinational (memoryless) digital circuit that computes the multiplication of a 2×2 matrix and a 2×1 vector.
  - Your design must contain at least two modules, a top-level module ‘matx_top’ that instantiates the entire circuit and a ‘dot’ module that computes the inner-product of two 2×1 vectors.
  - Each entry in the matrix and vector is a 4-bit unsigned number.
- Deadline: 3/29, 23:55pm. You must upload your Verilog files to the E3 website by the deadline.

# I/O ports of the ‘matx_top’ Module

- Your module should be called ‘matx_top’, with the following input/output ports:




  - $A$ and $x$ are the input 2×2 matrix and 2×1 vector, respectively.
  - $y = Ax$ is the output 2×1 vector.

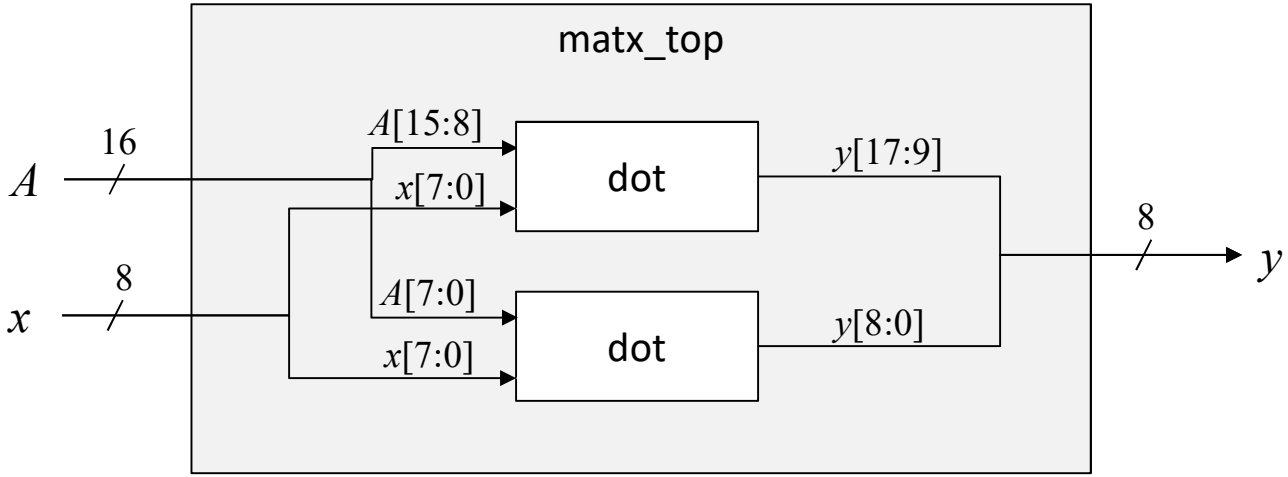
# Data Signal Format

- The matrix $A_{2\times 2} = \begin{pmatrix} a_{00} & a_{01} \\ a_{10} & a_{11} \end{pmatrix}$ is input using the 16-bit signal $A$ in row-major order: $A = [a_{00}, a_{01}, a_{10}, a_{11}]$
  - Note that each $a_{ij}$ is a 4-bit unsigned number.

- The vectors $x = \begin{pmatrix} x_0 \\ x_1 \end{pmatrix}$ and $y = \begin{pmatrix} y_0 \\ y_1 \end{pmatrix}$ are represented similarly: $x = [x_0, x_1]$, $y = [y_0, y_1]$.
  - Note that each $x_i$ is a 4-bit unsigned number and each $y_i$ is a 9-bit unsigned number.

# Block Diagram of the ‘matx_top’ Module

- The block diagram of the top-level module should be as follows:




- The module ‘dot’ computes the inner-product of two 2×1 vectors.

# Requirements for Verilog HW#1

- The top-level module you designed must be declared as follows:

```
module matx_top(input [15:0] A, input [7:0] x, output [17:0] y);

  /* Implement your design here. */

endmodule
```

- Do not upload your testbench module to E3, just upload the `matx_top()` module and its supporting modules (if you have more than one modules/files). TA's will use their own testbench to test your module.