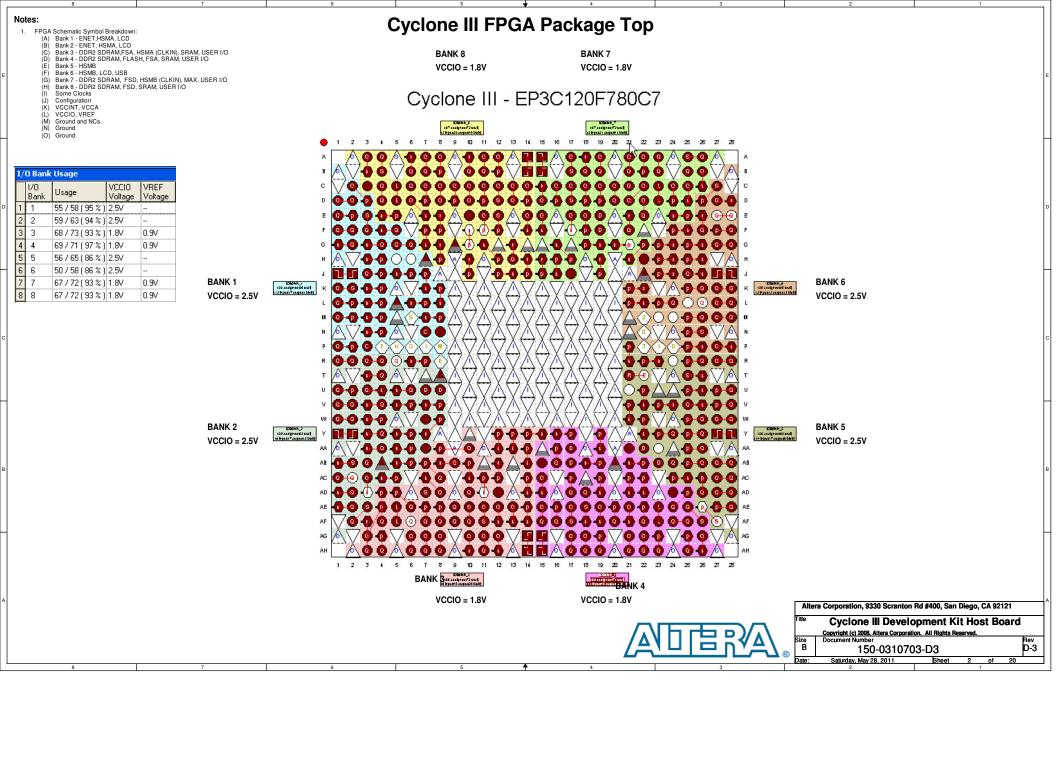
| NOTES: | REV | DATE | PAGES | DESCRIPTION |
|---|------------|------------------------|--------------|--|
| 1. Project Drawing Numbers: Raw PCB Gerber Files 110-0310703-D1 Gerber Files 120-0310703-D1 PCB Design Files 120-0310703-D1 Assembly Drawing 130-0310703-D1 Fab Drawing 140-0310703-D1 Fab Drawing 140-0310703-D1 Schematic Drawing 150-0310703-D1 Bill of Materials 170-0310703-D1 Schematic Design Files 180-0310703-D1 Schematic Design Files 180-0310703-D1 | B-1 C-1 | 8/13/2007 10/2/2007 | ALL | Release B-1 Moved C507 to pwr instead of gnd, Changed D35 to 40V schottky, Routed DEV. SEL & JTAG_SEL jumper signals back to MAXII, Changed VCCA and VCCD PLL power decoupling, Changed R35,R38 to DNI, Changed CPU_RESETn pullup to 2.5V and changed MAXII pin to 2.5V bank, Changed current sense circuit completely to version from SIII Host Board and added more measurements, Moved several MAXII pins to accomodate more 2.5V signals to power measurement circuit. Changed OLED display connector to DNI, Increased output and coupling caps on -12V reg Changed U36,U37,C79,R85,C78,C478,R227,R228_C247-248, R140 to DNI (do not |
| Functional Specification 210-0310703-D1 PCB Layout Guidelines 220-0310703-D1 Assembly Rework 320-0310703-D1 | | 10/9/2007 | 3,4,5 | install), shorted pins 1 to 5 on U36, shorted pins 1 to 3 on U37. Changed R13,R24,R26,R32,R43,R4,R46,R48,R49,R51,R80,R81,R134 from 3mohm to 9mohm. Changed LTC1865L to LTC2402 (24-bits). Added pullup to LCD_SERn. |
| 2. 938 Parts, 61 Library Parts, 803 Nets, 4689 Pins | D-2 | 10/2/2008 | 16 | Change the R54-R56, R60-62, and R77-R79 part number from 220 ohm reistors to 0 ohm resistors to match the BOM. |
| | D-3 E-1 | 12/3/2008 5/20/2011 | 16 1,4,12 | Change R61 from 0 ohm to 220 ohm. Change bias voltages V1 V2 V3 V4 V5 to positive voltages and remove -12V regulator circuit. LCD changed from F-51852 series to F-55472 series. Depopulated U9 Cypress USB Device |
| | | | | PAGE DESCRIPTION |
| Cyclone III F780 Development Kit Host | | | | 1 Title, Notes, Block Diagram, Revision History |
| | | | | 2 C3 FPGA Package Top |
| Block Diagram | | | | 3 Power 1 |
| Power State | | | | 4 Power 2 |
| Port B RJ45 | | | | 5 Current Sense - |
| | | | | 6 Cyclone III Power |
| Display + 125MHz + 1 | | | | 7 Cyclone III Clocks |
| CMOS CMOS CMOS CMOS | | | | 8 MAX II |
| | | | | 9 DDR2 SDRAM (x72) |
| c | ٦ | | | 10 DDR2 SDRAM POWER & TERM |
| 2.5V CMOS 2.5V CMOS 10/100/1000 | | | | 11 SRAM & FLASH |
| * EPM2243GF256 * Ethernet PHY | * | | | 12 USB 2.0 |
| (×32) | | | | 13 10/100/1000 Ethernet |
| 8MB SRAM 1.8V CMOS 2.5V CMOS Cropbics LCD | 7 | | | 14 HSM Connectors |
| | * | | | 15 HSM Termination |
| (x32) Cyclone III | | | | 16 User IO & Connector |
| 64MB*Flash SMA hyxat EP3C120F780 SMA Output | ٦ | | | 17 Cyclone III Configuration |
| (x16) Character LCD | * | | | 18 Cyclone III Banks 1,2,5&6 |
| | | | | 19 Cyclone III Banks 3,4,7&8 |
| 256MB DDR2 1.8V SSTI 2.5V CMOS LP Filter and | 1 | | | 20 Decoupling |
| Dual-Channel 1.8V SSTL Audio Amp | * | | | 21 |
| (x72) | | | | 22 |
| | | | | 23 |
| | | | | 24 |
| 50MHz PC | | | | 25 |
| Buttons, Quad 7-Seg, Speaker | | | | 26 |
| Switches User LEDs Header | | | | 27 |
| SWITCHES OSEI LEDS Header | | | | Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121 |
| | | | | Title Cyclone III Development Kit Host Board |
| | Ы | | \triangle | Copyright (c) 2008. Altera Corporation. All Rights Reserved. |
| Digital Ground | Ш | <u> 三元</u> | <u>A</u> | Size Document Number Rev E-1 |
| 8 7 6 5 1 4 | | 3 | | 2 1 |

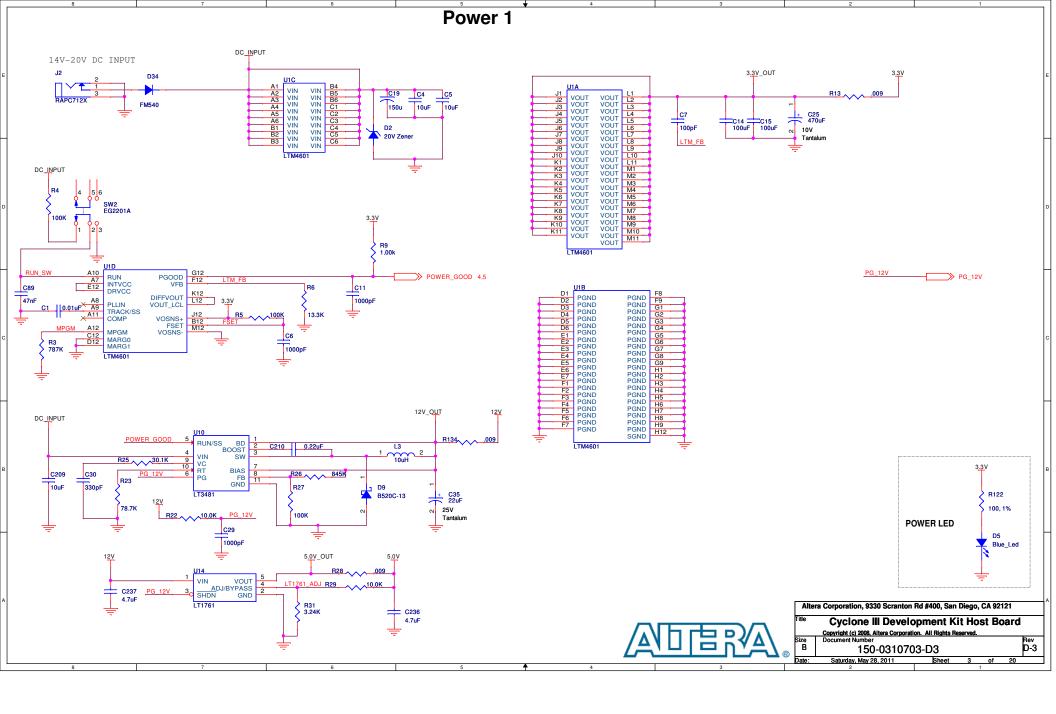
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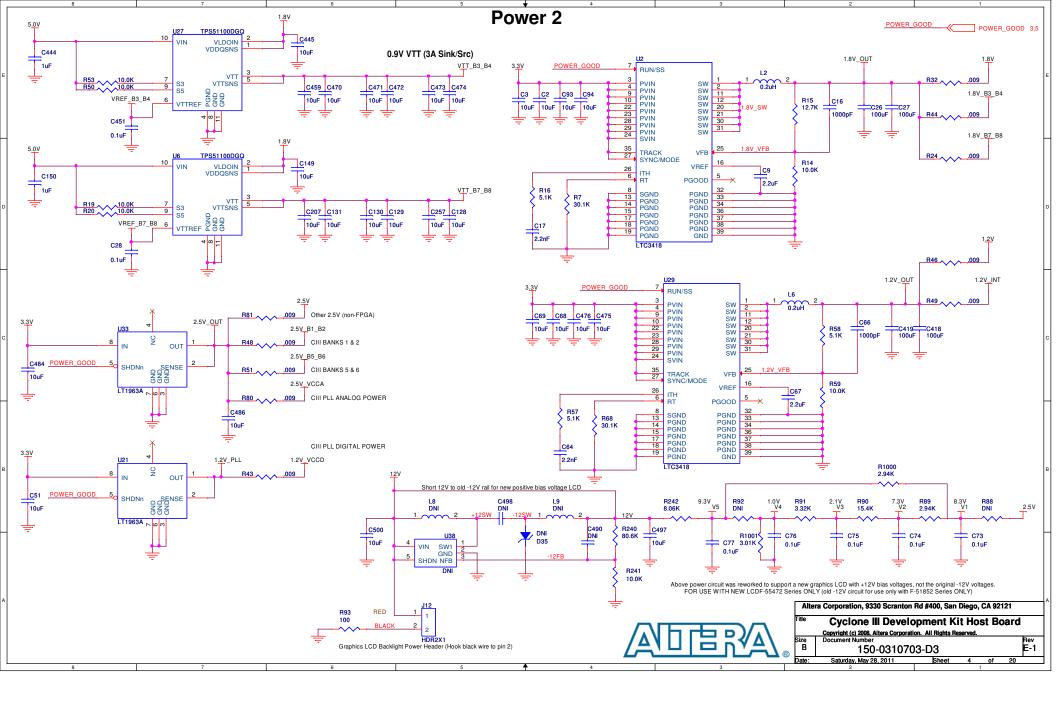
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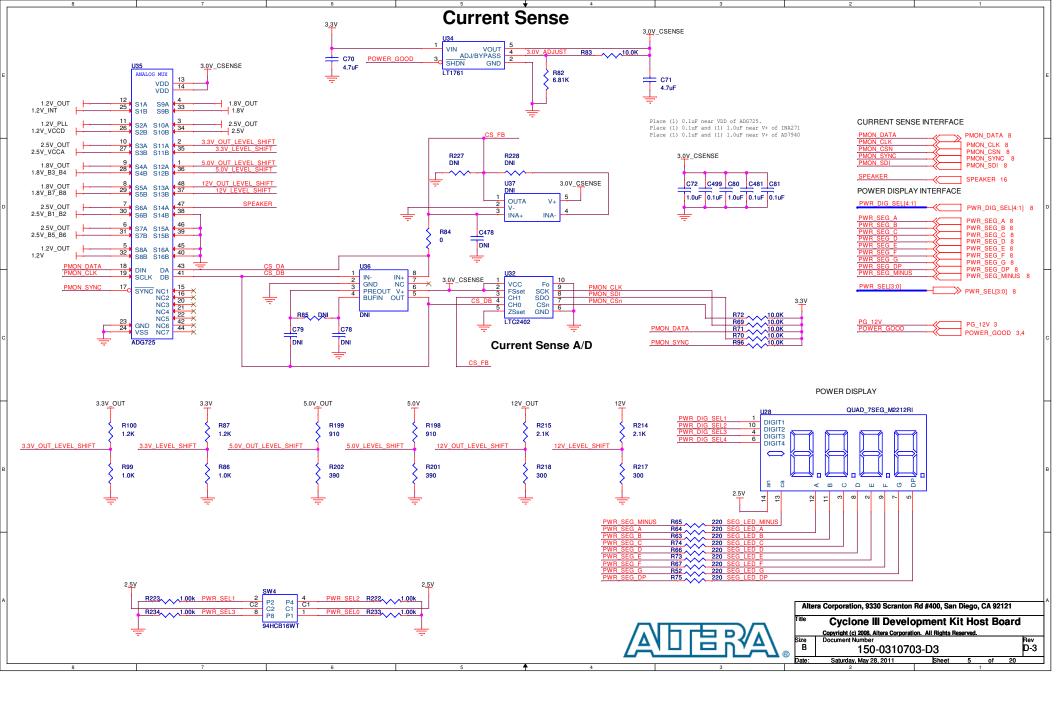
PAGES

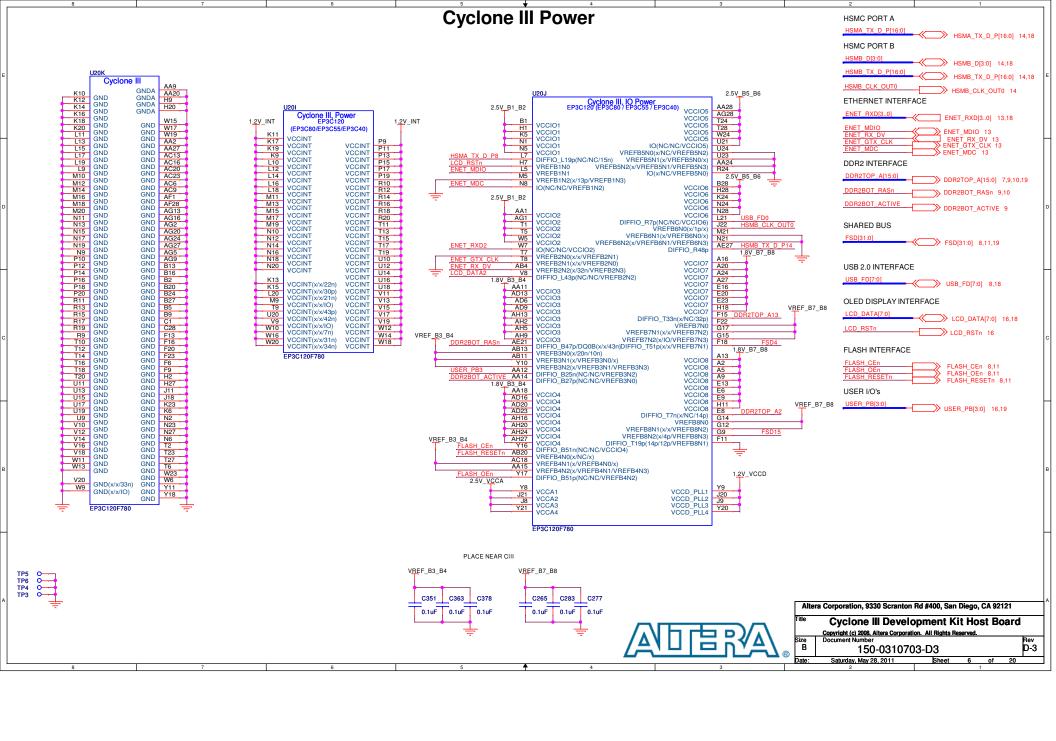
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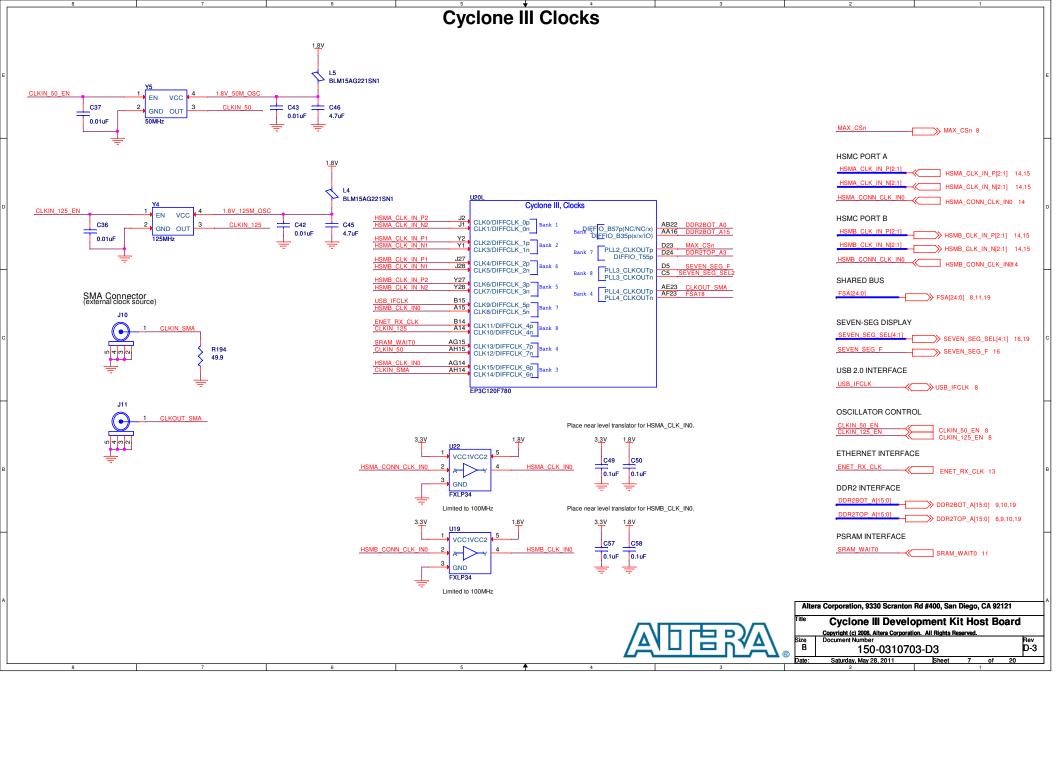


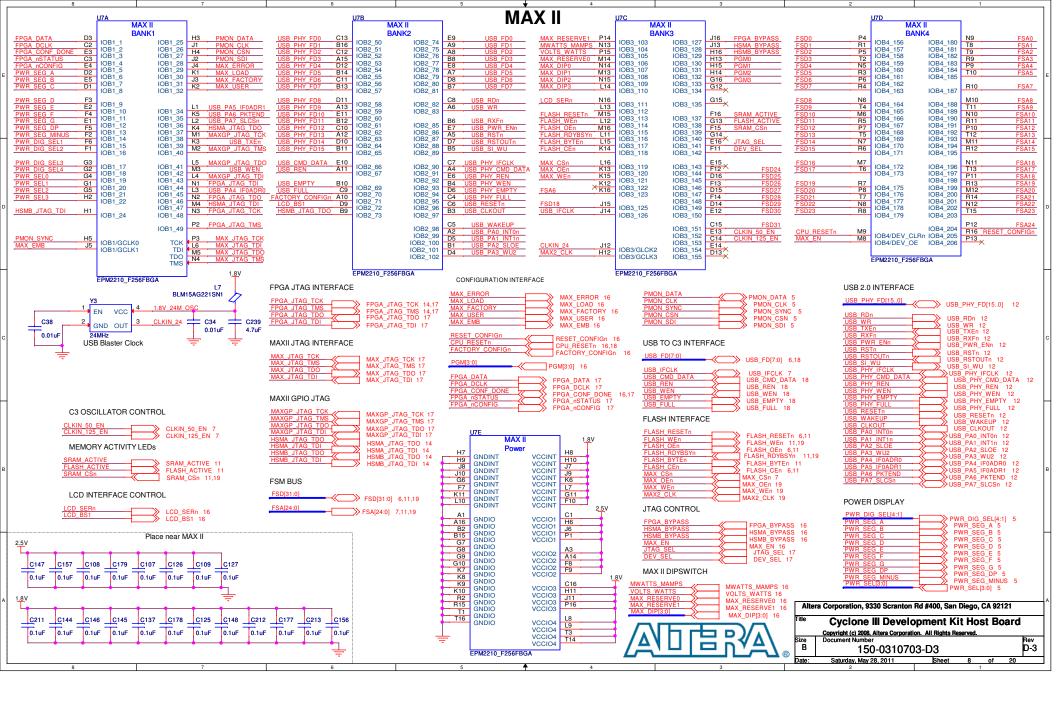


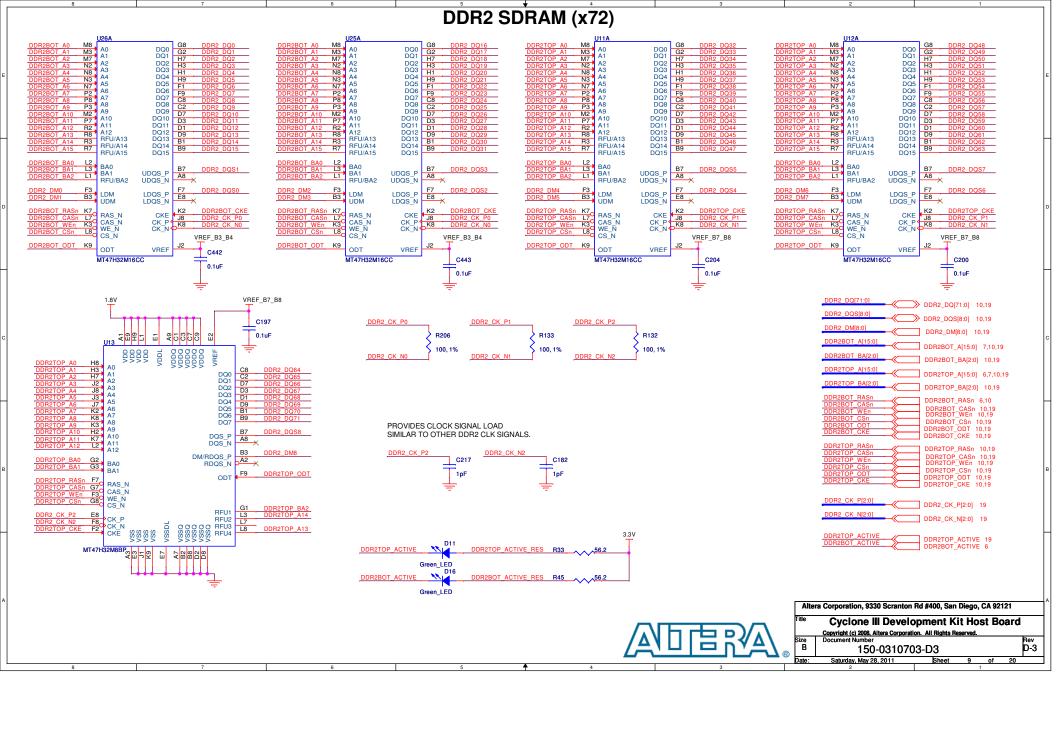


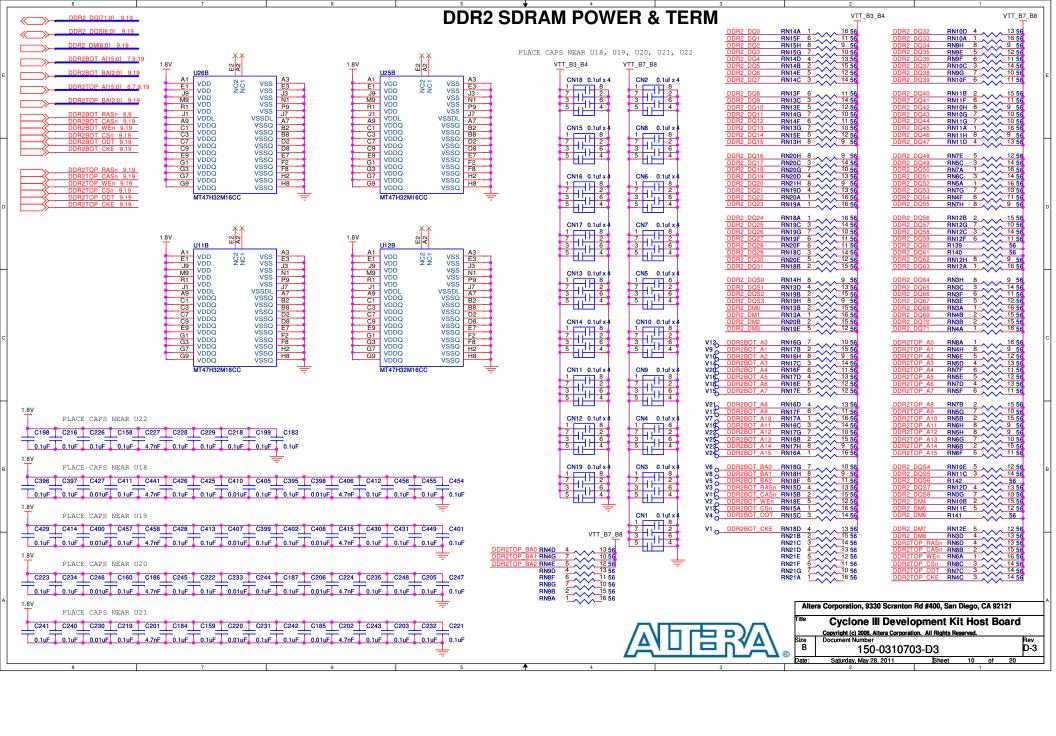


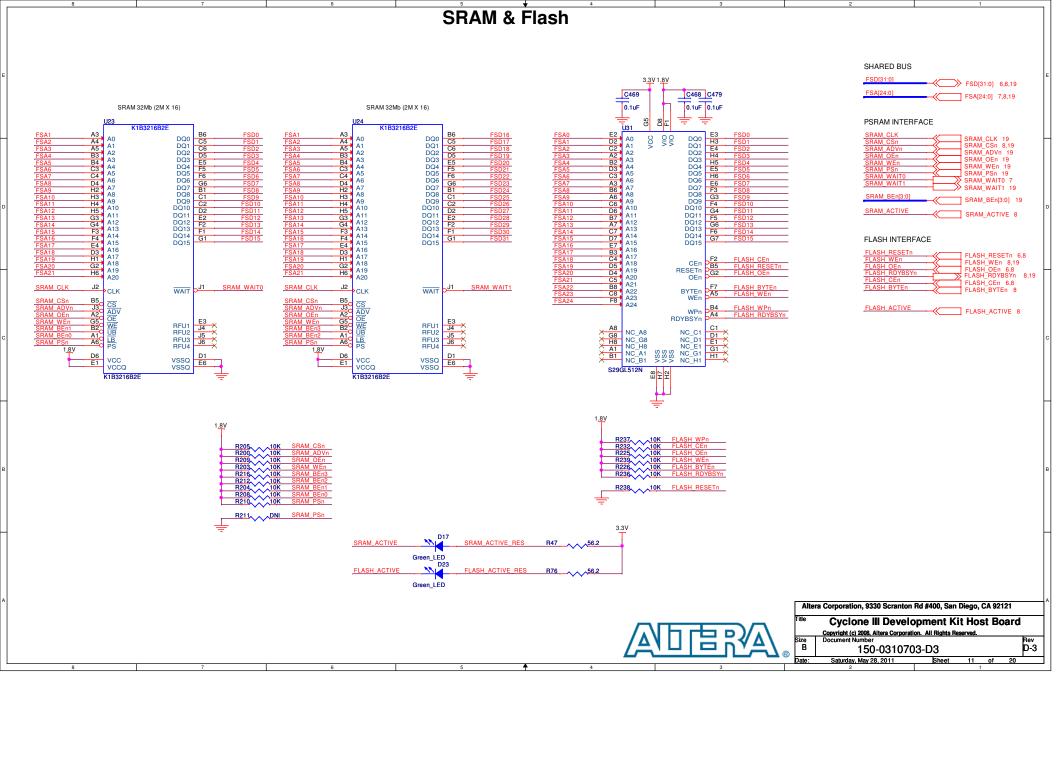


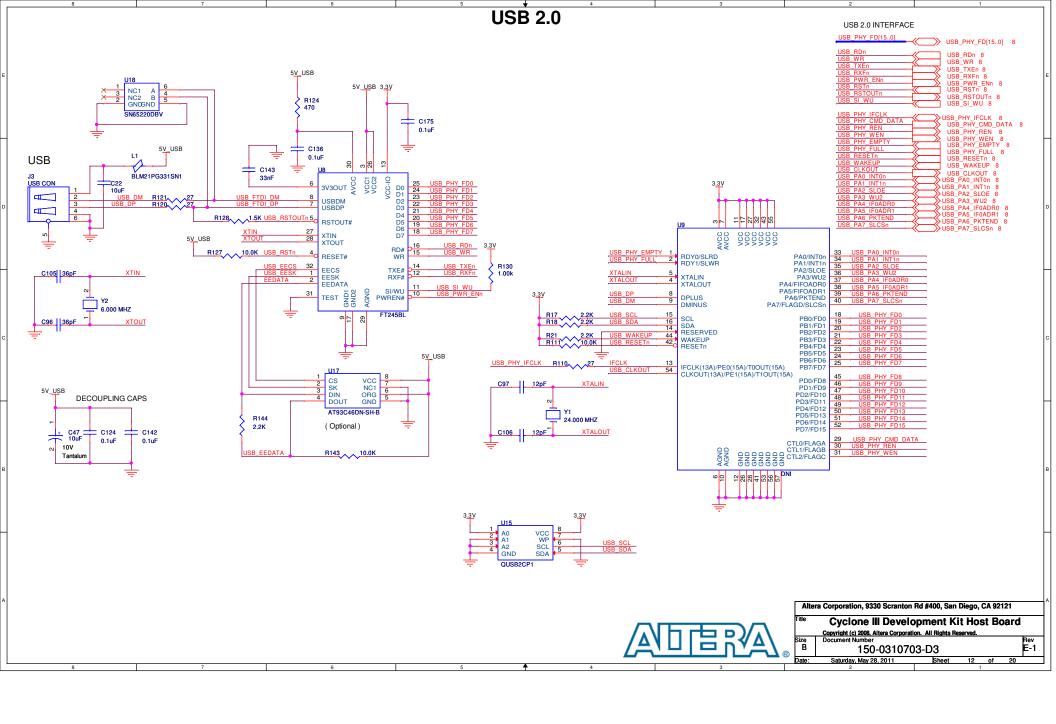


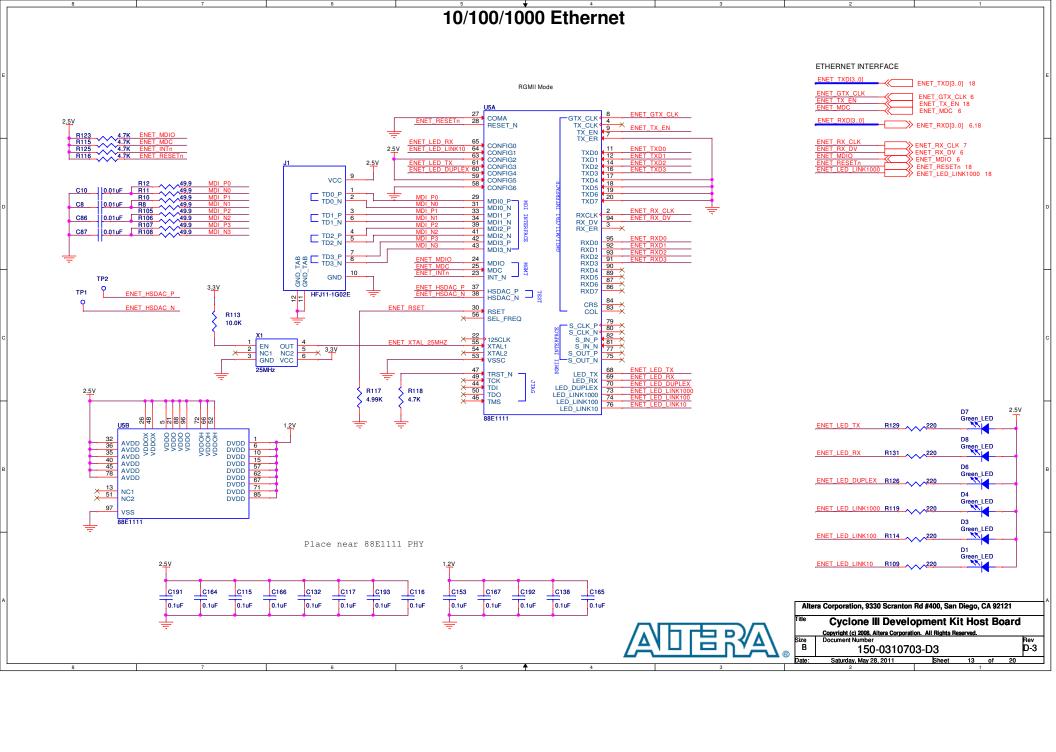


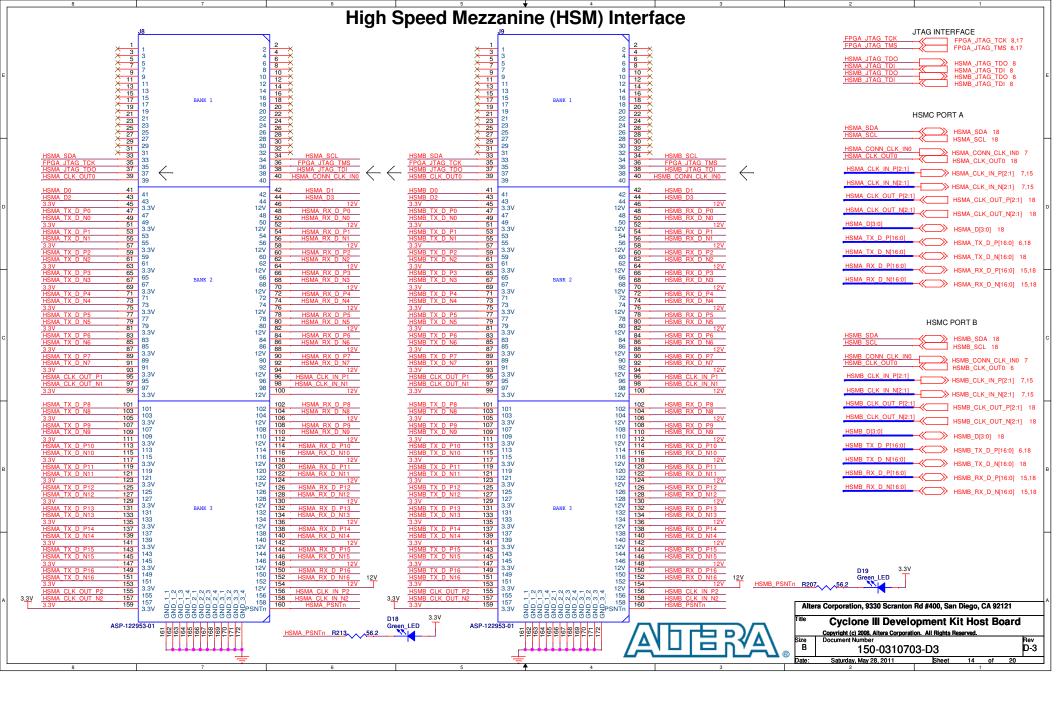














High Speed Mezzanine (HSM) Termination



