NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0310703-D1
Gerber Files	110-0310703-D1
PCB Design Files	120-0310703-D1
Assembly Drawing	130-0310703-D1
Fab Drawing	140-0310703-D1
Schematic Drawing	150-0310703-D3
PCB Film	160-0310703-D1
Bill of Materials	170-0310703-D1
Schematic Design Files	180-0310703-D1
Functional Specification	210-0310703-D1
PCB Layout Guidelines	220-0310703-D1
Assembly Rework	320-0310703-D1

2. 938 Parts, 61 Library Parts, 803 Nets, 4689 Pins

PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	C3 FPGA Package Top
3	Power 1
4	Power 2
5	Current Sense
6	Cyclone III Power
7	Cyclone III Clocks
8	MAX II
9	DDR2 SDRAM (x72)
10	DDR2 SDRAM POWER & TERM
11	SRAM & FLASH
12	USB 2.0
13	10/100/1000 Ethernet
14	HSM Connectors
15	HSM Termination
16	User IO & Connector
17	Cyclone III Configuration
18	Cyclone III Banks 1,2,5&6
19	Cyclone III Banks 3,4,7&8
20	Decoupling
21	
22	
23	
24	
25	
26	
27	

Cyclone III F780 Development Kit Host
Block Diagram

Digital Ground

Cyclone III FPGA Package Top

Notes:
1. FPGA Schematic Symbol Breakdown:
   - (A) Bank 1 - ENET,HSMA, LCD
   - (B) Bank 2 - ENET, HSMA, LCD
   - (C) Bank 3 - DDR2 SDRAM,FSA, HSMA (CLKIN), SRAM, USER I/O
   - (D) Bank 4 - DDR2 SDRAM, FLASH, FSA, SRAM, USER I/O
   - (E) Bank 5 - HSMB
   - (F) Bank 6 - HSMB, LCD, USB
   - (G) Bank 7 - DDR2 SDRAM, FSD, HSMB (CLKIN), MAX, USER I/O
   - (H) Bank 8 - DDR2 SDRAM, FSD, SRAM, USER I/O
   - (I) Some Clocks
   - (J) Configuration
   - (K) VCCINT, VCCA
   - (L) VCCIO, VREF
   - (M) Ground and NCs
   - (N) Ground
   - (O) Ground

I/O Bank	Usage	VCCIO Voltage	VREF Voltage
1	55 / 58 (95 %)	2.5V	--
2	59 / 63 (94 %)	2.5V	--
3	68 / 73 (93 %)	1.8V	0.9V
4	69 / 71 (97 %)	1.8V	0.9V
5	56 / 65 (86 %)	2.5V	--
6	50 / 58 (86 %)	2.5V	--
7	67 / 72 (93 %)	1.8V	0.9V
8	67 / 72 (93 %)	1.8V	0.9V

BANK 8
VCCIO = 1.8V

BANK 7
VCCIO = 1.8V

Cyclone III - EP3C120F780C7

BANK 1
VCCIO = 2.5V

BANK 2
VCCIO = 2.5V

BANK 6
VCCIO = 2.5V

BANK 5
VCCIO = 2.5V

BANK 3
VCCIO = 1.8V

BANK 4
VCCIO = 1.8V

Title: **Cyclone III Development Kit Host Board**

Size: B

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Power 1

14V-20V DC INPUT

DC_INPUT

J2
RAPC712X

D34
FM540

U1C
A1 VIN VIN B4
A2 VIN VIN B5
A3 VIN VIN B6
A4 VIN VIN C1
A5 VIN VIN C2
A6 VIN VIN C3
B1 VIN VIN C4
B2 VIN VIN C5
B3 VIN VIN C6
LTM4601

C19 150u
C4 10uF
C5 10uF

D2 20V Zener

DC_INPUT

R4 100K

SW2 EG2201A

RUN_SW

C89 47nF

C1 0.01uF

MPGM

R3 787K

U1D
A10 RUN   PGOOD G12
A7 INTVCC   VFB   F12
E12 DRVCC
A8 PLLIN   DIFFVOUT K12
A9 TRACK/SS VOUT_LCL L12
A11 COMP
A12 MPGM   VOSNS+ J12
C12 MARG0   FSET   B12
D12 MARG1   VOSNS- M12
LTM4601

3.3V
R9 1.00k

LTM_FB

R6 13.3K

R5 100K
FSET

C6 1000pF

C11 1000pF

POWER_GOOD 4,5

U1A
J1 VOUT VOUT L1
J2 VOUT VOUT L2
J3 VOUT VOUT L3
J4 VOUT VOUT L4
J5 VOUT VOUT L5
J6 VOUT VOUT L6
J7 VOUT VOUT L7
J8 VOUT VOUT L8
J9 VOUT VOUT L9
J10 VOUT VOUT L10
K1 VOUT VOUT L11
K2 VOUT VOUT M1
K3 VOUT VOUT M2
K4 VOUT VOUT M3
K5 VOUT VOUT M4
K6 VOUT VOUT M5
K7 VOUT VOUT M6
K8 VOUT VOUT M7
K9 VOUT VOUT M8
K10 VOUT VOUT M9
K11 VOUT VOUT M10
        VOUT M11
LTM4601

3.3V_OUT

C7 100pF
LTM_FB

C14 100uF
C15 100uF

C25 470uF 10V Tantalum

R13 .009

3.3V

PG_12V   PG_12V

U1B
D1 PGND PGND F8
D2 PGND PGND F9
D3 PGND PGND G1
D4 PGND PGND G2
D5 PGND PGND G3
D6 PGND PGND G4
E1 PGND PGND G5
E2 PGND PGND G6
E3 PGND PGND G7
E4 PGND PGND G8
E5 PGND PGND G9
E6 PGND PGND H1
E7 PGND PGND H2
F1 PGND PGND H3
F2 PGND PGND H4
F3 PGND PGND H5
F4 PGND PGND H6
F5 PGND PGND H7
F6 PGND PGND H8
F7 PGND PGND H9
         PGND H12
         SGND
LTM4601

DC_INPUT

POWER_GOOD

U10
5 RUN/SS BD   1
4 VIN   BOOST 2
9   SW   3
10 VC
6 RT   BIAS   7
  PG   FB   8
         GND   11
LT3481

R25 30.1K
PG_12V
R23 78.7K

12V
R22 10.0K PG_12V

C209 10uF
C30 330pF

C29 1000pF

C210 0.22uF

R26 845K
R27
100K

L3 10uH

D9 B520C-13

12V_OUT   12V
R134 .009

C35 22uF 25V Tantalum

12V

C237 4.7uF
PG_12V

U14
1 VIN VOUT 5
  ADJ/BYPASS 4
3 SHDN GND 2
LT1761

5.0V_OUT   5.0V
R28 .009

LT1761_ADJ R29 10.0K

R31 3.24K

C236 4.7uF

3.3V
R122 100, 1%

POWER LED

D5 Blue_Led

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Cyclone III Development Kit Host Board

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ALTERA

Power 2

POWER_GOOD   POWER_GOOD 3,5

U27 TPS51100DGQ

5.0V
C444 1uF
10 VIN
VLDOIN 2
VDDQSNS 1
C445 10uF
1.8V

0.9V VTT (3A Sink/Src)

VTT 3
VTTSNS 5
VTT_B3_B4

R53 10.0K 7 S3
R50 10.0K 9 S5
VREF_B3_B4 6 VTTREF
PGND 4 GND 8 GND 11

C451 0.1uF

C459 10uF C470 10uF C471 10uF C472 10uF C473 10uF C474 10uF

U6 TPS51100DGQ

5.0V
C150 1uF
10 VIN
VLDOIN 2
VDDQSNS 1
C149 10uF
1.8V

VTT 3
VTTSNS 5
VTT_B7_B8

R19 10.0K 7 S3
R20 10.0K 9 S5
VREF_B7_B8 6 VTTREF
PGND 4 GND 8 GND 11

C28 0.1uF

C207 10uF C131 10uF C130 10uF C129 10uF C257 10uF C128 10uF

U2 LTC3418

3.3V POWER_GOOD 7 RUN/SS
3 PVIN 4 PVIN 9 PVIN 10 PVIN 22 PVIN 23 PVIN 28 PVIN 29 PVIN 24 SVIN
C3 10uF C2 10uF C93 10uF C94 10uF

SW 1 SW 2 SW 11 SW 12 SW 20 SW 21 SW 30 SW 31

L2 0.2uH 1.8V_SW
R15 12.7K C16 1000pF C26 100uF C27 100uF R32 .009 1.8V
1.8V_OUT
1.8V_B3_B4
R44 .009

35 TRACK 27 SYNC/MODE   VFB 25 1.8V_VFB
R24 .009 1.8V_B7_B8

26 ITH 6 RT   VREF 16   PGOOD 5
R16 5.1K R7 30.1K
C9 2.2uF
R14 10.0K

8 SGND 13 PGND 14 PGND 15 PGND 17 PGND 18 PGND 19 PGND
PGND 32 PGND 33 PGND 34 PGND 36 PGND 37 PGND 38 GND 39

C17 2.2nF

U33 LT1963A

3.3V
8 IN   NC 4   OUT 1 2.5V_OUT
2.5V
R81 .009 Other 2.5V (non-FPGA)
R48 .009 CIII BANKS 1 & 2 2.5V_B1_B2
5 SHDNn   SENSE 2
C484 10uF POWER_GOOD
GND 7 GND 6 GND 3
R51 .009 CIII BANKS 5 & 6 2.5V_B5_B6
R80 .009 CIII PLL ANALOG POWER 2.5V_VCCA
C486 10uF

CIII PLL DIGITAL POWER

U21 LT1963A

3.3V
8 IN   NC 4   OUT 1 1.2V_PLL
R43 .009 1.2V_VCCD
5 SHDNn   SENSE 2
C51 10uF POWER_GOOD
GND 7 GND 6 GND 3

U29 LTC3418

3.3V POWER_GOOD 7 RUN/SS
3 PVIN 4 PVIN 9 PVIN 10 PVIN 22 PVIN 23 PVIN 28 PVIN 29 PVIN 24 SVIN
C69 10uF C68 10uF C476 10uF C475 10uF

SW 1 SW 2 SW 11 SW 12 SW 20 SW 21 SW 30 SW 31

L6 0.2uH
R58 5.1K C66 1000pF C419 100uF C418 100uF R49 .009 1.2V_INT
1.2V_OUT
R46 .009 1.2V

35 TRACK 27 SYNC/MODE   VFB 25 1.2V_VFB

26 ITH 6 RT   VREF 16   PGOOD 5
R57 5.1K R68 30.1K
C67 2.2uF
R59 10.0K

13 SGND 14 PGND 15 PGND 17 PGND 18 PGND 19 PGND
PGND 32 PGND 33 PGND 34 PGND 36 PGND 37 PGND 38 GND 39

C64 2.2nF

12V
Short 12V to old -12V rail for new positive bias voltage LCD

L8 DNI C498 DNI L9 DNI
C500 10uF +12SW -12SW 12V
U38
4 VIN SW1 1
5 SHDN GND 2 NFB 3
DNI
D35 DNI
-12FB
C490 DNI
R240 80.6K R241 10.0K
R242 8.06K C497 10uF
V5 9.3V R92 DNI R1001 3.01K C77 0.1uF
V4 1.0V R91 3.32K C76 0.1uF
V3 2.1V R90 15.4K C75 0.1uF
V2 7.3V R89 2.94K C74 0.1uF
V1 8.3V R88 DNI C73 0.1uF
2.5V
R1000 2.94K

Above power circuit was reworked to support a new graphics LCD with +12V bias voltages, not the original -12V voltages.
FOR USE WITH NEW LCDF-55472 Series ONLY (old -12V circuit for use only with F-51852 Series ONLY)

R93 100 RED J12
BLACK **HDR2X1**
Graphics LCD Backlight Power Header (Hook black wire to pin 2)

Title: **Cyclone III Development Kit Host Board**

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Current Sense

Current Sense A/D

U35 ANALOG MUX

3.3V			3.0V_CSENSE

U34
VIN VOUT 5
ADJ/BYPASS 3.0V_ADJUST R83 10.0K
SHDN GND
LT1761

C70 4.7uF
POWER_GOOD
R82 6.81K
C71 4.7uF

Place (1) 0.1uF near VDD of ADG725.
Place (1) 0.1uF and (1) 1.0uF near V+ of INA271
Place (1) 0.1uF and (1) 1.0uF near V+ of AD7940

U35 ADG725

3.0V_CSENSE

13 VDD			
14 VDD			
12 S1A	S9A 4	1.2V_OUT / 1.2V_INT	1.8V_OUT / 1.8V
25 S1B	S9B 33		
11 S2A	S10A 3	1.2V_PLL / 1.2V_VCCD	2.5V_OUT / 2.5V
26 S2B	S10B 34		
10 S3A	S11A 2	2.5V_OUT / 2.5V_VCCA	3.3V_OUT_LEVEL_SHIFT / 3.3V_LEVEL_SHIFT
27 S3B	S11B 35		
9 S4A	S12A 1	1.8V_OUT / 1.8V_B3_B4	5.0V_OUT_LEVEL_SHIFT / 5.0V_LEVEL_SHIFT
28 S4B	S12B 36		
8 S5A	S13A 48	1.8V_OUT / 1.8V_B7_B8	12V_OUT_LEVEL_SHIFT / 12V_LEVEL_SHIFT
29 S5B	S13B 37		
7 S6A	S14A 47	2.5V_OUT / 2.5V_B1_B2	SPEAKER
30 S6B	S14B 38		
6 S7A	S15A 46	2.5V_OUT / 2.5V_B5_B6	
31 S7B	S15B 39		
5 S8A	S16A 45	1.2V_OUT / 1.2V	
32 S8B	S16B 40		
18 DIN	DA 43	PMON_DATA	CS_DA
19 SCLK	DB 41	PMON_CLK	CS_DB
17 SYNC	NC1 15	PMON_SYNC	
	NC2 16		
	NC3 20		
	NC4 21		
	NC5 22		
23 GND	NC6 42		
24 VSS	NC7 44		

CS_FB

R227 DNI   R228 DNI

U37 DNI
1 OUTA   V+ 5
2 V-
3 INA+   INA- 4
3.0V_CSENSE

R84 0   C478 DNI

U36 DNI
IN- IN+ 8
1 GND NC 7
2 PREOUT V+ 6
3 BUFIN OUT 5
4

R85 DNI
C79 DNI   C78 DNI

CS_DA
CS_DB

3.0V_CSENSE

C72 1.0uF C499 0.1uF C80 1.0uF C481 0.1uF C81 0.1uF

3.0V_CSENSE

U32
1 VCC   Fo 10
2 FSset SCK 9
3 CH1 SDO 8
4 CH0 CSn 7
CS_DB 4 ZSset GND 6
LTC2402

PMON_CLK
PMON_SDI
PMON_CSn

PMON_DATA
PMON_SYNC

3.3V
R72 10.0K
R69 10.0K
R71 10.0K
R70 10.0K
R96 10.0K

CS_FB

CURRENT SENSE INTERFACE

PMON_DATA → PMON_DATA 8
PMON_CLK → PMON_CLK 8
PMON_CSN → PMON_CSN 8
PMON_SYNC → PMON_SYNC 8
PMON_SDI → PMON_SDI 8

SPEAKER → SPEAKER 16

POWER DISPLAY INTERFACE

PWR_DIG_SEL[4:1] → PWR_DIG_SEL[4:1] 8
PWR_SEG_A → PWR_SEG_A 8
PWR_SEG_B → PWR_SEG_B 8
PWR_SEG_C → PWR_SEG_C 8
PWR_SEG_D → PWR_SEG_D 8
PWR_SEG_E → PWR_SEG_E 8
PWR_SEG_F → PWR_SEG_F 8
PWR_SEG_G → PWR_SEG_G 8
PWR_SEG_DP → PWR_SEG_DP 8
PWR_SEG_MINUS → PWR_SEG_MINUS 8

PWR_SEL[3:0] → PWR_SEL[3:0] 8

PG_12V → PG_12V 3
POWER_GOOD → POWER_GOOD 3,4

Power Display (level shift resistor dividers)

3.3V_OUT	3.3V	5.0V_OUT	5.0V	12V_OUT	12V
R100 1.2K	R87 1.2K	R199 910	R198 910	R215 2.1K	R214 2.1K
3.3V_OUT_LEVEL_SHIFT	3.3V_LEVEL_SHIFT	5.0V_OUT_LEVEL_SHIFT	5.0V_LEVEL_SHIFT	12V_OUT_LEVEL_SHIFT	12V_LEVEL_SHIFT
R99 1.0K	R86 1.0K	R202 390	R201 390	R218 300	R217 300

POWER DISPLAY

U28 QUAD_7SEG_M2212RI

PWR_DIG_SEL1 1 DIGIT1
PWR_DIG_SEL2 10 DIGIT2
PWR_DIG_SEL3 4 DIGIT3
PWR_DIG_SEL4 6 DIGIT4

an 14   ca 13
A 12 B 11 C 3 D 8 E 2 F 9 G 7 DP 5

2.5V

PWR_SEG_MINUS	R65 220	SEG_LED_MINUS
PWR_SEG_A	R64 220	SEG_LED_A
PWR_SEG_B	R63 220	SEG_LED_B
PWR_SEG_C	R74 220	SEG_LED_C
PWR_SEG_D	R66 220	SEG_LED_D
PWR_SEG_E	R73 220	SEG_LED_E
PWR_SEG_F	R67 220	SEG_LED_F
PWR_SEG_G	R52 220	SEG_LED_G
PWR_SEG_DP	R75 220	SEG_LED_DP

SW4 94HCB16WT

2.5V
R223 1.00k PWR_SEL1 2 P2 P4 4 PWR_SEL2 R222 1.00k
C2 C1
R234 1.00k PWR_SEL3 8 P8 P1 1 PWR_SEL0 R233 1.00k
2.5V

Cyclone III Power

HSMC PORT A
HSMA_TX_D_P[16:0] → HSMA_TX_D_P[16:0] 14,18

HSMC PORT B
HSMB_D[3:0] → HSMB_D[3:0] 14,18
HSMB_TX_D_P[16:0] → HSMB_TX_D_P[16:0] 14,18
HSMB_CLK_OUT0 → HSMB_CLK_OUT0 14

ETHERNET INTERFACE
ENET_RXD[3..0] → ENET_RXD[3..0] 13,18
ENET_MDIO → ENET_MDIO 13
ENET_RX_DV → ENET_RX_DV 13
ENET_GTX_CLK → ENET_GTX_CLK 13
ENET_MDC → ENET_MDC 13

DDR2 INTERFACE
DDR2TOP_A[15:0] → DDR2TOP_A[15:0] 7,9,10,19
DDR2BOT_RASn → DDR2BOT_RASn 9,10
DDR2BOT_ACTIVE → DDR2BOT_ACTIVE 9

SHARED BUS
FSD[31:0] → FSD[31:0] 8,11,19

USB 2.0 INTERFACE
USB_FD[7:0] → USB_FD[7:0] 8,18

OLED DISPLAY INTERFACE
LCD_DATA[7:0] → LCD_DATA[7:0] 16,18
LCD_RSTn → LCD_RSTn 16

FLASH INTERFACE
FLASH_CEn → FLASH_CEn 8,11
FLASH_OEn → FLASH_OEn 8,11
FLASH_RESETn → FLASH_RESETn 8,11

USER I/O's
USER_PB[3:0] → USER_PB[3:0] 16,19

U20K — Cyclone III (EP3C120F780)

GND / GNDA pin bank

U20I — Cyclone III, Power
EP3C120 (EP3C80/EP3C55/EP3C40)
VCCINT
EP3C120F780

U20J — Cyclone III, IO Power
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

PLACE NEAR CIII

VREF_B3_B4
C351 0.1uF C363 0.1uF C378 0.1uF

VREF_B7_B8
C265 0.1uF C283 0.1uF C277 0.1uF

TP5 TP6 TP4 TP3

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Cyclone III Clocks

1.8V

L5
BLM15AG221SN1

CLKIN_50_EN

Y5
1 EN VCC 4   1.8V_50M_OSC
2 GND OUT 3   CLKIN_50
50MHz

C37
0.01uF

C43
0.01uF

C46
4.7uF

1.8V

L4
BLM15AG221SN1

CLKIN_125_EN

Y4
1 EN VCC 4   1.8V_125M_OSC
2 GND OUT 3   CLKIN_125
125MHz

C36
0.01uF

C42
0.01uF

C45
4.7uF

SMA Connector
(external clock source)

J10
1 CLKIN_SMA

R194
49.9

J11
1 CLKOUT_SMA

U20L
Cyclone III, Clocks

HSMA_CLK_IN_P2	J2	CLK0/DIFFCLK_0p
HSMA_CLK_IN_N2	J1	CLK1/DIFFCLK_0n	Bank 1
HSMA_CLK_IN_P1	Y2	CLK2_DIFFCLK_1p
HSMA_CLK_IN_N1	Y1	CLK3/DIFFCLK_1n	Bank 2
HSMB_CLK_IN_P1	J27	CLK4/DIFFCLK_2p
HSMB_CLK_IN_N1	J28	CLK5/DIFFCLK_2n	Bank 6
HSMB_CLK_IN_P2	Y27	CLK6/DIFFCLK_3p
HSMB_CLK_IN_N2	Y28	CLK7/DIFFCLK_3n	Bank 5
USB_IFCLK	B15	CLK9/DIFFCLK_5p
HSMB_CLK_IN0	A15	CLK8/DIFFCLK_5n	Bank 7
ENET_RX_CLK	B14	CLK11/DIFFCLK_4p
CLKIN_125	A14	CLK10/DIFFCLK_4n	Bank 8
SRAM_WAIT0	AG15	CLK13/DIFFCLK_7p
CLKIN_50	AH15	CLK12/DIFFCLK_7n	Bank 4
HSMA_CLK_IN0	AG14	CLK15/DIFFCLK_6p
CLKIN_SMA	AH14	CLK14/DIFFCLK_6n	Bank 3

Bank   DIFFIO_B57p(NC/NC/x)
       DIFFIO_B35p(x/x/IO)

Bank 7   PLL2_CLKOUTp
         DIFFIO_T55p

Bank 8   PLL3_CLKOUTp
         PLL3_CLKOUTn

Bank 4   PLL4_CLKOUTp
         PLL4_CLKOUTn

AB22 DDR2BOT_A0
AA16 DDR2BOT_A15
D23   MAX_CSn
D24   DDR2TOP_A3
D5   SEVEN_SEG_F
C5   SEVEN_SEG_SEL2
AE23 CLKOUT_SMA
AF23 FSA18

EP3C120F780

Place near level translator for HSMA_CLK_IN0.

3.3V   1.8V
U22
1 VCC1VCC2 5
HSMA_CONN_CLK_IN0 2 A   Y 4   HSMA_CLK_IN0
3 GND
FXLP34

3.3V 1.8V
C49   C50
0.1uF 0.1uF

Limited to 100MHz

Place near level translator for HSMB_CLK_IN0.

3.3V   1.8V
U19
1 VCC1VCC2 5
HSMB_CONN_CLK_IN0 2 A   Y 4   HSMB_CLK_IN0
3 GND
FXLP34

3.3V 1.8V
C57   C58
0.1uF 0.1uF

Limited to 100MHz

MAX_CSn   MAX_CSn 8

HSMC PORT A
HSMA_CLK_IN_P[2:1]   HSMA_CLK_IN_P[2:1] 14,15
HSMA_CLK_IN_N[2:1]   HSMA_CLK_IN_N[2:1] 14,15
HSMA_CONN_CLK_IN0   HSMA_CONN_CLK_IN0 14

HSMC PORT B
HSMB_CLK_IN_P[2:1]   HSMB_CLK_IN_P[2:1] 14,15
HSMB_CLK_IN_N[2:1]   HSMB_CLK_IN_N[2:1] 14,15
HSMB_CONN_CLK_IN0   HSMB_CONN_CLK_IN0 14

SHARED BUS
FSA[24:0]   FSA[24:0] 8,11,19

SEVEN-SEG DISPLAY
SEVEN_SEG_SEL[4:1]   SEVEN_SEG_SEL[4:1] 16,19
SEVEN_SEG_F   SEVEN_SEG_F 16

USB 2.0 INTERFACE
USB_IFCLK   USB_IFCLK 8

OSCILLATOR CONTROL
CLKIN_50_EN   CLKIN_50_EN 8
CLKIN_125_EN   CLKIN_125_EN 8

ETHERNET INTERFACE
ENET_RX_CLK   ENET_RX_CLK 13

DDR2 INTERFACE
DDR2BOT_A[15:0]   DDR2BOT_A[15:0] 9,10,19
DDR2TOP_A[15:0]   DDR2TOP_A[15:0] 6,9,10,19

PSRAM INTERFACE
SRAM_WAIT0   SRAM_WAIT0 11

Title
Cyclone III Development Kit Host Board

Size B
Document Number
150-0310703-D3
Rev D-3

MAX II

U7A — MAX II BANK1 (EPM2210_F256FBGA)

Net	Pin		Pin	Net
FPGA_DATA	D3	IOB1_1		
FPGA_DCLK	C2	IOB1_2		
FPGA_CONF_DONE	E3	IOB1_3		
FPGA_nSTATUS	C3	IOB1_4		
FPGA_nCONFIG	E4	IOB1_5		
PWR_SEG_A	D2	IOB1_6		
PWR_SEG_B	E5	IOB1_7		
PWR_SEG_C	D1	IOB1_8		
PWR_SEG_D	F3	IOB1_9		
PWR_SEG_E	E2	IOB1_10		
PWR_SEG_F	F4	IOB1_11		
PWR_SEG_G	E1	IOB1_12		
PWR_SEG_DP	F5	IOB1_13		
PWR_SEG_MINUS	F2	IOB1_14		
PWR_DIG_SEL1	F6	IOB1_15		
PWR_DIG_SEL2	F1	IOB1_16		
PWR_DIG_SEL3	G3	IOB1_17		
PWR_DIG_SEL4	G2	IOB1_18		
PWR_SEL0	G4	IOB1_19		
PWR_SEL1	G1	IOB1_20		
PWR_SEL2	G5	IOB1_21		
PWR_SEL3	H2	IOB1_22		
HSMB_JTAG_TDI	H1	IOB1_24		
PMON_SYNC	H5	IOB1/GCLK0		
MAX_EMB	J5	IOB1/GCLK1		

Pin	Port	Net
H3	IOB1_25	PMON_DATA
J1	IOB1_26	PMON_CLK
H4	IOB1_27	PMON_CSN
J2	IOB1_28	PMON_SDI
J4	IOB1_29	MAX_ERROR
K1	IOB1_30	MAX_LOAD
J3	IOB1_31	MAX_FACTORY
K2	IOB1_32	MAX_USER
L1	IOB1_34	USB_PA5_IF0ADR1
K5	IOB1_35	USB_PA6_PKTEND
L2	IOB1_36	USB_PA7_SLCSn
K4	IOB1_37	HSMA_JTAG_TDO
M1	IOB1_38	MAXGP_JTAG_TCK
K3	IOB1_39	USB_TXEn
M2	IOB1_40	MAXGP_JTAG_TMS
L5	IOB1_41	MAXGP_JTAG_TDO
M3	IOB1_42	USB_WEN
L4	IOB1_43	MAXGP_JTAG_TDI
N1	IOB1_44	FPGA_JTAG_TCK
L3	IOB1_45	USB_PA4_IF0ADR0
N2	IOB1_46	FPGA_JTAG_TDO
M4	IOB1_47	HSMA_JTAG_TDI
N3	IOB1_48	FPGA_JTAG_TCK
P2	IOB1_49	FPGA_JTAG_TMS
P3	TCK	MAX_JTAG_TCK
L6	TDI	MAX_JTAG_TDI
M5	TDO	MAX_JTAG_TDO
N4	TMS	MAX_JTAG_TMS

U7B — MAX II BANK2 (EPM2210_F256FBGA)

Pin	Port		Net	Pin	Port
H3	IOB2_50	USB_PHY_FD0	C13	IOB2_74	
	IOB2_51	USB_PHY_FD1	B16	IOB2_75	
	IOB2_52	USB_PHY_FD2	C12	IOB2_76	
	IOB2_53	USB_PHY_FD3	A15	IOB2_77	
	IOB2_54	USB_PHY_FD4	D12	IOB2_78	
	IOB2_55	USB_PHY_FD5	B14	IOB2_79	
	IOB2_56	USB_PHY_FD6	C11	IOB2_80	
	IOB2_57	USB_PHY_FD7	B13	IOB2_81	
	IOB2_58	USB_PHY_FD8	D11	IOB2_82	
	IOB2_59	USB_PHY_FD9	A13	IOB2_83	
	IOB2_60	USB_PHY_FD10	E11	IOB2_85	
	IOB2_61	USB_PHY_FD11	B12	IOB2_86	
	IOB2_62	USB_PHY_FD12	C10	IOB2_87	
	IOB2_63	USB_PHY_FD13	A12	IOB2_88	
	IOB2_64	USB_PHY_FD14	D10	IOB2_89	
	IOB2_65	USB_PHY_FD15	B11		
	IOB2_66	USB_CMD_DATA	E10	IOB2_90	
	IOB2_67	USB_WEN	A11	IOB2_91	
		USB_REN		IOB2_92	
	IOB2_69	USB_EMPTY	B10	IOB2_93	
	IOB2_70	USB_FULL	C9	IOB2_94	
	IOB2_71	FACTORY_CONFIGn	A10	IOB2_95	
	IOB2_72	LCD_BS1	D9	IOB2_96	
	IOB2_73	HSMB_JTAG_TDO	B9	IOB2_97	
				IOB2_98	
				IOB2_99	
				IOB2_100	USB_PA0_INT0n A2
				IOB2_101	USB_PA1_INT1n B1
				IOB2_102	USB_PA2_SLOE D4

USB_FD0 E9 / USB_FD1 A9 / USB_FD2 A8 / USB_FD3 B8 / USB_FD4 E8 / USB_FD5 A7 / USB_FD6 D8 / USB_FD7 B7 / USB_RDn C8 / USB_WR A6 / USB_RXFn B6 / USB_PWR_ENn E7 / USB_RSTn A5 / USB_RSTOUTn D7 / USB_SI_WU B5 / USB_PHY_IFCLK C7 / USB_PHY_CMD_DATA C6 / USB_PHY_REN E6 / USB_PHY_EMPTY D6 / USB_PHY_WEN C4 / USB_RESETn C6 / USB_CLKOUT B3 / USB_WAKEUP C5 / USB_PA0_INT0n A2 / USB_PA1_INT1n B1 / USB_PA2_SLOE B1 / USB_PA3_WU2 D4

U7C — MAX II BANK3 (EPM2210_F256FBGA)

Pin	Port		Net	Pin
	IOB3_103	FPGA_BYPASS	J16	IOB3_127
	IOB3_104	HSMA_BYPASS	J13	IOB3_128
	IOB3_105	HSMB_BYPASS	H16	IOB3_129
	IOB3_106	PGM0	H13	IOB3_130
	IOB3_107	PGM1	H15	IOB3_131
	IOB3_108	PGM2	H14	IOB3_132
	IOB3_109	PGM3	G16	IOB3_133
	IOB3_110		G12	IOB3_134
	IOB3_111	LCD_SERn N16		IOB3_135
	IOB3_112		L13	
	IOB3_113	FLASH_RESETn M15		IOB3_137
	IOB3_114	FLASH_WEn L12		IOB3_138
	IOB3_115	FLASH_OEn M16		IOB3_139
	IOB3_116	FLASH_RDYBSYn L11		IOB3_140
	IOB3_117	FLASH_BYTEn L15		IOB3_141
	IOB3_118	FLASH_CEn K14		IOB3_142
	IOB3_119	MAX_CSn L16		IOB3_143
	IOB3_120	MAX_OEn K13		IOB3_144
	IOB3_121	MAX_WEn K15		IOB3_145
	IOB3_122		K12	IOB3_146
	IOB3_123	FSA6 K16		IOB3_147
	IOB3_125	FSD18 J15		IOB3_148
	IOB3_126	USB_IFCLK J14		IOB3_149
				IOB3_150
	IOB3_151	CLKIN_50_EN C15		IOB3_152
	IOB3_153	CLKIN_125_EN E13		IOB3_154
	IOB3_155		E14	

MAX_RESERVE1 P14 / MWATTS_MAMPS N13 / VOLTS_WATTS P15 / MAX_RESERVE0 M14 / MAX_DIP0 N14 / MAX_DIP1 M13 / MAX_DIP2 N15 / MAX_DIP3 L14
CLKIN_24 J12 / MAX2_CLK H12 / IOB3/GLCK2 / IOB3/GLCK3

U7D — MAX II BANK4 (EPM2210_F256FBGA)

Net	Pin	Port		Pin	Port	Net
FSD0	P4	IOB4_156		N9	IOB4_180	FSA0
FSD2	P5	IOB4_157		T8	IOB4_181	FSA1
FSD3	T2	IOB4_158		T9	IOB4_182	FSA2
FSD4	N5	IOB4_159		P9	IOB4_183	FSA3
FSD5	R3	IOB4_160		T10	IOB4_184	FSA4
FSD6	P6	IOB4_161			IOB4_185	FSA5
FSD7	R4	IOB4_162		R10		FSA7
		IOB4_163				
FSD8	N6	IOB4_164		M10	IOB4_188	FSA8
FSD9	T4	IOB4_165		T11	IOB4_189	FSA9
FSD10	M6	IOB4_166		N10	IOB4_190	FSA10
FSD11	R5	IOB4_167		R11	IOB4_191	FSA11
FSD12	P7	IOB4_168		P10	IOB4_192	FSA12
FSD13	T5	IOB4_169		T12	IOB4_193	FSA13
FSD14	N7	IOB4_170		M11	IOB4_194	FSA14
FSD15	R6	IOB4_171		R12	IOB4_195	FSA15
FSD16	M7	IOB4_172		N11	IOB4_196	FSA16
FSD17	T6	IOB4_173		T13	IOB4_197	FSA17
FSD24	F12			P11	IOB4_198	FSA18
FSD25	D16			R9	IOB4_199	FSA19
FSD26	F13			P8	IOB4_200	FSA20
FSD27	D15			M12	IOB4_201	FSA21
FSD28	F14			N12	IOB4_202	FSA22
FSD29	D14			T15	IOB4_203	FSA23
FSD30	E12					
FSD31	C15			M8	IOB4_204	FSA24
CLKIN_50_EN	E13			R16	IOB4_205	RESET_CONFIGn
CLKIN_125_EN	C14			P13	IOB4_206	
CPU_RESETn	M9					
MAX_EN	M8					

IOB4/DEV_CLRn / IOB4/DEV_OE

USB Blaster Clock

Y3 — 1.8V_24M_OSC, 24MHz
- EN / VCC / GND / OUT
- CLKIN_24
- C38 0.01uF / C34 0.01uF / C239 4.7uF
- L7 BLM15AG221SN1, 1.8V

FPGA JTAG INTERFACE
FPGA_JTAG_TCK → FPGA_JTAG_TCK 14,17
FPGA_JTAG_TMS → FPGA_JTAG_TMS 14,17
FPGA_JTAG_TDO → FPGA_JTAG_TDO 17
FPGA_JTAG_TDI → FPGA_JTAG_TDI 17

MAXII JTAG INTERFACE
MAX_JTAG_TCK → MAX_JTAG_TCK 17
MAX_JTAG_TMS → MAX_JTAG_TMS 17
MAX_JTAG_TDO → MAX_JTAG_TDO 17
MAX_JTAG_TDI → MAX_JTAG_TDI 17

MAXII GPIO JTAG
MAXGP_JTAG_TCK → MAXGP_JTAG_TCK 17
MAXGP_JTAG_TMS → MAXGP_JTAG_TMS 17
MAXGP_JTAG_TDO → MAXGP_JTAG_TDO 17
MAXGP_JTAG_TDI → MAXGP_JTAG_TDI 17
HSMA_JTAG_TDO → HSMA_JTAG_TDO 14
HSMA_JTAG_TDI → HSMA_JTAG_TDI 14
HSMB_JTAG_TDO → HSMB_JTAG_TDO 14
HSMB_JTAG_TDI → HSMB_JTAG_TDI 14

C3 OSCILLATOR CONTROL
CLKIN_50_EN → CLKIN_50_EN 7
CLKIN_125_EN → CLKIN_125_EN 7

MEMORY ACTIVITY LEDs
SRAM_ACTIVE → SRAM_ACTIVE 11
FLASH_ACTIVE → FLASH_ACTIVE 11
SRAM_CSn → SRAM_CSn 11,19

LCD INTERFACE CONTROL
LCD_SERn → LCD_SERn 16
LCD_BS1 → LCD_BS1 16

FSM BUS
FSD[31:0] → FSD[31:0] 6,11,19
FSA[24:0] → FSA[24:0] 7,11,19

CONFIGURATION INTERFACE
MAX_ERROR → MAX_ERROR 16
MAX_LOAD → MAX_LOAD 16
MAX_FACTORY → MAX_FACTORY 16
MAX_USER → MAX_USER 16
MAX_EMB → MAX_EMB 16
RESET_CONFIGn → RESET_CONFIGn 16
CPU_RESETn → CPU_RESETn 16,18
FACTORY_CONFIGn → FACTORY_CONFIGn 16
PGM[3:0] → PGM[3:0] 16
FPGA_DATA → FPGA_DATA 17
FPGA_DCLK → FPGA_DCLK 17
FPGA_CONF_DONE → FPGA_CONF_DONE 16,17
FPGA_nSTATUS → FPGA_nSTATUS 17
FPGA_nCONFIG → FPGA_nCONFIG 17

PMON
PMON_DATA → PMON_DATA 5
PMON_CLK → PMON_CLK 5
PMON_SYNC → PMON_SYNC 5
PMON_CSN → PMON_CSN 5
PMON_SDI → PMON_SDI 5

USB TO C3 INTERFACE
USB_FD[7:0] → USB_FD[7:0] 6,18
USB_IFCLK → USB_IFCLK 7
USB_CMD_DATA → USB_CMD_DATA 18
USB_REN → USB_REN 18
USB_WEN → USB_WEN 18
USB_EMPTY → USB_EMPTY 18
USB_FULL → USB_FULL 18

FLASH INTERFACE
FLASH_RESETn → FLASH_RESETn 6,11
FLASH_WEn → FLASH_WEn 11,19
FLASH_OEn → FLASH_OEn 6,11
FLASH_RDYBSYn → FLASH_RDYBSYn 11,19
FLASH_BYTEn → FLASH_BYTEn 11
FLASH_CEn → FLASH_CEn 6,11
MAX_CSn → MAX_CSn 7
MAX_OEn → MAX_OEn 19
MAX_WEn → MAX_WEn 19
MAX2_CLK → MAX2_CLK 19

JTAG CONTROL
FPGA_BYPASS → FPGA_BYPASS 16
HSMA_BYPASS → HSMA_BYPASS 16
HSMB_BYPASS → HSMB_BYPASS 16
MAX_EN → MAX_EN 16
JTAG_SEL → JTAG_SEL 17
DEV_SEL → DEV_SEL 17

MAX II DIPSWITCH
MWATTS_MAMPS → MWATTS_MAMPS 16
VOLTS_WATTS → VOLTS_WATTS 16
MAX_RESERVE0 → MAX_RESERVE0 16
MAX_RESERVE1 → MAX_RESERVE1 16
MAX_DIP[3:0] → MAX_DIP[3:0] 16

USB 2.0 INTERFACE
USB_PHY_FD[15:0] → USB_PHY_FD[15..0] 12
USB_RDn → USB_RDn 12
USB_WR → USB_WR 12
USB_TXEn → USB_TXEn 12
USB_RXFn → USB_RXFn 12
USB_PWR_ENn → USB_PWR_ENn 12
USB_RSTn → USB_RSTn 12
USB_RSTOUTn → USB_RSTOUTn 12
USB_SI_WU → USB_SI_WU 12
USB_PHY_IFCLK → USB_PHY_IFCLK 12
USB_PHY_CMD_DATA → USB_PHY_CMD_DATA 12
USB_PHY_REN → USB_PHY_REN 12
USB_PHY_WEN → USB_PHY_WEN 12
USB_PHY_EMPTY → USB_PHY_EMPTY 12
USB_PHY_FULL → USB_PHY_FULL 12
USB_RESETn → USB_RESETn 12
USB_WAKEUP → USB_WAKEUP 12
USB_CLKOUT → USB_CLKOUT 12
USB_PA0_INT0n → USB_PA0_INT0n 12
USB_PA1_INT1n → USB_PA1_INT1n 12
USB_PA2_SLOE → USB_PA2_SLOE 12
USB_PA3_WU2 → USB_PA3_WU2 12
USB_PA4_IF0ADR0 → USB_PA4_IF0ADR0 12
USB_PA5_IF0ADR1 → USB_PA5_IF0ADR1 12
USB_PA6_PKTEND → USB_PA6_PKTEND 12
USB_PA7_SLCSn → USB_PA7_SLCSn 12

POWER DISPLAY
PWR_DIG_SEL[4:1] → PWR_DIG_SEL[4:1] 5
PWR_SEG_A → PWR_SEG_A 5
PWR_SEG_B → PWR_SEG_B 5
PWR_SEG_C → PWR_SEG_C 5
PWR_SEG_D → PWR_SEG_D 5
PWR_SEG_E → PWR_SEG_E 5
PWR_SEG_F → PWR_SEG_F 5
PWR_SEG_G → PWR_SEG_G 5
PWR_SEG_DP → PWR_SEG_DP 5
PWR_SEG_MINUS → PWR_SEG_MINUS 5
PWR_SEL[3:0] → PWR_SEL[3:0] 5

U7E — MAX II Power (EPM2210_F256FBGA)

GNDINT: H7, H9, J8, J10, G6, F7, K11, L10
VCCINT: H8, H10, J7, J9, K6, L7, G11, F10
GNDIO: A1, A16, B2, B15, G7, G8, G9, G10, K7, K8, K9, K10, R2, R15, T1, T16
VCCIO1: C1, H6, J6, P1
VCCIO2: A3, A14, F8, F9
VCCIO3: C16, H11, J11, P16
VCCIO4: L8, L9, T3, T14

2.5V / 1.8V

Place near MAX II
2.5V: C147, C157, C108, C179, C107, C126, C109, C127 (0.1uF each)
1.8V: C211, C144, C146, C145, C137, C178, C125, C148, C212, C177, C213, C156 (0.1uF each)

Title: **Cyclone III Development Kit Host Board**
Size: B
Document Number: 150-0310703-D3
Rev: D-3
Date: Saturday, May 28, 2011
Sheet 8 of 20

ALTERA

DDR2 SDRAM (x72)

U26A — MT47H32M16CC

Pin	Signal		DQ	Signal
DDR2BOT_A0	M8	A0	DQ0	DDR2_DQ0	G8
DDR2BOT_A1	M3	A1	DQ1	DDR2_DQ1	G2
DDR2BOT_A2	M7	A2	DQ2	DDR2_DQ2	H7
DDR2BOT_A3	N2	A3	DQ3	DDR2_DQ3	H3
DDR2BOT_A4	N8	A4	DQ4	DDR2_DQ4	H1
DDR2BOT_A5	N3	A5	DQ5	DDR2_DQ5	H9
DDR2BOT_A6	N7	A6	DQ6	DDR2_DQ6	F9
DDR2BOT_A7	P2	A7	DQ7	DDR2_DQ7	F1
DDR2BOT_A8	P8	A8	DQ8	DDR2_DQ8	C8
DDR2BOT_A9	P3	A9	DQ9	DDR2_DQ9	C2
DDR2BOT_A10	M2	A10	DQ10	DDR2_DQ10	D7
DDR2BOT_A11	P7	A11	DQ11	DDR2_DQ11	D1
DDR2BOT_A12	R2	A12	DQ12	DDR2_DQ12	D9
DDR2BOT_A13	R8	RFU/A13	DQ13	DDR2_DQ13	B1
DDR2BOT_A14	R3	RFU/A14	DQ14	DDR2_DQ14	B7
DDR2BOT_A15	R7	RFU/A15	DQ15	DDR2_DQ15	B9
DDR2BOT_BA0	L2	BA0			
DDR2BOT_BA1	L3	BA1	UDQS_P	DDR2_DQS1	B7
DDR2BOT_BA2	L1	RFU/BA2	UDQS_N		A8
DDR2_DM0	F3	LDM	LDQS_P	DDR2_DQS0	F7
DDR2_DM1		UDM	LDQS_N		E8
DDR2BOT_RASn	K7	RAS_N	CKE	DDR2BOT_CKE	K2
DDR2BOT_CASn	L7	CAS_N	CK_P	DDR2_CK_P0	J8
DDR2BOT_WEn	K3	WE_N	CK_N	DDR2_CK_N0	K8
DDR2BOT_CSn	L8	CS_N			
DDR2BOT_ODT	K9	ODT	VREF	VREF_B3_B4	J2

C442 0.1uF

U25A — MT47H32M16CC

Pin	Signal		DQ	Signal
DDR2BOT_A0	M8	A0	DQ0	DDR2_DQ16	G8
DDR2BOT_A1	M3	A1	DQ1	DDR2_DQ17	G2
DDR2BOT_A2	M7	A2	DQ2	DDR2_DQ18	H7
DDR2BOT_A3	N2	A3	DQ3	DDR2_DQ19	H3
DDR2BOT_A4	N8	A4	DQ4	DDR2_DQ20	H1
DDR2BOT_A5	N3	A5	DQ5	DDR2_DQ21	H9
DDR2BOT_A6	N7	A6	DQ6	DDR2_DQ22	F9
DDR2BOT_A7	P2	A7	DQ7	DDR2_DQ23	F1
DDR2BOT_A8	P8	A8	DQ8	DDR2_DQ24	C8
DDR2BOT_A9	P3	A9	DQ9	DDR2_DQ25	C2
DDR2BOT_A10	M2	A10	DQ10	DDR2_DQ26	D7
DDR2BOT_A11	P7	A11	DQ11	DDR2_DQ27	D1
DDR2BOT_A12	R2	A12	DQ12	DDR2_DQ28	D9
DDR2BOT_A13	R8	RFU/A13	DQ13	DDR2_DQ29	B1
DDR2BOT_A14	R3	RFU/A14	DQ14	DDR2_DQ30	B7
DDR2BOT_A15	R7	RFU/A15	DQ15	DDR2_DQ31	B9
DDR2BOT_BA0	L2	BA0			
DDR2BOT_BA1	L3	BA1	UDQS_P	DDR2_DQS3	B7
DDR2BOT_BA2	L1	RFU/BA2	UDQS_N		A8
DDR2_DM2	F3	LDM	LDQS_P	DDR2_DQS2	F7
DDR2_DM3		UDM	LDQS_N		E8
DDR2BOT_RASn	K7	RAS_N	CKE	DDR2BOT_CKE	K2
DDR2BOT_CASn	L7	CAS_N	CK_P	DDR2_CK_P0	J8
DDR2BOT_WEn	K3	WE_N	CK_N	DDR2_CK_N0	K8
DDR2BOT_CSn	L8	CS_N			
DDR2BOT_ODT	K9	ODT	VREF	VREF_B3_B4	J2

C443 0.1uF

U11A — MT47H32M16CC

Pin	Signal		DQ	Signal
DDR2TOP_A0	M8	A0	DQ0	DDR2_DQ32	G8
DDR2TOP_A1	M3	A1	DQ1	DDR2_DQ33	G2
DDR2TOP_A2	M7	A2	DQ2	DDR2_DQ34	H7
DDR2TOP_A3	N2	A3	DQ3	DDR2_DQ35	H3
DDR2TOP_A4	N8	A4	DQ4	DDR2_DQ36	H1
DDR2TOP_A5	N3	A5	DQ5	DDR2_DQ37	H9
DDR2TOP_A6	N7	A6	DQ6	DDR2_DQ38	F9
DDR2TOP_A7	P2	A7	DQ7	DDR2_DQ39	F1
DDR2TOP_A8	P8	A8	DQ8	DDR2_DQ40	C8
DDR2TOP_A9	P3	A9	DQ9	DDR2_DQ41	C2
DDR2TOP_A10	M2	A10	DQ10	DDR2_DQ42	D7
DDR2TOP_A11	P7	A11	DQ11	DDR2_DQ43	D1
DDR2TOP_A12	R2	A12	DQ12	DDR2_DQ44	D9
DDR2TOP_A13	R8	RFU/A13	DQ13	DDR2_DQ45	B1
DDR2TOP_A14	R3	RFU/A14	DQ14	DDR2_DQ46	B7
DDR2TOP_A15	R7	RFU/A15	DQ15	DDR2_DQ47	B9
DDR2TOP_BA0	L2	BA0			
DDR2TOP_BA1	L3	BA1	UDQS_P	DDR2_DQS5	B7
DDR2TOP_BA2	L1	RFU/BA2	UDQS_N		A8
DDR2_DM4	F3	LDM	LDQS_P	DDR2_DQS4	F7
DDR2_DM5		UDM	LDQS_N		E8
DDR2TOP_RASn	K7	RAS_N	CKE	DDR2TOP_CKE	K2
DDR2TOP_CASn	L7	CAS_N	CK_P	DDR2_CK_P1	J8
DDR2TOP_WEn	K3	WE_N	CK_N	DDR2_CK_N1	K8
DDR2TOP_CSn	L8	CS_N			
DDR2TOP_ODT	K9	ODT	VREF	VREF_B7_B8	J2

C204 0.1uF

U12A — MT47H32M16CC

Pin	Signal		DQ	Signal
DDR2TOP_A0	M8	A0	DQ0	DDR2_DQ48	G8
DDR2TOP_A1	M3	A1	DQ1	DDR2_DQ49	G2
DDR2TOP_A2	M7	A2	DQ2	DDR2_DQ50	H7
DDR2TOP_A3	N2	A3	DQ3	DDR2_DQ51	H3
DDR2TOP_A4	N8	A4	DQ4	DDR2_DQ52	H1
DDR2TOP_A5	N3	A5	DQ5	DDR2_DQ53	H9
DDR2TOP_A6	N7	A6	DQ6	DDR2_DQ54	F9
DDR2TOP_A7	P2	A7	DQ7	DDR2_DQ55	F1
DDR2TOP_A8	P8	A8	DQ8	DDR2_DQ56	C8
DDR2TOP_A9	P3	A9	DQ9	DDR2_DQ57	C2
DDR2TOP_A10	M2	A10	DQ10	DDR2_DQ58	D7
DDR2TOP_A11	P7	A11	DQ11	DDR2_DQ59	D1
DDR2TOP_A12	R2	A12	DQ12	DDR2_DQ60	D9
DDR2TOP_A13	R8	RFU/A13	DQ13	DDR2_DQ61	B1
DDR2TOP_A14	R3	RFU/A14	DQ14	DDR2_DQ62	B7
DDR2TOP_A15	R7	RFU/A15	DQ15	DDR2_DQ63	B9
DDR2TOP_BA0	L2	BA0			
DDR2TOP_BA1	L3	BA1	UDQS_P	DDR2_DQS7	B7
DDR2TOP_BA2	L1	RFU/BA2	UDQS_N		A8
DDR2_DM6	F3	LDM	LDQS_P	DDR2_DQS6	F7
DDR2_DM7		UDM	LDQS_N		E8
DDR2TOP_RASn	K7	RAS_N	CKE	DDR2TOP_CKE	K2
DDR2TOP_CASn	L7	CAS_N	CK_P	DDR2_CK_P1	J8
DDR2TOP_WEn	K3	WE_N	CK_N	DDR2_CK_N1	K8
DDR2TOP_CSn	L8	CS_N			
DDR2TOP_ODT	K9	ODT	VREF	VREF_B7_B8	J2

C200 0.1uF

U13 — MT47H32M8BP

1.8V
VREF_B7_B8
C197 0.1uF

VDD / VDDL / VDDQ / VREF

Signal	Pin		DQ	Signal
DDR2TOP_A0	H8	A0	DQ0	DDR2_DQ64	C8
DDR2TOP_A1	H3	A1	DQ1	DDR2_DQ65	C2
DDR2TOP_A2	H7	A2	DQ2	DDR2_DQ66	D7
DDR2TOP_A3	J2	A3	DQ3	DDR2_DQ67	D1
DDR2TOP_A4	J8	A4	DQ4	DDR2_DQ68	D9
DDR2TOP_A5	J7	A5	DQ5	DDR2_DQ69	B1
DDR2TOP_A6	J7	A6	DQ6	DDR2_DQ70	B7
DDR2TOP_A7	K2	A7	DQ7	DDR2_DQ71	B9
DDR2TOP_A8	K8	A8			
DDR2TOP_A9	K3	A9	DQS_P	DDR2_DQS8	B7
DDR2TOP_A10	H2	A10	DQS_N		A8
DDR2TOP_A11	K7	A11			
DDR2TOP_A12	L2	A12	DM/RDQS_P	DDR2_DM8	A2
			RDQS_N		B3
DDR2TOP_BA0	G2	BA0	ODT	DDR2TOP_ODT	F9
DDR2TOP_BA1	G3	BA1			
DDR2TOP_RASn	F7	RAS_N			
DDR2TOP_CASn	F3	CAS_N	RFU1	DDR2TOP_BA2	G1
DDR2TOP_WEn	G7	WE_N	RFU2	DDR2TOP_A14	L3
DDR2TOP_CSn	G8	CS_N	RFU3		L7
DDR2_CK_P2	E8	CK_P	RFU4	DDR2TOP_A13	L8
DDR2_CK_N2	F8	CK_N			
DDR2TOP_CKE	F2	CKE			

PROVIDES CLOCK SIGNAL LOAD
SIMILAR TO OTHER DDR2 CLK SIGNALS.

DDR2_CK_P0 — R206 100, 1% — DDR2_CK_N0
DDR2_CK_P1 — R133 100, 1% — DDR2_CK_N1
DDR2_CK_P2 — R132 100, 1% — DDR2_CK_N2

DDR2_CK_P2 — C217 1pF
DDR2_CK_N2 — C182 1pF

DDR2TOP_ACTIVE — D11 Green_LED — DDR2TOP_ACTIVE_RES — R33 56.2 — 3.3V
DDR2BOT_ACTIVE — D16 Green_LED — DDR2BOT_ACTIVE_RES — R45 56.2

DDR2_DQ[71:0] → DDR2_DQ[71:0] 10,19
DDR2_DQS[8:0] → DDR2_DQS[8:0] 10,19
DDR2_DM[8:0] → DDR2_DM[8:0] 10,19
DDR2BOT_A[15:0] → DDR2BOT_A[15:0] 7,10,19
DDR2BOT_BA[2:0] → DDR2BOT_BA[2:0] 10,19
DDR2TOP_A[15:0] → DDR2TOP_A[15:0] 6,7,10,19
DDR2TOP_BA[2:0] → DDR2TOP_BA[2:0] 10,19

DDR2BOT_RASn → DDR2BOT_RASn 6,10
DDR2BOT_CASn → DDR2BOT_CASn 10,19
DDR2BOT_WEn → DDR2BOT_WEn 10,19
DDR2BOT_CSn → DDR2BOT_CSn 10,19
DDR2BOT_ODT → DDR2BOT_ODT 10,19
DDR2BOT_CKE → DDR2BOT_CKE 10,19

DDR2TOP_RASn → DDR2TOP_RASn 10,19
DDR2TOP_CASn → DDR2TOP_CASn 10,19
DDR2TOP_WEn → DDR2TOP_WEn 10,19
DDR2TOP_CSn → DDR2TOP_CSn 10,19
DDR2TOP_ODT → DDR2TOP_ODT 10,19
DDR2TOP_CKE → DDR2TOP_CKE 10,19

DDR2_CK_P[2:0] → DDR2_CK_P[2:0] 19
DDR2_CK_N[2:0] → DDR2_CK_N[2:0] 19

DDR2TOP_ACTIVE → DDR2TOP_ACTIVE 19
DDR2BOT_ACTIVE → DDR2BOT_ACTIVE 6

DDR2 SDRAM POWER & TERM

DDR2_DQ[71:0]   9,19
DDR2_DQS[8:0]   9,19
DDR2_DM[8:0]   9,19
DDR2BOT_A[15:0]   7,9,19
DDR2BOT_BA[2:0]   9,19
DDR2TOP_A[15:0]   6,7,9,19
DDR2TOP_BA[2:0]   9,19

DDR2BOT_RASn   6,9
DDR2BOT_CASn   9,19
DDR2BOT_WEn   9,19
DDR2BOT_CSn   9,19
DDR2BOT_ODT   9,19
DDR2BOT_CKE   9,19

DDR2TOP_RASn   9,19
DDR2TOP_CASn   9,19
DDR2TOP_WEn   9,19
DDR2TOP_CSn   9,19
DDR2TOP_ODT   9,19
DDR2TOP_CKE   9,19

PLACE CAPS NEAR U18, U19, U20, U21, U22

1.8V U26B MT47H32M16CC
1.8V U25B MT47H32M16CC
1.8V U11B MT47H32M16CC
1.8V U12B MT47H32M16CC

VTT_B3_B4   VTT_B7_B8

PLACE CAPS NEAR U22
C198 C216 C226 C158 C227 C228 C229 C218 C199 C183
0.1uF 0.1uF 0.1uF 0.1uF 4.7nF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

PLACE CAPS NEAR U18
C396 C397 C427 C411 C441 C426 C425 C410 C405 C395 C398 C406 C412 C456 C455 C454
0.1uF 0.1uF 0.01uF 0.1uF 4.7nF 0.1uF 0.1uF 0.01uF 0.1uF 0.1uF 0.01uF 4.7nF 0.1uF 0.1uF 0.1uF 0.1uF

PLACE CAPS NEAR U19
C429 C414 C400 C457 C458 C428 C413 C407 C399 C402 C408 C415 C430 C431 C449 C401
0.1uF 0.1uF 0.01uF 0.1uF 4.7nF 0.1uF 0.1uF 0.01uF 0.1uF 0.1uF 0.01uF 4.7nF 0.1uF 0.1uF 0.1uF 0.1uF

PLACE CAPS NEAR U20
C223 C234 C246 C160 C186 C245 C222 C233 C244 C187 C206 C224 C235 C248 C205 C247
0.1uF 0.1uF 0.01uF 0.1uF 4.7nF 0.1uF 0.1uF 0.01uF 0.1uF 0.1uF 0.01uF 4.7nF 0.1uF 0.1uF 0.1uF 0.1uF

PLACE CAPS NEAR U21
C241 C240 C230 C219 C201 C184 C159 C220 C231 C242 C185 C202 C243 C203 C232 C221
0.1uF 0.1uF 0.01uF 0.1uF 4.7nF 0.1uF 0.1uF 0.01uF 0.1uF 0.1uF 0.01uF 4.7nF 0.1uF 0.1uF 0.1uF 0.1uF

CN18 0.1uf x 4   CN2 0.1uf x 4
CN15 0.1uf x 4   CN8 0.1uf x 4
CN16 0.1uf x 4   CN6 0.1uf x 4
CN17 0.1uf x 4   CN7 0.1uf x 4
CN13 0.1uf x 4   CN5 0.1uf x 4
CN14 0.1uf x 4   CN10 0.1uf x 4
CN11 0.1uf x 4   CN9 0.1uf x 4
CN12 0.1uf x 4   CN4 0.1uf x 4
CN19 0.1uf x 4   CN3 0.1uf x 4
CN1 0.1uf x 4

VTT_B3_B4   VTT_B7_B8

SRAM & Flash

SRAM 32Mb (2M X 16)

U23 K1B3216B2E

Pin	Signal		Pin	Signal
A3	A0	DQ0	B6	FSD0
A4	A1	DQ1	C5	FSD1
A5	A2	DQ2	C6	FSD2
B3	A3	DQ3	D5	FSD3
B4	A4	DQ4	E5	FSD4
C3	A5	DQ5	F5	FSD5
C4	A6	DQ6	F6	FSD6
D4	A7	DQ7	G6	FSD7
H2	A8	DQ8	B1	FSD8
H3	A9	DQ9	C1	FSD9
H4	A10	DQ10	C2	FSD10
H5	A11	DQ11	D2	FSD11
G3	A12	DQ12	E2	FSD12
G4	A13	DQ13	F2	FSD13
F3	A14	DQ14	F1	FSD14
E4	A15	DQ15	G1	FSD15
D3	A16			
H1	A17			
G2	A18			
H6	A19			
	A20			

FSA1...FSA21 on address pins

J2	CLK	WAIT	J1	SRAM_WAIT0
B5	CS			
J3	ADV			
A2	OE			
G5	WE	RFU1	E3	
B2	UB	RFU2	J4	
A1	LB	RFU3	J5	
A6	PS	RFU4	J6	
E1	VCC	VSSQ	D1	
D6	VCCQ	VSSQ	E6	

K1B3216B2E

1.8V

SRAM 32Mb (2M X 16)

U24 K1B3216B2E

Pin	Signal		Pin	Signal
A3	A0	DQ0	B6	FSD16
A4	A1	DQ1	C5	FSD17
A5	A2	DQ2	C6	FSD18
B3	A3	DQ3	D5	FSD19
B4	A4	DQ4	E5	FSD20
C3	A5	DQ5	F5	FSD21
C4	A6	DQ6	F6	FSD22
D4	A7	DQ7	G6	FSD23
H2	A8	DQ8	B1	FSD24
H3	A9	DQ9	C1	FSD25
H4	A10	DQ10	C2	FSD26
H5	A11	DQ11	D2	FSD27
G3	A12	DQ12	E2	FSD28
G4	A13	DQ13	F2	FSD29
F3	A14	DQ14	F1	FSD30
E4	A15	DQ15	G1	FSD31
D3	A16			
H1	A17			
G2	A18			
H6	A19			
	A20			

J2	CLK	WAIT	J1	SRAM_WAIT1
B5	CS			
J3	ADV			
A2	OE			
G5	WE	RFU1	E3	
B2	UB	RFU2	J4	
A1	LB	RFU3	J5	
A6	PS	RFU4	J6	
E1	VCC	VSSQ	D1	
D6	VCCQ	VSSQ	E6	

K1B3216B2E

1.8V

3.3V 1.8V

C469 0.1uF   C468 C479 0.1uF 0.1uF

U31 S29GL512N

Pin	Signal		Pin	Signal
E2	A0	DQ0	E3	FSD0
D2	A1	DQ1	H3	FSD1
C2	A2	DQ2	E4	FSD2
B2	A3	DQ3	H4	FSD3
D3	A4	DQ4	H5	FSD4
C3	A5	DQ5	E5	FSD5
A3	A6	DQ6	H6	FSD6
B6	A7	DQ7	F3	FSD7
A6	A8	DQ8	E6	FSD8
C6	A9	DQ9	G3	FSD9
D6	A10	DQ10	F4	FSD10
B7	A11	DQ11	F5	FSD11
A7	A12	DQ12	G4	FSD12
C7	A13	DQ13	G5	FSD13
A4	A14	DQ14	F6	FSD14
D7	A15	DQ15	G7	FSD15
E7	A16			
B3	A17			
C4	A18	CEn	F2	FLASH_CEn
D5	A19	RESETn	B5	FLASH_RESETn
D4	A20	OEn	G2	FLASH_OEn
C5	A21			
B8	A22	BYTEn	A5	FLASH_BYTEn
C8	A23	WEn	E1	FLASH_WEn
F8	A24			
		WPn	B4	FLASH_WPn
		RDYBSYn	A4	FLASH_RDYBSYn

VCC VIO VIO G5 D8 F1

A8	NC_A8	NC_C1	C1
G8	NC_G8	NC_D1	D1
H8	NC_H8	NC_E1	E1
A1	NC_A1	NC_G1	G1
B1	NC_B1	NC_H1	H1

VSS VSS VSS   E8 H7 H2

S29GL512N

SHARED BUS

FSD[31:0]   FSD[31:0] 6,8,19

FSA[24:0]   FSA[24:0] 7,8,19

PSRAM INTERFACE

SRAM_CLK	SRAM_CLK 19
SRAM_CSn	SRAM_CSn 8,19
SRAM_ADVn	SRAM_ADVn 19
SRAM_OEn	SRAM_OEn 19
SRAM_WEn	SRAM_WEn 19
SRAM_PSn	SRAM_PSn 19
SRAM_WAIT0	SRAM_WAIT0 7
SRAM_WAIT1	SRAM_WAIT1 19
SRAM_BEn[3:0]	SRAM_BEn[3:0] 19
SRAM_ACTIVE	SRAM_ACTIVE 8

FLASH INTERFACE

FLASH_RESETn	FLASH_RESETn 6,8
FLASH_WEn	FLASH_WEn 8,19
FLASH_OEn	FLASH_OEn 6,8
FLASH_RDYBSYn	FLASH_RDYBSYn 8,19
FLASH_CEn	FLASH_CEn 6,8
FLASH_BYTEn	FLASH_BYTEn 8
FLASH_ACTIVE	FLASH_ACTIVE 8

1.8V

R205	10K	SRAM_CSn
R200	10K	SRAM_ADVn
R209	10K	SRAM_OEn
R203	10K	SRAM_WEn
R216	10K	SRAM_BEn3
R212	10K	SRAM_BEn2
R204	10K	SRAM_BEn1
R208	10K	SRAM_BEn0
R210	10K	SRAM_PSn
R211	DNI	SRAM_PSn

1.8V

R237	10K	FLASH_WPn
R232	10K	FLASH_CEn
R225	10K	FLASH_OEn
R239	10K	FLASH_WEn
R226	10K	FLASH_BYTEn
R236	10K	FLASH_RDYBSYn
R238	10K	FLASH_RESETn

3.3V

SRAM_ACTIVE   D17   SRAM_ACTIVE_RES   R47   56.2
Green_LED

FLASH_ACTIVE   D23   FLASH_ACTIVE_RES   R76   56.2
Green_LED

Title: Cyclone III Development Kit Host Board

Size: B

Document Number: 150-0310703-D3

Rev: D-3

USB 2.0

USB 2.0 INTERFACE

USB_PHY_FD[15..0]   USB_PHY_FD[15..0]   8

USB_RDn   USB_RDn   8
USB_WR   USB_WR   8
USB_TXEn   USB_TXEn   8
USB_RXFn   USB_RXFn   8
USB_PWR_ENn   USB_PWR_ENn   8
USB_RSTn   USB_RSTn   8
USB_RSTOUTn   USB_RSTOUTn   8
USB_SI_WU   USB_SI_WU   8

USB_PHY_IFCLK   USB_PHY_IFCLK   8
USB_PHY_CMD_DATA   USB_PHY_CMD_DATA   8
USB_PHY_REN   USB_PHY_REN   8
USB_PHY_WEN   USB_PHY_WEN   8
USB_PHY_EMPTY   USB_PHY_EMPTY   8
USB_PHY_FULL   USB_PHY_FULL   8
USB_RESETn   USB_RESETn   8
USB_WAKEUP   USB_WAKEUP   8
USB_CLKOUT   USB_CLKOUT   8
USB_PA0_INT0n   USB_PA0_INT0n   8
USB_PA1_INT1n   USB_PA1_INT1n   8
USB_PA2_SLOE   USB_PA2_SLOE   8
USB_PA3_WU2   USB_PA3_WU2   8
USB_PA4_IF0ADR0   USB_PA4_IF0ADR0   8
USB_PA5_IF0ADR1   USB_PA5_IF0ADR1   8
USB_PA6_PKTEND   USB_PA6_PKTEND   8
USB_PA7_SLCSn   USB_PA7_SLCSn   8

U18 SN65220DBV
1 NC1   A 6
3 NC2   B 4
2 GND GND 5

USB
J3 USB CON

5V_USB
L1 BLM21PG331SN1
C22 10uF
R121 27
R120 27
USB_DM   USB_FTDI_DM
USB_DP   USB_FTDI_DP

R128 1.5K USB_RSTOUTn
R127 10.0K USB_RSTn

5V_USB
R124 470
C136 0.1uF
C143 33nF

5V_USB 3.3V
C175 0.1uF

U8 FT245BL
3V3OUT   D0 25 USB_PHY_FD0
                D1 24 USB_PHY_FD1
USBDM   D2 23 USB_PHY_FD2
USBDP   D3 22 USB_PHY_FD3
                D4 21 USB_PHY_FD4
RSTOUT#   D5 20 USB_PHY_FD5
                D6 19 USB_PHY_FD6
XTIN 27   D7 18 USB_PHY_FD7
XTOUT 28
RESET#   RD# 16 USB_RDn
                WR 15 USB_WR
EECS   TXE# 14 USB_TXEn
EESK   RXF# 12 USB_RXFn
EEDATA
                SI/WU 11 USB_SI_WU
TEST   PWREN# 10 USB_PWR_ENn
GND1 GND2 AGND

USB_EECS   32
USB_EESK   1
           2

3.3V
R130 1.00k

U17 AT93C46DN-SH-B
1 CS   VCC 8
2 SK   NC1 7
3 DIN   ORG 6
4 DOUT   GND 5
(Optional)

R144 2.2K
R143 10.0K
USB_EEDATA

5V_USB

DECOUPLING CAPS
C47 10uF
C124 0.1uF
C142 0.1uF
10V Tantalum

XTIN / XTOUT
C105 36pF   XTIN
Y2 6.000 MHZ
C96 36pF   XTOUT

3.3V

U9

AVCC AVCC VCC VCC VCC VCC VCC VCC
3 7 11 17 27 32 43 55

USB_PHY_EMPTY 1 RDY0/SLRD   PA0/INT0n 33 USB_PA0_INT0n
USB_PHY_FULL   2 RDY1/SLWR   PA1/INT1n 34 USB_PA1_INT1n
                                  PA2/SLOE   35 USB_PA2_SLOE
XTALIN   5 XTALIN   PA3/WU2   36 USB_PA3_WU2
XTALOUT   4 XTALOUT   PA4/FIFOADR0 37 USB_PA4_IF0ADR0
                                  PA5/FIFOADR1 38 USB_PA5_IF0ADR1
USB_DP   8 DPLUS   PA6/PKTEND   39 USB_PA6_PKTEND
USB_DM   9 DMINUS   PA7/FLAGD/SLCSn 40 USB_PA7_SLCSn

R17 2.2K USB_SCL 15 SCL   PB0/FD0 18 USB_PHY_FD0
R18 2.2K USB_SDA 16 SDA   PB1/FD1 19 USB_PHY_FD1
                   14 RESERVED   PB2/FD2 20 USB_PHY_FD2
R21 2.2K USB_WAKEUP 44 WAKEUP PB3/FD3 21 USB_PHY_FD3
R111 10.0K USB_RESETn 42 RESETn PB4/FD4 22 USB_PHY_FD4
                                  PB5/FD5 23 USB_PHY_FD5
                                  PB6/FD6 24 USB_PHY_FD6
                                  PB7/FD7 25 USB_PHY_FD7

USB_PHY_IFCLK R110 27 IFCLK 13 IFCLK(13A)/PE0(15A)/T0OUT(15A)
USB_CLKOUT   54 CLKOUT(13A)/PE1(15A)/T1OUT(15A)
                                  PD0/FD8 45 USB_PHY_FD8
                                  PD1/FD9 46 USB_PHY_FD9
C97 12pF XTALIN   PD2/FD10 47 USB_PHY_FD10
Y1 24.000 MHZ   PD3/FD11 48 USB_PHY_FD11
                                  PD4/FD12 49 USB_PHY_FD12
                                  PD5/FD13 50 USB_PHY_FD13
C106 12pF XTALOUT   PD6/FD14 51 USB_PHY_FD14
                                  PD7/FD15 52 USB_PHY_FD15

                   CTL0/FLAGA 29 USB_PHY_CMD_DATA
                   CTL1/FLAGB 30 USB_PHY_REN
                   CTL2/FLAGC 31 USB_PHY_WEN

AGND AGND GND GND GND GND GND GND GND
6 10 12 26 28 41 53 56 57
DNI

U15 QUSB2CP1
3.3V   3.3V
1 A0   VCC 8
2 A1   WP 7
3 A2   SCL 6 USB_SCL
4 GND   SDA 5 USB_SDA

Title
Cyclone III Development Kit Host Board

Size B
Document Number 150-0310703-D3
Rev E-1

10/100/1000 Ethernet

RGMII Mode

ETHERNET INTERFACE

ENET_TXD[3..0] — ENET_TXD[3..0] 18

ENET_GTX_CLK — ENET_GTX_CLK 6
ENET_TX_EN — ENET_TX_EN 18
ENET_MDC — ENET_MDC 6

ENET_RXD[3..0] — ENET_RXD[3..0] 6,18

ENET_RX_CLK — ENET_RX_CLK 7
ENET_RX_DV — ENET_RX_DV 6
ENET_MDIO — ENET_MDIO 6
ENET_RESETn — ENET_RESETn 18
ENET_LED_LINK1000 — ENET_LED_LINK1000 18

U5A
88E1111

U5B
88E1111

2.5V

R123	4.7K	ENET_MDIO
R115	4.7K	ENET_MDC
R125	4.7K	ENET_INTn
R116	4.7K	ENET_RESETn

C10	0.01uF	R12	49.9	MDI_P0
C8	0.01uF	R11	49.9	MDI_N0
		R10	49.9	MDI_P1
C86	0.01uF	R8	49.9	MDI_N1
		R105	49.9	MDI_P2
C87	0.01uF	R106	49.9	MDI_N2
		R107	49.9	MDI_P3
		R108	49.9	MDI_N3

TP2

TP1

ENET_HSDAC_P
ENET_HSDAC_N

3.3V

R113
10.0K

J1
HFJ11-1G02E

X1
25MHz
EN OUT
NC1 NC2
GND VCC

R117
4.99K

R118
4.7K

ENET_RSET
ENET_XTAL_25MHZ

Place near 88E1111 PHY

1.2V

2.5V

| C191 | C164 | C115 | C166 | C132 | C117 | C193 | C116 |
| 0.1uF | 0.1uF | 0.1uF | 0.1uF | 0.1uF | 0.1uF | 0.1uF | 0.1uF |

| C153 | C167 | C192 | C138 | C165 |
| 0.1uF | 0.1uF | 0.1uF | 0.1uF | 0.1uF |

ENET_LED_TX	R129	220	D7 Green_LED
ENET_LED_RX	R131	220	D8 Green_LED
ENET_LED_DUPLEX	R126	220	D6 Green_LED
ENET_LED_LINK1000	R119	220	D4 Green_LED
ENET_LED_LINK100	R114	220	D3 Green_LED
ENET_LED_LINK10	R109	220	D1 Green_LED

2.5V

Title: **Cyclone III Development Kit Host Board**

Size B
Document Number 150-0310703-D3
Rev D-3

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High Speed Mezzanine (HSM) Interface

J8

BANK 1

BANK 2

BANK 3

HSMA_SDA
FPGA_JTAG_TCK
HSMA_JTAG_TDO
HSMA_CLK_OUT0

HSMA_D0
HSMA_D2
3.3V
HSMA_TX_D_P0
HSMA_TX_D_N0
3.3V
HSMA_TX_D_P1
HSMA_TX_D_N1
3.3V
HSMA_TX_D_P2
HSMA_TX_D_N2
3.3V
HSMA_TX_D_P3
HSMA_TX_D_N3
3.3V
HSMA_TX_D_P4
HSMA_TX_D_N4
3.3V
HSMA_TX_D_P5
HSMA_TX_D_N5
3.3V
HSMA_TX_D_P6
HSMA_TX_D_N6
3.3V
HSMA_TX_D_P7
HSMA_TX_D_N7
3.3V
HSMA_CLK_OUT_P1
HSMA_CLK_OUT_N1
3.3V

HSMA_TX_D_P8
HSMA_TX_D_N8
3.3V
HSMA_TX_D_P9
HSMA_TX_D_N9
3.3V
HSMA_TX_D_P10
HSMA_TX_D_N10
3.3V
HSMA_TX_D_P11
HSMA_TX_D_N11
3.3V
HSMA_TX_D_P12
HSMA_TX_D_N12
3.3V
HSMA_TX_D_P13
HSMA_TX_D_N13
3.3V
HSMA_TX_D_P14
HSMA_TX_D_N14
3.3V
HSMA_TX_D_P15
HSMA_TX_D_N15
3.3V
HSMA_TX_D_P16
HSMA_TX_D_N16
3.3V
HSMA_CLK_OUT_P2
HSMA_CLK_OUT_N2
3.3V

HSMA_SCL
FPGA_JTAG_TMS
HSMA_JTAG_TDI
HSMA_CONN_CLK_IN0

HSMA_D1
HSMA_D3
12V
HSMA_RX_D_P0
HSMA_RX_D_N0
12V
HSMA_RX_D_P1
HSMA_RX_D_N1
12V
HSMA_RX_D_P2
HSMA_RX_D_N2
12V
HSMA_RX_D_P3
HSMA_RX_D_N3
12V
HSMA_RX_D_P4
HSMA_RX_D_N4
12V
HSMA_RX_D_P5
HSMA_RX_D_N5
12V
HSMA_RX_D_P6
HSMA_RX_D_N6
12V
HSMA_RX_D_P7
HSMA_RX_D_N7
12V
HSMA_CLK_IN_P1
HSMA_CLK_IN_N1
12V

HSMA_RX_D_P8
HSMA_RX_D_N8
12V
HSMA_RX_D_P9
HSMA_RX_D_N9
12V
HSMA_RX_D_P10
HSMA_RX_D_N10
12V
HSMA_RX_D_P11
HSMA_RX_D_N11
12V
HSMA_RX_D_P12
HSMA_RX_D_N12
12V
HSMA_RX_D_P13
HSMA_RX_D_N13
12V
HSMA_RX_D_P14
HSMA_RX_D_N14
12V
HSMA_RX_D_P15
HSMA_RX_D_N15
12V
HSMA_RX_D_P16
HSMA_RX_D_N16
12V
HSMA_CLK_IN_P2
HSMA_CLK_IN_N2
HSMA_PSNTn

ASP-122953-01

HSMA_PSNTn   R213   56.2
D18 Green_LED   3.3V

J9

BANK 1

BANK 2

BANK 3

HSMB_SDA
FPGA_JTAG_TCK
HSMB_JTAG_TDO
HSMB_CLK_OUT0

HSMB_D0
HSMB_D2
3.3V
HSMB_TX_D_P0
HSMB_TX_D_N0
3.3V
HSMB_TX_D_P1
HSMB_TX_D_N1
3.3V
HSMB_TX_D_P2
HSMB_TX_D_N2
3.3V
HSMB_TX_D_P3
HSMB_TX_D_N3
3.3V
HSMB_TX_D_P4
HSMB_TX_D_N4
3.3V
HSMB_TX_D_P5
HSMB_TX_D_N5
3.3V
HSMB_TX_D_P6
HSMB_TX_D_N6
3.3V
HSMB_TX_D_P7
HSMB_TX_D_N7
3.3V
HSMB_CLK_OUT_P1
HSMB_CLK_OUT_N1
3.3V

HSMB_TX_D_P8
HSMB_TX_D_N8
3.3V
HSMB_TX_D_P9
HSMB_TX_D_N9
3.3V
HSMB_TX_D_P10
HSMB_TX_D_N10
3.3V
HSMB_TX_D_P11
HSMB_TX_D_N11
3.3V
HSMB_TX_D_P12
HSMB_TX_D_N12
3.3V
HSMB_TX_D_P13
HSMB_TX_D_N13
3.3V
HSMB_TX_D_P14
HSMB_TX_D_N14
3.3V
HSMB_TX_D_P15
HSMB_TX_D_N15
3.3V
HSMB_TX_D_P16
HSMB_TX_D_N16
3.3V
HSMB_CLK_OUT_P2
HSMB_CLK_OUT_N2
3.3V

HSMB_SCL
FPGA_JTAG_TMS
HSMB_JTAG_TDI
HSMB_CONN_CLK_IN0

HSMB_D1
HSMB_D3
12V
HSMB_RX_D_P0
HSMB_RX_D_N0
12V
HSMB_RX_D_P1
HSMB_RX_D_N1
12V
HSMB_RX_D_P2
HSMB_RX_D_N2
12V
HSMB_RX_D_P3
HSMB_RX_D_N3
12V
HSMB_RX_D_P4
HSMB_RX_D_N4
12V
HSMB_RX_D_P5
HSMB_RX_D_N5
12V
HSMB_RX_D_P6
HSMB_RX_D_N6
12V
HSMB_RX_D_P7
HSMB_RX_D_N7
12V
HSMB_CLK_IN_P1
HSMB_CLK_IN_N1
12V

HSMB_RX_D_P8
HSMB_RX_D_N8
12V
HSMB_RX_D_P9
HSMB_RX_D_N9
12V
HSMB_RX_D_P10
HSMB_RX_D_N10
12V
HSMB_RX_D_P11
HSMB_RX_D_N11
12V
HSMB_RX_D_P12
HSMB_RX_D_N12
12V
HSMB_RX_D_P13
HSMB_RX_D_N13
12V
HSMB_RX_D_P14
HSMB_RX_D_N14
12V
HSMB_RX_D_P15
HSMB_RX_D_N15
12V
HSMB_RX_D_P16
HSMB_RX_D_N16
12V
HSMB_CLK_IN_P2
HSMB_CLK_IN_N2
HSMB_PSNTn

ASP-122953-01

HSMB_PSNTn   R207   56.2
D19 Green_LED   3.3V

JTAG INTERFACE

FPGA_JTAG_TCK → FPGA_JTAG_TCK 8,17
FPGA_JTAG_TMS → FPGA_JTAG_TMS 8,17
HSMA_JTAG_TDO → HSMA_JTAG_TDO 8
HSMA_JTAG_TDI → HSMA_JTAG_TDI 8
HSMB_JTAG_TDO → HSMB_JTAG_TDO 8
HSMB_JTAG_TDI → HSMB_JTAG_TDI 8

HSMC PORT A

HSMA_SDA → HSMA_SDA 18
HSMA_SCL → HSMA_SCL 18
HSMA_CONN_CLK_IN0 → HSMA_CONN_CLK_IN0 7
HSMA_CLK_OUT0 → HSMA_CLK_OUT0 18
HSMA_CLK_IN_P[2:1] → HSMA_CLK_IN_P[2:1] 7,15
HSMA_CLK_IN_N[2:1] → HSMA_CLK_IN_N[2:1] 7,15
HSMA_CLK_OUT_P[2:1] → HSMA_CLK_OUT_P[2:1] 18
HSMA_CLK_OUT_N[2:1] → HSMA_CLK_OUT_N[2:1] 18
HSMA_D[3:0] → HSMA_D[3:0] 18
HSMA_TX_D_P[16:0] → HSMA_TX_D_P[16:0] 6,18
HSMA_TX_D_N[16:0] → HSMA_TX_D_N[16:0] 18
HSMA_RX_D_P[16:0] → HSMA_RX_D_P[16:0] 15,18
HSMA_RX_D_N[16:0] → HSMA_RX_D_N[16:0] 15,18

HSMC PORT B

HSMB_SDA → HSMB_SDA 18
HSMB_SCL → HSMB_SCL 18
HSMB_CONN_CLK_IN0 → HSMB_CONN_CLK_IN0 7
HSMB_CLK_OUT0 → HSMB_CLK_OUT0 6
HSMB_CLK_IN_P[2:1] → HSMB_CLK_IN_P[2:1] 7,15
HSMB_CLK_IN_N[2:1] → HSMB_CLK_IN_N[2:1] 7,15
HSMB_CLK_OUT_P[2:1] → HSMB_CLK_OUT_P[2:1] 18
HSMB_CLK_OUT_N[2:1] → HSMB_CLK_OUT_N[2:1] 18
HSMB_D[3:0] → HSMB_D[3:0] 18
HSMB_TX_D_P[16:0] → HSMB_TX_D_P[16:0] 6,18
HSMB_TX_D_N[16:0] → HSMB_TX_D_N[16:0] 18
HSMB_RX_D_P[16:0] → HSMB_RX_D_P[16:0] 15,18
HSMB_RX_D_N[16:0] → HSMB_RX_D_N[16:0] 15,18

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High Speed Mezzanine (HSM) Termination

By default all of the data signal on the HSMC's are single ended. 100 Ohm resistors should be installed between the P/N pairs in order to use differential signals.

R190 DNI HSMA_RX_D_P0 / HSMA_RX_D_N0
R187 DNI HSMA_RX_D_P1 / HSMA_RX_D_N1
R186 DNI HSMA_RX_D_P2 / HSMA_RX_D_N2
R181 DNI HSMA_RX_D_P3 / HSMA_RX_D_N3
R180 DNI HSMA_RX_D_P4 / HSMA_RX_D_N4
R176 DNI HSMA_RX_D_P5 / HSMA_RX_D_N5
R175 DNI HSMA_RX_D_P6 / HSMA_RX_D_N6
R172 DNI HSMA_RX_D_P7 / HSMA_RX_D_N7

R166 DNI HSMA_RX_D_P8 / HSMA_RX_D_N8
R165 DNI HSMA_RX_D_P9 / HSMA_RX_D_N9
R160 DNI HSMA_RX_D_P10 / HSMA_RX_D_N10
R159 DNI HSMA_RX_D_P11 / HSMA_RX_D_N11
R156 DNI HSMA_RX_D_P12 / HSMA_RX_D_N12
R155 DNI HSMA_RX_D_P13 / HSMA_RX_D_N13
R152 DNI HSMA_RX_D_P14 / HSMA_RX_D_N14
R151 DNI HSMA_RX_D_P15 / HSMA_RX_D_N15
R148 DNI HSMA_RX_D_P16 / HSMA_RX_D_N16

R150 DNI HSMB_RX_D_P0 / HSMB_RX_D_N0
R149 DNI HSMB_RX_D_P1 / HSMB_RX_D_N1
R154 DNI HSMB_RX_D_P2 / HSMB_RX_D_N2
R153 DNI HSMB_RX_D_P3 / HSMB_RX_D_N3
R158 DNI HSMB_RX_D_P4 / HSMB_RX_D_N4
R157 DNI HSMB_RX_D_P5 / HSMB_RX_D_N5
R162 DNI HSMB_RX_D_P6 / HSMB_RX_D_N6
R161 DNI HSMB_RX_D_P7 / HSMB_RX_D_N7

R167 DNI HSMB_RX_D_P8 / HSMB_RX_D_N8
R174 DNI HSMB_RX_D_P9 / HSMB_RX_D_N9
R173 DNI HSMB_RX_D_P10 / HSMB_RX_D_N10
R179 DNI HSMB_RX_D_P11 / HSMB_RX_D_N11
R178 DNI HSMB_RX_D_P12 / HSMB_RX_D_N12
R184 DNI HSMB_RX_D_P13 / HSMB_RX_D_N13
R183 DNI HSMB_RX_D_P14 / HSMB_RX_D_N14
R189 DNI HSMB_RX_D_P15 / HSMB_RX_D_N15
R188 DNI HSMB_RX_D_P16 / HSMB_RX_D_N16

HSMA_CLK_IN_P1 R185
HSMA_CLK_IN_N1 DNI

HSMA_CLK_IN_P2 R147
HSMA_CLK_IN_N2 DNI

HSMB_CLK_IN_P1 R168
HSMB_CLK_IN_N1 DNI

HSMB_CLK_IN_P2 R192
HSMB_CLK_IN_N2 DNI

HSMC PORT A

HSMA_CLK_IN_P[2:1]   HSMA_CLK_IN_P[2:1]   7,14
HSMA_CLK_IN_N[2:1]   HSMA_CLK_IN_N[2:1]   7,14

HSMA_RX_D_P[16:0]   HSMA_RX_D_P[16:0]   14,18
HSMA_RX_D_N[16:0]   HSMA_RX_D_N[16:0]   14,18

HSMC PORT B

HSMB_CLK_IN_P[2:1]   HSMB_CLK_IN_P[2:1]   7,14
HSMB_CLK_IN_N[2:1]   HSMB_CLK_IN_N[2:1]   7,14

HSMB_RX_D_P[16:0]   HSMB_RX_D_P[16:0]   14,18
HSMB_RX_D_N[16:0]   HSMB_RX_D_N[16:0]   14,18

ALTERA®

User IO & Connector

Character LCD

3.3V

MAX_ERROR D21 Red_LED RES_MAX_ERROR R224 100, 1%
MAX_LOAD D20 Green_LED RES_MAX_LOAD R219 56.2
MAX_FACTORY D24 Green_LED RES_MAX_FACTORY R235 56.2
MAX_USER D22 Green_LED RES_MAX_USER R231 56.2
MAX_EMB D10 Green_LED RES_MAX_EMB R30 56.2

3.3V

USER_LED0 D33 Green_LED RESn_LED0 R243 56.2
USER_LED1 D32 Green_LED RESn_LED1 R244 56.2
USER_LED2 D31 Green_LED RESn_LED2 R245 56.2
USER_LED3 D30 Green_LED RESn_LED3 R246 56.2
USER_LED4 D29 Green_LED RESn_LED4 R247 56.2
USER_LED5 D28 Green_LED RESn_LED5 R248 56.2
USER_LED6 D27 Green_LED RESn_LED6 R249 56.2
USER_LED7 D26 Green_LED RESn_LED7 R250 56.2

5.0V

J4
VO 1 3
LCD_WEn 5
LCD_DATA0 7
LCD_DATA2 9
LCD_DATA4 11
LCD_DATA6 13
1 2 4 LCD_D_Cn
3 4 6 LCD_EN
5 6 8 LCD_DATA1
7 8 10 LCD_DATA3
9 10 12 LCD_DATA5
11 12 14 LCD_DATA7
13 14
HDR2X7

2.5V
C82 0.1uF C83 0.01uF
12V
C84 0.1uF C389 10uF 25V Tantalum

10.0K R102

Graphics LCD
J13
LCD_CSn 1
LCD_RSTn 2
LCD_D_Cn 3
LCD_WEn 4
LCD_E_RDn 5
LCD_DATA0 6
LCD_DATA1 7
LCD_DATA2 8
LCD_DATA3 9
LCD_DATA4 10
LCD_DATA5 11
LCD_DATA6 12
LCD_DATA7 13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
LCD_BS1 28
LCD_SERn 29
30
31
32
FPC_FFC_30PIN

V5
V2 V1
V3
V4
V5

1.8V 2.5V

S6 1 2 RESET_CONFIGn R103 10.0K
S5 1 2 CPU_RESETn R101 10.0K
S7 1 2 FACTORY_CONFIGn R104 10.0K

U30 QUAD_7SEG_M2212RI
SEVEN_SEG_SEL1 1 DIGIT1
SEVEN_SEG_SEL2 10 DIGIT2
SEVEN_SEG_SEL3 4 DIGIT3
SEVEN_SEG_SEL4 6 DIGIT4

an ca
A B C D E F G DP

2.5V
14 13 12 11 3 8 2 9 7 5

SEVEN_SEG_MINUS R61 220 LED_MINUS
SEVEN_SEG_A R60 0 LED_A
SEVEN_SEG_B R54 0 LED_B
SEVEN_SEG_C R78 0 LED_C
SEVEN_SEG_D R56 0 LED_D
SEVEN_SEG_E R77 0 LED_E
SEVEN_SEG_F R55 0 LED_F
SEVEN_SEG_G R62 0 LED_G
SEVEN_SEG_DP R79 0 LED_DP

HSMA_RX_LED D14 Green_LED RESn_HSMA_RX_LED R193 56.2
HSMA_TX_LED D12 Green_LED RESn_HSMA_TX_LED R182 56.2
HSMB_RX_LED D15 Green_LED RESn_HSMB_RX_LED R191 56.2
HSMB_TX_LED D13 Green_LED RESn_HSMB_TX_LED R177 56.2

FPGA_CONF_DONE D25 Green_LED

2.5V 12V
J15
LCD_DATA7 5
LCD_DATA6 6
LCD_DATA5 7
LCD_DATA4 8
LCD_DATA3 9
LCD_DATA2 10
LCD_DATA1 11
LCD_DATA0 12
LCD_E_RDn 13
LCD_WEn 14
LCD_D_Cn 15
LCD_BS1 16
LCD_RSTn 17
LCD_CSn 18
1
2
3
4
19
20
DNI

R252 10.0K

USER I/O's
MWATTS_MAMPS → MWATTS_MAMPS 8
VOLTS_WATTS → VOLTS_WATTS 8
MAX_RESERVE0 → MAX_RESERVE0 8
MAX_RESERVE1 → MAX_RESERVE1 8

FPGA_BYPASS → FPGA_BYPASS 8
HSMA_BYPASS → HSMA_BYPASS 8
HSMB_BYPASS → HSMB_BYPASS 8
MAX_EN → MAX_EN 8

MAX_ERROR → MAX_ERROR 8
MAX_LOAD → MAX_LOAD 8
MAX_FACTORY → MAX_FACTORY 8
MAX_USER → MAX_USER 8
MAX_EMB → MAX_EMB 8

USER_LED0 → USER_PB[3:0] 6,19
USER_DIPSW[7:0] → USER_DIPSW[7:0] 19
USER_LED[7:0] → USER_LED[7:0] 19

RESET_CONFIGn → RESET_CONFIGn 8
CPU_RESETn → CPU_RESETn 8,18
FACTORY_CONFIGn → FACTORY_CONFIGn 8
FPGA_CONF_DONE → FPGA_CONF_DONE 8,17

PGM[3:0] → PGM[3:0] 8
MAX_DIP[3:0] → MAX_DIP[3:0] 8
MAX_EN → MAX_EN 8

SPEAKER_OUT → SPEAKER_OUT 18
SPEAKER → SPEAKER 5

SEVEN-SEG INTERFACE
SEVEN_SEG_SEL[4:1] → SEVEN_SEG_SEL[4:1] 7,19
SEVEN_SEG_A → SEVEN_SEG_A 19
SEVEN_SEG_B → SEVEN_SEG_B 19
SEVEN_SEG_C → SEVEN_SEG_C 19
SEVEN_SEG_D → SEVEN_SEG_D 19
SEVEN_SEG_E → SEVEN_SEG_E 19
SEVEN_SEG_F → SEVEN_SEG_F 7
SEVEN_SEG_G → SEVEN_SEG_G 19
SEVEN_SEG_DP → SEVEN_SEG_DP 19
SEVEN_SEG_MINUS → SEVEN_SEG_MINUS 19

OLED DISPLAY INTERFACE
LCD_DATA[7:0] → LCD_DATA[7:0] 6,18
LCD_CSn → LCD_CSn 18
LCD_RSTn → LCD_RSTn 6
LCD_D_Cn → LCD_D_Cn 18
LCD_WEn → LCD_WEn 18
LCD_E_RDn → LCD_E_RDn 18
LCD_BS1 → LCD_BS1 8
LCD_SERn → LCD_SERn 8

2x16 LED DISPLAY INTERFACE
LCD_EN → LCD_EN 18

HSMC INTERFACE
HSMA_RX_LED → HSMA_RX_LED 18
HSMA_TX_LED → HSMA_TX_LED 18
HSMB_RX_LED → HSMB_RX_LED 18
HSMB_TX_LED → HSMB_TX_LED 18

1.8V
PBSwitch S4 1 2 USER_PB0 R98 10.0K
S3 1 2 USER_PB1 R97 10.0K
S2 1 2 USER_PB2 R95 10.0K
S1 1 2 USER_PB3 R94 10.0K

2.5V
JTAG CHAIN
SW3
1 8 FPGA_BYPASS R138 10.0K
2 7 HSMA_BYPASS R137 10.0K
3 6 HSMB_BYPASS R136 10.0K
4 5 MAX_EN R135 10.0K
TDA04H0SB1

1.8V

SW6 DIP_SW_8
16 1 USER_DIPSW0 RN2H 8 9 10K
15 2 USER_DIPSW1 RN2G 7 10 10K
14 3 USER_DIPSW2 RN2F 6 11 10K
13 4 USER_DIPSW3 RN2E 5 12 10K
12 5 USER_DIPSW4 RN2D 4 13 10K
11 6 USER_DIPSW5 RN2C 3 14 10K
10 7 USER_DIPSW6 RN2B 2 15 10K
9 8 USER_DIPSW7 RN2A 1 16 10K

MAX II CONTROL
SW1 DIP_SW_8
16 1 MWATTS_MAMPS RN1H 8 9 10K
15 2 VOLTS_WATTS RN1G 7 10 10K
14 3 MAX_RESERVE0 RN1F 6 11 10K
13 4 MAX_RESERVE1 RN1E 5 12 10K
12 5 MAX_DIP0 RN1D 4 13 10K
11 6 MAX_DIP1 RN1C 3 14 10K
10 7 MAX_DIP2 RN1B 2 15 10K
9 8 MAX_DIP3 RN1A 1 16 10K

Audio Amp
C39 1.0uF
C41 1.0uF
SP_INp
U16
SHUTDOWN 1 VDD
BYPASS 2 VO2
IN+ 3 VO1
IN- 4 SP_INn GND
LM4990

SPEAKER_OUT R42 100, 1% SPEAKER C44 0.22uF R38 20.0K
R39 20.0K
C48 0.1uF

2.5V
R36
R41 0
DNI R37
J5 HDR4X1
Speaker Header
R40 DNI

2.5V
SW5
R221 1.00k PGM1
R230 1.00k PGM3
C2 2 P2 P4 4 C1
C2 P1 1
P8 8
94HCB16WT
PGM2 R220 1.00k
PGM0 R229 1.00k

Cyclone III Configuration

USB Blaster Programming Header
(uses JTAG mode only)

2.5V

J14
2	1	JTAG_TCK
4	3	JTAG_TDO
6	5	JTAG_TMS
8	7	
10	9	JTAG_TDI

70247-1051

2.5V

R2   1.00k
R1   1.00k

R112 1.00k

FPGA_JTAG_TCK   R197   DNI   C390   DNI

U20M
Cyclone III Configuration

FPGA_nSTATUS	M6	nSTATUS	TCK	P5	FPGA_JTAG_TCK
FPGA_nCONFIG	P4	nCONFIG	TMS	P8	FPGA_JTAG_TMS
FPGA_CONF_DONE	P24	CONF_DONE	TDO	P6	FPGA_JTAG_TDO
			TDI	P7	FPGA_JTAG_TDI
FPGA_DCLK	P3	DCLK			
FPGA_DATA	N7	DATA0	MSEL0	N22	MSEL0
			MSEL1	P23	MSEL1
FPGA_nCE	R8	nCE	MSEL2	M22	MSEL2_3 R163 0
			MSEL3	P22	

2.5V_B5_B6

EP3C120F780

MSEL2_3   R169   DNI

Passive Serial Standard: MSEL[3:0]=0000
Passive Serial Fast: MSEL[3:0]=1100
MSEL pins have internal 5kOhm pull-downs.

CONFIGURATION INTERFACE

FPGA_DATA	FPGA_DATA 8
FPGA_DCLK	FPGA_DCLK 8
FPGA_CONF_DONE	FPGA_CONF_DONE 8,16
FPGA_nSTATUS	FPGA_nSTATUS 8
FPGA_nCONFIG	FPGA_nCONFIG 8

FPGA JTAG INTERFACE

FPGA_JTAG_TCK	FPGA_JTAG_TCK 8,14
FPGA_JTAG_TMS	FPGA_JTAG_TMS 8,14
FPGA_JTAG_TDO	FPGA_JTAG_TDO 8
FPGA_JTAG_TDI	FPGA_JTAG_TDI 8

MAXII JTAG INTERFACE

MAX_JTAG_TCK	MAX_JTAG_TCK 8
MAX_JTAG_TMS	MAX_JTAG_TMS 8
MAX_JTAG_TDO	MAX_JTAG_TDO 8
MAX_JTAG_TDI	MAX_JTAG_TDI 8

MAXII GPIO JTAG

MAXGP_JTAG_TCK	MAXGP_JTAG_TCK 8
MAXGP_JTAG_TMS	MAXGP_JTAG_TMS 8
MAXGP_JTAG_TDO	MAXGP_JTAG_TDO 8
MAXGP_JTAG_TDI	MAXGP_JTAG_TDI 8

HSMC JTAG

| HSMA_JTAG_TDI | HSMA_JTAG_TDI 8,14 |
| HSMB_JTAG_TDI | HSMB_JTAG_TDI 8,14 |

JUMPER STATE TO MAX II

| JTAG_SEL | JTAG_SEL 8 |
| DEV_SEL | DEV_SEL 8 |

2.5V

C13   0.1uF

U3
ANALOG SWITCH

	16	VDD	NC1	2	MAX_JTAG_TCK
JTAG_TCK	4	COM1	NO1	3	FPGA_JTAG_TCK
JTAG_TMS	7	COM2	NC2	5	MAX_JTAG_TMS
			NO2	6	FPGA_JTAG_TMS
JTAG_TDO	9	COM3	NC3	11	MAX_JTAG_TDO
			NO3	10	FPGA_JTAG_TDO
JTAG_TDI	12	COM4	NC4	14	MAX_JTAG_TDI
			NO4	13	FPGA_JTAG_TDI
DEV_SEL	1	SEL	L:COMx=NCx		
	15	EN	H:COMx=NOx		
	8	GND			

TS3A5018

2.5V

C12   0.1uF

U4
ANALOG SWITCH

	16	VDD	NC1	2	MAX_JTAG_TCK
	4	COM1	NO1	3	MAXGP_JTAG_TCK
	7	COM2	NC2	5	MAX_JTAG_TMS
			NO2	6	MAXGP_JTAG_TMS
	9	COM3	NC3	11	MAX_JTAG_TDO
			NO3	10	MAXGP_JTAG_TDO
	12	COM4	NC4	14	MAX_JTAG_TDI
			NO4	13	MAXGP_JTAG_TDI
JTAG_SEL	1	SEL	L:COMx=NCx		
	15	EN	H:COMx=NOx		
	8	GND			

DNI

2.5V

R251	100, 1%	FPGA_CONF_DONE
R164	10.0K	FPGA_nSTATUS
R170	10.0K	FPGA_nCONFIG

R171   10.0K   FPGA_nCE

XJ1   881545-2
XJ2   881545-2

JTAG CYCLONE III OR MAXII SELECT   2.5V

J6
| 1 | DEV_SEL | R34 | 10.0K |
| 2 | | | |

CON2

MAX II JTAG CHAIN OR JTAG PINS SELECT   2.5V

J7
| 1 | JTAG_SEL | R35 | 10.0K |
| 2 | | | |

CON2

JTAG REFERENCE

JUMPER1 will be usede to select between a direct JTAG connection to the FPGA or the MAXII. By default it will select a direct connection to the FPGA.
JUMPER2 will be used to select between configuring with the IP or the MAX II JTAG header. By default it will select to configure with the IP.

JTAG Header

| JTAG_TCK |
| JTAG_TMS |
| JTAG_TDO |
| JTAG_TDI |

JUMPER 1

JUMPER 2

DIP Switch

FPGA_BYPASS
HSMA_BYPASS
HSMB_BYPASS
MAX_EN

MAX II CPLD

GPIO PINS
TCK
TMS
TDI
TDO
OE
IP/JTAG SELECT
FPGA/MAXII SELECT
GPIO PIN
GPIO PIN
GPIO PIN
DEV_OE
GPIO PINS

(2.5V)
| TCK |
| TMS |
| TDI |
| TDO |
FPGA

(2.5V)
| TCK |
| TMS |
| TDI |
| TDO |
| PSNTi |
HSMC Port A

(2.5V)
| TCK |
| TMS |
| TDI |
| TDO |
| PSNTi |
HSMC Port B

USB CONFIG

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Cyclone III Banks 1, 2, 5 & 6

U20A — Cyclone III, Bank 1A
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

U20B — Cyclone III, Bank 2
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

U20N — Cyclone III, Bank 1B
EP3C120 (EP3C80/EP3C55/EP3C40)
EP3C120F780

U20O — Cyclone III, Bank 5B
EP3C120 (EP3C80/EP3C55/EP3C40)
EP3C120F780

U20E — Cyclone III, Bank 5A
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

U20F — Cyclone III, Bank 6A
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

U20P — Cyclone III, Bank 6B
EP3C120 (EP3C80/EP3C55/EP3C40)
EP3C120F780

HSMC PORT A
HSMA_SDA 14
HSMA_SCL 14
HSMA_CLK_OUT0 14
HSMA_RX_LED 16
HSMA_TX_LED 16
HSMA_CLK_OUT_P[2:1] 14
HSMA_CLK_OUT_N[2:1] 14
HSMA_D[3:0] 14
HSMA_TX_D_P[16:0] 6,14
HSMA_TX_D_N[16:0] 14
HSMA_RX_D_P[16:0] 14,15
HSMA_RX_D_N[16:0] 14,15

HSMC PORT B
HSMB_SCL 14
HSMB_SDA 14
HSMB_RX_LED 16
HSMB_TX_LED 16
HSMB_CLK_OUT_P[2:1] 14
HSMB_CLK_OUT_N[2:1] 14
HSMB_D[3:0] 14
HSMB_TX_D_P[16:0] 6,14
HSMB_TX_D_N[16:0] 14
HSMB_RX_D_P[16:0] 14,15
HSMB_RX_D_N[16:0] 14,15

ETHERNET INTERFACE
ENET_TXD[3:0] 13
ENET_RXD[3:0] 6,13
ENET_TX_EN 13
ENET_RESETn 13
ENET_LED_LINK1000 13

USB 2.0 INTERFACE
USB_FD[7:0] 6,8
USB_CMD_DATA 8
USB_REN 8
USB_WEN 8
USB_EMPTY 8
USB_FULL 8
SPEAKER_OUT 16

OLED DISPLAY INTERFACE
LCD_DATA[7:0] 6,16
LCD_CSn 16
LCD_D_Cn 16
LCD_WEn 16
LCD_E_RDn 16

2x16 LED DISPLAY INTERFACE
LCD_EN 16

USER I/O
CPU_RESETn 8,16

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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Cyclone III Banks 3, 4, 7 & 8

U20C — Cyclone III, Bank 3
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

U20D — Cyclone III, Bank 4
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

U20R — Cyclone III, Bank 8B
EP3C120 (EP3C80/EP3C55/EP3C40)
EP3C120F780

U20G — Cyclone III, Bank 7A
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

U20Q — Cyclone III, Bank 7B
EP3C120 (EP3C80/EP3C55/EP3C40)
EP3C120F780

U20H — Cyclone III, Bank 8A
EP3C120 (EP3C80 / EP3C55 / EP3C40)
EP3C120F780

SEVEN-SEG INTERFACE

SEVEN_SEG_SEL[4:1] SEVEN_SEG_SEL[4:1] 7,16
SEVEN_SEG_A   SEVEN_SEG_A 16
SEVEN_SEG_B   SEVEN_SEG_B 16
SEVEN_SEG_C   SEVEN_SEG_C 16
SEVEN_SEG_D   SEVEN_SEG_D 16
SEVEN_SEG_E   SEVEN_SEG_E 16
SEVEN_SEG_F   SEVEN_SEG_F 16
SEVEN_SEG_G   SEVEN_SEG_G 16
SEVEN_SEG_MINUS   SEVEN_SEG_MINUS 16
SEVEN_SEG_DP   SEVEN_SEG_DP 16

MAX_OEn   MAX_OEn 8
MAX_WEn   MAX_WEn 8
MAX2_CLK   MAX2_CLK 8

SHARED BUS

FSD[31:0]   FSD[31:0] 6,8,11
FSA[24:0]   FSA[24:0] 7,8,11

FLASH INTERFACE

FLASH_WEn   FLASH_WEn 8,11
FLASH_RDYBSYn   FLASH_RDYBSYn 8,11

DDR2 INTERFACE

DDR2BOT_A[15:0]   DDR2BOT_A[15:0] 7,9,10
DDR2BOT_BA[2:0]   DDR2BOT_BA[2:0] 9,10
DDR2TOP_A[15:0]   DDR2TOP_A[15:0] 6,7,9,10
DDR2TOP_BA[2:0]   DDR2TOP_BA[2:0] 9,10

DDR2BOT_CASn   DDR2BOT_CASn 9,10
DDR2BOT_WEn   DDR2BOT_WEn 9,10
DDR2BOT_CSn   DDR2BOT_CSn 9,10
DDR2BOT_ODT   DDR2BOT_ODT 9,10
DDR2BOT_CKE   DDR2BOT_CKE 9,10

DDR2TOP_RASn   DDR2TOP_RASn 9,10
DDR2TOP_CASn   DDR2TOP_CASn 9,10
DDR2TOP_WEn   DDR2TOP_WEn 9,10
DDR2TOP_CSn   DDR2TOP_CSn 9,10
DDR2TOP_ODT   DDR2TOP_ODT 9,10
DDR2TOP_CKE   DDR2TOP_CKE 9,10
DDR2TOP_ACTIVE   DDR2TOP_ACTIVE 9

DDR2_CK_P[2:0]   DDR2_CK_P[2:0] 9
DDR2_CK_N[2:0]   DDR2_CK_N[2:0] 9
DDR2_DM[8:0]   DDR2_DM[8:0] 9,10
DDR2_DQ[71:0]   DDR2_DQ[71:0] 9,10
DDR2_DQS[8:0]   DDR2_DQS[8:0] 9,10

PSRAM INTERFACE

SRAM_BEn[3:0]   SRAM_BEn[3:0] 11
SRAM_CLK   SRAM_CLK 11
SRAM_CSn   SRAM_CSn 8,11
SRAM_ADVn   SRAM_ADVn 11
SRAM_OEn   SRAM_OEn 11
SRAM_PSn   SRAM_PSn 11
SRAM_WAIT0   SRAM_WAIT0 7,11
SRAM_WAIT1   SRAM_WAIT1 11
SRAM_WEn   SRAM_WEn 11

USER I/O's

USER_PB[3:0]   USER_PB[3:0] 6,16
USER_DIPSW[7:0]   USER_DIPSW[7:0] 16
USER_LED[7:0]   USER_LED[7:0] 16

1.8V_B3_B4
R195 49.9 RUP2
R196 49.9 RDN2

1.8V_B7_B8
R145 49.9 RUP4
R146 49.9 RDN4

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Decoupling

1.2V_INT

C54 470uF 10V Tantalum	C40 470uF 10V Tantalum	C308 2.2nF	C321 2.2nF	C330 2.2nF	C322 2.2nF	C323 2.2nF	C340 2.2nF	C288 3.3nF	C303 3.3nF	C313 3.3nF	C333 3.3nF	C344 3.3nF	C359 3.3nF
C348 0.01uF	C287 0.01uF	C314 0.01uF	C326 0.01uF	C366 0.01uF	C301 4.7nF	C278 4.7nF	C320 4.7nF	C302 4.7nF	C331 4.7nF	C357 4.7nF	C310 4.7nF	C284 4.7nF	C338 4.7nF	C324 4.7nF
C291 0.01uF	C354 0.01uF	C345 0.01uF	C325 0.01uF	C296 0.01uF	C297 0.01uF	C289 0.01uF	C360 0.01uF	C343 0.01uF	C290 0.01uF	C334 0.01uF	C346 0.01uF	C312 0.01uF	C315 0.01uF	C305 0.01uF	C368 0.01uF
C285 22nF	C295 22nF	C352 22nF	C341 22nF	C365 22nF	C364 22nF	C339 22nF	C280 22nF	C332 22nF	C286 47nF	C342 47nF	C358 47nF	C311 47nF	C361 100nF	C328 100nF	C292 100nF
C327 0.1uF	C347 0.1uF	C298 0.1uF	C335 0.1uF	C316 0.1uF	C317 0.1uF	C299 0.1uF	C275 1.0uF	C274 1.0uF	C367 1.0uF	C369 1.0uF	C355 1.0uF	C349 1.0uF	C336 1.0uF	C318 1.0uF	C306 1.0uF

1.2V

| C61 470uF 10V Tantalum | C420 2.2nF | C435 3.3nF | C464 4.7nF | C446 0.01uF |

1.8V

| C60 470uF 10V Tantalum | C422 1.0nF | C409 1.0nF | C423 1.0nF | C438 1.0nF | C394 1.0nF | C251 1.0nF | C250 1.0nF | C439 1.0nF | C403 1.0nF | C161 1.0nF | C214 1.0nF | C434 1.0nF |
| | C20 1.0uF | C53 1.0uF | C447 100uF | C31 100uF | C52 100uF |

1.8V_B3_B4

| C59 470uF 10V Tantalum | C371 1.0nF | C377 1.0nF | C374 1.0nF | C380 1.0nF | C372 1.0nF | C376 1.0nF | C381 1.0nF | C404 2.2nF | C387 2.2nF | C385 2.2nF | C416 2.2nF | C375 2.2nF | C392 2.2nF | C424 2.2nF |
| | C370 4.7nF | C432 4.7nF | C417 4.7nF | C433 0.01uF | C453 0.01uF | C440 0.01uF | C393 22nF | C391 47nF | C386 0.1uF | C452 0.1uF | C450 1.0uF | C448 100uF |

3.3V

C24 470uF 10V Tantalum	C62 470uF 10V Tantalum	C170 2.2nF	C91 2.2nF	C437 2.2nF	C194 2.2nF	C480 2.2nF	C133 2.2nF	C141 3.3nF	C98 3.3nF	C466 3.3nF	C436 3.3nF	C491 3.3nF	C168 3.3nF
C135 4.7nF	C103 4.7nF	C139 4.7nF	C460 4.7nF	C465 4.7nF	C140 47nF	C99 47nF	C112 47nF	C488 0.47uF	C119 0.47uF	C88 0.47uF	C173 0.47uF	C122 0.47uF
C120 0.01uF	C121 0.01uF	C118 0.01uF	C238 0.01uF	C92 0.01uF	C155 0.01uF	C134 0.01uF	C477 0.01uF	C485 0.01uF	C225 0.01uF	C463 0.01uF	C461 0.01uF	C100 0.01uF	C101 0.01uF	C85 0.01uF
C487 0.01uF	C489 0.01uF	C90 0.01uF	C171 0.1uF	C123 0.1uF	C111 0.1uF	C493 0.1uF	C482 0.1uF	C172 0.1uF	C95 0.1uF	C174 0.1uF	C23 0.1uF	C32 0.1uF	C65 1.0uF	C18 1.0uF
C102 22nF	C104 22nF	C492 22nF	C249 22nF	C483 22nF	C462 22nF	C467 22nF	C110 22nF	C113 22nF	C421 22nF	C176 22nF	C169 22nF	C21 100uF	C63 100uF

2.5V

| C154 1.0nF | C190 1.0nF | C496 1.0nF | C114 2.2nF | C495 2.2nF | C494 4.7nF | C189 100uF |

2.5V_B5_B6

| C293 2.2nF | C307 4.7nF | C329 0.01uF | C350 0.1uF | C276 100uF |

2.5V_B1_B2

| C294 2.2nF | C309 4.7nF | C353 0.01uF | C279 0.1uF | C384 100uF |

1.2V_VCCD

| C272 2.2nF | C382 4.7nF | C373 0.01uF | C267 0.01uF | C263 0.1uF | C362 0.1uF | C383 0.1uF | C281 0.1uF | C273 0.1uF | C388 4.7uF | C304 470uF 10V Tantalum |

2.5V_VCCA

| C337 1.0nF | C300 2.2nF | C379 2.2nF | C356 4.7nF | C319 0.01uF | C268 22nF | C282 0.1uF | C55 4.7uF | C56 47uF |

1.8V_B7_B8

| C33 470uF 10V Tantalum | C256 1.0nF | C252 1.0nF | C262 1.0nF | C271 1.0nF | C258 1.0nF | C266 1.0nF | C270 1.0nF | C196 2.2nF | C260 2.2nF | C259 2.2nF | C254 2.2nF | C255 2.2nF | C253 2.2nF | C269 2.2nF |
| C215 4.7nF | C264 4.7nF | C162 4.7nF | C208 0.01uF | C188 0.01uF | C163 0.01uF | C195 22nF | C180 47nF | C181 0.1uF | C151 0.1uF | C261 1.0uF | C152 100uF |

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