



# **Cyclone III Development Board**

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## **Reference Manual**



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## Introduction

This document describes the hardware features of the Cyclone® III development board, including detailed pin-out information to enable you to create custom FPGA designs that interface with all components of the board.



For information about setting up and powering up the Cyclone III development board and using the kit's demo software, refer to the *Cyclone III Development Kit User Guide*.

## General Description

The Cyclone® III development board provides a hardware platform for developing and prototyping low-power, high-volume, and feature-rich designs as well as to demonstrate the Cyclone III device's on-chip memory, embedded multipliers, and the Nios® II embedded processor.

With up to 4 Mbits of embedded memory and 288 embedded 18-bit × 18-bit multipliers, the Cyclone III device supplies internal memory while also providing external support for high-speed, low-latency memory access via dual-channel DDR SDRAM and low-power SRAM.

Built on TSMC's 65-nm low-power process technology, Cyclone III devices are designed to provide low static and dynamic power consumption. Additionally, with the support of the Quartus® II software's PowerPlay technology, designs are automatically optimized for power consumption. Therefore, the Cyclone III development board provides a power-optimized, integrated solution for memory-intensive, high-volume applications.

Accordingly, the Cyclone III development board is especially suitable for wireless, video and image processing, and other high-bandwidth, parallel processing applications. Through the use of Altera®-provided video and image intellectual property (or other MegaCore® functions) and board expansion connectors, you can enable the inter-operability of the Cyclone III device, allowing application-specific customization of the development board.



For more information about the Altera Video and Image Processing Suite MegaCore functions, refer to the *Video and Image Processing Suite User Guide*.

To get you started, Altera provides application-specific design examples. The pre-built and tested design examples allow you to:

- Create a Cyclone III FPGA design in an hour
- View Cyclone III FPGA power measurement examples
- Design a 32-bit soft processor system inside the Cyclone III FPGA in an hour

The Cyclone III development board has the following main features:

- High logic density to implement more functions and features
- Embedded memory for high-bandwidth applications
- Expandable through two Altera High-Speed Mezzanine Card (HSMC) connectors
- 256-MB of dual channel DDR2 SDRAM with a 72-bit data width
- Supports high-speed external memory interfaces including dual-channel DDR SDRAM and low-power SRAM
- Four user push-button switches
- Eight user LEDs
- Power consumption display

The Cyclone III development board provides the following advantages:

- Unique combination of low-cost, low-power Cyclone III FPGA that supports high-volume, memory-intensive designs
- Highest multiplier-to-logic ratio FPGA in the industry
- Lowest cost, density- and power-optimized FPGA
- Quartus II development software's power optimization tools

## Board Component Blocks

The board features the following major component blocks:

- 780-pin Altera Cyclone III EP3C120 FPGA in a BGA package
  - 119K logic elements (LEs)
  - 3,888 Kbits of memory
  - 288  $18 \times 18$  multiplier blocks
  - Four phase locked loops (PLLs)
  - 20 global clock networks
  - 531 user I/Os
  - 1.2-V core power
- 256-pin Altera MAX<sup>®</sup> II EPM2210G CPLD in a FineLine Ball Grid Array (FBGA) package
  - 1.8-V core power
- On-board memory
  - 256-MB dual-channel DDR2 SDRAM
  - 8-MB SRAM
  - 64-MB flash memory

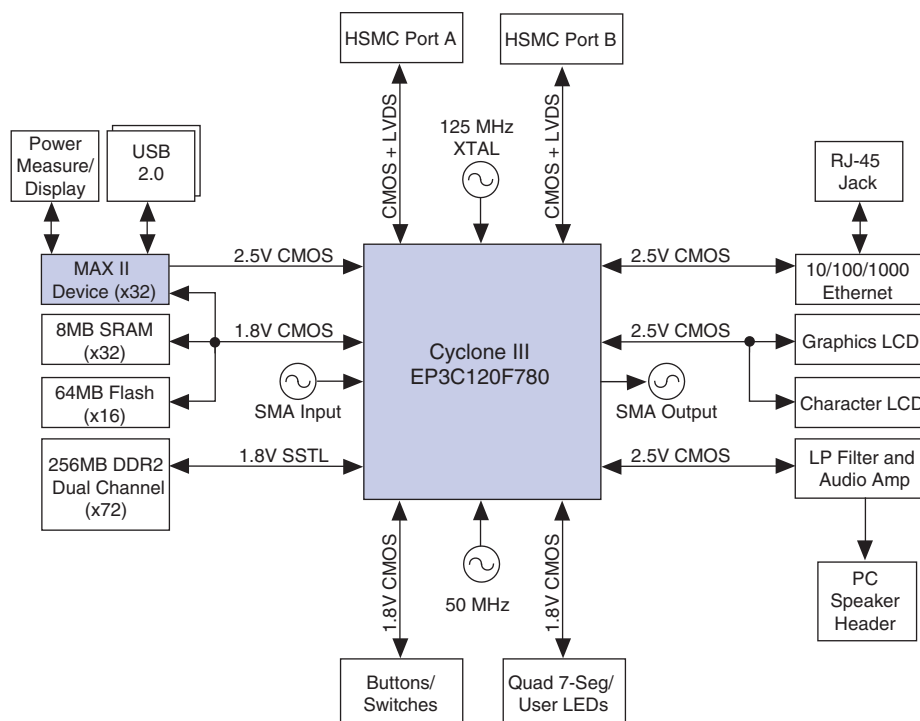
- FPGA configuration circuitry
  - MAX II CPLD and flash passive serial configuration
  - On-board USB-Blaster™ circuitry using the Quartus II Programmer
- On-board clocking circuitry
  - Two clock oscillators to support Cyclone III device user logic
    - 50 MHz
    - 125 MHz
  - 80 I/O, 6 clocks, SMBus, and JTAG
  - SMA connector for external clock input and output
- General user and configuration interfaces
  - LEDs/displays:
    - Eight user LEDs
    - One transmit/receive LED (TX/RX) per HSMC interface
    - One configuration done LED
    - Ethernet LEDs
    - User 7-segment display
    - Power consumption display
  - Memory activity LEDs:
    - SRAM
    - FLASH
    - DDR2 Top
    - DDR2 Bottom
  - Push-buttons:
    - One user reset push-button (CPU reset)
    - Four general user push-buttons
    - One system reset push-button (user configuration)
    - One factory push-button switch (factory configuration)
  - DIP switches:
    - One MAX control DIP switch
    - One JTAG control switch
    - Eight user DIP switches
    - Speaker header
- Displays
  - 128 × 64 graphics LCD
  - 16 × 2 line character LCD

- Power supply
  - 14 V – 20 V DC input
  - On-board power measurement circuitry
  - Up to 19.8 W per HSMC interface
- Mechanical
  - 6" × 8" board
  - Bench-top design

## Block Diagram

Figure 1-1 shows the functional block diagram of the Cyclone III development board.

**Figure 1-1.** Cyclone III Development Board Block Diagram



## Handling the Board

When handling the board, it is important to observe the following precaution:



**Static Discharge Precaution:** Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precaution when touching the board.



### Introduction

This chapter introduces all the important components on the Cyclone III development board. [Figure 2-1](#) illustrates all component locations and [Table 2-1](#) describes component features.

The chapter is divided into the following sections:

- “Featured FPGA (U20)” on page 2-4
- “MAX II CPLD” on page 2-6
- “Configuration, Status, and Setup Elements” on page 2-14
- “Clocking Circuitry” on page 2-22
- “General User Interfaces” on page 2-25
- “Communication Ports and Interface Cards” on page 2-36
- “On-Board Memory” on page 2-47
- “Power Supply” on page 2-62
- “Statement of China-RoHS Compliance” on page 2-64



A complete set of board schematics, a physical layout database, and GERBER files for the Cyclone III development board are installed in the Cyclone III Development Kit documents directory.



For information about powering up the development board and installing the demo software, refer to the [Cyclone III Development Kit User Guide](#).

### Board Overview

This section provides an overview of the Cyclone III development board, including an annotated board image and component descriptions.

[Figure 2-1](#) shows the top view of the Cyclone III development board.

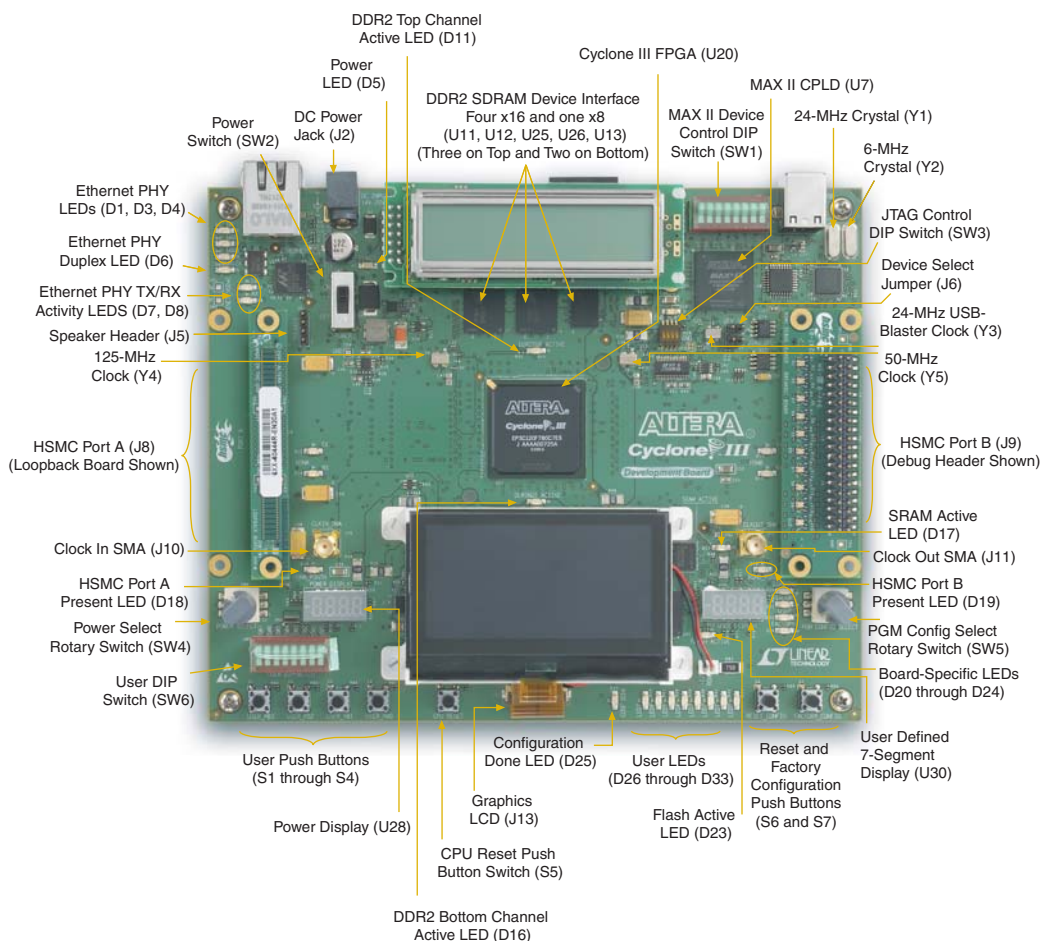
**Figure 2–1.** Top View of the Cyclone III Development Board

Table 2–1 describes the components and lists their corresponding board references.

**Table 2–1.** Cyclone III Development Board (Part 1 of 3)

| Board Reference                                | Type                           | Description  |
|--|--------------------------------|--|
| <b>Featured Devices</b>                        |                                |  |
| U20  | FPGA                           | EP3C120, 780-pin FineLine BGA package.   |
| U7   | CPLD                           | EPM2210G, 256-pin device in a FineLine BGA package.  |
| <b>Configuration Status and Setup Elements</b> |                                |  |
| J6   | Device select (DEV_SEL) jumper | Sets target device for JTAG signals when using an external USB-Blaster or equivalent.            |
| J3   | Input                          | Type B USB connector that allows for connecting a Type A-B USB cable between a PC and the board. |
| D20 through D24                                | User LEDs                      | Board-specific configuration green LEDs.   |
| D25  | Configuration done LED         | Green LED that illuminates when the FPGA is successfully configured.                             |
| D12 through D15                                | Channel activity LEDs          | Green LEDs that indicate the RX and TX activity on the HSMC Ports A or B.                        |
| J5   | Header                         | Speaker header.  |

**Table 2–1.** Cyclone III Development Board (Part 2 of 3)

| Board Reference                      | Type   | Description   |
|--------------------------------------|--|---|
| D1, D3, D4                           | Ethernet PHY LEDs                            | Green Ethernet PHY LEDs. Illuminate when Ethernet PHY is using the 10/100/1000 Mbps (D1, D3, D4) connection speeds. |
| D6                                   | Duplex Ethernet PHY LED                      | Green Ethernet PHY LED. Illuminates when Ethernet PHY is both sending and receiving data.                           |
| D5                                   | Power LED                                    | Blue LED indicates when power is applied to the board.  |
| D7, D8                               | Ethernet PHY transmit/receive activity LEDs  | Green LED. Illuminates when transmit/receive data is active from the Ethernet PHY.                                  |
| SW1                                  | MAX II device control DIP switch             | Controls various features specific to the Cyclone III development board.  |
| SW3                                  | JTAG control switch                          | JTAG control DIP switch used to remove or include devices in the active JTAG chain.                                 |
| D17                                  | SRAM active                                  | SRAM active LED. Illuminates when the SRAM device is accessed.  |
| D23                                  | Flash active                                 | Flash active LED. Illuminates when the flash device is accessed.  |
| U28                                  | Power display                                | Displays power measured by the MAX II CPLD.   |
| D16                                  | DDR2 LED                                     | Indicates that the DDR2 top devices are active.   |
| D11                                  | DDR2 LED                                     | Indicates that the DDR2 bottom devices are active.  |
| <b>Clock Circuitry</b>               |  |   |
| Y4                                   | 125 MHz                                      | 125-MHz clock oscillator used for the system clock.   |
| Y5                                   | 50 MHz                                       | 50-MHz clock oscillator used for data processing.   |
| Y1                                   | 24-MHz crystal                               | Cypress USB PHY.  |
| Y2                                   | 6-MHz crystal                                | USB PHY FTDI reference clock.   |
| Y3                                   | 24 MHz                                       | MAX II device clock.  |
| J10                                  | SMA clock input                              | SMA connector that allows the provision of an external clock input.   |
| J11                                  | SMA clock output                             | SMA connector that allows the provision of an external clock output.  |
| <b>General User Input and Output</b> |  |   |
| S1 through S4                        | User push buttons                            | Four 1.8-V push-button switches for user-defined, logic inputs.   |
| S5                                   | CPU reset push button                        | One 1.8-V push-button switch for FPGA logic and CPU reset.  |
| S6 and S7                            | Reset and factory configuration push buttons | Two 1.8-V push-button switches that control FPGA configuration from flash memory.                                   |
| D26 through D33                      | User LEDs                                    | Eight user-defined LEDs.  |
| SW5                                  | PGM CONFIG SELECT                            | Rotary switch to select which FPGA configuration file to use in flash memory.                                       |
| SW4                                  | Power select rotary switch                   | Power rail select for on-board power monitor.   |
| U30                                  | User display                                 | User-defined, green 7-segment display.  |
| J4                                   | Character LCD                                | 14-pin LCD display.   |
| J13                                  | Graphics LCD                                 | 30-position dot matrix graphics LCD display.  |
| <b>Memory</b>                        |  |   |
| U31                                  | Flash  | 64 MB of flash memory with a 16-bit data bus.   |

**Table 2-1.** Cyclone III Development Board (Part 3 of 3)

| Board Reference                  | Type                   | Description   |
|----------------------------------|------------------------|---|
| U23 and U24                      | SRAM                   | The SRAM devices connect to the MAX II device as well as the flash memory device.   |
| U11, U12, U13, U25, U26          | DDR2 SDRAM             | Four ×16 devices and a single ×8 device.  |
| <b>Components and Interfaces</b> |                        |   |
| U6                               | USB device             | USB device that provides JTAG programming of on-board devices, including the Cyclone III device and flash memory device.                                    |
| U3                               | Ethernet cable jack    | The RF-45 jack is for Ethernet cable connection. The connector is fed by a 10/100/1000 base T PHY device with an RGMII interface to the Cyclone III device. |
| J8, J9                           | HSMC Port A and Port B | High-speed mezzanine header allows for the connection of HSMC daughter cards.   |
| <b>Power Supply</b>              |                        |   |
| J2                               | DC power jack          | 14–20 V DC power source.  |
| SW2                              | Input                  | Switches the board's power on and off.  |

## Featured FPGA (U20)

The Cyclone III Development Kit features the EP3C120F780 device (U20) in a 780-pin BGA package.



For more information about Cyclone III devices, refer to the *Cyclone III Device Handbook*.

Table 2-2 lists the main Cyclone III device features.

**Table 2-2.** Cyclone III Device Features

| Feature               | Quantity |
|-----------------------|----------|
| Logic elements        | 119,088  |
| Memory (Kbits)        | 3,888    |
| Multipliers           | 288      |
| PLLs                  | 4        |
| Global clock networks | 20       |

Table 2-3 lists the Cyclone III component reference and manufacturing information.

**Table 2-3.** Cyclone III Component Reference and Manufacturing Information

| Board Reference | Description             | Manufacturer       | Manufacturing Part Number | Manufacturer Website                               |
|-----------------|-------------------------|--------------------|---------------------------|--|
| U20             | Memory rich FPGA device | Altera Corporation | EP3C120F780               | <a href="http://www.altera.com">www.altera.com</a> |

Table 2–4 lists the Cyclone III EP3C120F780C7 device pin count.

**Table 2–4.** Cyclone III Device Pin Count

| Function                        | I/O Type                 | I/O Count | Special Pins  |
|---------------------------------|--------------------------|-----------|---|
| Oscillators and SMAs            | 1.8-V CMOS               | 4         | Three clock inputs, one output                        |
| DDR2                            | 1.8-V SSTL               | 148       | Nine data strobe signal (DQS), 10 V <sub>REF</sub>    |
| Flash/SRAM/MAX                  | 1.8-V CMOS               | 78        | —   |
| Horizontal bank OCT calibration | 1.8-V CMOS               | 4         | 2 Rup, 2 Rdn  |
| Vertical bank OCT calibration   | 2.5-V CMOS               | 4         | 2 Rup, 2 Rdn  |
| Passive serial configuration    | 2.5-V CMOS               | 2         | DATA0, DCLK   |
| Ethernet                        | 2.5-V CMOS               | 16        | 1 clock input   |
| Buttons, Switches, LEDs         | 1.8-V CMOS               | 34        | DEV_CLR   |
| Character LCD, Graphics LCD     | 2.5-V CMOS               | 14        | —   |
| Speaker header                  | 2.5-V CMOS               | 1         | —   |
| USB                             | 2.5-V CMOS               | 14        | 1 clock input   |
| HSMC Port A                     | 2.5-V CMOS<br>2.5-V LVDS | 86        | 5 clock inputs<br>(1 single-ended,<br>2 differential) |
| HSMC Port B                     | 2.5-V CMOS<br>2.5-V LVDS | 86        | 5 clock inputs<br>(1 single-ended,<br>2 differential) |
| Device I/O total: 491           |                          |           |   |

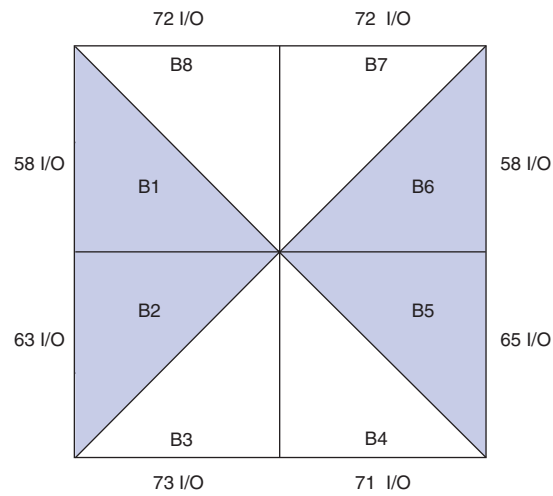


For additional information about Altera devices, go to [www.altera.com/products/devices](http://www.altera.com/products/devices).

## I/O and Clocking Resources

This section lists specific I/O and clocking resources available with the EP3C120F780C7 device, which is the largest of the Cyclone III devices.

Figure 2–2 illustrates the available I/O bank resources on the EP3C120F780C7 device.

**Figure 2–2.** Cyclone III Device I/O Bank Resources

## MAX II CPLD

The board utilizes an Altera MAX II CPLD for the following purposes:

- Power-up configuration of the FPGA from flash memory
- Embedded USB-Blaster core for USB-based configuration of the FPGA
- Power consumption monitoring and display

Additionally, the MAX II device is also used to help dual-footprint the FTDI and Cypress USB devices. Each device has a shared path between the USB device and the MAX II CPLD. The individual paths then drive to the FPGA separately. [Figure 2–3](#) illustrates the MAX II device's block diagram.

**Figure 2-3.** MAX II Device's Block Diagram

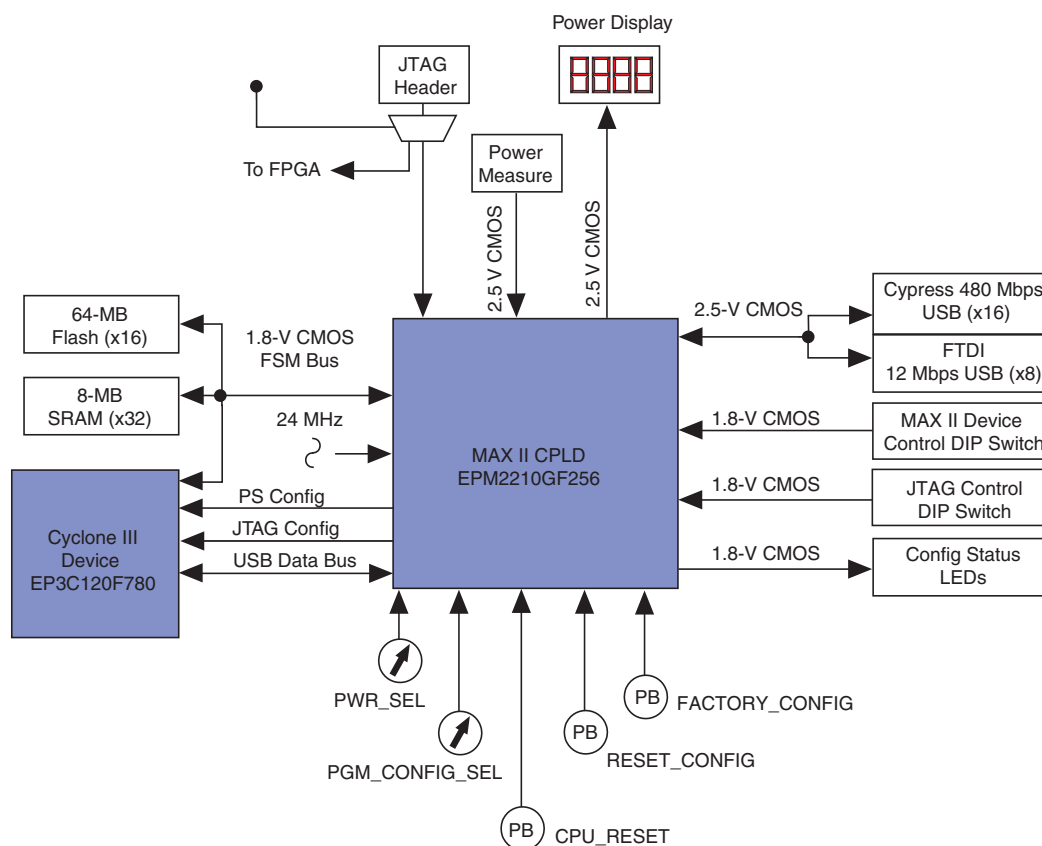


Table 2-5 lists the I/O signals present on the MAX II CPLD. The signal name and function are relative to the MAX II device.

**Table 2-5.** MAX II Device Pin-Out (Note 1) (Part 1 of 8)

| MAX II Pin Number | I/O Standard | Signal Direction | Schematic Signal Name |
|-------------------|--------------|------------------|-----------------------|
| P3                | —            | Input            | TCK                   |
| L6                | —            | Input            | TDI                   |
| M5                | —            | Output           | TDO                   |
| N4                | —            | Input            | TMS                   |
| C14               | 1.8 V        | Output           | CLKIN_125_EN          |
| J12               | 1.8 V        | Input            | CLKIN_24              |
| E13               | 1.8 V        | Output           | CLKIN_50_EN           |
| M9                | 1.8 V        | Input            | CPU_RESETh            |
| F11               | 1.8 V        | Input            | DEV_SEL               |
| A10               | 2.5 V        | Input            | FACTORY_CONFIGh       |
| G13               | 1.8 V        | Output           | FLASH_ACTIVE          |
| L15               | 1.8 V        | Output           | FLASH_BYTEh           |
| K14               | 1.8 V        | Output           | FLASH_CEn             |

**Table 2-5.** MAX II Device Pin-Out (*Note 1*) (Part 2 of 8)

| MAX II Pin Number | I/O Standard | Signal Direction | Schematic Signal Name |
|-------------------|--------------|------------------|-----------------------|
| M16               | 1.8 V        | Output           | FLASH_OEn             |
| L11               | 1.8 V        | Input            | FLASH_RDYBSYn         |
| M15               | 1.8 V        | Output           | FLASH_RESETh          |
| L12               | 1.8 V        | Output           | FLASH_WEn             |
| J16               | 1.8 V        | Input            | FPGA_BYPASS           |
| E3                | 2.5 V        | Input            | FPGA_CONF_DONE        |
| D3                | 2.5 V        | Output           | FPGA_DATA             |
| C2                | 2.5 V        | Output           | FPGA_DCLK             |
| N3                | 2.5 V        | Input            | FPGA_JTAG_TCK         |
| N1                | 2.5 V        | Output           | FPGA_JTAG_TDI         |
| N2                | 2.5 V        | Input            | FPGA_JTAG_TDO         |
| P2                | 2.5 V        | Input            | FPGA_JTAG_TMS         |
| E4                | 2.5 V        | Output           | FPGA_nCONFIG          |
| C3                | 2.5 V        | Input            | FPGA_nSTATUS          |
| N9                | 1.8 V        | Output           | FSA [0]               |
| T8                | 1.8 V        | Output           | FSA [1]               |
| N10               | 1.8 V        | Output           | FSA [10]              |
| R11               | 1.8 V        | Output           | FSA [11]              |
| P10               | 1.8 V        | Output           | FSA [12]              |
| T12               | 1.8 V        | Output           | FSA [13]              |
| M11               | 1.8 V        | Output           | FSA [14]              |
| R12               | 1.8 V        | Output           | FSA [15]              |
| N11               | 1.8 V        | Output           | FSA [16]              |
| T13               | 1.8 V        | Output           | FSA [17]              |
| P11               | 1.8 V        | Output           | FSA [18]              |
| R13               | 1.8 V        | Output           | FSA [19]              |
| T9                | 1.8 V        | Output           | FSA [2]               |
| M12               | 1.8 V        | Output           | FSA [20]              |
| R14               | 1.8 V        | Output           | FSA [21]              |
| N12               | 1.8 V        | Output           | FSA [22]              |
| T15               | 1.8 V        | Output           | FSA [23]              |
| P12               | 1.8 V        | Output           | FSA [24]              |
| R9                | 1.8 V        | Output           | FSA [3]               |
| P9                | 1.8 V        | Output           | FSA [4]               |
| T10               | 1.8 V        | Output           | FSA [5]               |
| K16               | 1.8 V        | Output           | FSA [6]               |
| R10               | 1.8 V        | Output           | FSA [7]               |
| M10               | 1.8 V        | Output           | FSA [8]               |
| T11               | 1.8 V        | Output           | FSA [9]               |



**Table 2-5.** MAX II Device Pin-Out *(Note 1)* (Part 3 of 8)

| MAX II Pin Number | I/O Standard | Signal Direction | Schematic Signal Name |
|-------------------|--------------|------------------|-----------------------|
| P4                | 1.8 V        | Bidirectional    | FSD [0]               |
| R1                | 1.8 V        | Bidirectional    | FSD [1]               |
| M6                | 1.8 V        | Bidirectional    | FSD [10]              |
| R5                | 1.8 V        | Bidirectional    | FSD [11]              |
| P7                | 1.8 V        | Bidirectional    | FSD [12]              |
| T5                | 1.8 V        | Bidirectional    | FSD [13]              |
| N7                | 1.8 V        | Bidirectional    | FSD [14]              |
| R6                | 1.8 V        | Bidirectional    | FSD [15]              |
| M7                | 1.8 V        | Bidirectional    | FSD [16]              |
| T6                | 1.8 V        | Bidirectional    | FSD [17]              |
| J15               | 1.8 V        | Bidirectional    | FSD [18]              |
| R7                | 1.8 V        | Bidirectional    | FSD [19]              |
| P5                | 1.8 V        | Bidirectional    | FSD [2]               |
| P8                | 1.8 V        | Bidirectional    | FSD [20]              |
| T7                | 1.8 V        | Bidirectional    | FSD [21]              |
| N8                | 1.8 V        | Bidirectional    | FSD [22]              |
| R8                | 1.8 V        | Bidirectional    | FSD [23]              |
| F12               | 1.8 V        | Bidirectional    | FSD [24]              |
| D16               | 1.8 V        | Bidirectional    | FSD [25]              |
| F13               | 1.8 V        | Bidirectional    | FSD [26]              |
| D15               | 1.8 V        | Bidirectional    | FSD [27]              |
| F14               | 1.8 V        | Bidirectional    | FSD [28]              |
| D14               | 1.8 V        | Bidirectional    | FSD [29]              |
| T2                | 1.8 V        | Bidirectional    | FSD [3]               |
| E12               | 1.8 V        | Bidirectional    | FSD [30]              |
| C15               | 1.8 V        | Bidirectional    | FSD [31]              |
| N5                | 1.8 V        | Bidirectional    | FSD [4]               |
| R3                | 1.8 V        | Bidirectional    | FSD [5]               |
| P6                | 1.8 V        | Bidirectional    | FSD [6]               |
| R4                | 1.8 V        | Bidirectional    | FSD [7]               |
| N6                | 1.8 V        | Bidirectional    | FSD [8]               |
| T4                | 1.8 V        | Bidirectional    | FSD [9]               |
| F7                | GNDINT       | Gnd              | —                     |
| G6                | GNDINT       | Gnd              | —                     |
| H7                | GNDINT       | Gnd              | —                     |
| H9                | GNDINT       | Gnd              | —                     |
| J8                | GNDINT       | Gnd              | —                     |
| J10               | GNDINT       | Gnd              | —                     |
| K11               | GNDINT       | Gnd              | —                     |

**Table 2-5.** MAX II Device Pin-Out (*Note 1*) (Part 4 of 8)

| MAX II Pin Number | I/O Standard | Signal Direction | Schematic Signal Name |
|-------------------|--------------|------------------|-----------------------|
| L10               | GNDINT       | Gnd              | —                     |
| A1                | GNDIO        | Gnd              | —                     |
| A16               | GNDIO        | Gnd              | —                     |
| B2                | GNDIO        | Gnd              | —                     |
| B15               | GNDIO        | Gnd              | —                     |
| G7                | GNDIO        | Gnd              | —                     |
| G8                | GNDIO        | Gnd              | —                     |
| G9                | GNDIO        | Gnd              | —                     |
| G10               | GNDIO        | Gnd              | —                     |
| K7                | GNDIO        | Gnd              | —                     |
| K8                | GNDIO        | Gnd              | —                     |
| K9                | GNDIO        | Gnd              | —                     |
| K10               | GNDIO        | Gnd              | —                     |
| R2                | GNDIO        | Gnd              | —                     |
| R15               | GNDIO        | Gnd              | —                     |
| T1                | GNDIO        | Gnd              | —                     |
| T16               | GNDIO        | Gnd              | —                     |
| J13               | 1.8 V        | Input            | HSMA_BYPASS           |
| M4                | 2.5 V        | Output           | HSMA_JTAG_TDI         |
| K4                | 2.5 V        | Input            | HSMA_JTAG_TDO         |
| H16               | 1.8 V        | Input            | HSMB_BYPASS           |
| H1                | 2.5 V        | Output           | HSMA_B_JTAG_TDI       |
| B9                | 2.5 V        | Input            | HSMB_JTAG_TDO         |
| E16               | 1.8 V        | Input            | JTAG_SEL              |
| D9                | 2.5 V        | Output           | LCD_BS1               |
| N16               | 1.8 V        | Output           | LCD_SERn              |
| L16               | 1.8 V        | Input            | MAX_CSn               |
| N14               | 1.8 V        | Input            | MAX_DIP[0]            |
| M13               | 1.8 V        | Input            | MAX_DIP[1]            |
| N15               | 1.8 V        | Input            | MAX_DIP[2]            |
| L14               | 1.8 V        | Input            | MAX_DIP[3]            |
| J5                | 2.5 V        | Output           | MAX_EMB               |
| M8                | 1.8 V        | Input            | MAX_EN                |
| J4                | 2.5 V        | Output           | MAX_ERROR             |
| J3                | 2.5 V        | Output           | MAX_FACTORY           |
| K1                | 2.5 V        | Output           | MAX_LOAD              |
| K13               | 1.8 V        | Input            | MAX_OEn               |
| M14               | 1.8 V        | Input            | MAX_RESERVE[0]        |
| P14               | 1.8 V        | Input            | MAX_RESERVE[1]        |

**Table 2-5.** MAX II Device Pin-Out (*Note 1*) (Part 5 of 8)

| MAX II Pin Number | I/O Standard | Signal Direction | Schematic Signal Name |
|-------------------|--------------|------------------|-----------------------|
| K2                | 2.5 V        | Output           | MAX_USER              |
| K15               | 1.8 V        | Input            | MAX_WEn               |
| H12               | 1.8 V        | Input            | MAX2_CLK              |
| M1                | 2.5 V        | Input            | MAXGP_JTAG_TCK        |
| L4                | 2.5 V        | Output           | MAXGP_JTAG_TDI        |
| L5                | 2.5 V        | Input            | MAXGP_JTAG_TDO        |
| M2                | 2.5 V        | Input            | MAXGP_JTAG_TMS        |
| N13               | 1.8 V        | Input            | MWATTS_MAMPS          |
| H13               | 1.8 V        | Input            | PGM[0]                |
| H15               | 1.8 V        | Input            | PGM[1]                |
| H14               | 1.8 V        | Input            | PGM[2]                |
| G16               | 1.8 V        | Input            | PGM[3]                |
| J1                | 2.5 V        | Output           | PMON_CLK              |
| J2                | 2.5 V        | Output           | PMON_CSN              |
| H3                | 2.5 V        | Bidir            | PMON_DATA             |
| H4                | 2.5 V        | Output           | PMON_SDI              |
| H5                | 2.5 V        | Output           | PMON_SYNC             |
| F6                | 2.5 V        | Output           | PWR_DIG_SEL[1]        |
| F1                | 2.5 V        | Output           | PWR_DIG_SEL[2]        |
| G3                | 2.5 V        | Output           | PWR_DIG_SEL[3]        |
| G2                | 2.5 V        | Output           | PWR_DIG_SEL[4]        |
| D2                | 2.5 V        | Output           | PWR_SEG_A             |
| E5                | 2.5 V        | Output           | PWR_SEG_B             |
| D1                | 2.5 V        | Output           | PWR_SEG_C             |
| F3                | 2.5 V        | Output           | PWR_SEG_D             |
| F5                | 2.5 V        | Output           | PWR_SEG_DP            |
| E2                | 2.5 V        | Output           | PWR_SEG_E             |
| F4                | 2.5 V        | Output           | PWR_SEG_F             |
| E1                | 2.5 V        | Output           | PWR_SEG_G             |
| F2                | 2.5 V        | Output           | PWR_SEG_MINUS         |
| G4                | 2.5 V        | Input            | PWR_SEL[0]            |
| G1                | 2.5 V        | Input            | PWR_SEL[1]            |
| G5                | 2.5 V        | Input            | PWR_SEL[2]            |
| H2                | 2.5 V        | Input            | PWR_SEL[3]            |
| D13               | —            | —                | RESERVED_INPUT        |
| E14               | —            | —                | RESERVED_INPUT        |
| E15               | —            | —                | RESERVED_INPUT        |
| G12               | —            | —                | RESERVED_INPUT        |
| G14               | —            | —                | RESERVED_INPUT        |

**Table 2-5.** MAX II Device Pin-Out (*Note 1*) (Part 6 of 8)

| MAX II Pin Number | I/O Standard | Signal Direction | Schematic Signal Name |
|-------------------|--------------|------------------|-----------------------|
| G15               | —            | —                | RESERVED_INPUT        |
| K12               | —            | —                | RESERVED_INPUT        |
| L13               | —            | —                | RESERVED_INPUT        |
| P13               | —            | —                | RESERVED_INPUT        |
| R16               | —            | Input            | RESET_CONFIGn         |
| F16               | —            | Output           | SRAM_ACTIVE           |
| F15               | —            | Input            | SRAM_CSn              |
| B3                | 2.5 V        | Input            | USB_CLKOUT            |
| E10               | 2.5 V        | Input            | USB_CMD_DATA          |
| B10               | 2.5 V        | Output           | USB_EMPTY             |
| E9                | 2.5 V        | Bidirectional    | USB_FD[0]             |
| A9                | 2.5 V        | Bidirectional    | USB_FD[1]             |
| A8                | 2.5 V        | Bidirectional    | USB_FD[2]             |
| B8                | 2.5 V        | Bidirectional    | USB_FD[3]             |
| E8                | 2.5 V        | Bidirectional    | USB_FD[4]             |
| A7                | 2.5 V        | Bidirectional    | USB_FD[5]             |
| D8                | 2.5 V        | Bidirectional    | USB_FD[6]             |
| B7                | 2.5 V        | Bidirectional    | USB_FD[7]             |
| C9                | 2.5 V        | Output           | USB_FULL              |
| J14               | 1.8 V        | Input            | USB_IFCLK             |
| A2                | 2.5 V        | Bidirectional    | USB_PA0_INT0n         |
| D5                | 2.5 V        | Bidirectional    | USB_PA1_INT1n         |
| B1                | 2.5 V        | Bidirectional    | USB_PA2_SLOE          |
| D4                | 2.5 V        | Bidirectional    | USB_PA3_WU2           |
| L3                | 2.5 V        | Bidirectional    | USB_PA4_IF0ADR0       |
| L1                | 2.5 V        | Bidirectional    | USB_PA5_IF0ADR1       |
| K5                | 2.5 V        | Bidirectional    | USB_PA6_PKTEND        |
| L2                | 2.5 V        | Bidirectional    | USB_PA7_SLCSn         |
| A4                | 2.5 V        | Input            | USB_PHY_CMD_DATA      |
| D6                | 2.5 V        | Output           | USB_PHY_EMPTY         |
| C13               | 2.5 V        | Bidirectional    | USB_PHY_FD[0]         |
| B16               | 2.5 V        | Bidirectional    | USB_PHY_FD[1]         |
| E11               | 2.5 V        | Bidirectional    | USB_PHY_FD[10]        |
| B12               | 2.5 V        | Bidirectional    | USB_PHY_FD[11]        |
| C10               | 2.5 V        | Bidirectional    | USB_PHY_FD[12]        |
| A12               | 2.5 V        | Bidirectional    | USB_PHY_FD[13]        |
| D10               | 2.5 V        | Bidirectional    | USB_PHY_FD[14]        |
| B11               | 2.5 V        | Bidirectional    | USB_PHY_FD[15]        |
| C12               | 2.5 V        | Bidirectional    | USB_PHY_FD[2]         |

**Table 2-5.** MAX II Device Pin-Out (*Note 1*) (Part 7 of 8)

| MAX II Pin Number | I/O Standard | Signal Direction | Schematic Signal Name |
|-------------------|--------------|------------------|-----------------------|
| A15               | 2.5 V        | Bidirectional    | USB_PHY_FD [3]        |
| D12               | 2.5 V        | Bidirectional    | USB_PHY_FD [4]        |
| B14               | 2.5 V        | Bidirectional    | USB_PHY_FD [5]        |
| C11               | 2.5 V        | Bidirectional    | USB_PHY_FD [6]        |
| B13               | 2.5 V        | Bidirectional    | USB_PHY_FD [7]        |
| D11               | 2.5 V        | Bidirectional    | USB_PHY_FD [8]        |
| A13               | 2.5 V        | Bidirectional    | USB_PHY_FD [9]        |
| C4                | 2.5 V        | Output           | USB_PHY_FULLL         |
| C7                | 2.5 V        | Input            | USB_PHY_IFCLK         |
| E6                | 2.5 V        | Input            | USB_PHY_REn           |
| B4                | 2.5 V        | Input            | USB_PHY_WEn           |
| E7                | 2.5 V        | Input            | USB_PWR_ENn           |
| C8                | 2.5 V        | Output           | USB_RDn               |
| A11               | 2.5 V        | Input            | USB_REn               |
| C6                | 2.5 V        | Output           | USB_RESETr            |
| A5                | 2.5 V        | Output           | USB_RSTn              |
| D7                | 2.5 V        | Input            | USB_RSTOUTn           |
| B6                | 2.5 V        | Input            | USB_RXFn              |
| B5                | 2.5 V        | Output           | USB_SI_WU             |
| K3                | 2.5 V        | Input            | USB_TXEn              |
| C5                | 2.5 V        | Output           | USB_WAKEUP            |
| M3                | 2.5 V        | Input            | USB_WEn               |
| A6                | 2.5 V        | Output           | USB_WR                |
| F10               | —            | Power            | VCCINT                |
| G11               | —            | Power            | VCCINT                |
| H8                | —            | Power            | VCCINT                |
| H10               | —            | Power            | VCCINT                |
| J7                | —            | Power            | VCCINT                |
| J9                | —            | Power            | VCCINT                |
| K6                | —            | Power            | VCCINT                |
| L7                | —            | Power            | VCCINT                |
| C1                | —            | Power            | VCCIO1                |
| H6                | —            | Power            | VCCIO1                |
| J6                | —            | Power            | VCCIO1                |
| P1                | —            | Power            | VCCIO1                |
| A3                | —            | Power            | VCCIO2                |
| A14               | —            | Power            | VCCIO2                |
| F8                | —            | Power            | VCCIO2                |
| F9                | —            | Power            | VCCIO2                |

**Table 2-5.** MAX II Device Pin-Out (Note 1) (Part 8 of 8)

| MAX II Pin Number | I/O Standard | Signal Direction | Schematic Signal Name |
|-------------------|--------------|------------------|-----------------------|
| C16               | —            | Power            | VCCIO3                |
| H11               | —            | Power            | VCCIO3                |
| J11               | —            | Power            | VCCIO3                |
| P16               | —            | Power            | VCCIO3                |
| L8                | —            | Power            | VCCIO4                |
| L9                | —            | Power            | VCCIO4                |
| T3                | —            | Power            | VCCIO4                |
| T14               | —            | Power            | VCCIO4                |
| P15               | 1.8 V        | Input            | VOLTS_WATTS           |

**Note to Table 2-5:**(1) For more information about the MAX II pin-out, refer to the Altera website at [www.altera.com/literature/lit-dp.jsp](http://www.altera.com/literature/lit-dp.jsp).

Table 2-6 lists the MAX II component reference and manufacturing information.

**Table 2-6.** MAX II Component Reference and Manufacturing Information

| Board Reference | Description   | Manufacturer       | Manufacturing Part Number | Manufacturer Website                               |
|-----------------|---|--------------------|---------------------------|--|
| U7              | 256-pin device in a FineLine Ball Grid Array (FBGA) package | Altera Corporation | EPM2210GF256C3N           | <a href="http://www.altera.com">www.altera.com</a> |

## Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements, and is divided into the following groups:

- “Configuration” on page 2-15
  - FPGA programming over USB
  - FPGA programming from flash memory
  - Flash programming over USB
- “Status Elements” on page 2-17
  - Board-specific LEDs
  - Power display
- “Setup Elements” on page 2-18
  - JTAG control DIP switch
  - MAX II device control DIP switch
  - System reset and configuration push buttons
  - POWER SELECT rotary switch
  - PGM CONFIG SELECT rotary switch
  - Speaker header


## Configuration

This section discusses FPGA, flash memory, and MAX II device programming methods supported by the Cyclone III development board.

### FPGA Programming Over USB

The FPGA can be configured at any time the board is powered on by using the USB 2.0 interface and the Quartus II Programmer in JTAG mode.

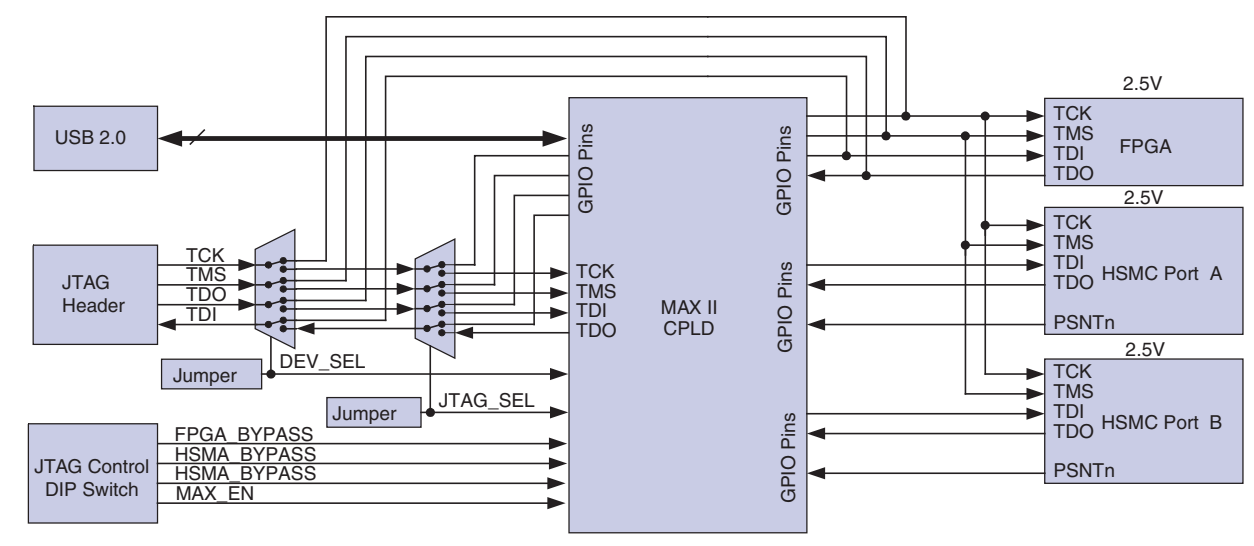
The JTAG chain is mastered by the embedded USB Blaster function found in the MAX II device. Only a USB cable is needed to program the Cyclone III FPGA. Any device can be bypassed by using the appropriate switch on the JTAG control DIP switch.

 Board reference SW1 position 5 (SW1.5), labeled MAX0, must be in the closed position (on) for this feature to properly work. If the SW1 switch is in the closed position, the parallel flash loader (PFL) megafunction in the MAX II CPLD may try to overwrite the FPGA image just downloaded over the USB immediately after completion.

For more information about:

- Advanced JTAG settings, refer to [Table 2-7](#).
- The JTAG control switch, refer to [“JTAG Control DIP Switch” on page 2-19](#).

**Figure 2-4.** JTAG Chain with the MAX II Device and the Cyclone III Device



The JTAG header can be used with an external USB-Blaster cable, or equivalent, to program either the MAX II CPLD or the Cyclone III FPGA. Most users of the Cyclone III development board do not use the JTAG header at all and instead use a USB cable along with the embedded USB-Blaster. Using an external USB-Blaster with the JTAG header requires disabling the embedded USB-Blaster function. See [Table 2-7](#).

**Table 2-7.** JTAG Settings (Note 1)

| Number | Description  | FPGA Bypass (SW3.1) | HSMA Bypass (SW3.2) | HSMB Bypass (SW3.3) | MAX Enable (SW3.4) | PFL Enable (SW1.5 MAX0) | Device Select (DEV_SEL) Jumper, J6 |
|--------|--|---------------------|---------------------|---------------------|--------------------|-------------------------|------------------------------------|
| 1      | Embedded USB Blaster (2), Cyclone III target device only   | 1                   | 0                   | 0                   | 0                  | 1                       | X                                  |
| 2      | Embedded USB Blaster (2) Cyclone III device + HSMC Port A  | 1                   | 1                   | 0                   | 0                  | 1                       | X                                  |
| 3      | Embedded USB Blaster (2), Cyclone III device + HSMC Port B | 1                   | 0                   | 1                   | 0                  | 1                       | X                                  |
| 4      | External USB Blaster (3), Cyclone III target device only   | X                   | X                   | X                   | 1                  | 1                       | Off                                |
| 5      | External USB Blaster (3), MAX II target device only        | X                   | X                   | X                   | X                  | X                       | On                                 |

**Notes to Table 2-7:**

- (1) The nomenclature SW3.1 is used to indicate board reference SW3, position 1; similarly SW1.5 is used to indicate board reference SW1, position 5.
- (2) Requires USB cable plugged into board reference J3.
- (3) Requires external USB-Blaster or equivalent plugged into board reference J14 (PCB bottom).

**FPGA Programming from Flash Memory**

On either power-up or by pressing the RESET\_CONFIG or FACTORY\_CONFIG push button, the MAX II CPLD device's PFL megafunction configures the Cyclone III FPGA from flash memory.

The PFL megafunction reads 16-bit data from the flash memory and converts it to passive serial format. The data is written to the Cyclone III device's dedicated DCLK and D0 configuration pins at 12 MHz.

FPGA configuration from flash memory can be sourced from one of eight images. The image is selected by the PGM\_CONFIG\_SELECT rotary switch, board reference SW5. The rotary switch has 16 positions, but only the first eight are used. The positions correspond to an offset in flash memory that the PFL is directed to for FPGA configuration data.



Board reference SW1 position 5 (SW1.5), labeled MAX0, must be in the open position (off) for this feature to be enabled. If the SW1 switch is in the open position, the PFL megafunction in the MAX II CPLD is disabled.

**Flash Programming over USB Interface**

The flash memory can be programmed at any time the board is powered up by using the USB 2.0 interface and the Quartus II Programmer's JTAG mode.

The development kit implements the Altera PFL megafunction for flash programming. The PFL is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash device. The development kit ships with a pre-built PFL design called `cycloneIII_3c120_dev_pfl`. The PFL design is programmed onto the FPGA whenever the flash is to be written using the Quartus II software.





For more information about:

- PFL megafunction, refer to *AN386: Using the Parallel Flash Loader with the Quartus II Software*.
- Basic flash programming instructions for the development board, refer to the *Programming the Flash Device* section of the *Cyclone III Development User Guide*.

## Status Elements

The development board includes general user, board specific, and HSMC user LEDs. This section discusses board-specific LEDs as well as the power display device.



For information about general and HSMC user-defined LEDs, refer to “*User-Defined LEDs*” on page 2-27.

### Board Specific LEDs

There are 14 board-specific LEDs, which are factory designated. Table 2-8 lists the LED board reference, name, and description.

**Table 2-8.** Board-Specific LEDs (Part 1 of 2)

| Board Reference | LED Name            | Description  |
|-----------------|---------------------|--|
| D5              | Power               | Illuminates when board power switch SW2 is on.<br>(Requires 14 V to 20 V input to DC input jack J2)  |
| D25             | CONF DONE           | Illuminates when FPGA is successfully configured. Driven by Cyclone III FPGA.  |
| D20             | Loading             | Illuminates when MAX II CPLD is actively configuring the FPGA. Driven by the MAX II CPLD.  |
| D21             | Error               | Illuminates when MAX II CPLD fails to successfully configure the FPGA. Driven by the MAX II CPLD.  |
| D24             | Factory             | Illuminates when FPGA is configured with the default factory FPGA design. Driven by the MAX II CPLD.   |
| D22             | User                | Illuminates when FPGA is configured with a design other than the default factory FPGA design. Driven by the MAX II CPLD.                     |
| D7              | ENET TX             | Illuminates when transmit data is active from the Ethernet PHY. Driven by the Marvell 88E1111 PHY.   |
| D8              | ENET RX             | Illuminates when receive data is active from the Ethernet PHY. Driven by the Marvell 88E1111 PHY.  |
| D1              | 10 MB               | Illuminates when Ethernet PHY is using the 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.                                      |
| D3              | 100 MB              | Illuminates when Ethernet PHY is using the 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.                                     |
| D4              | 1000 M              | Illuminates when Ethernet PHY is using the 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY. Also connects to Cyclone III FPGA. |
| D6              | Duplex              | Illuminates when Ethernet PHY is both sending and receiving data. Driven by the Marvell 88E1111 PHY.   |
| D18             | HSMC Port A present | Illuminates when HSMC Port A has a board or cable plugged such that pin 160 becomes grounded.  |

**Table 2–8.** Board-Specific LEDs (Part 2 of 2)

| Board Reference | LED Name            | Description  |
|-----------------|---------------------|--|
| D19             | HSMC Port B present | Illuminates when HSMC Port B has a board or cable plugged such that pin 160 becomes grounded.                |
| D17             | SRAM active         | Illuminates when SRAM is being accessed with a read or write transaction. Driven by the MAX II CPLD.         |
| D23             | Flash active        | Illuminates when flash memory is being accessed with a read or write transaction. Driven by the MAX II CPLD. |

Table 2–9 lists the board-specific LEDs component reference and manufacturing information.

**Table 2–9.** Board-Specific LEDs Component Reference and Manufacturing Information

| Board Reference                          | Description                             | Manufacturer | Manufacturing Part Number | Manufacturer Website                             |
|--|---|--------------|---------------------------|--|
| D1, D3, D4, D6-D8, D17-D19, D20, D22-D25 | Green LED, 1206, SMT, clear lens, 2.1 V | Lumex, Inc   | SML-LX1206GC-TR           | <a href="http://www.lumex.com">www.lumex.com</a> |
| D5                                       | Blue LED, 1206, SMT, clear lens, 3.5 V  | Lumex, Inc   | SML-LX1206USBC-TR         | <a href="http://www.lumex.com">www.lumex.com</a> |
| D21                                      | Red LED, 1206, SMT, clear lens, 2.0 V   | Lumex, Inc   | SML-LX1206IC-TR           | <a href="http://www.lumex.com">www.lumex.com</a> |

### Power Display (U28)

The power being measured by the MAX II CPLD and associated A/D is displayed on a dedicated 7-segment display connected to the MAX II device called *Power Display*. Although the 7-segment display is connected to the MAX II CPLD, it is also register-controllable from the FPGA using the FSM bus.

## Setup Elements

The development board includes user, JTAG control, and board-specific DIP switches. The board also includes system reset and configuration push button switches as well as rotary switches. This section discusses:

- JTAG control DIP switch
- MAX II device control DIP switch
- System reset and configuration push buttons
- POWER SELECT rotary switch
- PGM CONFIG SELECT rotary switch
- Speaker header

## JTAG Control DIP Switch

Board reference SW3 is a 4-position JTAG control DIP switch, and it is provided to either remove or include devices in the active JTAG chain. Additionally, JTAG control DIP switch is also used to disable the embedded USB Blaster cable when using an external USB Blaster cable. See [Table 2-10](#).

**Table 2-10.** JTAG Control DIP Switch Signal Name and Description

| DIP Switch | Signal Name | Description  |
|------------|-------------|--|
| 1          | FPGA_BYPASS | 1 = FPGA in JTAG chain<br>0 = FPGA not in JTAG chain                                   |
| 2          | HSMA_BYPASS | 1 = HSMC Port A in JTAG chain (only if installed)<br>0 = HSMC Port A not in JTAG chain |
| 3          | HSMB_BYPASS | 1 = HSMC Port B in JTAG chain (only if installed)<br>0 = HSMC Port B not in JTAG chain |
| 4          | MAX_EN      | 1 = MAX II device disabled<br>0 = MAX II device enabled                                |

Because the JTAG chain also contains the two HSMC interface connectors, the SW3 DIP switch allows data to bypass the HSMC interfaces as well as the MAX II CPLD. See [“FPGA Programming Over USB” on page 2-15](#).



For information about user-defined DIP switches, refer to [“User-Defined DIP Switches” on page 2-26](#).

[Table 2-11](#) lists the JTAG control switch component reference and manufacturing information.

**Table 2-11.** JTAG Control Switch Component Reference and Manufacturing Information

| Board Reference | Description                     | Manufacturer                  | Manufacturing Part Number |
|-----------------|---------------------------------|-------------------------------|---------------------------|
| SW3             | Four-position slider DIP switch | C&K Components ITT industries | TDA04H0SB1                |

## MAX II Device Control DIP Switch

Board reference SW1 is the board settings DIP switch, which controls various features specific to the Cyclone III development board and factory default (board test system) FPGA design: On = logic 0 and Off = logic 1.

[Table 2-12](#) lists the switch position, name, and description.

**Table 2-12.** MAX II Device Control DIP Switch Position, Name, and Description (Part 1 of 2)

| Switch | Name     | Description   |
|--------|----------|---|
| 8      | MAX_DIP3 | Reserved  |
| 7      | MAX_DIP2 | Reserved  |
| 6      | MAX_DIP1 | Reserved  |
| 5      | MAX_DIP0 | 1 = MAX II device PFL enabled, 0 = MAX II device PFL disabled |

**Table 2-12.** MAX II Device Control DIP Switch Position, Name, and Description (Part 2 of 2)

| Switch | Name         | Description  |
|--------|--------------|--|
| 4      | MAX_RESERVE1 | Reserved   |
| 3      | MAX_RESERVE0 | Reserved   |
| 2      | VOLTS_WATTS  | 1 = power display shows mW/mA, 0 = power display shows voltage |
| 1      | MWATTS_MAMPS | 1 = power display shows mA, 0 = power display shows mW         |

Table 2-13 lists the MAX II device control DIP switch component reference and manufacturing information.

**Table 2-13.** MAX II Device Control DIP Switch Component Reference and Manufacturing Information

| Board Reference | Description                  | Manufacturer         | Manufacturing Part Number | Manufacturer Website                                   |
|-----------------|------------------------------|----------------------|---------------------------|--|
| SW1             | 8-position rocker DIP switch | Grayhill Corporation | 76SB08ST                  | <a href="http://www.grayhill.com">www.grayhill.com</a> |

### System Reset and Configuration Switches

Board reference S6 is the system reset push button switch, RESET\_CONFIGn, which is an input to the MAX II device. It forces a reconfiguration of the FPGA from flash memory. The location in flash memory is based on the input from the board settings rotary switch position for the signals PGM [2 : 0]. The MAX II device uses the RESET\_CONFIGn pin as its reset along with the CPU\_RESETn push button.

Board reference S5 is the CPU reset push button switch, CPU\_RESET, which is an input to both the Cyclone III FPGA and the MAX II CPLD. The CPU\_RESET push button is intended to be the master reset signal for the FPGA design loaded in the Cyclone III device, and connects to the special function pin called DEV\_CLR on the FPGA but is also a regular I/O pin. The MAX II device uses this as its reset along with the RESET\_CONFIG and FACTORY\_CONFIG push buttons.

Board reference S7 is the factory push button switch (FACTORY\_CONFIG), which is an input to the MAX II device. The FACTORY\_CONFIG pin forces a reconfiguration of the FPGA with the factory default FPGA design, which is located at the base of flash memory. See Table 2-14.


**Table 2-14.** Push Button Switch Signal Name and Function

| Board Reference | Description              | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number | MAX II Device Pin Number |
|-----------------|--------------------------|--------------|-----------------------|-------------------------------|--------------------------|
| S7              | User defined push button | 1.8 V        | FACTORY_CONFIG        | —                             | A10                      |
| S6              | User defined push button | 1.8 V        | RESET_CONFIGn         | —                             | R16                      |
| S5              | User defined push button | 1.8 V        | CPU_RESET             | T21                           | M9                       |

Table 2-15 lists the push-button switch component reference and manufacturing information.

**Table 2-15.** Push-Button Switch Component Reference and Manufacturing Information

| Board Reference | Description        | Manufacturer | Manufacturing Part Number | Manufacturer Website                                     |
|-----------------|--------------------|--------------|---------------------------|--|
| S5-S7           | Push button switch | Panasonic    | EVQAPAC07K                | <a href="http://www.panasonic.com">www.panasonic.com</a> |

 For information about user-defined push buttons, refer to “User-Defined Push Button Switches” on page 2-26.

### POWER SELECT Rotary Switch

A 16-position rotary switch, board reference SW4, is used to select the current power rail whose power is being measured and displayed on the power display. The rotary switch is connected to the MAX II CPLD, but it also registers readable by the FPGA using the FSM shared bus (flash, SRAM, and MAX II device). Table 2-16 lists the power select rotary switch number, name, power pin, and description.

**Table 2-16.** Power Select Rotary Switch Number, Name, Pin, and Description

| Number | Schematic Signal Name | Power Pin Name | Description  |
|--------|-----------------------|----------------|--|
| 0      | 1.2V_INT              | VCCINT         | FPGA core power  |
| 1      | 1.2V_VCCD             | VCCD_PLL       | FPGA PLL digital power   |
| 2      | 2.5V_VCCA             | VCCA           | FPGA PLL analog power and auxiliary circuit power                |
| 3      | 1.8V_IO_B3_B4         | VCCIO3, VCCIO4 | FPGA I/O power banks 3, 4  |
| 4      | 1.8V_IO_B7_B8         | VCCIO7, VCCIO8 | FPGA I/O power banks 7, 8  |
| 5      | 2.5V_IO_B1_B2         | VCCIO1, VCCIO2 | FPGA I/O power banks 1, 2  |
| 6      | 2.5V_IO_B5_B6         | VCCIO5, VCCIO6 | FPGA I/O power banks 5, 6  |
| 7      | 1.2V                  | —              | All non-FPGA 1.2-V power (Ethernet)                              |
| 8      | 1.8V                  | —              | All non-FPGA 1.8-V power (SRAM, Flash, MAX II, and DDR2 devices) |
| 9      | 2.5V                  | —              | All non-FPGA 2.5-V power (Ethernet, LEDs, LCD)                   |
| A      | 3.3V                  | —              | All 3.3-V power (voltage only) (1)                               |
| B      | 5.0V                  | —              | All 5.0-V power (voltage only) (1)                               |
| C      | 12V                   | —              | All 12-V power (voltage only) (1)                                |
| D      | —                     | —              | —  |
| E      | —                     | —              | —  |
| F      | —                     | —              | —  |

**Note to Table 2-16:**

- (1) Display shows resistor divider output, not actual voltage as the A/D cannot take in sources higher than 3.0 V. See schematic page 5 for resistor dividers. Current (mA) displays for these voltages are only accurate to see a change in current from one circuit state to another. The absolute current levels should not be referenced.

Table 2-17 lists power select rotary switch component reference and manufacturing information.

**Table 2-17.** Power Select Rotary Switch Component Reference and Manufacturing Information

| Board Reference | Description               | Manufacturer         | Manufacturing Part Number | Manufacturer Website                                   |
|-----------------|---------------------------|----------------------|---------------------------|--|
| SW4             | 16-position rotary switch | Grayhill Corporation | 94HCB16WT                 | <a href="http://www.grayhill.com">www.grayhill.com</a> |

### PGM CONFIG SELECT Rotary Switch

A 16-position rotary switch, board reference SW5, is used to select the location in flash memory to load the Cyclone III FPGA design. The rotary switch has 16 positions but only the first eight are used. For information about the flash memory locations, refer to [Table 2-58 on page 2-60](#).

[Table 2-18](#) lists PGM configuration select rotary switch component reference and manufacturing information.

**Table 2-18.** PGM CONFIG SELECT Rotary Switch Component Reference and Manufacturing Information

| Board Reference | Description   | Manufacturer         | Manufacturing Part Number | Manufacturer Website                                   |
|-----------------|---------------|----------------------|---------------------------|--|
| SW5             | Rotary switch | Grayhill Corporation | 94HCB16WT                 | <a href="http://www.grayhill.com">www.grayhill.com</a> |

### Speaker Header (J5)

A four-pin 0.1" pitch header is used for a PC speaker connection. The FPGA drives an R/C filter from a 2.5-V CMOS I/O pin allowing tones to be generated by driving different frequencies to the pin.

[Table 2-19](#) lists power select rotary switch component reference and manufacturing information.

**Table 2-19.** Power Select Rotary Switch Component Reference and Manufacturing Information

| Board Reference | Description    | Manufacturer | Manufacturing Part Number | Manufacturer Website                               |
|-----------------|----------------|--------------|---------------------------|--|
| J5              | Speaker header | Samtec       | TSW-104-07-G-S            | <a href="http://www.samtec.com">www.samtec.com</a> |

## Clocking Circuitry

This section describes Cyclone III FPGA clocking inputs and outputs. A diagram is provided for each section.

### Cyclone III FPGA Clock Inputs

[Figure 2-5](#) outlines the clocking inputs to the Cyclone III FPGA.

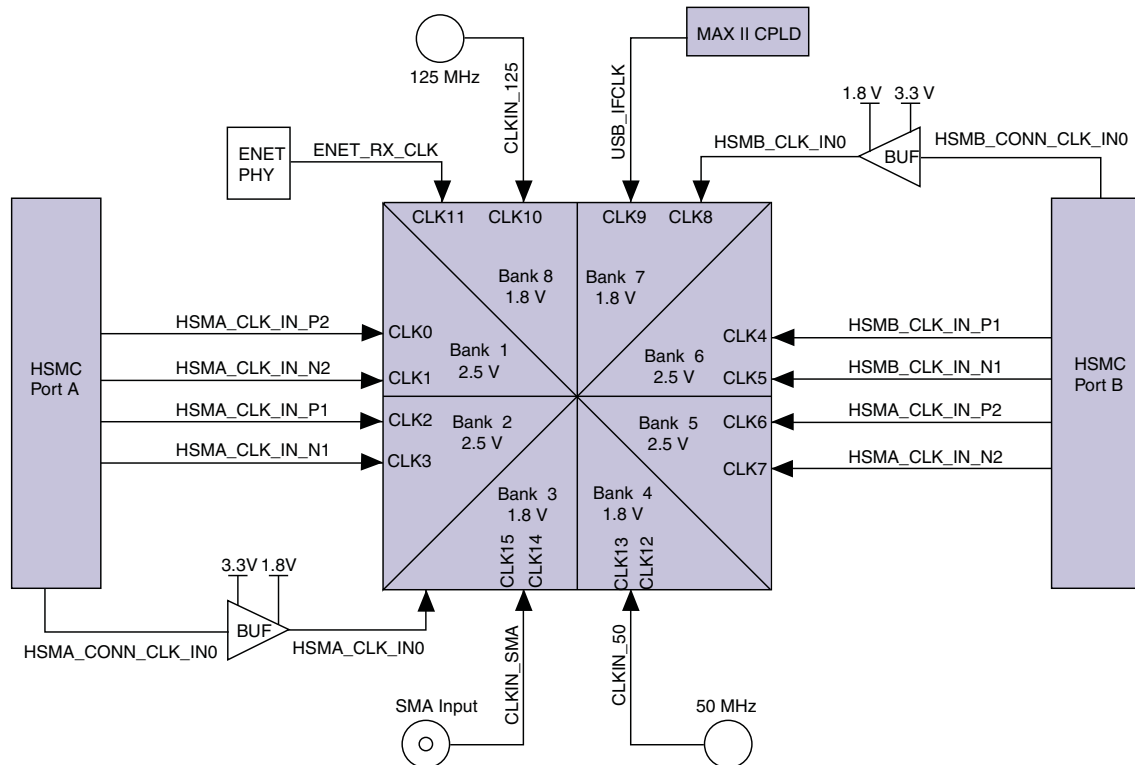


Some signals are connected to 1.8-V banks and some are connected to 2.5-V banks. Refer to the [Cyclone III Device Handbook](#) for information about allowable levels for driving these inputs from external sources.

The clock 1 and clock 2 signals from the HSMC interface can be used as LVDS pairs or as eight separate clock signals. These signals include HSMA\_CLK\_IN\_P2/N2, HSMA\_CLK\_IN\_P1/N1, HSMB\_CLK\_IN\_P2/N2, and HSMB\_CLK\_IN\_P1/N1. These signals may also be used for bidirectional data. If used in LVDS mode, install applicable termination resistors between P/N pairs. A voltage translator, National Semiconductor part number FXLP34, is located in between the HSMC interfaces and the Cyclone III FPGA to reduce LVTTTL to 1.8-V CMOS input levels for clock 0 signals HSMA\_CLK\_IN0 and HSMB\_CLK\_IN0.

For more information, refer to the Cyclone III development board schematics included in the development kit.

**Figure 2-5.** Cyclone III FPGA Clock Inputs



## Cyclone III FPGA Clock Outputs

Figure 2-6 outlines the clocking outputs from the Cyclone III FPGA.

Some signals are connected to 1.8-V banks and some are connected to 2.5-V banks. Refer to the *Cyclone III Device Handbook* for information about voltage output levels.

The clock 1 and clock 2 signals from the HSMC interface can be used as LVDS pairs or as eight separate clock signals. These signals include HSMA\_CLK\_IN\_P2/N2, HSMA\_CLK\_IN\_P1/N1, HSMB\_CLK\_IN\_P2/N2, and HSMB\_CLK\_IN\_P1/N1. These signals may also be used for bidirectional data.

The CLKOUT\_SMA signal connects to the Cyclone III FPGA using a dedicated PLL output pin, PLL4\_CLKOUTp. This pin does not have to be used with the PLL as it can also drive data or other trigger signals.

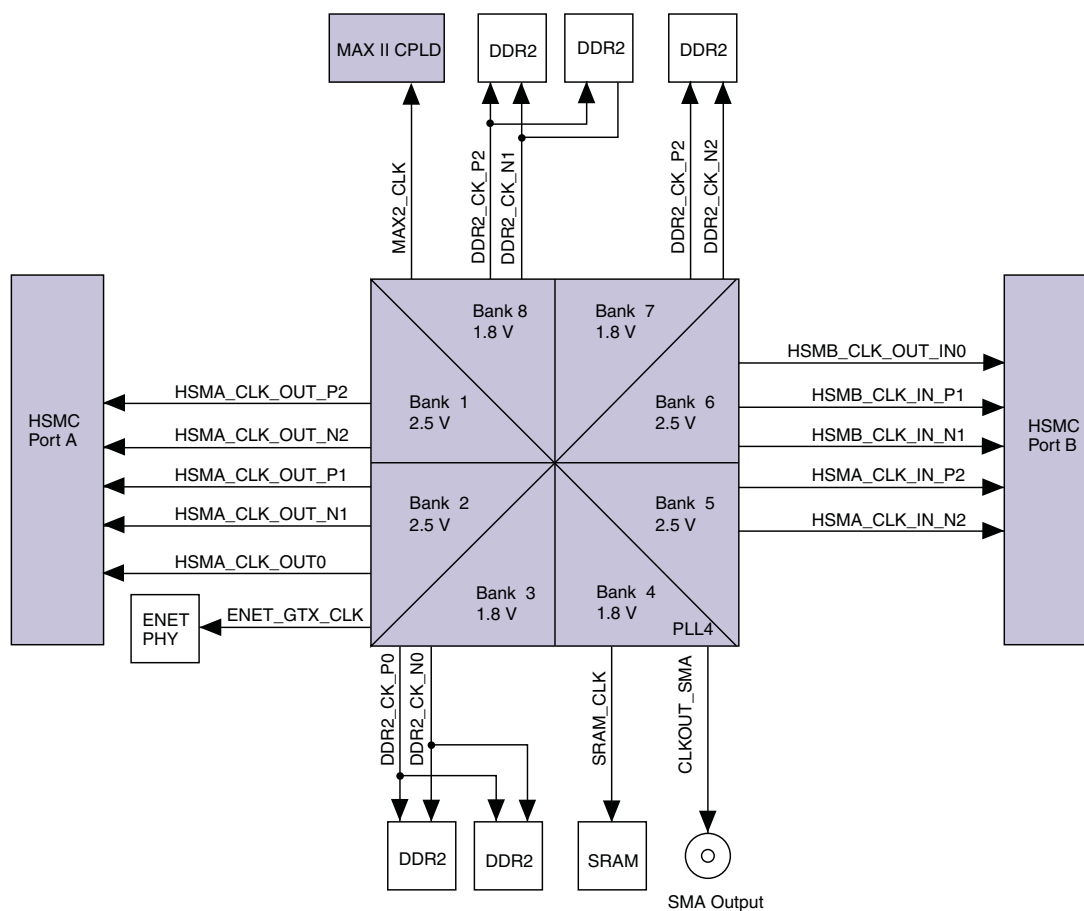
**Figure 2–6.** Cyclone III FPGA Clock Outputs

Table 2–20 shows the clocking parts list.

**Table 2–20.** Cyclone III Development Board Clocking Parts List

| Board Reference | Description                         | Manufacturer            | Manufacturer Part Number | Manufacturer Website   |
|-----------------|-------------------------------------|-------------------------|--------------------------|--|
| Y5              | 50-MHz LVDS oscillator              | Pletronics              | SM5545TEX-50.00M         | <a href="http://www.pletronics.com">www.pletronics.com</a>   |
| Y4              | 125-MHz LVDS oscillator             | Pletronics              | SM5545TEX-125.00M        | <a href="http://www.pletronics.com">www.pletronics.com</a>   |
| J10, J11        | SMA for external clock input/output | Lighthouse Technologies | LTI-SASF546-P26-X1       | <a href="http://www.rfconnector.com">www.rfconnector.com</a> |
| Y1              | 24-MHz crystal                      | Abracon Corporation     | ABL-24.000MHZ-12         | <a href="http://www.abracon.com">www.abracon.com</a>         |
| Y2              | 6-MHz crystal                       | Abracon Corporation     | ABL-6.000MHZ-B2          | <a href="http://www.abracon.com">www.abracon.com</a>         |
| X1              | 25-MHz crystal oscillator           | ECS, Inc.               | ECS-3953C-250-B          | <a href="http://www.ecsxtal.com">www.ecsxtal.com</a>         |
| Y3              | 24-MHz crystal oscillator           | Pletronics              | SM5545TEX-24.00M         | <a href="http://www.pletronics.com">www.pletronics.com</a>   |



Table 2–21 lists the board’s clock distribution system.

**Table 2–21.** Cyclone III Development Board Clock Distribution

| Source  | Schematic Signal Name   | I/O Standard | Signal Originates From | Signal Propagates To              |
|---|-------------------------|--------------|------------------------|-----------------------------------|
| 125-MHz (Y4) oscillator   | clk <sub>in</sub> _125  | Input        | Y4                     | Cyclone III device pin A14        |
| 50-MHz (Y5) oscillator  | clk <sub>in</sub> _50   | Input        | Y5                     | Cyclone III device pin E13        |
| User input (SMA clock input)  | clk <sub>in</sub> _sma  | Input        | J10                    | Cyclone III device pin AH14       |
| User output (SMA clock output)  | clk <sub>out</sub> _sma | Output       | J11                    | From Cyclone III device pin AE23  |
| 25 MHz (reference clock);<br>This clock can change both<br>speed and direction depending<br>on the Ethernet link speed<br>(10/100/1000) | enet_rx_clk             | Input        | U5                     | Cyclone III device pin B14        |
| 24-MHz (Y3) oscillator  | clk <sub>in</sub> _24   | Input        | Y3                     | MAX II device pin J12<br>(Bank 3) |
| 6-MHz crystal   | XTIN/XTOUT              | Input        | Y2                     | FTDI USB PHY                      |
| 24-MHz crystal  | XTALIN/XTALOUT          | Input        | Y1                     | Cypress USB PHY                   |

## Oscillators

There are several on-board crystals and crystal oscillators driving reference clocks to different devices. Table 2–22 lists the board’s oscillators.

**Table 2–22.** Board Oscillators

| Number | Frequency   | Description                                 |
|--------|-------------|---|
| 1      | 6.000 MHz   | Crystal for FTDI USB PHY                    |
| 2      | 24.000 MHz  | Crystal for Cypress USB PHY                 |
| 3      | 24.000 MHz  | Crystal oscillator for MAX II CPLD          |
| 4      | 25.000 MHz  | Crystal oscillator for Ethernet PHY         |
| 5      | 50.000 MHz  | Crystal oscillator for Cyclone III FPGA PLL |
| 6      | 125.000 MHz | Crystal oscillator for Cyclone III FPGA PLL |

## General User Interfaces

To allow you to fully leverage the I/O capabilities of the Cyclone III device for debugging, control, and monitoring purposes, the following general user interfaces are available on the board:

- Push buttons
- DIP switches
- LEDs
- 7-segment displays
- LCD displays

## User-Defined Push Button Switches

The development board includes four general user, one user reset, one system reset, and one factory push button switch.



For information on the system reset and factory push button switches, refer to “System Reset and Configuration Switches” on page 2-20.

Board references S1 through S4 are push button switches allowing general user I/O interfaces to the Cyclone III device. There is no board-specific function for these four push buttons.

Board reference S5 is the user reset push button switch, CPU\_RESETh, which is an input to the Cyclone III device and MAX II CPLD. It is intended to be the master reset signal for the FPGA design loaded into the Cyclone III device. This connects to the special function pin called the DEV\_CLR on the FPGA, but it also is a regular I/O pin. The MAX II device uses the DEV\_CLR pin as its reset along with the RESET\_CONFIGn push button.

Table 2-23 lists the schematic signal name and corresponding Cyclone III pin number.

**Table 2-23.** Push Button Switch Signal Name and Function

| Board Reference | Schematic Signal Name | Cyclone III Device Pin Number | MAX II Device Pin Number |
|-----------------|-----------------------|-------------------------------|--------------------------|
| S1              | USER_PB3              | AA12                          | —                        |
| S2              | USER_PB2              | AH3                           | —                        |
| S3              | USER_PB1              | AC12                          | —                        |
| S4              | USER_PB0              | AD7                           | —                        |
| S5              | CPU_RESETh            | T21                           | M9                       |

Table 2-24 lists the push button switch component reference and manufacturing information.

**Table 2-24.** Push Button Switch Component Reference and Manufacturing Information

| Board Reference | Description        | Manufacturer | Manufacturing Part Number | Manufacturer Website                                     |
|-----------------|--------------------|--------------|---------------------------|--|
| S1 through S5   | Push button switch | Panasonic    | EVQPAC07K                 | <a href="http://www.panasonic.com">www.panasonic.com</a> |

## User-Defined DIP Switches

Board reference SW6 is an 8-pin DIP switch. The switches in SW6 are user-defined, and are provided for additional FPGA input control. Each pin can be set to a logic 1 by pushing it to the open position, and each pin can be set to a logic 0 by pushing it to the closed position. There is no board-specific function for these switches.

Table 2-25 lists the user DIP switch setting, schematic signal name, and corresponding Cyclone III device’s pin number.

**Table 2-25.** User-Defined DIP Switch Pin-Out (SW6)

| Board Reference<br>SW6 DIP Switch | Description                   | I/O Standard | Schematic<br>Signal Name | Cyclone III<br>Device<br>Pin Number |
|-----------------------------------|-------------------------------|--------------|--------------------------|-------------------------------------|
| SW6 pin 1                         | User-defined DIP switch pin 1 | 1.8 V        | USER_DIPSW0              | AC14                                |
| SW6 pin 2                         | User-defined DIP switch pin 2 | 1.8 V        | USER_DIPSW1              | AD18                                |
| SW6 pin 3                         | User-defined DIP switch pin 3 | 1.8 V        | USER_DIPSW2              | AG23                                |
| SW6 pin 4                         | User-defined DIP switch pin 4 | 1.8 V        | USER_DIPSW3              | AC19                                |
| SW6 pin 5                         | User-defined DIP switch pin 5 | 1.8 V        | USER_DIPSW4              | AD14                                |
| SW6 pin 6                         | User-defined DIP switch pin 6 | 1.8 V        | USER_DIPSW5              | G20                                 |
| SW6 pin 7                         | User-defined DIP switch pin 7 | 1.8 V        | USER_DIPSW6              | AB15                                |
| SW6 pin 8                         | User-defined DIP switch pin 8 | 1.8 V        | USER_DIPSW7              | AF25                                |

Table 2-26 lists the user-defined DIP switch component reference and manufacturing information.

**Table 2-26.** User-Defined DIP Switch Component Reference and Manufacturing Information

| Board Reference | Description                  | Manufacturer         | Manufacturing<br>Part Number | Manufacturer<br>Website                                |
|-----------------|------------------------------|----------------------|------------------------------|--|
| SW6             | 8-position rocker DIP switch | Grayhill Corporation | 76SB08ST                     | <a href="http://www.grayhill.com">www.grayhill.com</a> |

## User-Defined LEDs

The board includes general, HSMC, and DDR2 user-defined LEDs. This section discusses all user-defined LEDs.



For information about board specific or status LEDs, refer to “Status Elements” on page 2-17.

### General User-Defined LEDs

Board references D26 through D33 are eight user LEDs, which allow status and debugging signals to be driven to LEDs from the FPGA designs loaded into the Cyclone III device. There is no board-specific function for these LEDs.

Table 2-27 lists the general user LED reference number, schematic signal name, and corresponding Cyclone III device pin number.

**Table 2-27.** LED Reference Number, Schematic Signal Name, and Cyclone III Device Pin Number (Part 1 of 2)

| LED Board<br>Reference | Description      | I/O Standard | Schematic Signal<br>Name | Cyclone III Device<br>Pin Number |
|------------------------|------------------|--------------|--------------------------|----------------------------------|
| D26                    | User-defined LED | 1.8 V        | USER_LED7                | AF19                             |
| D27                    | User-defined LED | 1.8 V        | USER_LED6                | AG19                             |
| D28                    | User-defined LED | 1.8 V        | USER_LED5                | AC17                             |
| D29                    | User-defined LED | 1.8 V        | USER_LED4                | AE15                             |
| D30                    | User-defined LED | 1.8 V        | USER_LED3                | AD19                             |
| D31                    | User-defined LED | 1.8 V        | USER_LED2                | AF18                             |

**Table 2-27.** LED Reference Number, Schematic Signal Name, and Cyclone III Device Pin Number (Part 2 of 2)

| LED Board Reference | Description      | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|---------------------|------------------|--------------|-----------------------|-------------------------------|
| D32                 | User-defined LED | 1.8 V        | USER_LED1             | AE20                          |
| D33                 | User-defined LED | 1.8 V        | USER_LED0             | AD15                          |

Table 2-28 lists the general user-defined LED component reference and manufacturing information.

**Table 2-28.** General User-Defined LED Component Reference and Manufacturing Information

| Board Reference | Description                              | Manufacturer | Manufacturing Part Number | Manufacturer Website                             |
|-----------------|--|--------------|---------------------------|--|
| D26-D33         | Green LEDs, 1206, SMT, clear lens, 2.1 V | Lumex, Inc.  | SML-LX1206GC-TR           | <a href="http://www.lumex.com">www.lumex.com</a> |

### HSMC User-Defined LEDs

The HSMC cards Port A and Port B have two LEDs located nearby. There are no board-specific functions for the HSMC LEDs; however, the HSMC LEDs are labeled TX and RX, and are intended to display data flow to and from connected HSMC cards. The LEDs are driven by the Cyclone III device.

Table 2-29 lists the HSMC user-defined LED board reference number, schematic signal name, and corresponding Cyclone III device pin number.

**Table 2-29.** HSMC User LEDs

| Board Reference | Description   | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|---|--------------|-----------------------|-------------------------------|
| D12             | User-defined but labeled TX in silk-screen for HSMC Port A. | 1.8 V        | HSMA_TX_LED           | AA3                           |
| D14             | User-defined but labeled RX in silk-screen for HSMC Port A. | 1.8 V        | HSMA_RX_LED           | AE1                           |
| D13             | User-defined but labeled TX in silk-screen for HSMC Port B. | 1.8 V        | HSMB_TX_LED           | D28                           |
| D15             | User-defined but labeled RX in silk-screen for HSMC Port B. | 1.8 V        | HSMB_RX_LED           | F26                           |

Table 2-30 lists the HSMC user-defined LED component reference and manufacturing information.

**Table 2-30.** HSMC User-Defined LED Component Reference and Manufacturing Information

| Board Reference | Description                             | Manufacturer | Manufacturing Part Number | Manufacturer Website                             |
|-----------------|---|--------------|---------------------------|--|
| D12-D15         | Green LED, 1206, SMT, clear lens, 2.1 V | Lumex, Inc.  | SML-LX1206GC-TR           | <a href="http://www.lumex.com">www.lumex.com</a> |

## DDR2 User-Defined LEDs

Each channel of DDR2 memory has an LED near the respective DDR2 device. There is no board-specific function for these LEDs; however, they are labeled `DDR2TOP_ACTIVE` and `DDR2BOT_ACTIVE` on the silkscreen and are intended to be illuminated when each respective memory channel is being accessed. The LEDs are driven by the Cyclone III device.

Table 2-31 lists the DDR2 user-defined LED board reference number, schematic signal name, and corresponding Cyclone III device pin number.

**Table 2-31.** DDR2 User—Defined LEDs

| Board Reference | Schematic Signal Name | Cyclone III Device Pin Number  |
|-----------------|-----------------------|--|
| D11             | DDR2TOP_ACTIVE        | User defined but labeled <code>DDR2TOP_ACTIVE</code> on the silkscreen for DDR2TOP memory channel. |
| D16             | DDR2BOT_ACTIVE        | User defined but labeled <code>DDR2BOT_ACTIVE</code> in silkscreen for DDR2BOT memory channel.     |

Table 2-32 lists the memory user-defined LED component reference and manufacturing information.

**Table 2-32.** Memory User-Defined LED Component Reference and Manufacturing Information

| Board Reference | Description                            | Manufacturer | Manufacturing Part Number | Manufacturer Website                             |
|-----------------|--|--------------|---------------------------|--|
| D11 and D16     | Green LED, 1206, SMT, clear lens 2.1 V | Lumex, Inc.  | SML-LX1206GC-TR           | <a href="http://www.lumex.com">www.lumex.com</a> |

## 7-Segment Displays

This section discusses the following two on-board displays:

- User 7-segment display
- Power 7-segment display

### User 7-Segment Display

Board reference U30 is a four-digit, user-defined, 7-segment display that is labeled User Display. Each segment's LED driver input signals are multiplexed to each of the four digits and a minus sign. A small HDL code snippet continuously writes to each of the four segments so that they appear constantly illuminated.


Table 2-33 lists the 7-segment display pin-out.

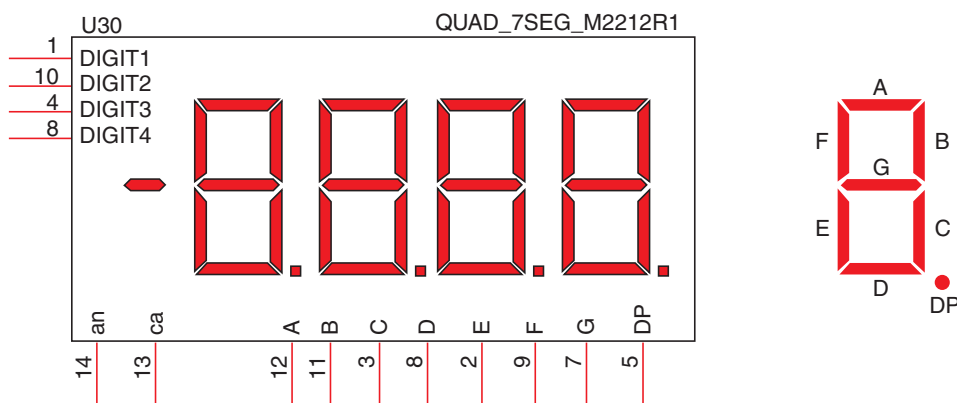
**Table 2-33.** 7-Segment Display Pin-Out (Part 1 of 2)

| Board Reference | Description                 | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Name |
|-----------------|-----------------------------|--------------|-----------------------|-----------------------------|
| U30 pin 12      | User-defined display signal | 1.8 V        | SEVEN_SEG_A           | AD5                         |
| U30 pin 11      | User-defined display signal | 1.8 V        | SEVEN_SEG_B           | A3                          |
| U30 pin 3       | User-defined display signal | 1.8 V        | SEVEN_SEG_C           | C4                          |
| U30 pin 8       | User-defined display signal | 1.8 V        | SEVEN_SEG_D           | D4                          |

**Table 2-33.** 7-Segment Display Pin-Out (Part 2 of 2)

| Board Reference | Description                        | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Name |
|-----------------|------------------------------------|--------------|-----------------------|-----------------------------|
| U30 pin 9       | User-defined display signal        | 1.8 V        | SEVEN_SEG_E           | E5                          |
| U30 pin 7       | User-defined display signal        | 1.8 V        | SEVEN_SEG_F           | D5                          |
| U30 pin 5       | User-defined display signal        | 1.8 V        | SEVEN_SEG_G           | AE6                         |
| U30 pin 2       | User-defined display signal        | 1.8 V        | SEVEN_SEG_DP          | AD4                         |
| U30 pin 13      | User-defined display signal        | 1.8 V        | SEVEN_SEG_SEL1        | B3                          |
| U30 pin 1       | User-defined display select signal | 1.8 V        | SEVEN_SEG_SEL2        | C5                          |
| U30 pin 10      | User-defined display select signal | 1.8 V        | SEVEN_SEG_SEL3        | E4                          |
| U30 pin 4       | User-defined display select signal | 1.8 V        | SEVEN_SEG_SEL4        | C3                          |
| U30 pin 6       | User-defined display select signal | 1.8 V        | SEVEN_SEG_MINUS       | G19                         |

 The four-pin, 7-segment display uses fewer pins than 2-digit, 7-segment displays. See [Figure 2-7](#).

**Figure 2-7.** 7-Segment Display

[Table 2-34](#) lists the 7-segment display component reference and manufacturing information.

**Table 2-34.** 7-Segment Display Component Reference and Manufacturing Information

| Board Reference | Description                  | Manufacturer | Manufacturing Part Number | Manufacturer Website                             |
|-----------------|------------------------------|--------------|---------------------------|--|
| U30             | 7-segment, green LED display | Lumex, Inc.  | LDQ-M2212R1               | <a href="http://www.lumex.com">www.lumex.com</a> |

### Power 7-Segment Display

The power measured by the MAX II CPLD and associated A/D is displayed on board reference U28, which is a dedicated 7-segment display connected to the MAX II CPLD, labeled *Power Display*.

[Table 2-35](#) lists the power 7-segment display component reference and manufacturing information.

**Table 2-35.** Power 7-Segment Display Component Reference and Manufacturing Information

| Board Reference | Description                  | Manufacturer | Manufacturing Part Number | Manufacturer Website                             |
|-----------------|------------------------------|--------------|---------------------------|--|
| U28             | 7-segment, green LED display | Lumex, Inc.  | LDQ-M2212R1               | <a href="http://www.lumex.com">www.lumex.com</a> |

## LCD Displays

The development board is designed to accommodate two separate displays:

- Character LCD
- Graphics LCD

The first display is a 16-character, by 2-line LCD display. The second is a 128 × 64 pixel transmissive graphics LCD. These two share a common bus but have separate control signals so they can operate simultaneously. This section describes both displays.

### Character LCD (J4)

The board contains a single 14-pin 0.1" pitch dual-row header, used to interface to a 16-character by 2-line LCD display, Lumex (part number LCM-S01602DSR/C). The LCD has a 14-pin receptacle that mounts directly to the board's 14-pin header, so it can be easily removed for access to components under the display—or to use the header for debugging or other purposes.

Table 2-36 summarizes the character LCD interface pins. Signal name and direction are relative to the Cyclone III FPGA. For functional descriptions, see Table 2-37.

**Table 2-36.** Character LCD Header I/O

| Board Reference | Description             | I/O Standard | Schematic Signal Name | Cyclone III Pin Number |
|-----------------|-------------------------|--------------|-----------------------|------------------------|
| J22 pin 7       | LCD data bus bit 0      | 2.5 V        | LCD_DATA0             | AA4                    |
| J22 pin 8       | LCD data bus bit 1      | 2.5 V        | LCD_DATA1             | AD1                    |
| J22 pin 9       | LCD data bus bit 2      | 2.5 V        | LCD_DATA2             | V8                     |
| J22 pin 10      | LCD data bus bit 3      | 2.5 V        | LCD_DATA3             | AB5                    |
| J22 pin 11      | LCD data bus bit 4      | 2.5 V        | LCD_DATA4             | AE2                    |
| J22 pin 12      | LCD data bus bit 5      | 2.5 V        | LCD_DATA5             | V5                     |
| J22 pin 13      | LCD data bus bit 6      | 2.5 V        | LCD_DATA6             | V6                     |
| J22 pin 14      | LCD data bus bit 7      | 2.5 V        | LCD_DATA7             | AB3                    |
| J22 pin 4       | LCD data/command select | 2.5 V        | LCD_D_Cn              | D27                    |
| J22 pin 5       | LCD write enable        | 2.5 V        | LCD_D_WEn             | AC4                    |
| J22 pin 6       | LCD chip select         | 2.5 V        | LCD_D_CS <sub>n</sub> | AB24                   |

Table 2-37 shows pin definitions, and is an excerpt from the Lumex data sheet.



For more information such as timing, character maps, interface guidelines, and related documentation, visit [www.lumex.com](http://www.lumex.com).

**Table 2-37.** Character LCD Display Pin Definitions

| Pin Number | Symbol   | Level     | Function  |               |
|------------|----------|-----------|---|---------------|
| 1          | $V_{DD}$ | —         | Power supply  | 5 V           |
| 2          | $V_{SS}$ | —         |   | GND (0 V)     |
| 3          | $V_0$    | —         |   | For LCD drive |
| 4          | RS       | H/L       | Register select signal<br>H: Data input<br>L: Instruction input |               |
| 5          | R/W      | H/L       | H: Data read (module to MPU)<br>L: Data write (MPU to module)   |               |
| 6          | E        | H, H to L | Enable  |               |
| 7~14       | DB0~DB7  | H/L       | Data bus, software selectable 4 or 8 bit mode                   |               |

Figure 2-8 shows a functional block diagram of the Lumex LCD display device. The 8-bit data bus is shared with the graphics LCD, but the control signals are all separate.



The particular model used does not have a backlight and the LCD drive pin is not connected.

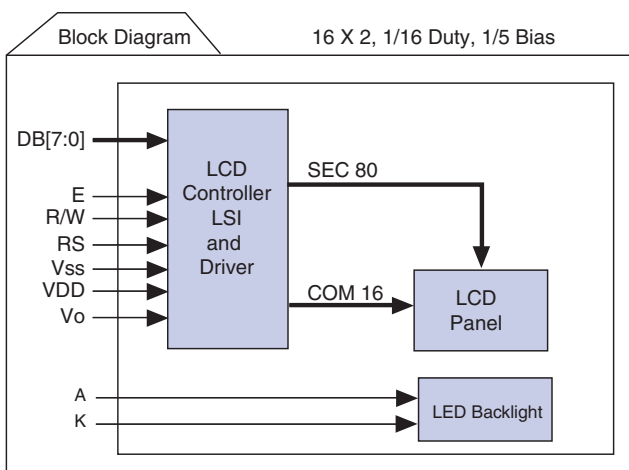
**Figure 2-8.** LCD Display Block Diagram

Table 2-38 lists the character LCD display component reference and manufacturing information.

**Table 2-38.** Character LCD Display Component Reference and Manufacturing Information

| Board Reference | Description                                | Manufacturer | Manufacturing Part Number | Manufacturer Website                               |
|-----------------|--|--------------|---------------------------|--|
| J4              | 2 × 7 pin, 100 mil, vertical header        | Samtec       | TSM-107-01-G-DV           | <a href="http://www.samtec.com">www.samtec.com</a> |
|                 | 2 × 16 character display, 5 × 8 dot matrix | Lumex        | LCM-S01602DSR/C           | <a href="http://www.lumex.com">www.lumex.com</a>   |



## Graphics LCD (J13)

The board contains a 30-pin, fine-pitch connector to interface directly to a 128 × 64 dot matrix graphics LCD display via a flex-cable that is soldered to the display itself. The display is an Optrex part number F-51852GNFQJ-LB-AIN (blue pixels) or F-51852GNFQJ-LB-CAN (green pixels). The pin-out of this interface connector is compatible with a variety of displays.



The data signals are bused with the 14-pin LCD header.



For the graphics LCD data sheet and related documentation, visit [www.optrex.com](http://www.optrex.com).

Table 2-39 lists the graphics LCD pin name, description, and type. Signal name and direction are relative to the Cyclone III FPGA.

**Table 2-39.** Graphics LCD Interface I/O

| Board Reference | Description  | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|--|--------------|-----------------------|-------------------------------|
| J13 pin 6       | LCD data bus bit 0   | 2.5 V        | LCD_DATA0             | AA4                           |
| J13 pin 7       | LCD data bus bit 1   | 2.5 V        | LCD_DATA1             | AD1                           |
| J13 pin 8       | LCD data bus bit 2   | 2.5 V        | LCD_DATA2             | V8                            |
| J13 pin 9       | LCD data bus bit 3   | 2.5 V        | LCD_DATA3             | AB5                           |
| J13 pin 10      | LCD data bus bit 4   | 2.5 V        | LCD_DATA4             | AE2                           |
| J13 pin 11      | LCD data bus bit 5   | 2.5 V        | LCD_DATA5             | V5                            |
| J13 pin 12      | LCD data bus bit 6 _or SCLK  | 2.5 V        | LCD_DATA6             | V6                            |
| J13 pin 13      | LCD data bus bit 7 _or SDATA                                       | 2.5 V        | LCD_DATA7             | AB3                           |
| J13 pin 28      | Parallel interface selection<br>_high = 68 series, low = 80 series | 2.5 V        | LCD_BS1               | (1)                           |
| J13 pin 1       | LCD chip select  | 2.5 V        | LCD_CS <sub>n</sub>   | AB24                          |
| J13 pin 3       | LCD data/command select  | 2.5 V        | LCD_D_C <sub>n</sub>  | D27                           |
| J13 pin 5       | LCD read enable  | 2.5 V        | LCD_E_RD <sub>n</sub> | V7                            |
| J13 pin 2       | LCD reset  | 2.5 V        | LCD_RST <sub>n</sub>  | H7                            |
| J13 pin 29      | LCD parallel/serial data select                                    | 2.5 V        | LCD_SER <sub>n</sub>  | (1)                           |
| J13 pin 4       | LCD write enable   | 2.5 V        | LCD_WE <sub>n</sub>   | AC4                           |

**Note to Table 2-39:**

(1) For the corresponding Cyclone III device pin number, refer to the MAX II device pin-out information in Table 2-5 on page 2-7.



For more information about the data sheet and related documentation, visit Lumex at [www.lumex.com](http://www.lumex.com).

Table 2–40 is an excerpt from the OPTREX data sheet showing pin definitions for both serial and parallel interfaces. The included display has a parallel interface.

**Table 2–40.** Graphics LCD Pin Definitions

| Pin Number | Parallel I/F     |  |
|------------|------------------|--|
|            | Name             | Description  |
| 1          | CS1              | Chip select signal L: active   |
| 2          | RES              | Reset signal L: reset  |
| 3          | A0               | H: D0 to D7 are display data; L: D0 to D7 are instructions   |
| 4          | WR               | 80 family CPU: reset signal L: active  |
| 5          | RD               | 80 family CPU: reset signal L: active  |
| 6          | D0               | Display data   |
| 7          | D1               | Display data   |
| 8          | D2               | Display data   |
| 9          | D3               | Display data   |
| 10         | D4               | Display data   |
| 11         | D5               | Display data   |
| 12         | D6(SCL)          | Display data (serial data clock signal input)  |
| 13         | D7(S1)           | Display data (serial data input)   |
| 14         | V <sub>D0</sub>  | Power supply for logic   |
| 15         | V <sub>SS</sub>  | Power supply (0 V <sub>GND</sub> )   |
| 16         | V <sub>OUT</sub> | DC/DC voltage converter output   |
| 17         | C3-              | DC/DC voltage converter negative connection  |
| 18         | C1+              | DC/DC voltage converter positive connection  |
| 19         | C1-              | DC/DC voltage converter negative connection  |
| 20         | C2-              | DC/DC voltage converter negative connection  |
| 21         | C2+              | DC/DC voltage converter positive connection  |
| 22         | V <sub>1</sub>   | Power supply for LCD drive $V_1 = 1/9 \cdot V_S$   |
| 23         | V <sub>2</sub>   | Power supply for LCD drive $V_2 = 2/9 \cdot V_S$   |
| 24         | V <sub>3</sub>   | Power supply for LCD drive $V_3 = 7/9 \cdot V_S$   |
| 25         | V <sub>4</sub>   | Power supply for LCD drive $V_4 = 8/9 \cdot V_S$   |
| 26         | V <sub>5</sub>   | Power supply for LCD drive V <sub>5</sub> , V <sub>OUT</sub>   |
| 27         | V <sub>R</sub>   | Voltage adjustment pin. Applies voltage between V <sub>CC</sub> and V <sub>S</sub> using a resistive divider |
| 28         | C86              | Interface mode select signal H:68 series L: 80 series  |
| 29         | P/S              | Parallel/serial data select signal H: parallel L: serial   |
| 30         | N/C              | Non-connection   |



Board defaults graphics LCD interface to 80 series CPU mode and parallel interface. These defaults can be modified by writing to the appropriate register in the MAX II CPLD using the FSM bus.

Figure 2-9 is an excerpt from the OPTREX data sheet showing the control chip in the LCD module. The control chip is from New Japan Radio Corporation (part number NJU6676), and Figure 2-9 illustrates the functional block diagram of the display driver.

For more information, contact Optrex American at [www.optrex.com](http://www.optrex.com) or New Japan Radio at [www.njr.co.jp/index\\_e.htm](http://www.njr.co.jp/index_e.htm).

**Figure 2-9.** Graphics LCD Functional Block Diagram of Display Driver

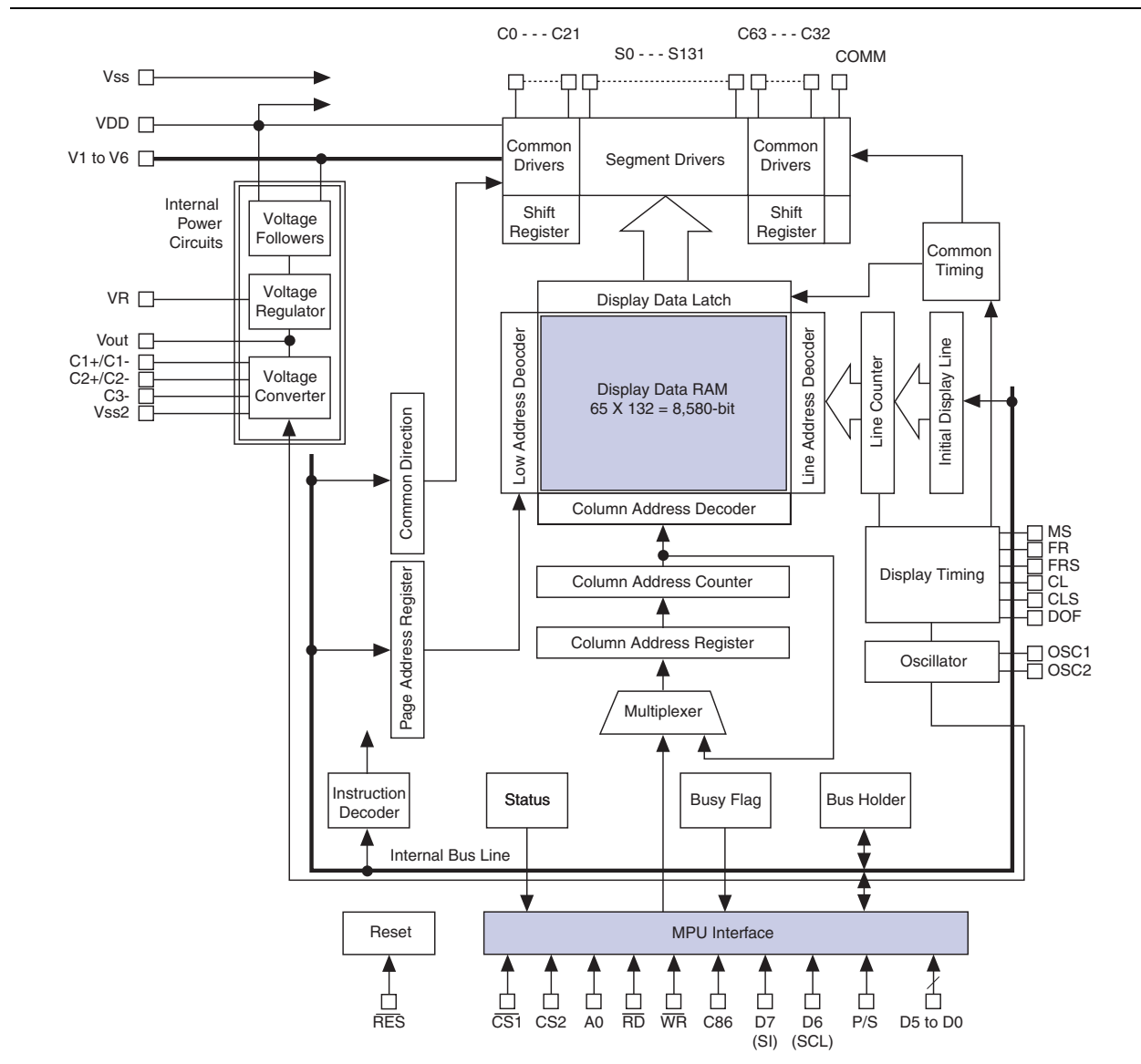
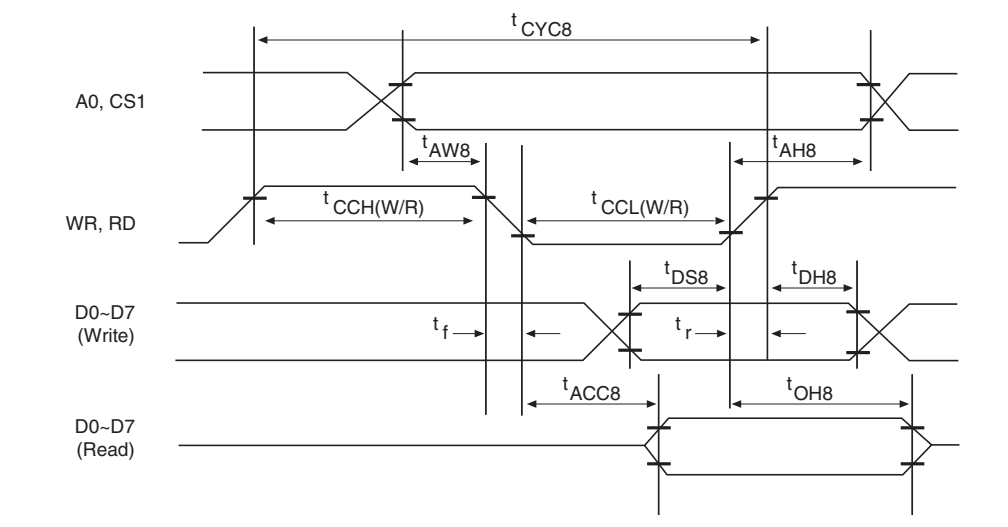


Figure 2–10 is an excerpt from the Optrex data sheet and shows the module interface signals for both read and write transactions.

**Figure 2–10.** Graphics LCD Timing Diagram



For more information about timing parameters, visit [www.optrex.com](http://www.optrex.com).

Table 2–41 lists the graphics LCD display component reference and manufacturing information.

**Table 2–41.** Graphics LCD Display Component Reference and Manufacturing Information

| Board Reference | Description  | Manufacturer            | Manufacturing Part Number | Manufacturer Website                               |
|-----------------|--|-------------------------|---------------------------|--|
| J13             | FPC/FFC 30-position flick lock connector, bottom contact | Hirose Electronics, Co. | FH12S-30S-0.55H(55)       | <a href="http://www.hirose.com">www.hirose.com</a> |
|                 | 128 × 64 graphics module, blue LCD (1)                   | Optrex America, Inc.    | F-51852GNFQJ-LB-AIN       | <a href="http://www.optrex.com">www.optrex.com</a> |
|                 | 128 × 64 graphics module, green LCD (1)                  | Optrex America, Inc.    | F-51852GNFQJ-LG-ACN       | <a href="http://www.optrex.com">www.optrex.com</a> |

**Note to Table 2–41:**

(1) The Cyclone III development board is shipped with either a blue or green Optrex LED display.

## Communication Ports and Interface Cards

This section describes the board's communication ports and interface cards relative to the Cyclone III device.

The board supports the following communication ports:

- USB 2.0 MAC/PHY
- 10/100/1000 Ethernet
- High-speed mezzanine cards

## USB 2.0 MAC/PHY

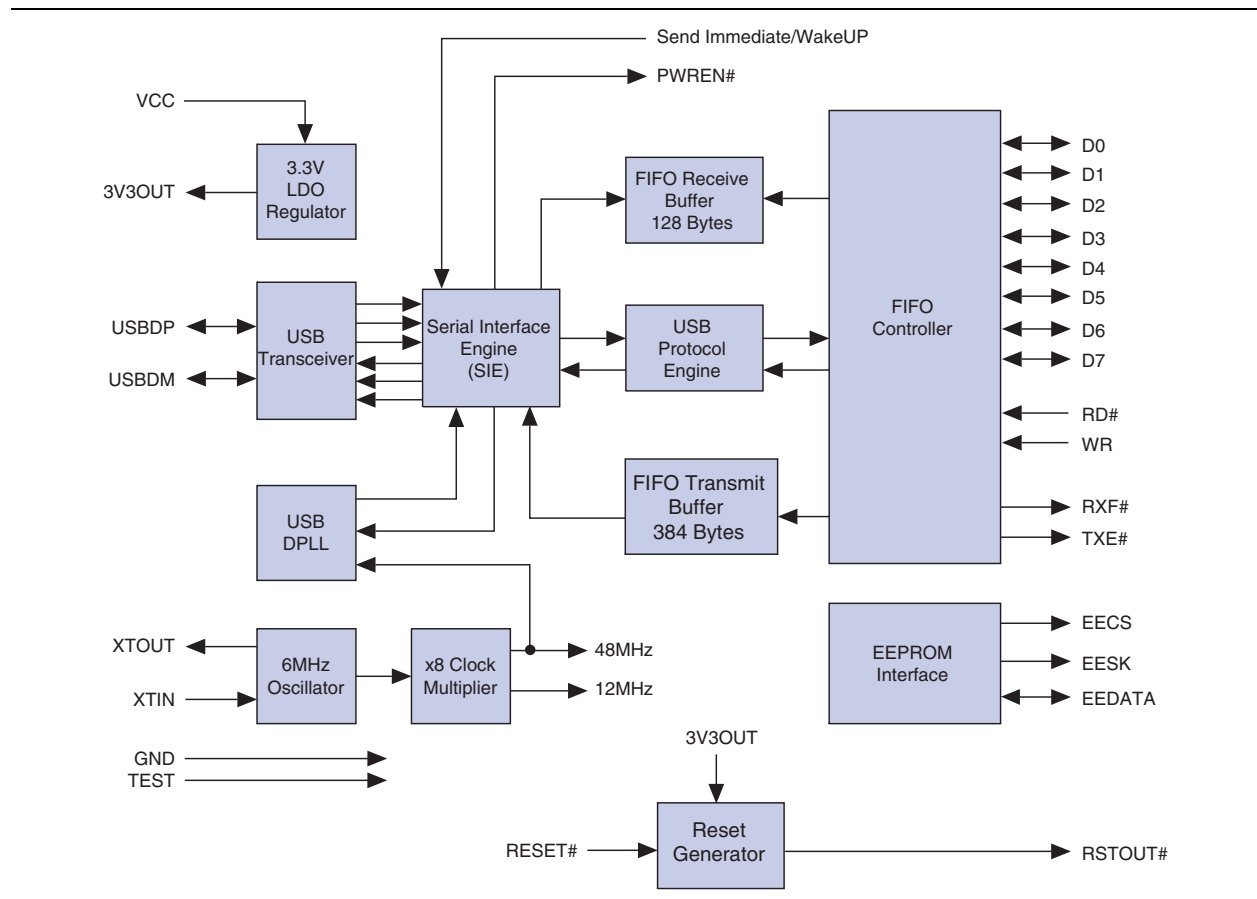
The board incorporates the FTDI USB 2.0 PHY chip. The FT245BL (LQFP package) provides an easy cost-effective method of transferring data to/from a peripheral and a host PC at up to 8 million bits (1 Megabyte) per second (Mbps). The simple, FIFO-like design makes interfacing easier.

The device interfaces to J3, a Type B USB connector similar to those used by common peripherals such as digital cameras and printers. The maximum speed of the interface is 12 Mbps. Typical application speeds are around 1.5 Mbps; however, actual system speed may vary.

The primary usage for the USB device is to provide JTAG programming of on-board devices such as the FPGA and flash memory. The interface is also the default means through which the FPGA connects to host PC applications such as SignalTap® II, DSP Builder, and the Nios II JTAG universal asynchronous receiver/transmitter (UART).

Figure 2-11 shows the functional block diagram of the FTDI USB PHY device.

**Figure 2-11.** FTDI USB PHY Block Diagram



For more information about the data sheet and related documentation, contact FTDI at [www.ftdichip.com](http://www.ftdichip.com).

Table 2–42 lists the FTDI USB interface pins. Signal name and direction are relative to the MAX II CPLD.

**Table 2–42.** FTDI USB PHY Interface I/O

| Signal Names   | Description                | Type                          |
|----------------|----------------------------|-------------------------------|
| USB_FD (7 : 0) | FIFO data bus              | 2.5-V CMOS in/out (8 bit) (1) |
| USB_RDn        | FIFO data bus read enable  | 2.5-V CMOS in (1)             |
| USB_WR         | FIFO data bus write enable | 2.5-V CMOS in (1)             |
| USB_RXFn       | FIFO data bus RX enable    | 2.5-V CMOS out (1)            |
| USB_TXEn       | FIFO data bus TX enable    | 2.5-V CMOS out (1)            |
| USB_EECS       | EEPROM select              | N/A                           |
| USB_EESK       | EEPROM clock               | N/A                           |
| USB_EEDATA     | EEPROM dData               | N/A                           |
| USB_DP         | USB PHY +                  | N/A                           |
| USB_DM         | USB PHY –                  | N/A                           |
| USB_RSTn       | Reset in                   | 2.5-V CMOS output (1)         |
| USB_RSTOUTn    | Reset out                  | 2.5-V CMOS input (1)          |
| USB_XTIN       | 6-MHz crystal input        | N/A                           |
| USB_XTOUT      | 6-MHz crystal output       | N/A                           |
| USB_PWRENn     | Power enable               | 2.5-V CMOS input (1)          |
| USB_SI_WU      | Send immediate / wake up   | 2.5-V CMOS input (1)          |
| VCC            | 5-V core power             | 5.0 V (powered by USB host)   |
| VCCIO          | I/O power                  | 3.3 V                         |
| AVCC           | Analog power               | 1.2 V                         |
| AGND           | Analog ground              | 1.2 V                         |
| GND            | Ground                     | Ground                        |

**Note to Table 2–42:**

(1) The FTDI USB 2.0 device uses 3.3-V LVTTTL levels driving into 2.5-V I/O banks on the MAX II CPLD.

Table 2–43 lists the FTDI USB interface component reference and manufacturing information.

**Table 2–43.** FTDI Interface Component Reference and Manufacturing Information

| Board Reference | Description     | Manufacturer | Manufacturing Part Number | Manufacturer Web Site                                  |
|-----------------|-----------------|--------------|---------------------------|--|
| U8              | FTDI USB device | FTDI Ltd     | FT245BL                   | <a href="http://www.ftdichip.com">www.ftdichip.com</a> |

## 10/100/1000 Ethernet

The 10/100/1000 Ethernet PHY port is provided using a dedicated 10/100/1000 base-T, auto-negotiating Ethernet PHY with reduced Gigabit media independent interface (RGMII) to the FPGA. The target device is the Marvell 88E1111, which uses 2.5-V and 1.2-V power rails. The Marvell 88E1111 requires a 25-MHz reference clock driven from a dedicated oscillator.

The Marvell device is provided for copper RS-45 Ethernet connectivity and comes in the BCC96 leadless chip carrier package. The device interfaces to a HALO HFJ11-1G02E model RJ-45.

The PHY device provides 32 internal management registers that can be accessed using the Management Interface (MDIO). The MDIO address of the PHY device is configured to the value 18 (0x12).

Figure 2–12 shows the interface between the FPGA and the PHY device.

**Figure 2–12.** Interface Between the FPGA and the PHY Device

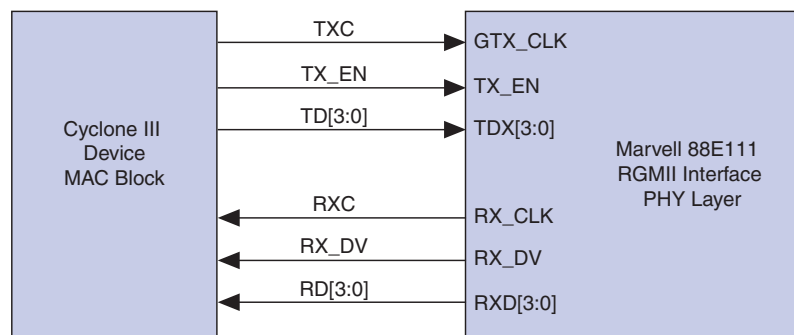


Table 2–44 lists the signal name, description, and I/O standard for the Ethernet PHY interface I/O. The signal name and type are relative to the Cyclone III device, i.e., the I/O setting and direction.

**Table 2–44.** Ethernet PHY Interface I/O (Part 1 of 2)

| Board Reference | Description                             | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|---|--------------|-----------------------|-------------------------------|
| U5 pin 8        | RGMII interface transmit clock          | 2.5 V        | ENET_GTX_CLK          | T8                            |
| U5 pin 73       | 1000 MB link established                | 2.5 V        | ENET_LED_LINK1000     | AC25                          |
| U5 pin 25       | Management bus data clock               | 2.5 V        | ENET_MDC              | N8                            |
| U5 pin 24       | Management bus data                     | 2.5 V        | ENET_MDIO             | L5                            |
| U5 pin 28       | Reset                                   | 2.5 V        | ENET_RESETN           | AD2                           |
| U5 pin 2        | RGMII interface receive clock           | 1.8 V        | ENET_RX_CLK           | B14                           |
| U5 pin 95       | RGMII interface receive data bus bit 0  | 2.5 V        | ENET_RX_D0            | W8                            |
| U5 pin 92       | RGMII interface receive data bus bit 1  | 2.5 V        | ENET_RX_D1            | AA6                           |
| U5 pin 93       | RGMII interface receive data bus bit 2  | 2.5 V        | ENET_RX_D2            | W7                            |
| U5 pin 91       | RGMII interface receive data bus bit 3  | 2.5 V        | ENET_RX_D3            | Y6                            |
| U5 pin 94       | RGMII interface receive control         | 2.5 V        | ENET_RX_DV            | AB4                           |
| U5 pin 11       | RGMII interface transmit data bus bit 0 | 2.5 V        | ENET_TX_D0            | W4                            |

**Table 2-44.** Ethernet PHY Interface I/O (Part 2 of 2)

| Board Reference | Description                             | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|---|--------------|-----------------------|-------------------------------|
| U5 pin 12       | RGMII interface transmit data bus bit 1 | 2.5 V        | ENET_TX_D1            | AA5                           |
| U5 pin 14       | RGMII interface transmit data bus bit 2 | 2.5 V        | ENET_TX_D2            | Y5                            |
| U5 pin 16       | RGMII interface transmit data bus bit 3 | 2.5 V        | ENET_TX_D3            | W3                            |
| U5 pin 9        | RGMII interface transmit control        | 2.5 V        | ENET_TX_EN            | AA7                           |

Table 2-45 is an excerpt from the Marvell data sheet with a summary of RGMII interface signals and their functions.

**Table 2-45.** RGMII Signal Definitions

| Schematic Signal Name | Marvell Device Pin Name | RGMII Spec Pin Name | Description  |
|-----------------------|-------------------------|---------------------|--|
| ENET_GTX_CLK          | GTX_CLK                 | TXC                 | 125-MHz, 25-MHz, or 2.5-MHz transmit clock with $\pm 50$ ppm tolerance based on the selected speed.  |
| ENET_TX_EN            | TX_EN                   | TX_CTL              | Transmit control signals. TX_EN is encoded on the rising edge of GTX_CLK, TX_ER, XORed with TX_EN is encoded on this falling edge of GTX_CLK.  |
| ENET_TXD [3 : 0]      | TXD [3 : 0]             | TD [3 : 0]          | Transmit data. In 1000 base-T and 1000 base-X modes, TXD [3 : 0] are presented on both edges of GTX_CLK. In 100 base-T and 10 base-T modes, TXD [3 : 0] are presented on the rising edge of GTX_CLK. |
| ENET_RX_CLK           | RX_CLK                  | RXC                 | 125-MHz, 25-MHz, or 2.5-MHz receive clock $\pm 50$ ppm tolerance derived from the received data stream and based on the selected speed.  |
| ENET_RX_DV            | RX_DV                   | RX_CTL              | Receive control signals. RX_DV is encoded on the rising edge of RX_CLK, RX_ER, XORed with RX_DV is encoded on the falling edge of RX_CLK.  |
| ENET_RXD [3 : 0]      | RXD [3 : 0]             | RD [3 : 0]          | Receive data. In 1000 base-T and 1000 base-X modes, RXD [3 : 0] are presented on both edges of RX_CLK. In 100 base-TX and 10 base-T modes, RXD [3 : 0] are presented on the rising edge of RX_CLK.   |

Table 2-46 lists the 10/100/1000 Ethernet PHY component reference and manufacturing information.

**Table 2-46.** Ethernet PHY Component Reference and Manufacturing Information

| Board Reference | Description                | Manufacturer          | Manufacturing Part Number | Manufacturer Website                                 |
|-----------------|----------------------------|-----------------------|---------------------------|--|
| U5              | Ethernet PHY Base-T device | Marvell Semiconductor | 88E1111-B2-CAA1C000       | <a href="http://www.marvell.com">www.marvell.com</a> |



For more information about the data sheet and related documentation, contact Marvell at [www.marvell.com](http://www.marvell.com).



## High-Speed Mezzanine Cards

The board contains two HSMC interfaces called Port A and Port B. These HSMC interfaces support both single-ended and differential signaling. The connector part number is Samtec ASP-122953-01. The HSMC interface also allows for JTAG, SMBus, clock outputs and inputs, as well as power for compatible HSMC cards.

The HSMC is an Altera-developed specification, which allows users to expand the functionality of the development board through the addition of daughter cards (HSMC cards).

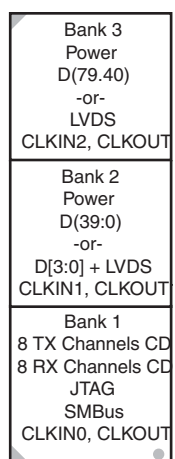


For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, visit [www.altera.com](http://www.altera.com).

The HSMC connector has 172 total pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting as both a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as is done in the QSH-DP/QTH-DP series. Bank 2 and Bank 3 have all of the pins populated as done in the QSH/QTH series.

The Cyclone III development board does not use Bank 1 transceiver signals intended for clock-data-recover (CDR) applications such as PCI Express and Rapid I/O®. These 32 pins are left floating. Banks 2 and 3 are fully supported and can be used in two different configurations. See [Figure 2-13](#).

**Figure 2-13.** HSMC Signal and Bank Diagram



The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to LVDS, mini-LVDS, and RSDS with up to 17-channels full-duplex. Resistor locations are provided for board-level differential termination on designated receiver pairs, but are not installed as CMOS utilization of these pins is the default usage model.



As noted in the HSMC specification, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or the generic differential pin-out.

Table 2-47 lists the HSMC Port A interface signal name, description, and I/O standard. Signal name and direction are relative to the Cyclone III FPGA, which is the HSMC host.

**Table 2-47.** HSMC Port A Interface Signal Name, Description, and Type (Part 1 of 3)

| Board Reference | Description                            | I/O Standard  | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|--|---------------|-----------------------|-------------------------------|
| J8 pin 33       | Management serial data                 | 2.5 V         | HSMA_SDA              | AC1                           |
| J8 pin 34       | Management serial clock                | 2.5 V         | HSMA_SCL              | AC3                           |
| J8 pin 35       | JTAG clock signal                      | 2.5 V         | FPGA_JTAG_TCK         | P5                            |
| J8 pin 36       | JTAG mode select signal                | 2.5 V         | FPGA_JTAG_TMS         | P8                            |
| J8 pin 39       | Dedicated CMOS clock out               | 2.5 V         | HSMA_CLK_OUT0         | Y7                            |
| J8 pin 40       | Dedicated CMOS clock in                | 1.8 V         | HSMA_CLK_IN0          | AG14                          |
| J8 pin 41       | Dedicated CMOS I/O bit 0               | 2.5 V         | HSMA_D0               | AB6                           |
| J8 pin 42       | Dedicated CMOS I/O bit 1               | 2.5 V         | HSMA_D1               | AF2                           |
| J8 pin 43       | Dedicated CMOS I/O bit 2               | 2.5 V         | HSMA_D2               | AE3                           |
| J8 pin 44       | Dedicated CMOS I/O bit 3               | 2.5 V         | HSMA_D3               | AC5                           |
| J8 pin 47       | LVDS TX or CMOS I/O bit 0              | LVDS or 2.5 V | HSMA_TX_D_P0          | R7                            |
| J8 pin 48       | LVDS RX or CMOS I/O bit 0              | LVDS or 2.5 V | HSMA_RX_D_P0          | AB2                           |
| J8 pin 49       | LVDS TX or CMOS I/O bit 0              | LVDS or 2.5 V | HSMA_TX_D_N0          | R6                            |
| J8 pin 50       | LVDS RX or CMOS I/O bit 0              | LVDS or 2.5 V | HSMA_RX_D_N0          | AB1                           |
| J8 pin 53       | LVDS TX bit 1p or CMOS I/O data 8      | LVDS or 2.5 V | HSMA_TX_D_P1          | V4                            |
| J8 pin 54       | LVDS RX bit 1p or CMOS I/O data 9      | LVDS or 2.5 V | HSMA_RX_D_P1          | Y4                            |
| J8 pin 55       | LVDS TX bit 1n or CMOS I/O data bit 10 | LVDS or 2.5 V | HSMA_TX_D_N1          | V3                            |
| J8 pin 56       | LVDS RX bit 1n or CMOS I/O data bit 11 | LVDS or 2.5 V | HSMA_RX_D_N1          | Y3                            |
| J8 pin 59       | LVDS TX bit 2p or CMOS I/O data bit 12 | LVDS or 2.5 V | HSMA_TX_D_P2          | T4                            |
| J8 pin 60       | LVDS RX bit 2p or CMOS I/O data bit 13 | LVDS or 2.5 V | HSMA_RX_D_P2          | U3                            |
| J8 pin 61       | LVDS TX bit 2n or CMOS I/O data bit 14 | LVDS or 2.5 V | HSMA_TX_D_N2          | T3                            |
| J8 pin 62       | LVDS RX bit 2n or CMOS I/O data bit 15 | LVDS or 2.5 V | HSMA_RX_D_N2          | U4                            |
| J8 pin 65       | LVDS TX bit 3p or CMOS I/O data bit 16 | LVDS or 2.5 V | HSMA_TX_D_P3          | R3                            |
| J8 pin 66       | LVDS RX bit 3p or CMOS I/O data bit 17 | LVDS or 2.5 V | HSMA_RX_D_P3          | W2                            |
| J8 pin 67       | LVDS TX bit 3n or CMOS I/O data bit 18 | LVDS or 2.5 V | HSMA_TX_D_N3          | R4                            |
| J8 pin 68       | LVDS RX bit 3n or CMOS I/O data bit 19 | LVDS or 2.5 V | HSMA_RX_D_N3          | W1                            |
| J8 pin 71       | LVDS TX bit 4p or CMOS I/O data bit 20 | LVDS or 2.5 V | HSMA_TX_D_P4          | M8                            |
| J8 pin 72       | LVDS RX bit 4p or CMOS I/O data bit 21 | LVDS or 2.5 V | HSMA_RX_D_P4          | V2                            |
| J8 pin 73       | LVDS TX or 4n CMOS I/O data bit 22     | LVDS or 2.5 V | HSMA_TX_D_N4          | M7                            |
| J8 pin 74       | LVDS RX 4n or CMOS I/O data bit 23     | LVDS or 2.5 V | HSMA_RX_D_N4          | V1                            |
| J8 pin 77       | LVDS TX 5p or CMOS I/O data bit 24     | LVDS or 2.5 V | HSMA_TX_D_P5          | P2                            |
| J8 pin 78       | LVDS RX 5p or CMOS I/O data bit 25     | LVDS or 2.5 V | HSMA_RX_D_P5          | U2                            |

**Table 2-47.** HSMC Port A Interface Signal Name, Description, and Type (Part 2 of 3)

| Board Reference | Description                         | I/O Standard  | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|-------------------------------------|---------------|-----------------------|-------------------------------|
| J8 pin 79       | LVDS TX 5n or CMOS I/O data bit 26  | LVDS or 2.5 V | HSMA_TX_D_N5          | P1                            |
| J8 pin 80       | LVDS RX 5n or CMOS I/O data bit 27  | LVDS or 2.5 V | HSMA_RX_D_N5          | U1                            |
| J8 pin 83       | LVDS TX 6p or CMOS I/O data bit 28  | LVDS or 2.5 V | HSMA_TX_D_P6          | M4                            |
| J8 pin 84       | LVDS RX 6p or CMOS I/O data bit 29  | LVDS or 2.5 V | HSMA_RX_D_P6          | U6                            |
| J8 pin 85       | LVDS TX 6n or CMOS I/O data bit 30  | LVDS or 2.5 V | HSMA_TX_D_N6          | M3                            |
| J8 pin 86       | LVDS RX 6n or CMOS I/O data bit 31  | LVDS or 2.5 V | HSMA_RX_D_N6          | U5                            |
| J8 pin 89       | LVDS TX 7p or CMOS I/O data bit 32  | LVDS or 2.5 V | HSMA_TX_D_P7          | M2                            |
| J8 pin 90       | LVDS RX 7p or CMOS I/O data bit 33  | LVDS or 2.5 V | HSMA_RX_D_P7          | R2                            |
| J8 pin 91       | LVDS TX 7n or CMOS I/O data bit 34  | LVDS or 2.5 V | HSMA_TX_D_N7          | M1                            |
| J8 pin 92       | LVDS RX 7n or CMOS I/O data bit 35  | LVDS or 2.5 V | HSMA_RX_D_N7          | R1                            |
| J8 pin 95       | LVDS or CMOS clock out              | LVDS or 2.5 V | HSMA_CLK_OUT_P1       | G6                            |
| J8 pin 96       | LVDS or CMOS clock in               | LVDS or 2.5 V | HSMA_CLK_IN_P1        | Y2                            |
| J8 pin 97       | LVDS or CMOS clock out              | LVDS or 2.5 V | HSMA_CLK_OUT_N1       | G5                            |
| J8 pin 98       | LVDS or CMOS clock in               | LVDS or 2.5 V | HSMA_CLK_IN_N1        | Y1                            |
| J8 pin 101      | LVDS TX 8p or CMOS I/O data bit 40  | LVDS or 2.5 V | HSMA_TX_D_P8          | L7                            |
| J8 pin 102      | LVDS RX 8p or CMOS I/O data bit 41  | LVDS or 2.5 V | HSMA_RX_D_P8          | N4                            |
| J8 pin 103      | LVDS TX 8n or CMOS I/O data bit 42  | LVDS or 2.5 V | HSMA_TX_D_N8          | L6                            |
| J8 pin 104      | LVDS RX 8n or CMOS I/O data bit 43  | LVDS or 2.5 V | HSMA_RX_D_N8          | N3                            |
| J8 pin 107      | LVDS TX 9p or CMOS I/O data bit 44  | LVDS or 2.5 V | HSMA_TX_D_N9          | K8                            |
| J8 pin 108      | LVDS RX 9p or CMOS I/O data bit 45  | LVDS or 2.5 V | HSMA_TX_D_P9          | L4                            |
| J8 pin 109      | LVDS TX 9n or CMOS I/O data bit 46  | LVDS or 2.5 V | HSMA_RX_D_P9          | L8                            |
| J8 pin 110      | LVDS RX 9n or CMOS I/O data bit 47  | LVDS or 2.5 V | HSMA_RX_D_N9          | L3                            |
| J8 pin 113      | LVDS TX 10p or CMOS I/O data bit 48 | LVDS or 2.5 V | HSMA_TX_D_P10         | K4                            |
| J8 pin 114      | LVDS RX 10p or CMOS I/O data bit 49 | LVDS or 2.5 V | HSMA_RX_D_P10         | L2                            |
| J8 pin 115      | LVDS TX 10n or CMOS I/O data bit 50 | LVDS or 2.5 V | HSMA_TX_D_N10         | K3                            |
| J8 pin 116      | LVDS RX 10n or CMOS I/O data bit 51 | LVDS or 2.5 V | HSMA_RX_D_N10         | L1                            |
| J8 pin 119      | LVDS TX 11p or CMOS I/O data bit 52 | LVDS or 2.5 V | HSMA_TX_D_P11         | J4                            |
| J8 pin 120      | LVDS RX 11p or CMOS I/O data bit 53 | LVDS or 2.5 V | HSMA_RX_D_P11         | K2                            |
| J8 pin 121      | LVDS TX 11n or CMOS I/O data bit 54 | LVDS or 2.5 V | HSMA_TX_D_N11         | J3                            |
| J8 pin 122      | LVDS RX 11n or CMOS I/O data bit 55 | LVDS or 2.5 V | HSMA_RX_D_N11         | K1                            |
| J8 pin 125      | LVDS TX 12p or CMOS I/O data bit 56 | LVDS or 2.5 V | HSMA_TX_D_P12         | J7                            |
| J8 pin 126      | LVDS RX 12p or CMOS I/O data bit 57 | LVDS or 2.5 V | HSMA_RX_D_P12         | J6                            |
| J8 pin 127      | LVDS TX 12n or CMOS I/O data bit 58 | LVDS or 2.5 V | HSMA_TX_D_N12         | K7                            |
| J8 pin 128      | LVDS RX 12n or CMOS I/O data bit 59 | LVDS or 2.5 V | HSMA_RX_D_N12         | J5                            |
| J8 pin 131      | LVDS TX 13p or CMOS I/O data bit 60 | LVDS or 2.5 V | HSMA_TX_D_P13         | G2                            |
| J8 pin 132      | LVDS RX 13p or CMOS I/O data bit 61 | LVDS or 2.5 V | HSMA_RX_D_P13         | H4                            |
| J8 pin 133      | LVDS TX 13n or CMOS I/O data bit 62 | LVDS or 2.5 V | HSMA_TX_D_N13         | G1                            |
| J8 pin 134      | LVDS RX 13n or CMOS I/O data bit 63 | LVDS or 2.5 V | HSMA_RX_D_N13         | H3                            |

**Table 2-47.** HSMC Port A Interface Signal Name, Description, and Type (Part 3 of 3)

| Board Reference | Description  | I/O Standard  | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|--|---------------|-----------------------|-------------------------------|
| J8 pin 137      | LVDS TX 14p or CMOS I/O data bit 64                              | LVDS or 2.5 V | HSMA_RX_D_P14         | F5                            |
| J8 pin 138      | LVDS TX 14p or CMOS I/O data bit 65                              | LVDS or 2.5 V | HSMA_TX_D_N14         | G4                            |
| J8 pin 139      | LVDS RX 14n or CMOS I/O data bit 66                              | LVDS or 2.5 V | HSMA_TX_D_P14         | F4                            |
| J8 pin 140      | LVDS RX 14n or CMOS I/O data bit 67                              | LVDS or 2.5 V | HSMA_RX_D_N14         | G3                            |
| J8 pin 143      | LVDS RX 15p or CMOS I/O data bit 68                              | LVDS or 2.5 V | HSMA_TX_D_P15         | E2                            |
| J8 pin 144      | LVDS TX 15p or CMOS I/O data bit 69                              | LVDS or 2.5 V | HSMA_RX_D_P15         | F2                            |
| J8 pin 145      | LVDS RX 15n or CMOS I/O data bit 70                              | LVDS or 2.5 V | HSMA_TX_D_N15         | E1                            |
| J8 pin 146      | LVDS TX 15n or CMOS I/O data bit 71                              | LVDS or 2.5 V | HSMA_RX_D_N15         | F1                            |
| J8 pin 149      | LVDS RX 16p or CMOS I/O data bit 72                              | LVDS or 2.5 V | HSMA_TX_D_P16         | D3                            |
| J8 pin 150      | LVDS TX 16p or CMOS I/O data bit 73                              | LVDS or 2.5 V | HSMA_RX_D_P16         | E3                            |
| J8 pin 151      | LVDS TX 16n or CMOS I/O data bit 74                              | LVDS or 2.5 V | HSMA_TX_D_N16         | C2                            |
| J8 pin 152      | LVDS RX 16n or CMOS I/O data bit 75                              | LVDS or 2.5 V | HSMA_RX_D_N16         | F3                            |
| J8 pin 155      | LVDS or CMOS clock out   | LVDS          | HSMA_CLK_OUT_P2       | D2                            |
| J8 pin 156      | LVDS or CMOS clock in  | LVDS          | HSMA_CLK_IN_P2        | J2                            |
| J8 pin 157      | LVDS or CMOS clock out   | 2.5 V         | HSMA_CLK_OUT_N2       | D1                            |
| J8 pin 158      | LVDS or CMOS clock in  | 2.5 V         | HSMA_CLK_IN_N2        | J1                            |
| N/A             | User LED intended to show RX data activity on the HSMC interface | 2.5 V         | HSMA_RX_D_LED         | AE1                           |
| N/A             | User LED intended to show TX data activity on the HSMC interface | 2.5 V         | HSMA_TX_D_LED         | AA3                           |

Table 2-48 lists the HSMC Port B interface signal name, description, and I/O standard. Signal name and direction are relative to the Cyclone III FPGA, which is the HSMC host.

**Table 2-48.** HSMC Port B Interface Signal Name, Description, and Type (Part 1 of 4)

| Board Reference | Description                       | I/O Standard  | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|-----------------------------------|---------------|-----------------------|-------------------------------|
| J9 pin 33       | Management serial data            | 2.5 V         | HSMB_SDA              | H26                           |
| J9 pin 34       | Management serial clock           | 2.5 V         | HSMB_SCL              | H25                           |
| J9 pin 35       | JTAG clock signal                 | 2.5 V         | FPGA_JTAG_TCK         | P5                            |
| J9 pin 36       | JTAG mode select signal           | 2.5 V         | FPGA_JTAG_TMS         | P8                            |
| J9 pin 39       | Dedicated CMOS clock out          | 2.5 V         | HSMB_CLK_OUT0         | J22                           |
| J9 pin 40       | Dedicated CMOS clock in           | 2.5 V         | HSMB_CLK_IN0          | A15                           |
| J9 pin 41       | Dedicated CMOS I/O bit 0          | 2.5 V         | HSMB_D0               | G24                           |
| J9 pin 42       | Dedicated CMOS I/O bit 1          | 2.5 V         | HSMB_D1               | H23                           |
| J9 pin 43       | Dedicated CMOS I/O bit 2          | 2.5 V         | HSMB_D2               | G25                           |
| J9 pin 44       | Dedicated CMOS I/O bit 3          | 2.5 V         | HSMB_D3               | H24                           |
| J9 pin 47       | LVDS TX 0p or CMOS I/O data bit 4 | LVDS or 2.5 V | HSMB_TX_D_P0          | J25                           |
| J9 pin 48       | LVDS RX 0p or CMOS I/O data bit 5 | LVDS or 2.5 V | HSMB_RX_D_P0          | F27                           |

**Table 2-48.** HSMC Port B Interface Signal Name, Description, and Type (Part 2 of 4)

| Board Reference | Description                        | I/O Standard  | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|------------------------------------|---------------|-----------------------|-------------------------------|
| J9 pin 49       | LVDS TX 0n or CMOS I/O data bit 6  | LVDS or 2.5 V | HSMB_TX_D_N0          | J26                           |
| J9 pin 50       | LVDS RX 0n or CMOS I/O data bit 7  | LVDS or 2.5 V | HSMB_RX_D_N0          | F28                           |
| J9 pin 53       | LVDS TX 1p or CMOS I/O data bit 8  | LVDS or 2.5 V | HSMB_TX_D_P1          | L23                           |
| J9 pin 54       | LVDS RX 1p or CMOS I/O data bit 9  | LVDS or 2.5 V | HSMB_RX_D_P1          | G27                           |
| J9 pin 55       | LVDS TX 1n or CMOS I/O data bit 10 | LVDS or 2.5 V | HSMB_TX_D_N1          | L24                           |
| J9 pin 56       | LVDS RX 1n or CMOS I/O data bit 11 | LVDS or 2.5 V | HSMB_RX_D_N1          | G28                           |
| J9 pin 59       | LVDS TX 2p or CMOS I/O data bit 12 | LVDS or 2.5 V | HSMB_TX_D_P2          | M25                           |
| J9 pin 60       | LVDS RX 2p or CMOS I/O data bit 13 | LVDS or 2.5 V | HSMB_RX_D_P2          | K25                           |
| J9 pin 61       | LVDS TX 2n or CMOS I/O data bit 14 | LVDS or 2.5 V | HSMB_TX_D_N2          | M26                           |
| J9 pin 62       | LVDS RX 2n or CMOS I/O data bit 15 | LVDS or 2.5 V | HSMB_RX_D_N2          | K26                           |
| J9 pin 65       | LVDS TX 3p or CMOS I/O data bit 16 | LVDS or 2.5 V | HSMB_TX_D_P3          | N25                           |
| J9 pin 66       | LVDS RX 3p or CMOS I/O data bit 17 | LVDS or 2.5 V | HSMB_RX_D_P3          | K27                           |
| J9 pin 67       | LVDS TX 3n or CMOS I/O data bit 18 | LVDS or 2.5 V | HSMB_TX_D_N3          | N26                           |
| J9 pin 68       | LVDS RX 3n or CMOS I/O data bit 19 | LVDS or 2.5 V | HSMB_RX_D_N3          | K28                           |
| J9 pin 71       | LVDS TX 4p or CMOS I/O data bit 20 | LVDS or 2.5 V | HSMB_TX_D_P4          | R27                           |
| J9 pin 72       | LVDS RX 4p or CMOS I/O data bit 21 | LVDS or 2.5 V | HSMB_RX_D_P4          | L27                           |
| J9 pin 73       | LVDS TX 4n or CMOS I/O data bit 22 | LVDS or 2.5 V | HSMB_TX_D_N4          | R28                           |
| J9 pin 74       | LVDS RX 4n or CMOS I/O data bit 23 | LVDS or 2.5 V | HSMB_RX_D_N4          | L28                           |
| J9 pin 77       | LVDS TX 5p or CMOS I/O data bit 24 | LVDS or 2.5 V | HSMB_TX_D_P5          | R25                           |
| J9 pin 78       | LVDS RX 5p or CMOS I/O data bit 25 | LVDS or 2.5 V | HSMB_RX_D_P5          | M27                           |
| J9 pin 79       | LVDS TX 5n or CMOS I/O data bit 26 | LVDS or 2.5 V | HSMB_TX_D_N5          | R26                           |
| J9 pin 80       | LVDS RX 5n or CMOS I/O data bit 27 | LVDS or 2.5 V | HSMB_RX_D_N5          | M28                           |
| J9 pin 83       | LVDS TX 6p or CMOS I/O data bit 28 | LVDS or 2.5 V | HSMB_TX_D_P6          | U25                           |
| J9 pin 84       | LVDS RX 6p or CMOS I/O data bit 29 | LVDS or 2.5 V | HSMB_RX_D_P6          | P25                           |
| J9 pin 85       | LVDS TX 6n or CMOS I/O data bit 30 | LVDS or 2.5 V | HSMB_TX_D_N6          | U26                           |
| J9 pin 86       | LVDS RX 6n or CMOS I/O data bit 31 | LVDS or 2.5 V | HSMB_RX_D_N6          | P26                           |
| J9 pin 89       | LVDS TX 7p or CMOS I/O data bit 32 | LVDS or 2.5 V | HSMB_TX_D_P7          | V27                           |
| J9 pin 90       | LVDS RX 7p or CMOS I/O data bit 33 | LVDS or 2.5 V | HSMB_RX_D_P7          | P27                           |
| J9 pin 91       | LVDS TX 7n or CMOS I/O data bit 34 | LVDS or 2.5 V | HSMB_TX_D_N7          | V28                           |
| J9 pin 92       | LVDS RX 7n or CMOS I/O data bit 35 | LVDS or 2.5 V | HSMB_RX_D_N7          | P28                           |
| J9 pin 95       | LVDS or CMOS clock out             | LVDS or 2.5 V | HSMB_CLK_OUT_P1       | AC26                          |
| J9 pin 96       | LVDS or CMOS clock in              | LVDS or 2.5 V | HSMB_CLK_IN_P1        | J27                           |
| J9 pin 97       | LVDS or CMOS clock out             | LVDS or 2.5 V | HSMB_CLK_OUT_N1       | AD26                          |
| J9 pin 98       | LVDS or CMOS clock in              | LVDS or 2.5 V | HSMB_CLK_IN_N1        | J28                           |
| J9 pin 101      | LVDS TX 8p or CMOS I/O data bit 40 | LVDS or 2.5 V | HSMB_TX_D_P8          | V25                           |
| J9 pin 102      | LVDS RX 8p or CMOS I/O data bit 41 | LVDS or 2.5 V | HSMB_RX_D_P8          | P21                           |
| J9 pin 103      | LVDS TX 8n or CMOS I/O data bit 42 | LVDS or 2.5 V | HSMB_TX_D_N8          | V26                           |
| J9 pin 104      | LVDS RX 8n or CMOS I/O data bit 43 | LVDS or 2.5 V | HSMB_RX_D_N8          | R21                           |

**Table 2–48.** HSMC Port B Interface Signal Name, Description, and Type (Part 3 of 4)

| Board Reference | Description                         | I/O Standard  | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|-------------------------------------|---------------|-----------------------|-------------------------------|
| J9 pin 107      | LVDS TX 9p or CMOS I/O data bit 44  | LVDS or 2.5 V | HSMB_TX_D_N9          | W25                           |
| J9 pin 108      | LVDS RX 9p or CMOS I/O data bit 45  | LVDS or 2.5 V | HSMB_TX_D_P9          | R22                           |
| J9 pin 109      | LVDS TX 9n or CMOS I/O data bit 46  | LVDS or 2.5 V | HSMB_RX_D_P9          | W26                           |
| J9 pin 110      | LVDS RX 9n or CMOS I/O data bit 47  | LVDS or 2.5 V | HSMB_RX_D_N9          | R23                           |
| J9 pin 113      | LVDS TX 10p or CMOS I/O data bit 48 | LVDS or 2.5 V | HSMB_TX_D_P10         | Y25                           |
| J9 pin 114      | LVDS RX 10p or CMOS I/O data bit 49 | LVDS or 2.5 V | HSMB_RX_D_P10         | T25                           |
| J9 pin 115      | LVDS TX 10n or CMOS I/O data bit 50 | LVDS or 2.5 V | HSMB_TX_D_N10         | Y26                           |
| J9 pin 116      | LVDS RX 10n or CMOS I/O data bit 51 | LVDS or 2.5 V | HSMB_RX_D_N10         | T26                           |
| J9 pin 119      | LVDS TX 11p or CMOS I/O data bit 52 | LVDS or 2.5 V | HSMB_TX_D_P11         | AA25                          |
| J9 pin 120      | LVDS RX 11p or CMOS I/O data bit 53 | LVDS or 2.5 V | HSMB_RX_D_P11         | U27                           |
| J9 pin 121      | LVDS TX 11n or CMOS I/O data bit 54 | LVDS or 2.5 V | HSMB_TX_D_N11         | AA26                          |
| J9 pin 122      | LVDS RX 11n or CMOS I/O data bit 55 | LVDS or 2.5 V | HSMB_RX_D_N11         | U28                           |
| J9 pin 125      | LVDS TX 12p or CMOS I/O data bit 56 | LVDS or 2.5 V | HSMB_TX_D_P12         | AB25                          |
| J9 pin 126      | LVDS RX 12p or CMOS I/O data bit 57 | LVDS or 2.5 V | HSMB_RX_D_P12         | U22                           |
| J9 pin 127      | LVDS TX 12n or CMOS I/O data bit 58 | LVDS or 2.5 V | HSMB_TX_D_N12         | AB26                          |
| J9 pin 128      | LVDS RX 12n or CMOS I/O data bit 59 | LVDS or 2.5 V | HSMB_RX_D_N12         | V22                           |
| J9 pin 131      | LVDS TX 13p or CMOS I/O data bit 60 | LVDS or 2.5 V | HSMB_TX_D_P13         | Y23                           |
| J9 pin 132      | LVDS RX 13p or CMOS I/O data bit 61 | LVDS or 2.5 V | HSMB_RX_D_P13         | W28                           |
| J9 pin 133      | LVDS TX 13n or CMOS I/O data bit 62 | LVDS or 2.5 V | HSMB_TX_D_N13         | Y24                           |
| J9 pin 134      | LVDS RX 13n or CMOS I/O data bit 63 | LVDS or 2.5 V | HSMB_RX_D_N13         | W27                           |
| J9 pin 137      | LVDS TX 14p or CMOS I/O data bit 64 | LVDS or 2.5 V | HSMB_RX_D_P14         | AE27                          |
| J9 pin 138      | LVDS TX 14p or CMOS I/O data bit 65 | LVDS or 2.5 V | HSMB_TX_D_N14         | V23                           |
| J9 pin 139      | LVDS RX 14n or CMOS I/O data bit 66 | LVDS or 2.5 V | HSMB_TX_D_P14         | AE28                          |
| J9 pin 140      | LVDS RX 14n or CMOS I/O data bit 67 | LVDS or 2.5 V | HSMB_RX_D_N14         | V24                           |
| J9 pin 143      | LVDS RX 15p or CMOS I/O data bit 68 | LVDS or 2.5 V | HSMB_TX_D_P15         | W22                           |
| J9 pin 144      | LVDS TX 15p or CMOS I/O data bit 69 | LVDS or 2.5 V | HSMB_RX_D_P15         | AB27                          |
| J9 pin 145      | LVDS RX 15n or CMOS I/O data bit 70 | LVDS or 2.5 V | HSMB_TX_D_N15         | Y22                           |
| J9 pin 146      | LVDS TX 15n or CMOS I/O data bit 71 | LVDS or 2.5 V | HSMB_RX_D_N15         | AB28                          |
| J9 pin 149      | LVDS RX 16p or CMOS I/O data bit 72 | LVDS or 2.5 V | HSMB_TX_D_P16         | V21                           |
| J9 pin 150      | LVDS TX 16p or CMOS I/O data bit 73 | LVDS or 2.5 V | HSMB_RX_D_P16         | AC27                          |
| J9 pin 151      | LVDS TX 16n or CMOS I/O data bit 74 | LVDS or 2.5 V | HSMB_TX_D_N16         | W21                           |
| J9 pin 152      | LVDS RX 16n or CMOS I/O data bit 75 | LVDS or 2.5 V | HSMB_RX_D_N16         | AC28                          |
| J9 pin 155      | LVDS or CMOS clock out              | LVDS          | HSMB_CLK_OUT_P2       | AD27                          |
| J9 pin 156      | LVDS or CMOS clock in               | LVDS          | HSMB_CLK_IN_P2        | Y27                           |
| J9 pin 157      | LVDS or CMOS clock out              | 2.5 V         | HSMB_CLK_OUT_N2       | AD28                          |
| J9 pin 158      | LVDS or CMOS clock in               | 2.5 V         | HSMB_CLK_IN_N2        | Y28                           |



**Table 2-48.** HSMC Port B Interface Signal Name, Description, and Type (Part 4 of 4)

| Board Reference | Description  | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|--|--------------|-----------------------|-------------------------------|
| N/A             | User LED intended to show RX data activity on the HSMC interface | 2.5 V        | HSMB_RX_D_LED         | F26                           |
| N/A             | User LED intended to show TX data activity on the HSMC interface | 2.5 V        | HSMB_TX_D_LED         | D28                           |

The board provides both 12 V and 3.3 V to installed daughter cards up to 18.6 W each. [Table 2-49](#) shows the maximum current allowed per voltage.

**Table 2-49.** HSMC Power Supply

| Voltage | Minimum Current From Host | Minimum Wattage |
|---------|---------------------------|-----------------|
| 12 V    | 1.0 A                     | 12.0 W          |
| 3.3 V   | 2.0 A                     | 6.6 W           |

[Table 2-50](#) lists HSMC component reference and manufacturing information.

**Table 2-50.** HSMC Component Reference and Manufacturing Information

| Board Reference | Description   | Manufacturer | Manufacturing Part Number | Manufacturer Website                               |
|-----------------|---|--------------|---------------------------|--|
| J8 and J9       | High-speed mezzanine card (HSMC), custom version of QSH-DP family high speed socket | Samtec       | ASP-122953-01             | <a href="http://www.samtec.com">www.samtec.com</a> |

## On-Board Memory

This section describes the on-board memory interface support, provides signal name, type, and signal connectivity relative to the Cyclone III device.

The board has the following on-board memory:

- DDR2 SDRAM
- SRAM

### DDR2 SDRAM

The board has 256 MB of dual-channel DDR2 SDRAM memory with a 72-bit data width. These devices use the 1.8-V SSTL signaling standard.

The data bus can be configured as two separate buses of 32 bits each, or a single 32-bit and a single 40-bit bus. One address/control bus is referred to as TOP and the other is referred to as BOT (bottom), as they connect to the respective Cyclone III device edges. The interface comprises four  $\times 16$  devices for the 64-bit datapath, and a single  $\times 8$  device for the ECC bits for a total of 5 devices (3 to TOP, 2 to BOT). The Micron part numbers are MT47H32M16CC-3 for the  $\times 16$  devices and MT47H32M8BP-3 for the  $\times 8$  device.

The two address buses are large enough to support any size JEDEC-compliant DDR2 device, as they have all 16 address pins and all three bank pins connected. The Micron components shipped on the board all have 13 row addresses, 2 bank addresses, and 10 column addresses.



Unused control pins should be left tri-stated to reduce power consumption.

There are three clock pairs driven from the FPGA to the memories. The first two pairs clock two memory devices each. The last clock drives the 5th memory device as well as an additional capacitive load to make all clocks have similar loading.

The maximum frequency is 167 MHz (333 Mbps per pin). The theoretical bandwidth of the entire DDR2 interface is 2667 Mbps plus ECC, or 3,000 Mbps raw throughput.



For more information, visit Micron at [www.micron.com](http://www.micron.com).

The data interface to the FPGA fabric runs at either one-half or one-quarter the physical layer data rate when using the Altera DDR2 MegaCore function, which equates to a doubling or quadrupling of the physical data bus width (144 bits or 288 bits, respectively). For example, a 72-bit interface with a 200-MHz external clock speed can have a 200 MHz 144-bit internal bus or a 100 MHz 288-bit interface.

To allow for the use of memory device ODT functionality, the ODT signal is connected. Because a board-level Class I termination is also available, use of this feature is optional. Termination resistors are approximately 50Ω to match the trace impedance of the signals on the board. Clocks are terminated using a single 100Ω resistor across each P/N pair. Altera recommends using the 50ΩOCT on the FPGA for data, and the 10 mA setting for the address and control pins. The DDR2 devices should use the reduced drive strength setting available as a register option.

Table 2-51 lists the DDR2 interface signal name, description, and I/O standard. Signal name and direction are relative to the Cyclone III FPGA.

**Table 2-51.** DDR2 Interface I/O (Part 1 of 5)

| Board Reference | Description           | I/O Standard   | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|-----------------------|----------------|-----------------------|-------------------------------|
| U25, U26 pin K8 | Differential clock 0n | SSTL18 Class 1 | DDR2_CK_N0            | AF14                          |
| U11, U12 pin K8 | Differential clock 1n | SSTL18 Class 1 | DDR2_CK_N1            | G11                           |
| U13 pin F8      | Differential clock 2n | SSTL18 Class 1 | DDR2_CK_N2            | H19                           |
| U25, U26 pin J8 | Differential clock 0p | SSTL18 Class 1 | DDR2_CK_P0            | AE14                          |
| U11, U12 pin J8 | Differential clock 1p | SSTL18 Class 1 | DDR2_CK_P1            | H12                           |
| U13 pin E8      | Differential clock 2p | SSTL18 Class 1 | DDR2_CK_P2            | J19                           |
| U26 pin F3      | Data mask 0           | SSTL18 Class 1 | DDR2_DM0              | AH19                          |
| U26 pin B3      | Data mask 1           | SSTL18 Class 1 | DDR2_DM1              | AC15                          |
| U25 pin F3      | Data mask 2           | SSTL18 Class 1 | DDR2_DM2              | AF8                           |
| U25 pin B3      | Data mask 3           | SSTL18 Class 1 | DDR2_DM3              | AB9                           |
| U11 pin F3      | Data mask 4           | SSTL18 Class 1 | DDR2_DM4              | B10                           |
| U11 pin B3      | Data mask 5           | SSTL18 Class 1 | DDR2_DM5              | A8                            |
| U12 pin F3      | Data mask 6           | SSTL18 Class 1 | DDR2_DM6              | E15                           |



**Table 2-51.** DDR2 Interface I/O (Part 2 of 5)

| Board Reference | Description | I/O Standard   | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|-------------|----------------|-----------------------|-------------------------------|
| U12 pin B3      | Data mask 7 | SSTL18 Class 1 | DDR2_DM7              | C20                           |
| U13 pin B3      | Data mask 8 | SSTL18 Class 1 | DDR2_DM8              | B23                           |
| U26 pin G8      | Data 0      | SSTL18 Class 1 | DDR2_DQ0              | AG22                          |
| U26 pin G2      | Data 1      | SSTL18 Class 1 | DDR2_DQ1              | AH21                          |
| U26 pin D7      | Data 10     | SSTL18 Class 1 | DDR2_DQ10             | AH18                          |
| U26 pin D3      | Data 11     | SSTL18 Class 1 | DDR2_DQ11             | AH17                          |
| U26 pin D1      | Data 12     | SSTL18 Class 1 | DDR2_DQ12             | AF15                          |
| U26 pin D9      | Data 13     | SSTL18 Class 1 | DDR2_DQ13             | AE17                          |
| U26 pin B1      | Data 14     | SSTL18 Class 1 | DDR2_DQ14             | AF16                          |
| U26 pin B9      | Data 15     | SSTL18 Class 1 | DDR2_DQ15             | AB16                          |
| U25 pin G8      | Data 16     | SSTL18 Class 1 | DDR2_DQ16             | AE11                          |
| U25 pin G2      | Data 17     | SSTL18 Class 1 | DDR2_DQ17             | AG11                          |
| U25 pin H7      | Data 18     | SSTL18 Class 1 | DDR2_DQ18             | AG10                          |
| U25 pin H3      | Data 19     | SSTL18 Class 1 | DDR2_DQ19             | AH11                          |
| U26 pin H7      | Data 2      | SSTL18 Class 1 | DDR2_DQ2              | AH22                          |
| U25 pin H1      | Data 20     | SSTL18 Class 1 | DDR2_DQ20             | AE9                           |
| U25 pin H9      | Data 21     | SSTL18 Class 1 | DDR2_DQ21             | AE12                          |
| U25 pin F1      | Data 22     | SSTL18 Class 1 | DDR2_DQ22             | AF10                          |
| U25 pin F9      | Data 23     | SSTL18 Class 1 | DDR2_DQ23             | AE13                          |
| U25 pin C8      | Data 24     | SSTL18 Class 1 | DDR2_DQ24             | AC8                           |
| U25 pin C2      | Data 25     | SSTL18 Class 1 | DDR2_DQ25             | AH7                           |
| U25 pin D7      | Data 26     | SSTL18 Class 1 | DDR2_DQ26             | AG8                           |
| U25 pin D3      | Data 27     | SSTL18 Class 1 | DDR2_DQ27             | AH8                           |
| U25 pin D1      | Data 28     | SSTL18 Class 1 | DDR2_DQ28             | AG7                           |
| U25 pin D9      | Data 29     | SSTL18 Class 1 | DDR2_DQ29             | AA10                          |
| U26 pin H3      | Data 3      | SSTL18 Class 1 | DDR2_DQ3              | AG21                          |
| U25 pin B1      | Data 30     | SSTL18 Class 1 | DDR2_DQ30             | AF7                           |
| U25 pin B9      | Data 31     | SSTL18 Class 1 | DDR2_DQ31             | AD10                          |
| U11 pin G8      | Data 32     | SSTL18 Class 1 | DDR2_DQ32             | A12                           |
| U11 pin G2      | Data 33     | SSTL18 Class 1 | DDR2_DQ33             | C14                           |
| U11 pin H7      | Data 34     | SSTL18 Class 1 | DDR2_DQ34             | A11                           |
| U11 pin H3      | Data 35     | SSTL18 Class 1 | DDR2_DQ35             | C13                           |
| U11 pin H1      | Data 36     | SSTL18 Class 1 | DDR2_DQ36             | D15                           |
| U11 pin H9      | Data 37     | SSTL18 Class 1 | DDR2_DQ37             | C12                           |
| U11 pin F1      | Data 38     | SSTL18 Class 1 | DDR2_DQ38             | E14                           |
| U11 pin F9      | Data 39     | SSTL18 Class 1 | DDR2_DQ39             | D13                           |
| U26 pin H1      | Data 4      | SSTL18 Class 1 | DDR2_DQ4              | AD17                          |
| U11 pin C8      | Data 40     | SSTL18 Class 1 | DDR2_DQ40             | B7                            |

**Table 2-51.** DDR2 Interface I/O (Part 2 of 5)

| Board Reference | Description | I/O Standard   | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|-------------|----------------|-----------------------|-------------------------------|
| U12 pin B3      | Data mask 7 | SSTL18 Class 1 | DDR2_DM7              | C20                           |
| U13 pin B3      | Data mask 8 | SSTL18 Class 1 | DDR2_DM8              | B23                           |
| U26 pin G8      | Data 0      | SSTL18 Class 1 | DDR2_DQ0              | AG22                          |
| U26 pin G2      | Data 1      | SSTL18 Class 1 | DDR2_DQ1              | AH21                          |
| U26 pin D7      | Data 10     | SSTL18 Class 1 | DDR2_DQ10             | AH18                          |
| U26 pin D3      | Data 11     | SSTL18 Class 1 | DDR2_DQ11             | AH17                          |
| U26 pin D1      | Data 12     | SSTL18 Class 1 | DDR2_DQ12             | AF15                          |
| U26 pin D9      | Data 13     | SSTL18 Class 1 | DDR2_DQ13             | AE17                          |
| U26 pin B1      | Data 14     | SSTL18 Class 1 | DDR2_DQ14             | AF16                          |
| U26 pin B9      | Data 15     | SSTL18 Class 1 | DDR2_DQ15             | AB16                          |
| U25 pin G8      | Data 16     | SSTL18 Class 1 | DDR2_DQ16             | AE11                          |
| U25 pin G2      | Data 17     | SSTL18 Class 1 | DDR2_DQ17             | AG11                          |
| U25 pin H7      | Data 18     | SSTL18 Class 1 | DDR2_DQ18             | AG10                          |
| U25 pin H3      | Data 19     | SSTL18 Class 1 | DDR2_DQ19             | AH11                          |
| U26 pin H7      | Data 2      | SSTL18 Class 1 | DDR2_DQ2              | AH22                          |
| U25 pin H1      | Data 20     | SSTL18 Class 1 | DDR2_DQ20             | AE9                           |
| U25 pin H9      | Data 21     | SSTL18 Class 1 | DDR2_DQ21             | AE12                          |
| U25 pin F1      | Data 22     | SSTL18 Class 1 | DDR2_DQ22             | AF10                          |
| U25 pin F9      | Data 23     | SSTL18 Class 1 | DDR2_DQ23             | AE13                          |
| U25 pin C8      | Data 24     | SSTL18 Class 1 | DDR2_DQ24             | AC8                           |
| U25 pin C2      | Data 25     | SSTL18 Class 1 | DDR2_DQ25             | AH7                           |
| U25 pin D7      | Data 26     | SSTL18 Class 1 | DDR2_DQ26             | AG8                           |
| U25 pin D3      | Data 27     | SSTL18 Class 1 | DDR2_DQ27             | AH8                           |
| U25 pin D1      | Data 28     | SSTL18 Class 1 | DDR2_DQ28             | AG7                           |
| U25 pin D9      | Data 29     | SSTL18 Class 1 | DDR2_DQ29             | AA10                          |
| U26 pin H3      | Data 3      | SSTL18 Class 1 | DDR2_DQ3              | AG21                          |
| U25 pin B1      | Data 30     | SSTL18 Class 1 | DDR2_DQ30             | AF7                           |
| U25 pin B9      | Data 31     | SSTL18 Class 1 | DDR2_DQ31             | AD10                          |
| U11 pin G8      | Data 32     | SSTL18 Class 1 | DDR2_DQ32             | A12                           |
| U11 pin G2      | Data 33     | SSTL18 Class 1 | DDR2_DQ33             | C14                           |
| U11 pin H7      | Data 34     | SSTL18 Class 1 | DDR2_DQ34             | A11                           |
| U11 pin H3      | Data 35     | SSTL18 Class 1 | DDR2_DQ35             | C13                           |
| U11 pin H1      | Data 36     | SSTL18 Class 1 | DDR2_DQ36             | D15                           |
| U11 pin H9      | Data 37     | SSTL18 Class 1 | DDR2_DQ37             | C12                           |
| U11 pin F1      | Data 38     | SSTL18 Class 1 | DDR2_DQ38             | E14                           |
| U11 pin F9      | Data 39     | SSTL18 Class 1 | DDR2_DQ39             | D13                           |
| U26 pin H1      | Data 4      | SSTL18 Class 1 | DDR2_DQ4              | AD17                          |
| U11 pin C8      | Data 40     | SSTL18 Class 1 | DDR2_DQ40             | B7                            |

**Table 2-51.** DDR2 Interface I/O (Part 3 of 5)

| Board Reference | Description   | I/O Standard   | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|---------------|----------------|-----------------------|-------------------------------|
| U11 pin C2      | Data 41       | SSTL18 Class 1 | DDR2_DQ41             | C11                           |
| U11 pin D7      | Data 42       | SSTL18 Class 1 | DDR2_DQ42             | A7                            |
| U11 pin D3      | Data 43       | SSTL18 Class 1 | DDR2_DQ43             | C10                           |
| U11 pin D1      | Data 44       | SSTL18 Class 1 | DDR2_DQ44             | E11                           |
| U11 pin D9      | Data 45       | SSTL18 Class 1 | DDR2_DQ45             | B6                            |
| U11 pin B1      | Data 46       | SSTL18 Class 1 | DDR2_DQ46             | H13                           |
| U11 pin B9      | Data 47       | SSTL18 Class 1 | DDR2_DQ47             | D10                           |
| U12 pin G8      | Data 48       | SSTL18 Class 1 | DDR2_DQ48             | C17                           |
| U12 pin G2      | Data 49       | SSTL18 Class 1 | DDR2_DQ49             | B19                           |
| U26 pin H9      | Data 5        | SSTL18 Class 1 | DDR2_DQ5              | AH23                          |
| U12 pin H7      | Data 50       | SSTL18 Class 1 | DDR2_DQ50             | B18                           |
| U12 pin H3      | Data 51       | SSTL18 Class 1 | DDR2_DQ51             | C19                           |
| U12 pin H1      | Data 52       | SSTL18 Class 1 | DDR2_DQ52             | D20                           |
| U12 pin H9      | Data 53       | SSTL18 Class 1 | DDR2_DQ53             | C16                           |
| U12 pin F1      | Data 54       | SSTL18 Class 1 | DDR2_DQ54             | A19                           |
| U12 pin F9      | Data 55       | SSTL18 Class 1 | DDR2_DQ55             | E17                           |
| U12 pin C8      | Data 56       | SSTL18 Class 1 | DDR2_DQ56             | C21                           |
| U12 pin C2      | Data 57       | SSTL18 Class 1 | DDR2_DQ57             | C22                           |
| U12 pin D7      | Data 58       | SSTL18 Class 1 | DDR2_DQ58             | A21                           |
| U12 pin D3      | Data 59       | SSTL18 Class 1 | DDR2_DQ59             | A22                           |
| U26 pin F1      | Data 6        | SSTL18 Class 1 | DDR2_DQ6              | AE19                          |
| U12 pin D1      | Data 60       | SSTL18 Class 1 | DDR2_DQ60             | C24                           |
| U12 pin D9      | Data 61       | SSTL18 Class 1 | DDR2_DQ61             | B21                           |
| U12 pin B1      | Data 62       | SSTL18 Class 1 | DDR2_DQ62             | D21                           |
| U12 pin B9      | Data 63       | SSTL18 Class 1 | DDR2_DQ63             | E18                           |
| U13 pin C8      | Data 64       | SSTL18 Class 1 | DDR2_DQ64             | E22                           |
| U13 pin C2      | Data 65       | SSTL18 Class 1 | DDR2_DQ65             | C25                           |
| U13 pin D7      | Data 66       | SSTL18 Class 1 | DDR2_DQ66             | A23                           |
| U13 pin D3      | Data 67       | SSTL18 Class 1 | DDR2_DQ67             | B25                           |
| U13 pin D1      | Data 68       | SSTL18 Class 1 | DDR2_DQ68             | A26                           |
| U13 pin D9      | Data 69       | SSTL18 Class 1 | DDR2_DQ69             | F21                           |
| U26 pin F9      | Data 7        | SSTL18 Class 1 | DDR2_DQ7              | AF24                          |
| U13 pin B1      | Data 70       | SSTL18 Class 1 | DDR2_DQ70             | B26                           |
| U13 pin B9      | Data 71       | SSTL18 Class 1 | DDR2_DQ71             | D22                           |
| U26 pin C8      | Data 8        | SSTL18 Class 1 | DDR2_DQ8              | AG18                          |
| U26 pin C2      | Data 9        | SSTL18 Class 1 | DDR2_DQ9              | AG17                          |
| U26 pin F7      | Data strobe 0 | SSTL18 Class 1 | DDR2_DQS0             | AE18                          |
| U26 pin B7      | Data strobe 1 | SSTL18 Class 1 | DDR2_DQS1             | AF17                          |

**Table 2-51.** DDR2 Interface I/O (Part 4 of 5)

| Board Reference             | Description                      | I/O Standard    | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------------------|----------------------------------|-----------------|-----------------------|-------------------------------|
| U25 pin F7                  | Data strobe 2                    | SSTL18 Class 1  | DDR2_DQS2             | AF11                          |
| U25 pin B7                  | Data strobe 3                    | SSTL18 Class 1  | DDR2_DQS3             | AE10                          |
| U11 pin F7                  | Data strobe 4                    | SSTL18 Class 1  | DDR2_DQS4             | D12                           |
| U11 pin B7                  | Data strobe 5                    | SSTL18 Class 1  | DDR2_DQS5             | E12                           |
| U12 pin F7                  | Data strobe 6                    | SSTL18 Class 1  | DDR2_DQS6             | B17                           |
| U12 pin B7                  | Data strobe 7                    | SSTL18 Class 1  | DDR2_DQS7             | D17                           |
| U13 pin B7                  | Data strobe 8                    | SSTL18 Class 1  | DDR2_DQS8             | A25                           |
| U25, U26 pin M8             | Bottom address 0                 | SSTL18 Class 1  | DDR2BOT_A0            | AB22                          |
| U25, U26 pin M3             | Bottom address 1                 | SSTL18 Class 1  | DDR2BOT_A1            | AG6                           |
| U25, U26 pin M2             | Bottom address 10                | SSTL18 Class 1  | DDR2BOT_A10           | AE4                           |
| U25, U26 pin P7             | Bottom address 11                | SSTL18 Class 1  | DDR2BOT_A11           | AF21                          |
| U25, U26 pin R2             | Bottom address 12                | SSTL18 Class 1  | DDR2BOT_A12           | Y12                           |
| U25, U26 pin R8             | Bottom address 13                | SSTL18 Class 1  | DDR2BOT_A13           | Y14                           |
| U25, U26 pin R3             | Bottom address 14                | SSTL18 Class 1  | DDR2BOT_A14           | AF12                          |
| U25, U26 pin R7             | Bottom address 15                | SSTL18 Class 1  | DDR2BOT_A15           | AA16                          |
| U25, U26 pin M7             | Bottom address 2                 | SSTL18 Class 1  | DDR2BOT_A2            | Y13                           |
| U25, U26 pin N2             | Bottom address 3                 | SSTL18 Class 1  | DDR2BOT_A3            | AE7                           |
| U25, U26 pin N8             | Bottom address 4                 | SSTL18 Class 1  | DDR2BOT_A4            | AB12                          |
| U25, U26 pin N3             | Bottom address 5                 | SSTL18 Class 1  | DDR2BOT_A5            | AC7                           |
| U25, U26 pin N7             | Bottom address 6                 | SSTL18 Class 1  | DDR2BOT_A6            | AD12                          |
| U25, U26 pin P2             | Bottom address 7                 | SSTL18 Class 1  | DDR2BOT_A7            | AB8                           |
| U25, U26 pin P8             | Bottom address 8                 | SSTL18 Class 1  | DDR2BOT_A8            | AH12                          |
| U25, U26 pin P3             | Bottom address 9                 | SSTL18 Class 1  | DDR2BOT_A9            | AB10                          |
| LED D16 pin 2               | Bottom bus activity LED          | 1.8 V           | DDR2BOT_ACTIVE        | AA14                          |
| U25, U26 pin L2             | Bottom bank address 0            | SSTL18 Class 1  | DDR2BOT_BA0           | AF3                           |
| U25, U26 pin L3             | Bottom bank address 1            | SSTL18 Class 1  | DDR2BOT_BA1           | AF5                           |
| U25, U26 pin L1             | Bottom bank address 2            | SSTL18 Class 1  | DDR2BOT_BA2           | AH4                           |
| U25, U26 pin L7             | Bottom column address strobe     | SSTL-18 Class I | DDR2BOT_CASn          | AD21                          |
| U25, U26 pin K2             | Bottom clock enable              | SSTL-18 Class I | DDR2BOT_CKE           | AG4                           |
| U25, U26 pin L8             | Bottom chip select               | SSTL-18 Class I | DDR2BOT_CSn           | AC21                          |
| U25, U26 pin K9             | Bottom on-die termination enable | SSTL-18 Class I | DDR2BOT_ODT           | AE24                          |
| U25, U26 pin K7             | Bottom row address strobe        | SSTL-18 Class I | DDR2BOT_RASn          | AE21                          |
| U25, U26 pin K3             | Bottom write enable              | SSTL-18 Class I | DDR2BOT_WEn           | AE5                           |
| U11, U12 pin M8, U13 pin H8 | Top address 0                    | SSTL18 Class 1  | DDR2TOP_A0            | J13                           |
| U11, U12 pin M3, U13 pin H3 | Top address 1                    | SSTL18 Class 1  | DDR2TOP_A1            | G18                           |
| U11, U12 pin M2, U13 pin H2 | Top address 10                   | SSTL18 Class 1  | DDR2TOP_A10           | A17                           |

**Table 2-51.** DDR2 Interface I/O (Part 5 of 5)

| Board Reference             | Description                   | I/O Standard    | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------------------|-------------------------------|-----------------|-----------------------|-------------------------------|
| U11, U12 pin P7, U13 pin K7 | Top address 11                | SSTL18 Class 1  | DDR2TOP_A11           | D8                            |
| U11, U12 pin R2, U13 pin L2 | Top address 12                | SSTL18 Class 1  | DDR2TOP_A12           | D25                           |
| U11, U12 pin R8, U13 pin L8 | Top address 13                | SSTL18 Class 1  | DDR2TOP_A13           | F15                           |
| U11, U12 pin R3, U13 pin L3 | Top address 14                | SSTL18 Class 1  | DDR2TOP_A14           | B12                           |
| U11, U12 pin R7             | Top address 15                | SSTL18 Class 1  | DDR2TOP_A15           | H16                           |
| U11, U12 pin M7, U13 pin H7 | Top address 2                 | SSTL18 Class 1  | DDR2TOP_A2            | E8                            |
| U11, U12 pin N2, U13 pin J2 | Top address 3                 | SSTL18 Class 1  | DDR2TOP_A3            | D24                           |
| U11, U12 pin N8, U13 pin J8 | Top address 4                 | SSTL18 Class 1  | DDR2TOP_A4            | D7                            |
| U11, U12 pin N3, U13 pin J3 | Top address 5                 | SSTL18 Class 1  | DDR2TOP_A5            | J15                           |
| U11, U12 pin N7, U13 pin J7 | Top address 6                 | SSTL18 Class 1  | DDR2TOP_A6            | H15                           |
| U11, U12 pin P2, U13 pin K2 | Top address 7                 | SSTL18 Class 1  | DDR2TOP_A7            | J16                           |
| U11, U12 pin P8, U13 pin K8 | Top address 8                 | SSTL18 Class 1  | DDR2TOP_A8            | H8                            |
| U11, U12 pin P3, U13 pin K3 | Top address 9                 | SSTL18 Class 1  | DDR2TOP_A9            | D16                           |
| LED D11 pin 2               | Top bus activity LED          | 1.8 V           | DDR2TOP_ACTIVE        | E10                           |
| U11, U12 pin L2, U13 pin G2 | Top bank address 0            | SSTL18 Class 1  | DDR2TOP_BA0           | C23                           |
| U11, U12 pin L3, U13 pin G3 | Top bank address 1            | SSTL18 Class 1  | DDR2TOP_BA1           | D19                           |
| U11, U12 pin L1, U13 pin G1 | Top bank address 2            | SSTL18 Class 1  | DDR2TOP_BA2           | C26                           |
| U11, U12 pin L7, U13 pin G7 | Top column address strobe     | SSTL-18 Class I | DDR2TOP_CASn          | F14                           |
| U11, U12 pin K2, U13 pin F2 | Top clock enable              | SSTL-18 Class I | DDR2TOP_CKE           | E21                           |
| U11, U12 pin L8, U13 pin G8 | Top chip select               | SSTL-18 Class I | DDR2TOP_CSn           | C7                            |
| U11, U12 pin K9, U13 pin F9 | Top on-die termination enable | SSTL-18 Class I | DDR2TOP_ODT           | A6                            |
| U11, U12 pin K7, U13 pin F7 | Top row address strobe        | SSTL-18 Class I | DDR2TOP_RASn          | F8                            |
| U11, U12 pin K3, U13 pin F3 | Top write enable              | SSTL-18 Class I | DDR2TOP_WEn           | A10                           |

Table 2-52 lists the DDR2 interface component reference and manufacturing information.

**Table 2-52.** DDR2 Interface Component Reference and Manufacturing Information

| Board Reference    | Description          | Manufacturer            | Manufacturing Part Number | Manufacturer Website                               |
|--------------------|----------------------|-------------------------|---------------------------|--|
| U11, U12, U25, U26 | DDR2 SDRAM 34 M × 16 | Micron Technology, Inc. | MT47H32M16CC-3:B          | <a href="http://www.micron.com">www.micron.com</a> |
| U13                | DDR2 SDRAM 32 M × 8  | Micron Technology, Inc. | MT47H32M8BP-3:B           | <a href="http://www.micron.com">www.micron.com</a> |

## SRAM

The board features 8 MB of SRAM memory with a 32-bit data bus. The devices use 1.8-V CMOS signaling and are optimized for low cost and power.

The 32-bit interface comprises two  $\times 16$  devices. The Samsung part features a maximum frequency of 104 MHz (104 Mbps). The theoretical bandwidth of the entire interface is 416 Mbps.

The SRAM devices are part of a shared bus with connectivity to the MAX II CPLD as well as the flash memory, which is called the FSM bus. All three devices use 1.8-V CMOS signaling. Altera recommends using the 50- $\Omega$  OCT setting on the FPGA and the one-half drive setting on the SRAM.

Table 2-53 lists the SRAM interface signal name, description, and I/O standard. Signal name and type are relative to the Cyclone III device, i.e., I/O setting and direction.

**Table 2-53.** SRAM Interface I/O (Part 1 of 3)

| Board Reference | Description                    | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|--------------------------------|--------------|-----------------------|-------------------------------|
| U23 pin A1      | Byte enables bit 0             | 1.8 V        | SRAM_BEn0             | AF20                          |
| U23 pin B2      | Byte enables bit 1             | 1.8 V        | SRAM_BEn1             | AH26                          |
| U24 pin A1      | Byte enables bit 2             | 1.8 V        | SRAM_BEn2             | AE22                          |
| U24 pin B2      | Byte enables bit 3             | 1.8 V        | SRAM_BEn3             | AB21                          |
| U23, U24 pin J2 | Clock (drives two memories)    | 1.8 V        | SRAM_CLK              | AD22                          |
| U23, U24 pin B5 | Chip select                    | 1.8 V        | SRAM_CS <sub>n</sub>  | AB19                          |
| U23, U24 pin A2 | Output enable                  | 1.8 V        | SRAM_OEn              | AD25                          |
| U23, U24 pin A6 | Power save /MRS set pin        | 1.8 V        | SRAM_PSn              | B4                            |
| U23 pin J1      | Data wait bit 0                | 1.8 V        | SRAM_WAIT0            | AG15                          |
| U24 pin J1      | Data wait bit 1                | 1.8 V        | SRAM_WAIT1            | AH25                          |
| U23, U24 pin G5 | Write enable                   | 1.8 V        | SRAM_WEn              | AE25                          |
| U23, U24 pin J3 | Address valid                  | 1.8 V        | SRAM_ADV <sub>n</sub> | AA19                          |
| U23, U24 pin A3 | Address bit 1 (DWORD aligned)  | 1.8 V        | FSA1                  | AH10                          |
| U23, U24 pin A4 | Address bit 2 (DWORD aligned)  | 1.8 V        | FSA2                  | AA13                          |
| U23, U24 pin A5 | Address bit 3 (DWORD aligned)  | 1.8 V        | FSA3                  | AC10                          |
| U23, U24 pin B3 | Address bit 4 (DWORD aligned)  | 1.8 V        | FSA4                  | Y15                           |
| U23, U24 pin B4 | Address bit 5 (DWORD aligned)  | 1.8 V        | FSA5                  | AF22                          |
| U23, U24 pin C3 | Address bit 6 (DWORD aligned)  | 1.8 V        | FSA6                  | AF26                          |
| U23, U24 pin C4 | Address bit 7 (DWORD aligned)  | 1.8 V        | FSA7                  | AF4                           |
| U23, U24 pin D4 | Address bit 8 (DWORD aligned)  | 1.8 V        | FSA8                  | AD8                           |
| U23, U24 pin H2 | Address bit 9 (DWORD aligned)  | 1.8 V        | FSA9                  | AG26                          |
| U23, U24 pin H3 | Address bit 10 (DWORD aligned) | 1.8 V        | FSA10                 | AH6                           |
| U23, U24 pin H4 | Address bit 11 (DWORD aligned) | 1.8 V        | FSA11                 | AD24                          |
| U23, U24 pin H5 | Address bit 12 (DWORD aligned) | 1.8 V        | FSA12                 | AF9                           |
| U23, U24 pin G3 | Address bit 13 (DWORD aligned) | 1.8 V        | FSA13                 | AA8                           |

**Table 2-53.** SRAM Interface I/O (Part 2 of 3)

| Board Reference | Description                    | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|--------------------------------|--------------|-----------------------|-------------------------------|
| U23, U24 pin G4 | Address bit 14 (DWORD aligned) | 1.8 V        | FSA14                 | AC22                          |
| U23, U24 pin F3 | Address bit 15 (DWORD aligned) | 1.8 V        | FSA15                 | AE8                           |
| U23, U24 pin F4 | Address bit 16 (DWORD aligned) | 1.8 V        | FSA16                 | AF13                          |
| U23, U24 pin E4 | Address bit 17 (DWORD aligned) | 1.8 V        | FSA17                 | AB14                          |
| U23, U24 pin D3 | Address bit 18 (DWORD aligned) | 1.8 V        | FSA18                 | AF23                          |
| U23, U24 pin H1 | Address bit 19 (DWORD aligned) | 1.8 V        | FSA19                 | AG12                          |
| U23, U24 pin G2 | Address bit 20 (DWORD aligned) | 1.8 V        | FSA20                 | AB18                          |
| U23, U24 pin H6 | Address bit 21 (DWORD aligned) | 1.8 V        | FSA21                 | Y19                           |
| U23 pin B6      | Data bit 0                     | 1.8 V        | FSD0                  | J14                           |
| U23 pin C5      | Data bit 1                     | 1.8 V        | FSD1                  | D6                            |
| U23 pin C6      | Data bit 2                     | 1.8 V        | FSD2                  | J17                           |
| U23 pin D5      | Data bit 3                     | 1.8 V        | FSD3                  | G7                            |
| U23 pin E5      | Data bit 4                     | 1.8 V        | FSD4                  | F18                           |
| U23 pin F5      | Data bit 5                     | 1.8 V        | FSD5                  | C6                            |
| U23 pin F6      | Data bit 6                     | 1.8 V        | FSD6                  | H17                           |
| U23 pin G6      | Data bit 7                     | 1.8 V        | FSD7                  | C18                           |
| U23 pin B1      | Data bit 8                     | 1.8 V        | FSD8                  | D18                           |
| U23 pin C1      | Data bit 9                     | 1.8 V        | FSD9                  | G16                           |
| U23 pin C2      | Data bit 10                    | 1.8 V        | FSD10                 | G22                           |
| U23 pin D2      | Data bit 11                    | 1.8 V        | FSD11                 | F12                           |
| U23 pin E2      | Data bit 12                    | 1.8 V        | FSD12                 | D11                           |
| U23 pin F2      | Data bit 13                    | 1.8 V        | FSD13                 | E24                           |
| U23 pin F1      | Data bit 14                    | 1.8 V        | FSD14                 | H21                           |
| U23 pin G1      | Data bit 15                    | 1.8 V        | FSD15                 | G9                            |
| U24 pin B6      | Data bit 16                    | 1.8 V        | FSD16                 | A4                            |
| U24 pin C5      | Data bit 17                    | 1.8 V        | FSD17                 | G13                           |
| U24 pin C6      | Data bit 18                    | 1.8 V        | FSD18                 | H14                           |
| U24 pin D5      | Data bit 19                    | 1.8 V        | FSD19                 | B8                            |
| U24 pin E5      | Data bit 20                    | 1.8 V        | FSD20                 | C8                            |
| U24 pin F5      | Data bit 21                    | 1.8 V        | FSD21                 | F7                            |
| U24 pin F6      | Data bit 22                    | 1.8 V        | FSD22                 | B11                           |
| U24 pin G6      | Data bit 23                    | 1.8 V        | FSD23                 | B22                           |
| U24 pin B1      | Data bit 24                    | 1.8 V        | FSD24                 | A18                           |
| U24 pin C1      | Data bit 25                    | 1.8 V        | FSD25                 | G8                            |
| U24 pin C2      | Data bit 26                    | 1.8 V        | FSD26                 | J12                           |
| U24 pin D2      | Data bit 27                    | 1.8 V        | FSD27                 | D9                            |
| U24 pin E2      | Data bit 28                    | 1.8 V        | FSD28                 | C9                            |
| U24 pin F2      | Data bit 29                    | 1.8 V        | FSD29                 | E7                            |

**Table 2-53.** SRAM Interface I/O (Part 3 of 3)

| Board Reference | Description | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|-------------|--------------|-----------------------|-------------------------------|
| U24 pin F1      | Data bit 30 | 1.8 V        | FSD30                 | H10                           |
| U24 pin G1      | Data bit 31 | 1.8 V        | FSD31                 | J10                           |

Figure 2-14 illustrates the latency for both fixed and variable modes of operation. For asynchronous accesses, each of the two devices has its own WAIT pin wired to the Cyclone III device.



For Samsung SRAM pin definitions, data sheet, and other related documentation, refer to the Samsung website at [www.samsung.com](http://www.samsung.com).

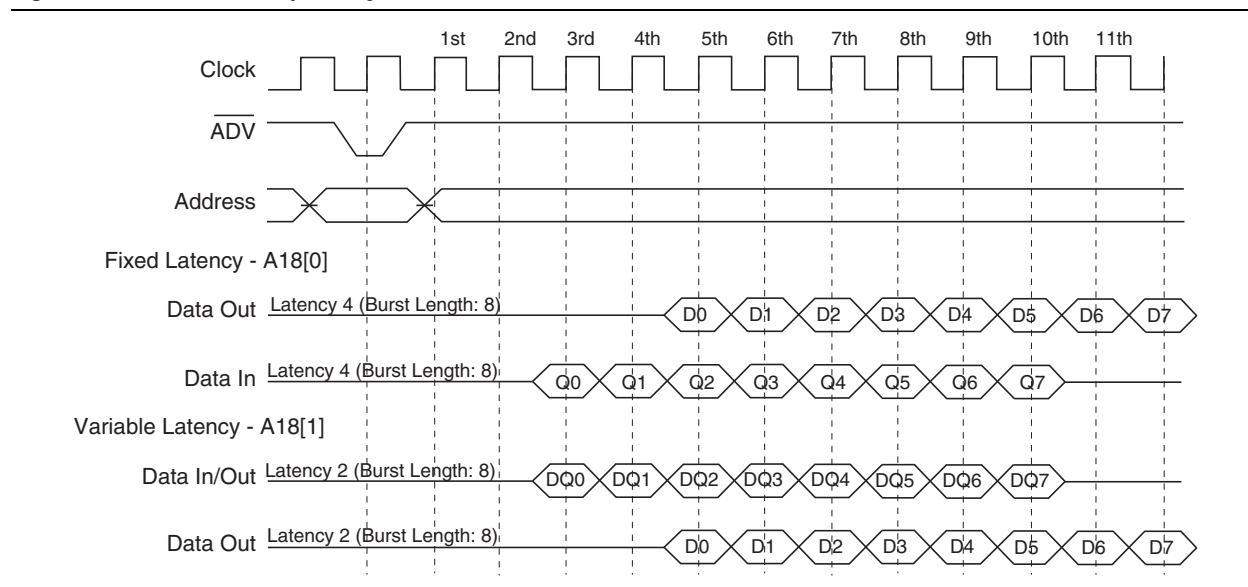
**Figure 2-14.** SRAM Latency Timing Illustration

Table 2-54 lists the Samsung device latency values based on operation frequency.

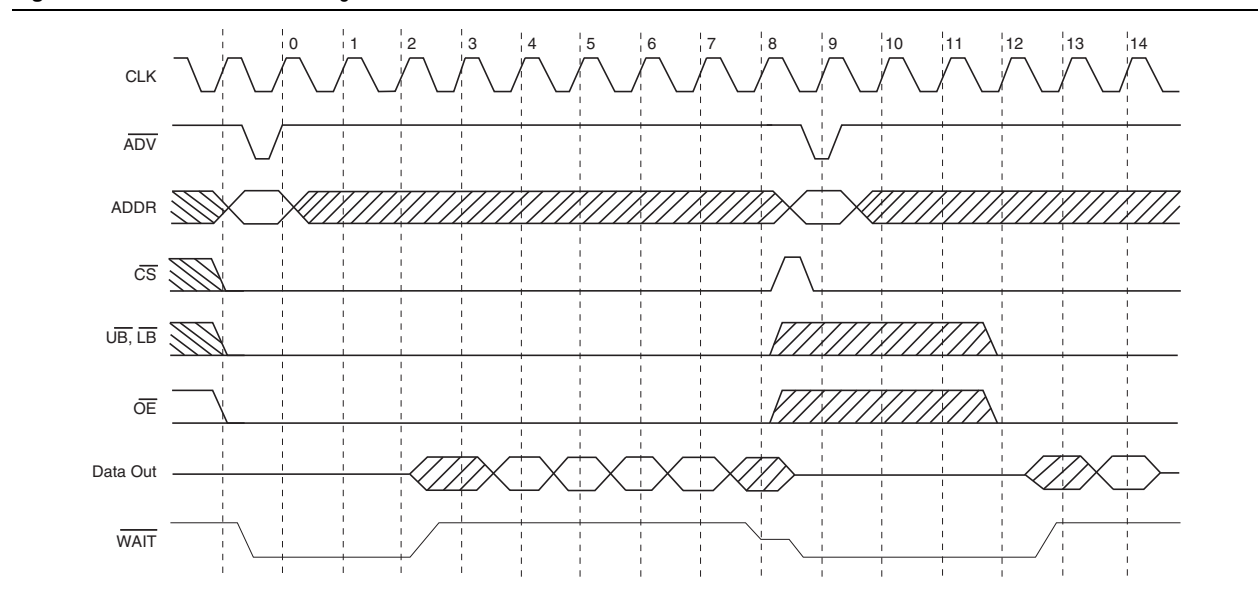
**Table 2-54.** SRAM Latency Vs. Frequency

| Item                           | Up to 66 MHz |          | Up to 80 MHz |          | Up to 104 MHz |          |
|--------------------------------|--------------|----------|--------------|----------|---------------|----------|
|                                | Fixed        | Variable | Fixed        | Variable | Fixed         | Variable |
| Latency set (A11:A10:A9)       | 4(0:0:1)     | 2(1:0:0) | 5(0:1:0)     | 3(0:0:0) | 7(1:0:1)      | 4(0:0:1) |
| Read latency (min)             | 4            | 2/4      | 5            | 3/5th    | 7             | 4/7      |
| First read data fetch clock    | 5th          | 3rd/5th  | 6th          | 4th/6th  | 8th           | 5th/8th  |
| Write latency (min)            | 2            | 2        | 3            | 3        | 4             | 4        |
| First write data loading clock | 3rd          | 3rd      | 3rd          | 4th      | 5th           | 5th      |



Figure 2-15 and Figure 2-16 show the Samsung device read and write access waveforms, respectively.

**Figure 2-15. SRAM Read Timing Waveforms**



**Figure 2-16. SRAM Write Timing Waveforms**

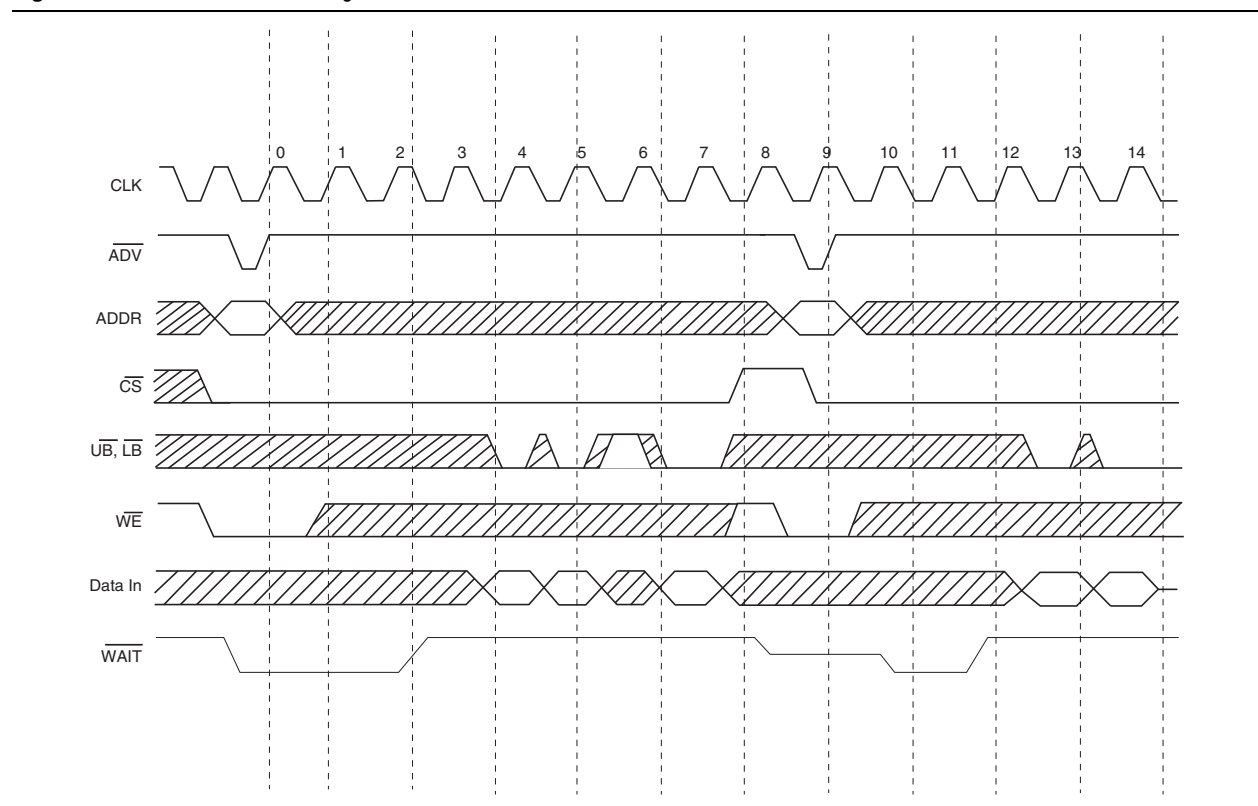


Table 2-55 lists the SRAM board reference and manufacturing information.

**Table 2-55.** SRAM Manufacturing Information

| Board Reference | Description              | Manufacturer          | Manufacturer Part Number | Manufacturer Website                                 |
|-----------------|--------------------------|-----------------------|--------------------------|--|
| U23, U24        | 32 MB (2 M × 16) of SRAM | Samsung Semiconductor | K1B3216B2E-BI70          | <a href="http://www.samsung.com">www.samsung.com</a> |



For more information about timing parameter values, mode register settings (MRS), or any other data regarding the Samsung device, visit [www.samsung.com](http://www.samsung.com).

## Flash Memory

The board features 64 MB of flash memory with a 16-bit data bus. The device uses 1.8-V CMOS signaling and is used for storing configuration files for the FPGA as well as any other files such as Nios software binaries, libraries, images, and sounds.

The interface uses a single Spansion device. The part number is S29GL512N11FFIV1. The device features CFI flash command support, byte- and word-mode operation, and 110 ns access times for a theoretical read bandwidth of 145 Mbps.

The flash device is part of a shared bus with connectivity to the MAX II CPLD as well as the SRAM memory, which is called the FSM bus. All three devices use 1.8-V CMOS signaling. Altera recommends using the 50-ΩOCT setting on the FPGA. The flash does not have a drive strength setting.

Table 2-56 shows the required signals for flash memory. Signal direction is relative to the FPGA.

**Table 2-56.** Flash Interface I/O (Part 1 of 2)

| Board Reference | Description                      | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|----------------------------------|--------------|-----------------------|-------------------------------|
| U31 pin F2      | Chip enable                      | 1.8 V        | FLASH_CEn             | Y16                           |
| U31 pin G2      | Output enable                    | 1.8 V        | FLASH_OEn             | Y17                           |
| U31 pin A4      | Ready/busy                       | 1.8 V        | FLASH_RDYBSYn         | AG25                          |
| U31 pin B5      | Reset                            | 1.8 V        | FLASH_RESEn           | AB20                          |
| U31 pin A5      | Write enable                     | 1.8 V        | FLASH_WEn             | AA21                          |
| U31 pin F7      | Word/byte                        | 1.8 V        | FLASH_BYTEn           | (1)                           |
| U31 pin E2      | Address bus bit 0 (word aligned) | 1.8 V        | FSA0                  | AC11                          |
| U31 pin D2      | Address bus bit 1 (word aligned) | 1.8 V        | FSA1                  | AH10                          |
| U31 pin C2      | Address bus bit 2 (word aligned) | 1.8 V        | FSA2                  | AA13                          |
| U31 pin A2      | Address bus bit 3 (word aligned) | 1.8 V        | FSA3                  | AC10                          |
| U31 pin B2      | Address bus bit 4 (word aligned) | 1.8 V        | FSA4                  | Y15                           |
| U31 pin D3      | Address bus bit 5 (word aligned) | 1.8 V        | FSA5                  | AF22                          |
| U31 pin C3      | Address bus bit 6 (word aligned) | 1.8 V        | FSA6                  | AF26                          |
| U31 pin A3      | Address bus bit 7 (word aligned) | 1.8 V        | FSA7                  | AF4                           |
| U31 pin B6      | Address bus bit 8 (word aligned) | 1.8 V        | FSA8                  | AD8                           |
| U31 pin A6      | Address bus bit 9 (word aligned) | 1.8 V        | FSA9                  | AG26                          |

**Table 2-56.** Flash Interface I/O (Part 2 of 2)

| Board Reference | Description                       | I/O Standard | Schematic Signal Name | Cyclone III Device Pin Number |
|-----------------|-----------------------------------|--------------|-----------------------|-------------------------------|
| U31 pin C6      | Address bus bit 10 (word aligned) | 1.8 V        | FSA10                 | AH6                           |
| U31 pin D6      | Address bus bit 11 (word aligned) | 1.8 V        | FSA11                 | AD24                          |
| U31 pin B7      | Address bus bit 12 (word aligned) | 1.8 V        | FSA12                 | AF9                           |
| U31 pin A7      | Address bus bit 13 (word aligned) | 1.8 V        | FSA13                 | AA8                           |
| U31 pin C7      | Address bus bit 14 (word aligned) | 1.8 V        | FSA14                 | AC22                          |
| U31 pin D7      | Address bus bit 15 (word aligned) | 1.8 V        | FSA15                 | AE8                           |
| U31 pin E7      | Address bus bit 16 (word aligned) | 1.8 V        | FSA16                 | AF13                          |
| U31 pin B3      | Address bus bit 17 (word aligned) | 1.8 V        | FSA17                 | AB14                          |
| U31 pin C4      | Address bus bit 18 (word aligned) | 1.8 V        | FSA18                 | AF23                          |
| U31 pin D5      | Address bus bit 19 (word aligned) | 1.8 V        | FSA19                 | AG12                          |
| U31 pin D4      | Address bus bit 20 (word aligned) | 1.8 V        | FSA20                 | AB18                          |
| U31 pin C5      | Address bus bit 21 (word aligned) | 1.8 V        | FSA21                 | Y19                           |
| U31 pin B8      | Address bus bit 22 (word aligned) | 1.8 V        | FSA22                 | AG3                           |
| U31 pin C8      | Address bus bit 23 (word aligned) | 1.8 V        | FSA23                 | AE16                          |
| U31 pin F8      | Address bus bit 24 (word aligned) | 1.8 V        | FSA24                 | AB7                           |
| U31 pin E3      | Data bit 0                        | 1.8 V        | FSD0                  | J14                           |
| U31 pin H3      | Data bit 1                        | 1.8 V        | FSD1                  | D6                            |
| U31 pin E4      | Data bit 2                        | 1.8 V        | FSD2                  | J17                           |
| U31 pin H4      | Data bit 3                        | 1.8 V        | FSD3                  | G7                            |
| U31 pin H5      | Data bit 4                        | 1.8 V        | FSD4                  | F18                           |
| U31 pin E5      | Data bit 5                        | 1.8 V        | FSD5                  | C6                            |
| U31 pin H6      | Data bit 6                        | 1.8 V        | FSD6                  | H17                           |
| U31 pin E6      | Data bit 7                        | 1.8 V        | FSD7                  | C18                           |
| U31 pin F3      | Data bit 8                        | 1.8 V        | FSD8                  | D18                           |
| U31 pin G3      | Data bit 9                        | 1.8 V        | FSD9                  | G16                           |
| U31 pin F4      | Data bit 10                       | 1.8 V        | FSD10                 | G22                           |
| U31 pin G4      | Data bit 11                       | 1.8 V        | FSD11                 | F12                           |
| U31 pin F5      | Data bit 12                       | 1.8 V        | FSD12                 | D11                           |
| U31 pin G6      | Data bit 13                       | 1.8 V        | FSD13                 | E24                           |
| U31 pin F6      | Data bit 14                       | 1.8 V        | FSD14                 | H21                           |
| U31 pin G7      | Data bit 15                       | 1.8 V        | FSD15                 | G9                            |

**Note to Table 2-56:**

- (1) For the corresponding Cyclone III device pin number, refer to the MAX II device pin-out information in [Table 2-5 on page 2-7](#).

Table 2–57 defines the flash memory map and lists the signals required for flash memory. Signal directions are relative to the Cyclone FPGA.

**Table 2–57.** Flash Memory Map Defined

| Signal Name   | Description                | I/O Standard                        |
|---|----------------------------|-------------------------------------|
| FSM_A (24:0)  | Address bus (word aligned) | 1.8-V LVCMOS out (25 bits)          |
| FSM_D (15:0)  | Data bus                   | N/A (Accounted for in SRAM section) |
| FLASH_CS <sub>n</sub>                                 | Chip select                | 1.8-V LVCMOS out                    |
| FLASH_OE <sub>n</sub>                                 | Output enable              | 1.8-V LVCMOS out                    |
| FLASH_WE <sub>n</sub>                                 | Write enable               | 1.8-V LVCMOS out                    |
| FLASH_RST <sub>n</sub>                                | Reset                      | 1.8-V LVCMOS out                    |
| FLASH_WP <sub>n</sub>                                 | Write protect              | N/A (Tie to VCC)                    |
| FLASH_RDYBSY <sub>n</sub>                             | Ready/not busy             | N/A (Tie to CPLD)                   |
| FLASH_BYTE <sub>n</sub>                               | Byte/word select           | N/A (Tie to CPLD)                   |
| VIO   | I/O power                  | 1.8 V                               |
| VCC   | Core power                 | 3.3 V                               |
| VSS   | Ground                     | Ground                              |
| Cyclone III device I/O totals: 29 1.8 V CMOS I/O pins |                            |                                     |

Table 2–58 shows the flash device memory map on the Cyclone III development board. The memory provides non-volatile storage for a minimum of eight FPGA bit streams, as well as various settings data used for on-board devices such as Ethernet TCP/IP defaults, PFL configuration bits, and data on the board itself. The remaining area is designated as user flash area for storage of software binaries and other data relevant to a user FPGA design.

**Table 2–58.** Flash Memory Map (Part 1 of 2)

| Name                 | Address                    |
|----------------------|----------------------------|
| PFL option bits      | 0x03FE.0080<br>0x03FE.0000 |
| Ethernet option bits | 0x03FD.FFEF<br>0x03FC.0000 |
| User space (32 MB)   | 0x03F9.FFFF<br>0x0200.0000 |
| Reserved             | 0x01FF.FFFF<br>0x01C0.0000 |
| FPGA design 7        | 0x01BE.EBE1<br>0x0188.0000 |
| FPGA design 6        | 0x0186.EBE1<br>0x0150.0000 |
| FPGA design 5        | 0x014E.EBE1<br>0x0118.0000 |
| FPGA design 4        | 0x0116.EBE1<br>0x00E0.0000 |

**Table 2-58.** Flash Memory Map (Part 2 of 2)

| Name                           | Address                    |
|--------------------------------|----------------------------|
| FPGA Design 3                  | 0x00DE.EBE1<br>0x00A8.0000 |
| FPGA Design 2                  | 0x00A6.EBE1<br>0x0070.0000 |
| FPGA Design 1                  | 0x006E.EBE1<br>0x0038.0000 |
| FPGA Design 0 (factory design) | 0x0036.EBE1<br>0x0000.0000 |



For information about the flash array command set and sequencing for register access, or any other data regarding the Spansion device, visit [www.spansion.com](http://www.spansion.com).

Table 2-59 and Table 2-60 are from the Spansion flash device data sheet. The tables show the top and bottom sections of the flash sector map, along with the manufacturer's sector address map.

**Table 2-59.** Flash Sector Map – Bottom

| Sector | A24-A16 |   |   |   |   |   |   |   |   | Sector Size<br>(KBytes)<br>Kwords | 8-Bit<br>Address Range<br>(In hexadecimal) | 16-bit<br>Address Range<br>(In hexadecimal) |
|--------|---------|---|---|---|---|---|---|---|---|-----------------------------------|--|---|
| SA0    | 0       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 128/64                            | 0000000-001FFFF                            | 0000000-000FFFF                             |
| SA1    | 0       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 128/64                            | 0020000-003FFFF                            | 0010000-001FFFF                             |
| SA2    | 0       | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 128/64                            | 0040000-005FFFF                            | 0020000-002FFFF                             |
| SA3    | 0       | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 128/64                            | 0060000-007FFFF                            | 0030000-003FFFF                             |
| SA4    | 0       | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 128/64                            | 0080000-009FFFF                            | 0040000-004FFFF                             |
| SA5    | 0       | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 128/64                            | 00A0000-00BFFFF                            | 0050000-005FFFF                             |

**Table 2-60.** Flash Sector Map – Top

| Sector | A24-A16 |   |   |   |   |   |   |   |   | Sector Size<br>(Kbytes)<br>Kwords | 8-Bit<br>Address Range<br>(In hexadecimal) | 16-bit<br>Address Range<br>(In hexadecimal) |
|--------|---------|---|---|---|---|---|---|---|---|-----------------------------------|--|---|
| SA508  | 1       | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 128/64                            | 3F80000-3F9FFFF                            | 1FC0000-1FCFFFF                             |
| SA509  | 1       | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 128/64                            | 3FA0000-3FBFFFF                            | 1FD0000-1FDFFFF                             |
| SA510  | 1       | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 128/64                            | 3FC0000-3FDFFFF                            | 1FE0000-1FEFFFF                             |
| SA511  | 1       | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128/64                            | 3FE0000-3FFFFFF                            | 1FF0000-1FFFFFF                             |

Table 2-61 lists Spansion flash board reference and manufacturing information.

**Table 2-61.** Spansion Flash Manufacturing Information

| Board Reference | Description           | Manufacturer | Manufacturer Part Number | Manufacturer Website                                   |
|-----------------|-----------------------|--------------|--------------------------|--|
| U31             | 64 MB of flash memory | Spansion LLC | S29GL512N11FFIV1         | <a href="http://www.spansion.com">www.spansion.com</a> |

## Power Supply

The board's power is provided through an IBM laptop style DC power input. The input voltage must be in the range of 14 V to 20 V. The DC voltage is then stepped down to the various power rails used by the components on the board and installed into the HSMC connectors.

Figure 2-17 shows the power distribution system, which uses current power rails as described in “POWER SELECT Rotary Switch” on page 2-21. Regulator inefficiencies and sharing are reflected in the currents shown.

[illegible]

## Power Measurement

Eight power supply rails have on-board voltage and current sense capabilities. These measurements are made using an 8-channel differential A/D converter from Linear Technology, with a serial data bus connected to the MAX II CPLD.

The MAX II CPLD contains a logic design that continually monitors the power rails and displays the current in mW on the dedicated four-digit 7-segment display. Rotary switch SW4 is used to select the power rail being displayed. The sense resistor is large enough that it can be easily probed by a user to confirm the display results. The results are also accessible from the FPGA through register access across the FSM bus.

Figure 2-18 illustrates the circuit.

**Figure 2-18.** Power Measurement Circuit

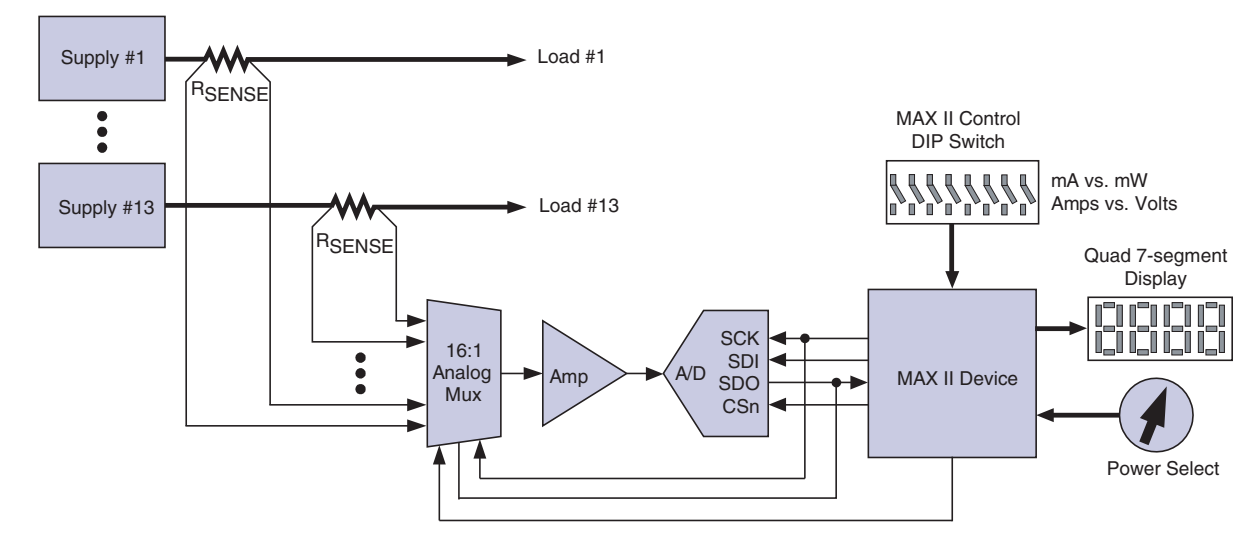


Table 2-16 on page 2-21 lists the power measurement rails. The *Schematic Signal Name* column lists the power rail being measured, and the power pins/devices attached to the power rail are listed in the *Power Pin Name* and *Description* columns.



## Statement of China-RoHS Compliance

Table 2-62 lists hazardous substances included with the kit.

**Table 2-62.** Table of Hazardous Substances' Name and Concentration *Notes (1), (2)* (Part 1 of 2)

| Part Name                     | Lead (Pb) | Cadmium (Cd) | Hexavalent Chromium (Cr6+) | Mercury (Hg) | Polybrominated biphenyls (PBB) | Polybrominated diphenyl Ethers (PBDE) |
|-------------------------------|-----------|--------------|----------------------------|--------------|--------------------------------|---------------------------------------|
| Cyclone III development board | X*        | 0            | 0                          | 0            | 0                              | 0                                     |
| 12-V power supply             | 0         | 0            | 0                          | 0            | 0                              | 0                                     |
| Type A-B USB cable            | 0         | 0            | 0                          | 0            | 0                              | 0                                     |



**Table 2-62.** Table of Hazardous Substances' Name and Concentration *Notes (1), (2)* (Part 2 of 2)

| Part Name  | Lead (Pb) | Cadmium (Cd) | Hexavalent Chromium (Cr6+) | Mercury (Hg) | Polybrominated biphenyls (PBB) | Polybrominated diphenyl Ethers (PBDE) |
|------------|-----------|--------------|----------------------------|--------------|--------------------------------|---------------------------------------|
| User guide | 0         | 0            | 0                          | 0            | 0                              | 0                                     |

**Notes to Table 2-62:**

- (1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.
- (2) X\* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.



## Revision History

The following table displays the revision history for this reference manual.

| Date         | Version | Changes Made   |
|--------------|---------|--|
| August 2008  | 1.2     | <ul style="list-style-type: none"> <li>■ Corrected “Schematic Signal Names” in <a href="#">Table 2–5</a> and added <a href="#">Note 1</a>.</li> <li>■ Updated JTAG settings in <a href="#">Table 2–7</a>.</li> <li>■ Updated <a href="#">Table 2–16</a>.</li> <li>■ Updated the power supply information of banks 1, 2, 5, and 6 in <a href="#">Figure 2–6</a>.</li> <li>■ Updated <a href="#">Note 1</a> in <a href="#">Table 2–39</a> and <a href="#">Note 1</a> in <a href="#">Table 2–39</a> to point to MAX II pin-out information.</li> <li>■ Updated “10/100/1000 Ethernet” section.</li> <li>■ Corrected unit in “Power Measurement” section.</li> <li>■ Converted document to new frame template and made textual and style changes.</li> </ul>   |
| March 2008   | 1.1     | <ul style="list-style-type: none"> <li>■ Added schematic information to, revised I/O standard terminology, and added data bit information to the HSMC Port A and Port B tables.</li> <li>■ Added schematic information to and revised I/O standard terminology to the DDR 2 interface I/O table.</li> <li>■ Added schematic information to and revised I/O standard terminology to the Ethernet PHY I/O table.</li> <li>■ Added schematic information to and revised I/O standard terminology to the flash memory I/O table.</li> <li>■ Added schematic information to and revised I/O standard terminology to the graphics LCD table.</li> <li>■ Added schematic information to and revised I/O standard terminology to the SRAM table.</li> <li>■ Updated power measurement table.</li> <li>■ Updated flash memory map table.</li> <li>■ Added flash memory map definition table.</li> </ul> |
| October 2007 | 1.0     | First publication  |

## How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

| Contact <small>Note 1</small>                           | Contact Method | Address  |
|---|----------------|--|
| Technical support                                       | Website        | <a href="http://www.altera.com/support">www.altera.com/support</a>       |
| Technical training                                      | Website        | <a href="http://www.altera.com/training">www.altera.com/training</a>     |
|   | Email          | <a href="mailto:custrain@altera.com">custrain@altera.com</a>             |
| Product literature                                      | Website        | <a href="http://www.altera.com/literature">www.altera.com/literature</a> |
| Non-technical support (General)<br>(Software Licensing) | Email          | <a href="mailto:nacomp@altera.com">nacomp@altera.com</a>                 |
|   | Email          | <a href="mailto:authorization@altera.com">authorization@altera.com</a>   |





**Note to Table:**

(1) You can also contact your local Altera sales office or sales representative.

## Typographic Conventions

This document uses the typographic conventions shown in the following table.

| Visual Cue                                      | Meaning  |
|---|--|
| <b>Bold Type with Initial Capital Letters</b>   | Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: <b>Save As</b> dialog box.   |
| <b>bold type</b>                                | External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: <b>f<sub>MAX</sub></b> , <b>\qdesigns</b> directory, <b>d:</b> drive, <b>chiptrip.gdf</b> file.   |
| <i>Italic Type with Initial Capital Letters</i> | Document titles are shown in italic type with initial capital letters. Example: <i>AN 75: High-Speed Board Design</i> .  |
| <i>Italic type</i>                              | Internal timing parameters and variables are shown in italic type. Examples: <i>t<sub>PIA</sub></i> , <i>n + 1</i> .<br>Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <file name>, <project name>.pdf.  |
| Initial Capital Letters                         | Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.   |
| "Subheading Title"                              | References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."   |
| Courier type                                    | Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input.<br>Active-low signals are denoted by suffix <i>n</i> , e.g., reset <i>n</i> .<br>Anything that must be typed exactly as it appears is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword SUBDESIGN), as well as logic function names (e.g., TRI) are shown in Courier. |
| 1., 2., 3., and a., b., c., etc.                | Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.   |
| ■ ● •   | Bullets are used in a list of items when the sequence of the items is not important.   |
| ✓   | The checkmark indicates a procedure that consists of one step only.  |
| ☞   | The hand points to information that requires special attention.  |

| <b>Visual Cue</b>   | <b>Meaning</b>   |
|---|--|
|  | The caution calls attention to a condition that could damage the product or design and should be read prior to starting or continuing with the procedure or process. |
|  | The warning calls attention to a condition that could cause injury to the user and should be read prior to starting or continuing the procedure or processes.        |
|  | The angled arrow indicates you should press the Enter key.   |
|  | The feet direct you to more information on a particular topic.   |

