Spartan®-3A FPGA Family DDR2 MIG Back-to-Back Bursts Wrapper

Reference Design on Spartan-3A/AN FPGA Starter Kits with ISE® 11.2 Software

Cliff Tsai
Xilinx

June 25, 2009

Limitations

- **Limited Warranty and Disclaimer.** These designs are provided to you “as is”. Xilinx and its licensors make and you receive no warranties or conditions, express, implied, statutory or otherwise, and Xilinx specifically disclaims any implied warranties of merchantability, non-infringement, or fitness for a particular purpose. Xilinx does not warrant that the functions contained in these designs will meet your requirements, or that the operation of these designs will be uninterrupted or error free, or that defects in the Designs will be corrected. Furthermore, Xilinx does not warrant or make any representations regarding use or the results of the use of the designs in terms of correctness, accuracy, reliability, or otherwise.

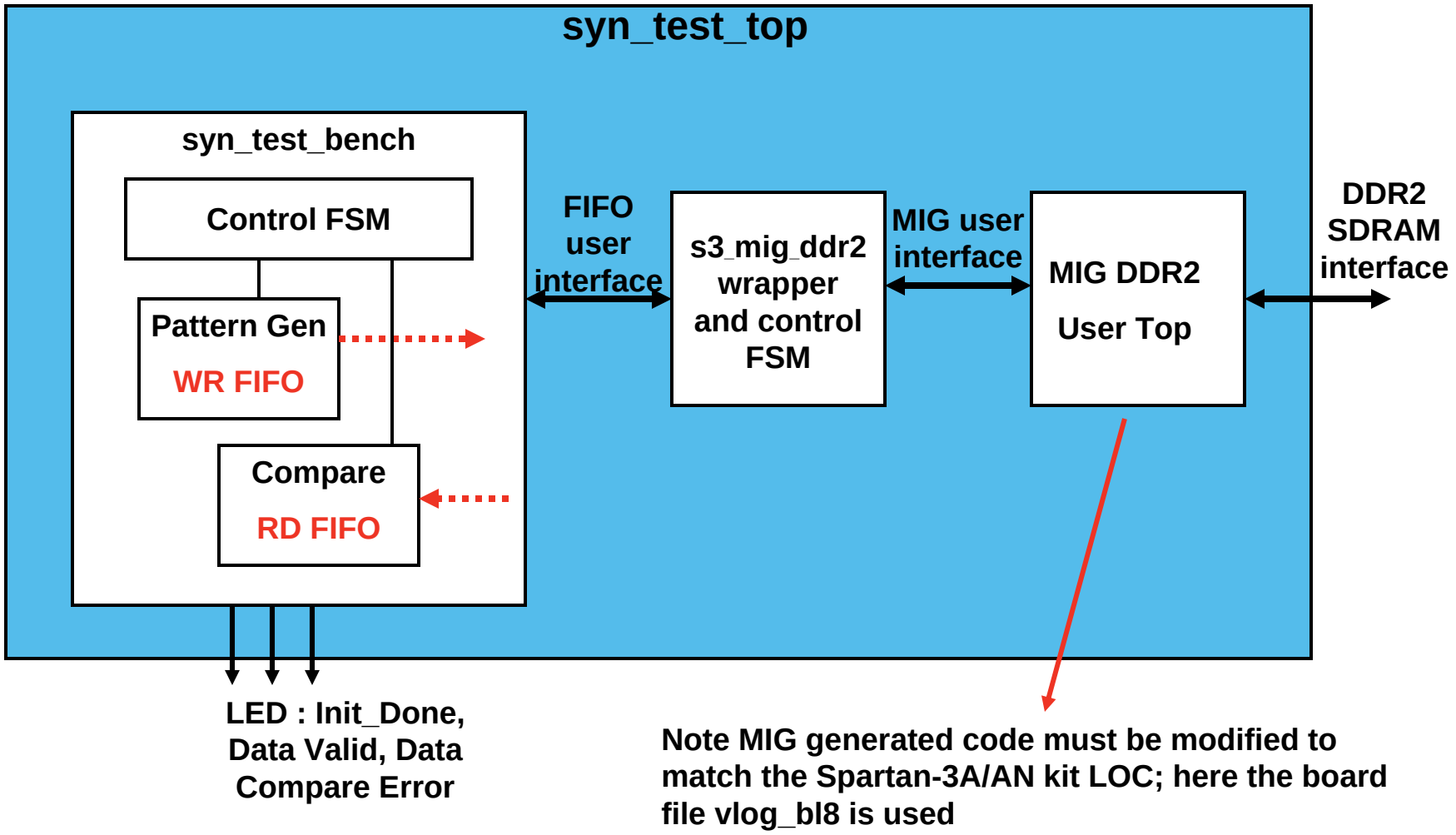
- **Limitation of Liability.** In no event will Xilinx or its licensors be liable for any loss of data, lost profits, cost or procurement of substitute goods or services, or for any special, incidental, consequential, or indirect damages arising from the use or operation of the designs or accompanying documentation, however caused and on any theory of liability. This limitation will apply even if Xilinx has been advised of the possibility of such damage. This limitation shall apply notwithstanding the failure of the essential purpose of any limited remedies herein.

- This design modules is **not** supported by Xilinx Technical support as an official Xilinx Product.

Features

- **A wrapper on top of the Memory Interface Generator (MIG) tool within the Core Generator (CoreGen) tool hiding the details of the original interface, initialization sequence and AREF requests handling**
- **Single User Clock Domain**
- **Easy FIFO-like user interface**
- **Automatically pausing when AREF requests occur (about every 7.8μs) during R/W bursts and continuing R/W once AREF is done**
- **Back-to-back bursts for performance improvement with different Burst Length**
  - Note the max number of back-to-back bursts is limited by column address and user R/W FIFO depth
- **Suitable for applications such as Video Line buffer access**

Reference Design Architecture



Reference Design RTL Hierarchy

- **sim_tb_top.v (simulation top instantiates syn_test_top and Micron DDR2 model)**
  - ***syn_test_top.v*** : Top module instantiates syn_test_bench, s3_mig_ddr2_wrapper and mig usr top
    - ***syn_test_bench.v*** : synthesizable test bench instantiates WR/RD FIFO and ctrl fsm to generate Write data and Read data comparison
    - ***s3_mig_ddr2_wrapper.v*** : wrapper for MIG and provides simple clock domain FIFO interface
    - ***s3_mig_wrapper_define.v*** : defines file control burst length and synthesizable test bench consecutive back-to-back burst number
    - ***mig_top_no_tb.v*** : used as top of vlog_bl8 for Spartan-3A/AN Kit LOC
  - Default *test_seed/bit_shift_seed* definition in *s*3_mig_wrapper_define.v
  - The Write Data Test Pattern is from ***1,2,3,4,5,6…….. To N-1***, so the RD Data comparison must match the Write Data Sequence

Reference Design Size and Timing (ISE 11)

- **The synthesizable testbench instantiates two 18KB Block RAM configured as one 511x32 Write FIFO and one 511x32 Read FIFO (FWFT mode),** total Block RAM usage is 5 include MIG control
  - So the max number of back-to-back bursts is int[511/8]
  - Check ***consecutive_burst*** in s3_mig_wrapper_define.v

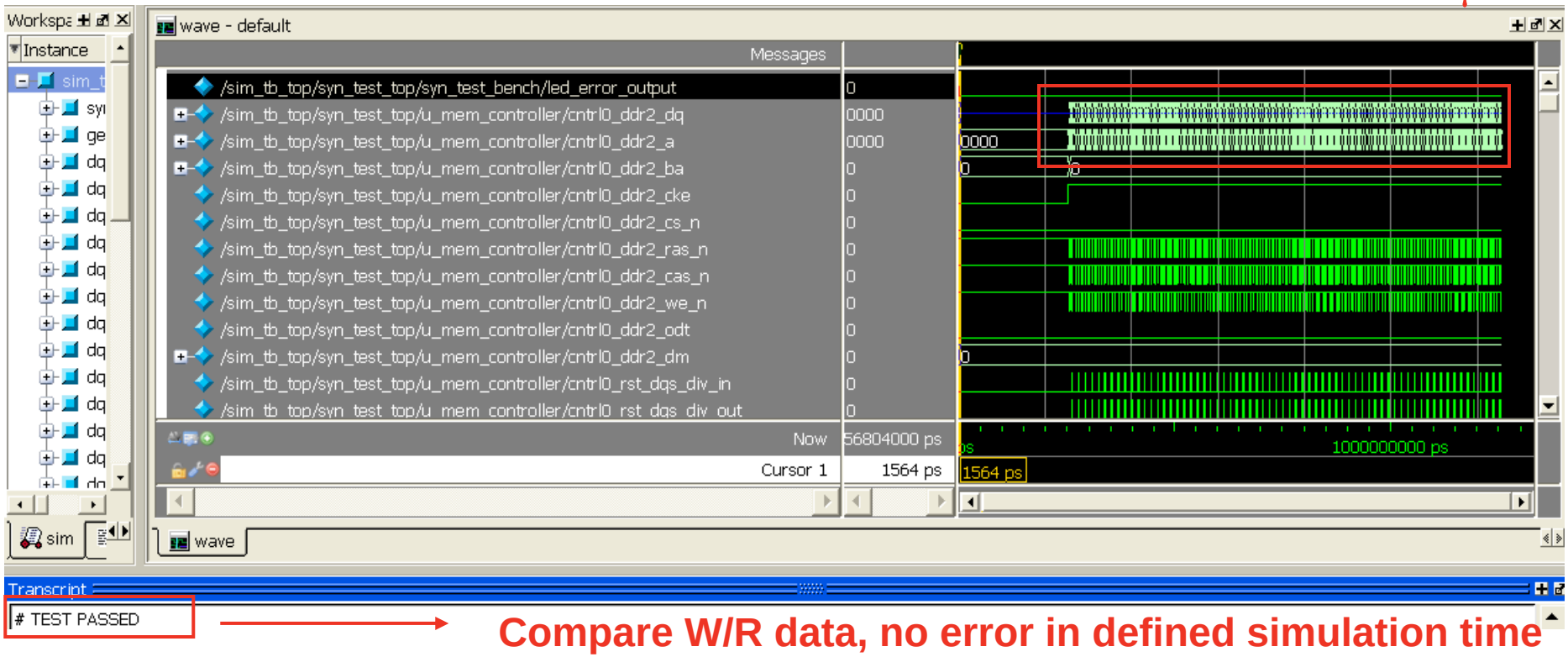
xc3s700a-4fg484	Device Utilization Summary		
Logic Utilization	**Used**	**Available**	**Utilization**
Total Number Slice Registers	1,421	11,776	12%
Number used as Flip Flops	1,420		
Number used as Latches	1		
Number of 4 input LUTs	1,262	11,776	10%
Number of occupied Slices	1,223	5,888	20%
Number of Slices containing only related logic	1,223	1,223	100%
Number of Slices containing unrelated logic	0	1,223	0%

  - The reference design runs at more than 133 MHz with -4 device, but was tested with a 133 MHz clk input on the Spartan-3A/AN kit

Simulation

- Double-click the ModelSim script file .\sim\sim.bat or type vsim –do sim.do under a console window
- Optionally change the simulation time in the sim.do

Bursts Write and Read in 1000µs



Compare W/R data, no error in defined simulation time

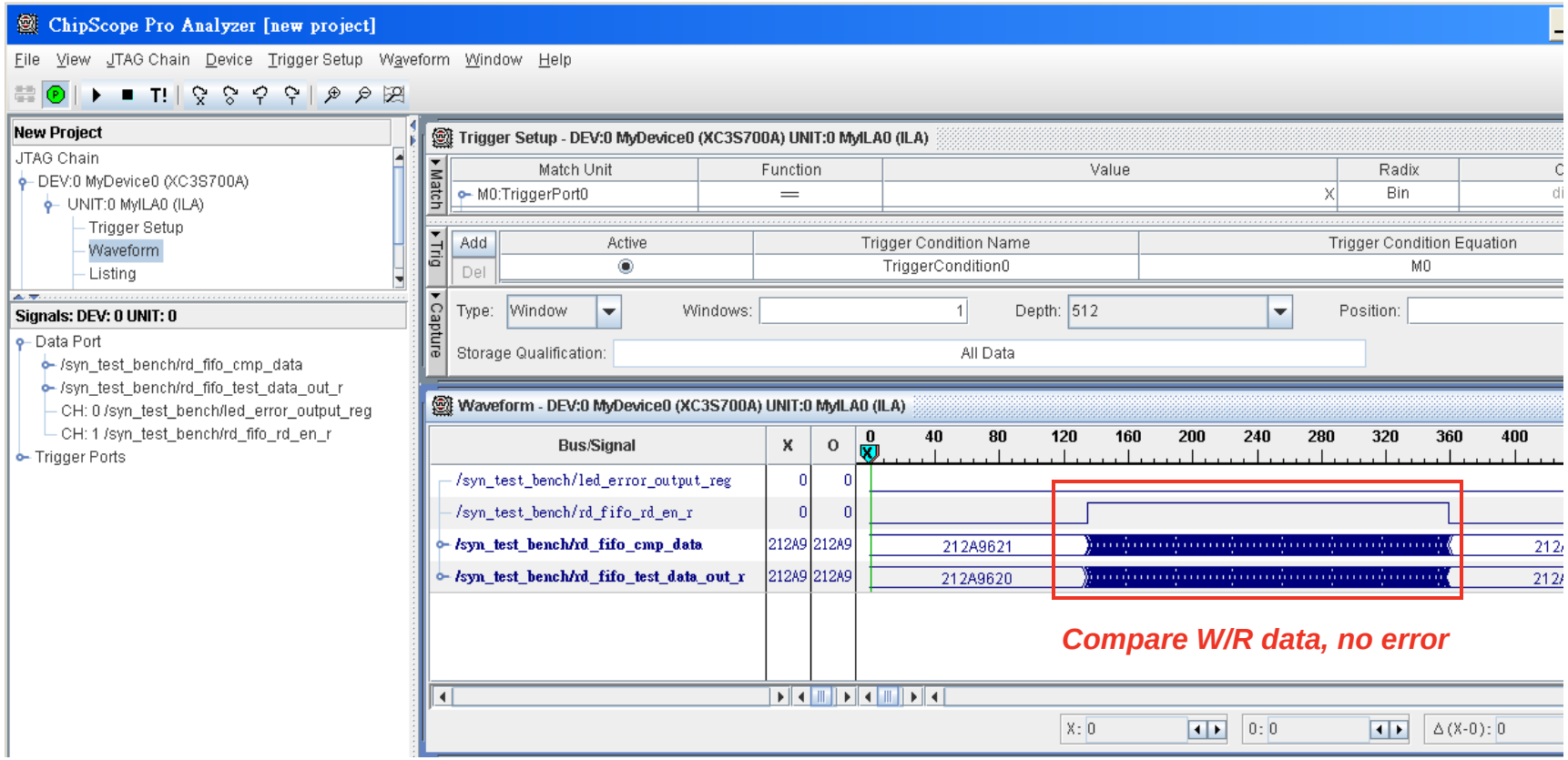
XILINX

Configuration of Spartan-3A/AN Starter Kit

- **Clocking**
  - 133 MHz Clock on IC14 socket for GCLK2 (V12)
- **DDR2 Performance Correction**
  - Xilinx has identified two component changes which improve the performance of the DDR2 SDRAM device
  - If you are using the DDR2 SDRAM device and experience sub-optimal performance, short out components FB4 and FB5
  - These are both located near the index pin on the DDR2 SDRAM
- **Output**
  - LD2 (On means : Init_done)
  - LD1 (On means : data valid)
  - LD0 (Off means : No data W/R comparison error)

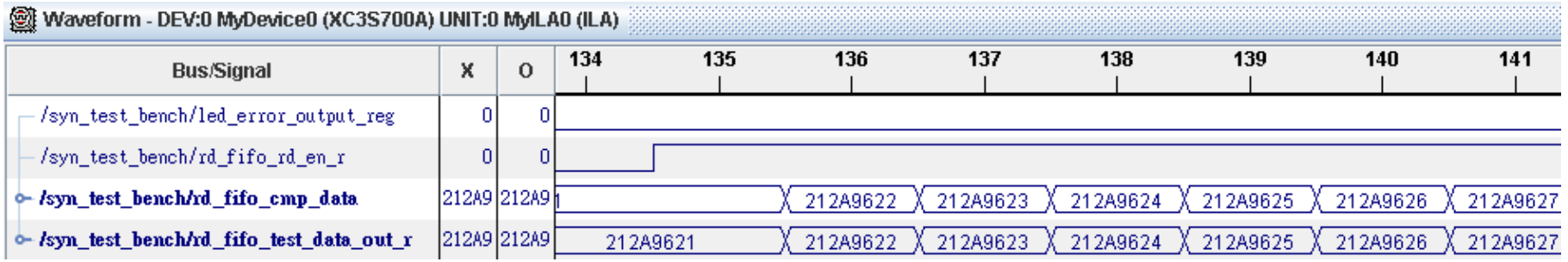
Implementation and ChipScope™ Pro Verification on Spartan-3A/AN Starter Kit

- Double-click *Analyze Design Using ChipScope Pro* under ISE GUI
- Use ChipScope Pro Analyzer 11 to configure FPGA and load ila_debug.cdc allowing the automatic Trigger/Data signal annotation

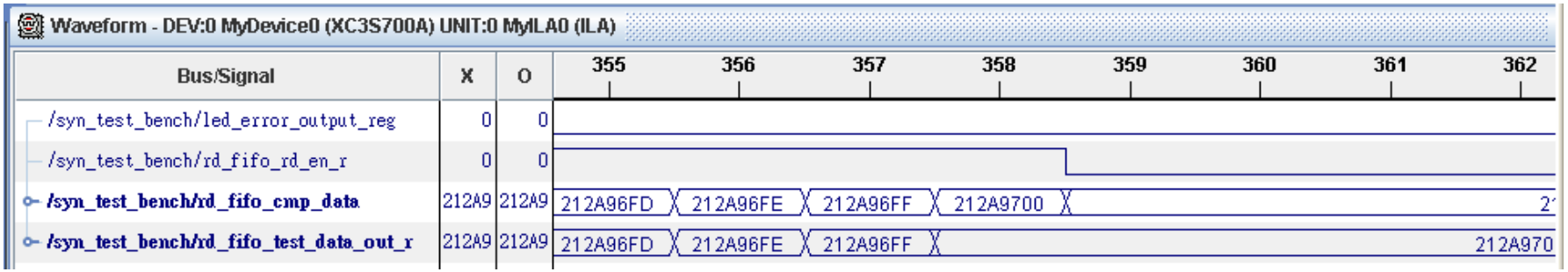


Enlarge the ChipScope Pro Waveform Window

- RD FIFO receives DDR2 Read data, and starts to output and perform comparison



- Last piece of RD Burst Data comparison



XILINX