# Spartan-3A LVDS Demonstration

A Reference Design for Spartan™-3A Starter kit

**Rev 1: June 2007**

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# LVDS Demonstration

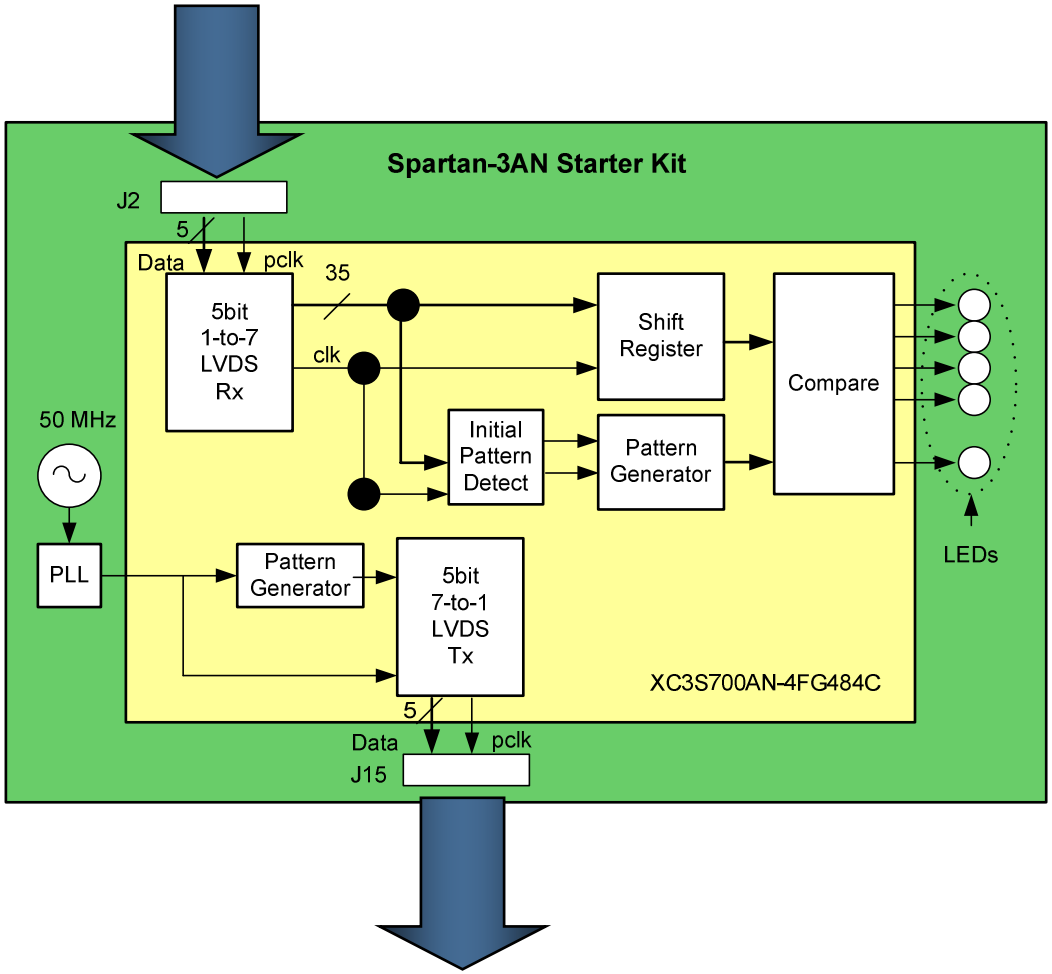
This demo shows how the Spartan-3A starter kit uses the ChipScope™ debugger to help check the high speed LVDS performance using low cost connectors (J2, J15).

While the design does NOT show the maximum achievable performance, the designer will get a very good idea of the performance and can see how to better understand the DCM operation and debugging without using extensive oscilloscope setups.

**Highlighted features**

- XAPP485 – LVDS Receiver that deserializes LVDS for FPD applications
- XAPP486 – LVDS Transmitter that serializes LVDS for FPD applications
- DCM
  - Clock synchronization is always critical in any high speed design. Even at the 600 Mbps data rates used by displays, balancing the routing delays within the device becomes an important factor. For the LVDS design the DCM is used to both synchronize incoming data as well as create the multiplied clock rates required for displays.
  - Additional features of the DCM are used to better understand the skew and approximate data eye size.
- ChipScope – Debugging high speed data
- VIO – Used to control demo using ChipScope

# LVDS Design Block Diagram




One of five different data patterns are generated by the Pattern Generator block. The data is then serialized using the 7-to-1 LVDS Tx block (XAPP486) and sent over a low cost twisted pair cable (not included).

The data is received and de-serialized using the LVDS deserializer (XAPP485). An equivalent pattern generator is then synchronized to the incoming data to check to ensure the data has been received correctly.

The number of pattern errors are tracked by flags within the design so that the design can determine which channel is failing. To see what data is transmitted and received the designer can use the supplied ChipScope project.

The parallel 100 ohm termination resistors that are required for LVDS receivers use the on-chip termination, DIFF_TERM.

# LVDS For Displays

- The design is set up to match commonly found display devices using LVDS. Further modifications may be easily made in the design files as discussed in XAPP485/486.

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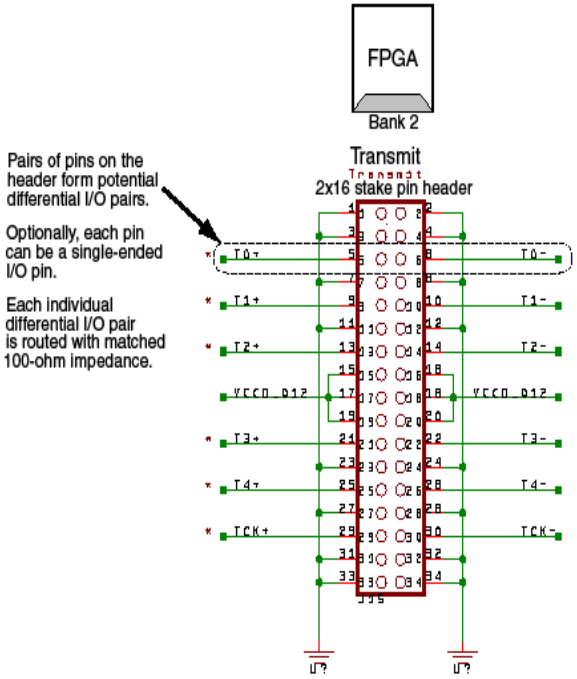
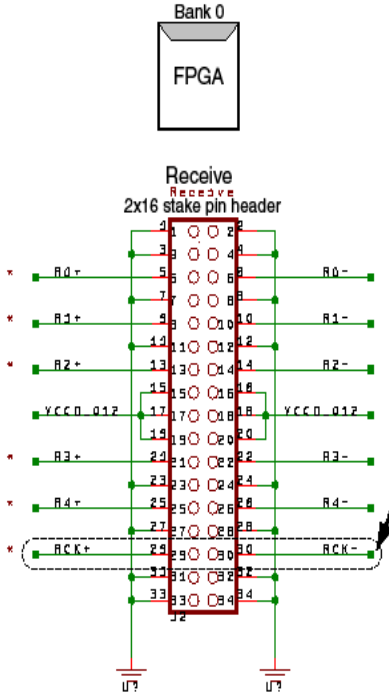
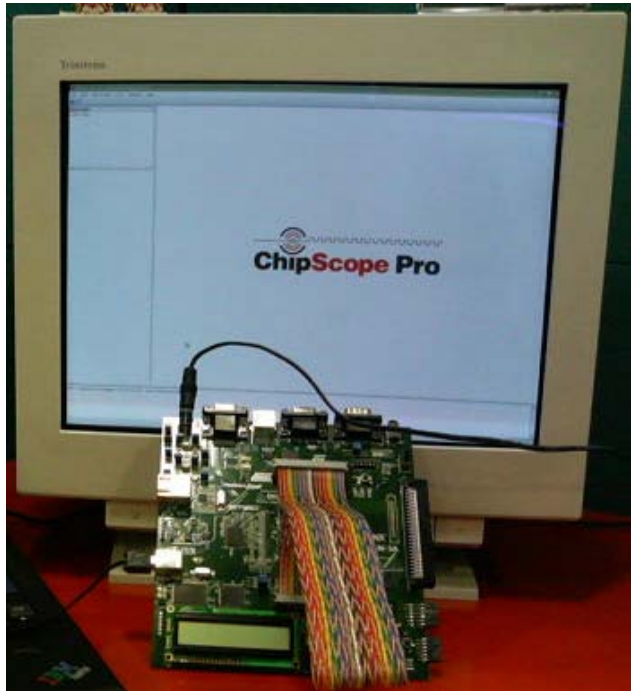


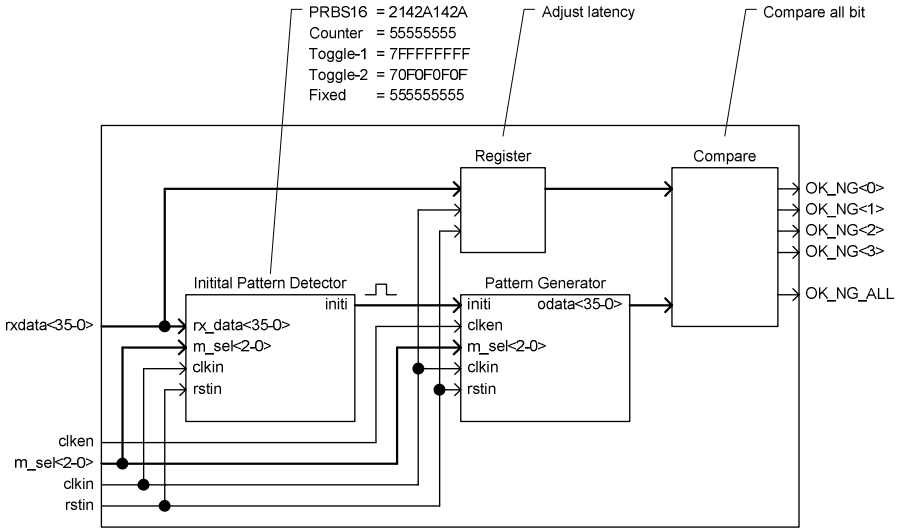

The receive clock differential pair feeds the GCLK6 and GCLK7 global clock inputs, which in turn connect to the top, right DCM labeled DCM_X2Y3

If using differential inputs, set the DIFF_TERM=TRUE constraint.
There are no external termination resistors provided on the board.

```
INST <I/O_BUFFER_INSTANTIATION_NAME> DIFF_TERM = "TRUE" ;
```

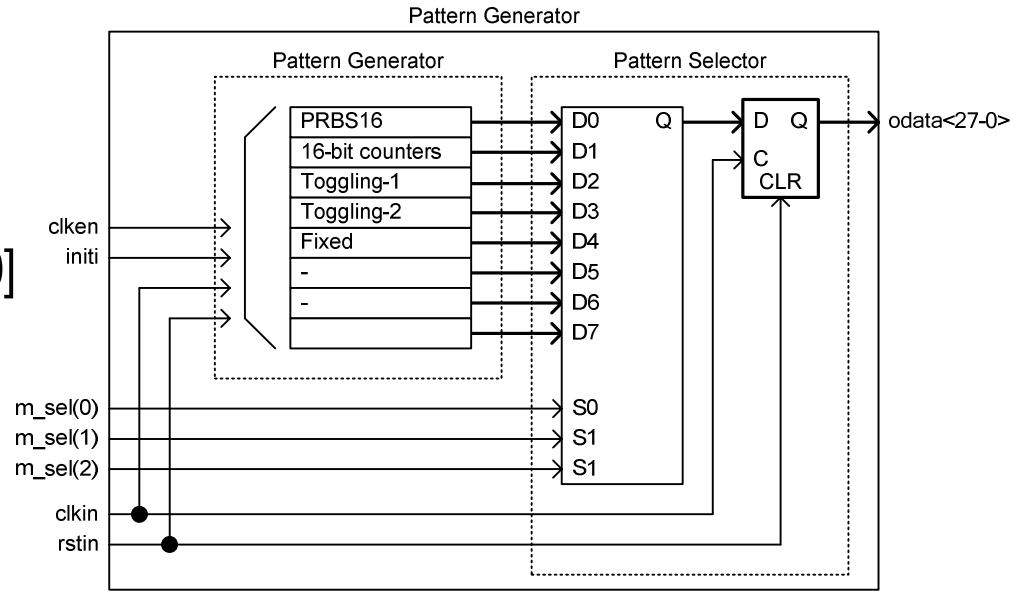
# Pattern Generator Controls

- The pattern generator has been set up to send one of several different patterns
- The VIO interface within the Chipscope Pro Analyzer allows the user to select the data pattern
- Initialization values are used to synchronize the receive and transmit pattern generators
- To fully stress the system, random noise (PRBS16) is best used to send both short and long pulses. Additionally toggle patterns and counters are useful during debugging and for helping determine how the errors occur.



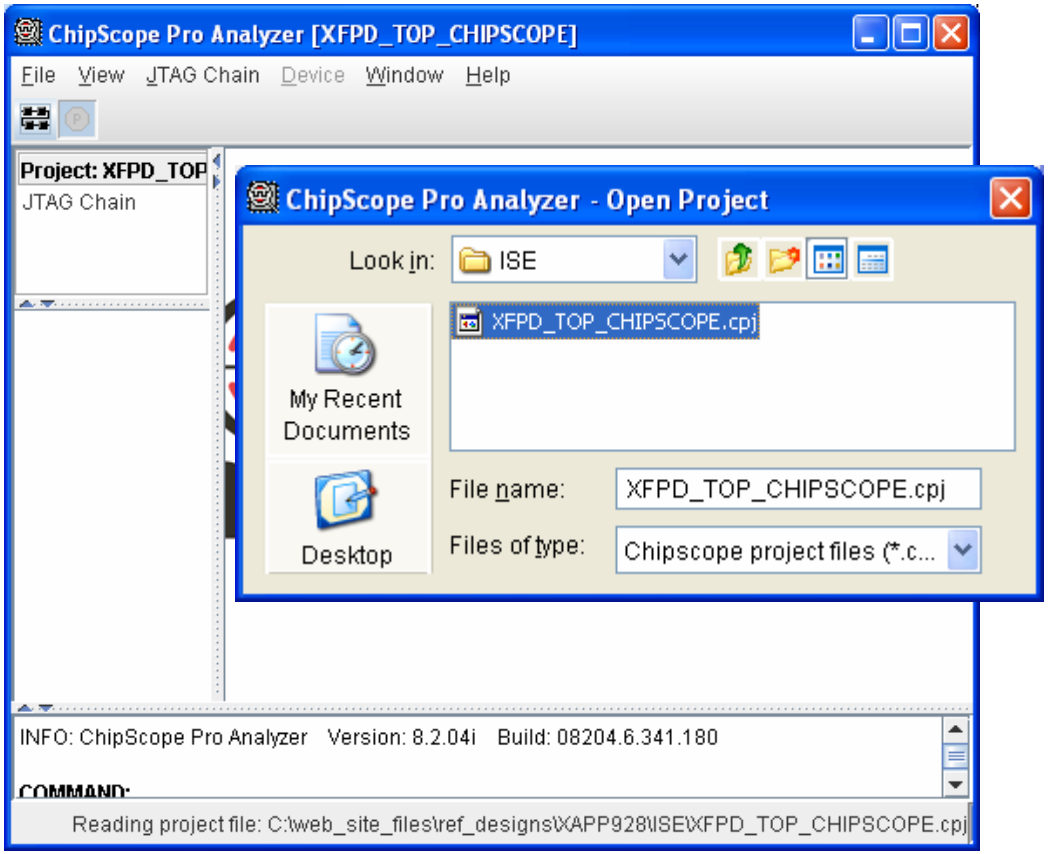
# Test Pattern

- PRBS16 – Eye diagram
- 16 bit counters
  - 35 bits by concatenating
  - Cnt[2:0] & Cnt[15:0] & Cnt[15:0]
- Toggling 1 –
  - ! 35'h7FFFFFFF
- Toggling 2
  - ! 35'h0F0F0F0F0
- Fixed
  - 35`h555555555



# LVDS Demo Setup

4) Using the provided files the device can now be:
   1) Configured with JTAG
   2) Programmed into Platform Flash
   3) Programmed into the SPI Flash
5) Power up the board and open ChipScope
6) Open the ChipScope project
7) Using the icon, open the JTAG cable



# Using ChipScope Pro

ChipScope™ Pro can insert logic analyzers, bus analyzers, and Virtual I/O software cores allowing the designer to view any internal signals. Captured signals can then be analyzed with ChipScope Pro Logic Analyzer.

- Control by VIO (Real time)

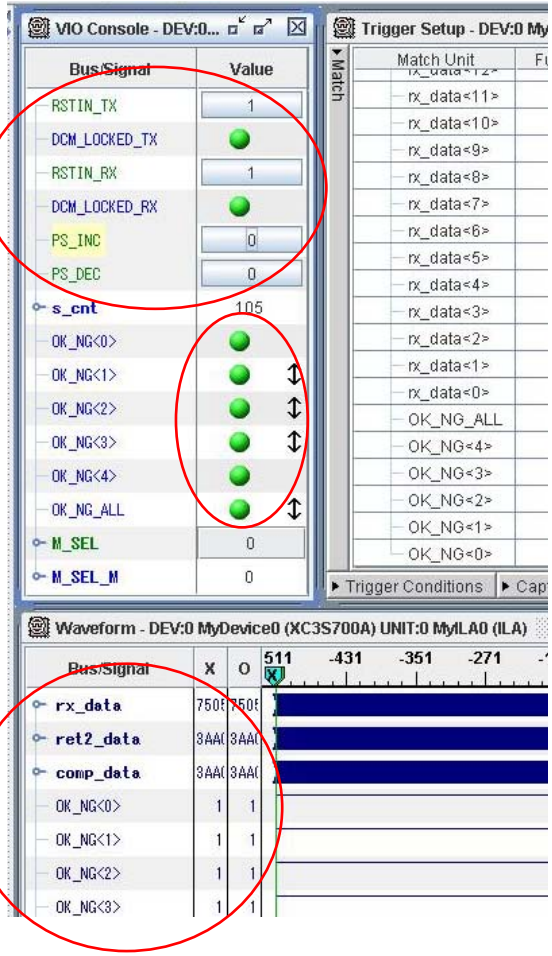
Asynchronous reset (Async_RST)
Phase shift control of DCM (ps_inc/ps_dec)
Select test mode of pattern generator (m_sel)

- Capture by VIO (Real time)

LOCKED signal of DCM (int_dcm_locked_rx)
Phase shift amount of DCM of receiver side (s_cnt)
Compare received data (OK_NG)

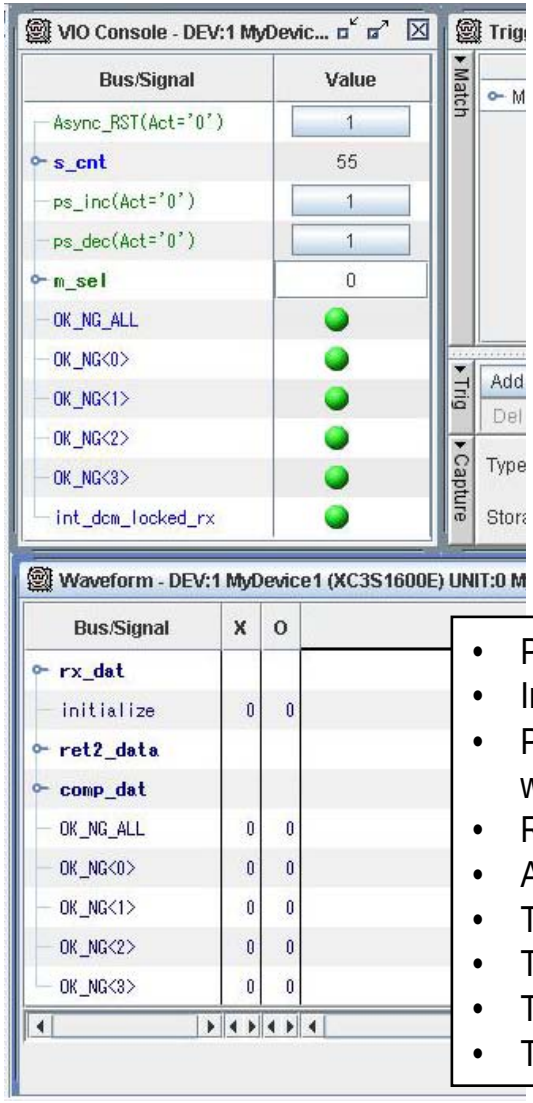
- Capture by ILA (Triggered)

35 bit data on the receiver side
Initialize pulse from the Initial Pattern Detector
35 bit data from the Pattern Generator on the receiver side
Compare results



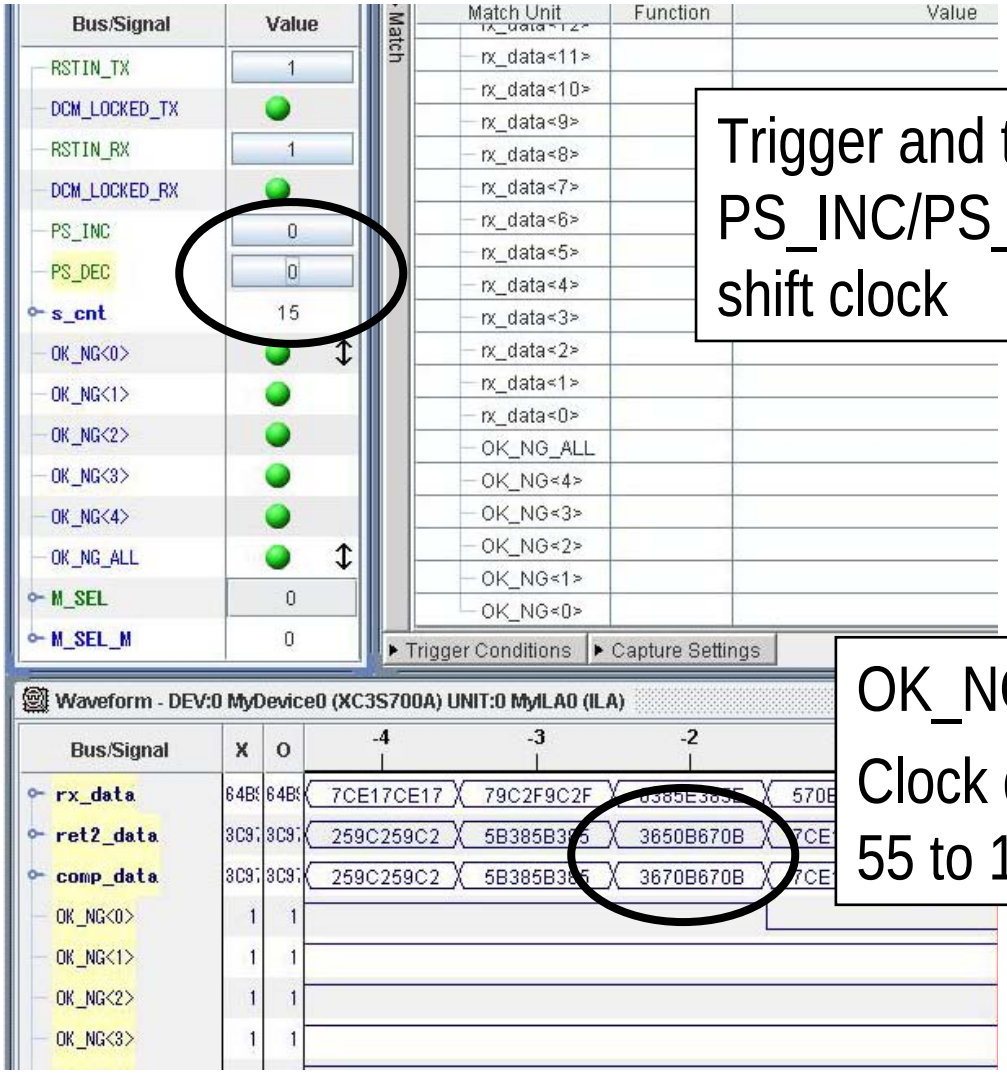
# ChipScope Pro Description

- Async reset for all circuit
- Phase Shift Value of DCM
- Phase Shift Value Increment Button
- Phase Shift Value Decrement Button
- Test Pattern Select Window
- All Signal Receive Correctly = Green
- Txdata(0) Receive Correctly = Green
- Txdata(1) Receive Correctly = Green
- Txdata(2) Receive Correctly = Green
- Txdata(3) Receive Correctly = Green
- LOCKED signal of DCM




- Parallel data at top4_rx
- Initialize pulse at the pattern detector
- Parallel data after re-timing for compare with the re-generate data
- Re-generate data by initialize pulse
- ALL Signal Receive Correctly = '1'
- Txdata(0) Receive Correctly = '1'
- Txdata(1) Receive Correctly = '1'
- Txdata(2) Receive Correctly = '1'
- Txdata(3) Receive Correctly = '1'

# Using ChipScope Pro




Trigger and then use PS_INC/PS_DEC to shift clock

OK_NG<0> - Error on channel 0

Clock decremented 40 taps from 55 to 15 ≈ 1.0 ns