MicroBlaze Spartan-3A Kit Reference Design

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Software Tools Requirements

- EDK 9.1.02
- ISE 9.1.03

Hardware Requirements

- Xilinx Spartan-3A Starter Kit board Rev. C or Rev. D
- USB Cable (provided with the Kit)
- Serial cable
- Ethernet cross-over cable

Contents

Two EDK projects using the same hardware build.

- system.xmp: memory test and system tests applications. A bootloader is provided for the system tests application to boot from NOR Flash.
- webserver.xmp: web server application based on XAPP433. A bootloader is provided for the web server application to boot from NOR Flash. Instructions to dual boot from the system tests application to the web server application are provided.

Files and Directories:

- system.mhs: hardware system definition used by Xilinx Platform Studio
- system.mss: software settings for the system tests application
- webserver.mss: software settings for the web server application
- bootloader_systest: bootloader application for the system tests application
- bootloader_web: bootloader application for the web server application
- data\system.ucf: constraint file for the FPGA
- etc: FPGA implementation and download options
- pcores: custom peripherals directory
- System_Tests: system tests application
- TestApp_Memory: memory tests application
- WebPage: web page contents
- WebServer: web server application

Embedded Processor System

The Embedded processor system is the same for all applications. Some software applications might not use certain peripherals.

The SOUTH push button is used for an external reset input.

DCMs are used to generate the clocks needed for the system. The 50 MHz external oscillator is the external clock input.

Refer to the Spartan-3A Starter Kit Board User Guide for information on components and features. Xilinx Platform Studio (XPS) is used to implement the hardware and software.

The table below shows the embedded system specifics.

	Version	Address Map	Type	Speed	Description
MicroBlaze	6.00.b	NA	Processor	66.67 MHz	4KB I-Cache, 4KB D-Cache
I/D LMB Ctrl	2.00.a	0x00000000 0x00003FFF	Memory		16KB of Internal Memory
DDR2 SDRAM Ctrl	1.02.a	0x24000000 0x27FFFFFF	EDK MCH OPB DDR2	133 MHz	DDR2 memory, 32MB x 16
Flash Ctrl	2.00.a	0x30000000 0x303FFFFF	EDK OPB EMC		NOR Flash, 2MB x 16 Can store multiple HW and SW images
RS232 DCE	1.00.b	0x40000000 0x4000FFFF	EDK OPB UartLite	9600 Bauds	UART using DCE port
LEDs 8-bit	3.01.b	0x40010000 0x4001FFFF	EDK OPB GPIO		LEDs LED0 through LED7
DIP Switches 4-bit	3.01.b	0x40020000 0x4002FFFF	EDK OPB GPIO		Switches SW0 through SW3
Buttons 3-bit	3.01.b	0x40040000 0x4004FFFF	EDK OPB GPIO		Push Buttons North, East, and West
Ethernet MAC	1.04.a	0x40080000 0x4008FFFF	EDK OPB Ethernet	10/100 Mbps	Ethernet MAC, FIFO mode, no DMA
Rotary switch	1.00.b	0x40400000 0x4040FFFF	Custom Peripheral		Rotary switch control
Timer	1.00.b	0x40100000 0x4010FFFF	EDK OPB Timer		Timer/Counter peripheral
Interrupt Controller	1.00.c	0x40200000 0x4020FFFF	EDK OPB INTC		3 inputs: UART, Timer, and Ethernet
Character LCD Ctrl	1.00.c	0x40800000 0x4080FFFF	Custom Peripheral		Character LCD using 4-bit mode
S3A ICAP Ctrl	1.00.a	0x41000000 0x4100FFFF	Custom Peripheral		Internal Configuration Access Port Ctrl Used for multi-boot operations
Debug Module	2.00.a	0x41400000 0x4140FFFF	EDK OPB MDM		Connects to MicroBlaze for JTAG debug
System reset	1.00.a	NA	EDK PROC SYS RST		Reset block for MicroBlaze and busses

Software Applications

TestApp_Memory
Simple DDR2 memory test included in the system.xmp and webserver.xmp projects. The application is located in the FPGA internal memory.

System_Tests
Included in the system.xmp project. The application tests the Ethernet MAC, Interrupt controller, LEDs, Rotary switch, and Character LCD. The code can be stored in Flash or downloaded through JTAG and is executed from DDR2 memory.

bootloader_systest
Included in the system.xmp project. The application copies an SREC formatted System_Tests application from Flash to DDR2. Follow the instructions below to store applications to Flash. The bootloader is located in the FPGA internal memory.

WebServer
Included in the webserver.xmp project. Refer to XAPP433 for details on the application. A new thread was added to control the character LCD with the Rotary switch. The code can be stored in Flash or downloaded through JTAG and is executed from DDR2 memory.

bootloader_web
Included in the webserver.xmp project. The application copies an SREC formatted WebServer application as well as the web page Memory File System from Flash to DDR2. Follow the instructions below to store applications to Flash. The bootloader is located in the FPGA internal memory.

Running the Memory Test

1. Open the system.xmp file using XPS
2. The Implementation is done by XPS
    a. Go to Hardware > Generate Bitstream to generate a bit file
3. Compile the code
    a. Go to Software > Build All User Applications
4. Place the Memory Test in internal memory
    a. Right-click on TestApp_Memory and select Mark to Initialize BRAMs
    b. Make sure that no other application is selected for BRAM initialization
5. Configure the FPGA
    a. Connect the USB cable
    b. Connect the serial cable
    c. Power on the S3A Starter Kit
    d. Open HyperTerminal at 9600,8,1, no parity
    e. Go to Device Configuration > Download Bitstream
6. The application will output the result of the DDR2 memory test to the serial terminal

Running the System Tests

Run the memory test above first. Continuing from Step 6

1. Open XMD
    a. Go to Debug > Launch XMD…
2. Type: cd system_tests
3. Type: rst
4. Download the application to DDR2
    a. In the XMD window type: dow executable.elf
5. Run the application
    a. In the XMD window type: run
    b. Close XMD by typing: exit
6. The application will output the result of the tests to the serial terminal and LCD. Rotating the rotary switch will change the LED outputs. Pushing on the rotary switch will exit the application

Running the WebServer application

For more information on the web server read XAPP433. The steps below are identical to the ones in XAPP433 except for step 5 on page 8. The address to download the MFS image is 0x25000000 instead of 0x2c000000

1. Open the webserver.xmp file using XPS
2. Clean the libraries
    a. Go to Software > Clean Libraries

3. Compile the code
    a. Go to Software > Build All User Applications
4. Place the bootloop program in internal memory
    a. Right-click on Default: microblaze_0_bootloop and select Mark to Initialize BRAMs
    b. Make sure that no other application is selected for BRAM initialization
5. Configure the FPGA
    a. Go to Device Configuration > Download Bitstream
6. Create the Memory File System image
    a. Go to Project > Launch EDK Shell
    b. Type: cd WebPage
    c. Type:

mfsgen –cvbfs ../WebServer/image.mfs 600 404.html index.html logoV2005.gif xapp433.pdf

    d. Close the shell
7. Connect a cross-over Ethernet cable
8. Configure the Host PC Ethernet settings following the instructions in XAPP433.pdf
9. Download the WebServer application to memory
    a. Open XMD
    b. Type: rst
    c. Type: dow -data WebServer/image.mfs 0x25000000
    d. Type: dow WebServer/executable.elf
    e. Type: con
    f. Type: exit
10. In the serial terminal, configure the Ethernet address for the target following the instructions from XAPP433
11. The rotary switch will update the first line of the LCD. Pushing on the switch will update Line 2 with the contents of Line 1
12. Open a web browser
    a. Type: http:/x.x.x.x:80 (use the IP address configured above in step 10)
    b. Follow the instructions on the web page

Storing the FPGA configurations and software images in Flash

These steps are optional.

It is recommended to set the board configuration mode to JTAG while doing the steps below.

Download the MicroBlaze BPI Flash Programmer design on the S3A Starter Kit reference design page.

The S3A Starter Kit includes a 32Mb NOR Flash which can be used to configure the FPGA and store software images and data files. Multiple configurations and images can be stored simultaneously. In this reference design, the System Tests application can start a reconfiguration of the FPGA with the WebServer application.

Refer to the Spartan-3 Generation Configuration User Guide to learn about MultiBoot and Master BPI Mode Configuration.

Below is the address map of the Flash contents used for this reference design (as viewed from MicroBlaze). A 3S700A configuration file takes up 6 blocks of Flash memory. The System_Tests application takes 2 blocks, the WebServer application 7 blocks, and the image.mfs 5 blocks.

The Flash could store more configurations and software images in the unused space.

First FPGA Configuration bootloader_systests in internal memory	0x30000000 0x3005FFFF
System_Tests Application SREC Format	0x30060000 0x3007FFFF
Second FPGA Configuration Bootloader_web in internal memory	0x30080000 0x300DFFFF
WebServer Application SREC Format	0x300E0000 0x30140000
WebPage Memory File System	0x30150000 0x3019FFFF
Unused	0x301A0000 0x303FFFFF

The Master BPI configuration mode uses the Flash in 8-bit mode while the embedded processor system uses the Flash in 16-bit mode. Using the Flash Programmer with the current XPS projects would cause configuration bytes to be swapped. An XPS project with the Flash configured for 8-bit mode has to be used to program the Flash with the FPGA configuration images.

Preparing the FPGA configuration files

The first FPGA configuration will contain the FPGA bit file as well as the System_Tests bootloader. The second FPGA configuration will contain the same FPGA bit file but with the WebServer bootloader.

1. Open the S3A Kit Reference Design system.xmp file using XPS
2. Clean the libraries
    a. Go to Software > Clean Libraries
3. Compile the code
    a. Go to Software > Build All User Applications
4. Place the bootloader_systests program in internal memory
    a. Right-click on bootloader_systests and select Mark to Initialize BRAMs
    b. Make sure that no other application is selected for BRAM initialization
5. Update the FPGA configuration file with the bootloader code
    a. Go to Device Configuration > Update Bitstream
6. Open iMPACT (Xilinx ISE 9.1i > Accessories)
    a. Double-click on "PROM File Formatter". Click Next
    b. Select “Xilinx PROM”, "BIN" file format, “systest_boot” as name and select the location directory for the generated files. Click Next
    c. Select "Auto Select PROM". Click Next. Click Finish. Click OK
    d. Select the download.bit file in the S3A Kit Reference Design *implementation* directory
    e. Select "No" when asked to add another device file. Click OK
    f. Double-click on "Generate File..."
    g. The “systest_boot.bin” file is a binary version of the FPGA bit file
7. Open the webserver.xmp file using XPS
8. Clean the libraries
    a. Go to Software > Clean Libraries
9. Compile the code
    a. Go to Software > Build All User Applications

10. Place the bootloader_web program in internal memory
    a. Right-click on bootloader_web and select Mark to Initialize BRAMs
    b. Make sure that no other application is selected for BRAM initialization
11. Update the FPGA configuration file with the bootloader code
    a. Go to Device Configuration > Update Bitstream
12. Open iMPACT (Xilinx ISE 9.1i > Accessories)
    a. Double-click on "PROM File Formatter". Click Next
    b. Select “Xilinx PROM”, "BIN" file format, “web_boot” as name and select the location directory for the generated files. Click Next
    c. Select "Auto Select PROM". Click Next. Click Finish. Click OK
    d. Select the download.bit file in the S3A Kit Reference Design *implementation* directory
    e. Select "No" when asked to add another device file. Click OK
    f. Double-click on "Generate File..."
    g. The “web_boot.bin” file is a binary version of the FPGA bit file
13. The FPGA configuration files, system_boot.bin and web_boot.bin are ready to be programmed into Flash.

Programming the FPGA configuration files into Flash

These steps require the use of the MicroBlaze BPI Flash Programmer design previously downloaded.

We will program the first image with no offset. The second image will be programmed at Flash offset 0x800000.

1. Open the BPI Flash Programmer system.xmp file with XPS
2. The system contains
    a. MicroBlaze v6 running at 50MHz
    b. LMB BRAM (32KB)
    c. OPB EMC Controller for BPI Flash (4MB)
    d. Hardware Debug Module
3. The Implementation is done by XPS
    a. Go to Hardware > Generate Bitstream to generate a bit file
4. Configure the FPGA
    a. Power on the S3A Starter Kit. Connect the USB cable
    b. Go to Device Configuration > Download Bitstream
5. Go to Device Configuration > Program Flash Memory
6. Select the "system_boot.bin" file generated by iMPACT. Click OK
7. Look at the XPS Console Window to verify that the Flash programming completed successfully
8. Go to Device Configuration > Program Flash Memory
9. Select the "web_boot.bin" file generated by iMPACT. Select an offset of 0x00800000. Click OK
10. Look at the XPS Console Window to verify that the Flash programming completed successfully
11. Close the XPS project

Programming the Software Images into Flash

The System_Tests and WebServer executables will be converted to SREC format before being programmed into Flash. The web page Memory File System will be programmed as is.

The System_Tests application will be modified to enable MultiBoot.

1. Open the S3A Kit Reference Design system.xmp file using XPS
2. Clean the libraries

    a. Go to Software > Clean Libraries
3. Modify the System_Tests code to enable MultiBoot
    a. Expand the Sources for the System_Tests application
    b. Double-click on system_tests.c
    c. At the end of the file uncomment:

XIo_Out32(XPAR_OPB_S3A_ICAP_0_BASEADDR, 0x00080000);

    d. This will start a reconfiguration starting at Flash address 0x800000 where the second FPGA configuration is located.
4. Compile the code
    a. Go to Software > Build All User Applications
5. Place the Default: microblaze_0_bootloop program in internal memory
    a. Right-click on Default: microblaze_0_bootloop and select Mark to Initialize BRAMs
    b. Make sure that no other application is selected for BRAM initialization
6. Configure the FPGA
    a. Go to Device Configuration > Download Bitstream
7. Program the System_Tests application into Flash at offset 0x60000
    a. Go to Device Configuration > Program Flash Memory
    b. Select the “executable.elf” file from the System_Tests directory
    c. Check the box “Auto-convert file to bootloadable SREC format when programming Flash”
    d. Select an offset of 0x00060000
    e. Click OK
    f. Look at the XPS Console Window to verify that the Flash programming completed successfully
8. Close the system.xmp project
9. Open the S3A Kit Reference Design webserver.xmp file using XPS
10. Clean the libraries
    a. Go to Software > Clean Libraries
11. Compile the code
    a. Go to Software > Build All User Applications
12. Place the Default: microblaze_0_bootloop program in internal memory
    a. Right-click on Default: microblaze_0_bootloop and select Mark to Initialize BRAMs
    b. Make sure that no other application is selected for BRAM initialization
13. Program the WebServer application into Flash at offset 0xE0000
    a. Go to Device Configuration > Program Flash Memory
    b. Select the “executable.elf” file from the WebServer directory
    c. Check the box “Auto-convert file to bootloadable SREC format when programming Flash”
    d. Select an offset of 0x000E0000
    e. Click OK
    f. Look at the XPS Console Window to verify that the Flash programming completed successfully
14. Program the image.mfs Memory File System into Flash at offset 0x150000
    a. Go to Device Configuration > Program Flash Memory
    b. Select the “image.mfs” file from the WebServer directory
    c. Select an offset of 0x00150000

d. Click OK

e. Look at the XPS Console Window to verify that the Flash programming completed successfully

15. Close XPS
16. Power off the S3A Starter Kit board

Running from Flash

The FPGA configuration files and software images are now programmed into Flash.

Change the board configuration mode to BPI Up.

Connect the serial cable (9600) and Ethernet cable.

After powering up the board the sequence of events will be:

1. The FPGA will be configured with the MicroBlaze system
2. The internal bootloader will load the System_Tests application from Flash to DDR2
3. The System_Tests application will execute from DDR2
4. Pressing the rotary switch button at the end of the tests will trigger a reconfiguration with the FPGA image stored at address 0x800000
5. The internal bootloader for the new configuration will load the image.mfs and WebServer application from Flash to DDR2
6. The WebServer application will execute from DDR2
7. Follow the earlier directions about running the WebServer application