Spartan-3A Starter Kit and Spartan-3AN Starter Kit Verification

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Author: Eric Crabill, Xilinx, Inc.

This document describes the verification tests and related procedures to perform an initial verification of the Spartan™-3A FPGA Starter Kit and the Spartan-3AN FPGA Starter Kit. These kits are identical with the exception of the particular FPGA device mounted on the PCB. Some tests described here are also intended to serve as production manufacturing tests. These tests may also be used by customers to assess the functionality of a potentially damaged board, which has particular value in an academic/educational environment.

For initial verification, and whenever power supply issues are suspected, it is prudent to complete test sections 1.0 and 2.0 before other tests. This reduces the possibility of damage in the event of an assembly or power supply problem.

IMPORTANT NOTE: Many of the non-volatile memory tests alter the contents of the device under test. As a result, data loss will occur. For example, if these tests are run on an "out-of-the-box" starter kit (pre-programmed with demo designs) the demo designs will no longer operate. To restore the starter kit to its original "out-of-the-box" state, please download the golden MCS files from the reference design page and follow the provided instructions.

Several tests require custom loopback hardware that is not provided with the starter kit. You must provide (build) your own loopback hardware. For more information, consult the design source to understand the expected loopback connectivity.

1.0 Visual Check

1.1 Inspect PCB assembly and component orientation.

1.1.1 Required: Schematic, Silkscreen Plots.

1.1.2 Set-Up: None.

1.1.3 Execution: Use the schematic as a guide, visually confirm that all components are present on the assembled PCB. There should be no extra components and no missing components. Visually inspect the orientation of all active components to ensure index pins are in the correct location. Does the board have appropriate rubber feet?

1.1.4 Expected Results: Record any gross assembly errors.

1.2 Inspect PCB top and bottom silkscreen for accuracy of all text and logos.

1.2.1 Required: Schematic, Silkscreen Plots.

1.2.2 Set-Up: None.

1.2.3 Execution: Use the schematic and top silkscreen plot as a guide, perform the following checks:

Footprints clearly identify index pins by some means.
Components are unambiguously associated with refdes.
No stray / floating refdes exist.
Annotated LOC values for each peripheral are correct.
No stray / floating annotated LOC values exist.
Note peripherals with no annotated LOC values.
Complex jumpers clearly identify jumper function and options.
Inclusion of all logos and logo placements.
Existence of area to record board serial number.

1.2.4 Expected Results: Record errors, omissions, and unexpected items.

1.3 Check for proper connector keep out, “plug check”.

1.3.1 Required: Mechanical cable samples to mate with each connector that exists: coaxial power, USB, coaxial SMA, Digilent FX2, Agilent soft-touch, Digilent SixPin, IDC34, PS/2, VGA, Stereo Audio, Serial DCE, Serial DTE, Ethernet.

1.3.2 Set-Up: None.

1.3.3 Execution: Plug everything in, check for physical conflicts. Visually inspect to determine if any headers and jumpers are blocked by connectors or cables.

1.3.4 Expected Results: Everything should fit; headers and jumpers should not be obscured. Note any physical conflicts between connectors, components, jumpers, or headers.

2.0 Pre-Power Check

2.1 Verify / set default jumper and switch positions.

2.1.1 Required: Spare jumper shorting blocks.

2.1.2 Set-Up: Remove pre-installed jumper shorting blocks from the board.

2.1.3 Execution: Set the following defaults:

J26, FPGA configuration mode, to JTAG.
SW5, power supply, to OFF.
SW4, FPGA operation mode, to RUN.
No other jumpers should be installed.
Other switch positions are “don’t care”.

2.1.4 Expected Results: None.

2.2 Power switch, indicator, and raw supply.

2.2.1 Required: Multi-meter.

2.2.2 Set-Up: Plug the power supply into the board power jack.

2.2.3 Execution: Measure the raw power supply at J14 using a multi-meter. Check for indication of voltage by inspecting the power indicator LD8. Set SW5 to ON. Repeat the check of LD8.

2.2.4 Expected Results: The raw power supply is expected to have a nominal value of 5.0 volts and present regardless of SW5 position. Switch SW5 should exhibit control over voltage regulation in a way that matches the silkscreen legend for SW5 and LD8.

2.3 Measure all eight isolated supplies.

2.3.1 Required: Multi-meter, 1.0 kohm load resistors.

2.3.2 Set-Up: The buck supply outputs may require the addition of a load resistor. This is not required for linear supply outputs.

2.3.3 Execution: With the power supplies enabled, measure outputs:

J9-1, VCCINT (nominally 1.2 volts, buck)
J10-1, VCCO_012 (nominally 3.3 volts, buck)
J11-1, VCCAUX (nominally 3.3 volts, linear)
J12-1, USB1V8 (nominally 1.8 volts, linear)
J40-1, DDR0V9 (nominally 0.9 volts, buck)
J13-1, DDR1V8 (nominally 1.8 volts, buck)
J41-1, DAC-REF_CD (nominally 3.3 volts, linear)
J42-1, VREF0V9 (nominally 0.9 volts, linear)

2.3.4 Expected Results: Each supply measurement should match the expected nominal value.

2.4 Measure all eight loaded supplies.

2.4.1 Required: Multi-meter, spare jumper shorting blocks.

2.4.2 Set-Up: Install jumpers on J9, J10, J11, J12, J40, J13, J41, and J42.

2.4.3 Execution: With the power supplies enabled, measure outputs:

J9-1, VCCINT (nominally 1.2 volts, buck)
J10-1, VCCO_012 (nominally 3.3 volts, buck)
J11-1, VCCAUX (nominally 3.3 volts, linear)
J12-1, USB1V8 (nominally 1.8 volts, linear)
J40-1, DDR0V9 (nominally 0.9 volts, buck)
J13-1, DDR1V8 (nominally 1.8 volts, buck)
J41-1, DAC-REF_CD (nominally 3.3 volts, linear)
J42-1, VREF0V9 (nominally 0.9 volts, linear)

2.4.4 Expected Results: Each supply measurement should match the expected nominal value.

2.5 Verify PWR/GND on jumpers, posts, and connectors.

2.5.1 Required: Multi-meter, Schematic.

2.5.2 Set-Up: None.

2.5.3 Execution: With power enabled, verify power by voltage measurement. With power physically removed, verify ground by impedance measurement. Verify the following pins:

GND: J17-A46, J17-A48, J17-B1, J17-B2, J17-B5 through J17-B45, J17-B47, J17-B50, J21-5, J22-5, J18-5, J19-5, J20-5, J34-A3, J34-A6, J34-A9, J34-A12, J34-B1, J34-B4, J34-B7, J34-B10, J34-B13, J4-1, J4-2, J5-1, J5-2, J6-1, J6-2, J46-3, J16-2, J25-5, J26-1 (pulldown), J26-3 (pulldown), J26-5 (pulldown), J38-5, J38-6, J38-7, J38-8, J38-10, J36-5, J27-5, J39-shield, J23-5, J28-3, J1-1, J1-2, J1-3, J1-4, J1-7, J1-8, J1-11, J1-12, J1-23, J1-24, J1-27, J1-28, J1-31, J1-32, J1-33, J1-34, J2-1, J2-2, J2-3, J2-4, J2-7, J2-8, J2-11, J2-12, J2-23, J2-24, J2-27, J2-28, J2-31, J2-32, J2-33, J2-34
VCC5V0: J17-A49, J17-A50, J17-B49, J28-5
VCCO_012: J17-A1, J17-A2, J21-6, J22-6, J22-1, J18-6, J19-6, J20-6, J25-6, J46-2 (pullup), J26-2 (pullup), J26-4 (pullup), J26-6 (pullup), J23-6, J1-15, J1-16, J1-17, J1-18, J1-19, J1-20, J2-15, J2-16, J2-17, J2-18, J2-19, J2-20
DAC-REF_CD: J22-2

2.5.4 Expected Results: Every post should be connected as indicated.

2.6 Static burn-in test to verify sustained operation.

2.6.1 Required: Nothing.

2.6.2 Set-Up: None.

2.6.3 Execution: Apply power, enable the power supplies, and let the board sit idle for an hour. Monitor the board during this time by touching component packages to identify devices which become exceptionally hot. This test may optionally be repeated using a programmed FPGA.

2.6.4 Expected Results: No smoke.

3.0 Configuration Check

3.1 Integrated USB download, verify JTAG scan integrity.

3.1.1 Required: Standard USB cable and Xilinx iMPACT.

3.1.2 Set-Up: With board power disabled, connect the board to the PC using the USB cable.

3.1.3 Execution: Turn on the board. During this test, the system may prompt you to allow a firmware update of the programming hardware. Accept any such update request. Launch iMPACT, start a new project for JTAG configuration via the USB programming hardware. Put all devices into BYPASS and run "Chain Integrity Test" from the Debug menu. Exit iMPACT, remove the USB cable, and re-insert it without cycling power. Launch iMPACT, start a new project for JTAG configuration via the USB programming hardware. Put all devices into BYPASS and run "Chain Integrity Test" from the Debug menu. Repeat this entire test, but swap the order of initial power application and initial cable attachment.

3.1.4 Expected Results: The results are the same for both test permutations. The PC should identify the USB programming hardware and install any required drivers. If a firmware update is performed, it should complete successfully. Once the USB device is enumerated by the system LD9, the Cable Ready status LED, should illuminate. iMPACT should identify the cable and enumerate the JTAG chain – containing the FPGA and PROM device(s). The "Chain Integrity Test" should pass.

3.1.5 Contingency Plan: If the integrated USB download is non-functional, attempt using external JTAG access with a programming cable.

3.2 Integrated USB download, verify FPGA direct programming.

3.2.1 Required: Standard USB cable and Xilinx iMPACT. At least one functional peripheral on board.

3.2.2 Set-Up: Connect the board to the PC using the USB cable. Place the FPGA into JTAG configuration mode by setting J26 correctly. Turn on the board.

3.2.3 Execution: Launch iMPACT, start a new project for JTAG configuration via the USB programming hardware. Assign the "boardtest" programming file to the FPGA and put all other devices in BYPASS. Program the device with verify enabled and check for evidence of configuration. Press the PROG pushbutton. The evidence of configuration should vanish. Repeat the test without cycling power.

3.2.4 Expected Results: The DONE indicator should initially be off. At the end of the programming step, the verify should pass and the DONE indicator should be on. At this point, and the device should show some evidence of configuration. After pressing the PROG pushbutton, the evidence of configuration should vanish and the DONE indicator should turn off. The second programming attempt should yield the same results as the first.

3.2.5 Contingency Plan: If the integrated USB download is non-functional, attempt using external JTAG access with a programming cable.

3.3 Integrated USB download, verify PROM direct programming.

3.3.1 Required: Standard USB cable and Xilinx iMPACT. MCS programming file for "boardtest" design with CCLK startup.

3.3.2 Set-Up: Connect the board to the PC using the USB cable. Place the FPGA into JTAG configuration mode by setting J26. Disable the PROM by removing all jumpers from J46. Turn on the board.

3.3.3 Execution: Launch iMPACT, start a new project for JTAG configuration via the USB programming hardware. Assign the "boardtest" programming file to the PROM and put all other devices in BYPASS. Program the device with verify enabled. Repeat this test with other settings of J46 (short 1-2, or short 2-3). It may be advisable to repeat the above 3 test scenarios, but with J26 set to master serial so that CCLK is running during PROM programming.

3.3.4 Expected Results: In all cases, iMPACT should indicate the device is successfully programmed.

3.3.5 Contingency Plan: If the integrated USB download is non-functional, attempt using external JTAG access with a programming cable.

3.4 Verify repeated master serial configuration of FPGA using PROM. Include check of PROG button, DONE indicator, and MODE jumper.

3.4.1 Required: Standard USB cable and Xilinx iMPACT. MCS programming file for "boardtest" design with CCLK startup.

3.4.2 Set-Up: Program the PROM with the "boardtest" design. Place the FPGA into Master Serial configuration mode by setting J26. Enable the PROM by shorting J46-1 to J46-2 (PROM enabled until DONE high). Turn off the power.

3.4.3 Execution: Turn on the power, inspect the DONE indicator and look for signs of activity. Press PROG, monitor the DONE indicator and look for signs of activity. Without cycling the power, erase and re-program the PROM, selecting to force FPGA re-configuration (via CF#). Monitor the DONE indicator and look for signs of activity. Repeat this test, but short J46-2 to J46-3 instead (PROM always enabled).

3.4.4 Expected Results: For each of the three events (power-on, button press, and configuration force) the DONE indicator should first be extinguished, then illuminate. Assertion of DONE should be followed by some evidence of activity.

3.4.5 Contingency Plan: None.

3.5 Verify ST serial flash programming via iMPACT.

3.5.1 Required: Jumper shorting blocks and Xilinx iMPACT. MCS programming file for "boardtest" design over SPI with CCLK startup.

3.5.2 Set-Up: Turn off the power. Enable the ST serial flash by shorting J1-ROMCS1 to J1-CSOB and J1-ROMCS0 to J1-CSOSEL. Remove any jumper from J46. Install a jumper on J16. Short J23 to J25 and turn on the power.

3.5.3 Execution: Start iMPACT in Direct SPI Configuration mode. Select the correct device (M25P16) and load the "boardtest" MCS file. Erase the device and then program it.

3.5.4 Expected Results: All erase and programming attempts should pass.

3.5.5 Contingency Plan: None.

3.6 Verify repeated SPI configuration of FPGA using ST serial flash. Include check of PROG button, DONE indicator, and MODE jumper.

3.6.1 Required: Jumper shorting blocks and Xilinx iMPACT. MCS programming file for "boardtest" design with CCLK startup.

3.6.2 Set-Up: Program the SPI flash memory device. Place the FPGA into SPI configuration mode by setting J26. Remove any jumper from J16. Turn off the power.

3.6.3 Execution: Turn on the power, inspect the DONE indicator and look for signs of activity. Press PROG, monitor the DONE indicator and look for signs of activity.

3.6.4 Expected Results: For each of the two events (power-on and button press) the DONE indicator should first be extinguished, then illuminate. Assertion of DONE should be followed by some evidence of activity.

3.6.5 Contingency Plan: None.

3.7 Verify AT serial flash programming via iMPACT.

3.7.1 Required: Jumper shorting blocks and Xilinx iMPACT. MCS programming file for "boardtest" design over SPI with CCLK startup.

3.7.2 Set-Up: Turn off the power. Enable the AT serial flash by shorting J1-ROMCS0 to J1-CSOB and J1-ROMCS1 to J1-CSOSEL. Remove any jumper from J46. Install a jumper on J16. Short J23 to J25 and turn on the power.

3.7.3 Execution: Start iMPACT in Direct SPI Configuration mode. Select the correct device (AT45DB161D) and load the "boardtest" MCS file. Erase the device and then program it.

3.7.4 Expected Results: All erase and programming attempts should pass.

3.7.5 Contingency Plan: None.

3.8 Verify repeated SPI configuration of FPGA using AT serial flash. Include check of PROG button, DONE indicator, and MODE jumper.

3.8.1 Required: Jumper shorting blocks and Xilinx iMPACT. MCS programming file for "boardtest" design with CCLK startup.

3.8.2 Set-Up: Program the SPI flash memory device. Place the FPGA into SPI configuration mode by setting J26. Remove any jumper from J16. Turn off the power.

3.8.3 Execution: Turn on the power, inspect the DONE indicator and look for signs of activity. Press PROG, monitor the DONE indicator and look for signs of activity.

3.8.4 Expected Results: For each of the two events (power-on and button press) the DONE indicator should first be extinguished, then illuminate. Assertion of DONE should be followed by some evidence of activity.

3.8.5 Contingency Plan: None.

3.9 Verify ST parallel flash programming.

3.9.1 Required: Jumper shorting blocks and Parallel Flash Programmer design bitstream. MCS programming file for "boardtest" design using BPI Up with CCLK startup. Serial cable for HyperTerminal use.

3.9.2 Set-Up: Remove jumpers from J1 and J46, turn on the power, and load the Parallel Flash Programmer via JTAG. Start a HyperTerminal session after attaching a serial cable.

3.9.3 Execution: Erase the device and then program it with the "boardtest" MCS file.

3.9.4 Expected Results: All erase and programming attempts should pass.

3.9.5 Contingency Plan: None.

3.10 Verify repeated BPI-UP configuration of FPGA using ST parallel flash. Include check of PROG button, DONE indicator, and MODE jumper.
- 3.10.1 Required: Jumper shorting blocks and Parallel Flash Programmer design bitstream. MCS programming file for "boardtest" design using BPI Up with CCLK startup. Serial cable for HyperTerminal use.
- 3.10.2 Set-Up: Program the Parallel Flash memory device. Place the FPGA into BPI Up configuration mode by setting J26. Turn off the power.
- 3.10.3 Execution: Turn on the power, inspect the DONE indicator and look for signs of activity. Press PROG, monitor the DONE indicator and look for signs of activity.
- 3.10.4 Expected Results: For each of the two events (power-on and button press) the DONE indicator should first be extinguished, then illuminate. Assertion of DONE should be followed by some evidence of activity.
- 3.10.5 Contingency Plan: None.

3.11 Verify external JTAG/SPI access using Xilinx USB cable.
- 3.11.1 Required: USB programming cable and iMPACT.
- 3.11.2 Set-Up1: Attach external programming cable to J25.
- 3.11.3 Execution1: Verify scan chain integrity. Attempt to program FPGA and PROM device(s) with "boardtest" programming file.
- 3.11.4 Set-Up2: Attach external programming cable to J23.
- 3.11.5 Execution2: Attempt to program AT and ST device(s) with "boardtest" programming file using direct SPI programming.
- 3.11.6 Expected Results: All programming attempts should succeed.
- 3.11.7 Contingency Plan: None.

3.12 Verify external JTAG/SPI access using Xilinx PC4 cable.
- 3.12.1 Required: PC4 programming cable and iMPACT.
- 3.12.2 Set-Up1: Attach external programming cable to J25.
- 3.12.3 Execution1: Verify scan chain integrity. Attempt to program FPGA and PROM device(s) with "boardtest" programming file.
- 3.12.4 Set-Up2: Attach external programming cable to J23.
- 3.12.5 Execution2: Attempt to program AT and ST device(s) with "boardtest" programming file using direct SPI programming.
- 3.12.6 Expected Results: All programming attempts should succeed.
- 3.12.7 Contingency Plan: None.

3.13 Verify external JTAG/SPI access using Xilinx MPR cable.
- 3.13.1 Required: MPR programming system and iMPACT.
- 3.13.2 Set-Up1: Attach external programming cable to J25.
- 3.13.3 Execution1: Verify scan chain integrity. Attempt to program FPGA and PROM device(s) with "boardtest" programming file.
- 3.13.4 Set-Up2: Attach external programming cable to J23.
- 3.13.5 Execution2: Attempt to program AT and ST device(s) with "boardtest" programming file using direct SPI programming.
- 3.13.6 Expected Results: All programming attempts should succeed.
- 3.13.7 Contingency Plan: None.

3.14 Verify suspend switch and awake indicator.

3.14.1 Required: At least one functional peripheral on board.

3.14.2 Set-Up: Configure the FPGA using the "boardtest" design.

3.14.3 Execution: Inspect peripherals for indication of activity, also inspect the awake indicator, LD13. Move the suspend switch into the suspend position. Inspect peripherals for indication of activity, also inspect the awake indicator. Return the switch to the run position. Inspect peripherals for indication of activity, also inspect the awake indicator. Repeat this sequence another time.

3.14.4 Expected Results: While the system is awake, the awake indicator should be illuminated and the design should be active. While the system is suspended, the awake indicator should be off and the design inactive.

3.14.5 Contingency Plan: None.

4.0 Clocks

4.1 Verify primary 50 MHz on-board oscillator.

4.1.1 Required: At least one functional peripheral on board.

4.1.2 Set-Up: Configure the FPGA using the "boardtest" design.

4.1.3 Execution: Inspect peripherals for indication of activity.

4.1.4 Expected Results: With two small exceptions, the entire "boardtest" design is clocked by the 50 MHz on-board oscillator. Any sign of correct output activity, on any port or display, indicates that the 50 MHz on-board oscillator is active and received by the FPGA.

4.1.5 Contingency Plan: If the 50 MHz on-board oscillator is non-functional, this must be debugged and corrected (using alternate clock inputs if required, accompanied by corresponding pin swaps in the "boardtest" UCF file). The "boardtest" design must have access to a 50 MHz clock to operate, and it is used in almost all of the subsequent tests.

4.2 Verify secondary on-board oscillator.

4.2.1 Required: VGA display. Standard 3.3v oscillator in DIP8 package. The frequency should be different than 50 MHz for ease of identification.

4.2.2 Set-Up: Configure the FPGA using the "boardtest" design.

4.2.3 Execution: The VGA display shows a "spinner" on the left side that changes state based on activity from the secondary on-board oscillator. First, test without the oscillator installed and note any spinner activity. Second, test with the oscillator installed and note any spinner activity.

4.2.4 Expected Results: Without the oscillator installed, the spinner should not change state. With the oscillator installed, the spinner should advance at a constant rate. There is another spinner on the right side of the display; it should not move at all.

4.2.5 Contingency Plan: If the VGA port is non-functional, derive a modified "boardtest" design with a 3-bit VGA port on an alternate connector (such as the six-pin accessory headers) by swapping pin assignments in the UCF file.

4.3 Verify SMA clock input connector.

4.3.1 Required: VGA display. Standard 3.3v oscillator with SMA connectivity. The frequency should be different than 50 MHz for ease of identification.

4.3.2 Set-Up: Configure the FPGA using the “boardtest” design.

4.3.3 Execution: The VGA display shows a “spinner” on the right side that changes state based on activity from the SMA clock input connector. First, test without the SMA clock input connected and note any spinner activity. Second, test with the SMA clock input connected and note any spinner activity.

4.3.4 Expected Results: Without the SMA clock input connected, the spinner should not change state. With the SMA clock input connected, the spinner should advance at a constant rate. There is another spinner on the left side of the display; it should not move at all.

4.3.5 Contingency Plan: If the VGA port is non-functional, derive a modified “boardtest” design with a 3-bit VGA port on an alternate connector (such as the six-pin accessory headers) by swapping pin assignments in the UCF file.

5.0 Simple Connectors

5.1 Verify Digilent FX2 connector.

5.1.1 Required: Serial cable from DCE port to PC, HyperTerminal. Loop back plug for this connector. Logic probe or equivalent (multi-meter, logic analyzer, etc…)

5.1.2 Set-Up1: Configure the FPGA using the "boardtest" design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the "boardtest" design source. Make sure nothing is plugged into the connector to be tested.

5.1.3 Execution1: In the HyperTerminal window, press the "m" key to run the first "signal short test". Record the status result, either "p" or "f". Then press the "c" key to run the second "signal short test". Record the result, either "p" or "f".

5.1.4 Set-Up2: Starting from the previous set-up, insert the loop back plug.

5.1.5 Execution2: In the HyperTerminal window, press the "n" key to run the first "signal open test". Record the status result, either "p" or "f". Then press the "d" key to run the second "signal open test". Record the result, either "p" or "f".

5.1.6 Set-Up3: Connect a test lead/clip to FX2 connector pin FX2_CLKIO.

5.1.7 Execution 3: Using a logic probe or logic analyzer, visually inspect the FX2 connector pin FX2_CLKIO for activity.

5.1.8 Expected Results: All four tests should pass; inspection of the FX2_CLKIO pin should show behavior similar to LD0. Debug failing tests using a logic analyzer or Chip Scope; use of the extended "boardtest" status reporting commands to print out the location of the first failing pin.

5.1.9 Contingency Plan: If the DCE port is non-functional, this must be debugged and corrected (using alternate pins if required, accompanied by corresponding pin swaps in the "boardtest" UCF file). The "boardtest" design requires a DCE port to run interactive tests.

5.2 Verify Agilent soft-touch connector. Note: The Agilent soft-touch connector shares all its pins with the Digilent FX2 connector. As the routes from the FPGA to the Digilent FX2 connector are through the Agilent soft-touch connector, the Digilent FX2 connector test also verifies the Agilent soft-touch connector.

5.3 Verify Digilent 6-pin I/O connectors.

5.3.1 Required: Serial cable from DCE port to PC, HyperTerminal. Loop back plugs for connectors J18 and J20. Note that J19 is not tested here, because it is not stuffed. However, the "reserved" I/O test may be used to test J19 if desired.

5.3.2 Set-Up1: Configure the FPGA using the "boardtest" design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the "boardtest" design source. Make sure nothing is plugged into the connectors to be tested.

5.3.3 Execution1: In the HyperTerminal window, press the "e" key to run the "signal short test". Record the status result, either "p" or "f".

5.3.4 Set-Up2: Starting from the previous set-up, insert the loop back plugs.

5.3.5 Execution2: In the HyperTerminal window, press the "f" key to run the "signal open test". Record the status result, either "p" or "f".

5.3.6 Expected Results: Both tests should pass. Debug failing tests using a logic analyzer or Chip Scope; use of the extended "boardtest" status reporting commands to print out the location of the first failing pin.

5.3.7 Contingency Plan: If the DCE port is non-functional, this must be debugged and corrected (using alternate pins if required, accompanied by corresponding pin swaps in the "boardtest" UCF file). The "boardtest" design requires a DCE port to run interactive tests.

5.4 Verify LVDS connectors.

5.4.1 Required: Serial cable from DCE port to PC, HyperTerminal. Loop back plugs for these two connectors (or, 12 shorting blocks, installed to create the same effect).

5.4.2 Set-Up1: Configure the FPGA using the "boardtest" design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the "boardtest" design source. Make sure nothing is plugged into the connectors to be tested.

5.4.3 Execution1: In the HyperTerminal window, press the "k" key to run the "signal short test". Record the status result, either "p" or "f".

5.4.4 Set-Up2: Starting from the previous set-up, insert the loop back plugs.

5.4.5 Execution2: In the HyperTerminal window, press the "l" key to run the "signal open test". Record the status result, either "p" or "f".

5.4.6 Expected Results: Both tests should pass. Debug failing tests using a logic analyzer or Chip Scope; use of the extended "boardtest" status reporting commands to print out the location of the first failing pin.

5.4.7 Contingency Plan: If the DCE port is non-functional, this must be debugged and corrected (using alternate pins if required, accompanied by corresponding pin swaps in the "boardtest" UCF file). The "boardtest" design requires a DCE port to run interactive tests.

5.5 Verify PS/2 connector.

5.5.1 Required: Serial cable from DCE port to PC, HyperTerminal. Loop back plug for this connector.

5.5.2 Set-Up1: Configure the FPGA using the "boardtest" design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the "boardtest" design source. Make sure nothing is plugged into the connector to be tested.

5.5.3 Execution1: In the HyperTerminal window, press the "g" key to run the "signal short test". Record the status result, either "p" or "f".

5.5.4 Set-Up2: Starting from the previous set-up, insert the loop back plug.

5.5.5 Execution2: In the HyperTerminal window, press the "h" key to run the "signal open test". Record the status result, either "p" or "f".

5.5.6 Expected Results: Both tests should pass. Debug failing tests using a logic analyzer or Chip Scope; use of the extended "boardtest" status reporting commands to print out the location of the first failing pin.

5.5.7 Contingency Plan: If the DCE port is non-functional, this must be debugged and corrected (using alternate pins if required, accompanied by corresponding pin swaps in the "boardtest" UCF file). The "boardtest" design requires a DCE port to run interactive tests.

6.0 Memory Devices

6.1 Verify DDR2 SDRAM x16 device.

6.1.1 Required: Serial cable from DCE port to PC, HyperTerminal.

6.1.2 Set-Up: Configure the FPGA using the "boardtest" design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the "boardtest" design source.

6.1.3 Execution: In the HyperTerminal window, press the "7" key to read the SDRAM status. Record the status result, either "p" or "f".

6.1.4 Expected Results: This test should pass.

6.1.5 Contingency Plan: None.

6.2 Verify ST parallel flash device.

6.2.1 Required: Serial cable from DCE port to PC, HyperTerminal.

6.2.2 Set-Up1: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source.

6.2.3 Execution1: In the HyperTerminal window, press the “w” key to perform the cfi status test. Record the status result, either “p” or “f”.

6.2.4 Set-Up2: The following test must not be used during production test; it is for initial verification only. Using this test during production will corrupt the data stored in the parallel flash device.

6.2.5 Execution2: In the HyperTerminal window, press the “z” key to perform the data test. Record the status result, either “p” or “f”.

6.2.6 Set-Up3: The following test must not be used during production test; it is for initial verification only. Using this test during production will corrupt the data stored in the parallel flash device.

6.2.7 Execution3: In the HyperTerminal window, press the “y” key to perform the address test. Record the status result, either “p” or “f”.

6.2.8 Expected Results: All tests should pass.

6.2.9 Contingency Plan: None.

6.3 Verify ST serial flash device(s) and related jumpers.

6.3.1 Required: Serial cable from DCE port to PC, HyperTerminal.

6.3.2 Set-Up: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source. Short J1-ROMCS0 to J1-CSOB and J1-ROMCS1 to J1-CSOSEL.

6.3.3 Execution: In the HyperTerminal window, press the “q” key to perform the serial flash identification test. Record the status result, either “p” or “f”.

6.3.4 Expected Results: The test should pass.

6.3.5 Contingency Plan: None.

6.4 Verify AT serial flash device(s) and related jumpers.

6.4.1 Required: Serial cable from DCE port to PC, HyperTerminal.

6.4.2 Set-Up: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source. Short J1-ROMCS0 to J1-CSOB and J1-ROMCS1 to J1-CSOSEL.

6.4.3 Execution: In the HyperTerminal window, press the “r” key to perform the serial flash identification test. Record the status result, either “p” or “f”.

6.4.4 Expected Results: The test should pass.

6.4.5 Contingency Plan: None.

6.5 Verify Platform Flash device(s) and related jumpers.

6.5.1 Required: Serial cable from DCE port to PC, HyperTerminal.

6.5.2 Set-Up: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source. Locate J46, short J46-2 to J46-3 with a jumper.

6.5.3 Execution: In the HyperTerminal window, press the “u” key to perform the Platform Flash sync word read test. Record the status result, either “p” or “f”.

6.5.4 Expected Results: The test should pass.

6.5.5 Contingency Plan: None.

7.0 Peripherals

7.1 Verify four slide switches.

7.1.1 Required: Serial cable from DCE port to PC, HyperTerminal.

7.1.2 Set-Up: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source.

7.1.3 Execution: In the HyperTerminal window, press the “o” key to enter the mechanical input test. Toggle each of the slide switches. Record the output log. When finished, press any key to exit the mechanical switch test.

7.1.4 Expected Results: Mechanical activity and status should match:

SW0 moved up – y.4
SW0 moved dn – z.4
SW1 moved up – y.5
SW1 moved dn – z.5
SW2 moved up – y.6
SW2 moved dn – z.6
SW3 moved up – y.7
SW3 moved dn – z.7

7.1.5 Contingency Plan: If the DCE port is non-functional, this must be debugged and corrected (using alternate pins if required, accompanied by corresponding pin swaps in the “boardtest” UCF file). The “boardtest” design requires a DCE port to run interactive tests.

7.2 Verify four momentary pushbuttons.

7.2.1 Required: Serial cable from DCE port to PC, HyperTerminal.

7.2.2 Set-Up: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source.

7.2.3 Execution: In the HyperTerminal window, press the “o” key to enter the mechanical input test. Press and release each of the momentary pushbuttons. Record the output log. When finished, press any key to exit the mechanical switch test.

7.2.4 Expected Results: Mechanical activity and status should match:

BTN_E pressed – y.0
BTN_E released – z.0
BTN_S pressed – y.1
BTN_S released – z.1
BTN_W pressed – y.2
BTN_W released – z.2
BTN_N pressed – y.3
BTN_N released – z.3

7.2.5 Contingency Plan: If the DCE port is non-functional, this must be debugged and corrected (using alternate pins if required, accompanied by corresponding pin swaps in the “boardtest” UCF file). The “boardtest” design requires a DCE port to run interactive tests.

7.3 Verify rotary pushbutton.

7.3.1 Required: Serial cable from DCE port to PC, HyperTerminal.

7.3.2 Set-Up: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source.

7.3.3 Execution: In the HyperTerminal window, press the “o” key to enter the mechanical input test. Exercise the pushbutton feature of this knob. Rotate the knob several clicks in each direction. Record the output log. When finished, press any key to exit the mechanical switch test.

7.3.4 Expected Results: Mechanical activity and status should match:

KNOB pressed – y.9
KNOB released – z.9
KNOB rotate CW one “click” – y.8
KNOB rotate CCW one “click” – z.8

7.3.5 Contingency Plan: If the DCE port is non-functional, this must be debugged and corrected (using alternate pins if required, accompanied by corresponding pin swaps in the “boardtest” UCF file). The “boardtest” design requires a DCE port to run interactive tests.

7.4 Verify eight indicators.

7.4.1 Required: Nothing.

7.4.2 Set-Up: Configure the FPGA using the “boardtest” design.

7.4.3 Execution: Observe the LED indicators which should display a test pattern generated by the “boardtest” design.

7.4.4 Expected Results: Display of a “one-hot” pattern, rotating left every half second. Only one indicator is illuminated at a time; two or more illuminated at a time indicates a short or stuck-at-one fault. All indicators should light in sequence; skipping one ore more indicators indicates an open or stuck-at zero fault.

7.4.5 Contingency Plan: None.

7.5 Verify LCD display.

7.5.1 Required: Nothing.

7.5.2 Set-Up: Configure the FPGA using the “boardtest” design.

7.5.3 Execution: Observe the LCD display which should display a test pattern generated by the “boardtest” design.

7.5.4 Expected Results: The first line of the test pattern should read “WALKING ONE ZERO”. The second line of the test pattern consists of characters 01h, 02h, 04h, 08h, 10h, 20h, 40h, 80h, FEh, FDh, FBh, F7h, EFh, DFh, BFh, 7Fh. These are mostly non-ASCII characters, some of which are garbage.

7.5.5 Contingency Plan: None.

7.6 Verify 12-bit VGA output.

7.6.1 Required: VGA display.

7.6.2 Set-Up: Configure the FPGA using the “boardtest” design.

7.6.3 Execution: The VGA display should properly sync and display a test pattern generated by the “boardtest” design.

7.6.4 Expected Results: There are five regions in the test pattern to check:

Top left – Red DAC, 16 intensities from FS to OFF
Top center – Green DAC, 16 intensities from FS to OFF
Top right – Blue DAC, 16 intensities from FS to OFF
Mid left – Clock spinner (ignore for this test)
Mid center – Grayscale, 16 intensities from FS to OFF
Mid right – Clock spinner (ignore for this test)
Bottom – Vertical lines (resolution test pattern)

7.6.5 Contingency Plan: None.

7.7 Verify DCE, DTE serial ports.

7.7.1 Required: Serial cable from DCE port to PC, HyperTerminal. Loop back plug for DTE connector. Multi-meter.

7.7.2 Set-Up1: Configure the FPGA using the "boardtest" design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the "boardtest" design source. Make sure nothing is plugged into the DTE connector to be tested.

7.7.3 Execution1: In the HyperTerminal window, press the "a" key to run the DCE test. Record the status result, either "p" no response. If there is no response, recheck the connections and try again. If there is still no response, use the contingency plan. Once the DCE test is passing, press the "b" key to run the DTE test. Record the status result, either "p" or "f".

7.7.4 Set-Up2: Starting from the previous set-up, insert the loop back plug.

7.7.5 Execution2: In the HyperTerminal window, press the "b" key to re-run the DTE test. Record the status result, either "p" or "f".

7.7.6 Set-Up3: Remove all connectors/cables from DCE and DTE ports.

7.7.7 Execution 3: Using a multi-meter, verify that on the DCE connector, pin 7 and pin 8 are shorted together. Also verify that pin 1, pin 4, and pin 6 are shorted together. Verify that the two groups of shorted pins are not shorted to each other. Repeat this test for the DTE connector. Verify that the two pin groups on each connector are not shorted to any pin group on the other connector.

7.7.8 Expected Results: The DCE test should always pass. The first run of the DTE test without loop back should fail. The second run of the DTE test with loop back should pass. The pin continuity tests should behave as described in the test execution section.

7.7.9 Contingency Plan: If the DCE port is non-functional, this must be debugged and corrected (using alternate pins if required, accompanied by corresponding pin swaps in the "boardtest" UCF file). The "boardtest" design requires a DCE port to run interactive tests.

7.8 Verify both regulators adjustment via I2C.

7.8.1 Required: Serial cable from DCE port to PC, HyperTerminal. Loop back cables for analog connectors (two one-wire).

7.8.2 Set-Up: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source.

7.8.3 Execution: After the design is loaded, but before starting the test, remove jumpers from J12 and J41. Using the loop back cables, connect J12-1 to J22-3 and J41-1 to J22-4. This connects USB1V8 supply through AMP1 to ADC-A, and DAC_REF through AMP2 to ADC-B. In the HyperTerminal window, press the “v” key to run the test. Record the status result, either “p” or “f”. After the test completes, remove the loopback cables and re-install jumpers J12 and J41 before proceeding to other tests.

7.8.4 Expected Results: The test should pass.

7.8.5 Contingency Plan: If the ADC is non-functional, re-write a simple, slower test that may be verified via digital multi-meter.

7.9 Verify DAC, AMP, ADC, and connectors.

7.9.1 Required: Serial cable from DCE port to PC, HyperTerminal. Loop back cable for analog connectors (two wire).

7.9.2 Set-Up1: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source. Using the loop back cable, connect J21-1 to J22-3 and J21-2 to J22-4. This connects DAC-A through AMP1 to ADC-A, and DAC-B through AMP2 to ADC-B.

7.9.3 Execution1: In the HyperTerminal window, press the “s” key to run the test. Record the status result, either “p” or “f”.

7.9.4 Set-Up2: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source. Using the loop back cable, connect J21-3 to J22-3 and J21-4 to J22-4. This connects DAC-C through AMP1 to ADC-A, and DAC-D through AMP2 to ADC-B.

7.9.5 Execution2: In the HyperTerminal window, press the “t” key to run the test. Record the status result, either “p” or “f”.

7.9.6 Expected Results: Both tests should pass.

7.9.7 Contingency Plan: None.

7.10 Verify Ethernet analog and PHY.

7.10.1 Required: Serial cable from DCE port to PC, HyperTerminal. Loop back cable for Ethernet.

7.10.2 Set-Up1: Configure the FPGA using the “boardtest” design and set up a HyperTerminal session for 9600-8N1. A session configuration file resides with the “boardtest” design source.

7.10.3 Execution1: Observe the Ethernet port LEDs, both should be off. In the HyperTerminal window, press the “0” key to reset the PHY. Then, press the “1” key to run the SMI test. Record the status result, either “p” or “f”.

7.10.4 Set-Up2: Insert the Ethernet loop back cable. Observe the Ethernet port LEDs. The right indicator should illuminate, indicating link up.

7.10.5 Execution2: In the HyperTerminal window, press the “6” key to run the data test. Observe the LEDs, the activity indicator should blink. Record the status result, either “p” or “f”.

7.10.6 Expected Results: Both tests should pass.

7.10.7 Contingency Plan: None.

7.11 Verify stereo audio output.

7.11.1 Required: Headphones or speakers with stereo mini-plug.

7.11.2 Set-Up: Configure the FPGA using the “boardtest” design.

7.11.3 Execution: The “boardtest” design generates a repeated “left” and “right” test sound.

7.11.4 Expected Results: The “left” sound should be heard through the left speaker/headphone and the “right” sound should be heard through the right speaker/headphone.

7.11.5 Contingency Plan: None.