Switching

G54ACC

Lecture 7

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What is it all about?

- How do we move traffic from one part of the network to another?
- Connect end-systems to switches, and switches to each other
- Data arriving to an input port of a switch have to be moved to one or more of the output ports

Contents

- Types of Switching Element
- Requirements
- Multistage Networks

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- Types of Switching Element
  - Classification
  - Functions
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Types of Switching Elements

- Telephone switches
  - ...switch samples
- Datagram routers
  - ...switch datagrams
- ATM switches
  - ...switch ATM cells

Classification

- Packet *vs*. circuit switches
  - Packets have headers and samples don't
- Connectionless *vs*. connection oriented
  - Connection oriented switches need a call setup
  - Setup is handled in *control plane* by *switch controller*
  - Connectionless switches deal with *self-contained* datagrams

	Connectionless (router)	*Connection-oriented (switching system)*
Packet switch	Internet router	ATM switching system
Circuit switch		Telephone switching system

Other Switching Element Functions

- Participate in routing algorithms
  - ...to build routing tables
- Resolve contention for output trunks
  - ...scheduling
- Admission control
  - ...to guarantee resources to certain streams

Contents

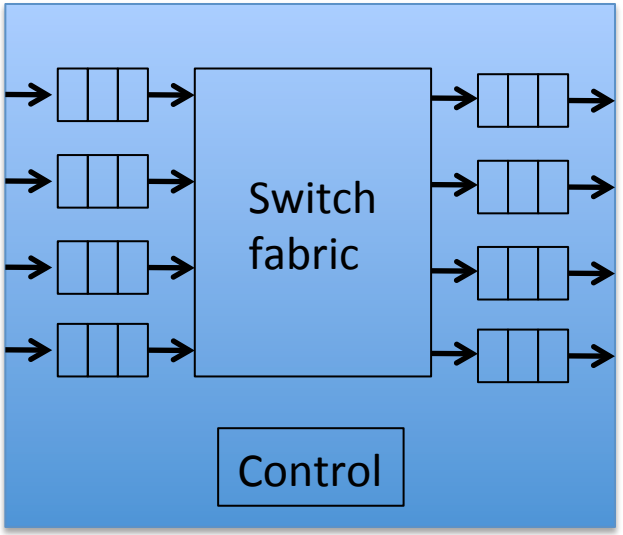
- Types of Switching Element
- Requirements
  - First generation
  - Second generation
  - Third generation
  - Crossbar
- Multistage Networks

Requirements

- *Capacity* of switch
  - The maximum rate at which it can move information, assuming all data paths are simultaneously active
- Primary goal: Maximize capacity
  - ...subject to cost and reliability constraints
- Secondary:
  - Circuit switch must reject call if can't find a path for samples from input to output
    - Minimize call blocking
  - Packet switch must reject a packet if it can't find a buffer to store it awaiting access to output trunk
    - Minimize packet loss and reordering

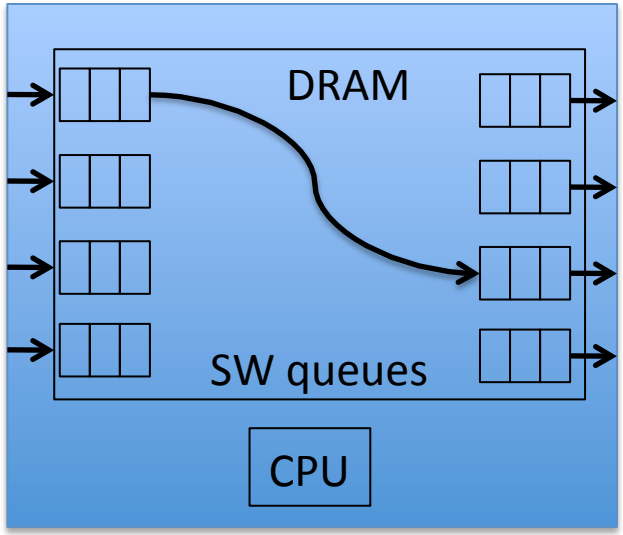
A Generic Switch

- Input buffers
- Output buffers
- *Line-card* has
  - Input and output buffers, and
  - Transmission interfaces
- *Switch fabric* or *Interconnect*
- A processor for control functions (routing, etc.)



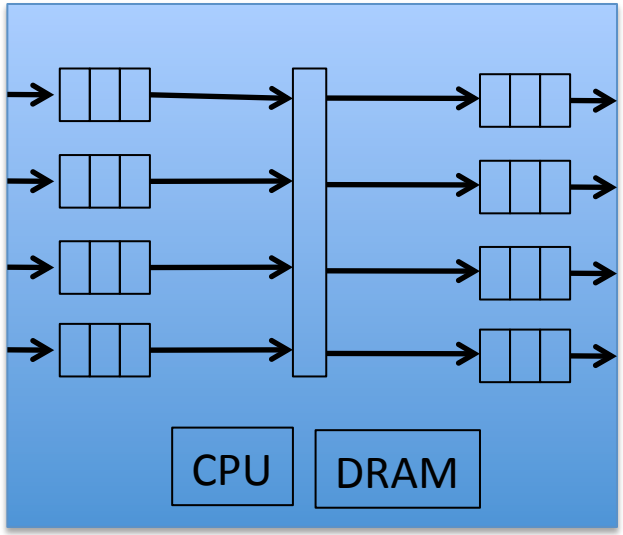
First Generation

- All buffers in one simple memory system
- CPU makes forwarding decision and copies packets/manipulates queues
- Most simple Ethernet switches and cheap packet routers
  - e.g. home routers
- Bottlenecks:
  - CPU, host-adaptor or I/O bus
  - First Cisco routers were built using 200MHz SPARC boards



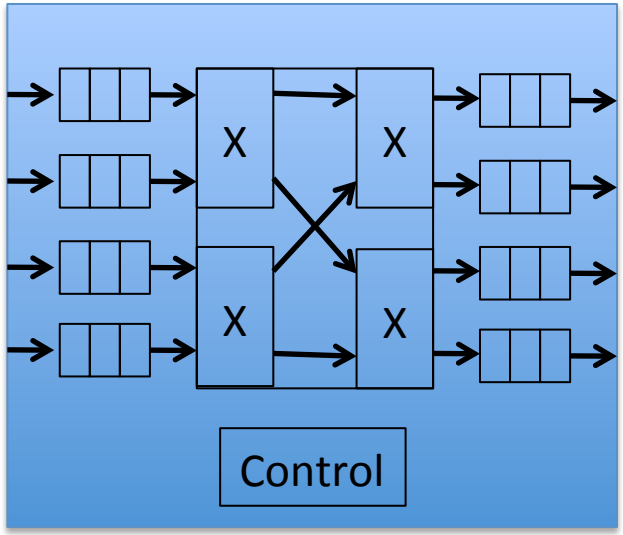
Second Generation

- Line cards contain
  - Input & output buffers
  - Forwarding intelligence
- Simple bus interconnect
- CPU populates forwarding tables from
  - Routing protocol, or
  - Connection set up
- Bottleneck is bus
  - FORE ATM switches used 2.4Gbps bus

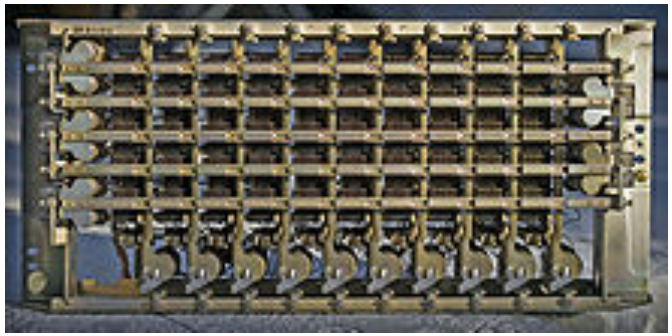


Third Generation

- Simple bus does not scale well
- Need parallel paths
- Introduce interconnection networks

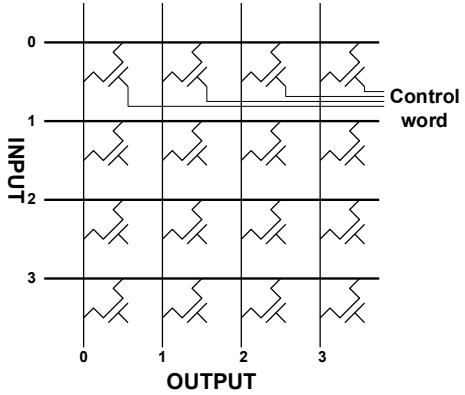


Crossbar



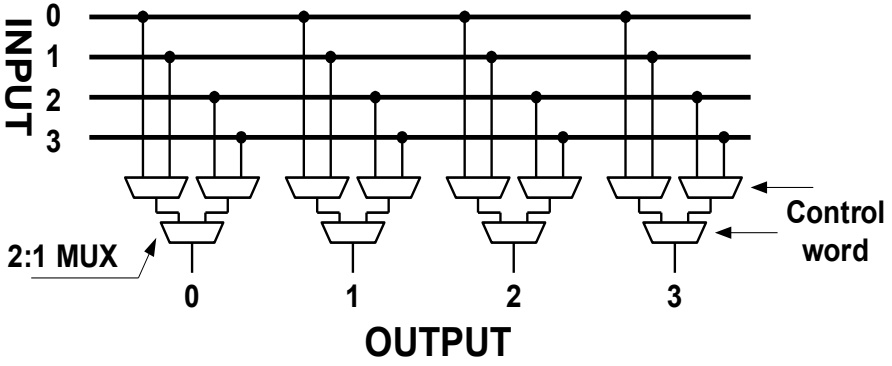
Simplest possible space-division switch

- X-Y based crossbar



- Scalability: N^2
- Speed: **limited by capacity at input and output lines**
- Control: N^2 **bits**

- Mux based crossbar



- Scalability: N^2
- Speed: **limited by capacity only at input line**
- Control: $N*\log_2 N$ **bits**

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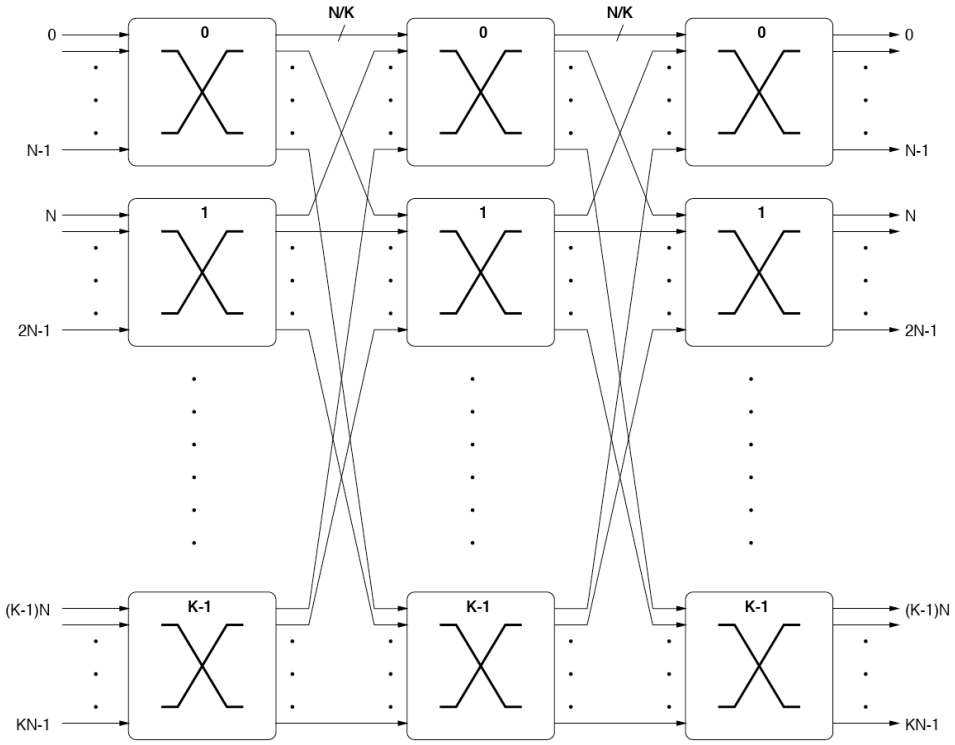
- Types of Switching Element
- Requirements
- Multistage Networks
  - Buffering
  - CIOQ
  - VOQ
  - Blocking

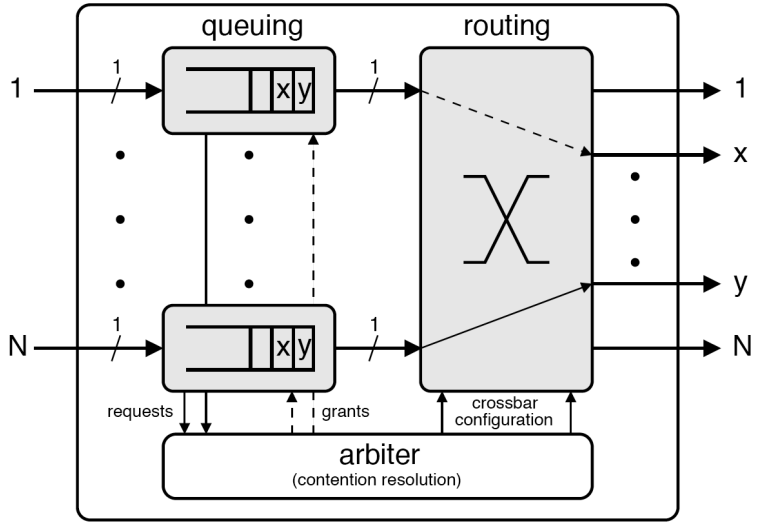
Multistage Networks

- Build large fabrics from smaller crossbar
- What might be some problems here?
- Number of crosspoints?
- Input and output capacity depends on buffering strategy



Input Buffering

- One queue per input
- Input and output capacity equals transmission line rate
- Needs *arbitration* to decide who wins
- Problem: *head of line blocking*
  - with uniformly randomly distributed packets, utilization ≈ 58.6%
  - Worse with *hot spots*

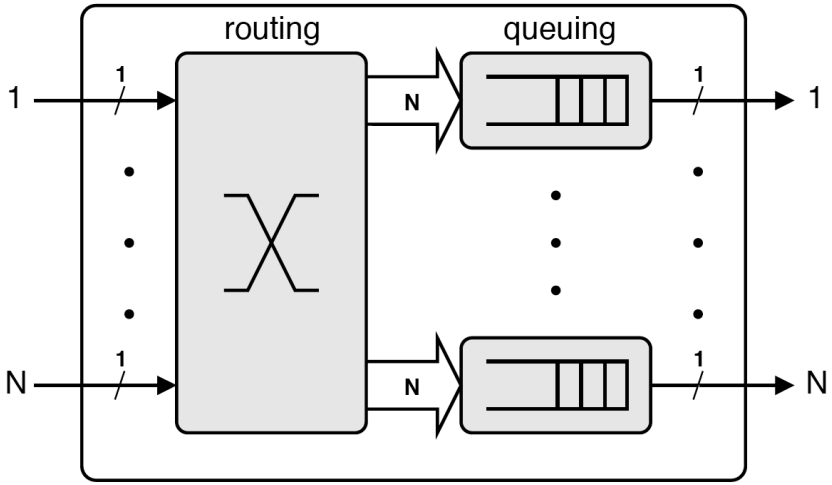


As *N* grows large, HoL limits utilization to (2 – √2) ≈ 58.6%

Aggregate fabric capacity 2*N*

Output Buffering

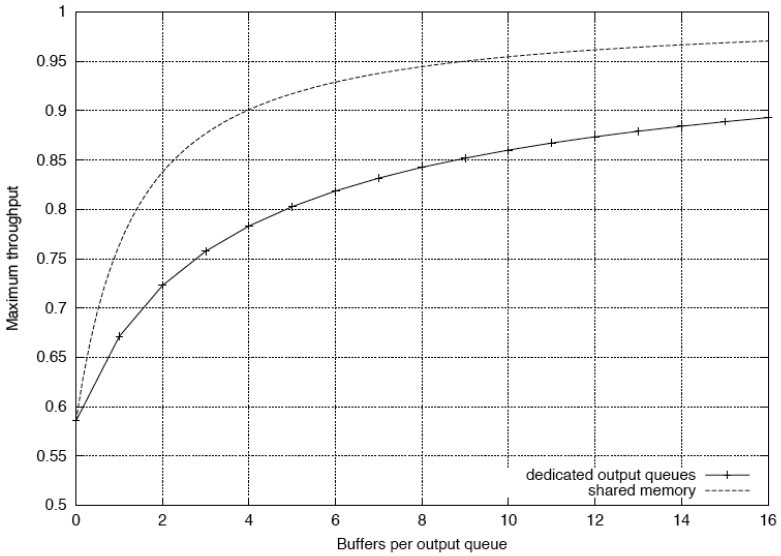
- One queue per output
  - No queues at input
- Input capacity is same as transmission line rate
- Output capacity is *N* times line rate
- Switch fabric output grows as N^2
- Can achieve 100% throughput

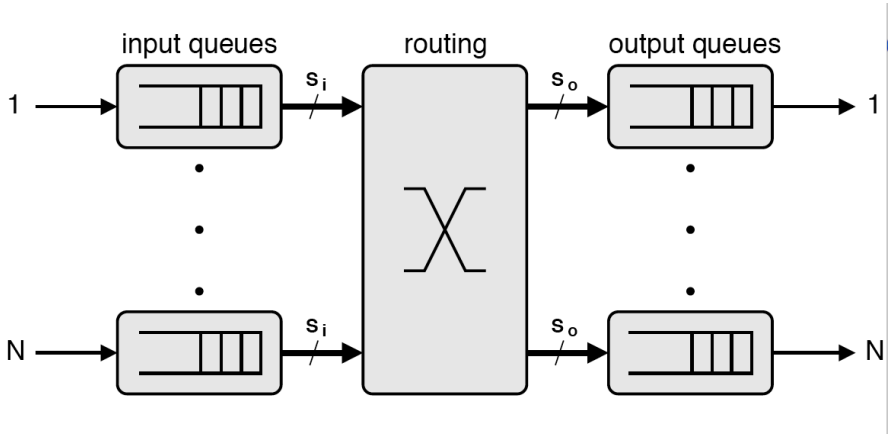


100% throughput

Aggregate fabric capacity is $N(N+1)$

CIOQ



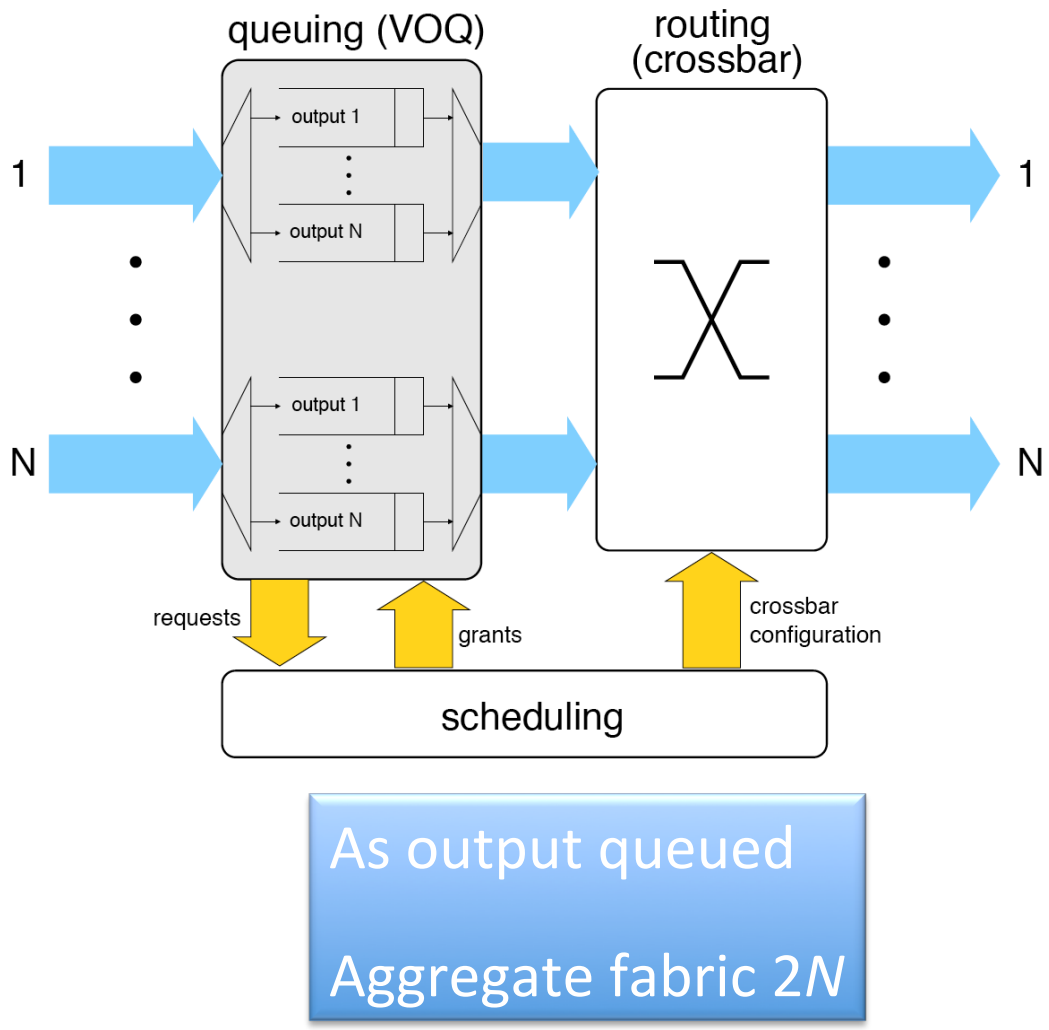


- Combined input and output queues
- Apply speed up S_i at input and S_o at output

Apply speed ups S_i and S_o

Aggregate fabric $N(S_o + S_i)$

VOQ



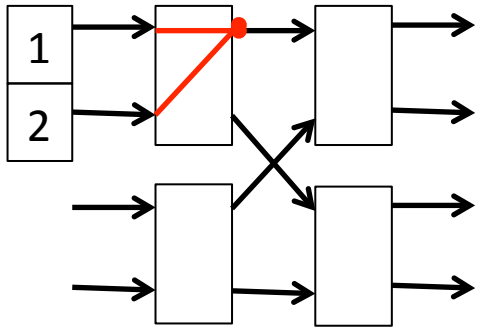
- Virtual output queues
- All magic and complexity in the arbitration

As output queued

Aggregate fabric 2*N*

Blocking

- We have come across HoL. Where else?
  - Internal blocking in complex switch fabrics
  - Two packets need same internal link



Dealing with Blocking

- Overprovisioning
  - Internal links much faster than inputs
- Buffers at input or output
- Backpressure
  - Prevent packet from entering until path is available
- Parallel switch fabrics
  - Increases effective switching capacity

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  - Blocking

Quiz (1)

1. What is the key difference between a packet switch and a circuit switch? Give an example of each.
2. What is the key difference between a connection-oriented and a connection-less switch? Give an example of each.
3. Why are input and output buffers required in a line card?
4. Why is admission control required to guarantee resource to streams? Can you think of an alternative?
5. Describe the evolution from first to third generation switches. What are the costs of increasing performance?

Quiz (2)

6. What is the trade-off between X-Y and mux based crossbar switches?
7. Give two factors that impact scaling a multistage crossbar switch.
8. When does HoL blocking occur, and why is it a problem?
9. One solution to HoL blocking is output buffering – why is it not always used? (What cost does it incur?)
10. What other situations can cause blocking inside the switch, and how can they be alleviated?