UNIVERSIDAD AUTÓNOMA DE BAJA CALIFORNIA

Facultad de Ciencias Químicas e Ingeniería

Materia: Microprocesadores y Microcontroladores

Practica 10 Generador de Frecuencia y Convertidor Analógico-Digital del ATmega1280

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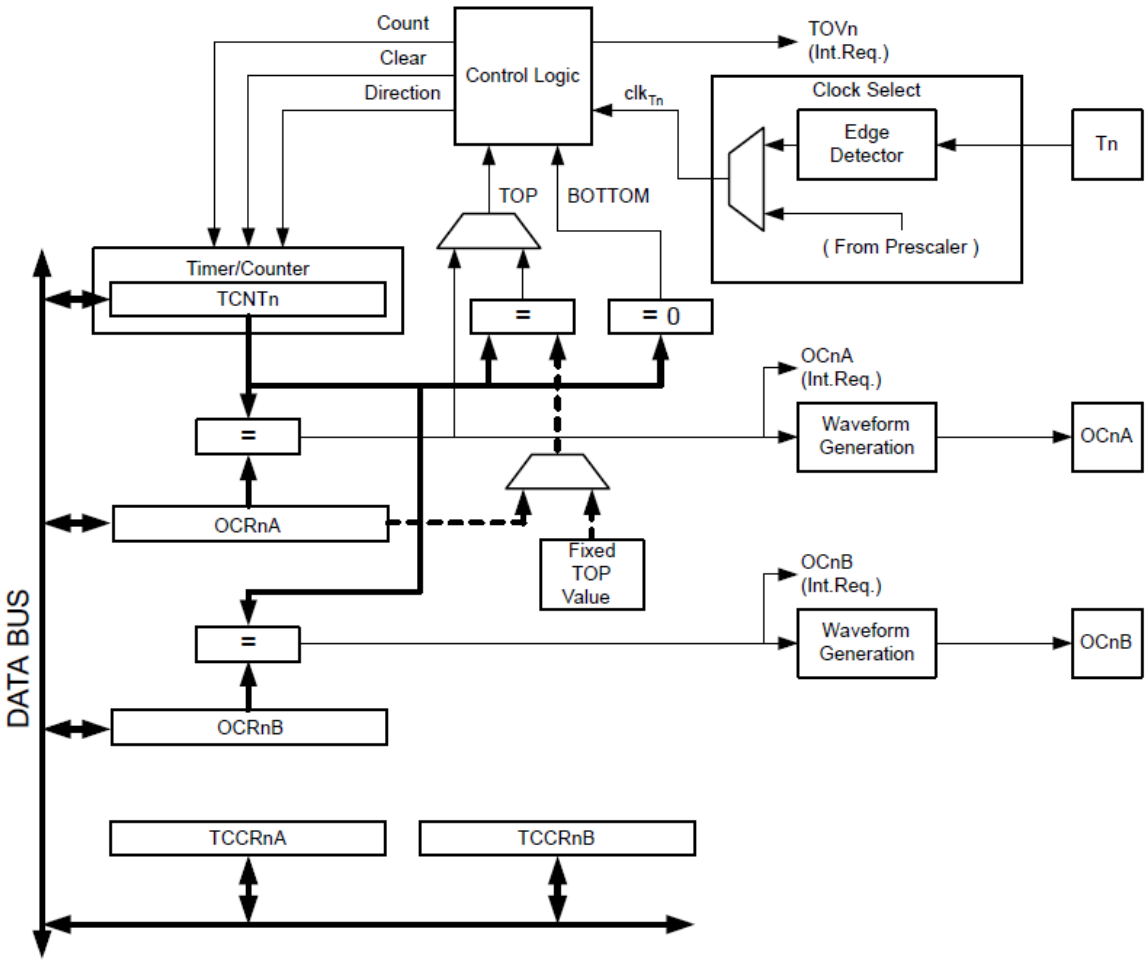
Teoría

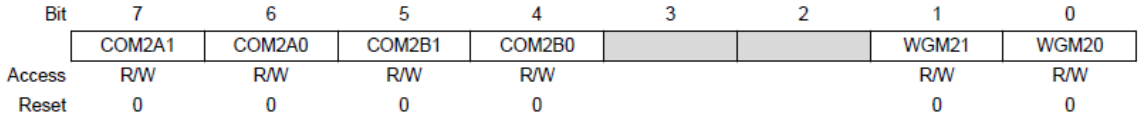
Timer 2

Las siguientes imágenes contiene los registros con sus respectivos bits utilizados para la programación de timer2.

Figure 19-1. 8-bit Timer/Counter Block Diagram

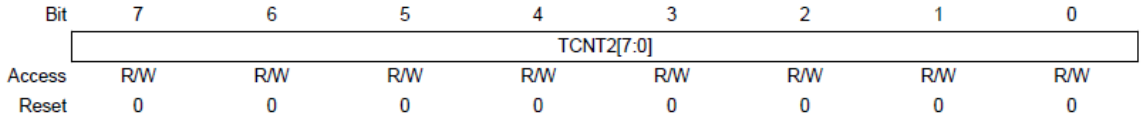


Name: TCCR2A
Offset: 0xB0
Reset: 0x00
Property: -



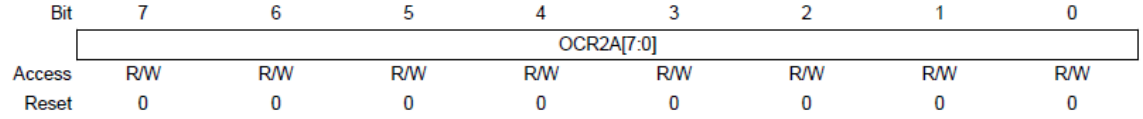
Bit	7	6	5	4	3	2	1	0
	COM2A1	COM2A0	COM2B1	COM2B0			WGM21	WGM20
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

Name: TCNT2
Offset: 0xB2
Reset: 0x00
Property: -



Bit	7	6	5	4	3	2	1	0
	TCNT2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Name: OCR2A
Offset: 0xB3
Reset: 0x00
Property: -



Bit	7	6	5	4	3	2	1	0
	OCR2A[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

COM2A1	COM2A0	Description
0	0	Normal port operation, OC2A disconnected.
0	1	Toggle OC2A on Compare Match.
1	0	Clear OC2A on Compare Match.
1	1	Set OC2A on Compare Match .

Table 19-9. Waveform Generation Mode Bit Description

Mode	WGM22	WGM21	WGM20	Timer/Counter Mode of Operation	TOP	Update of OCR0x at	TOV Flag Set on[1]
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	BOTTOM	MAX
4	1	0	0	Reserved	-	-	-
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	-	-	-
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP

ADC

By default, the successive approximation circuitry requires an input clock frequency between 50kHz and 200kHz to get maximum resolution. If a lower resolution than 10 bits is needed, the input clock frequency to the ADC can be higher than 200kHz to get a higher sample rate.

A normal conversion takes 13 ADC clock cycles.

In Single Conversion mode, always select the channel before starting the conversion. The cannel selection may be changed one ADC clock cycle after writing one to ADSC. However, the simplest method is to wait for the conversion to complete before changing the channel selection.

VREF can be selected as either AVCC, internal 2.56V reference, or external AREF pin.

0x000 represents analog ground, and 0x3FF represents the selected reference voltage minus one LSB.

ADC Conversion Result

After the conversion is complete (ADCSRA.ADIF is set), the conversion result can be found in the ADC Result Registers (ADCL, ADCH).

For single ended conversion, the result is

$$\mathrm{ADC} = \frac{V_{\mathrm{IN}} \cdot 1024}{V_{\mathrm{REF}}}$$

where V_{IN} is the voltage on the selected input pin, and V_{REF} the selected voltage reference (see also descriptions of ADMUX.REFSn and ADMUX.MUX). 0x000 represents analog ground, and 0x3FF represents the selected reference voltage minus one LSB.

Name: ADMUX
Offset: 0x7C
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

REFS[1:0]	Voltage Reference Selection
00	AREF, Internal V_{ref} turned off
01	AV_{CC} with external capacitor at AREF pin
10	Internal 1.1V Voltage Reference with external capacitor at AREF pin
11	Internal 2.56V Voltage Reference with external capacitor at AREF pin

Note: If differential channels are selected, only 2.56V should be used as Internal Voltage Reference.

Name: ADCSRA
Offset: 0x7A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 26-5. ADC Prescaler Selections

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Name: ADCL and ADCH
Offset: 0x78
Reset: 0x00
Property: ADLAR = 0

Bit	15	14	13	12	11	10	9	8
							ADC9	ADC8
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 – ADCn: ADC Conversion Result
These bits represent the result from the conversion. Refer to ADC Conversion Result for details.

Conclusión

En esta práctica aprendí a programar el timer2 como generador de frecuencia y modular el ancho de pulso de esta. Además, aprendí a configurar el ADC.
Lo más complicado en esta práctica fue el encontrar un buen lugar en el que la antena funcionara bien, en base a las lecturas tomadas se estableció un valor que al ser detectado activara la alarma y un led.

Link evidencia

https://drive.google.com/drive/folders/1EizpNeRq-Edc4BGwnW7LnfT49J5QTsYS?usp=sharing

nota: acorte el tiempo de encendido de la alarma debido a que mi conexión es muy lenta y no quería demorar mucho en subir el video.

Bibliografía
Physics of music. https://pages.mtu.edu/~suits/notefreqs.html