**CMPEN 371: Advanced Digital Design**

**Fall 2015**

**Lab 5: Datapath and Control**

**Due: 6 October 2015**

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**ACKNOWLEDGEMENT**

This work is entirely our own and I did not provide any assistance except as noted. The approximate contribution of each team member is as follows:

100% Morayo Ogunsina \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Grading Rubric**

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| **Criteria** | **Grade** |
| Design (Sound algorithm, good block diagrams / state diagrams / state tables, efficient design, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 6 |
| Translate to VHDL (VHDL matches design docs, good comments / whitespace, follows guidelines, efficient coding, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 6 |
| Test in Simulator (test bench or script for each component and FSM, good coverage, components / FSMs verified, etc.)  Excellent: 3; Good: 2; Satisfactory: 1; Unsatisfactory: 0; Failure: -1 or worse | / 3 |
| Test in Hardware (demo in lab)   * Button sequences are detected and mode is indicated on 7-segment display * Train mode works on LEDs * Ping pong mode works on LEDs * Physics mode works on LEDs * Wall mode works * Other | / 35 |
| Bonus (optional challenge, etc.) |  |
| Penalty (late demo, late submission on ANGEL, team member absent from demo, etc.)  Demo late in lab: -5; Demo up to 5 days late: -10; Demo more than 5 days late: -20  Submitted late or incompletely on ANGEL: -5; Not submitted on ANGEL: no grade for lab |  |
| TOTAL | / 50 |

**DESIGN**

The following design documents are attached:

Filename Description

Lab5\_BlockDiagram Block diagram includes Top Level BD and Components BD.

PingPongS Component State Diagram

PingPongT Component State Table.

WallS Component State Diagram

WallT Component State Table

PhysicsS Component State Diagram

PhysicsT Component State Table

TrainT Component State Table

TrainS Component State Diagram

WordTo8 WordTo8dig7seg Block Diagram.

DataPath DataPath Block Diagram.

**TRANSLATE TO VHDL**

The following HDL models are attached:

Filename Description

Lab5\_mao5270 Top Level: displays registers with various functions and the register number.

TrainMode\_FSM Component : A train of 10 LEDs moving every 0.2 second

PingPongMode\_FSM Component : An LED train that moves back and forth bouncing, off the ends

PhyscisMode\_FSM Component : An LED train that triggers a bundle of LEDs to move .

WallMode\_FSM Component : An LED train that bounces back and forth from wall hit

DataPath Component : Data Path of the FSMs

WordTo8dig7seg Component : Converts a 31-bit hexadecimal number to the segment and anode

The following HDL models and other files are not attached but are submitted electronically:

Filename Description

OneShot Component: Produces a one cycle pulse when input goes from low to high.

Debouncer Componentl: Removes rapid transitions, so that mechanical transition results

in one signal transitions.

Register\_nbit Component: An edge sensitive bit storage device that is enabled

synchronously.

Counter\_nbit Component: A counter that counts up per button press.

PulseGenerator Component: Produces a one -cycle pulse every (maxCount +1 )

cycles.

Dff\_CE Component: A D Flip-Flop device that is enabled synchronously.

Mux4to1 Component: Modified to a Generic Mux8to1

**TEST IN SIMULATOR**

The following files were used for testing to verify the design:

Filename Description

HexToSevenSeg\_tb Test bench: Display hex digit.

The only form of tests carried out was in the iSIM .No test benches or tcl files were used to test the components. Each component created was tested before using them to create bigger components.

**TEST IN HARDWARE**

The project implements all the functionality specified.

**PERFORMANCE**

The following cost and performance metrics were obtained:

Area (resources used)

Number of Slice Registers: 159 out of 126.

Number of Slice LUTs: 257 out of 63.

Delay

Minimum Period: 5.167ns

Maximum Frequency: 193.536 MHz

The critical path goes from OSC (OneShotCenterButton), through *DFF and FSM0*, to *STATUS\_in [4](in FSM\_OFF).*

**QUESTIONS**

(There are no questions for this lab)