**CMPEN 371: Advanced Digital Design**

**Fall 2017**

**Basic Combination Design Lab**

**Due: October 4th, 2017**

**Team Serial Code: 2B**

**Siti Nadira, Nor Badrul Aman, sfn5077**

**Morayo Ogunsina, mao5270**

**ACKNOWLEDGEMENT**

This work is entirely our own and I did not provide any assistance except as noted. The approximate contribution of each team member is as follows:

50% Morayo Ogunsina

50% Siti Nadira, Nor Badrul Aman

**Grading Fabric**

|  |  |
| --- | --- |
| **Criteria** | **Grade** |
| Design (Sound algorithm, good block diagrams / state diagrams / state tables, efficient design, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 10 |
| Translate to VHDL (VHDL matches design docs, good comments / whitespace, follows guidelines, efficient coding, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 10 |
| Test in Simulator (test bench or script for each component and FSM, good coverage, components / FSMs verified, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 15 |
| Test in Hardware (demo in lab)   * Describe connection between your VHDL and the block diagrams * Describe your test benches * Demonstrate simulation of top level, how to drill down to lowest levels for debugging * Run Tcl test script (provided at demo time) to fully verify top level | / 15 |
| Bonus (optional challenge, etc.) |  |
| Penalty (late demo, late submission on CANVAS, team member absent from demo, etc.)  Demo late in lab: -2; Demo up to 5 days late: -5; Demo more than 5 days late: -10  Submitted late or incompletely on CANVAS: -5; Not submitted on CANVAS: no grade for lab |  |
| TOTAL | / 50 |

**DESIGN**

The following design documents are attached:

Filename Description

{filename} Detailed (1-2) pages design document explaining the design in top-down approach (e.g., defining inputs and outputs, operation logic (e.g., Truth Table, K-maps), how system can decomposed into sub-components, and the interaction between these different components). In addition to the major details of the internal design of each component.

{filename} Top level block diagram.

{filename} Block diagram of components and the interconnections between them.

{filename} {Scan or quality picture of hand drawn block diagrams, list all files here}

{filename} {Schematic Diagram after verifying the design}

*{Submit electronically and attach hard copies of block diagram(s).}*

**VHDL Design or TRANSLATE TO VHDL**

The following HDL models are attached:

Filename Description

{filename} Top Level: {Brief description of HDL model}

{filename} Component 1: {Brief description of HDL model}

{filename} Component 2: {Brief description of HDL model}

…..

…..

{filename} Component N: {Brief description of HDL model}

*{Submit electronically and attach hard copies of top level design and every component the system is composed of. Print HDL from Xilinx Vivado, select printer preferences then select print on both sides of paper, two pages per side.}*

*{Discuss anything relevant to the digital design that is not obvious from the documents and HDL models such as truth tables, etc.}*

**TEST IN SIMULATOR**

{Brief description of the simulation & test files and in what order they should be used (if specific order is necessarily).}

The following files were used for testing to verify the design:

Filename Description

{filename} {Simulation File (testbench.vhd)}

{filename} {Simulation Results File}

{filename} {Tcl file, if any Tcl commands are used}

*{Submit these files electronically but do not attach hard copies. Briefly discuss testing methodology and results. Were tests performed using Tcl script, VHDL test bench or a combination? Were all input combinations tested (exhaustive testing) or just a subset? If exhaustive testing was not done, how were the test vectors chosen? Briefly discuss results, such as “All tests passed” or “All tests passed except…”}*

**TEST IN HARDWARE**

*{Briefly describe what works and what does not. For example, “The project implements all the functionality specified in the lab handout except…”}*

**QUESTIONS**

*{Answer the following questions directly in this document when possible. If not possible, attach a hard copy of the answer and indicate “see attached.”}*

--- No extra questions this week.