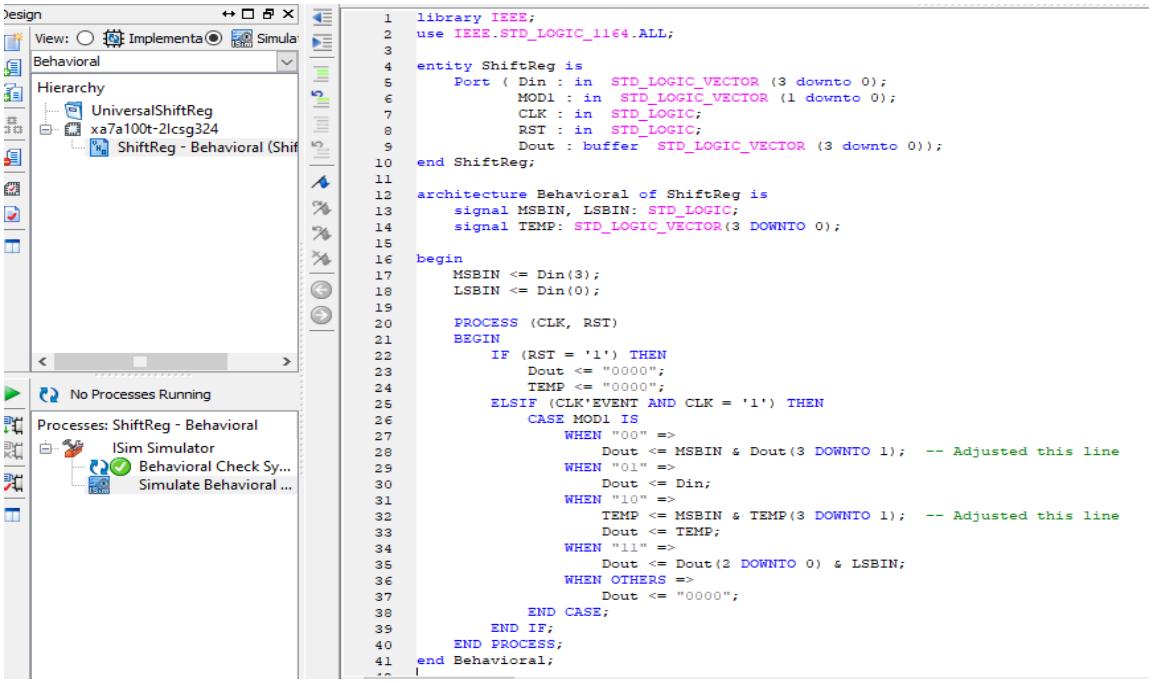
Exp.4 (universal Shift Register)

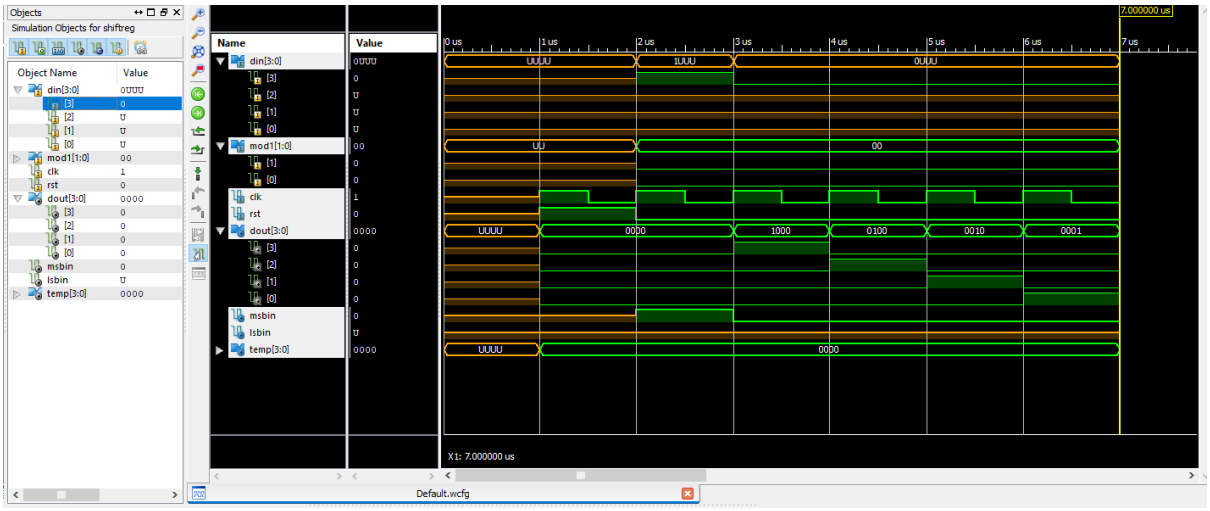
Code:

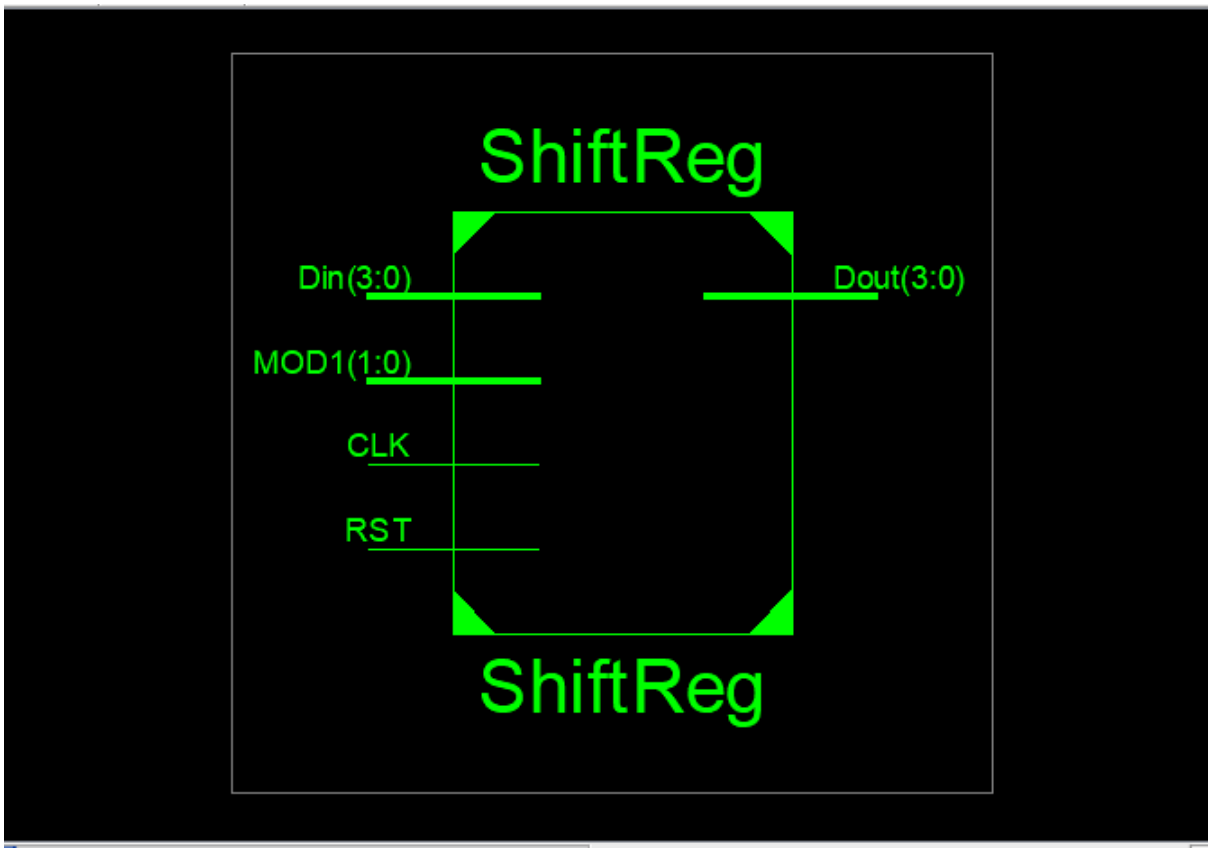
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entityShiftReg is
   Port ( Din : in  STD_LOGIC_VECTOR (3 downto 0);
MOD1 : in  STD_LOGIC_VECTOR (1 downto 0);
CLK : in  STD_LOGIC;
RST : in  STD_LOGIC;
Dout : buffer  STD_LOGIC_VECTOR (3 downto 0));
endShiftReg;

architecture Behavioral of ShiftReg is
signal MSBIN, LSBIN: STD_LOGIC;
signal TEMP: STD_LOGIC_VECTOR(3 DOWNTO 0);
begin
MSBIN <= Din(3);
   LSBIN <= Din(0);
   PROCESS (CLK, RST)
   BEGIN
      IF (RST = '1') THEN
Dout<= "0000";
         TEMP <= "0000";
      ELSIF (CLK'EVENT AND CLK = '1') THEN
         CASE MOD1 IS
            WHEN "00" =>
Dout<= MSBIN &Dout(3 DOWNTO 1);  -- Adjusted this line
            WHEN "01" =>
Dout<= Din;
```

```
            WHEN "10" =>
                TEMP <= MSBIN &TEMP(3 DOWNTO 1);  -- Adjusted this line
Dout<= TEMP;
            WHEN "11" =>
Dout<= Dout(2 DOWNTO 0) & LSBIN;
            WHEN OTHERS =>
Dout<= "0000";
          END CASE;
       END IF;
   END PROCESS;
end  Behavioral;
```



Output:


Objects
Simulation Objects for shiftreg
Object Name
Value
din[3:0]
mod1[1:0]
clk
rst
dout[3:0]
msbin
lsbin
temp[3:0]
Name
Value
7.000000 us
0 us
1 us
2 us
3 us
4 us
5 us
6 us
7 us
UUUU
1UUU
0UUU
UU
00
0000
1000
0100
0010
0001
X1: 7.000000 us
Default.wcfg


ShiftReg
Din(3:0)
Dout(3:0)
MOD1(1:0)
CLK
RST
ShiftReg