

## **Exp.4 (universal Shift Register)**

### **Code:**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity ShiftReg is
    Port ( Din : in  STD_LOGIC_VECTOR (3 downto 0);
          MOD1 : in  STD_LOGIC_VECTOR (1 downto 0);
          CLK : in  STD_LOGIC;
          RST : in  STD_LOGIC;
          Dout : buffer STD_LOGIC_VECTOR (3 downto 0));
end ShiftReg;

architecture Behavioral of ShiftReg is
    signal MSBIN, LSBIN: STD_LOGIC;
    signal TEMP: STD_LOGIC_VECTOR(3 DOWNT0 0);
begin
    MSBIN <= Din(3);
    LSBIN <= Din(0);
    PROCESS (CLK, RST)
    BEGIN
        IF (RST = '1') THEN
            Dout<= "0000";
            TEMP <= "0000";
        ELSIF (CLK'EVENT AND CLK = '1') THEN
            CASE MOD1 IS
                WHEN "00" =>
                    Dout<= MSBIN &Dout(3 DOWNT0 1); -- Adjusted this line
                WHEN "01" =>
                    Dout<= Din;
```

```

        WHEN "10" =>
            TEMP <= MSBIN & TEMP(3 DOWNT0 1); -- Adjusted this line
Dout<= TEMP;

        WHEN "11" =>
Dout<= Dout(2 DOWNT0 0) & LSBIN;

        WHEN OTHERS =>
Dout<= "0000";

    END CASE;

END IF;

END PROCESS;

end Behavioral;

```

```

1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity ShiftReg is
5      Port ( Din : in  STD_LOGIC_VECTOR (3 downto 0);
6            MOD1 : in  STD_LOGIC_VECTOR (1 downto 0);
7            CLK : in  STD_LOGIC;
8            RST : in  STD_LOGIC;
9            Dout : buffer STD_LOGIC_VECTOR (3 downto 0));
10 end ShiftReg;
11
12 architecture Behavioral of ShiftReg is
13     signal MSBIN, LSBIN: STD_LOGIC;
14     signal TEMP: STD_LOGIC_VECTOR(3 DOWNT0 0);
15
16 begin
17     MSBIN <= Din(3);
18     LSBIN <= Din(0);
19
20     PROCESS (CLK, RST)
21     BEGIN
22         IF (RST = '1') THEN
23             Dout <= "0000";
24             TEMP <= "0000";
25         ELSIF (CLK'EVENT AND CLK = '1') THEN
26             CASE MOD1 IS
27                 WHEN "00" =>
28                     Dout <= MSBIN & Dout(3 DOWNT0 1); -- Adjusted this line
29                 WHEN "01" =>
30                     Dout <= Din;
31                 WHEN "10" =>
32                     TEMP <= MSBIN & TEMP(3 DOWNT0 1); -- Adjusted this line
33                     Dout <= TEMP;
34                 WHEN "11" =>
35                     Dout <= Dout(2 DOWNT0 0) & LSBIN;
36                 WHEN OTHERS =>
37                     Dout <= "0000";
38             END CASE;
39         END IF;
40     END PROCESS;
41 end Behavioral;

```

## Output:

