6.823 Computer System Architecture
Snoopy Cache Coherence Protocol

Last Updated:
11/16/2005 12:21 PM

We introduce an invalidation coherence protocol for write-back caches similar to those employed by the SUN MBus. As in most invalidation protocols, only a single cache may *own* a modified copy of a cache line at any one time. However, in addition to allowing multiple shared copies of clean data, multiple shared copies of modified data may also exist. (Here, modified data refers to data different from memory. When multiple shared copies of modified data exist, one of the caches *owns* the current copy of the data instead of the memory.) All shared copies are invalidated any time a new modified (write) copy is created.

The MBus transactions with which we are concerned are:
* Coherent Read (**CR**): issued by a cache on a read miss to load a cache line.
* Coherent Read and Invalidate (**CRI**): issued by a cache on a write-allocate after a write miss.
* Coherent Invalidate (**CI**): issued by a cache on a write hit to a block that is in one of the shared states.
* Block Write (**WR**): issued by a cache on the write-back of a cache block.
* Coherent Write and Invalidate (**CWI**): issued by an I/O processor (DMA) on a block write (a full block at a time).

In addition to these primary bus transactions, there is:
* Cache to Cache Intervention (**CCI**): used by a cache to satisfy other caches' read transactions when appropriate. A **CCI** intervenes and overrides the answers normally supplied by memory. Data should be supplied using **CCI** whenever possible for faster response relative to the memory. However, only the cache that ***owns*** the data can respond by **CCI.**

The five possible states of a data block are:
* Invalid (**I**): Block is not present in the cache.
* Clean exclusive (**CE**): The cached data is consistent with memory, and no other cache has it.
* Owned exclusive (**OE**): The cached data is different from memory, and no other cache has it. This cache is responsible for supplying this data instead of memory when other caches request copies of this data.
* Clean shared (**CS**): The data has not been modified by the corresponding CPU since cached. Multiple **CS** copies and at most one **OS** copy of the same data could exist.
* Owned shared (**OS**): The data is different from memory. Other **CS** copies of the same data could exist. This cache is responsible for supplying this data instead of memory when other caches request copies of this data. (Note, this state can only be entered from the **OE** state.)