SPECIFICATIONS

AV_{DD} = DV_{DD} = V_{VCO} = SDV_{DD} = V_P = 3.3 V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range is −40°C to +85°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF_{IN} CHARACTERISTICS					
Input Frequency	10		250	MHz	For f < 10 MHz, ensure slew rate > 21 V/µs
Input Sensitivity	0.7		AV_{DD}	V p-p	Biased at AV_{DD}/2; ac coupling ensures AV_{DD}/2 bias
Input Capacitance		10		pF	
Input Current			±60	µA	
PHASE FREQUENCY DETECTOR (PFD)					
Phase Detector Frequency			32	MHz	Fractional-N
			45	MHz	Integer-N (band select enabled)
			90	MHz	Integer-N (band select disabled)
CHARGE PUMP					
I_{CP} Sink/Source[1]					R_{SET} = 5.1 kΩ
High Value		5		mA	
Low Value		0.312		mA	
R_{SET} Range	3.9		10	kΩ	
Sink and Source Current Matching		2		%	0.5 V ≤ V_{CP} ≤ 2.5 V
I_{CP} vs. V_{CP}		1.5		%	0.5 V ≤ V_{CP} ≤ 2.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = 2.0 V
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.5			V	
Input Low Voltage, V_{INL}			0.6	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}		3.0		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	DV_{DD} − 0.4			V	CMOS output selected
Output High Current, I_{OH}			500	µA	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	3.0		3.6	V	
DV_{DD}, V_{VCO}, SDV_{DD}, V_P		AV_{DD}			These voltages must equal AV_{DD}
DI_{DD} + AI_{DD}[2]		21	27	mA	
Output Dividers		6 to 36		mA	Each output divide-by-2 consumes 6 mA
I_{VCO}[2]		70	80	mA	
I_{RFOUT}[2]		21	26	mA	RF output stage is programmable
Low Power Sleep Mode		7	10	µA	
RF OUTPUT CHARACTERISTICS					
VCO Output Frequency	2200		4400	MHz	Fundamental VCO mode
Minimum VCO Output Frequency Using Dividers	34.375			MHz	2200 MHz fundamental output and divide-by-64 selected
VCO Sensitivity, K_V		40		MHz/V	
Frequency Pushing (Open-Loop)		1		MHz/V	
Frequency Pulling (Open-Loop)		90		kHz	Into 2.00 VSWR load
Harmonic Content (Second)		−19		dBc	Fundamental VCO output
		−20		dBc	Divided VCO output
Harmonic Content (Third)		−13		dBc	Fundamental VCO output
		−10		dBc	Divided VCO output

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum RF Output Power[3]		−4		dBm	Programmable in 3 dB steps
Maximum RF Output Power[3]		5		dBm	
Output Power Variation		±1		dB	
Minimum VCO Tuning Voltage		0.5		V	
Maximum VCO Tuning Voltage		2.5		V	
NOISE CHARACTERISTICS					
VCO Phase Noise Performance					VCO noise is measured in open-loop conditions
		−89		dBc/Hz	10 kHz offset from 2.2 GHz carrier
		−114		dBc/Hz	100 kHz offset from 2.2 GHz carrier
		−134		dBc/Hz	1 MHz offset from 2.2 GHz carrier
		−148		dBc/Hz	5 MHz offset from 2.2 GHz carrier
		−86		dBc/Hz	10 kHz offset from 3.3 GHz carrier
		−111		dBc/Hz	100 kHz offset from 3.3 GHz carrier
		−134		dBc/Hz	1 MHz offset from 3.3 GHz carrier
		−145		dBc/Hz	5 MHz offset from 3.3 GHz carrier
		−83		dBc/Hz	10 kHz offset from 4.4 GHz carrier
		−110		dBc/Hz	100 kHz offset from 4.4 GHz carrier
		−131		dBc/Hz	1 MHz offset from 4.4 GHz carrier
		−145		dBc/Hz	5 MHz offset from 4.4 GHz carrier
Normalized Phase Noise Floor (PN_{SYNTH})[4]					PLL loop BW = 500 kHz
		−220		dBc/Hz	ABP = 6 ns
		−221		dBc/Hz	ABP = 3 ns
Normalized 1/f Noise (PN_{1_f})[5]					10 kHz offset; normalized to 1 GHz
		−116		dBc/Hz	ABP = 6 ns
		−118		dBc/Hz	ABP = 3 ns
In-Band Phase Noise		−100		dBc/Hz	3 kHz from 2111.28 MHz carrier
Integrated RMS Jitter[6]		0.27		ps	
Spurious Signals Due to PFD Frequency		−80		dBc	
Level of Signal with RF Mute Enabled		−40		dBm	

[1] I_{CP} is internally modified to maintain constant loop gain over the frequency range.
[2] T_A = 25°C; AV_{DD} = DV_{DD} = V_{VCO} = 3.3 V; prescaler = 8/9; f_{REFIN} = 100 MHz; f_{PFD} = 25 MHz; f_{RF} = 4.4 GHz.
[3] Using 50 Ω resistors to V_{VCO}, into a 50 Ω load. Power measured with auxiliary RF output disabled. The current consumption of the auxiliary output is the same as for the main output.
[4] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log f_{PFD}. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: $PN_{SYNTH} = PN_{TOT} - 10\log(f_{PFD}) - 20\log N$.
[5] The PLL phase noise is composed of flicker (1/f) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at a frequency offset (f) is given by $PN = PN_{1\_f} + 10\log(10\text{ kHz}/f) + 20\log(f_{RF}/1\text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[6] f_{REFIN} = 122.88 MHz; f_{PFD} = 30.72 MHz; VCO frequency = 4222.56 MHz; RF_{OUT} = 2111.28 MHz; N = 137; loop BW = 60 kHz; I_{CP} = 2.5 mA; low noise mode. The noise was measured with an EVAL-ADF4351EB1Z and the Rohde & Schwarz FSUP signal source analyzer.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = V_{VCO} = SDV_{DD} = V_P = 3.3 V ± 10%; AGND = DGND = 0 V; 1.8 V and 3 V logic levels used; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit	Unit	Description
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

Timing Diagram

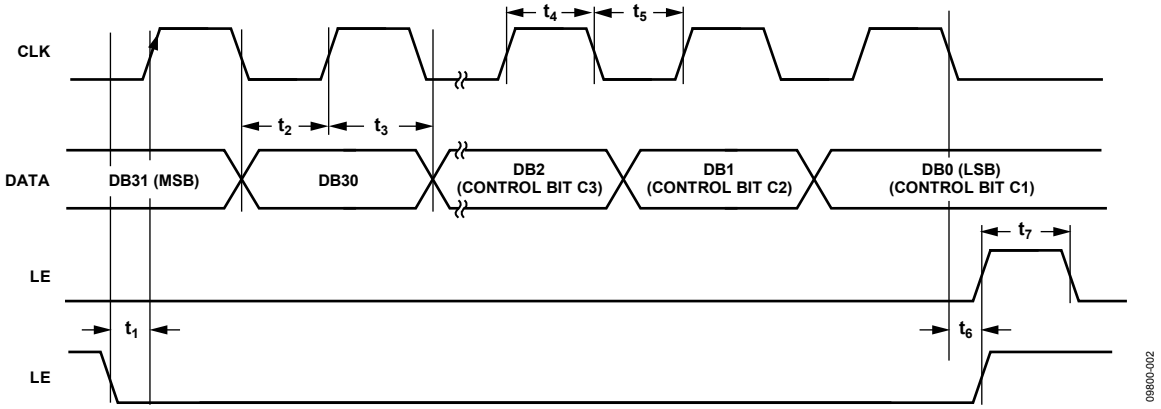

Figure 2. Timing Diagram