MCP4902/4912/4922

8/10/12-Bit Dual Voltage Output Digital-to-Analog Converter with SPI Interface

Features

- MCP4902: Dual 8-Bit Voltage Output DAC
- MCP4912: Dual 10-Bit Voltage Output DAC
- MCP4922: Dual 12-Bit Voltage Output DAC
- Rail-to-Rail Output
- SPI Interface with 20 MHz Clock Support
- Simultaneous Latching of the Dual DACs with $\overline{\text{LDAC}}$ pin
- Fast Settling Time of 4.5 µs
- Selectable Unity or 2x Gain Output
- External Voltage Reference Inputs
- External Multiplier Mode
- 2.7V to 5.5V Single-Supply Operation
- Extended Temperature Range: -40°C to +125°C

Applications

- Set Point or Offset Trimming
- Precision Selectable Voltage Reference
- Motor Control Feedback Loop
- Digitally-Controlled Multiplier/Divider
- Calibration of Optical Communication Devices

Related Products(1)

P/N	DAC Resolution	No. of ChannelS	Voltage Reference (V_{REF})
MCP4801	8	1	Internal (2.048V)
MCP4811	10	1	
MCP4821	12	1	
MCP4802	8	2	
MCP4812	10	2	
MCP4822	12	2	
MCP4901	8	1	External
MCP4911	10	1	
MCP4921	12	1	
MCP4902	**8**	**2**	
MCP4912	**10**	**2**	
MCP4922	**12**	**2**	

Note 1: The products listed here have similar AC/DC performances.

Description

The MCP4902/4912/4922 devices are dual 8-bit, 10-bit, and 12-bit buffered voltage output Digital-to-Analog Converters (DACs), respectively. The devices operate from a single 2.7V to 5.5V supply with SPI compatible Serial Peripheral Interface. The user can configure the full-scale range of the device to be V_{REF} or 2 * V_{REF} by setting the Gain Selection Option bit (gain of 1 of 2).

The user can shut down both DAC channels by using $\overline{\text{SHDN}}$ pin or shut down the DAC channel individually by setting the Configuration register bits. In Shutdown mode, most of the internal circuits in the shutdown channel are turned off for power savings and the output amplifier is configured to present a known high resistance output load (500 kΩ, typical).

The devices include double-buffered registers, allowing synchronous updates of two DAC outputs, using the $\overline{\text{LDAC}}$ pin. These devices also incorporate a Power-on Reset (POR) circuit to ensure reliable power-up.

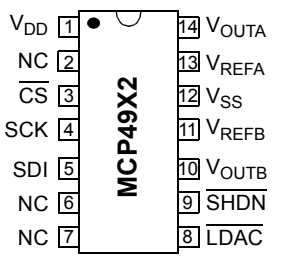
The devices utilize a resistive string architecture, with its inherent advantages of low DNL error and fast settling time. These devices are specified over the extended temperature range (+125°C).

The devices provide high accuracy and low noise performance for consumer and industrial applications where calibration or compensation of signals (such as temperature, pressure and humidity) are required.

The MCP4902/4912/4922 devices are available in the PDIP, SOIC and TSSOP packages.

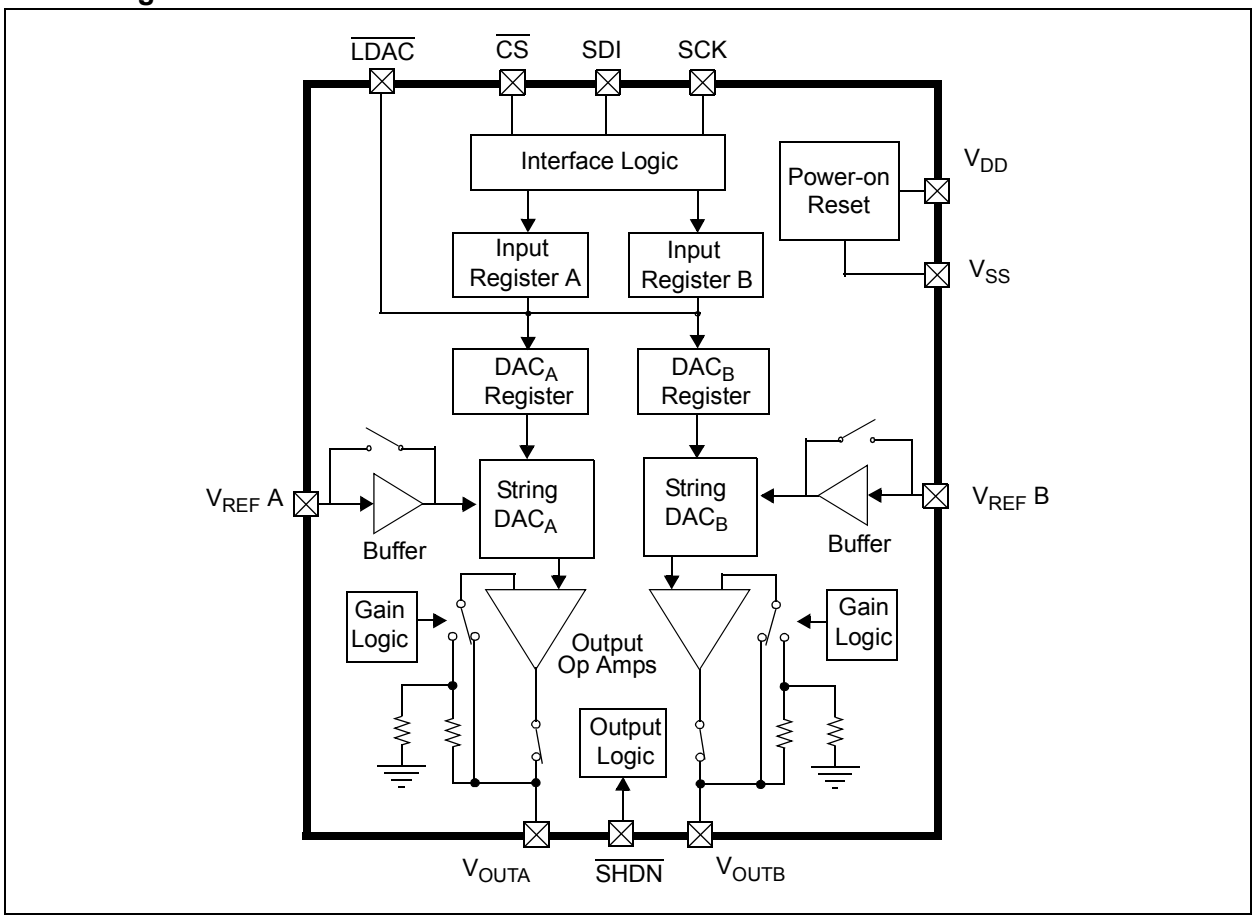
Package Types

14-Pin PDIP, SOIC, TSSOP



MCP4902: 8-bit dual DAC
MCP4912: 10-bit dual DAC
MCP4922: 12-bit dual DAC

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD}..... 6.5V
All inputs and outputs w.r.t ..... V_{SS} –0.3V to V_{DD}+0.3V
Current at Input Pins ..... ±2 mA
Current at Supply Pins ..... ±50 mA
Current at Output Pins ..... ±25 mA
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -55°C to +125°C
ESD protection on all pins ≥ 4 kV (HBM), ≥ 400V (MM)
Maximum Junction Temperature (T_J).....+150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF T_A = -40 to +85°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Operating Current	I_{DD}	—	350	700	µA	V_{DD} = 5V
		—	250	500	µA	V_{DD} = 3V V_{REF} input is unbuffered, all digital inputs are grounded, all analog outputs (V_{OUT}) are unloaded. Code = 000h.
Hardware Shutdown Current	I_{SHDN}	—	0.3	2	µA	Power-on Reset circuit is turned off
Software Shutdown Current	I_{SHDN_SW}	—	3.3	6	µA	Power-on Reset circuit stays on
Power-on-Reset Threshold	V_{POR}	—	2.0	—	V	
DC Accuracy						
MCP4902						
Resolution	n	8	—	—	Bits	
INL Error	INL	-1	±0.125	1	LSb	
DNL	DNL	-0.5	±0.1	+0.5	LSb	**Note 1**
MCP4912						
Resolution	n	10	—	—	Bits	
INL Error	INL	-3.5	±0.5	3.5	LSb	
DNL	DNL	-0.5	±0.1	+0.5	LSb	**Note 1**
MCP4922						
Resolution	n	12	—	—	Bits	
INL Error	INL	-12	±2	12	LSb	
DNL	DNL	-0.75	±0.2	+0.75	LSb	**Note 1**
Offset Error	V_{OS}	—	±0.02	1	% of FSR	Code = 0x000h

Note 1: Guaranteed monotonic by design over all codes.
2: This parameter is ensured by design, and not 100% tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF T_A = -40 to +85°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Offset Error Temperature Coefficient	V_{OS}/°C	—	0.16	—	ppm/°C	-45°C to 25°C
		—	-0.44	—	ppm/°C	+25°C to 85°C
Gain Error	g_E	—	-0.10	1	% of FSR	Code = 0xFFFh, not including offset error
Gain Error Temperature Coefficient	ΔG/°C	—	-3	—	ppm/°C	
Input Amplifier (V_{REF} Input)						
Input Range – Buffered Mode	V_{REF}	0.040	—	V_{DD} – 0.040	V	**Note 2** Code = 2048 V_{REF} = 0.2V p-p, f = 100 Hz and 1 kHz
Input Range – Unbuffered Mode	V_{REF}	0	—	V_{DD}	V	
Input Impedance	R_{VREF}	—	165	—	kΩ	Unbuffered Mode
Input Capacitance – Unbuffered Mode	C_{VREF}	—	7	—	pF	
Multiplier Mode -3 dB Bandwidth	f_{VREF}	—	450	—	kHz	V_{REF} = 2.5V ±0.2Vp-p, Unbuffered, G = 1x
	f_{VREF}	—	400	—	kHz	V_{REF} = 2.5V ±0.2 Vp-p, Unbuffered, G = 2x
Multiplier Mode – Total Harmonic Distortion	THD_{VREF}	—	-73	—	dB	V_{REF} = 2.5V ±0.2Vp-p, Frequency = 1 kHz
Output Amplifier						
Output Swing	V_{OUT}	—	0.01 to V_{DD} – 0.04	—	V	Accuracy is better than 1 LSb for V_{OUT} = 10 mV to (V_{DD} – 40 mV)
Phase Margin	θm	—	66	—	degrees	
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	15	24	mA	
Settling Time	$t_{settling}$	—	4.5	—	µs	Within 1/2 LSb of final value from 1/4 to 3/4 full-scale range
Dynamic Performance (Note 2)						
DAC-to-DAC Crosstalk		—	10	—	nV-s	
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (0111...1111 to 1000...0000)
Digital Feedthrough		—	10	—	nV-s	
Analog Crosstalk		—	10	—	nV-s	

Note 1: Guaranteed monotonic by design over all codes.

2: This parameter is ensured by design, and not 100% tested.

ELECTRICAL CHARACTERISTIC WITH EXTENDED TEMPERATURE

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF. Typical values are at +125°C by characterization or simulation.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Requirements						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Operating Current	I_{DD}	—	400	—	µA	V_{REF} input is unbuffered, all digital inputs are grounded, all analog outputs (VOUT) are unloaded. Code=000h
Hardware Shutdown Current	I_{SHDN}	—	1.5	—	µA	POR circuit is turned-off
Software Shutdown Current	I_{SHDN_SW}	—	5	—	µA	POR circuit stays turned-on
Power-On Reset threshold	V_{POR}	—	1.85	—	V	
DC Accuracy						
MCP4902						
Resolution	n	8	—	—	Bits	
INL Error	INL		±0.25		LSb	
DNL	DNL		±0.2		LSb	**Note 1**
MCP4912						
Resolution	n	10	—	—	Bits	
INL Error	INL		±1		LSb	
DNL	DNL		±0.2		LSb	**Note 1**
MCP4922						
Resolution	n	12	—	—	Bits	
INL Error	INL		±4		LSb	
DNL	DNL		±0.25		LSb	**Note 1**
Offset Error	V_{OS}	—	±0.02	—	% of FSR	Code 0x000h
Offset Error Temperature Coefficient	V_{OS}/°C	—	-5	—	ppm/°C	+25°C to +125°C
Gain Error	g_E	—	-0.10	—	% of FSR	Code = 0xFFFh, not including offset error
Gain Error Temperature Coefficient	ΔG/°C	—	-3	—	ppm/°C	
Input Amplifier (V_{REF} Input)						
Input Range – Buffered Mode	V_{REF}	—	0.040 to V_{DD} – 0.040	—	V	**Note 1** Code = 2048, V_{REF} = 0.2V p-p, f = 100 Hz and 1 kHz
Input Range – Unbuffered Mode	V_{REF}	0	—	V_{DD}	V	
Input Impedance	R_{VREF}	—	174	—	kΩ	Unbuffered mode
Input Capacitance – Unbuffered Mode	C_{VREF}	—	7	—	pF	

Note 1: Guaranteed monotonic by design over all codes.

2: This parameter is ensured by design, and not 100% tested.

ELECTRICAL CHARACTERISTIC WITH EXTENDED TEMPERATURE (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 2.048V, Output Buffer Gain (G) = 2x, R_L = 5 kΩ to GND, C_L = 100 pF. Typical values are at +125°C by characterization or simulation.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Multiplying Mode -3 dB Bandwidth	f_{VREF}	—	450	—	kHz	V_{REF} = 2.5V ±0.1 Vp-p, Unbuffered, G = 1x
	f_{VREF}	—	400	—	kHz	V_{REF} = 2.5V ±0.1 Vp-p, Unbuffered, G = 2x
Multiplying Mode – Total Harmonic Distortion	THD_{VREF}	—	—	—	dB	V_{REF} = 2.5V ±0.1Vp-p, Frequency = 1 kHz
Output Amplifier						
Output Swing	V_{OUT}	—	0.01 to V_{DD} – 0.04	—	V	Accuracy is better than 1 LSb for V_{OUT} = 10 mV to (V_{DD} – 40 mV)
Phase Margin	θm	—	66	—	degrees	
Slew Rate	SR	—	0.55	—	V/µs	
Short Circuit Current	I_{SC}	—	17	—	mA	
Settling Time	$t_{settling}$	—	4.5	—	µs	Within 1/2 LSb of final value from 1/4 to 3/4 full-scale range
Dynamic Performance (Note 2)						
DAC to DAC Crosstalk		—	10	—	nV-s	
Major Code Transition Glitch		—	45	—	nV-s	1 LSb change around major carry (`0111...1111` to `1000...0000`)
Digital Feedthrough		—	10	—	nV-s	
Analog Crosstalk		—	10	—	nV-s	

Note 1: Guaranteed monotonic by design over all codes.

2: This parameter is ensured by design, and not 100% tested.

AC CHARACTERISTICS (SPI TIMING SPECIFICATIONS)

Electrical Specifications: Unless otherwise indicated, V_{DD}= 2.7V – 5.5V, T_A= -40 to +125°C. Typical values are at +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Schmitt Trigger High-Level Input Voltage (All digital input pins)	V_{IH}	0.7 V_{DD}	—	—	V	
Schmitt Trigger Low-Level Input Voltage (All digital input pins)	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.05 V_{DD}	—	V	
Input Leakage Current	$I_{LEAKAGE}$	-1	—	1	µA	$\overline{SHDN}$ = $\overline{LDAC}$ = $\overline{CS}$ = SDI = SCK + V_{REF} = V_{DD} or V_{SS}
Digital Pin Capacitance (All inputs/outputs)	C_{IN}, C_{OUT}	—	10	—	pF	V_{DD} = 5.0V, T_A = +25°C, f_{CLK} = 1 MHz **(Note 1)**
Clock Frequency	F_{CLK}	—	—	20	MHz	T_A = +25°C **(Note 1)**
Clock High Time	t_{HI}	15	—	—	ns	**Note 1**
Clock Low Time	t_{LO}	15	—	—	ns	**Note 1**
$\overline{CS}$ Fall to First Rising CLK Edge	t_{CSSR}	40	—	—	ns	Applies only when $\overline{CS}$ falls with CLK high. **(Note 1)**
Data Input Setup Time	t_{SU}	15	—	—	ns	**Note 1**
Data Input Hold Time	t_{HD}	10	—	—	ns	**Note 1**
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	15	—	—	ns	**Note 1**
$\overline{CS}$ High Time	t_{CSH}	15	—	—	ns	**Note 1**
$\overline{LDAC}$ Pulse Width	t_{LD}	100	—	—	ns	**Note 1**
$\overline{LDAC}$ Setup Time	t_{LS}	40	—	—	ns	**Note 1**
SCK Idle Time before $\overline{CS}$ Fall	t_{IDLE}	40	—	—	ns	**Note 1**

Note 1: This parameter is ensured by design and not 100% tested.

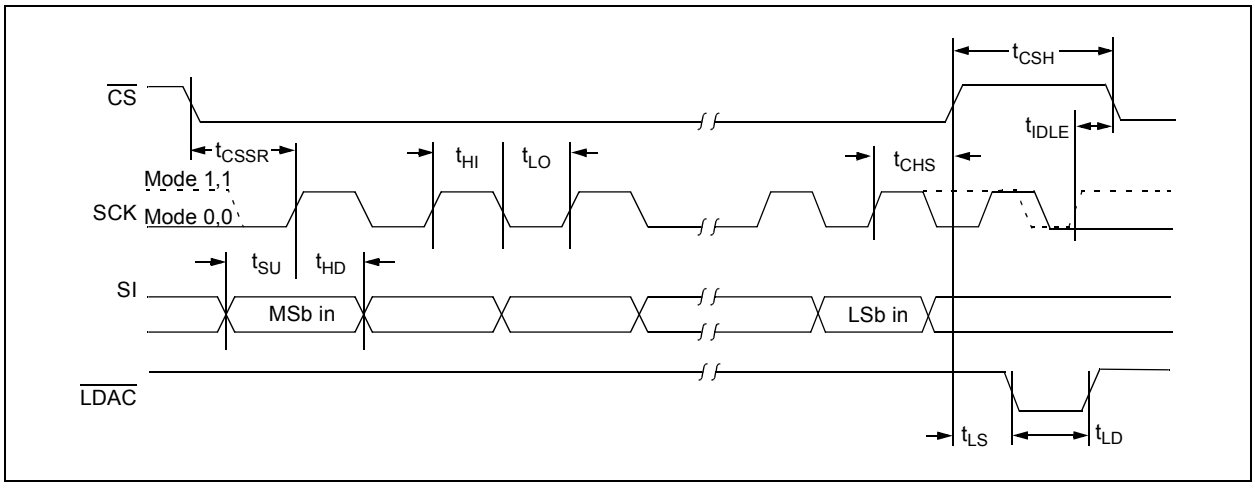


FIGURE 1-1: *SPI Input Timing Data.*

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP4902/4912/4922 devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the maximum junction temperature of 150°C.