|  |  |  |  |
| --- | --- | --- | --- |
| Port A | Pin | MUX | oliExt |
| A0 | PH0 | 0 | pinPortA[0] |
| A1 | PH2 | 0 | pinPortA[1] |
| A2 | PH7 | 0 | pinPortA[2] |
| A3 | PH9 | 0 | pinPortA[3] |
| A4 | PH10 | 0 | pinPortA[4] |
| A5 | PH11 | 0 | pinPortA[5] |
| A6 | PH12 | 0 | pinPortA[6] |
| A7 | PH13 | 0 | pinPortA[7] |
| A8 | PH14 | 0 | pinPortA[8] |
| A9 | PH15 | 0 | pinPortA[9] |
| A10 | PH16 | 0 | pinPortA[10] |
| A11 | PH17 | 0 | pinPortA[11] |
| A12 | PH18 | 0 | pinPortA[12] |
| A13 | PH19 | 0 | pinPortA[13] |
| A14 | PH20 | 0 | pinPortA[14] |
| A15 | PH21 | 0 | pinPortA[15] |

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| Port B | Pin | MUX | oliExt |
| B0 | PB3 | 0 | pinPortB[0] |
| B1 | PB4 | 0 | pinPortB[1] |
| B2 | PB5 | 0 | pinPortB[2] |
| B3 | PB6 | 0 | pinPortB[3] |
| B4 | PB7 | 0 | pinPortB[4] |
| B5 | PB8 | 0 | pinPortB[5] |
| B6 | PB10 | 0 | pinPortB[6] |
| B7 | PB11 | 0 | pinPortB[7] |
| B8 | PB12 | 0 | pinPortB[8] |
| B9 | PB13 | 0 | pinPortB[9] |
| B10 | PB14 | 0 | pinPortB[10] |
| B11 | PB15 | 0 | pinPortB[11] |
| B12 | PB16 | 0 | pinPortB[12] |
| B13 | PB17 | 0 | pinPortB[13] |
| B14 | PH22 | 0 | pinPortB[14] |
| B15 | PH23 | 0 | pinPortB[15] |

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| Port C | Pin | MUX | oliExt |
| C0 | PH24 | 0 | pinPortC[0] |
| C1 | PH25 | 0 | pinPortC[1] |
| C2 | PH26 | 0 | pinPortC[2] |
| C3 | PH27 | 0 | pinPortC[3] |
| C4 | PE0 | 0 | pinPortC[4] |
| C5 | PE1 | 0 | pinPortC[5] |
| C6 | PE2 | 0 | pinPortC[6] |
| C7 | PE3 | 0 | pinPortC[7] |

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| Port D | Pin | MUX | oliExt |
| D0 | PE4 | 0 | pinPortD[0] |
| D1 | PE5 | 0 | pinPortD[1] |
| D2 | PE6 | 0 | pinPortD[2] |
| D3 | PE7 | 0 | pinPortD[3] |
| D4 | PE8 | 0 | pinPortD[4] |
| D5 | PE9 | 0 | pinPortD[5] |
| D6 | PE10 | 0 | pinPortD[6] |
| D7 | PE11 | 0 | pinPortD[7] |

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| Port General | Pin | MUX | oliExt |
| G0 | PI14 | 0 | pinPortGeneral[0] |
| G1 | PI15 | 0 | pinPortGeneral[1] |

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| --- | --- | --- | --- |
| Display 7 Segments | Pin | MUX | oliExt |
| A | PG0 | 0 | pinDisplay[0] |
| B | PG1 | 0 | pinDisplay[1] |
| C | PG2 | 0 | pinDisplay[2] |
| D | PG3 | 0 | pinDisplay[3] |
| E | PG4 | 0 | pinDisplay[4] |
| F | PG5 | 0 | pinDisplay[5] |
| G | PI0 | 0 | pinDisplay[6] |
| Dot | PI1 | 0 | pinDisplay[7] |

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| SIM900 | Pin | MUX | oliExt |
| Reset | PC3 | 0 | pinSIM900[0] |
| LED | PC7 | 0 | pinSIM900[1] |
| On/Off | PC16 | 0 | pinSIM900[4] |
| RI | PI11 | 0 | pinSIM900[3] |
| RX | RX6 |  | ttyS4 |
| TX | TX6 |  | ttyS4 |

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| --- | --- | --- | --- |
| COM1 | Pin | MUX | oliExt |
| RX | RX2 | 3 | ttyS1 |
| TX | TX2 | 3 | ttyS1 |
| RTS | RTS2 | 3 | ttyS1 |
| CTS | CTS2 | 3 | ttyS1 |

|  |  |  |  |
| --- | --- | --- | --- |
| COM2 | Pin | MUX | oliExt |
| RX | RX3 | 4 | ttyS2 |
| TX | TX3 | 4 | ttyS2 |
| RTS | RTS3 | 4 | ttyS2 |
| CTS | CTS3 | 4 | ttyS2 |

Description of the GPIO configuration in the form:

port:<port><mux feature><pullup/down><drive capability><output level>

where:

**<port>** is the port to configure (ie. PH15)

**<mux feature>** is the function to configure the port for, mux 0 is as input, mux 1 as output and for 2-7 see [A10/PIO](http://linux-sunxi.org/A10/PIO), [A13/PIO](http://linux-sunxi.org/A13/PIO), or [A20/PIO](http://linux-sunxi.org/A20/PIO) for details.

**<pullup/down>** is 0 = disabled; 1 = pullup enabled; 2 = pulldown enabled (only valid when port is an input)

**<drive capability>** defines the output drive in mA, values are 0-3 corresponding to 10mA, 20mA, 30mA and 40mA.

**<output level>** sets the initial output level for the port; 0 = low; 1 = high (only valid for outputs)