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## **PolarFire® FPGA PCIe EndPoint DDR3L DDR4 Memory Controller Data Plane**

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### **Introduction**

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Microchip PolarFire® FPGAs contain fully integrated PCIe EndPoint and Root Port subsystems with optimized embedded controller blocks that use the Physical Layer Interface (PHY) of the transceiver. Each PolarFire device includes two embedded PCIe Subsystem (PCIESS) blocks that can be configured either separately or as a pair, using the PCIESS configurator in the Libero® SoC software.

The PCIESS is compliant with the PCI Express Base Specification, Revision 3.0 with Gen1/2 speed. It implements memory-mapped Advanced Microcontroller Bus Architecture (AMBA), and Advanced eXtensible Interface 4 (AXI4) access to the PCIe space and the PCIe access to the memory-mapped AXI4 space. For more information, see [PolarFire FPGA and PolarFire SoC FPGA PCI Express User Guide](#).

The DDR subsystem addresses memory solution requirements for a wide range of applications with varying power consumption and efficiency levels. The subsystem can be configured to support DDR4, DDR3, DDR3L, and LPDDR3 memory devices. The subsystem is intended for accessing DDR memories for applications that require high-speed data transfers and code execution. For more information about DDR memory controller, see [PolarFire FPGA and PolarFire SoC FPGA Memory Controller User Guide](#).

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## 1. PolarFire FPGA PCIe EndPoint, DDR3L, and DDR4 Memory Controller Data Plane

This document explains how to use the accompanying reference design to demonstrate the high-speed data transfer capability of the PolarFire FPGA using the hardened PCIe EndPoint, Soft DDR3L, and DDR4 controller IP. The PCIe controller, built-in Direct Memory Access (DMA) controller, and the CoreAXI4DMAController IP are used to achieve high-speed, bulk data transfers, as follows:

- The PCIe controller's built-in DMA controller performs bulk-data transfer between contiguous/scatter gather memory locations on a host PC and contiguous memory locations of DDR3L/DDR4/LSRAM.
- The CoreAXI4DMAController performs data transfers between DDR3L/DDR4 memory and LSRAM using the CoreAXI4DMA controller.

The demo also shows how to use pre-synthesized design simulations using PCIe BFM script to initiate the PCIe EndPoint DMA to perform data transfers between LSRAM, DDR3L, DDR4, and PCIe.

The Windows® kernel-mode PCIe device driver, developed using the Windows Driver Kit (WDK) platform, interacts with the PolarFire PCIe EndPoint from the host PC. A Graphic User Interface (GUI) application that runs on the host PC is provided to set up and initiate the DMA transactions between the host PC memory, DDR3L, DDR4, and the LSRAM memories of the PolarFire Evaluation/Splash kit through the PCIe interface.

A user application interface is provided for the GUI to interact with the PCIe driver. The GUI can also initiate the DMA transactions between DDR3L/DDR4 and LSRAM through UART IF. If the host PC PCIe slot is not available, the DMA between DDR3L/DDR4 and LSRAM is exercised through UART IF.

The PCIe EndPoint reference design can be programmed using any of the following options:

- Using the job file: To program the device using the job file provided along with the design files, see [6. Appendix 3: Programming the Device Using FlashPro Express](#).
- Using Libero SoC: To program the device using Libero SoC, see [2. Libero Design Flow](#). Use this option when the reference design is modified.



**Important:** The user can debug the PCIe features: PCIe lane status, LTSSM state machine, and other available PCIe features using SmartDebug. For more information about PCIE Debug using SmartDebug, see [SmartDebug User Guide](#).

### 1.1 Design Requirements

The following table lists the hardware, software, and IP requirements for this demo design.

**Table 1-1. Design Requirements**

Requirement	Version
Operating system	64-bit Windows® 10 Linux® CentOS Kernel version 3.10.0
<b>Hardware</b>	
PolarFire® Evaluation Kit (MPF300TS-FCG1152I) or PolarFire Splash Kit (MPF300T-1FCG484)	Rev D or later Rev 2 or later
PCIe Edge card ribbon cable (not provided with the kit)	—
Host PC with PCIe compliant slot with x4 or higher width	—

.....continued

Requirement	Version
<b>Software</b>	
Libero® SoC	See the <code>readme.txt</code> file provided in the design files for the software versions used with this reference design.
Modelsim®	
Synplify Pro®	



**Important:** Libero SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

## 1.2 Prerequisites

Before you begin, perform the following steps:

1. For demo design files, download the link:  
[www.microchip.com/en-us/application-notes/AN4597](http://www.microchip.com/en-us/application-notes/AN4597)
2. Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location:  
[Libero SoC Documentation](#)

The latest versions of ModelSim, Synplify Pro, and FTDI drivers are included in the Libero SoC installation package.

## 1.3 Demo Design

Figure 1-1 shows the top-level block diagram of the PCIe EndPoint demo design. Any external PCIe root-port or bridge can establish a PCIe link with the PolarFire FPGA PCIe EndPoint and access the control registers, DDR3L, DDR4, and fabric memory through BAR space using the Memory Write (MWr) and Memory Read (MRd) transaction layer packets (TLPs). The PCIe EndPoint converts these MWr and MRd TLPs into AXI4 initiator interface transactions and accesses the fabric memory through CoreAXI4Interconnect IP.

The PCIe Demo application on the host PC initiates the DMA transfers through the PCIe device drivers. The driver on the host PC allocates memory and initiates the DMA Engine in the PolarFire PCIe controller by accessing the PCIe DMA registers through BAR0. The PCIe controller has the following two independent DMA Engines:

- DMA Engine0: Performs DMA from host PC memory to DDR3L/DDR4/LSRAM.
- DMA Engine1: Performs DMA from DDR3L/DDR4/LSRAM to host PC memory.



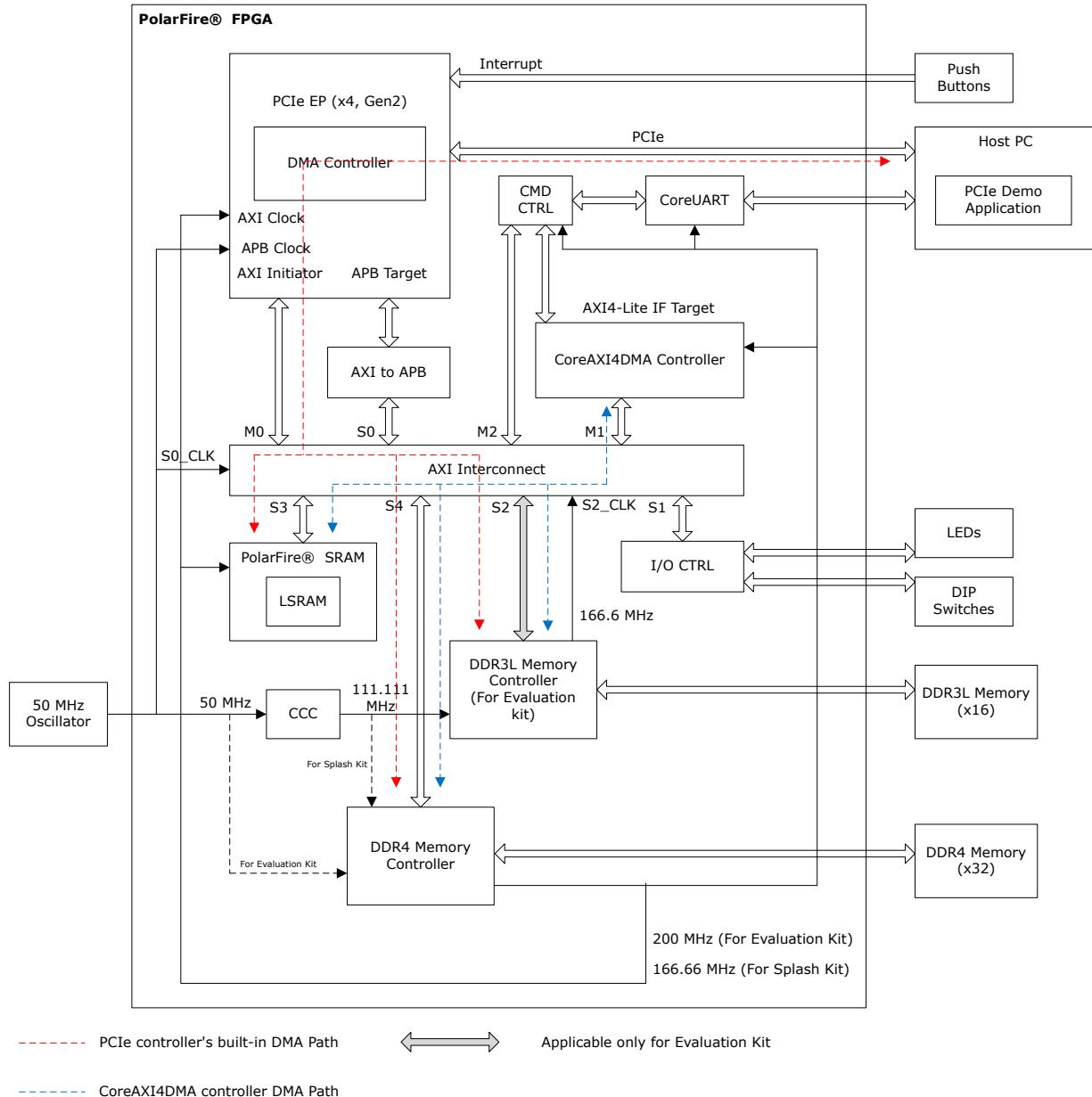
**Important:** For SGDMA type of DMA operations, the PCIe driver finds the available memory locations and creates the buffer descriptor chain for the different memory locations. It also configures the PCIe DMA for SGDMA and the base address of the first buffer descriptor.

The PCIe demo application initiates CoreAXI4DMA controller IP to perform the DMA between DDR3L memory and LSRAm. The following are the two channels of the CoreAXI4DMA controller IP:

- Channel0: Performs DMA from—DDR3L to DDR4, DDR3L to LSRAm, and DDR4 to LSRAm
- Channel1: Performs DMA from—DDR4 to DDR3L, LSRAm to DDR3L, and LSRAm to DDR4

The host PC application initiates the CoreAXI4DMA controller IP depending on the DMA type through BAR2 when the PCIe edge connector is connected to the host PC PCIe slot. The host PC application also initiates the CoreAXI4DMA controller IP through UART IF. This option is provided to exercise the DDR throughputs when the PolarFire Evaluation/Splash kit is not connected to the host PC PCIe slot.

Figure 1-1. PCIe Demo Design Top-Level Block Diagram



### 1.3.1 Design Data Flow

The demo design performs the following control plane operations:

- LED Blink: Host PC driver performs BAR2 MWr operation to EndPoint. The PCIe controller generates AXI write transaction on AXI\_IO\_CTRL logic's to blink LEDs.
- DIP Switch Read: Host PC driver performs BAR2 MRd to EndPoint. The PCIe controller generates AXI read transaction on AXI\_IO\_CTRL logic's to blink LEDs.
- MSI Interrupt Count: When on-board push button is pressed, the PCIe EndPoint generates interrupt to host PC and the host PC driver increments the corresponding interrupt counter.
- Memory Read/Write: Host PC driver configures the ATR2 translation address to DDR3L/DDR4/LSRAM base address. It performs BAR2 memory read/write transactions to DDR3L/DDR4/LSRAM memories.

The demo design supports the following types of DMA operations.

- Continuous DMA operations
- SGDMA Operations
- Core DMA Operations

### 1.3.1.1 Continuous DMA Operations

The PCIe DMA0/DMA1 controllers perform DMA between continuous memory locations when SGDMA mode is disabled. The following sections explain the data flow of DMA0 and DMA1.

#### 1.3.1.1.1 DMA0—Host PC Memory to DDR3L/DDR4/LSRAM

PCIe DMA Engine0 performs continuous DMA from host PC memory to DDR3L/DDR4/LSRAM memories as described in the following steps:

1. The PolarFire\_Pcie\_GUI application sets the DMA controller through the PCIe link. This includes DMA source and destination, address, and size.
2. DMA controller initiates a read transaction to the PCIe core.
3. The PCIe core sends the MRd TLP to the host PC.
4. The host PC returns a completion (CpID) TLP to the PCIe link.
5. This returned data is written to the DDR3L/DDR4/LSRAM memories using PCIe AXI initiator interface.
6. The DMA controller repeats this process (from steps 2 to 5) until the DMA size of data transfer is completed.
7. The DMA controller sends the MSI0 interrupt to the host PC, the driver on the host PC detects the interrupt, reads the DMA status, and the number of clock cycles consumed to complete the DMA transaction to the PolarFire\_Pcie\_GUI application.

#### 1.3.1.1.2 DMA1—DDR3L/DDR4/LSRAM to Host PC Memory

PCIe DMA Engine1 performs continuous DMA from DDR3L/DDR4/LSRAM memories to host PC memory as described in the following steps:

1. PolarFire\_Pcie\_GUI application sets up the DMA controller through the PCIe link. This includes DMA source and destination, address, and size.
2. DMA controller initiates an AXI burst read transaction to read the data from DDR3L/DDR4/LSRAM memories.
3. The DMA controller initiates write transaction to PCIe core with the read data. The PCIe core sends a MWr TLP to the host PC.
4. The DMA controller repeats this process (steps 2 and 3) until the DMA size of data transfer is completed.
5. The DMA controller sends the MSI1 interrupt to the host PC. The driver on the host PC detects the interrupt, reads the DMA status, and the number of clock cycles consumed to complete the DMA transaction to the PolarFire\_Pcie\_GUI application.

### 1.3.1.2 SGDMA Operations

The PCIe DMA0/DMA1 performs DMA between scattered host PC memory locations and continuous memories of PolarFire when SGDMA mode is enabled.

#### 1.3.1.2.1 Host PC Memory to DDR3L/DDR4

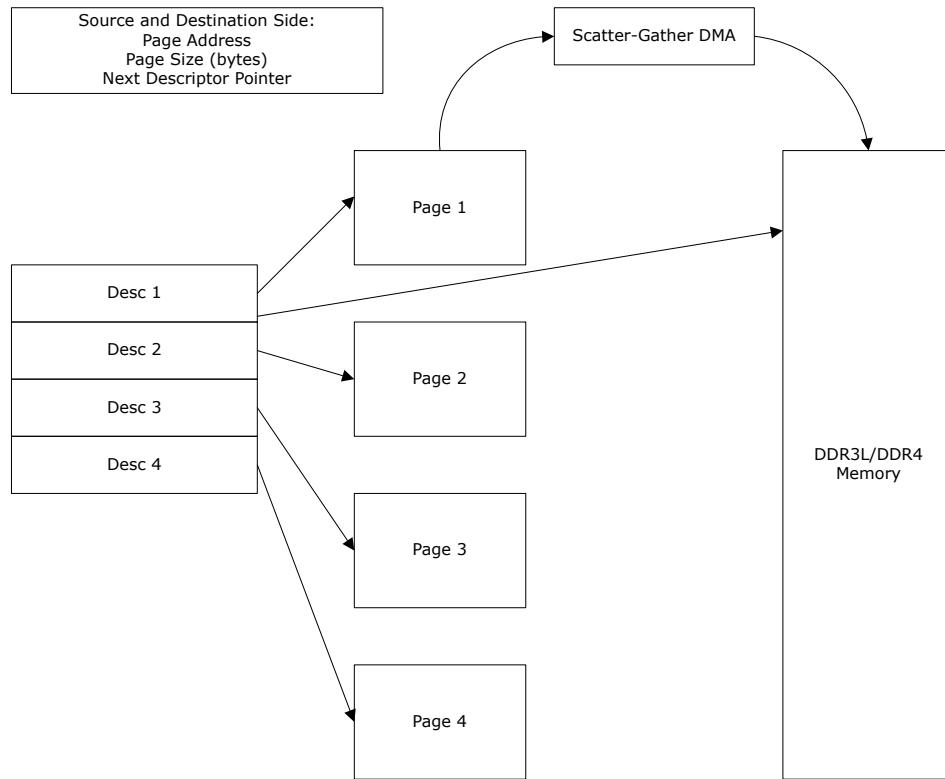
PCIe DMA Engine0 performs DMA from host PC memory to DDR3L/DDR4 memories as shown in the following figure.

The following steps describe the SGDMA operation of PCIe DMA0:

1. PolarFire\_Pcie\_GUI application requests the PCIe driver for SG DMA. The driver on the host PC allocates the available memory location and creates the buffer descriptors with the scattered memory location addresses and location size.
2. The destination DDR3L/DDR4 memory is treated as the continuous memory. The driver configures the PCIe DMA0 with the first buffer descriptor address and initiates the DMA.
3. DMA controller initiates read transaction to the PCIe core with the buffer descriptor address.
4. The PCIe core sends the MRd TLP to the host PC. The host PC returns a completion (CpID) TLP to the PCIe link.
5. The DMA controller extracts these buffer descriptors and initiates the read transaction to PCIe core with the host PC memory location address in the descriptor.

6. The PCIe core sends the MRd TLP to the host PC. The host PC returns a CplD TLP to the PCIe link.
7. This return data is written to the DDR3L/DDR4 memories using PCIe AXI initiator interface.
8. The DMA controller repeats this process (from steps 3 to 7) until the DMA size of data transfer is completed.
9. The DMA controller sends the MSI0 interrupt to the host PC. The driver on the host PC detects the interrupt, reads the DMA status, and the number of clock cycles consumed to complete the DMA transaction to the PolarFire\_Pcie\_GUI application.

**Figure 1-2. DMA0—Example of SG DMA Operation**



#### 1.3.1.2.2 DDR3L/DDR4 to Host PC Memory

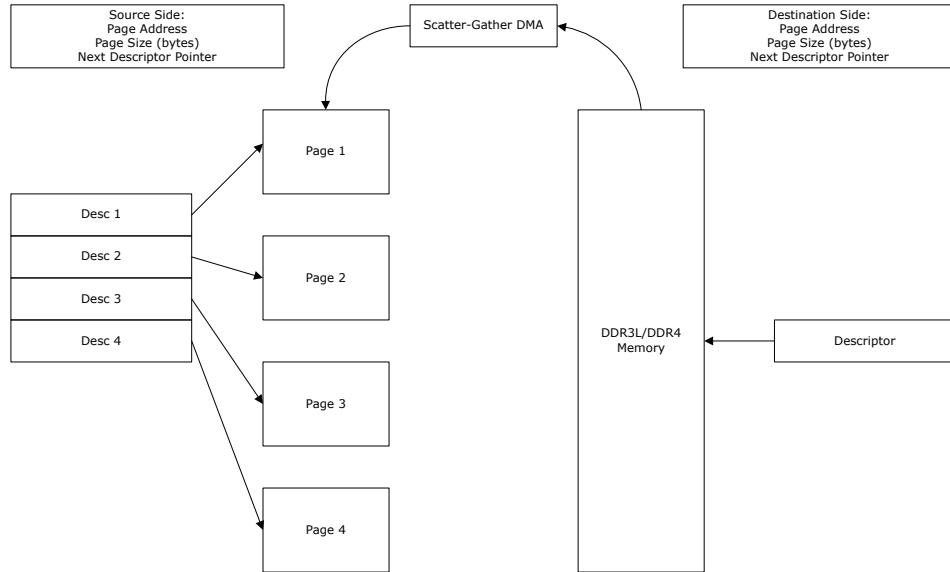
The PCIe DMA Engine1 performs DMA from DDR3L/DDR4 memories to host PC memory ([Figure 1-3](#)).

The following steps describe the SGDMA operation of PCIe DMA1:

1. PolarFire\_Pcie\_GUI application requests the PCIe driver for SG DMA. The driver on the host PC allocates the available memory locations and creates the buffer descriptors with the scattered memory location addresses and location size.
2. The source DDR3L/DDR4 memory is treated as the continuous memory. Single buffer descriptor is created in LSRAM with the base address of DDR3L/DDR4 memory. The LSRAM base address is provided to DMA controller for source descriptor address.
3. The driver configures the PCIe DMA1 with the first host PC destination buffer descriptor address and initiates the DMA.
4. DMA controller initiates read transaction to the PCIe core with the buffer descriptor address.
5. The PCIe core sends the MRd TLP to the host PC. The host PC returns a CplD TLP to the PCIe link.
6. The DMA controller extracts these buffer descriptors and initiates an AXI burst read transaction to read the data from DDR3L/DDR4 memories.
7. With this read data, DMA controller initiates the write transaction to PCIe core with the host PC memory location address in the descriptor.
8. The PCIe core sends the MWr TLP to the host PC.

9. The DMA controller repeats this process (from steps 4 to 8) until the DMA size of data transfer is completed.
10. The DMA controller sends the MSI1 interrupt to the host PC. The driver on the host PC detects the interrupt, reads the DMA status, and the number of clock cycles consumed to complete the DMA transaction to the PolarFire\_PCIE\_GUI application.

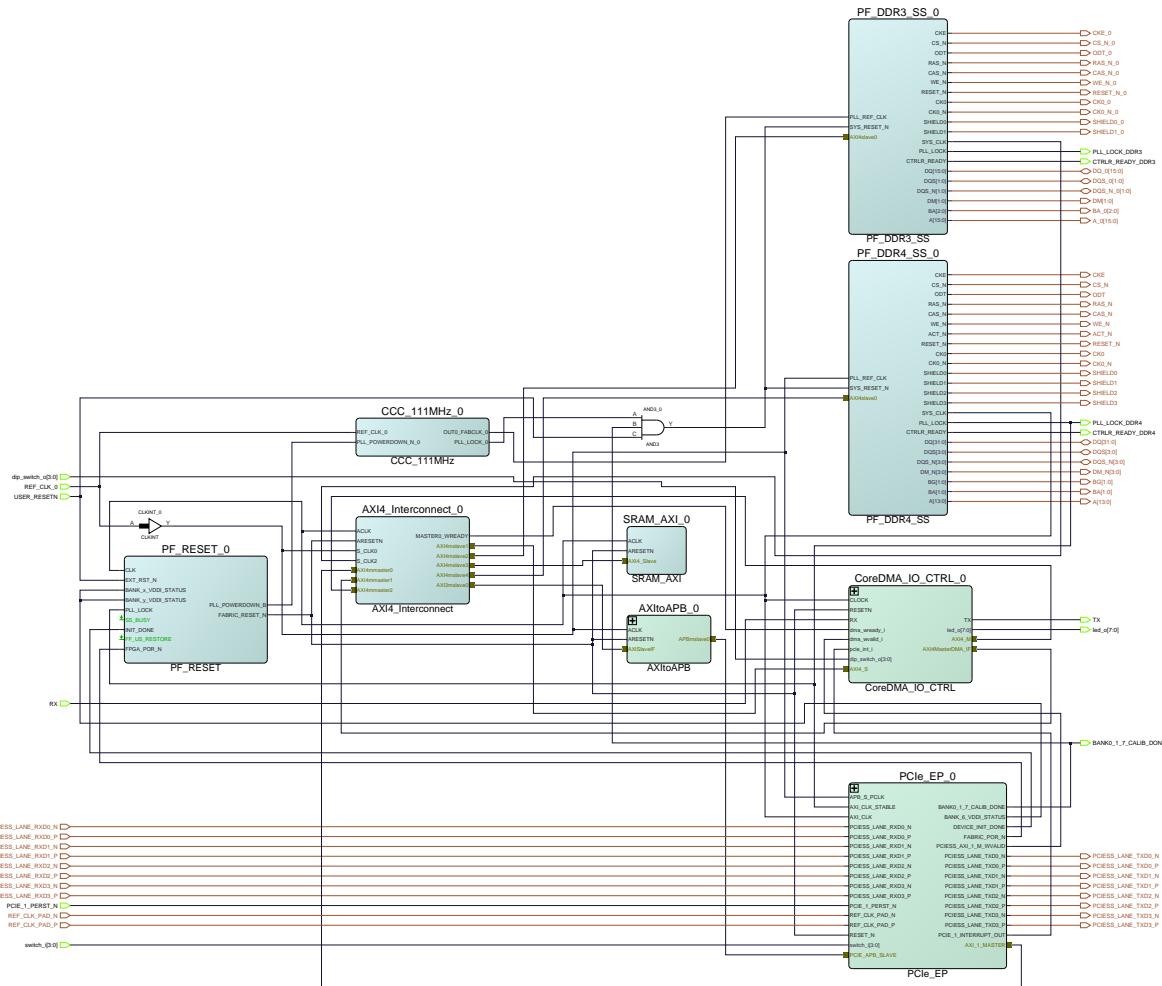
**Figure 1-3. DMA1—Example of SG DMA Operation**



### 1.3.2 Design Implementation

The following figure shows the Libero SoC software top-level design implementation of the PCIe EndPoint reference design.

Figure 1-4. PCIe EndPoint Reference Design



The top-level design includes the following SmartDesign components, memory controller subsystems, and AXI4Interconnect IP.

- PCIe EP subsystem
- CoreDMA and UART subsystem
- AXItoAPB
- DDR3L subsystem
- DDR4 subsystem
- AXI LSRAM
- AXI4Interconnect IP

### 1.3.2.1 PCIe EP Subsystem

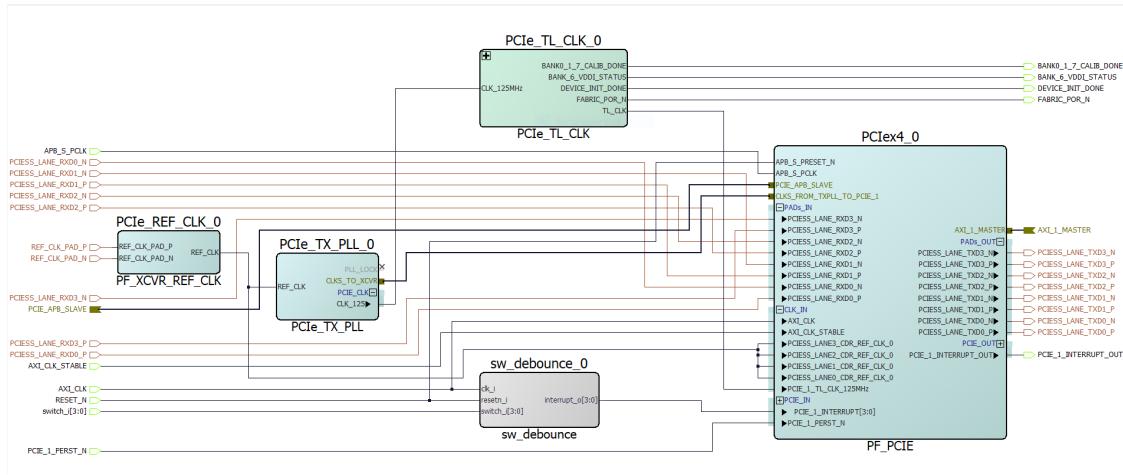
The PCIe\_EP SmartDesign implements PCIe EndPoint and its clocking scheme as shown in the following figure. It also includes the sw\_debounce module, which is used to suppress bounces from on-board push buttons and to generate a pulse to the PCIe controller interrupt line.

The PCIE core is configured as an EndPoint with maximum link speed and maximum link width—Gen2 (5.0 Gbps) link speed and  $\times 4$  link width. The **Simulation Level** in the configurator is set to **BFM** to simulate the design using PCIe BFM script. The PCIe fabric interface is always the same regardless of the link width or lane rate. The APB interface is enabled to access the PCIe DMA and Address translation registers.

The following two BARs are configured in 64-bit.

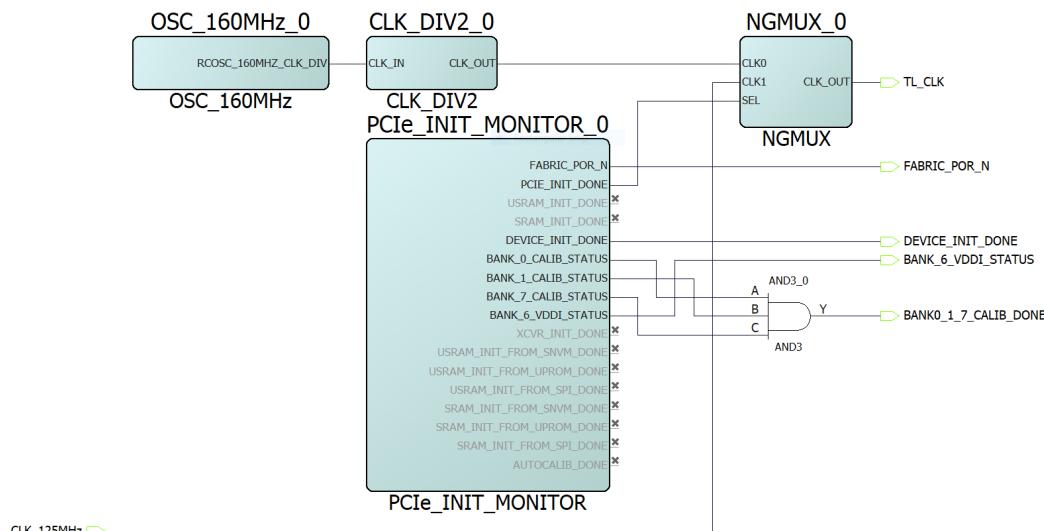
- **BAR0:** Accesses the PCIe DMA, address translation, and interrupt registers through the PCIe controller's APB interface. The address translation register associated with BAR0 is configured to translate the BAR0 address to the PCIe APB IF base address (0x0300\_0000).
  - **BAR2:** Accesses the fabric control registers and AXI LSRAM, DDR3L, and DDR4 memories. By default, the address translation register associated with BAR2 is configured to access the fabric control registers (0x1000\_0000). To access the LSRAM, DDR3L, and DDR4 memories, the driver on the host PC configures the BAR2 address translation register (TRSL\_ADDR) to LSRAM (0x3000\_0000)/DDR3L (0x2000\_0000)/DDR4 (0x4000\_0000) memory base address using the PCIe APB IF through BAR0.

**Figure 1-5. PCIe\_EP SmartDesign**



The PCIe\_TL\_CLK SmartDesign implements PCIe TL CLK for PolarFire devices. See [Figure 1-6](#). PCIe TL CLK must be connected to CLK\_125 MHz of Tx PLL. In PolarFire devices, TL CLK is available only after PCIe initialization. The 80 MHz clock is derived from the on-chip 160 MHz oscillator to drive the TL CLK during PCIe initialization. The NGMUX is used to switch this clock to the required CLK\_125 MHz after PCIe initialization. The BANK 0, BANK 1, and BANK 7 calibration status signals of PF Initialization Monitor IP is used to generate CALIB\_DONE signal, which is used for DDR3L/DDR4 reset.

**Figure 1-6. PCIe\_TL\_CLK SmartDesign**



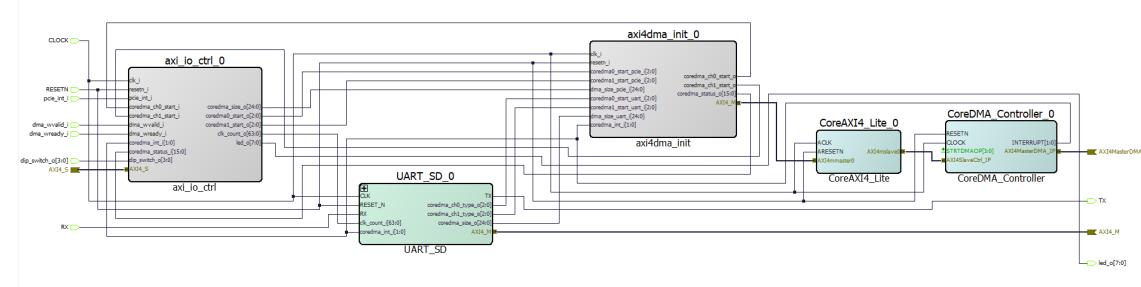
### 1.3.2.2 CoreDMA and UART Subsystem

The CoreDMA\_IO\_CTRL SmartDesign implements fabric registers, CoreDMA4DMA IP initialization, and UART\_SD. See the following figure.

The `axi4dma_init` logic initiates the CoreDMA through the AXI4Lite interface to perform the DMA as per commands from GUI. The `axi_iq_ctrl` block receives commands from PCIe BAR space and controls the IOs or `axi4dma_init` logic.

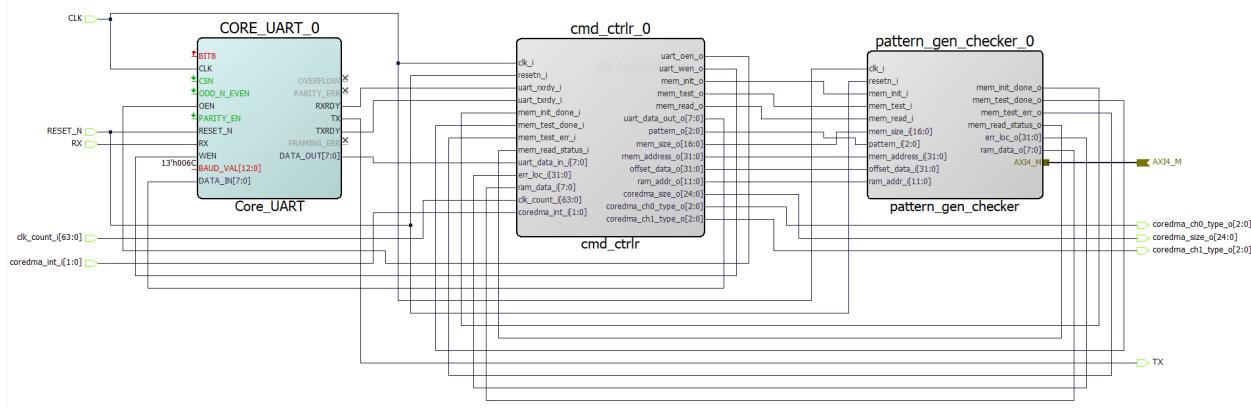
The CoreAXI4DMAController IP is configured for 64-bit AXI4 data width, and to generate interrupts for descriptor0 and descriptor1. Descriptor0 is used for—DDR3L to DDR4, DDR3L to LSRAm, and DDR4 to LSRAm DMA and descriptor1 is used for—DDR4 to DDR3L, LSRAm to DDR3L, and LSRAm to DDR4 DMA.

**Figure 1-7. CoreDMA\_IO\_CTRL SmartDesign**



The UART\_SD SmartDesign implements logic required to communicate with UART IF. See the following figure. The cmd\_ctrlr block receives commands from UART and triggers the logic to perform CoreDMA/DDR memory initialization. The pattern\_gen\_checker block initializes the DDR memory with the specified pattern and compares against the specified pattern.

**Figure 1-8. UART SmartDesign**



### 1.3.2.3 Memory Controller Subsystem

This section describes the various memory controller subsystem like DDR3L, DDR4, and AXI LSRAm.

#### 1.3.2.3.1 DDR3L

The DDR3L subsystem is configured to access the 16-bit DDR3L memory through an AXI4 interface. The “PolarFire evaluation kit DDR3L memory” preset is applied to configure all of the memory initialization and timing parameters in the DDR3L configurator.



**Important:** DDR3L is applicable only for Evaluation kit demo design.

#### 1.3.2.3.2 DDR4

The DDR4 subsystem is configured to access the 32-bit DDR4 memory through an AXI4 64-bit interface. The DDR4 memory initialization and timing parameters are configured as per the DDR4 memory on the PolarFire Evaluation/Splash kit. For more information about DDR4 subsystem configuration, see [5. Appendix 2: DDR4 Configuration](#).

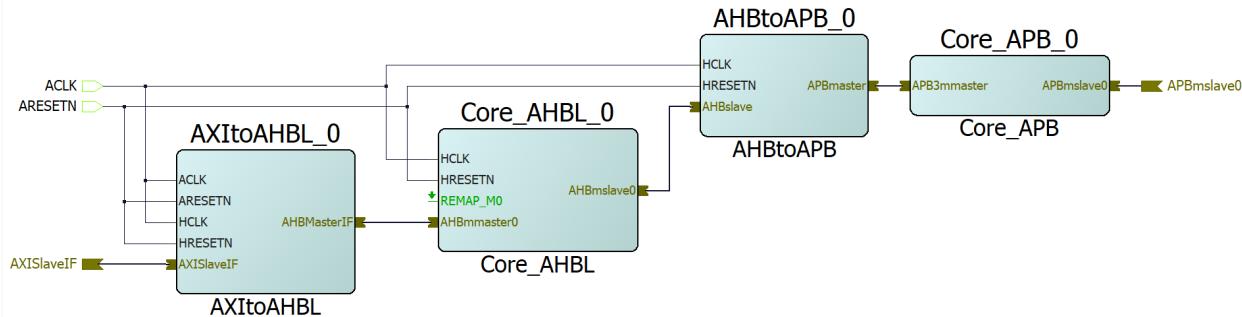
#### 1.3.2.3.3 AXI LSRAm

The AXI LSRAm in the design is configured for 4 KB. This 4 KB is over written if more than 4 KB of DMA operation is performed on LSRAm. This option is provided to exercise the throughputs with larger DMA size.

### 1.3.2.4 AXI to APB SmartDesign

The AXI\_to\_APB SmartDesign implements AXI to APB using different IP cores. See the following figure. AXI to APB IF is to access the PCIe control registers through the PCIe APB IF from the BAR0 space.

**Figure 1-9. AXI\_to\_APB SmartDesign**



### 1.3.2.5 CoreAXI4Interconnect IP

The CoreAXI4Interconnect IP is configured for the following initiator and target ports:

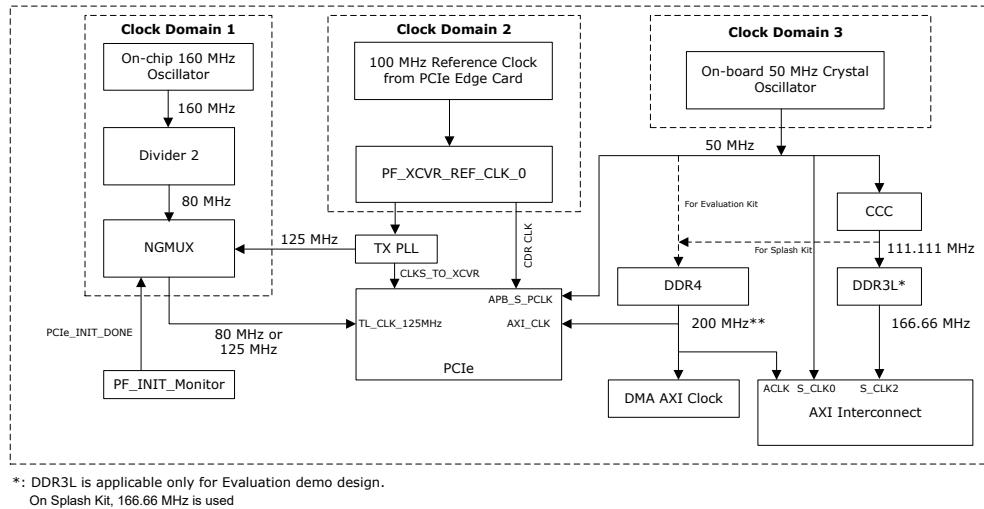
- Initiator0: PCIe
- Initiator1: CoreAXI4DMAController IP
- Initiator2: Pattern generator and checker logic (pattern\_gen\_checker block)
- Target0: AXItoAPB bridge (0x0000\_0000 to 0x0FFF\_FFFF)
- Target1: AXI Target Fabric Registers (0x1000\_0000 to 0x1FFF\_FFFF)
- Target2: DDR3L Subsystem (0x2000\_0000 to 0x2FFF\_FFFF) (not enabled for Splash kit)
- Target3: AXI4 LSRAAM (0x3000\_0000 to 0x3FFF\_FFFF)
- Target4: DDR4 Subsystem (0x4000\_0000 to 0x4FFF\_FFFF)

Slave0 is configured to convert AXI4 transactions to AXI3 transactions.

## 1.4 Clocking Structure

The following figure shows the clocking structure of PCIe EndPoint reference design.

- Clock Domain 1: Generates PCIe TL\_CLK. At power-up, it uses 80 MHz clock and switches to 125 MHz after completion of PCIe initialization.
- Clock Domain 2: Generates CDR reference and XCVR clocks for PCIe.
- Clock Domain 3: Generates 50 MHz clock for PCIe APB, DDR4 PLL reference, and CCC reference clocks. DDR4 subsystem generates a 200 MHz (166.66 MHz for Splash kit) clock for fabric AXI interface logic. DDR3L subsystem generates 166.66 MHz clock and is connected to AXI interconnect target2 CDC interface.

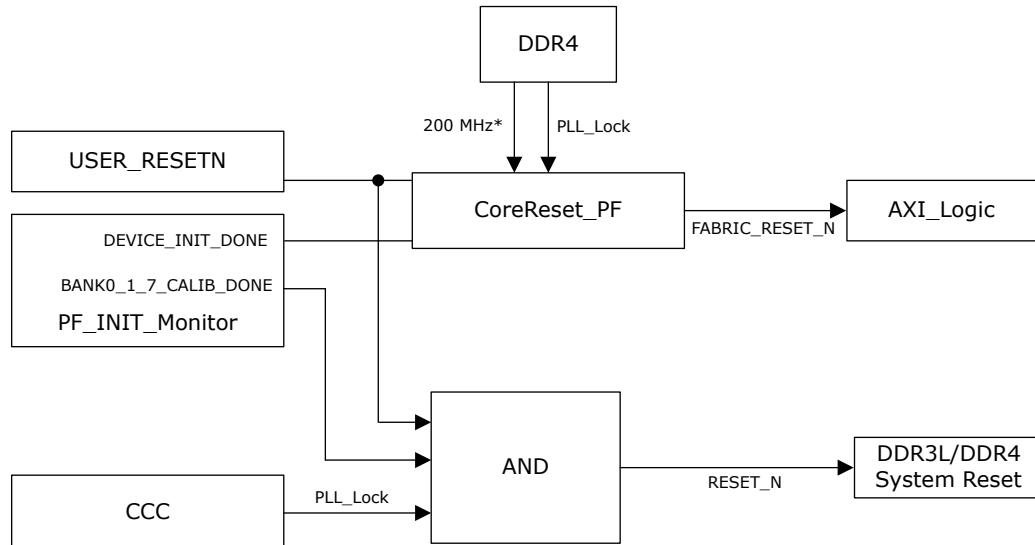
**Figure 1-10. Clocking Structure**

## 1.5 Reset Structure

The CoreReset\_PF synchronizes the external USER\_RESETN (SW6 on PolarFire Evaluation kit and SW2 on PolarFire Splash kit) to the DDR4 system clock (200 MHz) and generates the FABRIC\_RESET\_N, which drives the fabric AXI interface logic. CoreReset\_PF uses the DEVICE\_INIT\_DONE signal, which is asserted when the device initialization is complete. For more information about device initialization, see [PolarFire FPGA and PolarFire SoC FPGA Power-up and Resets User Guide](#).

For more information on CoreReset\_PF IP core, see *CoreReset\_PF handbook* from the Libero catalog.

The DDR3L/DDR4 subsystem does not require a synchronization reset as it has the reset synchronization logic. The following figure shows the reset structure in the reference design.

**Figure 1-11. Reset Structure**

\*: On Splash Kit, 166.66 MHz is used.

## 1.6 Throughput Measurement

The fabric logic uses 32-bit counters to count the number of clock cycles in each DMA transfer. The host PC application starts these counters while initiating the DMA transfers, and the fabric logic stops these counters at the end of the DMA transfer. The DMA Engine interrupts the host PC at the end of the DMA transfer and the host PC application reads the counters to calculate throughput as follows:

Throughput = Transfer Size (Byte) × Clock Frequency/Number of clock cycles taken for a transfer

The throughput includes all of the overhead of the AXI, PCIe, and DMA controller transactions.

## 1.7 Simulating the Design

Before you begin, perform the following steps:

1. Start Libero SoC in the **Project** menu, and click **Open Project**.
2. Browse `mpf_an4597_v2022p1_df/TCL_Scripts/Eval_Kit` or `mpf_an4597_v2022p1_df/TCL_Scripts/Splash_Kit`. For simulation, create the Libero Project using provided TCL scripts. See [Appendix 4 : Running the TCL script](#) to create the Libero Project.

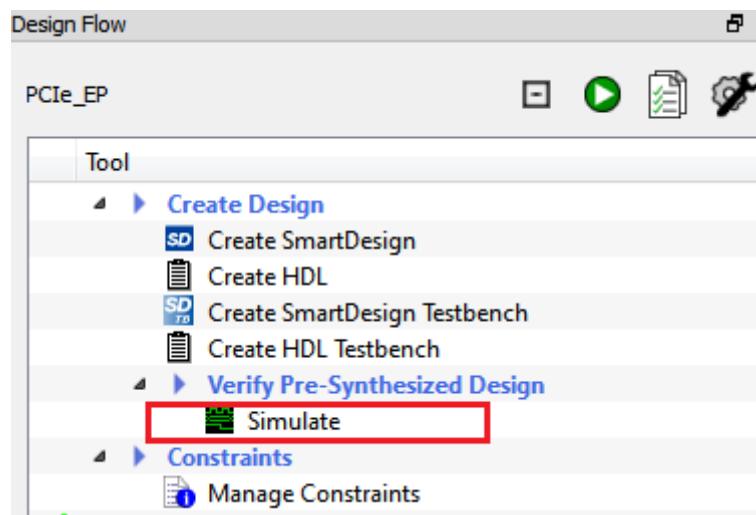
The PCIe BFM performs 1 KB DMA operations between PCIe and DDR3L, DDR4 and LSRAM memories by initiating AXI burst transactions. The PCIe simulation model replaces the entire PCIe EndPoint interface with a simple BFM that can send write transactions and read transactions over the AXI interface. These transactions are driven by a script file (`.bfm`) and allow easy simulation of the FPGA design connected to a PCIe interface. For more information about BFM commands, see [PolarFire FPGA and PolarFire SoC FPGA PCI Express User Guide](#). The micron DDR3L and DDR4 memory models are instantiated in the testbench for simulating DDR3L and DDR4 memory controllers.



**Important:** In the Design Flow tab, system verilog is selected, as the memory models from Micron are in the system verilog.

In the **Project settings > Design Flow** tab, double click **Simulate under Verify Pre-Synthesized Design** to simulate the design. The ModelSim tool takes 10 to 15 minutes to complete the simulation. See the following figure.

**Figure 1-12. Simulating the Design**



### 1.7.1 Simulation Flow

The following steps describe the PCIe BFM simulation flow.

1. At the start, the NSYSREST signal, reset all the components.
2. DDR3L and DDR4 memory controllers initializes the DDR3L/DDR4 memories and release the CTRLR\_READY.
3. The PCIe BFM starts executing the BFM script  
PCIe4\_PCIE4\_0\_PF\_PCIE\_PCIE1\_user.bfm.
4. The PCIe EndPoint AXI4 initiator interface initiates write and read burst transactions to SRAM\_AXI\_0, DDR3L, DDR4 through CoreAXI4Interconnect as per the .bfm script.
5. After 18  $\mu$ s, the simulation completes. **PCIE1 BFM Simulation Complete – 282 Instructions – NO ERRORS** message is displayed for **Evaluation kit**, as shown in [Figure 2-5](#).
6. After 13  $\mu$ s, the simulation completes. **PCIE1 BFM Simulation Complete – 272 Instructions – NO ERRORS** message is displayed for **Splash kit**. The ModelSim transcript window displays the BFM commands



**Important:**

- While running the scripts, simulation is running in batch mode by default which takes more time for the design to complete the build and compile flow. If users do not want to run the simulation, they can comment the simulation flow command in the script.tcl.
- For evaluation kit simulations, users might get errors in the Simulation window and user can ignore them.

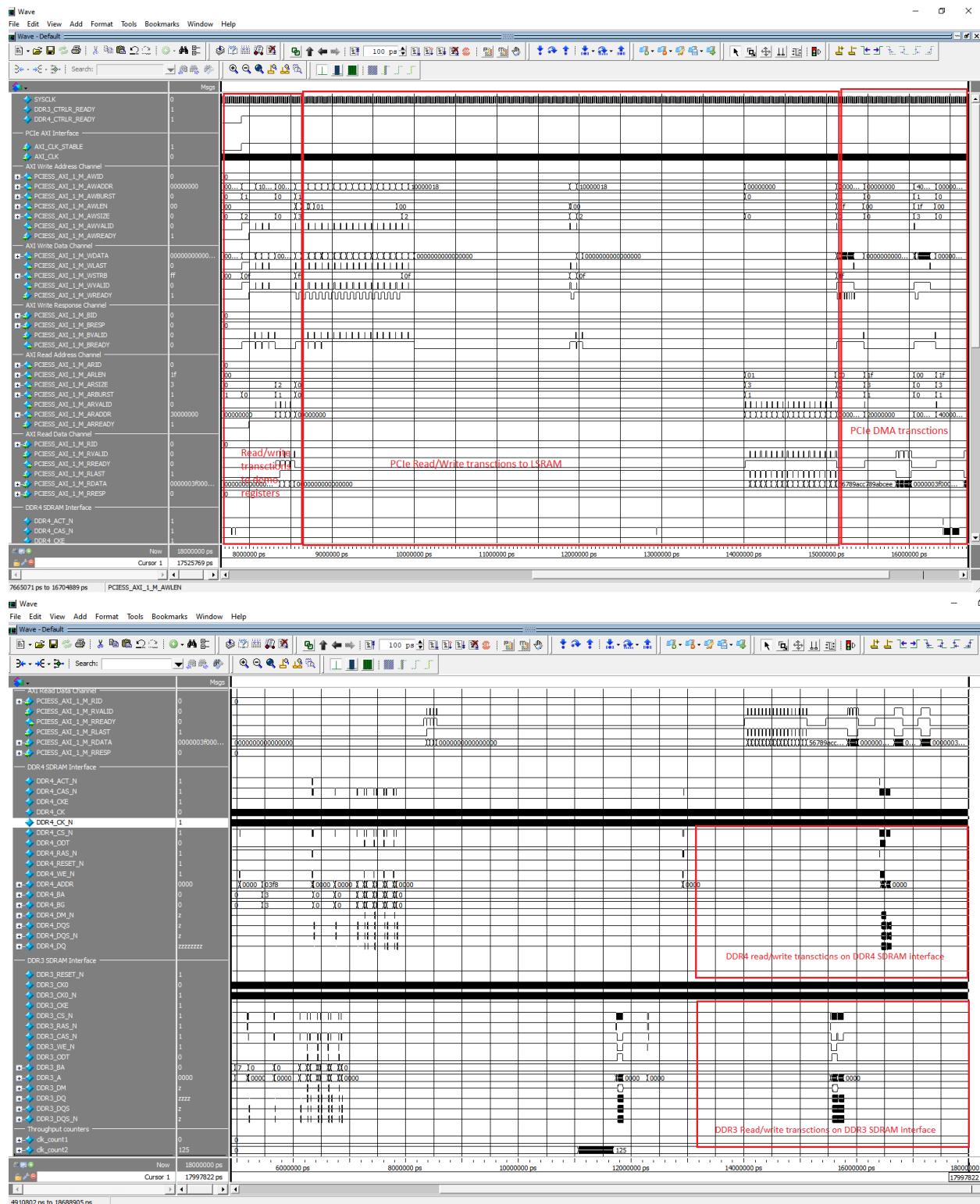
The ModelSim transcript window displays the BFM commands execution messages.

**Figure 1-13. Simulation Transcript Window**

```
# SFM: Data Read 300000a8 0000002b00000002c at 17686.250000ns
# SFM: Data Read 300000b0 0000002d00000002e at 17691.250000ns
# SFM: Data Read 300000b8 0000002f000000030 at 17696.250000ns
# SFM: Data Read 300000c0 00000031000000032 at 17701.250000ns
# SFM: Data Read 300000c8 00000033000000034 at 17706.250000ns
# SFM: Data Read 300000d0 00000035000000036 at 17711.250000ns
# SFM: Data Read 300000d8 00000037000000038 at 17716.250000ns
# SFM: Data Read 300000e0 0000003900000003a at 17721.250000ns
#
# -----
# -----DMA TRANSFER DONE(FROM FABRIC ADDRESS SPACE TO PCIe ADDRESS SPACE)-----
#
# SFM: Data Read 300000e8 0000003b00000003c at 17726.250000ns
# BFM:204:wait 1 starting at 17731 ns
# SFM: Data Read 300000f0 0000003d00000003e at 17731.250000ns
# BFM: ****End of PCIe BFM Simulation*****
# BFM:207:return
# SFM: Data Read 300000f8 0000003f000000040 at 17736.250000ns
#####
#
# PCIE1 BFM Simulation Complete - 282 Instructions - NO ERRORS
#
#####
```

The following figure shows the actual **Waveform** window displaying the sequence of data being written and read using BFM.

Figure 1-14. Simulation Waveform Window



## 2. Libero Design Flow

The Libero design flow involves the following processes:

- Synthesize
- Place and route
- Verify timing
- Design and Memory Initialization
- Generate Bitstream
- Run PROGRAM Action

### 2.1 Synthesize

Go to the **Design Flow** window and double click **Synthesize**.

When the synthesis is successful, a green tick mark appears ([Figure 2-5](#)).

#### 2.1.1 Resource Utilization

The following table lists the resource utilization of the PCIe Endpoint design for Evaluation kit. These values may vary slightly for different Libero runs, settings, and seed values.

**Table 2-1. Resource Utilization—Evaluation Kit**

Type	Used	Total	Percentage
4LUT	46323	299544	15.46
DFF	37776	299544	12.61
I/O Register	0	510	0.00
User I/O	154	512	30.08
– Single-ended I/O	138	512	26.95
– Differential I/O Pairs	8	256	3.13

The following table lists the resource utilization of the PCIe Endpoint design for Splash kit. These values may vary slightly for different Libero runs, settings, and seed values.

**Table 2-2. Resource Utilization—Splash Kit**

Type	Used	Total	Percentage
4LUT	32850	299544	10.97
DFF	26597	299544	8.88
I/O Register	0	242	0.00
User I/O	99	244	40.57
– Single-ended I/O	89	244	36.48
– Differential I/O Pairs	5	122	4.10

### 2.2 Place-and-Route

To place and route the design, the TX\_PLL, XCVR\_REF\_CLK, DDR3L, DDR4, and CCC need to be constrained using the **I/O Editor** as shown in the following figures.

Figure 2-1. I/O Editor—XCVR View

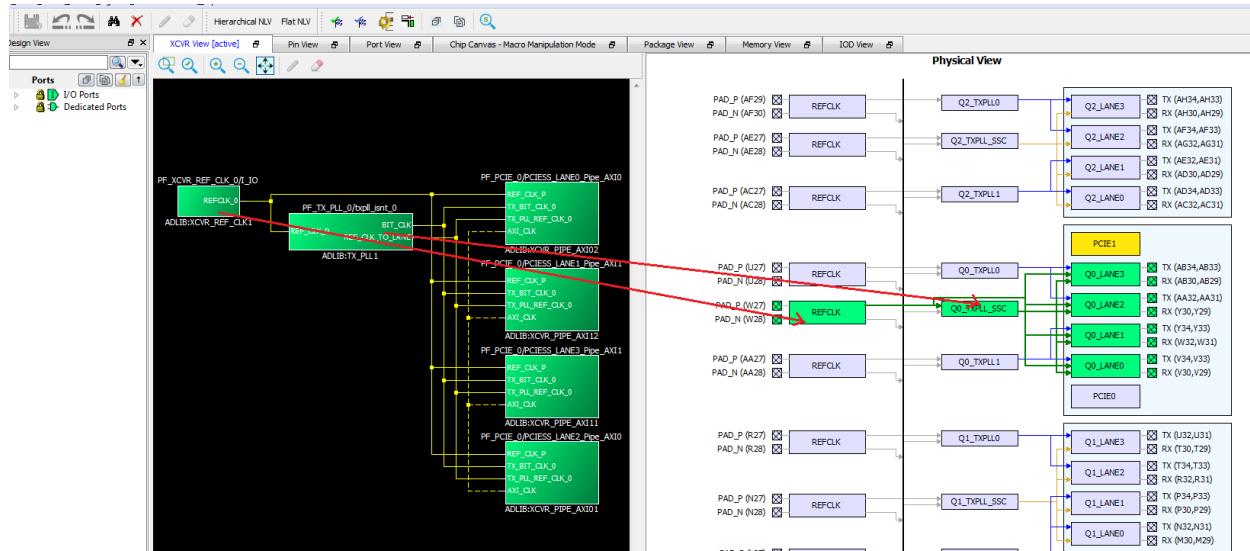


Figure 2-2. I/O Editor—DDR3L Memory View

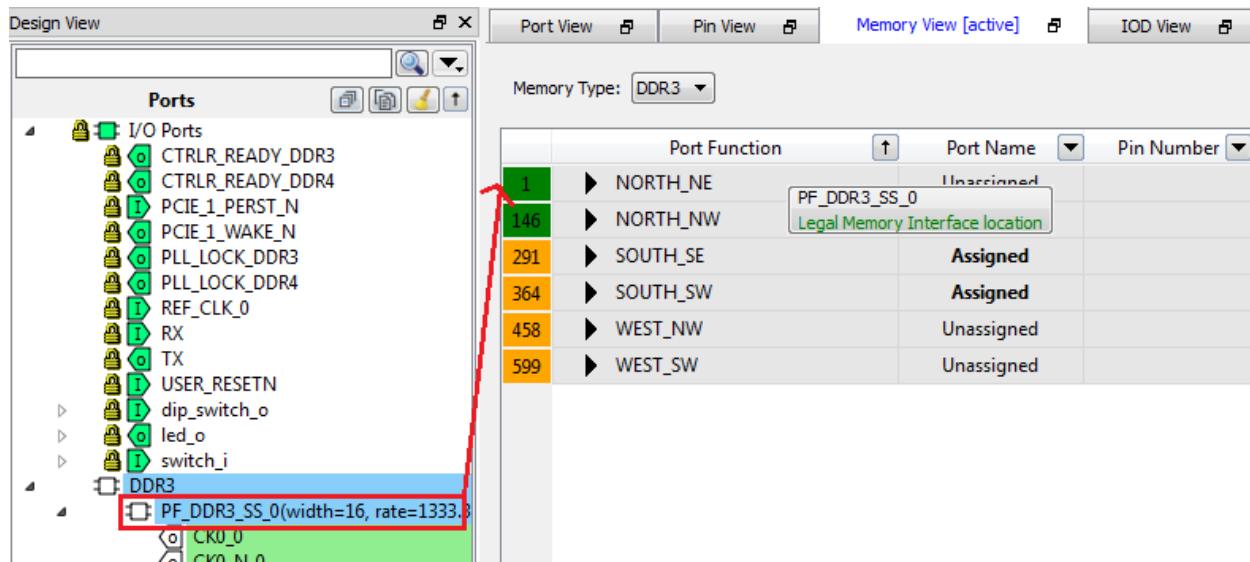
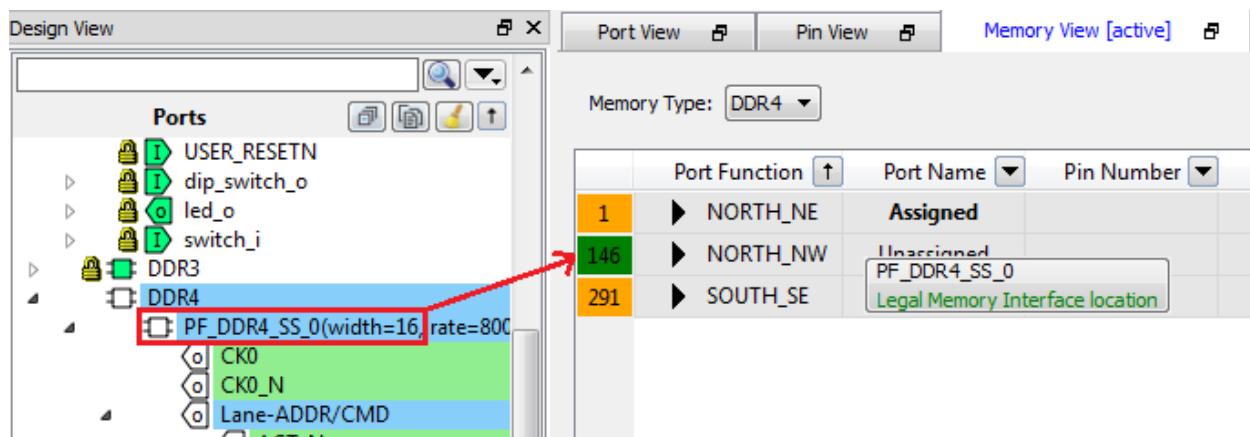
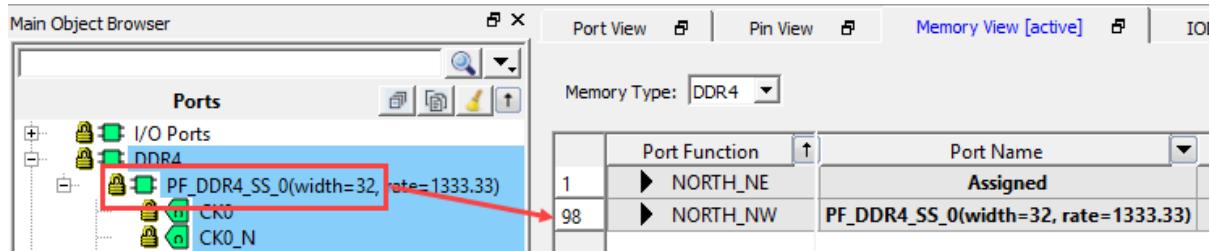


Figure 2-3. I/O Editor—DDR4 Memory View (For Evaluation Kit)

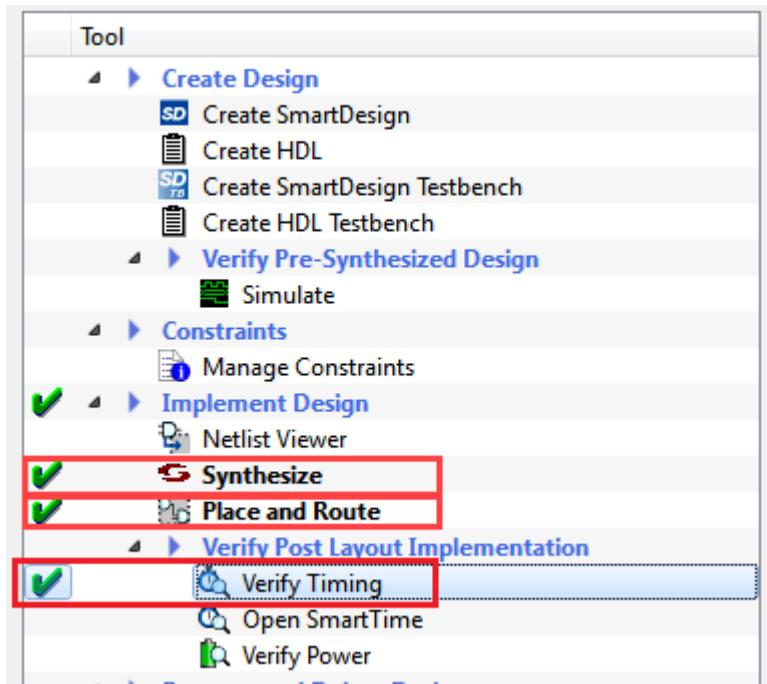


**Figure 2-4. I/O Editor—DDR4 Memory View (For Splash Kit)**

Go to the **Design Flow** window and double click **Place and Route**. When place and route is successful, a green tick mark appears, as shown in [Figure 2-5](#).

## 2.3 Verify Timing

Go to the **Design Flow** window and double click **Verify Timing**. When the design successfully meets the timing requirements, a green tick mark appears.

**Figure 2-5. Design Flow**

## 2.4 Generate Bitstream

To generate the bitstream, perform the following steps:

1. Double click **Generate Bitstream** from the **Design Flow** tab. When the bitstream is successfully generated, a green tick mark appears as shown in [Figure 2-8](#).
2. Right click **Generate Bitstream** and select **View Report** to view the corresponding log file in the **Reports** tab.

## 2.5 Run PROGRAM Action for Evaluation Kit

After generating the bitstream, the PolarFire device must be programmed. To program the PolarFire device, perform the following steps:

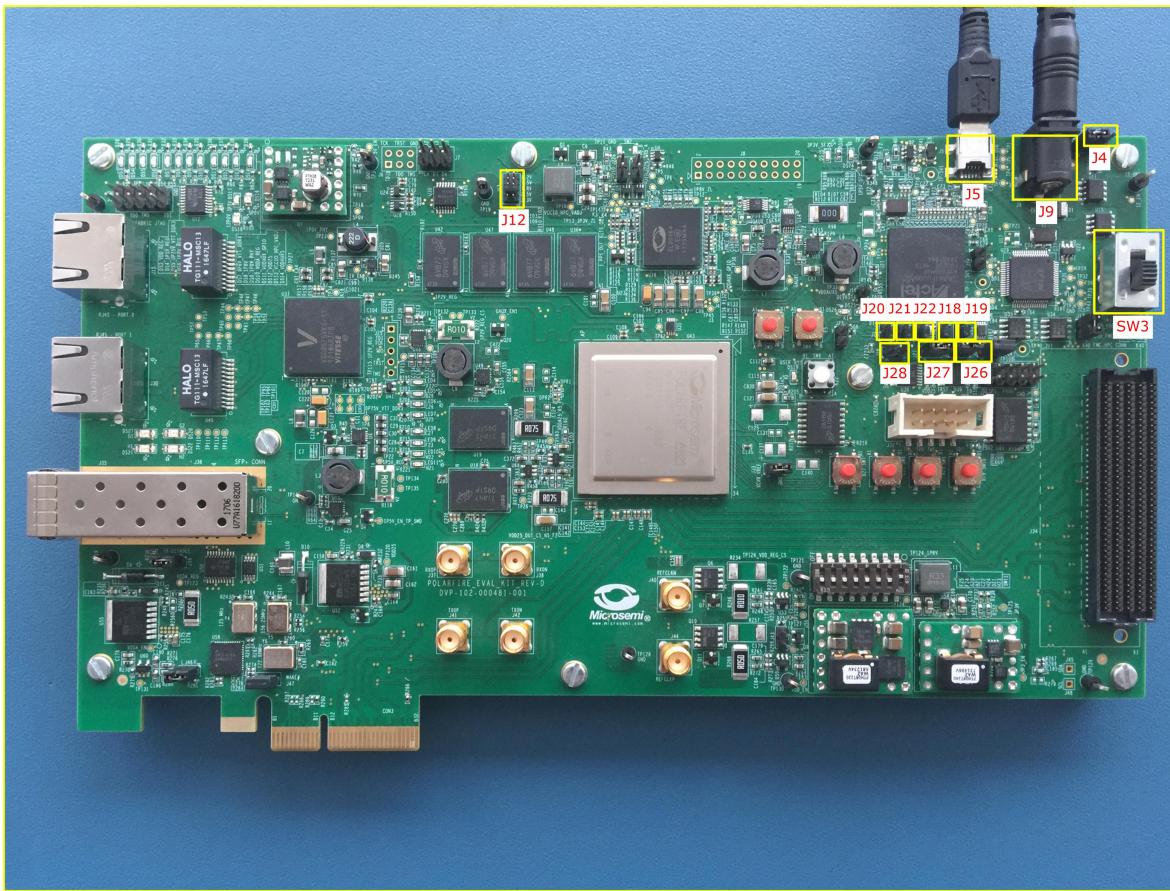
1. Ensure that the jumper settings on the board are the same as those listed in the following table.

**Table 2-3. Jumper Settings**

Jumper	Description
J18, J19, J20, J21, and J22	Short pin 2 and 3 for programming the PolarFire® FPGA through FTDI
J28	Short pin 1 and 2 for programming through the on-board FlashPro5
J26	Short pin 1 and 2 for programming through the FTDI SPI
J27	Short pin 1 and 2 for programming through the FTDI SPI
J4	Short pin 1 and 2 for manual power switching using SW3
J12	Short pin 3 and 4 for 2.5V

2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the Host PC to J5 (FTDI port) on the board.
4. Power on the board using the SW3 slide switch.

**Figure 2-6. Evaluation Kit Board Setup**



5. Double click **Run PROGRAM Action** from the Libero > Design Flow tab.

## 2.6

### Run PROGRAM Action for Splash Kit

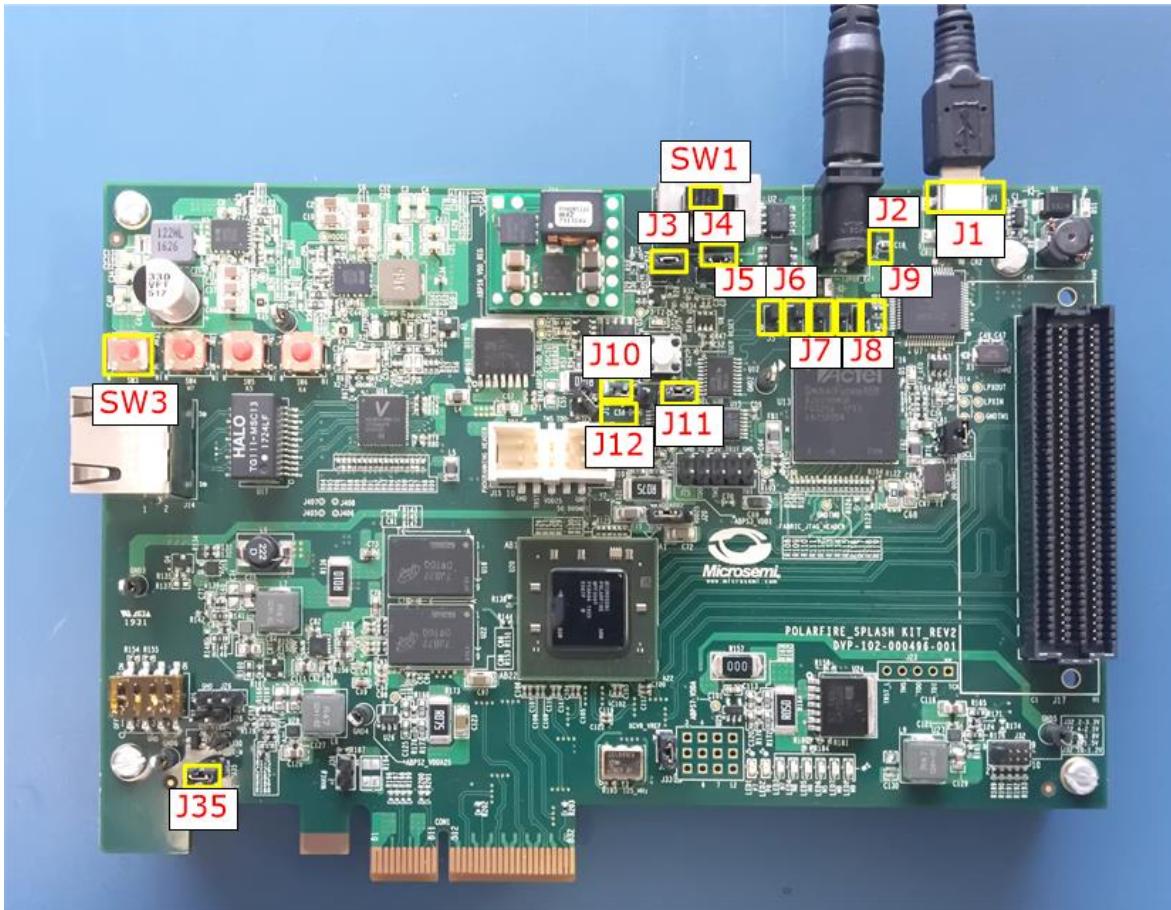
After generating the bitstream, the PolarFire device must be programmed. To program the PolarFire device, perform the following steps:

1. Ensure that the jumper settings on the board are the same as those listed in the following table.

**Table 2-4. Jumper Settings**

Jumper	Description
J5, J6, J7, J8, and J9	Short pin 2 and 3 for programming the PolarFire® FPGA through FTDI
J11	Short pin 1 and 2 for programming through the FTDI chip
J10	Short pin 1 and 2 for programming through the FTDI SPI
J4	Short pin 1 and 2 for manual power switching using SW1
J3	Open pin 1 and 2 for 1.0V

2. Connect the power supply cable to the J2 connector on the board.
3. Connect the USB cable from the Host PC to J1 (FTDI port) on the board.
4. Power on the board using the SW1 slide switch.

**Figure 2-7. Splash Kit Board Setup**

5. Double click **Run PROGRAM Action** from the Libero > Design Flow tab.

When the device is programmed successfully, a green tick mark appears, as shown in the following figure. See [3. Running the Demo](#) to run the PCIe EndPoint demo.

**Figure 2-8. Programming the Device**

### 3. Running the Demo

This section describes how to install and use the PCIe Demo application. The PolarFire PCIe demo application is a simple GUI that runs on the host PC to communicate with the PolarFire PCIe EndPoint device. It provides PCIe link status, driver information, and demo controls. The PolarFire PCIe demo application invokes the PCIe driver installed on the host PC and provides commands to the driver according to the selection made.

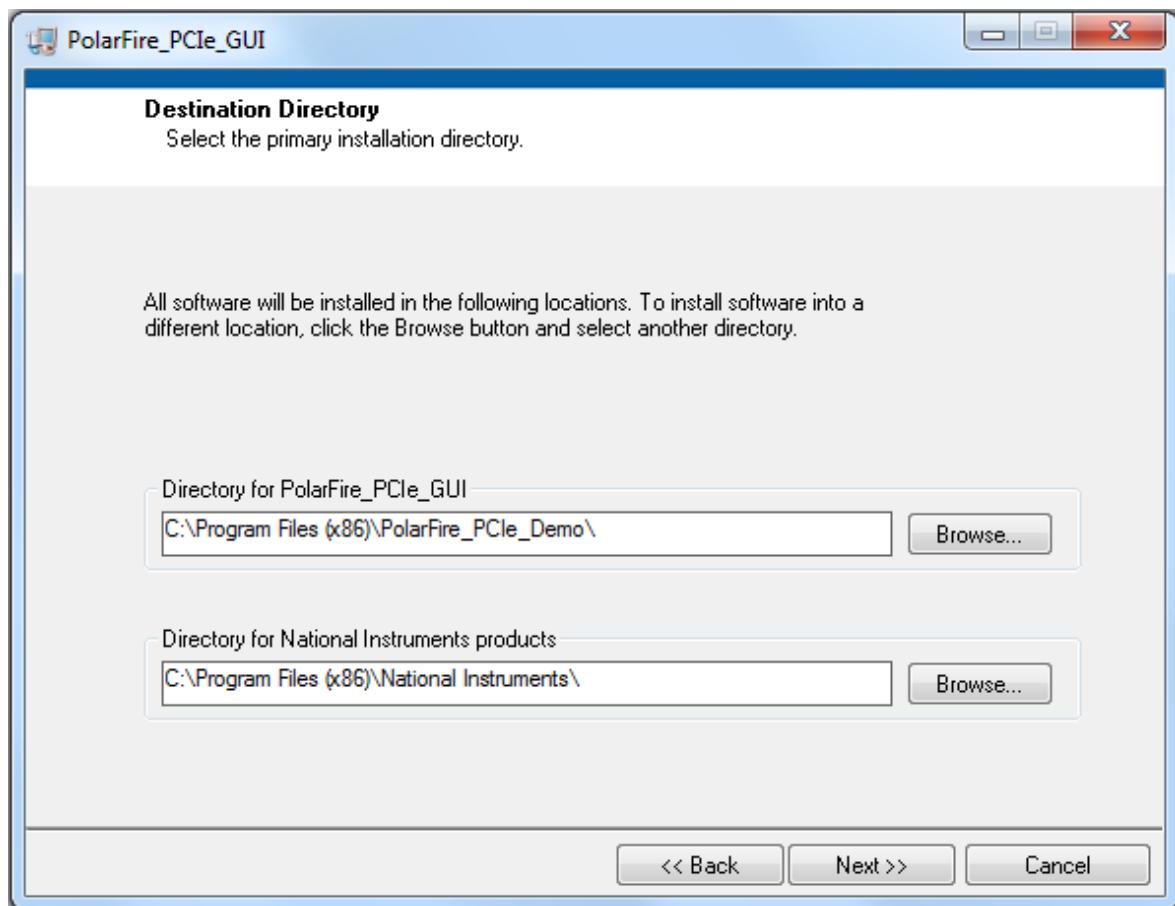
This section also describes how to connect the kit to the Host PC PCIe slot. If the host PC PCIe slot is not available, the DMA between DDR3L/DDR4 and LSRAM can be exercised through UART IF.

#### 3.1 Installing PCIe Demo Application

To install the PolarFire PCIe Demo application, perform the following steps:

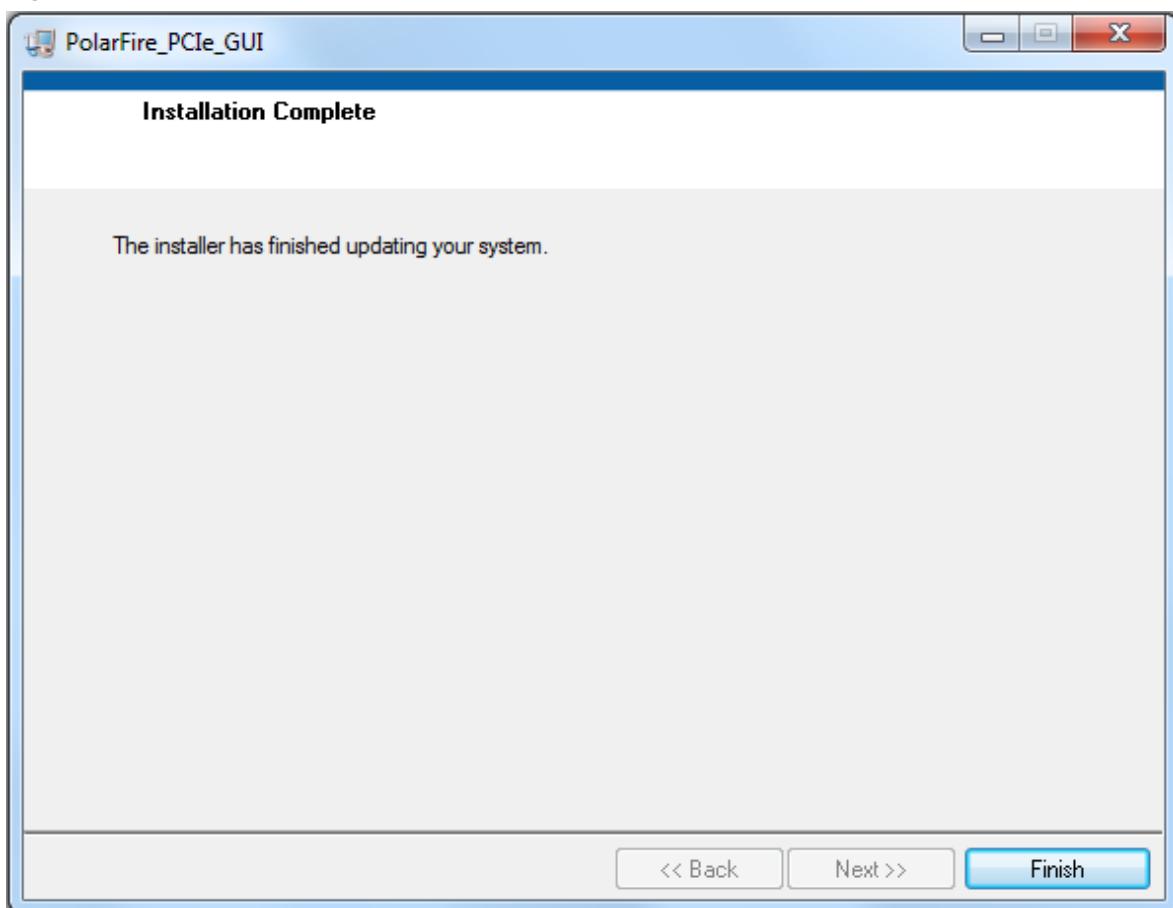
1. Install the GUI\_Installer (`setup.exe`) from the following design files folder:  
`mpf_an4597_v2022p1_df/GUI_Installer`
2. Double click the `setup.exe` in the provided GUI installation: (`GUI_Installer\setup.exe`).
3. Apply default options as shown in the following figure.

Figure 3-1. Installing PCIe Demo Application



4. Click **Next** to start the installation.
5. Click **Finish** to complete the installation.

**Figure 3-2. Successful Installation of PCIe Demo Application**



## 3.2 Running the Demo Through PCIe

This section shows how to connect the board to host PC PCIe slot, installing the PCIe drivers and running the demo application.

### 3.2.1 Connecting the Board to the Host PC PCIe Slot

1. After successful programming, power OFF the PolarFire Evaluation/Splash board and shut down the host PC.
2. Connect the CON3-PCIe Edge connector of the PolarFire Evaluation/Splash board to the host PC's PCIe slot through the PCI Edge card ribbon cable.

This demo is designed to work with any PCIe Gen2 compliant slot. If the host PC does not support Gen2 compliant slot, the demo switches to Gen1 mode.

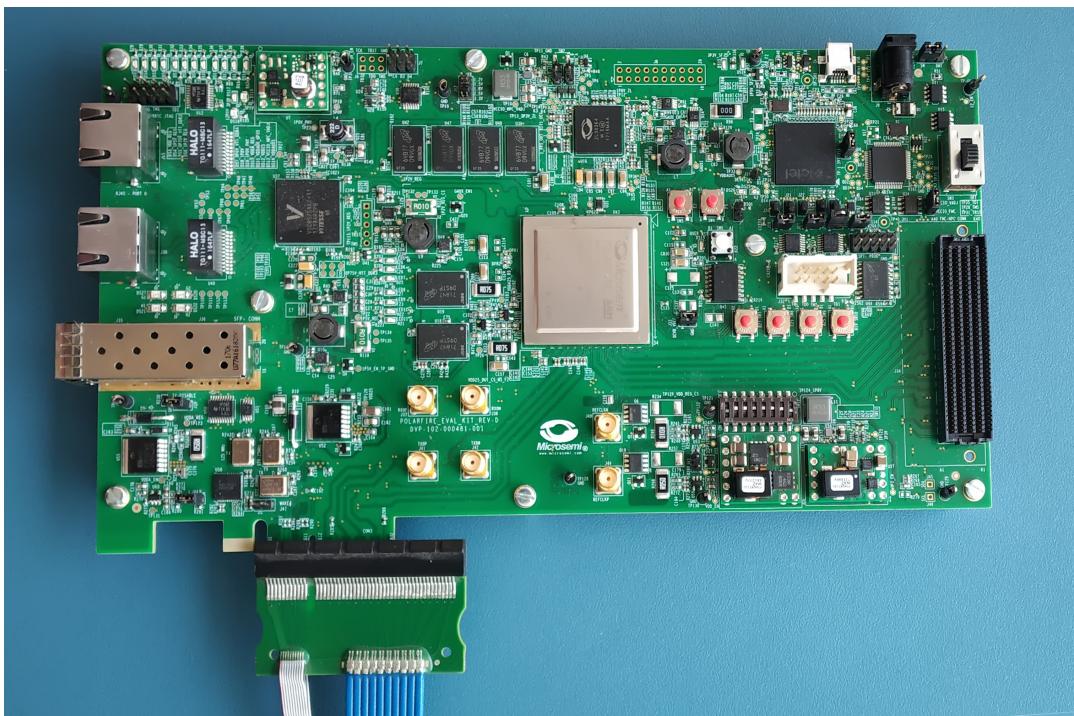


**Important:**

- Power OFF the host PC while inserting the PCIe Edge connector. If it is not powered OFF, the PCIe device detection and the selection of Gen1 or Gen2 mode might fail. The device detection and selection depend on the host PC PCIe configuration.
- After connecting the board to the host PC, the host PC may power on without manually switching on the PC.

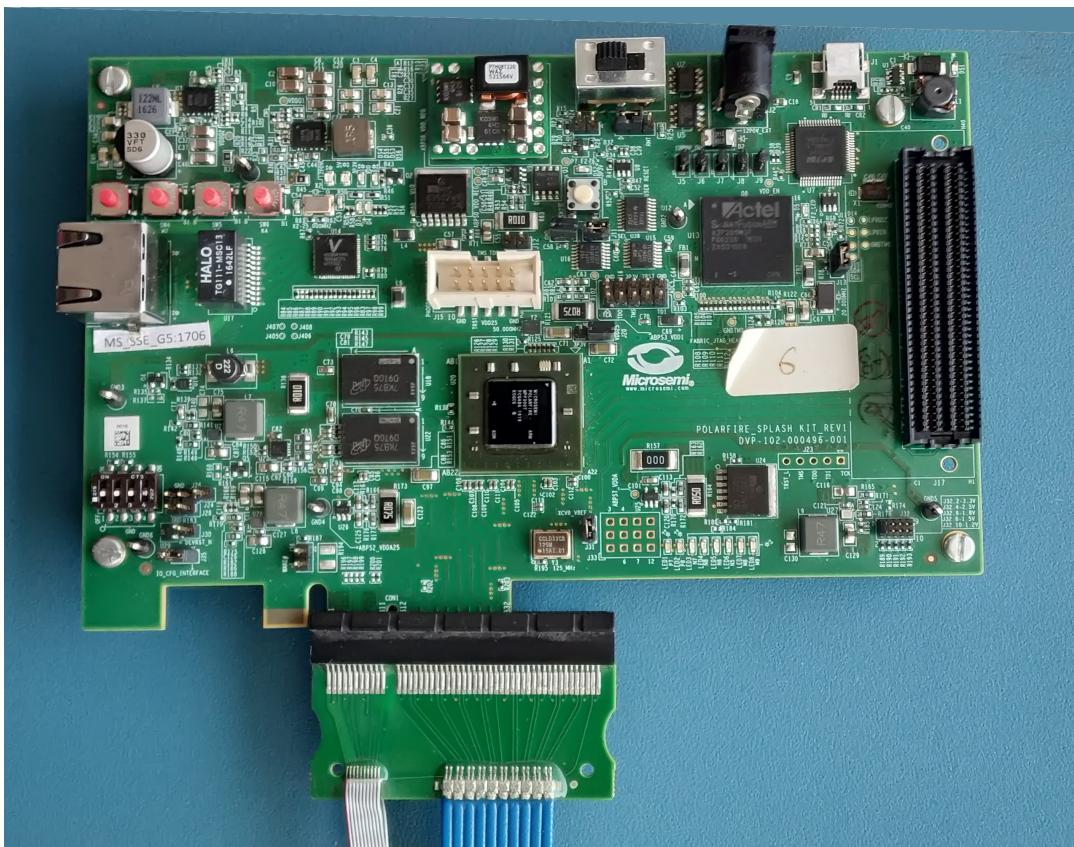
The following figure shows the board setup for the host PC in which the PolarFire Evaluation Kit is connected to the host PC PCIe slot using PCIe Edge Card Ribbon cable (not supplied with the kit).

**Figure 3-3. PolarFire Evaluation Kit Setup for Host PC**



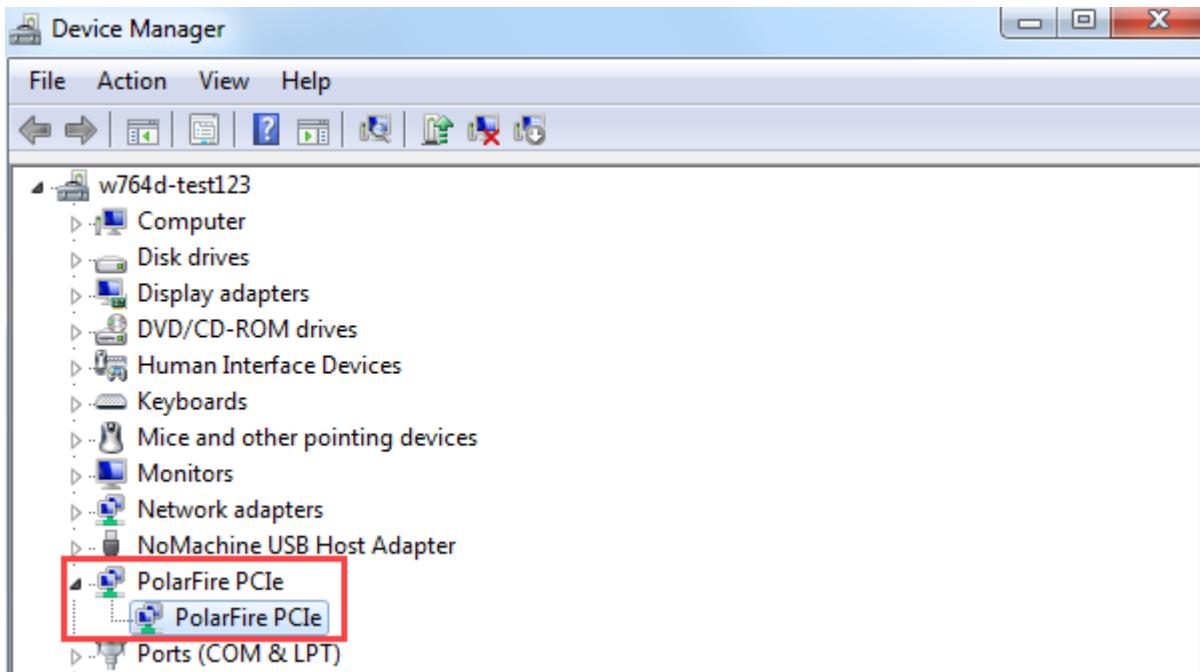
3. Power-on the power supply switch SW3.

The following figure shows the board setup for the host PC in which the PolarFire Splash Kit is connected to the host PC PCIe slot.



4. Power-on the power supply switch SW1.
  5. Power-on the host PC and check the **Device Manager** of the Host PC for the PCIe Device.
- The following figure shows the example **Device Manager** window.

Figure 3-4. Device Manager



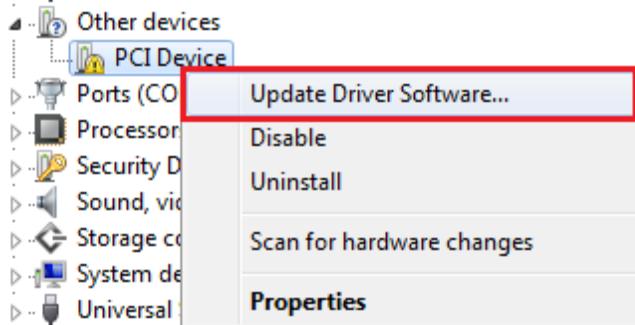
**Important:** If the device is still not detected, check if the BIOS version in the host PC is the latest and if PCI is enabled in the host PC BIOS.

### 3.2.2 Driver Installation

To install the PCIe drivers on the host PC, perform the following steps:

1. In the **Device Manager**, right click **PCI Device** and select **Update Driver Software...** as shown in the following figure. To install the drivers, administrative rights are required.

Figure 3-5. Update Driver Software

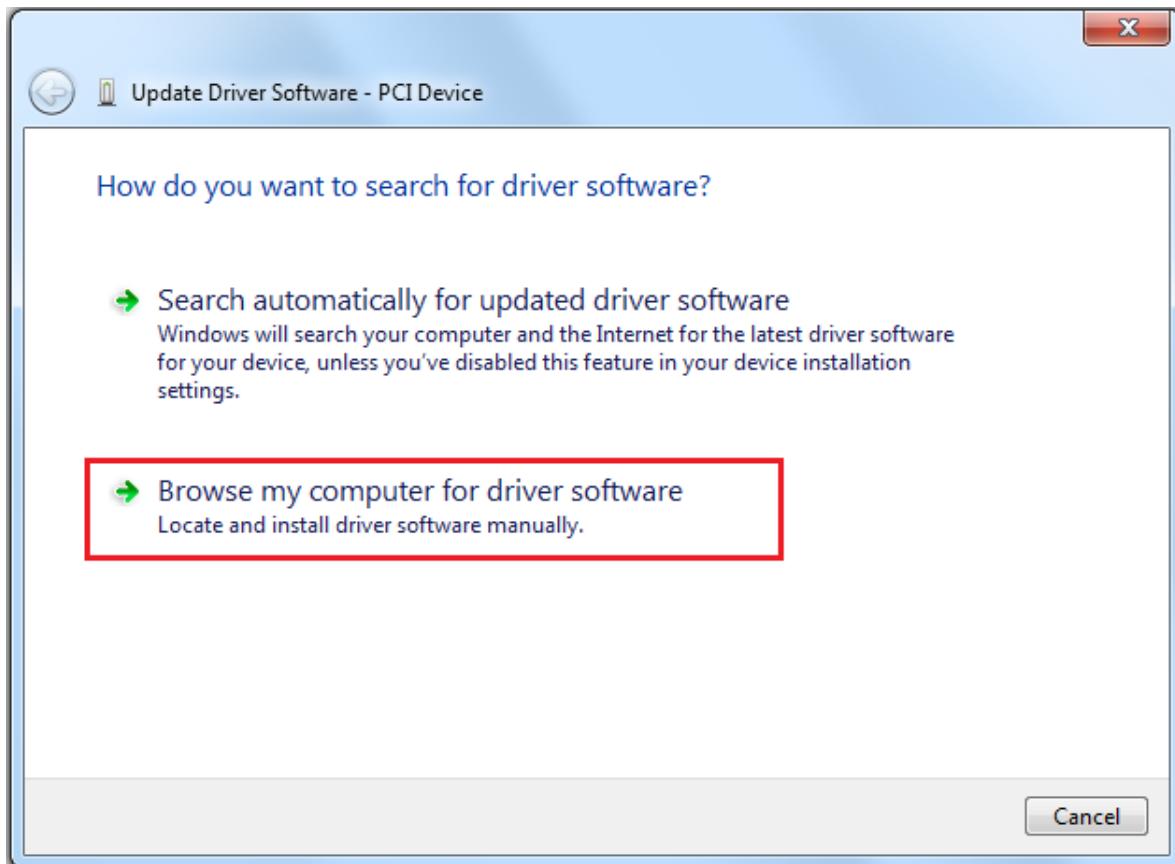




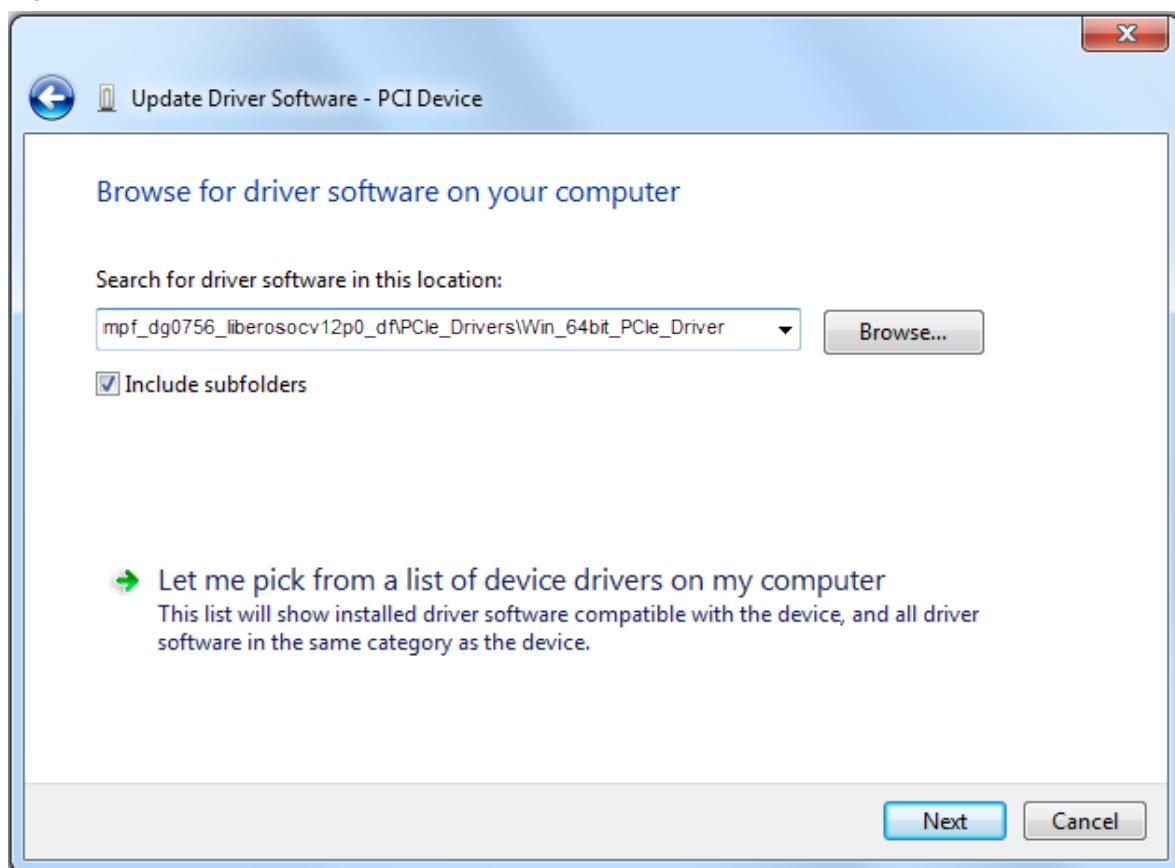
**Important:** Uninstall the existing Microchip PolarFire drivers on the host PC before proceeding to next step.

2. In the **Update Driver Software - PCIe Device** window, select **Browse my computer for driver software**, as shown in the following figure.

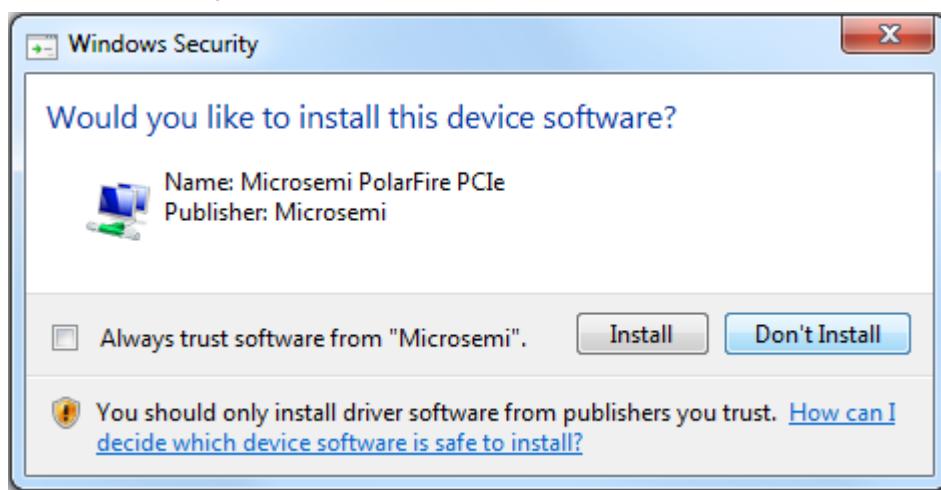
**Figure 3-6. Browse for Driver Software**

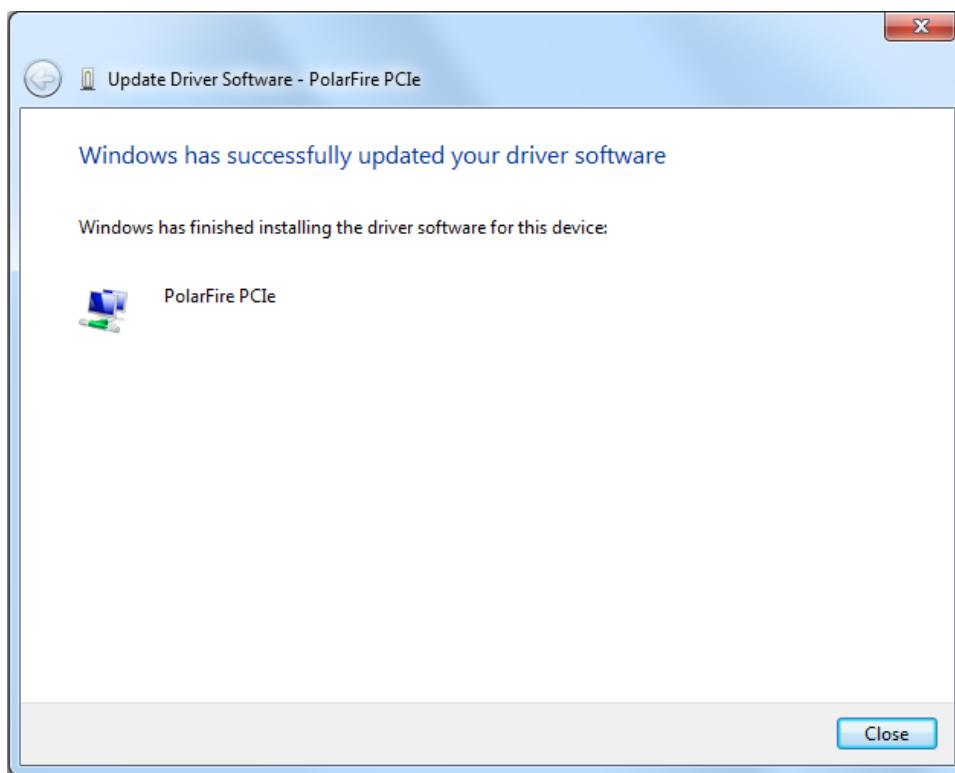


3. Browse the drivers folder: `mpf_an4597_v2022p1_df\PCIe_Drivers\Win_64bit_PCIE_Driver` and click **Next**, as shown in the following figure.

**Figure 3-7. Browse for Driver Software Continued**

4. The **Windows Security** dialog box is displayed. Click **Install** as shown in the following figure. After successful driver installation, a message appears. See [Figure 3-9](#).

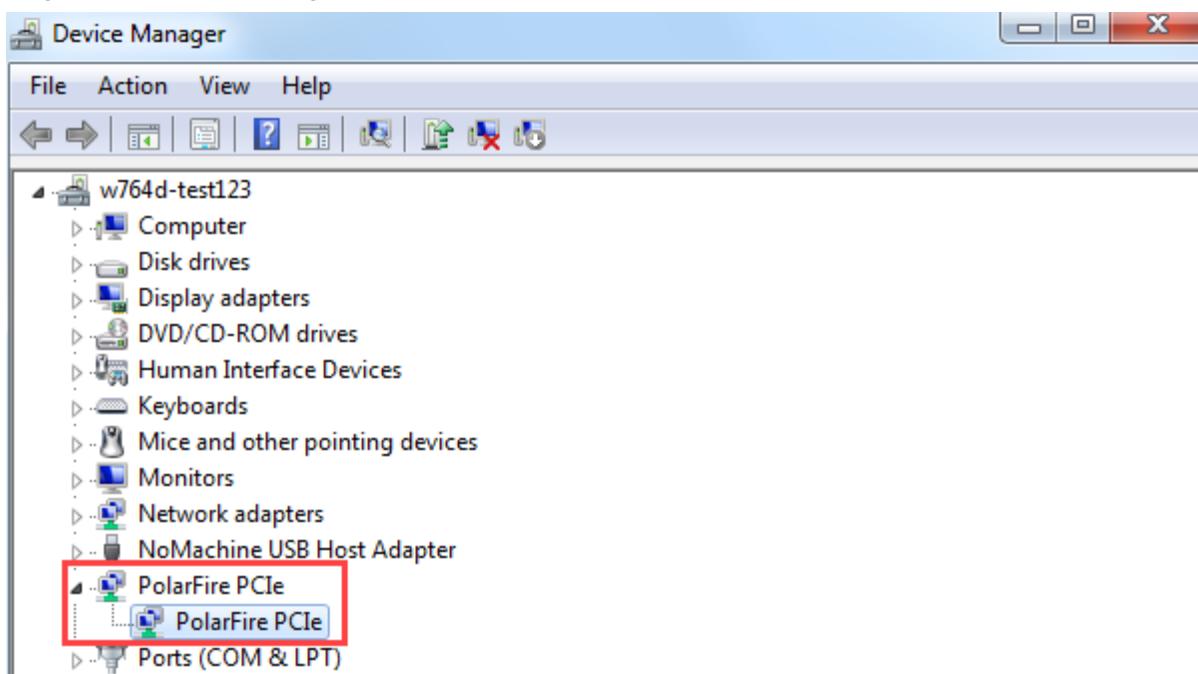
**Figure 3-8. Windows Security**

**Figure 3-9. Successful Driver Installation**

### 3.2.3 Running the PCIe Demo Application

To run the demo design, perform the following steps:

1. In the host PC **Device Manager**, to expand the **PolarFire PCIe** device, click **PolarFire PCIe**.

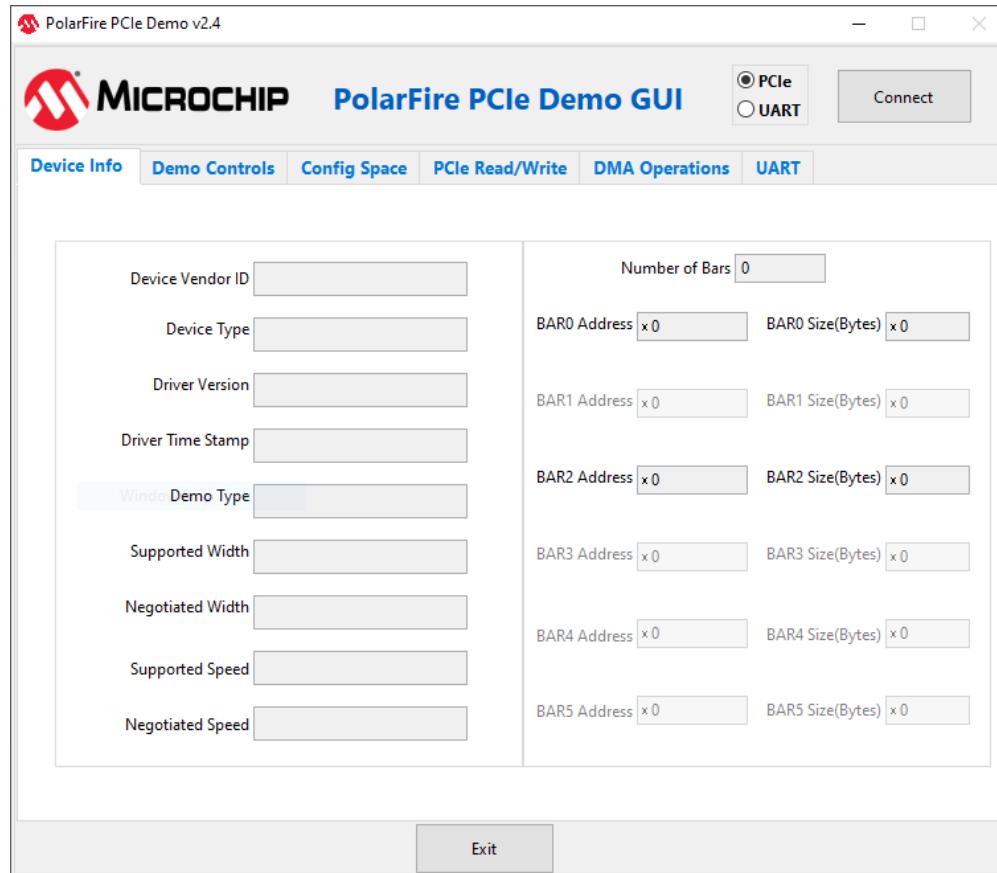
**Figure 3-10. Device Manager—PCIe Device Detection**



**Important:** If a warning message is displayed for PolarFire PCIe driver while accessing, uninstall and re-install the driver.

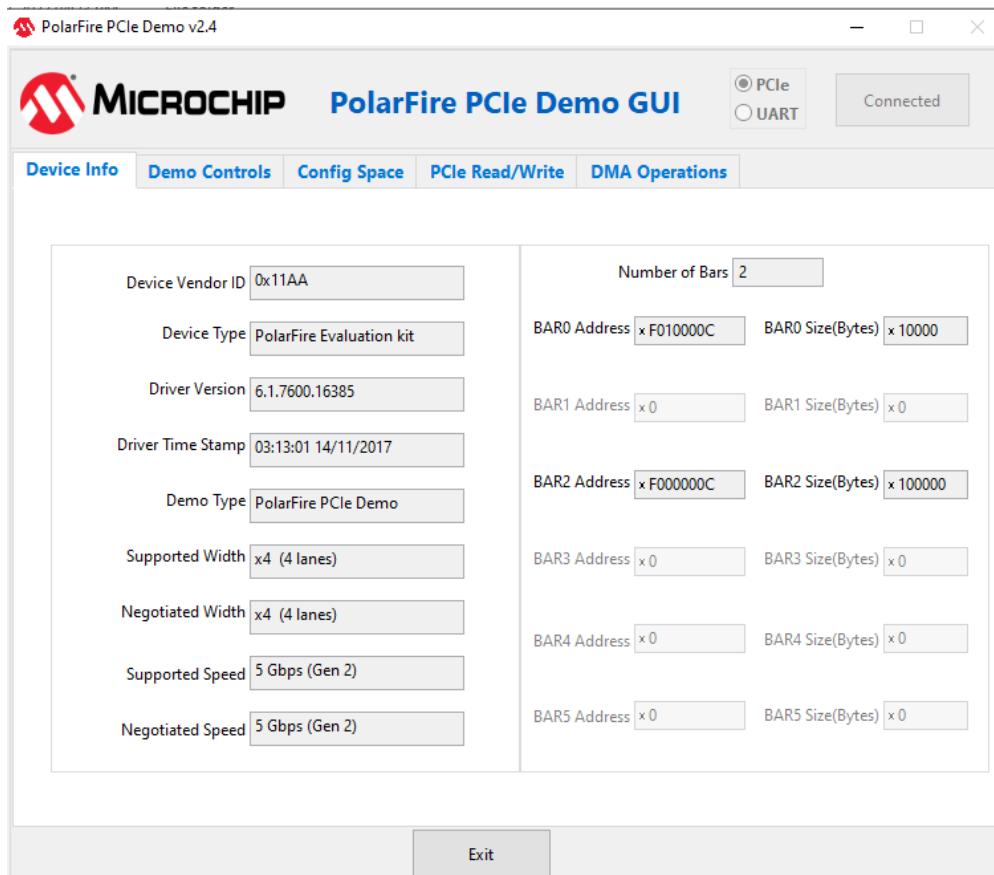
2. Go to All Programs > PolarFire\_PCIE\_GUI > PolarFire\_PCIE\_GUI. The **PolarFire PCIe Demo** window is displayed.

**Figure 3-11. PCIe EndPoint Demo Application**



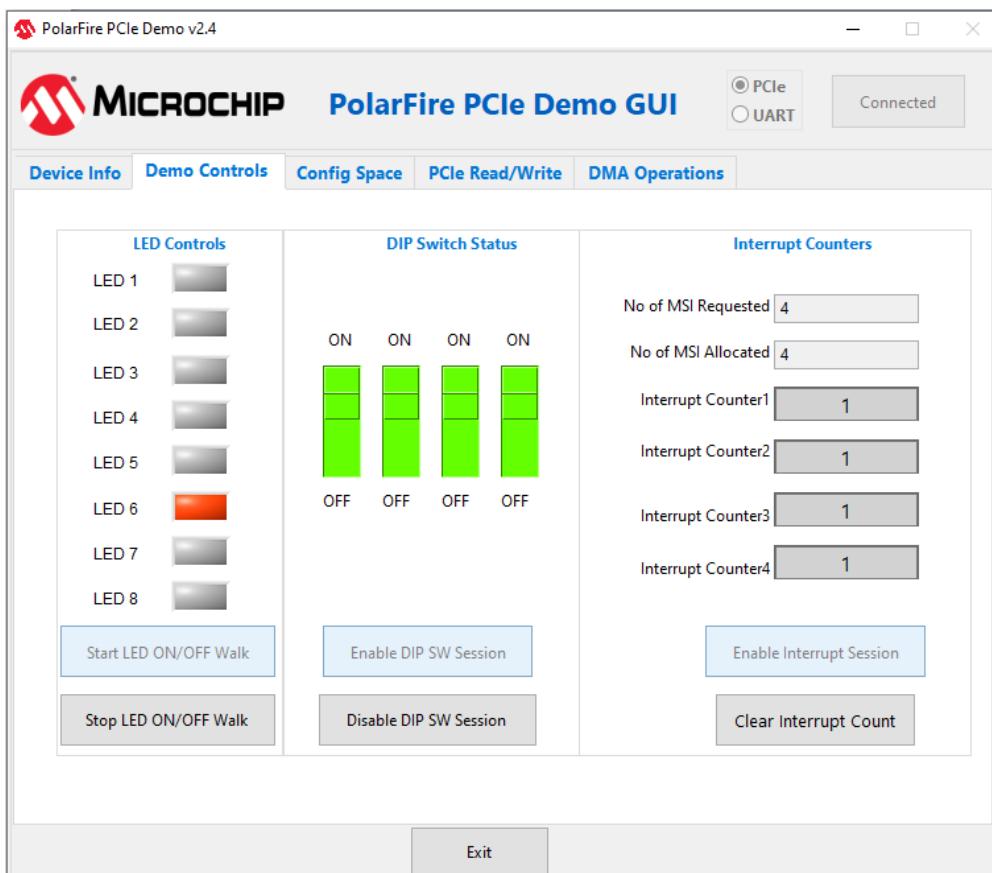
3. Click **Connect**. The application detects and displays the information related to the connected kit, such as Device Vendor ID, Device Type, Driver Version, Driver Time Stamp, Demo Type, Supported Width, Negotiated Width, Supported Speed, Negotiated Speed, Number of Bars, and BAR Address. See the following figure.

**Figure 3-12. Device Info**



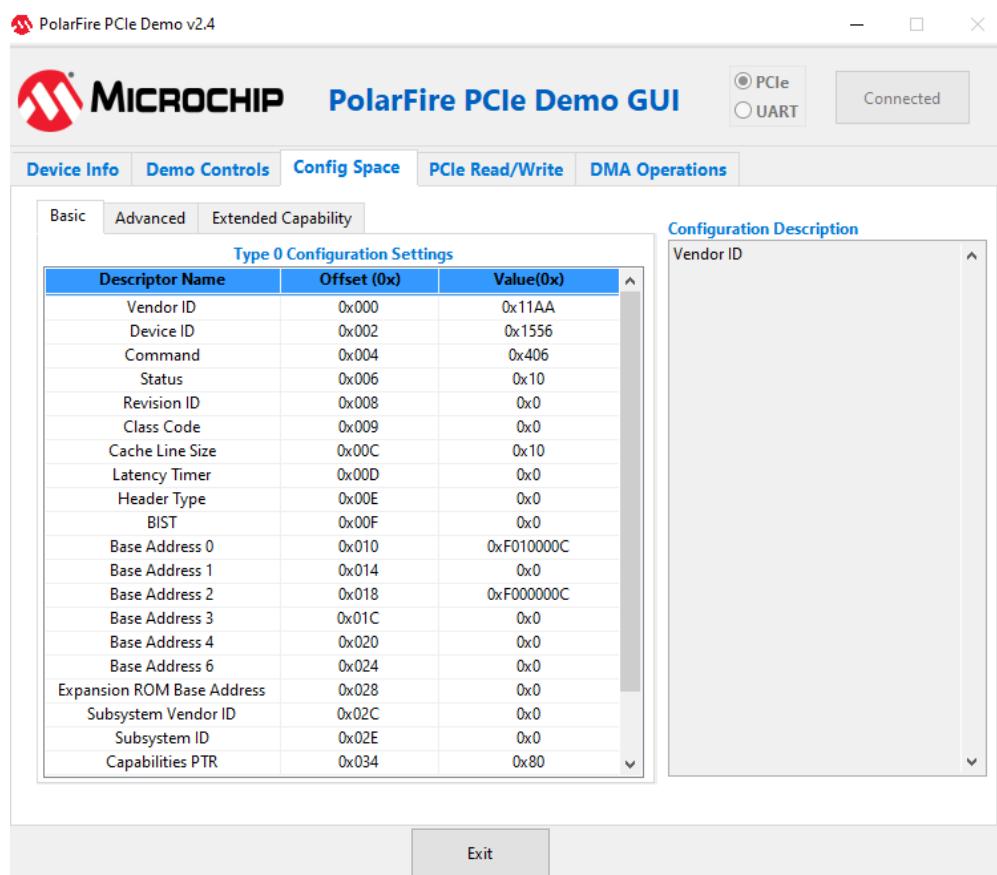
4. Click **Demo Controls** tab to display the **LED Controls**, **DIP Switch Status**, and **Interrupt Counters**.
5. Click **Start LED ON/OFF Walk**, **Enable DIP SW Session**, and **Enable Interrupt Session** to view the controlling LEDs (observe LED4 to LED11 on the PolarFire Evaluation Kit), getting the DIP switch (ON/OFF the DIP1 to DIP4 on the PolarFire Evaluation Kit/Splash Kit) status, and monitoring the interrupts (press SW7 to SW10 on the PolarFire Evaluation Kit and SW3 to SW6 on the PolarFire Splash Kit to generate interrupt) simultaneously. See the following figure.

**Figure 3-13. Demo Controls**



6. Click **Config Space** tab to view the details about the PCIe configuration space. See the following figure.

**Figure 3-14. Config Space**

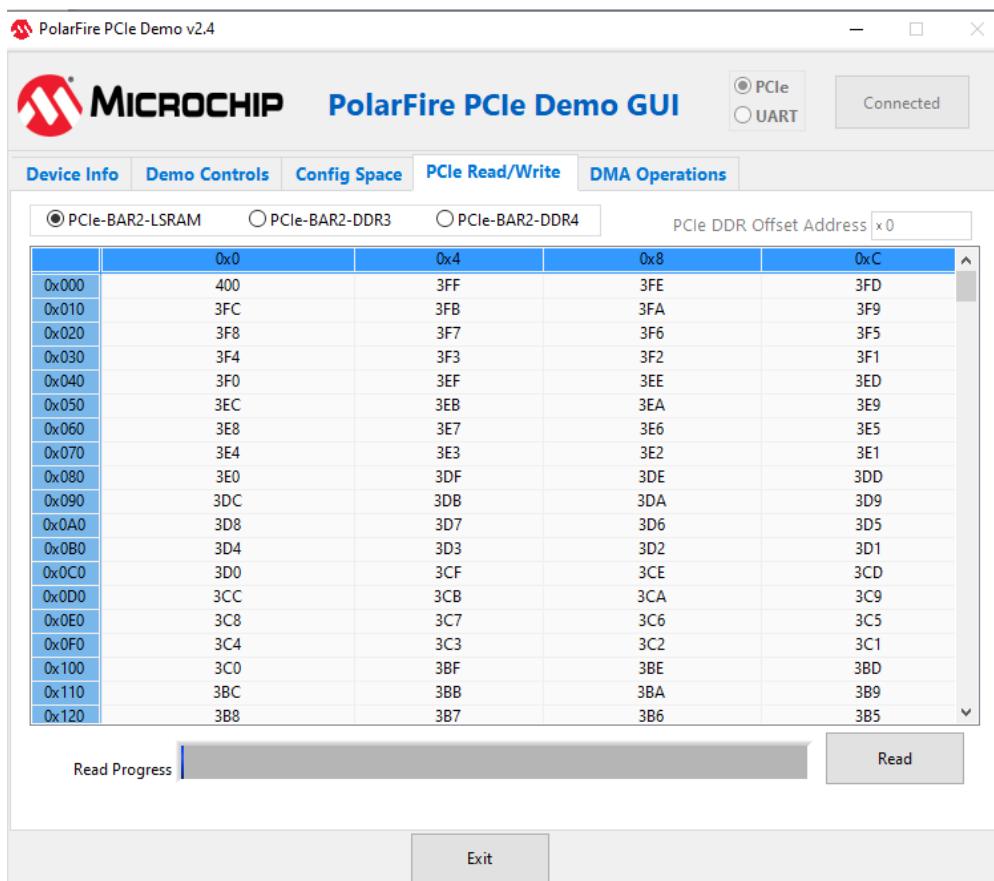


7. Click PCIe Read/Write tab to perform read and write operations to DDR/LSRAM using BAR2 space.
8. Select **LSRAM/DDR3L/DDR4** and then click **Read** to read the 4 KB memory mapped to BAR2 space for DDR and LSRAM. See the following figure.



**Important:** PCIe BAR2-DDR3L is applicable only for Evaluation kit.

Figure 3-15. PCIe BAR2 Memory Access—LSRAM



- Click DMA Operations tab for different DMA operations such as DDR and LSRAM.

**Important:** DDR3L DMA options are not applicable for Splash Kit demo.



### 3.2.3.1 Continuous DMA—Operations

The following instructions describe running DMA operations between PC and DDR3L, PC and DDR4, PC and LSRAM:

- Select one of the following options from the **DMA Transfer Type Selection** drop-down list:
  - PC->DDR3L**—to transfer the data from host PC to PolarFire DDR3L memory
  - DDR3L->PC**—to transfer the data from PolarFire DDR3L memory to host PC
  - Both- PC<->DDR3L**—to transfer the data from host PC to and from PolarFire DDR3L memory
  - PC->DDR4**—to transfer the data from host PC to PolarFire DDR4 memory
  - DDR4->PC**—to transfer the data from PolarFire DDR4 memory to host PC
  - Both PC<->DDR4**—to transfer the data from host PC to and from PolarFire DDR4 memory
  - PC->LSRAM**—to transfer the data from host PC to PolarFire LSRAM memory
  - LSRAM->PC**—to transfer the data from PolarFire LSRAM memory to host PC
  - Both PC<->LSRAM**—to transfer the data from host PC to and from PolarFire LSRAM memory
- Select **Transfer Size** (4 KB to 64 KB) from the drop-down list. The maximum contiguous DMA size is 64 KB because the host PC may not have a contiguous memory of more than 64 KB. For DMA operations that require more than 64 KB, use SGDMA.

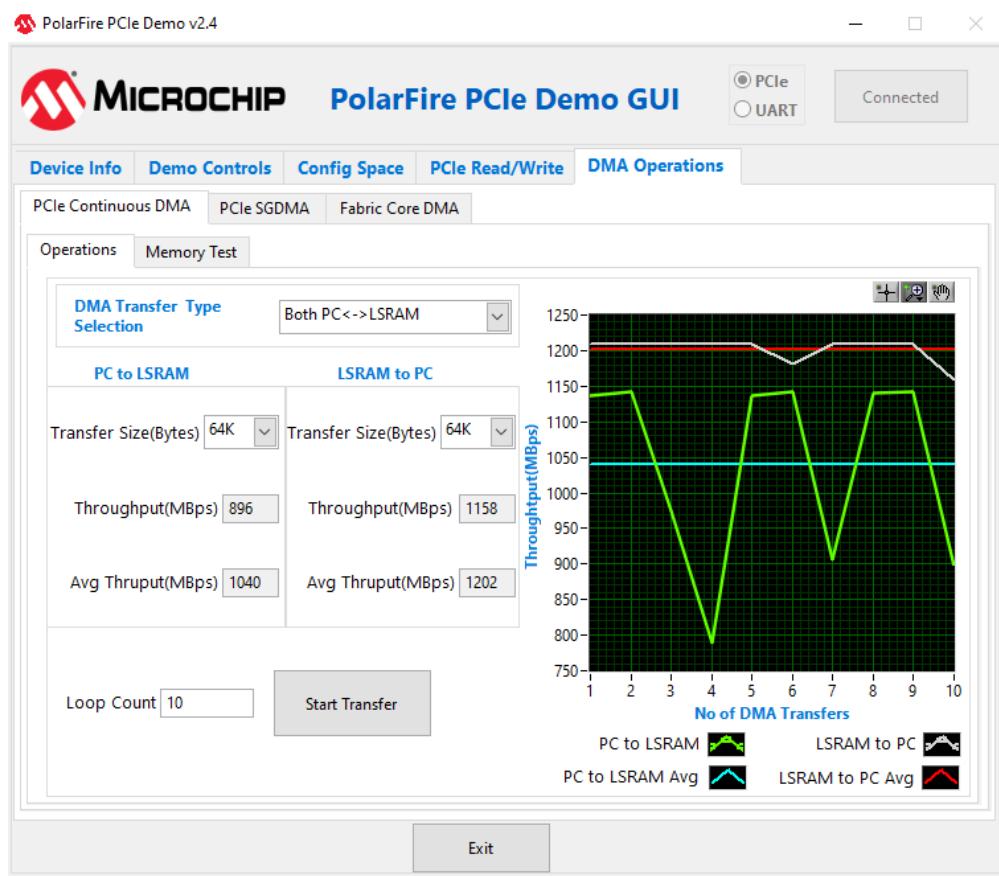
3. Enter the **Loop Count** in the box.
4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps.



**Important:** The AXI LSRAM in the design is configured for 4 KB. This 4 KB is overwritten if more than 4 KB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

The following figure shows the throughput and average throughput in MBps.

**Figure 3-16. Continuous DMA Operations with DMA Transfer Type Selection as Both PC and LSRAM**



### 3.2.3.2 Continuous DMA—Memory Test

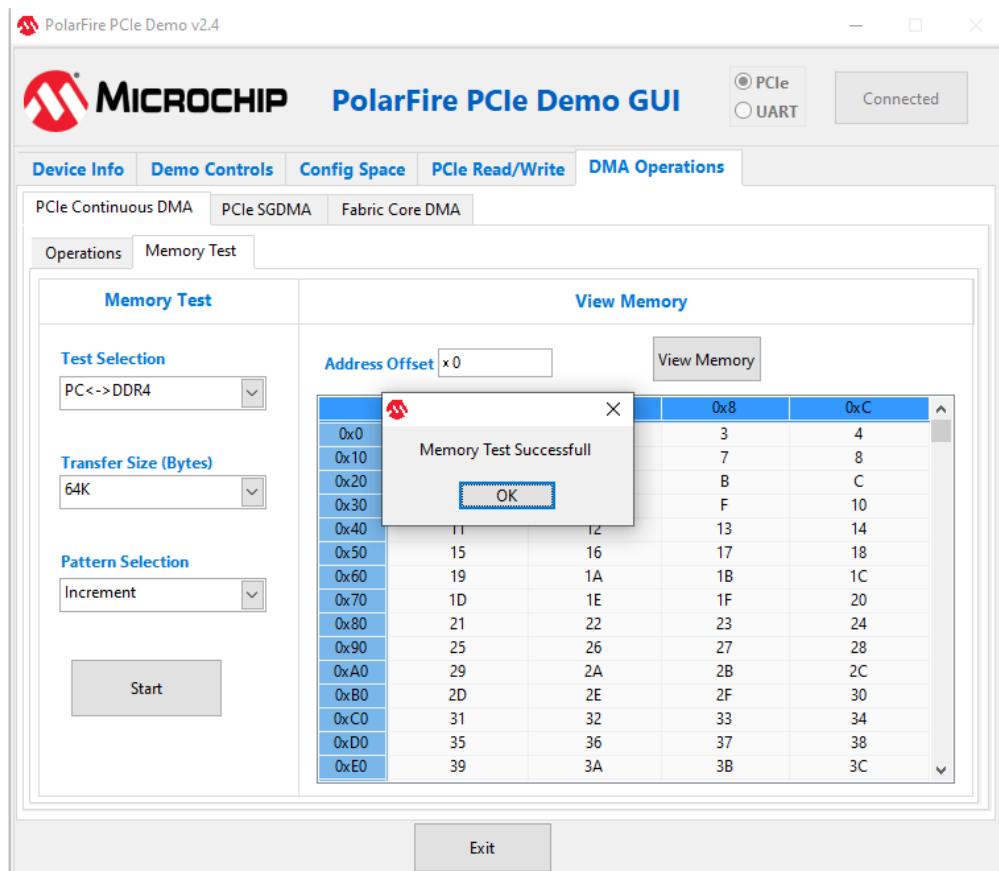
The following instructions describe running **Memory Test** between PC and DDR3L/DDR4/LSRAM:

1. Select one of the following options from the **Test Selection** drop-down list:
  - **PC<->DDR3L**—to transfer the data from host PC to and from PolarFire DDR3L memory
  - **PC<->DDR4**—to transfer the data from host PC to and from PolarFire DDR4 memory
  - **PC<->LSRAM**—to transfer the data from host PC to and from PolarFire LSRAM memory
2. Select **Transfer Size** (4 KB to 64 KB) from the drop-down list.
3. Select **Pattern Selection** from the drop-down list—Increment, Decrement, Random, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's.
4. Click **Start**. GUI performs the following task:
  - The host PC creates a buffer and initializes the memory
  - Initiates the PC to DDR DMA
  - Erases the PC buffer

- Initializes the DDR to PC DMA
- Compares the memory against expected memory

The following figure shows the **Memory Test Successful** window.

**Figure 3-17. Continuous DMA Memory Test—Memory Test Successful**



**Important:** If memory test fails, then GUI displays the first failed memory location.



**Important:** Change the **Offset Address** and click **View Memory** to read the RAM memory content.



### 3.2.3.3 SGDMA—Operations

The following instructions describe running SGDMA operations between PC and DDR3L, PC and DDR4:

1. Select one of the following options from the **DMA Transfer Type** Selection drop-down list:
  - **PC -> DDR3L**—to transfer the data from host PC to PolarFire DDR3L memory
  - **DDR3L-> PC**—to transfer the data from PolarFire DDR3L memory to host PC
  - **Both PC <->DDR3L**—to transfer the data from host PC to and from PolarFire DDR3L memory
  - **PC -> DDR4**—to transfer the data from host PC to PolarFire DDR4 memory
  - **DDR4-> PC**—to transfer the data from PolarFire DDR4 memory to host PC
  - **Both PC <->DDR4**—to transfer the data from host PC to and from PolarFire DDR4 memory

2. Select **Transfer Size** (4 KB to 64 KB) from the drop-down list.
3. Enter the **Loop Count** in the box. The **Buffer Descriptors** show the number of descriptors created by the host driver for each SGDMA operation.
4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in Mbps.

#### 3.2.3.4 SGDMA—Memory Test

The following instructions describe running **Memory Test** between PC and DDR3L/DDR4/LSRAM:

1. Select one of the following options from the **Test Selection** drop-down list:
  - **PC<->DDR3L**—to transfer the data from host PC to and from PolarFire DDR3L memory
  - **PC<->DDR4**—to transfer the data from host PC to and from PolarFire DDR4 memory
2. Select **Transfer Size** (4 KB to 1 MB) from the drop-down list.
3. Select **Pattern Selection** from the drop-down list—Increment, Decrement, Random, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's.
4. Click **Start**. GUI performs the following task:
  - The host PC creates a buffer and initializes the memory
  - Initiates the PC to DDR DMA
  - Erases the PC buffer
  - Initializes the DDR to PC DMA
  - Compares the memory against expected memory

**Memory Test Successful** window appears.

5. Click **OK**.

#### 3.2.3.5 Core DMA—Operations

The following instructions describe running **DMA operations** between LSRAM and DDR3L, LSRAM and DDR4, DDR3L and DDR4:

1. Select one of the following options from the **DMA Transfer Type Selection** drop-down list:
  - **LSRAM > DDR3L**—to transfer the data from LSRAM to PolarFire DDR3L memory
  - **DDR3L-> LSRAM**—to transfer the data from PolarFire DDR3L memory to LSRAM
  - **Both LSRAM <->DDR3L**—to transfer the data from LSRAM to and from PolarFire DDR3L memory
  - **LSRAM > DDR4**—to transfer the data from LSRAM to PolarFire DDR4 memory
  - **DDR4-> LSRAM**—to transfer the data from PolarFire DDR4 memory to LSRAM
  - **Both LSRAM <->DDR4**—to transfer the data from LSRAM to and from PolarFire DDR4 memory
  - **DDR4 -> DDR3L**—to transfer the data from DDR4 to DDR3L memory
  - **DDR3L -> DDR4**—to transfer the data from DDR3L to DDR4 memory
  - **Both DDR4 <-> DDR3L**—to transfer the data from DDR4 to and from DDR3L memory
2. Select **Transfer Size** (4 KB to 1 MB) from the drop-down list.
3. Enter the **Loop Count** in the box.
4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in Mbps.



**Important:** The AXI LSRAM in the design is configured for 4 KB. This 4 KB is overwritten if more than 4 KB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

5. Click **Exit**.

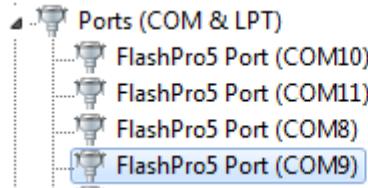
### 3.3

## Running the Demo Through UART

The following steps describe how to run a demo using UART if the host PC PCIe slot is not available:  
Check the **Device Manager** of the host PC for UART ports.

The following figure shows the example of UART ports in the **Device Manager** window.

**Figure 3-18. Device Manager—UART Ports**



The following steps describe how to run the reference design using UART IF:

1. Go to **All Programs > PolarFire\_PCIE\_GUI > PolarFire\_PCIE\_GUI**. The **PolarFire PCIe Demo** window is displayed.
2. Select **UART radio button** and click **Connect**.

The GUI application scans for UART port and after successful connection, displays the DMA Operations UART tab, as shown in [Figure 3-19](#).

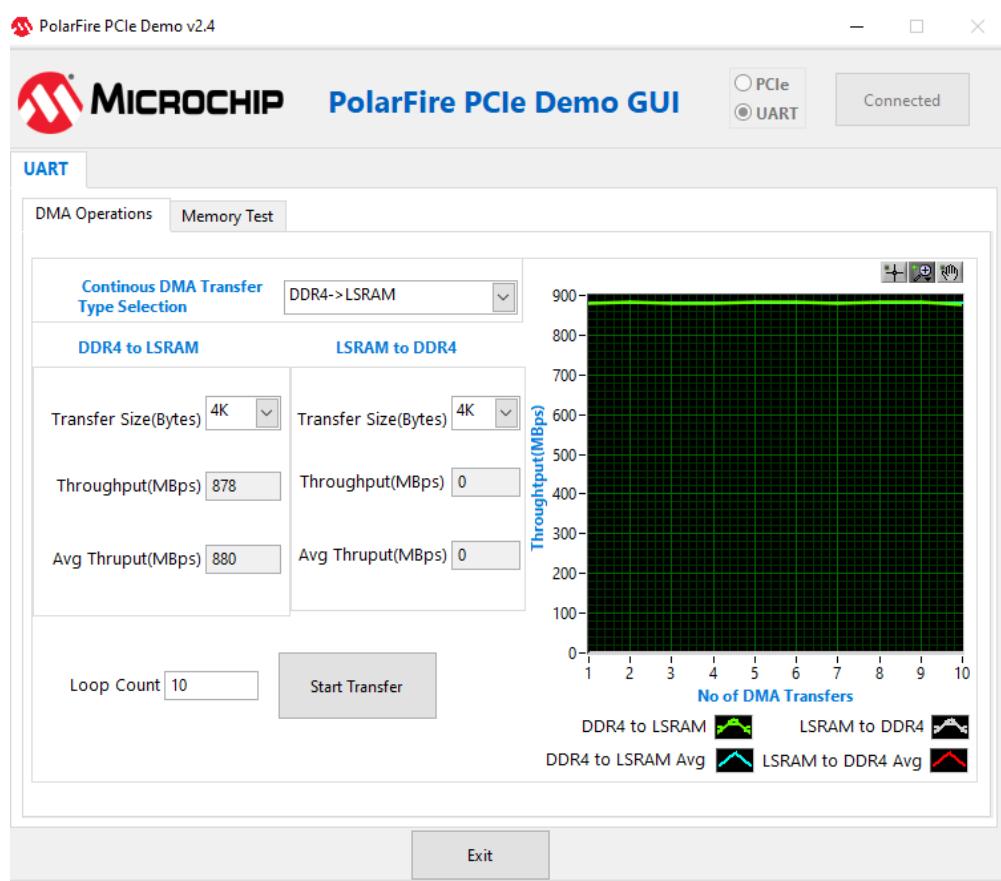
### 3.3.1

## UART—DMA Operations

The following instructions describe the different ways to read data through LSRAM and DDR:

1. Select one of the following options from the **Continuous DMA Transfer Type Selection** drop-down list:
  - **DDR3L -> LSRAM**: To transfer the data from DDR3L to PolarFire LSRAM memory.
  - **LSRAM -> DDR3L**: To transfer the data from PolarFire LSRAM memory to DDR3L.
  - **Both DDR3L <->LSRAM**: To transfer the data from DDR3L to and from PolarFire LSRAM memory.
  - **LSRAM -> DDR4**: To transfer the data from LSRAM to PolarFire DDR4 memory
  - **DDR4-> LSRAM**: To transfer the data from PolarFire DDR4 memory to LSRAM
  - **Both LSRAM <->DDR4**: To transfer the data from LSRAM to and from PolarFire DDR4 memory
  - **DDR4 -> DDR3L**: To transfer the data from DDR4 to DDR3L memory
  - **DDR3L -> DDR4**: To transfer the data from DDR3L to DDR4 memory
  - **Both DDR4 <-> DDR3L**: To transfer the data from DDR4 to and from DDR3L memory
  - **Both DDR3L<->DDR4**: To transfer the data from DDR3L to and from DDR4 memory.
2. Select **Transfer Size** (4 KB to 512 KB) from the drop-down lists.
3. Enter the **Loop Count** in the box.
4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows DMA throughput and average throughput from the DDR memory to the LSRAM.

Figure 3-19. UART—DMA Operations



**Important:** The AXI LSRAM in the design is configured for 4 KB. This 4 KB is over written if more than 4 KB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

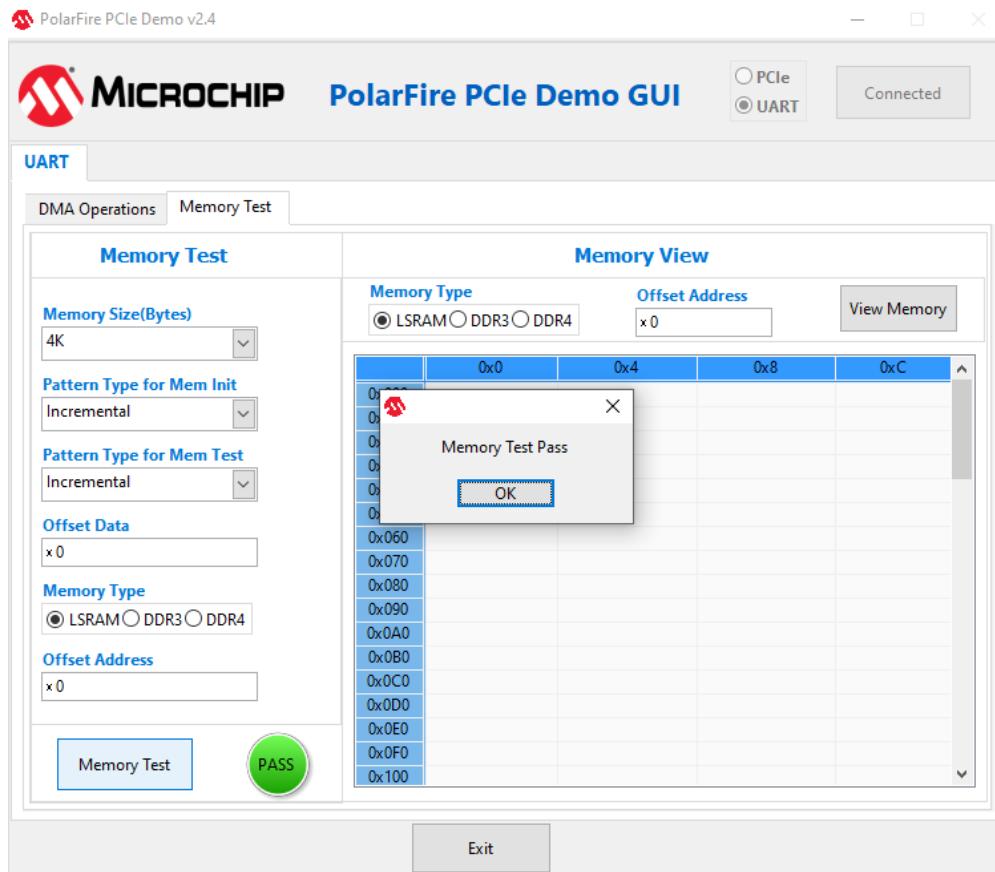
### 3.3.1.1 UART—Memory Test

The following instructions describe running **Memory Test** between PC and DDR3L/DDR4/LSRAM:

1. Select **Transfer Size** (4 KB to 1 MB) from the drop-down list.
2. Select **Pattern Selection** from the drop-down list—Increment, Decrement, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's. For successful Memory test operation, the Patter Type for Mem Init and Patter Type for Mem Test should be same.
3. Click **Memory Test**.
  - GUI sends command to fabric logic to initiate the LSRAM/DDR3L/DDR4 memory
  - GUI sends command to fabric logic to read and compare LSRAM/DDR3L/DDR4 memory

The following figure shows the **UART—Memory Test** tab.

Figure 3-20. UART—Memory Test



**Important:** Change the **Offset Address** and click **View Memory** to read the RAM memory content.

4. Click **View Memory**. It shows 1 KB of RAM memory content.
5. Click **OK**.
6. Click **Exit**.

### 3.3.2 Running the Demo Design on Linux®

The following steps describe how to run the demo design on Linux:

1. Switch **ON** the power supply switch on the PolarFire Evaluation Kit board or PolarFire Splash Kit.
2. Switch **ON** the CentOS Linux Host PC.
3. CentOS Linux Kernel detects the PolarFire Evaluation Kit board or PolarFire Splash Kit PCIe end point as Actel DevicePCIe end point as Actel Device.
4. On Linux Command Prompt, use the `lspci` command to display the PCIe information.  
`# lspci`

**Figure 3-21. PCIe Device Detection**

```
[root@localhost linux_pcie_driver]# lspci
00:00.0 Host bridge: Intel Corporation Xeon E5/Core i7 DMI2 (rev 07)
00:01.0 PCI bridge: Intel Corporation Xeon E5/Core i7 IIO PCI Express Root Port 1a (rev 07)
00:02.0 PCI bridge: Intel Corporation Xeon E5/Core i7 IIO PCI Express Root Port 2a (rev 07)
00:03.0 PCI bridge: Intel Corporation Xeon E5/Core i7 IIO PCI Express Root Port 3a in PCI Express M
00:04.0 System peripheral: Intel Corporation Xeon E5/Core i7 DMA Channel 0 (rev 07)
00:04.1 System peripheral: Intel Corporation Xeon E5/Core i7 DMA Channel 1 (rev 07)
00:04.2 System peripheral: Intel Corporation Xeon E5/Core i7 DMA Channel 2 (rev 07)
00:04.3 System peripheral: Intel Corporation Xeon E5/Core i7 DMA Channel 3 (rev 07)
00:04.4 System peripheral: Intel Corporation Xeon E5/Core i7 DMA Channel 4 (rev 07)
00:04.5 System peripheral: Intel Corporation Xeon E5/Core i7 DMA Channel 5 (rev 07)
00:04.6 System peripheral: Intel Corporation Xeon E5/Core i7 DMA Channel 6 (rev 07)
00:04.7 System peripheral: Intel Corporation Xeon E5/Core i7 DMA Channel 7 (rev 07)
00:05.0 System peripheral: Intel Corporation Xeon E5/Core i7 Address Map, VTd_Misc, System Manageme
00:05.2 System peripheral: Intel Corporation Xeon E5/Core i7 Control Status and Global Errors (rev
00:05.4 PIC: Intel Corporation Xeon E5/Core i7 I/O APIC (rev 07)
00:11.0 PCI bridge: Intel Corporation C600/X79 series chipset PCI Express Virtual Root Port (rev 05
00:16.0 Communication controller: Intel Corporation C600/X79 series chipset MEI Controller #1 (rev
00:16.2 IDE interface: Intel Corporation C600/X79 series chipset IDE-r Controller (rev 05)
00:16.3 Serial controller: Intel Corporation C600/X79 series chipset KT Controller (rev 05)
00:19.0 Ethernet controller: Intel Corporation 82579LM Gigabit Network Connection (Lewisville) (rev
00:1a.0 USB controller: Intel Corporation C600/X79 series chipset USB2 Enhanced Host Controller #2
00:1b.0 Audio device: Intel Corporation C600/X79 series chipset High Definition Audio Controller (r
00:1c.0 PCI bridge: Intel Corporation C600/X79 series chipset PCI Express Root Port 2 (rev b5)
00:1c.5 PCI bridge: Intel Corporation C600/X79 series chipset PCI Express Root Port 5 (rev b5)
00:1c.6 PCI bridge: Intel Corporation C600/X79 series chipset PCI Express Root Port 3 (rev b5)
00:1c.7 PCI bridge: Intel Corporation C600/X79 series chipset PCI Express Root Port 4 (rev b5)
00:1d.0 USB controller: Intel Corporation C600/X79 series chipset USB2 Enhanced Host Controller #1
00:1e.0 PCI bridge: Intel Corporation 82801 PCI Bridge (rev a5)
00:1f.0 ISA bridge: Intel Corporation C600/X79 series chipset LPC Controller (rev 05)
00:1f.2 RAID bus controller: Intel Corporation C600/X79 series chipset SATA RAID Controller (rev 05
00:1f.3 SMBus: Intel Corporation C600/X79 series chipset SMBus Host Controller (rev 05)
02:00.0 Serial Attached SCSI controller: Intel Corporation C602 chipset 4-Port SATA Storage Control
04:00.0 Non-VGA unclassified device: Actel Device 1556
05:00.0 VGA compatible controller: NVIDIA Corporation GK107GL [Quadro K600] (rev a1)
```

### 3.3.2.1 Drivers Installation

Enter the following commands in the Linux command prompt to install the PCIe drivers:

1. Change to g5\_endpoint\_driver directory by using the following command:  
`#cd <source_code_directory>/mpf_an4597_v2022p1_df\PCIe_Drivers\Linux_PCIE_Drivers`
2. Enter the make command on Linux Command Prompt to compile the Linux PCIe device driver code.  
`#make clean [To clean any *.o, *.ko files]`  
`#make`
3. The kernel module **mpci.ko** is created in the same directory.
4. Enter insmod command to insert the Linux PCIe device driver as a module.  
`#insmod mpc.ko`



**Important:** Root privileges are required to execute this command.

**Figure 3-22. PCIe Device Driver Installation**

```
[root@localhost linux_pcie_driver]# make
make -W -Wall -Wstrict-prototypes -Wmissing-prototypes -C /lib/modules/3.10.0-1062.7.1.el7.x86_64/build SUBDIRS=/root/linux_pcie_driver modules
make[1]: Entering directory `/usr/src/kernels/3.10.0-1062.7.1.el7.x86_64'
  CC [M]  /root/linux_pcie_driver/mpcie.o
  CC [M]  /root/linux_pcie_driver/mdma.o
  CC [M]  /root/linux_pcie_driver/misrdpc.o
  LD [M]  /root/linux_pcie_driver/mpci.o
Building modules, stage 2.
MODPOST 1 modules
  CC      /root/linux_pcie_driver/mpci.mod.o
  LD [M]  /root/linux_pcie_driver/mpci.ko
make[1]: Leaving directory `/usr/src/kernels/3.10.0-1062.7.1.el7.x86_64'
[root@localhost linux_pcie_driver]# insmod mpcl.ko
[root@localhost linux_pcie_driver]# ls /dev/MS_PCI_DEV
/dev/MS_PCI_DEV
```

### 3.3.2.1.1 Linux PCIe Application Compilation

1. Compile the Linux user space application as follows:

```
#cd <source_code_directory>/mpf_an4597_v2022p1_df\PCIe_Drivers\Linux_PCIE_Drivers
# make clean
# make all
```

After successful compilation, Linux PCIe application utility pcie\_app creates in the same directory.

2. On Linux Command Prompt, run the pcie\_app utility as:

```
#./pcie_app
```

The following figure shows the displayed **Help** menu.

**Figure 3-23. Linux PCIe Application Utility**

```
[root@localhost linux_pcie_app]# ls
Makefile pcie_appln_dma.c pcie_appln.h pcie_appln_main.c
[root@localhost linux_pcie_app]# make
gcc -c pcie_appln_main.c -o pcie_appln_main.o
gcc -c pcie_appln_dma.c -o pcie_appln_dma.o
gcc pcie_appln_main.o pcie_appln_dma.o -Wall -lm -o pcie_app
[root@localhost linux_pcie_app]# ls
Makefile pcie_app pcie_appln_dma.c pcie_appln_dma.o pcie_appln.h pcie_appln_main.c pcie_appln_main.o
[root@localhost linux_pcie_app]# ./pcie_app
welcome to PCI Demo
-----
PCI Device [/dev/MS_PCI_DEV] opened
1. Device info
2. Blink LEDs
3. Dip switch status
4. For Interrupt
5. Read/Write to bars space
6. PCIe configSpace information
7. PCIe DMA operation
```

### 3.3.2.1.2 Device Information

Enter 1 to get device information.

**Figure 3-24. Device Information**

```
-----  
PCI Device [/dev/MS_PCI_DEV] opened  
1. Device info  
2. Blink LEDs  
3. Dip switch status  
4. For Interrupt  
5. Read/Write to bars space  
6. PCIe configSpace information  
7. PCIe DMA operation  
1  
  
demo_type = PolarFire PCIe Demo  
device_status = Microsemi Device Detected  
device_type = PolarFire Evaluation kit  
number of BARs enabled = 2  
bar0_add = 0xe2b0000c  
bar0_size = 10000  
bar2_add = 0xe2a0000c  
bar2_size = 100000
```



**Important:** PCI device enumeration takes place during the boot time and base address register starting address will not be the same for every boot.

### 3.3.2.1.3 Blink LEDs

Enter 2 to blink leds.

**Figure 3-25. Blink LEDs**

```
1. Device info  
2. Blink LEDs  
3. Dip switch status  
4. For Interrupt  
5. Read/Write to bars space  
6. PCIe configSpace information  
7. PCIe DMA operation  
2  
-----  
Enter Led data  
55  
Blink LEDs success
```

### 3.3.2.1.4 DIP Switch Status

Enter 3 to get dip switch status.

**Figure 3-26. Dip Switch Status**

1. Device info
2. Blink LEDs
3. Dip switch status
4. For Interrupt
5. Read/Write to bars space
6. PCIe configSpace information
7. PCIe DMA operation

3

Blink LEDs success

SW1 : ON  
SW2 : ON  
SW3 : ON  
SW4 : ON

#### **3.3.2.1.5 For Interrupt**

Enter **4**, then enter **1** for interrupt count or **2** for clear.

**Figure 3-27. For Interrupt**

```
1. Device info  
2. Blink LEDs  
3. Dip switch status  
4. For Interrupt  
5. Read/Write to bars space  
6. PCIe configSpace information  
7. PCIe DMA operation  
4  
-----  
1. for ISR count, 2. for ISR clean  
1  
counter 1 = 0  
counter 2 = 0  
counter 3 = 0  
counter 4 = 0  
  
1. Device info  
2. Blink LEDs  
3. Dip switch status  
4. For Interrupt  
5. Read/Write to bars space  
6. PCIe configSpace information  
7. PCIe DMA operation  
4  
-----  
1. for ISR count, 2. for ISR clean  
1  
counter 1 = 0  
counter 2 = 0  
counter 3 = 0  
counter 4 = 1  
  
1. Device info  
2. Blink LEDs  
3. Dip switch status  
4. For Interrupt  
5. Read/Write to bars space  
6. PCIe configSpace information  
7. PCIe DMA operation  
4  
-----  
1. for ISR count, 2. for ISR clean  
2  
counter 1 = 0  
counter 2 = 0  
counter 3 = 0  
counter 4 = 0
```

### 3.3.2.1.6 For Read/Write to Bar Space

Enter **5** to read or write to bar space.

**Figure 3-28. For Bar Read/Write**

1. Device info
2. Blink LEDs
3. Dip switch status
4. For Interrupt
5. Read/Write to bars space
6. PCIe configSpace information
7. PCIe DMA operation

5

-----  
provide type 1.DDR-3, 2.LSRAM,3.DDR-4  
1

1. Read from bar space
  2. Write to bar space
- 2  
Enter the offset  
0x10  
Provide the data to write  
0x0a  
Write successful

1. Device info
2. Blink LEDs
3. Dip switch status
4. For Interrupt
5. Read/Write to bars space
6. PCIe configSpace information
7. PCIe DMA operation

5

-----  
provide type 1.DDR-3, 2.LSRAM,3.DDR-4

- 1  
1. Read from bar space  
2. Write to bar space  
1  
Enter the offset  
0x10  
read value = 0xa

### 3.3.2.1.7 For PCIe configspace

Enter **6**, then enter **2** for full PCIe configuration read.

**Figure 3-29. For PCIe configspace**

```
1. Device info  
2. Blink LEDs  
3. Dip switch status  
4. For Interrupt  
5. Read/Write to bars space  
6. PCIe configSpace information  
7. PCIe DMA operation  
6  
-----  
1.Read from PCIe ConfigSpace offset  
2.Read PCIe ConfigSpace  
2  
Vendor ID: 0x11aa  
Device ID: 0x1556  
Cmd Reg: 0x506  
Stat Reg: 0x10  
Revision ID: 0x0  
Class Prog: 0x0  
Device Class: 0x0  
Cache Line Size: 0x10  
Latency Timer: 0x0  
Header Type: 0x0  
BIST: 0x0  
BAR0: Addr:0xe2b0000c  
BAR1: Addr:0x0  
BAR2: Addr:0xe2a0000c  
BAR3: Addr:0x0  
BAR4: Addr:0x0  
BAR5: Addr:0x0  
CardBus CIS Pointer: 0x0  
Subsystem Vendor ID: 0x0  
Subsystem Device ID: 0x0  
Expansion ROM Base Address: 0x0  
IRQ Line: 0x3  
IRQ Pin: 0x4  
Min Gnt: 0x0  
Max Lat: 0x0  
MSIEnable: 0x1  
MultipleMessageCapable: 0x4  
MultipleMessageEnable: 0x4  
CapableOf64Bits: 0x1  
PerVectorMaskCapable: 0x0
```

### 3.3.2.1.8 For PCIe DMA Operation

Enter 7 for PCIe DMA operation.

- Maximum transfer length is 4k < transfer length < 1 MB.
- For DDR3L/4 maximum transfer length is 4k < transfer length < 1 MB.

- For LSRAM maximum transfer length is 4k < transfer length < 64 kB.

**Figure 3-30. For DMA Operation**

```

1. Device info
2. Blink LEDs
3. Dip switch status
4. For Interrupt
5. Read/Write to bars space
6. PCIe configSpace information
7. PCIe DMA operation
7
-----
```

```

Read/write to memory using DMA
-----
1. G5 Continuous Dma Write to DDR3
2. G5 Continuous Dma Read from DDR3
3. G5 Continuous Dma write/read DDR3
4. G5 Continuous Dma Write to DDR4
5. G5 Continuous Dma Read from DDR4
6. G5 Continuous Dma write/read DDR4
7. G5 Continuous Dma Write to LSRAM
8. G5 Continuous Dma Read from LSRAM
9. G5 Continuous Dma write/read LSRAM
10. G5 SG Dma Write to DDR3
11. G5 SG Dma Read from DDR3
12. G5 SG Dma write/read DDR3
13. G5 SG Dma Write to DDR4
14. G5 SG Dma Read from DDR4
15. G5 SG Dma write/read DDR4
```

Enter 3 for Continuous DMA write/read DDR3L.

**Figure 3-31. For Continuous DMA Write/Read DDR3L**

```

3
Tx size
4096
Rx size
4096
Enter the data pattern 1.inc 2. dec 3.rand 4.zero's 5.one's 6. AAA 7. 555
1
Write throughput = 648 MBPS
Read throughput = 412 MBPS
```

## 3.4 Throughput Summary of Evaluation Kit

The following tables list the throughput values observed.

**Table 3-1. PolarFire Throughput Summary—PCIe Continuous DMA Mode**

DMA Transfer Type	DMA Size	Throughput (MBps)	Average Throughput (MBps)
PC to LSRAM	64K	1091	1069
LSRAM to PC		1104	1147
Both PC to and from LSRAM		1124/1154	1093/1149

.....continued

DMA Transfer Type	DMA Size	Throughput (MBps)	Average Throughput (MBps)
PC to DDR4	64K	998	970
DDR4 to PC		523 <sup>1</sup>	523
Both PC to and from DDR4		998/523	972/523
PC to DDR3L	64K	468	460
DDR3L to PC		327 <sup>1</sup>	327
Both PC to and from DDR3L		468/327	465/327



**Important:**

1. The PCIe DMA performs maximum of 32 beat AXI burst transactions (not AXI4's maximum of 256 beat), which causes low read performance of DDR3L/DDR4.

**Table 3-2. PolarFire Throughput Summary—PCIe SGDMA Mode**

DMA Transfer Type	DMA Size	Throughput (MBps)	Average Throughput (MBps)
PC to DDR4	1 MB	986	984
DDR4 to PC		524 <sup>1</sup>	524
Both PC to and from DDR4		986/524	980/524
PC to DDR3L	1 MB	469	472
DDR3L to PC		325 <sup>1</sup>	325
Both PC to and from DDR3L		473/325	473/325



**Important:**

1. The PCIe DMA performs maximum of 32 beat AXI burst transactions (not maximum of 256 beat of AXI4), which causes low read performance of DDR3L/DDR4.

**Table 3-3. PolarFire Throughput Summary—Fabric Core DMA Mode**

DMA Transfer Type	DMA Size	Throughput (MBps)	Average Throughput (MBps)
LSRAM to DDR4	1 MB	1470	1470
DDR4 to LSRAM		1245	1245
Both LSRAM to and from DDR4		1470/1245	1470/1245
LSRAM to DDR3L	1 MB	574	574
DDR3L to LSRAM		553	553
Both LSRAM to and from DDR3L		574/554	574/554
DDR4 to DDR3L	1 MB	574	574
DDR3L to DDR4		553	553
Both DDR4 to and from DDR3L		574/553	574/553



**Important:** DDR3L throughput is less due to the AXI interconnect CDC path limitation.

### 3.5

### Throughput Summary of Splash Kit

The following table lists the throughput values observed.

**Table 3-4. PolarFire Throughput Summary—PCIe Continuous DMA Mode**

DMA Transfer Type	DMA Size	Throughput (MBps)	Average Throughput (MBps)
PC to LSRAM	64K	1268	1270
LSRAM to PC		1156	1156
Both PC to and from LSRAM		1271/1145	1236/1152
PC to DDR4	64K	1050	1187
DDR4 to PC		527 <sup>1</sup>	527
Both PC to and from DDR4		1242/528	1231/528



**Important:**

1. The PCIe DMA performs maximum of 32 beat AXI burst transactions (not maximum of 256 beat of AXI4), which causes low read performance of DDR4.

**Table 3-5. PolarFire Throughput Summary—PCIe SGDMA Mode**

DMA Transfer Type	DMA Size	Throughput (MBps)	Average Throughput (MBps)
PC to DDR4	1 MB	1215	1201
DDR4 to PC		528 <sup>1</sup>	528
Both PC to and from DDR4		1216/528	1207/528



**Important:**

1. The PCIe DMA performs maximum of 32 beat AXI burst transactions (not AXI4's maximum of 256 beat), which causes low read performance of DDR4.

**Table 3-6. PolarFire Throughput Summary—Fabric Core DMA Mode**

DMA Transfer Type	DMA Size	Throughput (MBps)	Average Throughput (MBps)
DDR4 to LSRAM	1 MB	1259	1258
LSRAM to DDR4		1470	1470
Both LSRAM to and from DDR4		1257/1470	1258/1470

## 4. Appendix 1: DDR3L and DDR4 Power Measurement

### 4.1 DDR3L

The PolarFire Evaluation Kit board has a current sense resistor (R118) for 1.5V power rail. Measure the voltage across the R118 using test points TP134 and TP135 and use the following equations to get the DDR3L power. This measurement includes PolarFire DDR3L IO power consumption and actual Micron DDR3L memory power consumption.

$$\text{Current (mA)} = \frac{\text{Measure voltage(mV)}}{R}$$

$$\text{Power (mW)} = \text{Current} \times \text{Voltage}$$

While running the demo, the measured voltage across R118 is 6.3 mV and resistor value is  $0.01\Omega$ .

$$\text{Current (mA)} = 6.3 \div 0.01 = 630 \text{ mA}$$

$$\text{Power} = 630 \times 1.5 = 945 \text{ MW}$$

### 4.2 DDR4

The PolarFire Evaluation Kit board has a current sense resistor (R222) for 1.2V power rail. Measure the voltage across the R222 using test points TP132 and TP133 and use the following equations to get the DDR4 power. This measurement includes PolarFire DDR4 IO power consumption and actual Micron DDR4 memory power consumption.

$$\text{Current (mA)} = \frac{\text{Measure voltage(mV)}}{R}$$

$$\text{Power (mW)} = \text{Current} \times \text{Voltage}$$

While running the demo, the measured voltage across R222 is 2.4 mV and resistor value is  $0.01\Omega$ .

$$\text{Current (mA)} = 2.4 \div 0.01 = 240 \text{ mA}$$

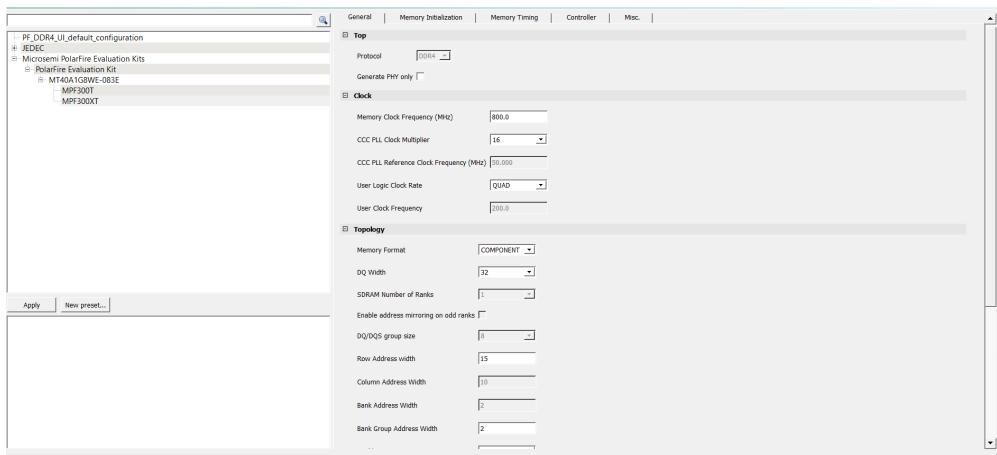
$$\text{Power} = 240 \times 1.2 = 288 \text{ MW}$$

## 5. Appendix 2: DDR4 Configuration

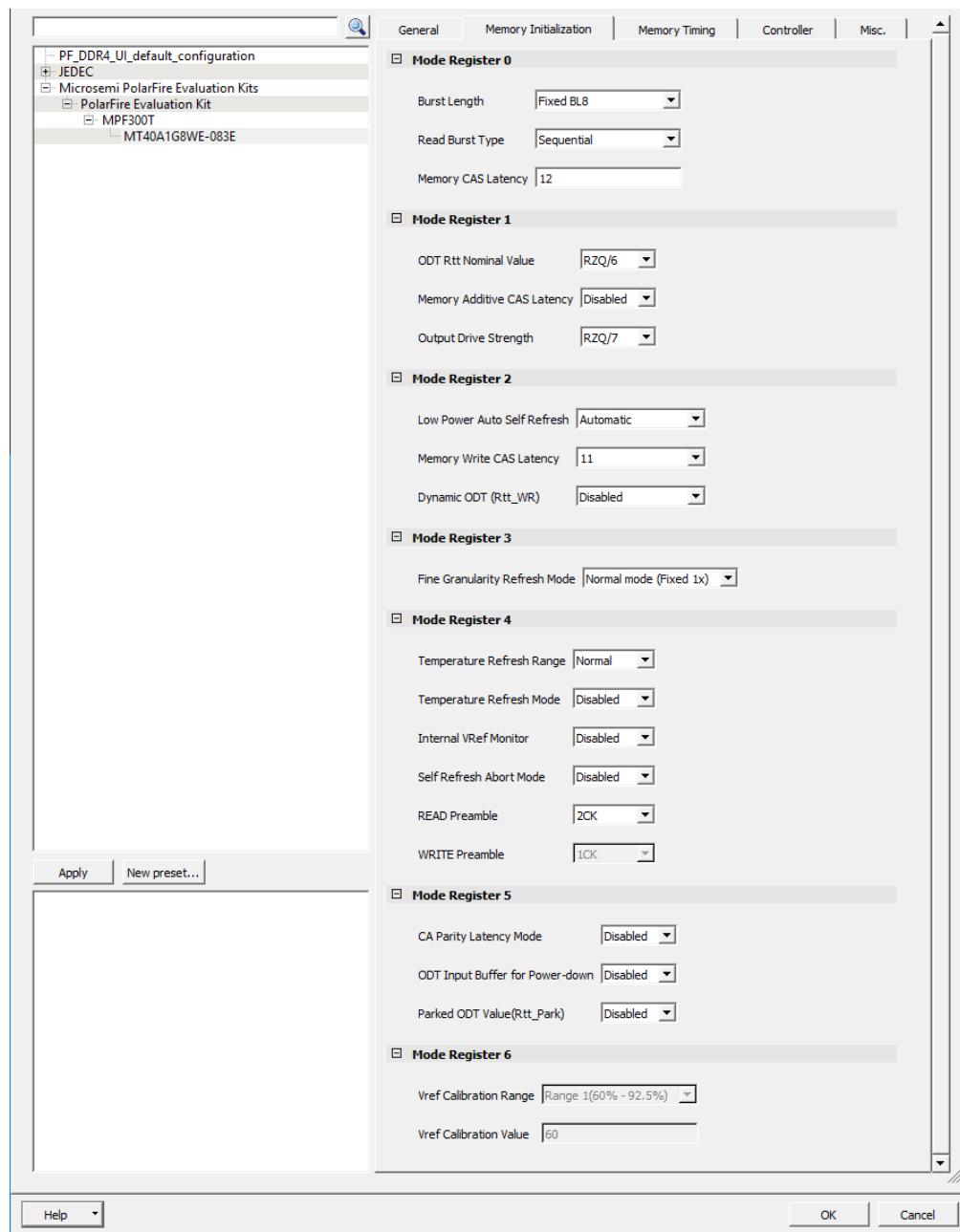
The DDR4 subsystem is configured to access the 32-bit DDR4 memory through an AXI4 64-bit interface. The DDR4 memory initialization and timing parameters are configured, as per the DDR4 memory on the PolarFire Evaluation kit.

The following figures show general configuration settings for the DDR4 memory.

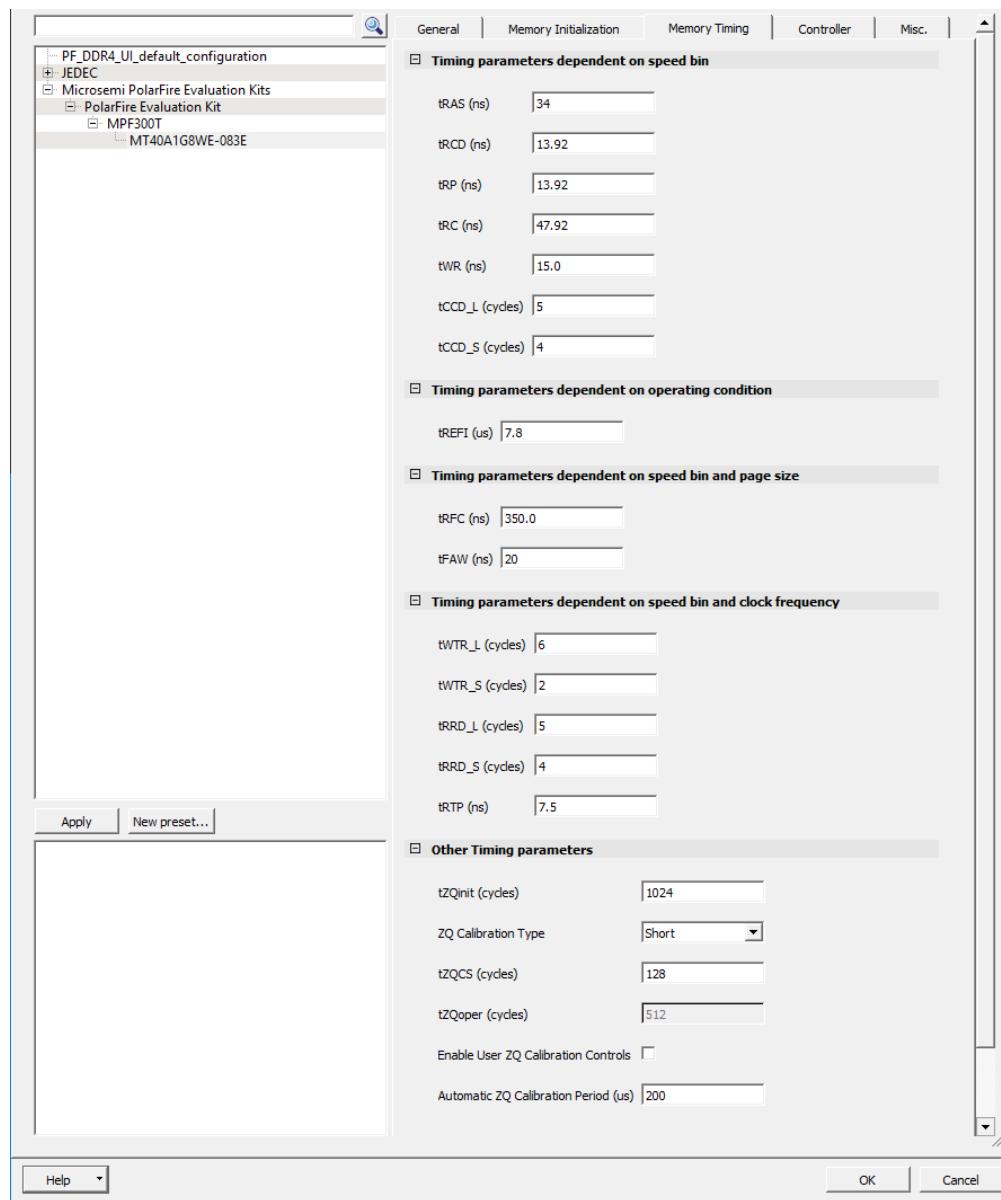
**Figure 5-1. DDR4 Configurator**



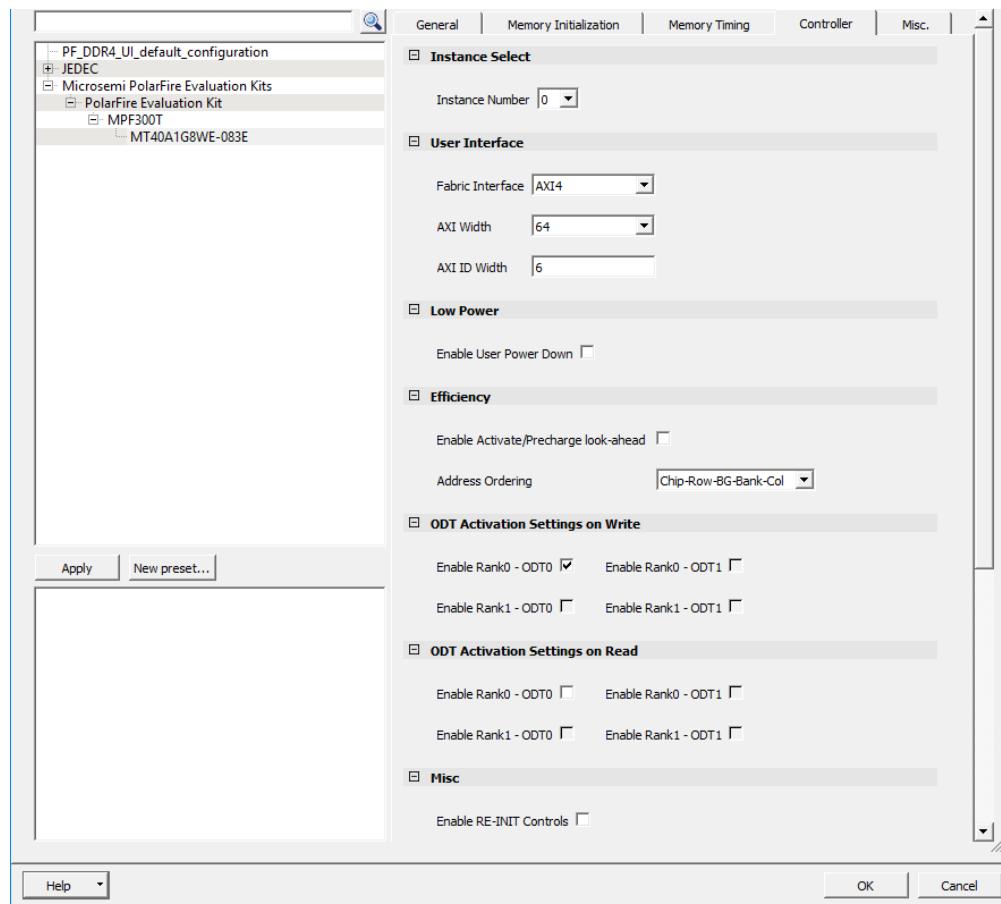
The following figure shows initialization configuration settings for the DDR4 memory.

**Figure 5-2. DDR4 Configurator—Memory Initialization**

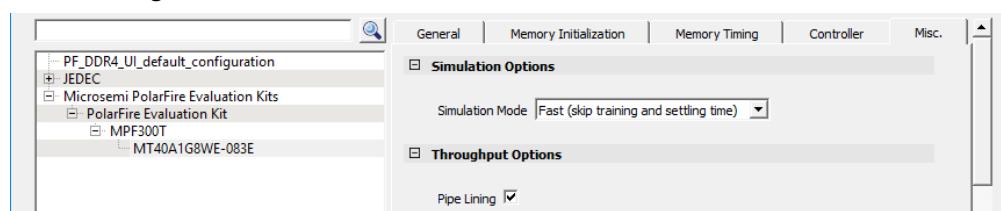
The following figure shows timing configuration settings for the DDR4 memory.

**Figure 5-3. DDR4 Configurator—Memory Timing**

The following figure shows controller configuration settings for the DDR4 memory.

**Figure 5-4. DDR4 Configurator—Controller**

The following figure shows miscellaneous configuration settings for the DDR4 memory.

**Figure 5-5. DDR4 Configurator—Misc**

## 6. Appendix 3: Programming the Device Using FlashPro Express

This section describes how to program the PolarFire device with the .job programming file using FlashPro Express. The .job file is available at the following design files folder location:

```
mpf_an4597_v2022p1_df\Programming_Job
```

To program the device, perform the following steps:

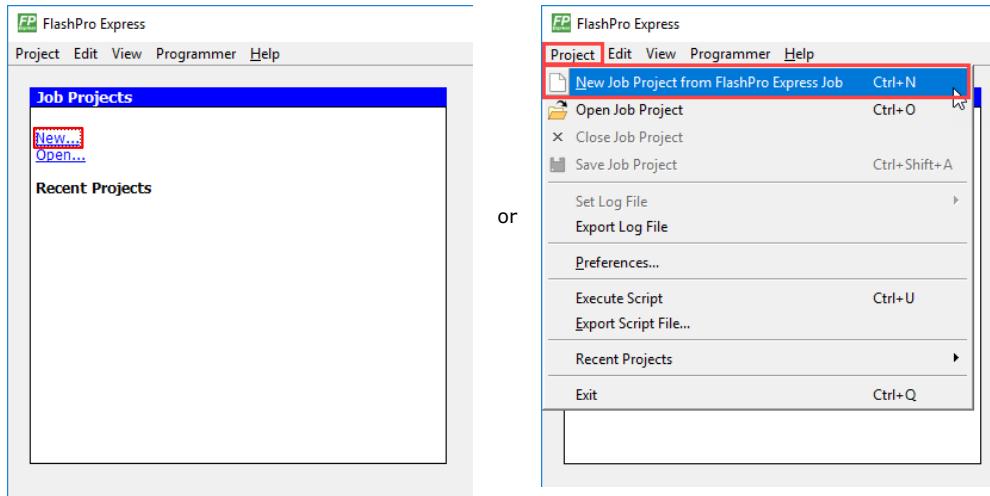
1. Ensure that the jumper settings on the board are the same as listed in [Table 2-3](#) (for evaluation) and [Table 2-4](#) (for splash).



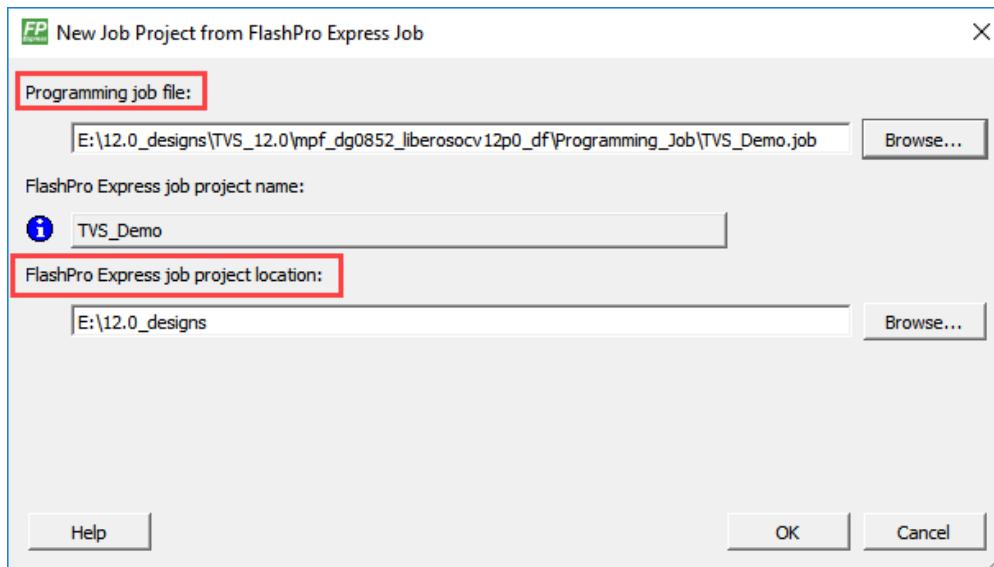
**Important:** The power supply switch must be switched off while making the jumper connections.

2. Connect the power supply cable to the J9 connector on the Evaluation board or J2 connector on the Splash board.
3. Connect the USB cable from the Host PC to the J5 (FTDI port) on the Evaluation board or J1 (FTDI port) on the Splash board.
4. Power on the board using the SW3 slide switch on the Evaluation board or SW1 slide switch on the Evaluation board.
5. On the host PC, launch the **FlashPro Express** software.
6. To create a new job, click **New** or in the **Project** menu, select **New Job Project from FlashPro Express Job**.

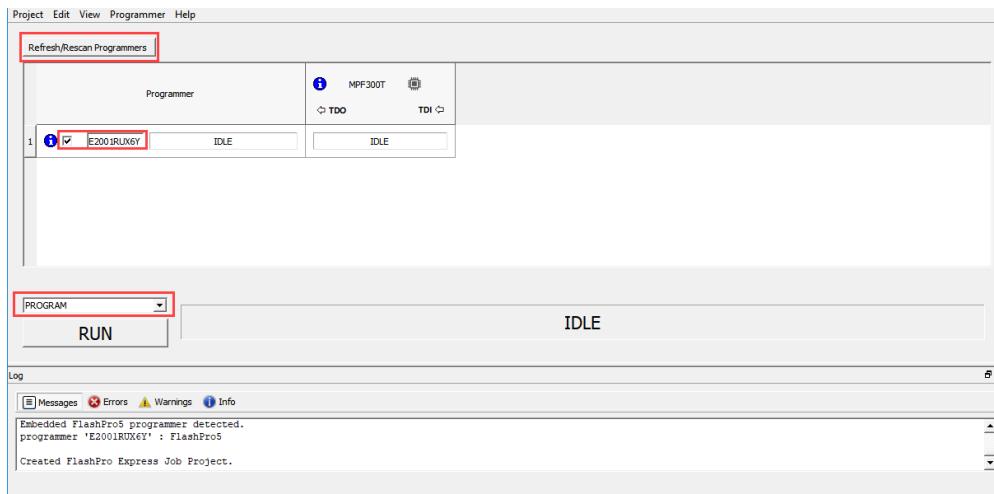
**Figure 6-1. FlashPro Express Job Project**



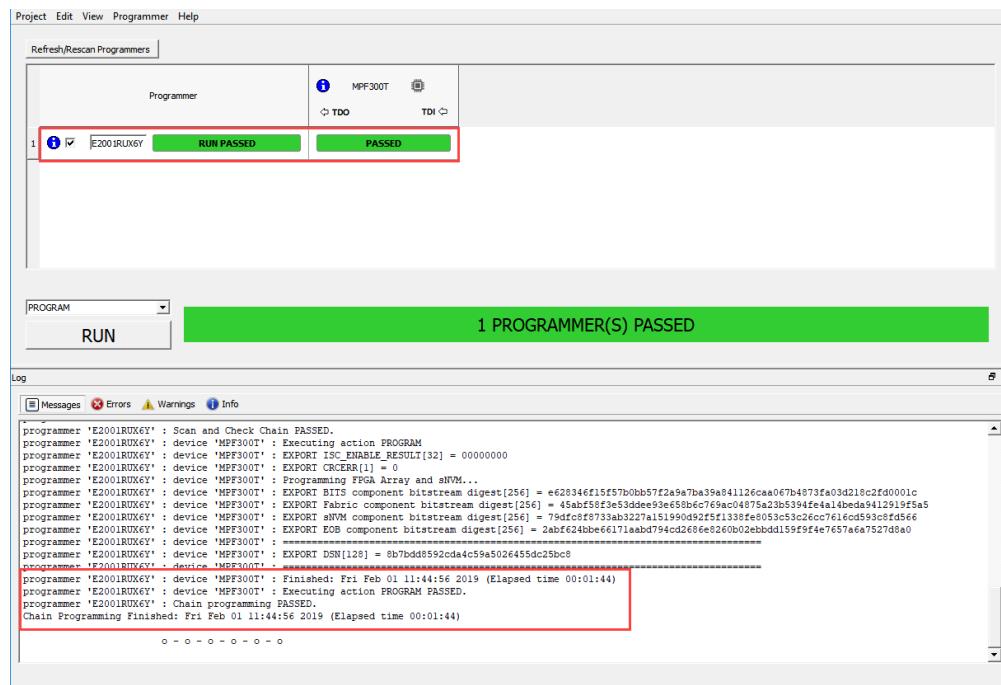
7. Enter the following in the New Job Project from FlashPro Express Job dialog box:
  - **Programming job file:** Click **Browse**, navigate to the location where the .job file is located, and select the file. The default location is: <download\_folder>\mpf\_an4597\_v2022p1\_df\Programming\_Job.
  - **FlashPro Express job project location:** Click **Browse** and navigate to the location where you want to save the project.

**Figure 6-2. New Job Project from FlashPro Express Job**

8. Click **OK**. The required programming file is selected and ready to be programmed in the device.
9. The FlashPro Express window appears, as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.

**Figure 6-3. Programming the Device**

10. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in the following figure. See [3. Running the Demo](#) to run the PCIe EndPoint demo.

**Figure 6-4. FlashPro Express—RUN PASSED**

11. Close FlashPro Express or in the **Project** tab, click **Exit**.

## 7. Appendix 4: Running the TCL Script

TCL scripts are provided in the design files folder under directory `TCL_Scripts`. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run the TCL, perform the following steps:

1. Launch the Libero software
2. Select **Project > Execute Script....**
3. Click **Browse** and select `script.tcl` from the downloaded `TCL_Scripts` directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within `TCL_Scripts` directory.

See the following for more information about TCL scripts:

- `mpf_an4597_v2022p1_df/TCL_Scripts/Eval_Kit/readme.txt`
- `mpf_an4597_v2022p1_df/TCL_Scripts/Splash_Kit/readme.txt`

See [Tcl Commands Reference Guide](#) for more details on TCL commands. Contact Technical Support for any queries encountered while running the TCL script.

## 8. **Appendix 5: DDR3L Configuration**

If you are using Rev E or Later kit , see [TU0775 Tutorial PolarFire FPGA: Building a Mi-V Processor Subsystem](#) for the configurations of DDR3L controller with the initialization and timing parameters for MT41K512M8DA-107: P part present on the Rev E PolarFire Evaluation Kit.

## 9. Appendix 6: References

This section lists documents that provide more information about the PCIe EndPoint and IP cores used in the reference design.

- For more information about PolarFire transceiver blocks, PF\_TX\_PLL, and PF\_XCVR\_REF\_CLK, see [PolarFire FPGA and PolarFire SoC FPGA Transceiver User Guide](#).
- For more information about PF\_PCIE, see [PolarFire FPGA and PolarFire SoC FPGA PCI Express User Guide](#).
- For more information about PF\_CCC, see [PolarFire FPGA and PolarFire SoC FPGA Clocking Resources User Guide](#).
- For more information about DDR3L/DDR4 memory, see [PolarFire FPGA and PolarFire SoC FPGA Memory Controller User Guide](#).
- For more information about Libero, ModelSim, and Synplify, see the [Libero SoC Documentation](#) web page.
- For more information about PolarFire FPGA Evaluation Kit, see [UG0747: PolarFire FPGA Evaluation Kit User Guide](#)
- For more information about PolarFire FPGA Splash Kit, see [UG0786: PolarFire FPGA Splash Kit User Guide](#)
- For more information about CoreAHBLite, see CoreAHBLite Handbook. This user guide can be downloaded from the Libero SoC Catalog.
- For more information about CoreAHBtoAPB3, see CoreAHBtoAPB3 Handbook. This user guide can be downloaded from the Libero SoC Catalog.
- For more information about CoreUART, see CoreUART User Guide. This user guide can be downloaded from the Libero SoC Catalog.

## 10. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

**Table 10-1. Revision History**

Revision	Date	Description
A	08/2022	<p>The following is the list of changes in revision A of the document:</p> <ul style="list-style-type: none"><li>• The document was migrated to the Microchip template.</li><li>• The document number was updated to DS00004597A from 50200756.</li><li>• The document ID was updated to AN4597 from DG0756.</li><li>• Replaced all Microsemi links with Microchip links.</li><li>• Renamed the DDR3 to DDR3L throughout the document.</li><li>• Updated <a href="#">Figure 1-4</a>.</li><li>• Updated <a href="#">Figure 1-5</a> and <a href="#">Figure 1-6</a>.</li><li>• Updated <a href="#">Figure 1-7</a> and <a href="#">Figure 1-8</a>.</li><li>• Updated <a href="#">Figure 1-9</a>.</li><li>• Updated content of <a href="#">1.7. Simulating the Design</a>.</li><li>• Updated design files location in <a href="#">3.1. Installing PCIe Demo Application</a>.</li><li>• Updated <a href="#">Figure 3-11</a>, <a href="#">Figure 3-12</a>, <a href="#">Figure 3-13</a>, <a href="#">Figure 3-14</a>, and <a href="#">Figure 3-15</a>.</li><li>• Updated <a href="#">Figure 3-16</a>, <a href="#">Figure 3-17</a>, <a href="#">Figure 3-19</a>, and <a href="#">Figure 3-20</a>.</li><li>• Updated .job file location in <a href="#">6. Appendix 3: Programming the Device Using FlashPro Express</a>.</li><li>• Updated TCL scripts file location <a href="#">7. Appendix 4: Running the TCL Script</a>.</li><li>• Added a new section <a href="#">8. Appendix 5: DDR3L Configuration</a>.</li></ul>
10.0	—	Added <a href="#">7. Appendix 4: Running the TCL Script</a> .
9.0	—	<p>The following is a summary of the changes made in this revision.</p> <ul style="list-style-type: none"><li>• Updated the document for Libero SoC v12.3.</li><li>• Removed the references to Libero version numbers.</li></ul>
8.0	—	The document was updated for Libero SoC v12.0 release.
7.0	—	Merged Splash kit related content and updated the document for Libero SoC PolarFire v2.3 release.
6.0	—	<p>The following is a summary of the changes made in revision 6.0 of this document.</p> <ul style="list-style-type: none"><li>• The document was updated for Libero SoC PolarFire v2.2 release.</li><li>• Information about DDR power measurement was added. See <a href="#">4. Appendix 1: DDR3L and DDR4 Power Measurement</a>.</li></ul>
5.0	—	The document was updated for Libero SoC PolarFire v2.1 release.
4.0	—	The document was updated to include features and enhancements introduced in the Libero SoC PolarFire v2.0 release.
3.0	—	<p>The following is a summary of the changes made in revision 3.0 of this document.</p> <ul style="list-style-type: none"><li>• The document was updated to include features and enhancements introduced in the Libero SoC PolarFire v1.1 SP1 release.</li><li>• Information about setting up the device and running the demo was added, see <a href="#">6. Appendix 3: Programming the Device Using FlashPro Express</a> and <a href="#">3. Running the Demo</a>.</li><li>• List of reference was added. For more information, see <a href="#">9. Appendix 6: References</a>.</li></ul>

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## Revision History

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Revision	Date	Description
2.0	—	<p>The following is a summary of the changes in revision 2.0 of this document.</p> <ul style="list-style-type: none"><li>• The document was updated for Libero SoC PolarFire v1.1 release.</li><li>• Information about resource utilization was added. For more information, see Resource Utilization.</li></ul>
1.0	—	The first publication of this document.

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