Condition Code Register (CCR) and the Condition Codes (Flags)

The Condition Code register contains

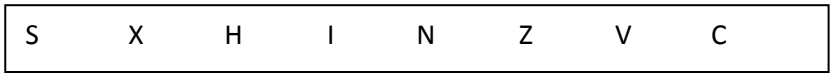
- Five flag or status indicators C, H, N, Z, V
- Two interrupt masking bits X, I
- STOP instruction control bit S

The five condition flags are:

- Carry/borrow Flag (C)
- Negative or Sign Flag (N)
- Zero Flag (Z)
- Overflow Flag (V)
- Half carry Flag (H)

The Flags are either Clear (0) or Set (1)

The bit positions in the CCR are:



Bit 7 Bit 0

DeBug 12 Display

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>rd

PP  PC    SP    X     Y     D = A:B   CCR = SXHI NZVC
38 0000  3C00  0000  0000     00:00         1001 0000
xx:0000  00            BGND
>

>

>_
```

C Status or Carry Flag

The C bit is set when a carry occurs during addition or a borrow occurs during subtraction.

N Status, Negative or Sign Flag

The N bit shows the state of the MSB of the result. N is most commonly used in two's complement arithmetic, where the MSB of a negative number is 1 and the MSB of a positive number is 0, but it has other uses. When the MSB of the result of an operation is a 1, then this flag will be set to a 1- otherwise it will be set to a zero.

Z Status or Zero Flag

The Z bit is set to a 1 when the result of an operation is zero (all bits are 0) otherwise it will be set to a zero .

V Status or Overflow Flag

The V bit is set when two's complement overflow occurs as a result of an operation. The V flag is set when the carry out from the most significant bit and the carry in to the most significant bit differ as a result of an arithmetic operation.

V = (Carry In to MSB) ExOR (Carry Out from MSB)

H Status or Half Carry Flag

The H bit indicates a carry from accumulator A (or B) bit 3 during an addition operation. And is often used to correct BCD format. H is updated only by the add accumulator A to accumulator B (ABA), add without carry (ADD), and add with carry (ADC) instructions.