Задание 4.

4.1. После выполнения следующих команд какое значение будет в регистре `r4`?

```
00 E59F0008 LDR r0, =0xF185
04 E59F1008 LDR r1, =0x8AC4
08 E0014000 AND r4, r1, r0
```

(A) 0x0000250B (B) 0x00008084 (C) 0x00000856
(D) 0x00000006 (E) 0x00000008 (F) другое

4.2. После выполнения следующих команд какое значение будет в регистре `r4`?

```
00 E59F0008 LDR r0, =0x7A48
04 E59F1008 LDR r1, =0xA7A
08 E1914200 ORRS r4, r1, r0, LSL #4
```

(A) 0x00000003 (B) 0x000AF647 (C) 0x000982DA
(D) 0x00021A4C (E) 0x0007AEFA (F) другое

4.3. После выполнения следующих команд какое значение будет в регистре `r2`?

```
00 E3A02000 MOV r2, #0x0
04 E3A010BE LDR r1, =0xBE
08 E1B010A1 MOVS r1, r1, LSR #1
0c E2A22000 ADC r2, r2, #0
10 E1B010A1 MOVS r1, r1, LSR #1
14 E2A22000 ADC r2, r2, #0
```

(A) 0x00000001 (B) 0x00000019 (C) 0x00000014
(D) 0x00000007 (E) 0x00000005 (F) другое

4.4. После выполнения следующих команд какое значение будет в регистре `r4`?

```
00 E59F0008 LDR r0, =0x37D1
04 E59F1008 LDR r1, =0x56D4
08 E0214360 EOR r4, r1, r0, ROR #6
```

(A) 0x28F8DC40 (B) 0x00000004 (C) 0x4400560B
(D) 0x84CCB5C7 (E) 0x00000001 (F) другое

Флаги Condition Code


Endianness
For ease of reading machine code and integer data in the second column are displayed in big endian format, byte data and strings in little endian format.

ASCII Table

	0	1	2	3	4	5	6	7
0	NUL	DLE	SPACE	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

Conditional Branch Instructions

Branch Instruction	Condition Code Flag Evaluation	Description
B (or BAL)	don't care	unconditional (branch always)
BEQ	Z	equal
BNE	$\bar{Z}$	not equal
BCS / BHS	C	unsigned ≥
BCC / BLO	$\bar{C}$	unsigned <
BMI	N	negative
BPL	$\bar{N}$	positive or zero
BVS	V	overflow
BVC	$\bar{V}$	no overflow
BHI	$C\bar{Z}$	unsigned >
BLS	$\bar{C} + Z$	unsigned ≤
BGE	$NV + \bar{N}\bar{V}$	signed ≥
BLT	$N\bar{V} + \bar{N}V$	signed <
BGT	$\bar{Z}(NV + \bar{N}\bar{V})$	signed >
BLE	$Z + N\bar{V} + \bar{N}V$	signed ≤

Summary of LDR/STR Addressing Modes

Addressing mode	Syntax	W,B	H,SH,SB	Operation
Immediate Offset	[<Rn>, #+/- <offset>]	√	√	address ← Rn +/- offset
Register Offset	[<Rn>, #+/- <Rm>]	√	√	address ← Rn +/- Rm
Scaled Register Offset	[<Rn>, #+/- <Rm>, <shift> #<count>]	√		address ← Rn +/- (Rm <shift> <count>)
Immediate Pre-indexed	[<Rn>, #+/- <offset>]!	√	√	Rn ← Rn +/- offset address ← Rn
Register Pre-indexed	[<Rn>, #+/- <Rm>]!	√	√	Rn ← Rn +/- Rm address ← Rn
Scaled Register Pre-indexed	[<Rn>, #+/- <Rm>, <shift> #<count>]!	√		Rn ← Rn +/- (Rm <shift> <count>) address ← Rn
Immediate Post-indexed	[<Rn>], #+/- <offset>	√	√	address ← Rn Rn ← Rn +/- offset
Register Post-indexed	[<Rn>], #+/- <Rm>	√	√	address ← Rn Rn ← Rn +/- Rm
Scaled Register Post-indexed	[<Rn>], #+/- <Rm>, <shift> #<count>	√		address ← Rn Rn ← Rn +/- (Rm <shift> <count>)