American University in Central Asia
Software Engineering Department
Computer Architecture (3 credits)
ID: 3268 COM 410.1
Spring Semester - 2020.

Syllabus

Lectures: Tuesday, 14:10;
Lab. Works: Tuesday, 15:35

Lecturer: **Melis S. Osmonov**, Candidate of Technical Sciences
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Office Hours: by appointment

Prerequisites:

COURSE DESCRIPTION

This course is a course on computer architecture with an emphasis on a quantitative approach to cost/performance design tradeoffs. The course covers the fundamentals of classical and modern processor design: performance and cost issues, instruction sets, pipelining, caches, physical memory, virtual memory, I/O superscalar and out-of-order instruction execution, speculative execution, long (SIMD) and short (multimedia) vector execution, multithreading, and an introduction to shared memory multiprocessors.

COURSE OBJECTIVES

- to learn fundamentals of classical and modern processor design;
- to study architecture of different processor through programming on assembler languages.

COURSE CONTENTS

- Introduction. History of computer architecture.
- Instruction set architecture.
- Performance.
- Technology.
- Pipelining.
- Caches.
- Virtual Memory.
- Superscalar.
- Scheduling.
- Multicore. Vectors

Lectures (30 academic hours)

№	Theme names and its contents	hours
1.	**Theme 1. Introduction.** History of computer architecture.	2
2.	**Theme 2. Instruction set architecture.** ISA Design Goals. MIPS, x86, ARM ISA. RISC and CISC. VLIW and EPIC.	4
3.	**Theme 3. Performance.** Metrics. Latency and throughput. Speedup. CPU Performance. Performance Pitfalls. Benchmarking.	2
4.	**Theme 4. Technology.** Technology basis. Manufacturing and cost. Transistor Switching Speed. Technology Scaling Trends. Power & Energy.	2
5.	**Theme 5. Pipelining.** Principles of pipelining. Data hazards. Control hazards. Structural Hazard. Bypassing.	2
6.	**Theme 6. Caches**. Basic memory hierarchy concepts. Types of Memory. Hardware Cache Organization. Finding Data via Indexing. Handling a Cache Miss	2
7.	**Theme 7. Virtual Memory.** Virtualizing Main Memory. Address Translation. Page Table Size. Multi-Level Page Table. Translation Lookaside Buffer.	4
8.	**Theme 8. Superscalar.** Superscalar scaling issues. Multiple fetch and branch prediction. Dependence-checks & stall logic. Wide bypassing. Register file & cache bandwidth. Multiple-issue designs. Superscalar. VLIW and EPIC (Itanium).	4
9.	**Theme 9. Scheduling.** Code scheduling to reduce pipeline stalls, to increase ILP (instruction level parallelism). Static scheduling. Compiler Scheduling. Static Scheduling Limitations. Dynamic scheduling. Register Renaming.	2
10.	**Theme 10. Multicore.** Thread-level parallelism (TLP). Shared memory model. Multiplexed uniprocessor. Hardware multithreading. Multiprocessing. Shared Memory Issues. Parallel Programming. Synchronization. Lock implementation. Cache coherence. Bus-based protocols. Directory protocols. Memory consistency models.	2
11.	**Theme 11. Vectors.**	2
12.	**Theme 12. Multiprocessor architecture.**	4

LAB WORKS

The goal of lab works is acquiring of practical skills in programming on Assembler languages.

▪ Lab work 1. Basic ARM Instructions.	10 points
▪ Lab work 2. ARM Branch instructions.	10 points
▪ Lab work 3. ARM addressing modes.	10 points
▪ Lab work 4. ARM subroutine calls.	20 points

EVALUATION AND GRADING:

The course grade will be calculated as follows:

• Programming assignments, lab exercises:	-	50 points
• Midterm Exam:		20 points
• Final Exam:	-	30 points

GRADES

Final course grades will be assigned as follows:

$95 < A \leq 100$ $90 < A^{-} \leq 95$ $85 < B^{+} \leq 90$ $80 < B \leq 85$

$75 < B^{-} \leq 80$ $70 < C^{+} \leq 75$ $65 < C \leq 70$ $60 < C^{-} \leq 65$

$55 < D^{+} \leq 60$ $50 < D \leq 55$ $F \leq 50$

TEXTBOOK

1. Hennessy John L., Patterson David A. ***Computer Architecture: A Quantitative Approach***. – Morgan Kaufmann, 2007.
2. Hennessy John L., Patterson David A. ***Computer Organization and Design MIPS Edition***: The Hardware/Software Interface. Fifth Edition: - Morgan Kaufmann, 2017.
3. Hennessy John L., Patterson David A. Computer Organization and Design ARM Edition: The Hardware Software Interface. - Morgan Kaufmann, 2017.
4. Clements Alan. ***Computer Organization and Architecture: Themes and Variations***. – Cengage Learning, 2014.

ADDITIONAL TEXTBOOKS

1. Jean-Loup Baer. ***Microprocessor Architecture From simple Pipelines to Chip Multiprocessors.*** - Cambridge University Press, 2010.
2. P.A. Carter. ***PC Assembly Language.*** - 2006
3. Hohl William, Hinds Christopher. ***ARM Assembly Language: Fundamentals and Techniques.*** – CRC Press, 2015.
4. Э.Таненбаум. ***Архитектура компьютера. 4-е издание***. – Питер, 2003.

COURSE POLICY

Requirements to student’s behavior do not go beyond the scope of AUCA Code of Honor.