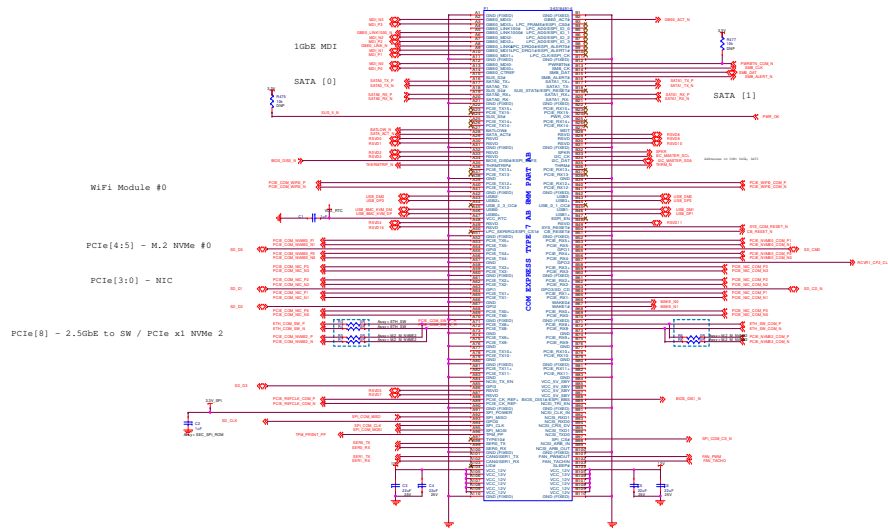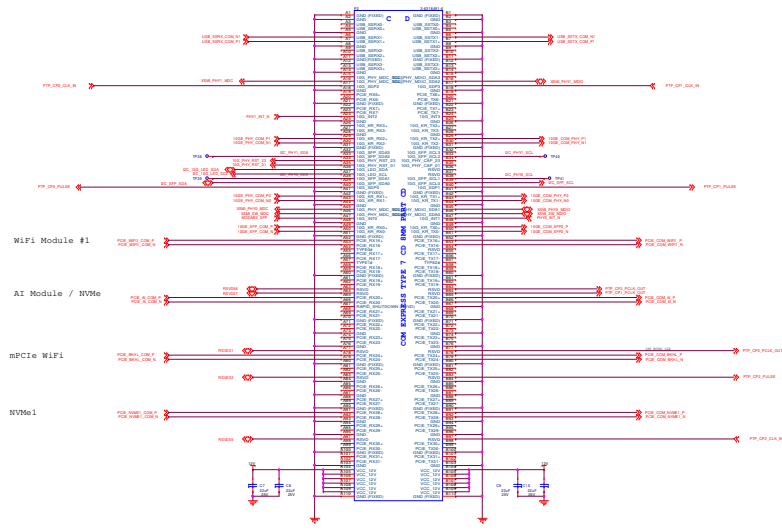# COM-EX Type7 Conn A/B
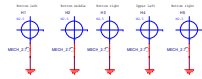
COM-EX Type7 Conn C/D

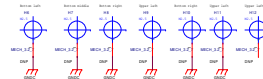COM Express type 7 C/D

1GbE MDI

SATA [0]

SATA [1]

WiFi Module #0

PCIe[4:5] - M.2 NVMe #0

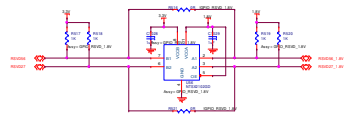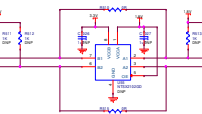PCIe[3:0] - NIC

PCIe[8] - 2.5GbE to SW / PCIe x1 NVMe 2

WiFi Module #1

AI Module / NVMe

mPCIe WiFi

NVMe1

COM Spacers

Mechanical Holes

SATA #0

SATA 0

GPIO Header
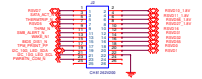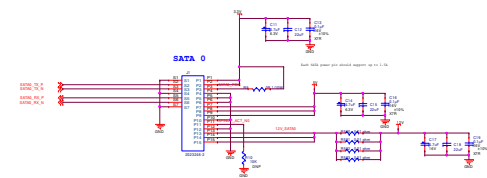
SATA #1

SATA 1
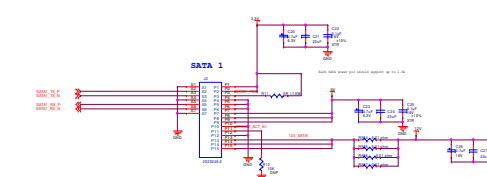
NVMe #2
M.2 Key-M
PCIe X1 Gen3
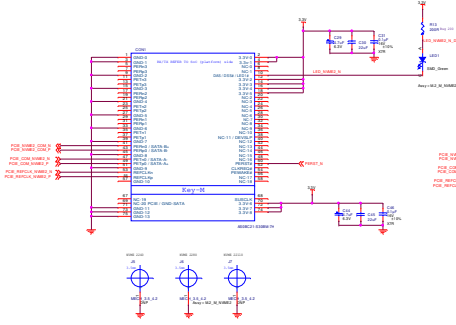
NVMe #1
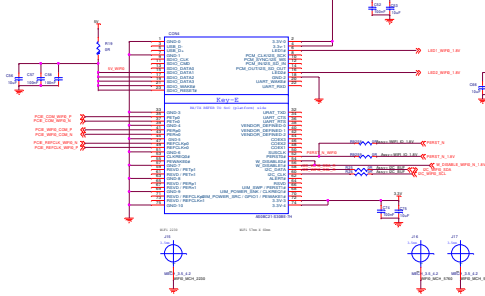## M.2 Key-M
PCIe X1 Gen3
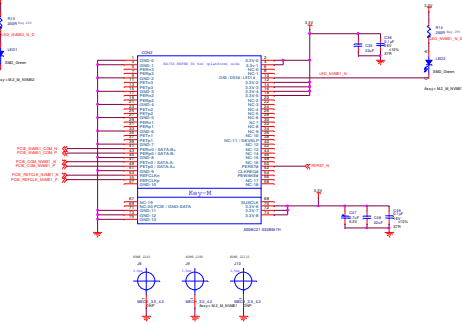
NVMe #0
M.2 Key-M
PCIe X2 Gen3
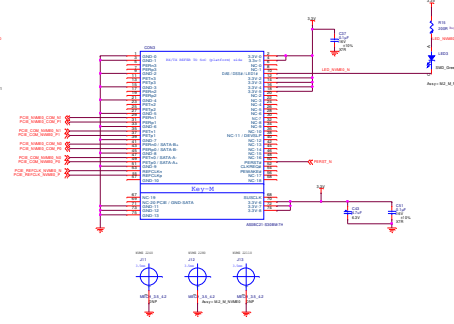
PCIe Edge Connector
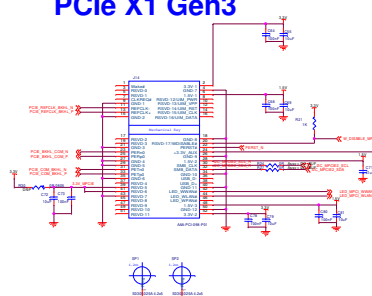## X4 Open Slot
PCIe X4 Gen3
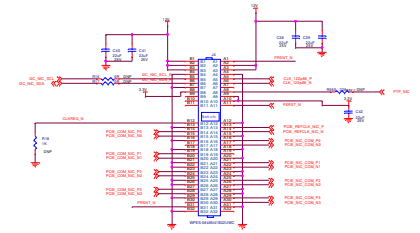
Wi-Fi 2.4GHz 802.11ax
M.2 Key-E
PCIe X1 Gen3

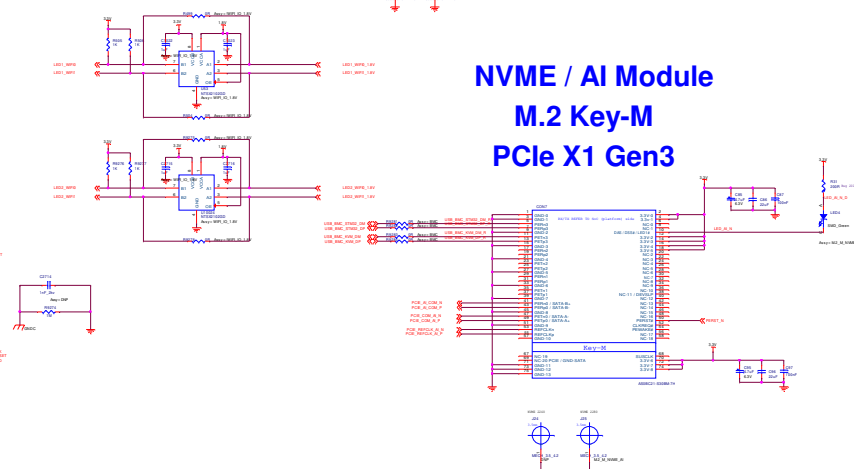# Wi-Fi 5GHz 802.11ax
M.2 Key-E
PCIe X1 Gen3
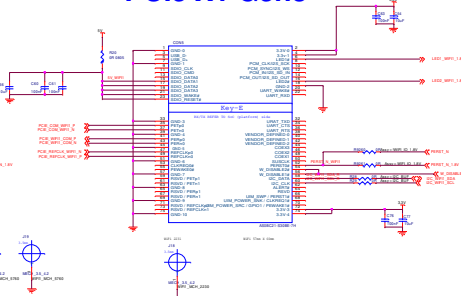
BackHaul 802.11ac wave2
mPCIe
PCIe X1 Gen3

LTE / 5G
M.2 Key-B
USB 3.0

uSIM0 connector

uSIM1 connector
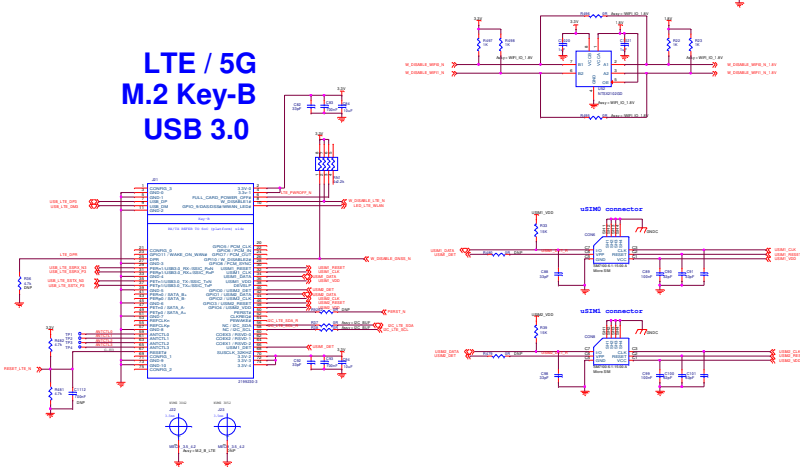
NVME / AI Module
## M.2 Key-M
PCIe X1 Gen3

Managment

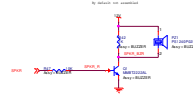**(Assy = MGMT)**

Management block connected to multinode BMC -
1. VBus powered (via 3.3v LDO)
2. USART2 pins PA2 (MCU TX) and PA3 (MCU RX)connected to application processor. Do not use USART1/2 on pins 14,15,8,9 since they are used for DFU mode.
3. USB DFU on pins PA11,PA12
4. I2C1 on PB6 (SCL) /PB7 (SDA)
5. SPI1 CLK/MISO/MOSI on PA5/PA6/PA7
6. PB0 / PB1 analog in (first 48v and second amplified current shunt voltage drop)
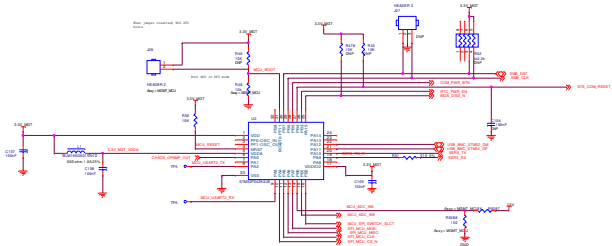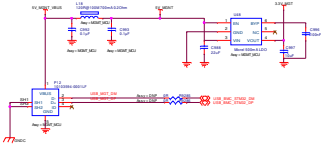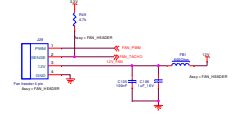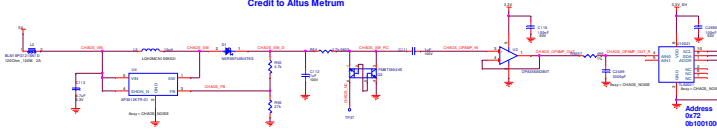
micro SD connector (bootable)
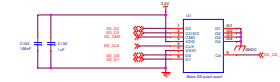
Single Tone Buzzer

FAN
(Assy = FAN_HEADER)

Noise generator ChaosKey

Credit to Altus Metrum

Address
0x72
0b1001000

Status LEDs
(Assy = STATUS_LEDS)

LTE STATUS

WIFI0 LED1

WIFI1 LED1

WIFI0 LED2

WIFI1 LED2

BR LINK

BR STATUS

Power

IO LED

Diplexers
(Assy = DIPLEXERS)

Onboard micro USB to serial console
(Assy = FTDI)

Reroute & RESET Buttons
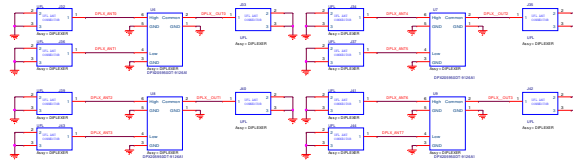
Warm Reset Button

RTC Battery

Secondary (FailSafe) Flash
(Assy = SEC_SPI_ROM)

I2C buffer

EEPROM Address
0x77
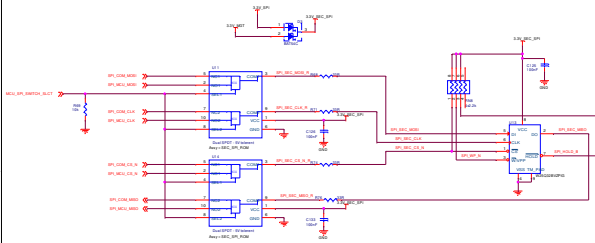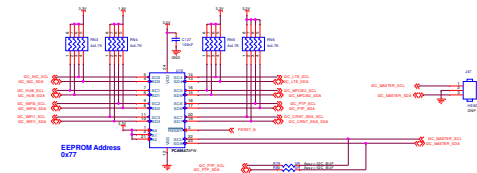
USB 2.0 Header
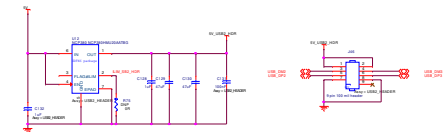
4x 1GbE SW

(Assy = ETH_SW)

88E6141
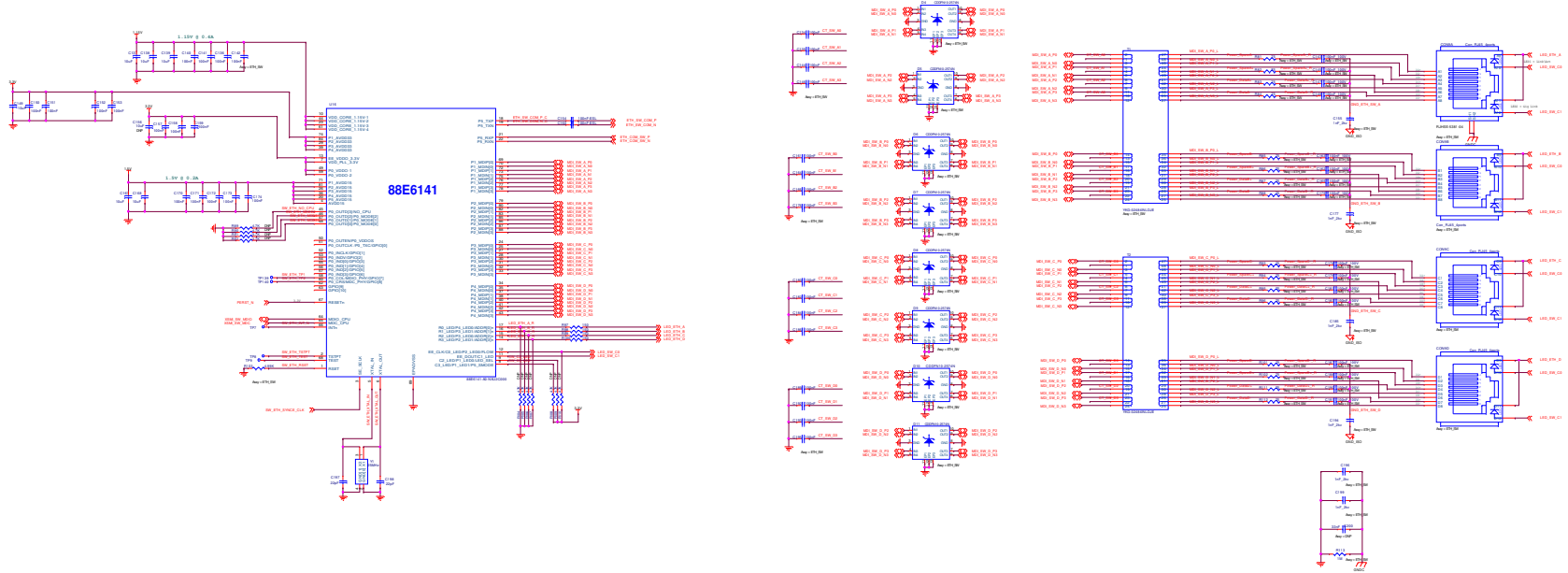
10GbE SFP+

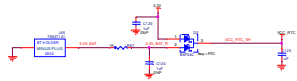(Assy = SFP+)
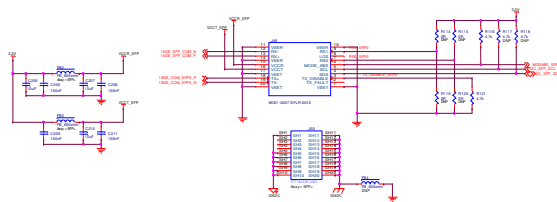
RJ45 1GbE

(Assy = RJ45_MDI)

88E2110 5GbE PHY0

(Assy = PHY0)

10GbE RJ45 Port PD

(Assy = PHY0)

Pair 2 - 1/2 / Data

Pair 3 - 3/6 / Data

Pair 1 - 4/5 / Spare

Pair 4 - 7/8 / Spare

Refer to datasheet for CO NFG details

PoE IDEAL DIODE BRIDGE

(Assy = POE_PD_PHY0)

802.3bt PD Controller + Flyback 12V@5.5A

(Assy = POE_PD_PHY0)
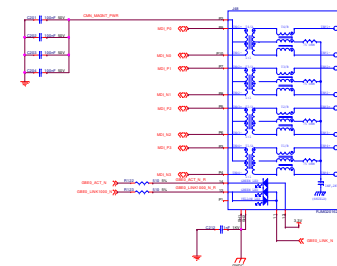
88E2110 5GbE PHY1

(Assy = PHY1)

boost 12V to 54V@0.7A
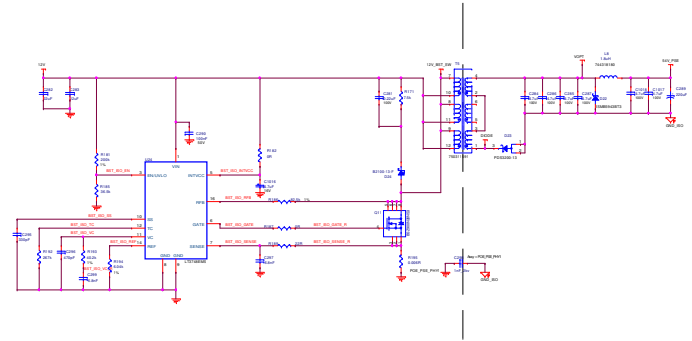
PSE Controller

5GbE RJ45 Port PSE

(Assy = PHY1)

Pair 2 - 1/2 / Data

Pair 3 - 3/6 / Data

Pair 1 - 4/5 / Spare

Pair 4 - 7/8 / Spare

USB 3.0 internal

(Assy = CP2_USB_HUB)

USB 3.0 HUB

(Assy = CP2_USB_HUB)

USB 3.0 HUB
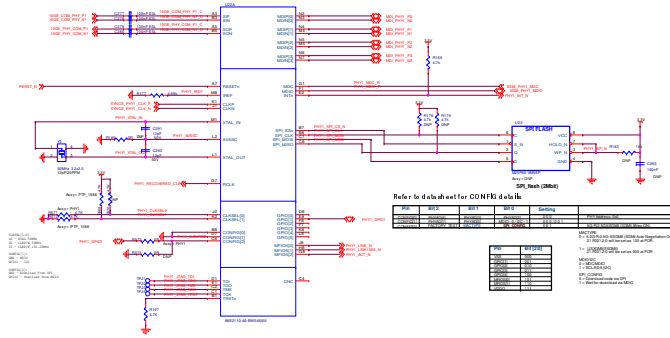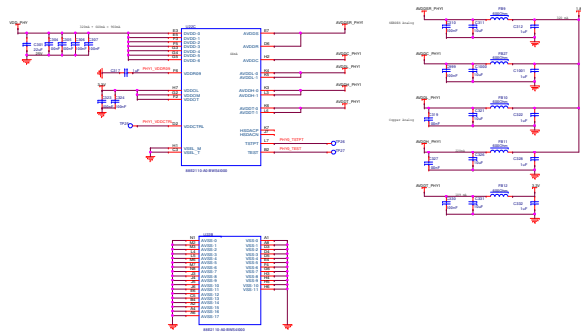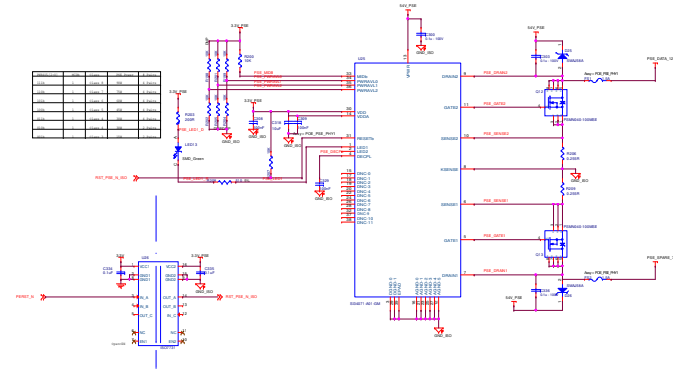
(Assy = CP2_USB_HUB)

1588v2 & SYNCE

PTP PULSE UFL

EEPROM Address
0x4C

RCLK to PHYs

PCIe Clock Buffer

DC JACK

3.3V

DNP - 500KHz
866KOhm - 650KHz

FCCM Mode

5V

FCCM 600KHz

Address
0x40

1.2V   1.5V   1.15V   1.8V

Note: 1.2V, 1.5V, 1.15V, 1.8V, 5V, VDD_PHY can be removed in BASE configuration

PHY_DVDD 0.88V / 0.8V

PWR_OK

CB_RESET / PERST