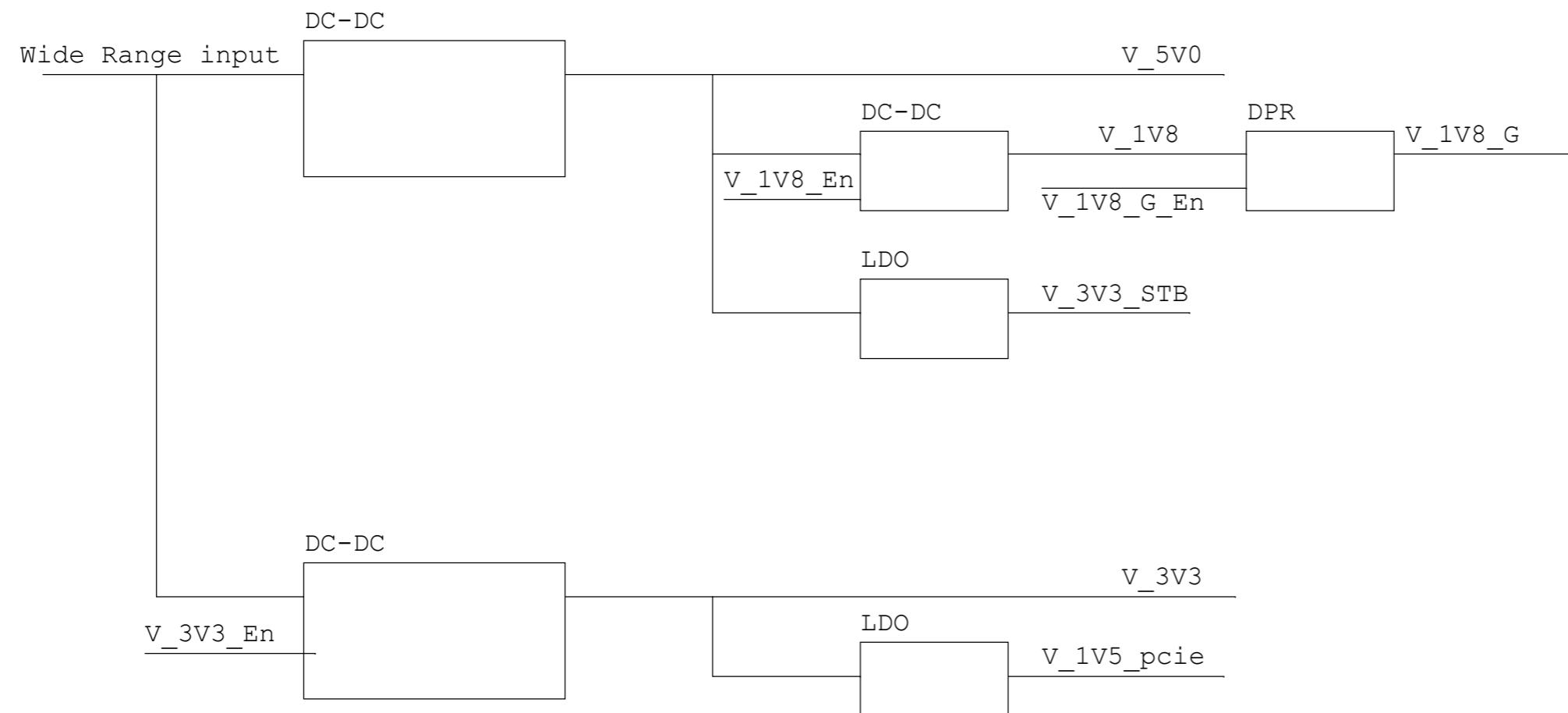
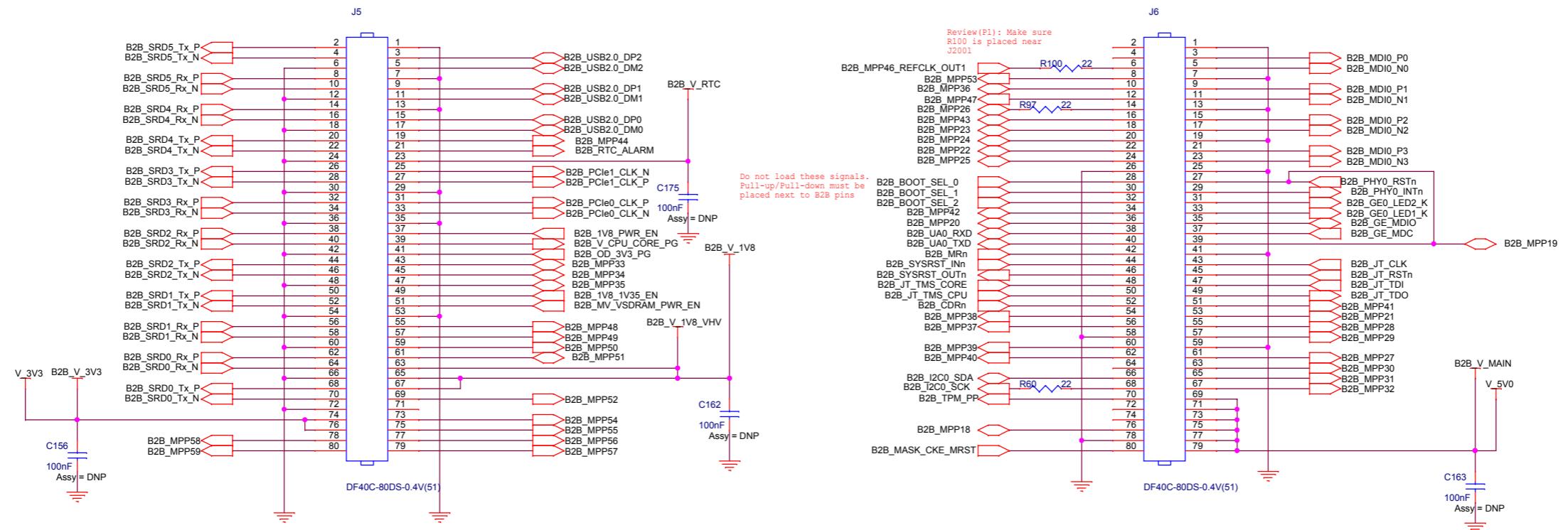


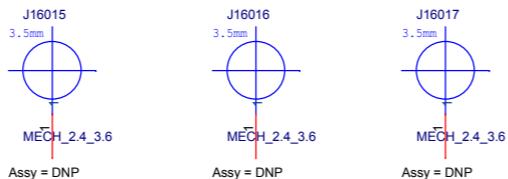
## To Extract BOM

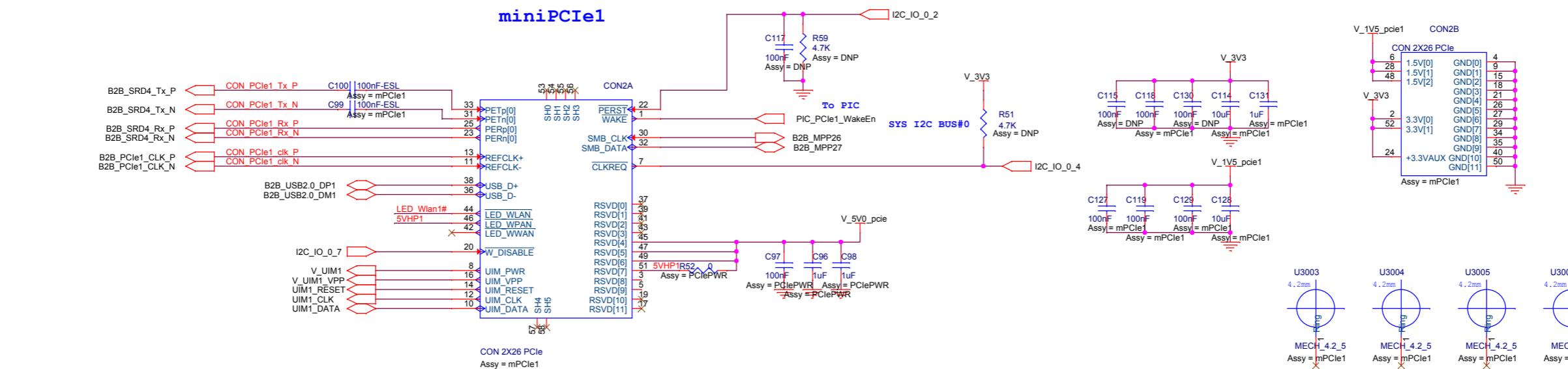
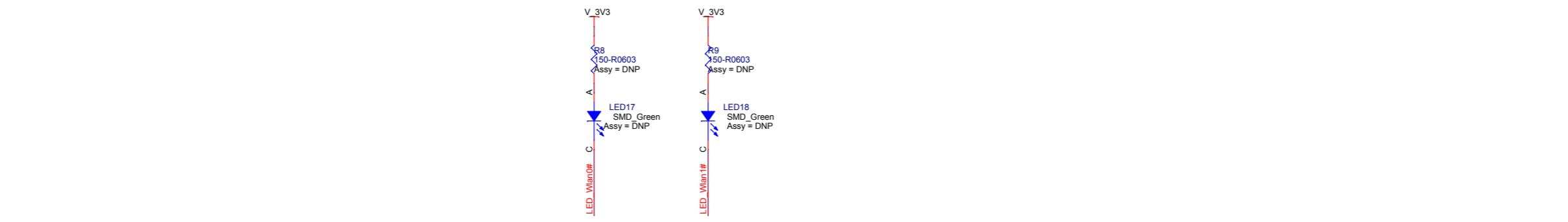
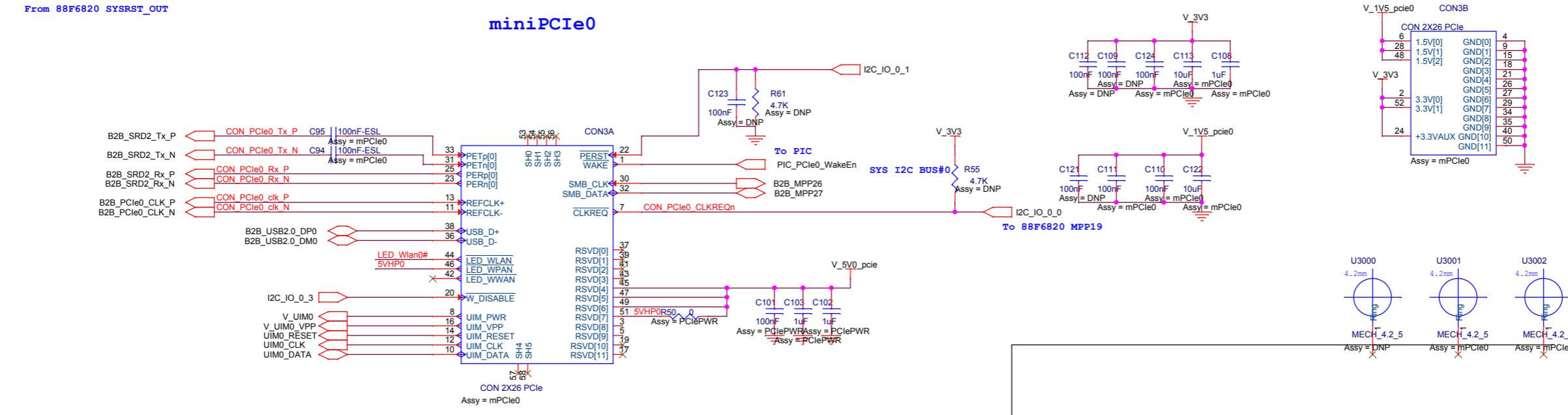
Item\tQuantity\tAssemblyOption\tPart\tPCB Footprint\tDescription\tDataSheet\tManufacturer\tManufacturer P/N\tSolidRun P/N\tReference  
{Item}\t{Quantity}\t{ASSY}\t{Value}\t{PCB Footprint}\t{DESCRIPTION}\t{Datasheet}\t{Manufacturer}\t{Manufacturer P/N}\t{SolidRun P/N}\t{Reference}

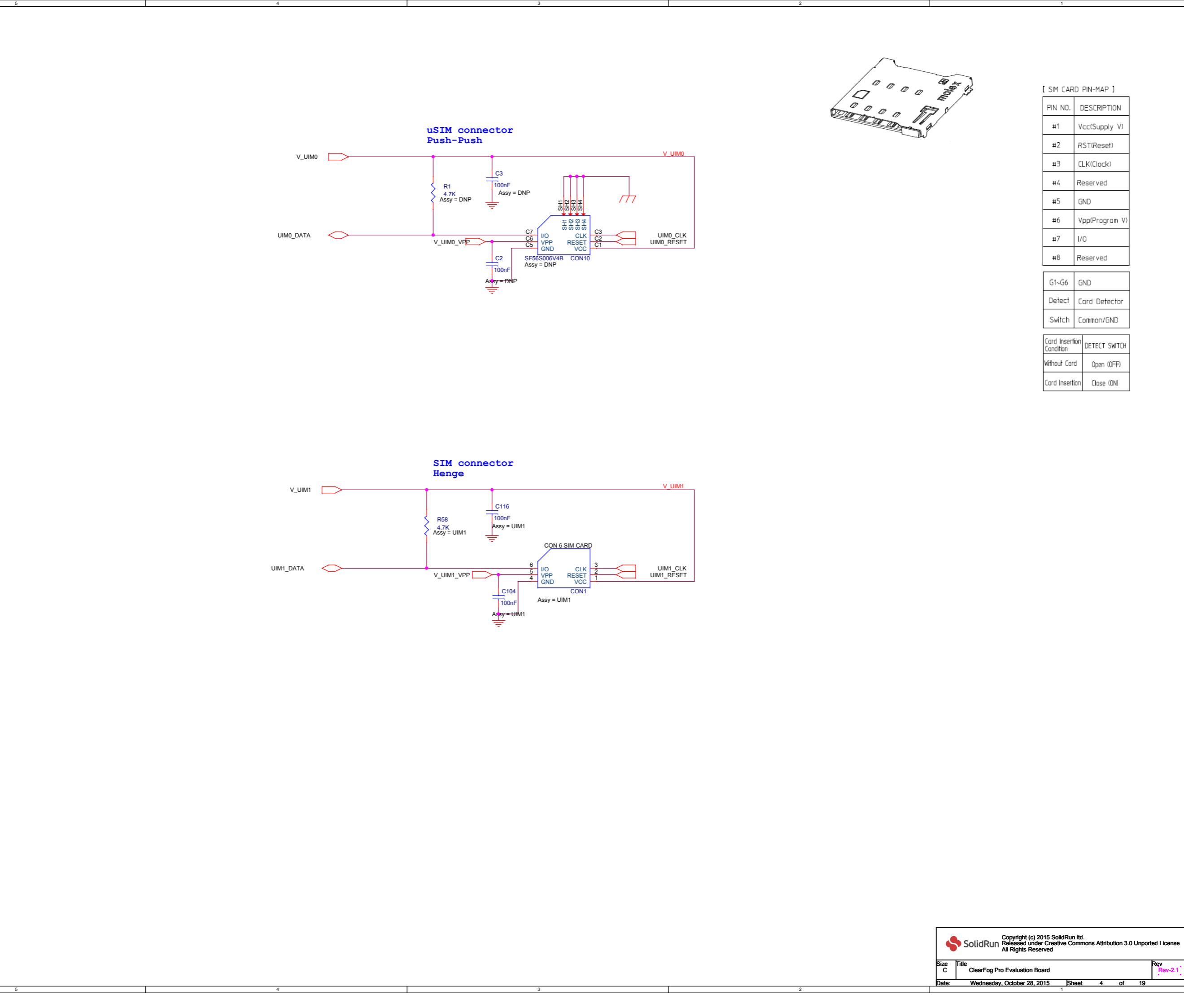


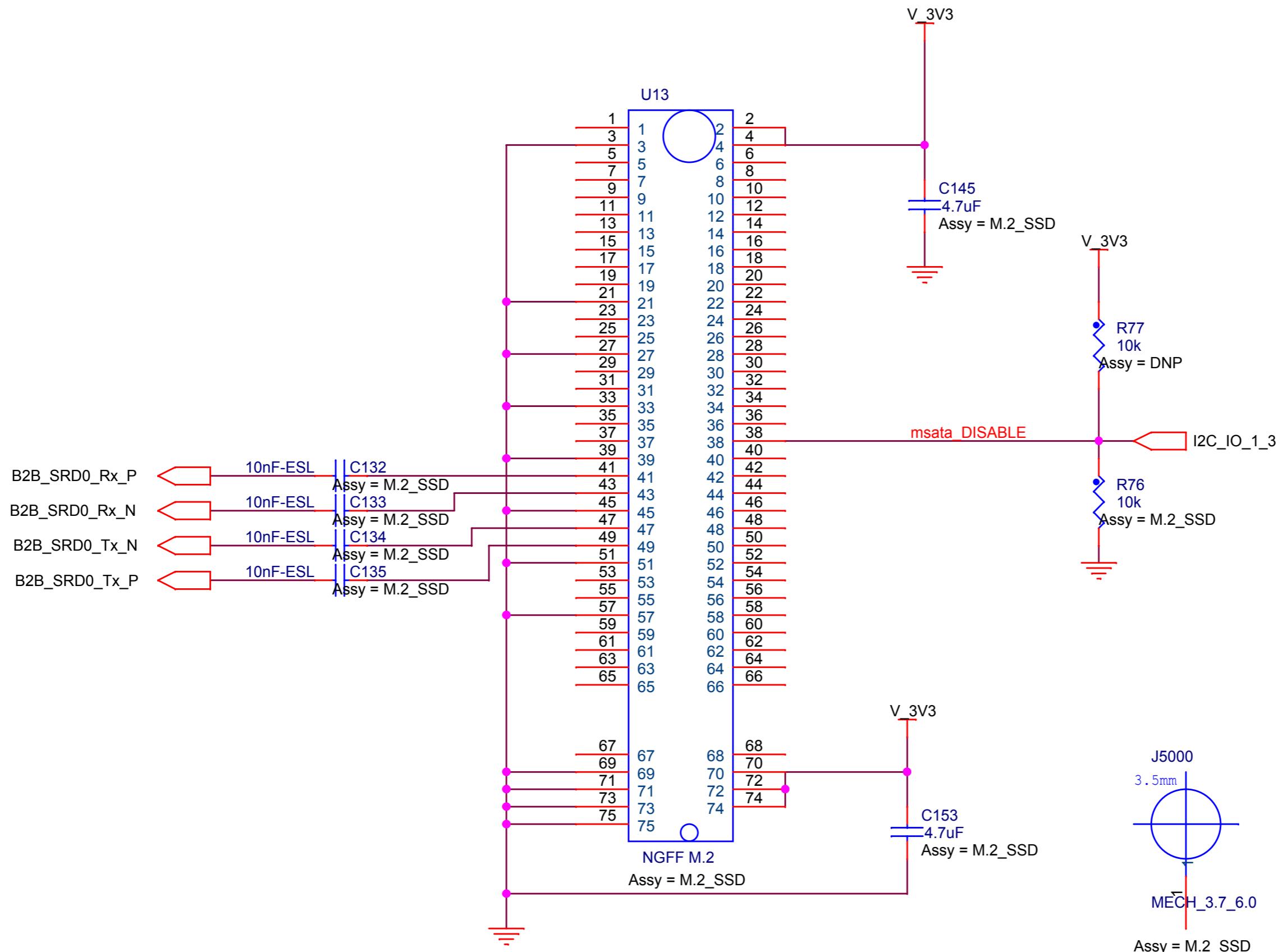


Three mechanical holes for the MicroSoM



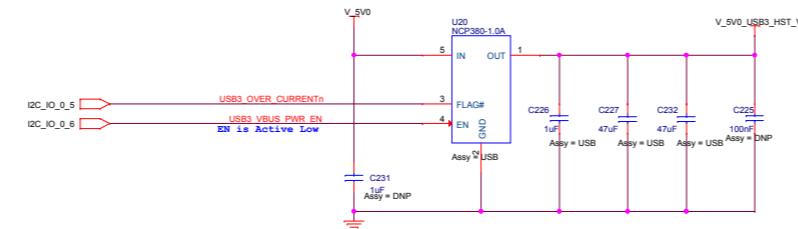
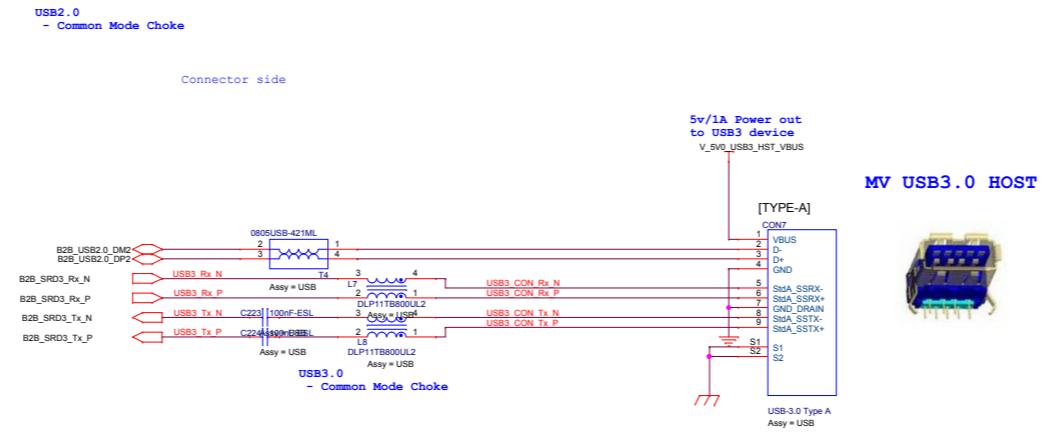


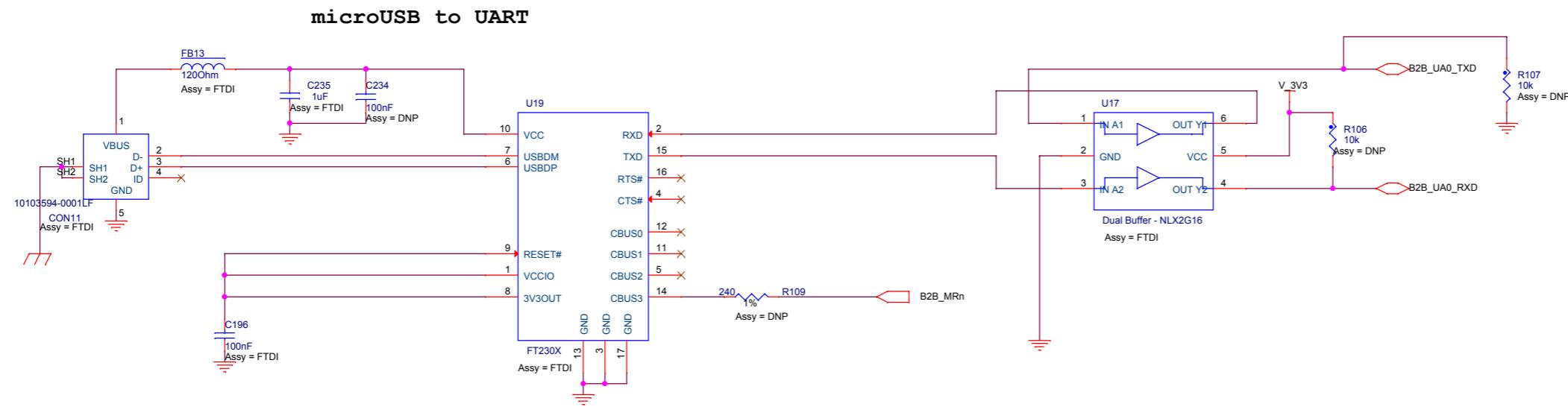


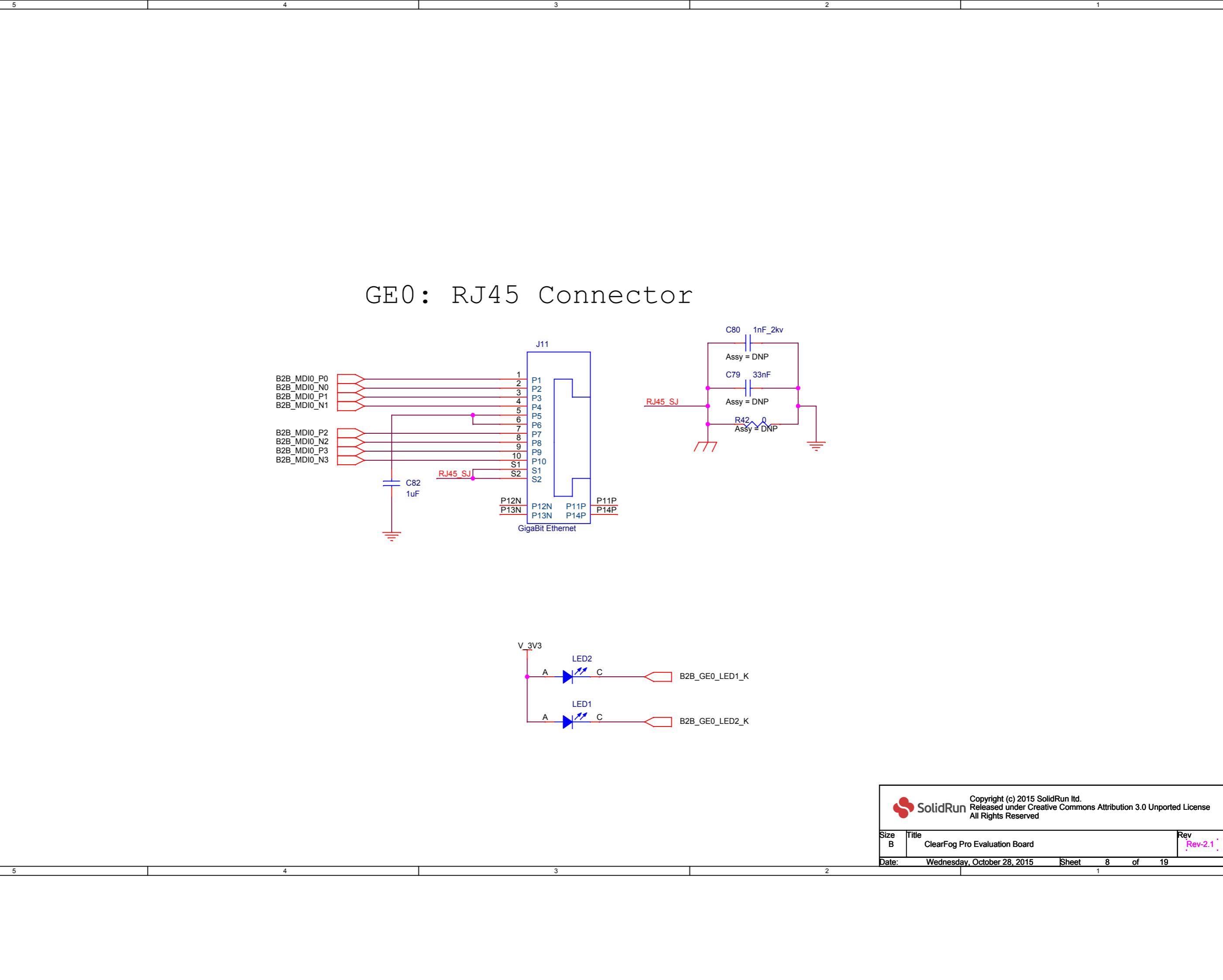


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Size	Title	Rev
A	ClearFog Pro Evaluation Board	
	Date: Wednesday, October 28, 2015	Rev
		Rev-2.1

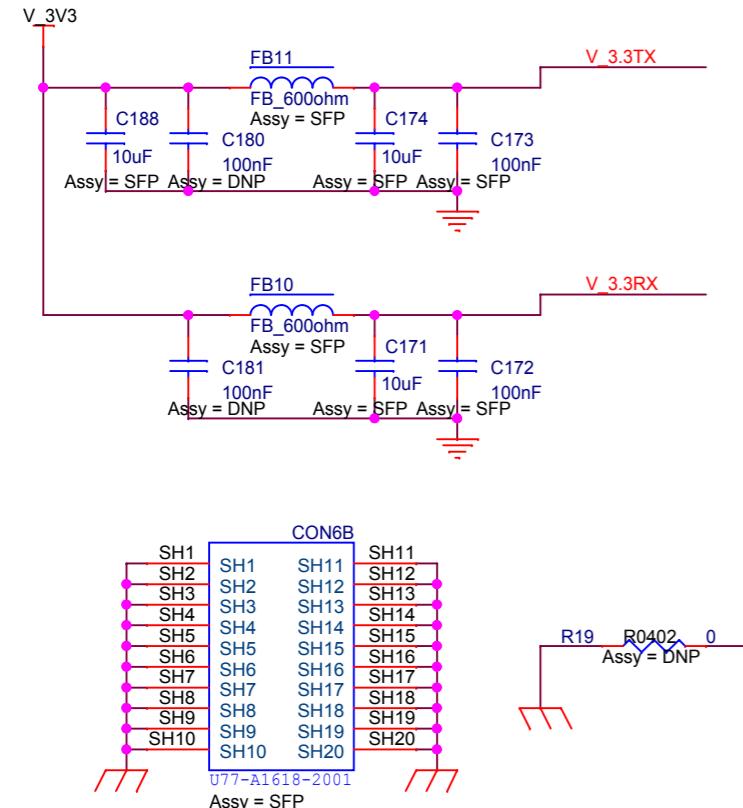






5 4 3 2 1  
SFP + defines maximum current  
withdraw from V\_3.3TX and V\_3.3RX as  
300mA each.

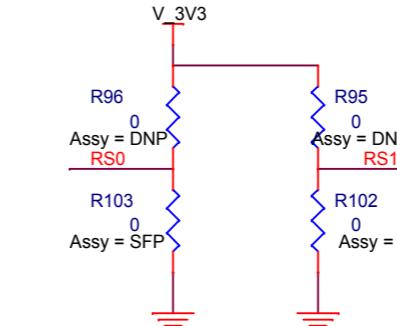
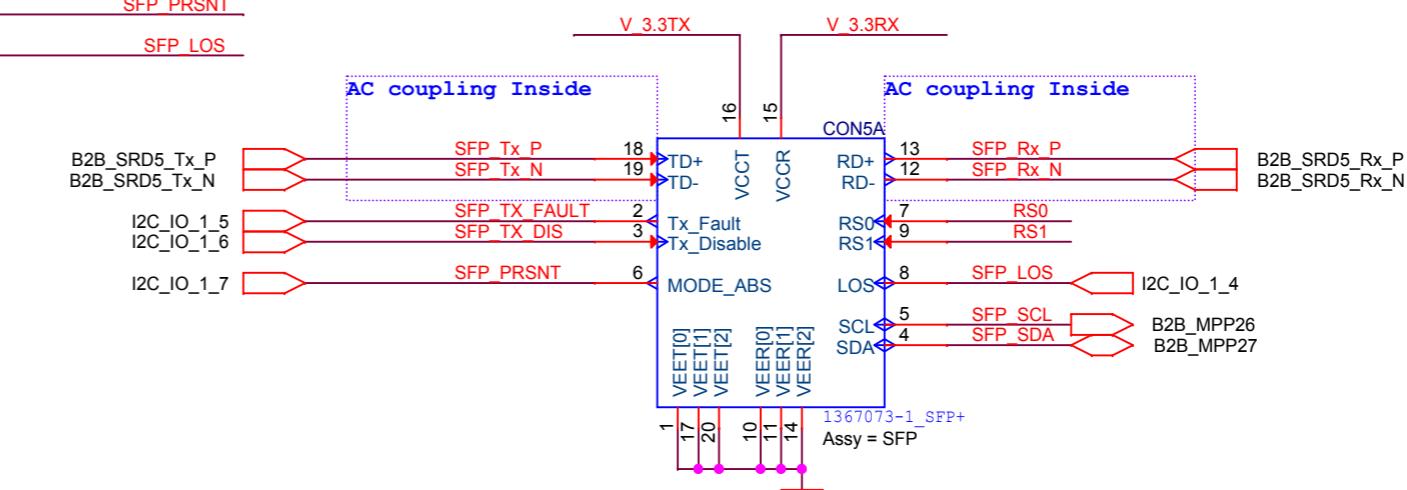
### SFP TRANSCEIVER Power



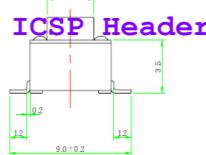
V\_3V3  
Replaced/Removed  
pullups with I2C\_IO  
expander's pullups.



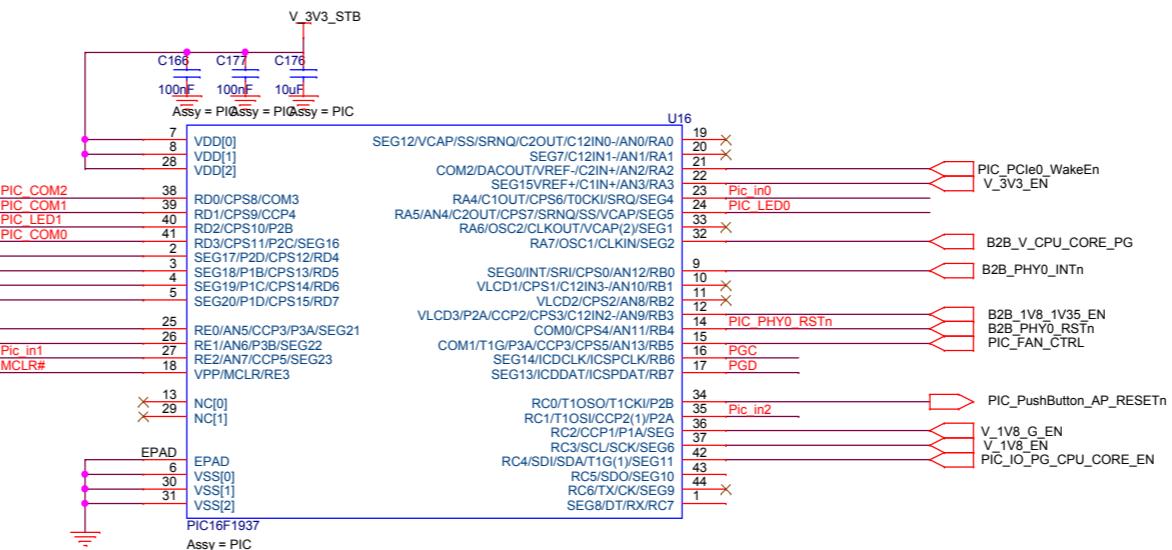
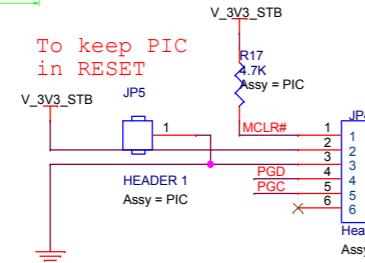
### SFP TRANSCEIVER



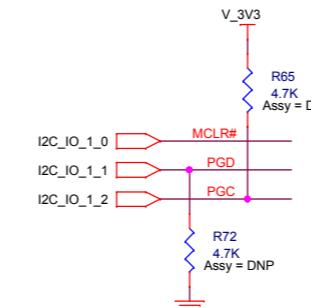
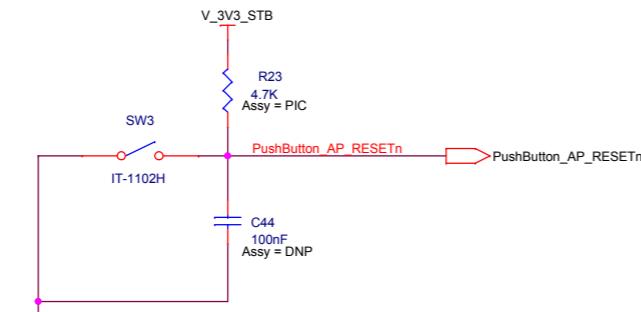
Copyright (c) 2015 SolidRun Ltd. Released under Creative Commons Attribution 3.0 Unported License All Rights Reserved		
Size B	Title ClearFog Pro Evaluation Board	Rev Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 9	of 19



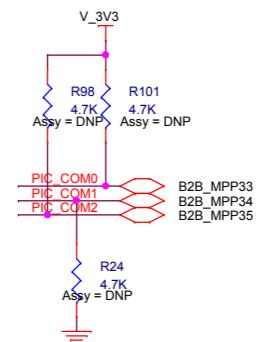
**PIC16F1937**



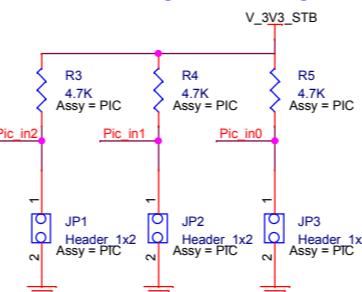
**AP Reset Switch (GPIO)**



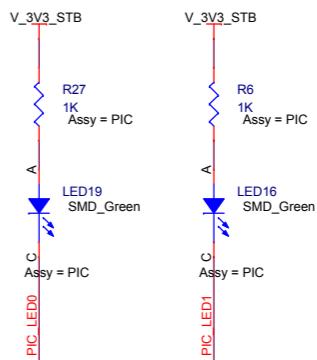
**COM with MV Device**



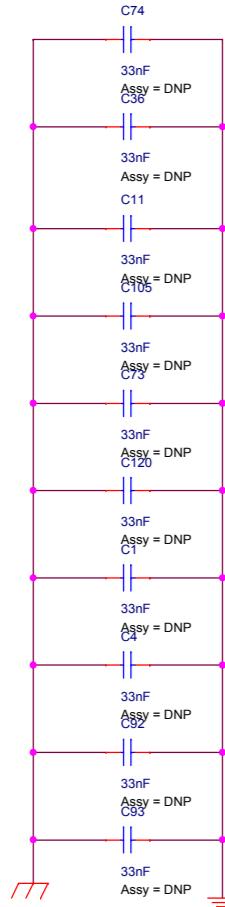
**For SW Configuration Usage**



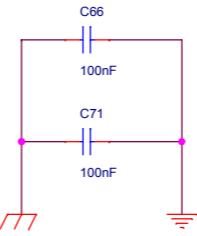
**LEDs**



Bypass capacitors between GNDC and GND

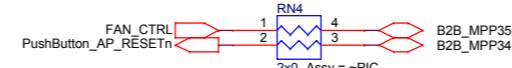
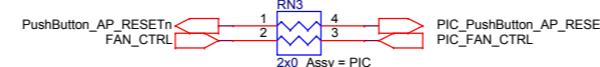
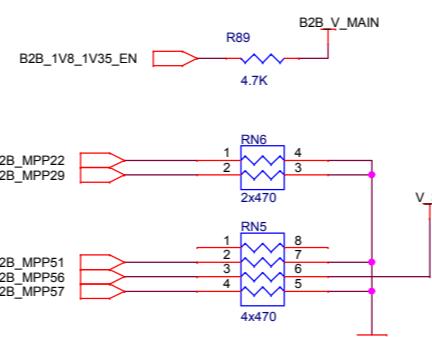
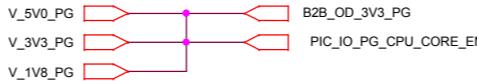


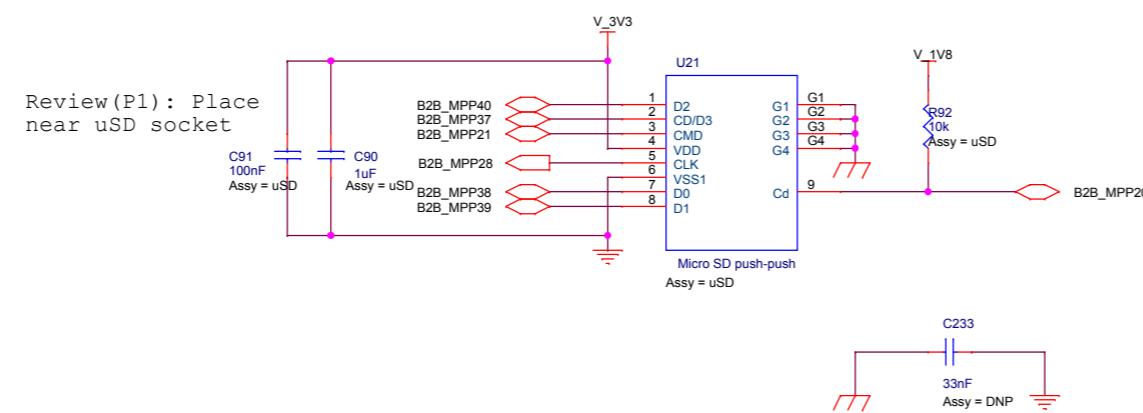
Bypass capacitors for MDIO  
passing underneath GNDC

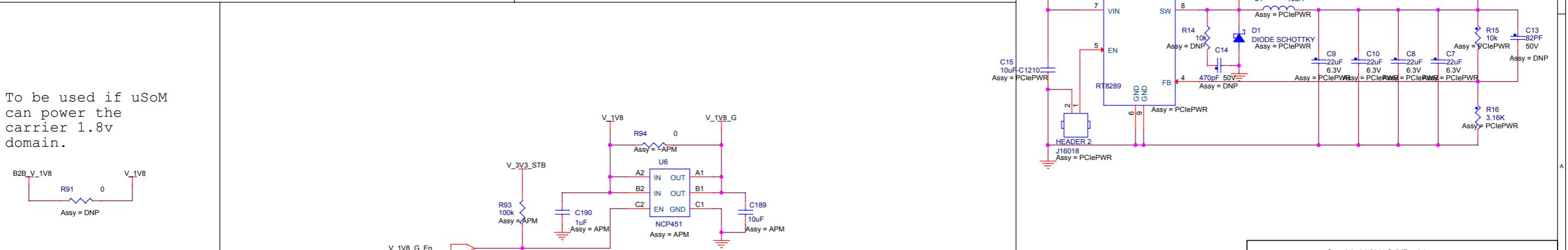
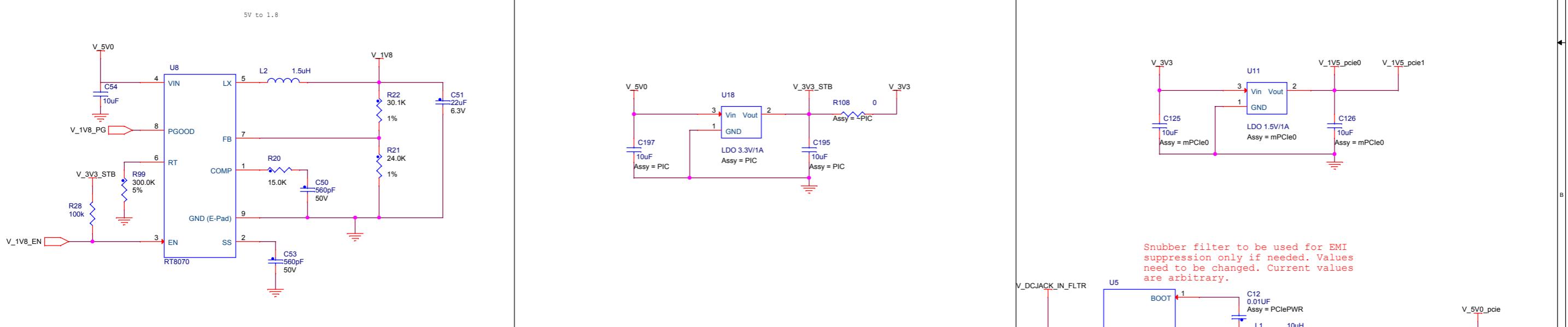
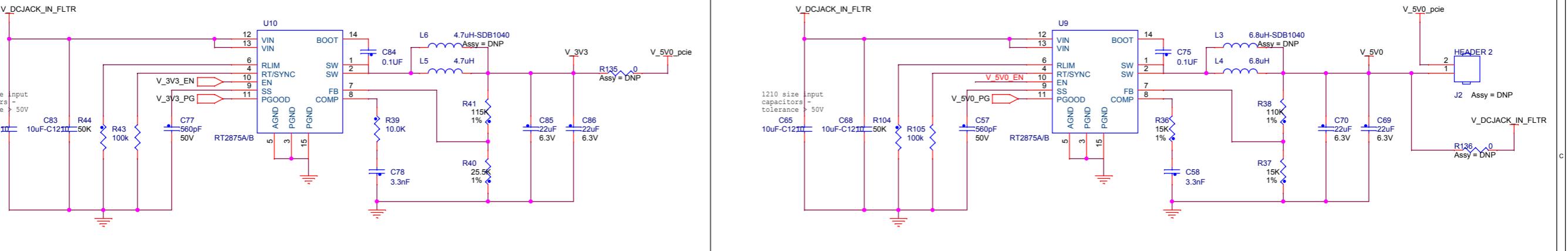
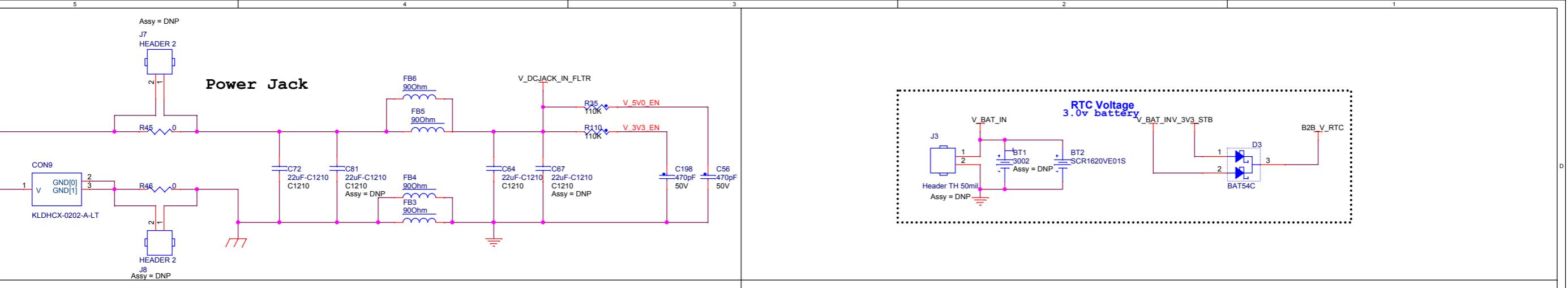


B2B\_SYSRST\_INn → B2B\_SYSRST\_OUTn

Carrier DC-DC PGOOD Signals will enable CPU DC-DC  
on uSoM. Signal is pulled up on uSom.

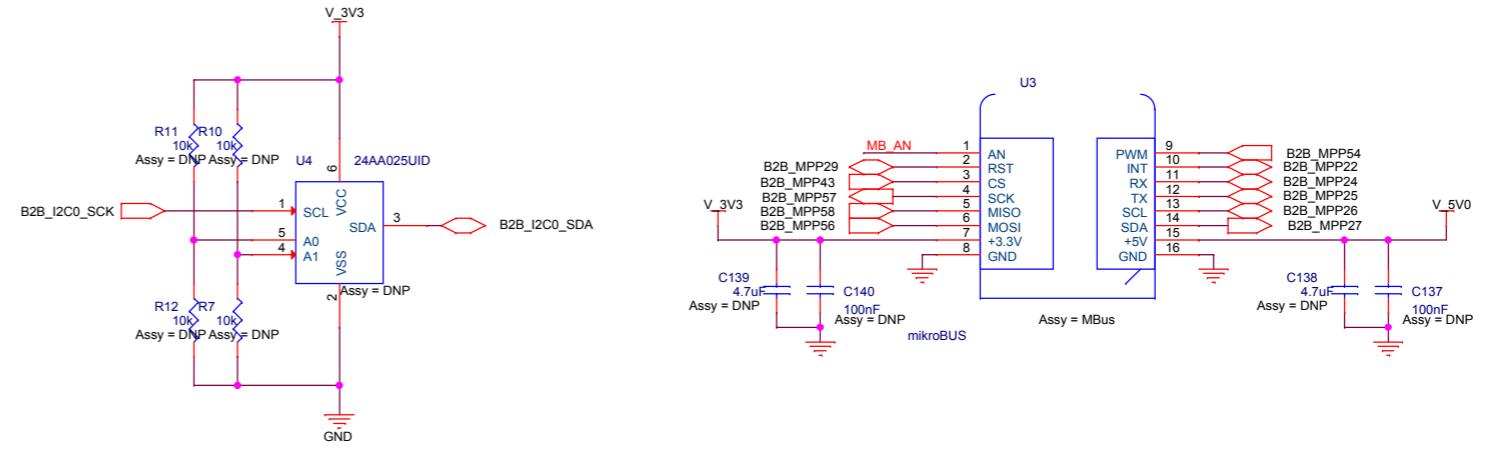
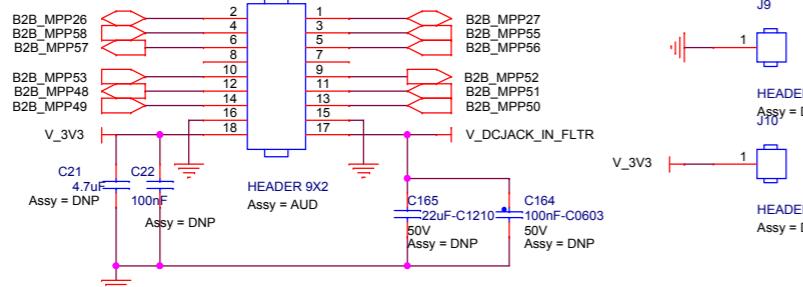




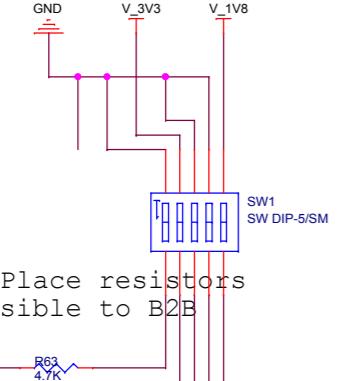


To be used if uSoM can power the carrier 1.8v domain.

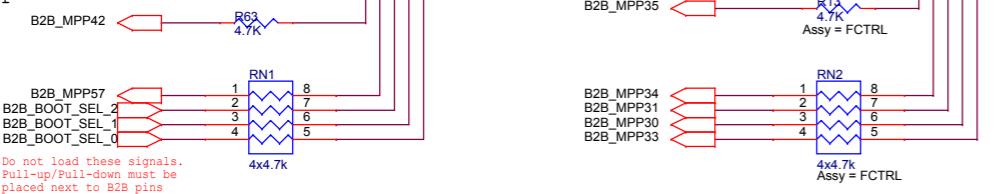
### SLIC TDM Module connectors



Internally pulled to 0x36:  
110110

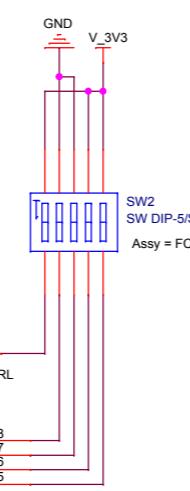


Layout (P1): Place resistors as close possible to B2B pins.



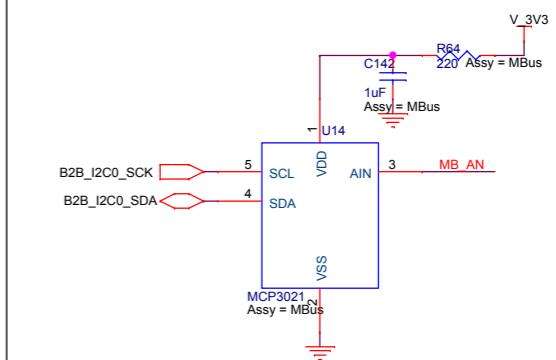
Do not load these signals.  
Pull-up/Pull-down must be placed next to B2B pins

Internally pulled to 0x0c:  
01100

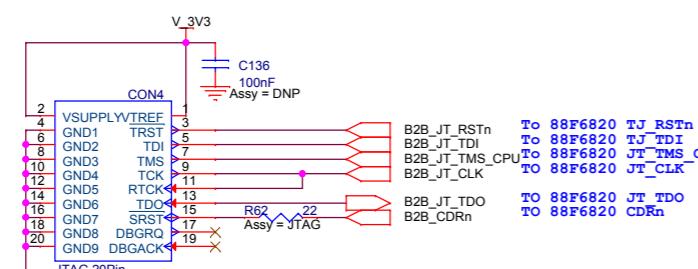


PART NO.	XX	X	/XX																																				
Device	Address Options	Temperature Range	Package																																				
Device: MCP3021T: 10-Bit 2-Wire Serial A/D Converter (Tape and Reel)																																							
Temperature Range: E = -40°C to +125°C																																							
Address Options:																																							
<table border="1"> <tr> <th>XX</th><th>A2</th><th>A1</th><th>A0</th></tr> <tr> <td>A0</td><td>= 0</td><td>0</td><td>0</td></tr> <tr> <td>A1</td><td>= 0</td><td>0</td><td>1</td></tr> <tr> <td>A2</td><td>= 0</td><td>1</td><td>0</td></tr> <tr> <td>A3</td><td>= 0</td><td>1</td><td>1</td></tr> <tr> <td>A4</td><td>= 1</td><td>0</td><td>0</td></tr> <tr> <td>A5 *</td><td>= 1</td><td>0</td><td>1</td></tr> <tr> <td>A6</td><td>= 1</td><td>1</td><td>0</td></tr> <tr> <td>A7</td><td>= 1</td><td>1</td><td>1</td></tr> </table>				XX	A2	A1	A0	A0	= 0	0	0	A1	= 0	0	1	A2	= 0	1	0	A3	= 0	1	1	A4	= 1	0	0	A5 *	= 1	0	1	A6	= 1	1	0	A7	= 1	1	1
XX	A2	A1	A0																																				
A0	= 0	0	0																																				
A1	= 0	0	1																																				
A2	= 0	1	0																																				
A3	= 0	1	1																																				
A4	= 1	0	0																																				
A5 *	= 1	0	1																																				
A6	= 1	1	0																																				
A7	= 1	1	1																																				
* Default option. Contact Microchip factory for other address options																																							
Package: OT = SOT-23, 5-lead (Tape and Reel)																																							

- Examples:
- a) MCP3021A0T-E/OT: Extended, A0 Address, Tape and Reel
  - b) MCP3021A1T-E/OT: Extended, A1 Address, Tape and Reel
  - c) MCP3021A2T-E/OT: Extended, A2 Address, Tape and Reel
  - d) MCP3021A3T-E/OT: Extended, A3 Address, Tape and Reel
  - e) MCP3021A4T-E/OT: Extended, A4 Address, Tape and Reel
  - f) MCP3021A5T-E/OT: Extended, A5 Address, Tape and Reel
  - g) MCP3021A6T-E/OT: Extended, A6 Address, Tape and Reel
  - h) MCP3021A7T-E/OT: Extended, A7 Address, Tape and Reel



RESET button



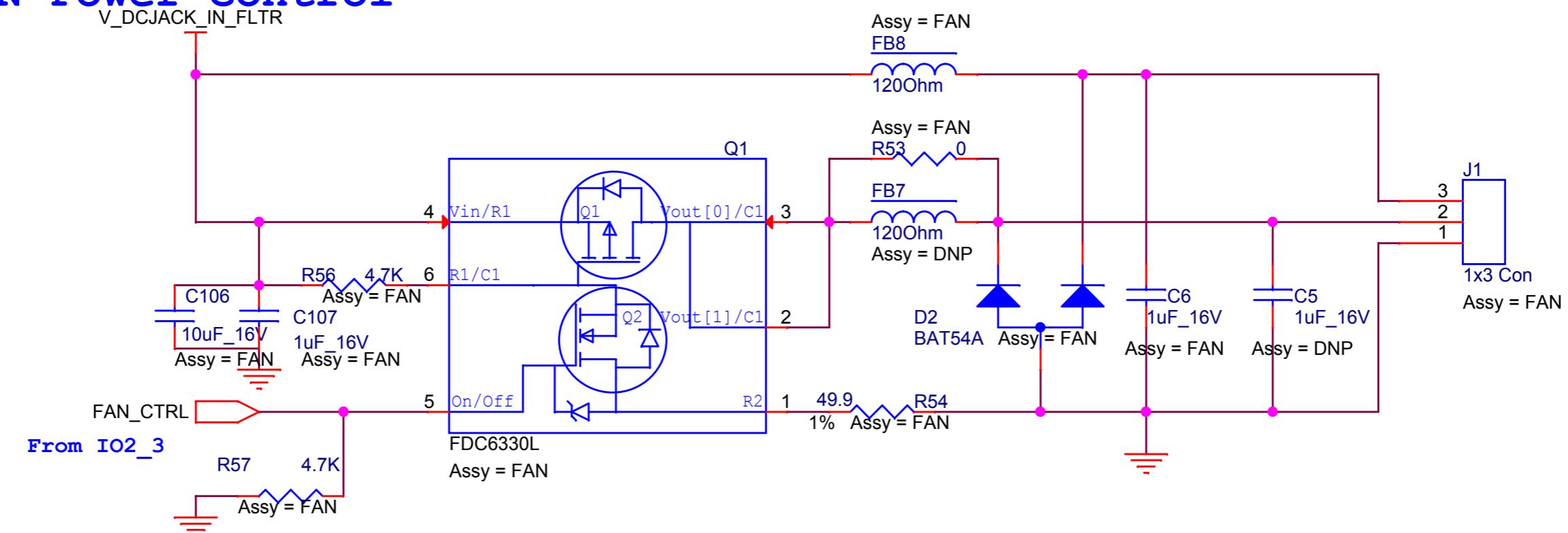
**PCA9555**  
16-bit I2C and SMBus I/O port with interrupt  
5 V tolerant I/Os

I/O port  
When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input with a weak pull-up to VDD. The input voltage may be raised above VDD to a maximum of 5.5 V

#### I/O Table

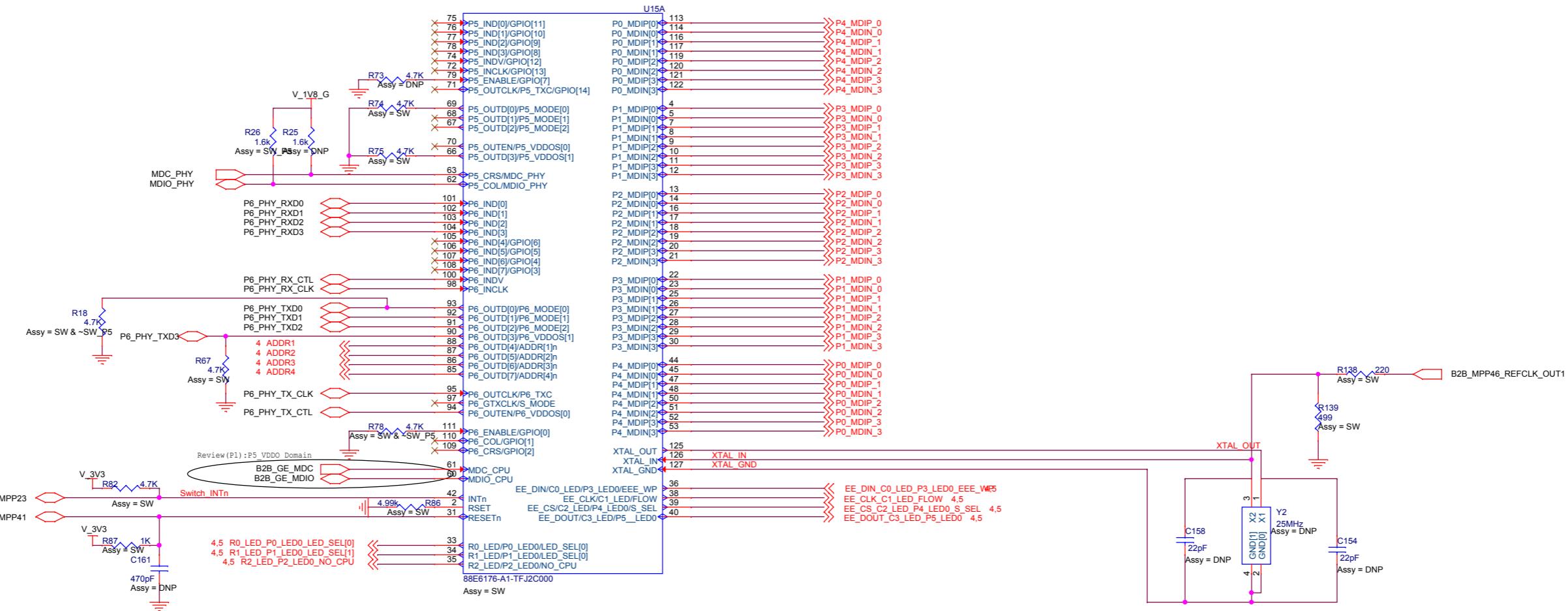
I02_0	I02_1	I02_2	I02_3	I02_4	I02_5	I02_6	I02_7	I03_0	I03_1	I03_2	I03_3	I03_4	I03_5	I03_6	I03_7	I04_0_0	I04_0_1	I04_0_2	I04_0_3	I04_0_4	I04_0_5	I04_0_6	I04_0_7	I04_1_0	I04_1_1	I04_1_2	I04_1_3	I04_1_4	I04_1_5	I04_1_6	I04_1_7
I02_0	I02_1	I02_2	I02_3	I02_4	I02_5	I02_6	I02_7	I03_0	I03_1	I03_2	I03_3	I03_4	I03_5	I03_6	I03_7	I04_0_0	I04_0_1	I04_0_2	I04_0_3	I04_0_4	I04_0_5	I04_0_6	I04_0_7	I04_1_0	I04_1_1	I04_1_2	I04_1_3	I04_1_4	I04_1_5	I04_1_6	I04_1_7
I02_8	I02_9	I02_10	I02_11	I02_12	I02_13	I02_14	I02_15	I03_8	I03_9	I03_10	I03_11	I03_12	I03_13	I03_14	I03_15	I04_1_8	I04_1_9	I04_1_10	I04_1_11	I04_1_12	I04_1_13	I04_1_14	I04_1_15	I04_2_0	I04_2_1	I04_2_2	I04_2_3	I04_2_4	I04_2_5	I04_2_6	I04_2_7
I02_16	I02_17	I02_18	I02_19	I02_20	I02_21	I02_22	I02_23	I03_16	I03_17	I03_18	I03_19	I03_20	I03_21	I03_22	I03_23	I04_2_8	I04_2_9	I04_2_10	I04_2_11	I04_2_12	I04_2_13	I04_2_14	I04_2_15	I04_3_0	I04_3_1	I04_3_2	I04_3_3	I04_3_4	I04_3_5	I04_3_6	I04_3_7
I02_24	I02_25	I02_26	I02_27	I02_28	I02_29	I02_30	I02_31	I03_24	I03_25	I03_26	I03_27	I03_28	I03_29	I03_30	I03_31	I04_3_8	I04_3_9	I04_3_10	I04_3_11	I04_3_12	I04_3_13	I04_3_14	I04_3_15	I04_4_0	I04_4_1	I04_4_2	I04_4_3	I04_4_4	I04_4_5	I04_4_6	I04_4_7
I02_32	I02_33	I02_34	I02_35	I02_36	I02_37	I02_38	I02_39	I03_32	I03_33	I03_34	I03_35	I03_36	I03_37	I03_38	I03_39	I04_4_8	I04_4_9	I04_4_10	I04_4_11	I04_4_12	I04_4_13	I04_4_14	I04_4_15	I04_5_0	I04_5_1	I04_5_2	I04_5_3	I04_5_4	I04_5_5	I04_5_6	I04_5_7
I02_40	I02_41	I02_42	I02_43	I02_44	I02_45	I02_46	I02_47	I03_40	I03_41	I03_42	I03_43	I03_44	I03_45	I03_46	I03_47	I04_5_8	I04_5_9	I04_5_10	I04_5_11	I04_5_12	I04_5_13	I04_5_14	I04_5_15	I04_6_0	I04_6_1	I04_6_2	I04_6_3	I04_6_4	I04_6_5	I04_6_6	I04_6_7
I02_48	I02_49	I02_50	I02_51	I02_52	I02_53	I02_54	I02_55	I03_48	I03_49	I03_50	I03_51	I03_52	I03_53	I03_54	I03_55	I04_6_8	I04_6_9	I04_6_10	I04_6_11	I04_6_12	I04_6_13	I04_6_14	I04_6_15	I04_7_0	I04_7_1	I04_7_2	I04_7_3	I04_7_4	I04_7_5	I04_7_6	I04_7_7
I02_56	I02_57	I02_58	I02_59	I02_60	I02_61	I02_62	I02_63	I03_56	I03_57	I03_58	I03_59	I03_60	I03_61	I03_62	I03_63	I04_7_8	I04_7_9	I04_7_10	I04_7_11	I04_7_12	I04_7_13	I04_7_14	I04_7_15	I04_8_0	I04_8_1	I04_8_2	I04_8_3	I04_8_4	I04_8_5	I04_8_6	I04_8_7
I02_64	I02_65	I02_66	I02_67	I02_68	I02_69	I02_70	I02_71	I03_64	I03_65	I03_66	I03_67	I03_68	I03_69	I03_70	I03_71	I04_8_8	I04_8_9	I04_8_10	I04_8_11	I04_8_12	I04_8_13	I04_8_14	I04_8_15	I04_9_0	I04_9_1	I04_9_2	I04_9_3	I04_9_4	I04_9_5	I04_9_6	I04_9_7
I02_72	I02_73	I02_74	I02_75	I02_76	I02_77	I02_78	I02_79	I03_72	I03_73	I03_74	I03_75	I03_76	I03_77	I03_78	I03_79	I04_9_8	I04_9_9	I04_9_10	I04_9_11	I04_9_12	I04_9_13	I04_9_14	I04_9_15	I04_10_0	I04_10_1	I04_10_2	I04_10_3	I04_10_4	I04_10_5	I04_10_6	I04_10_7
I02_80	I02_81	I02_82	I02_83	I02_84	I02_85	I02_86	I02_87	I03_80	I03_81	I03_82	I03_83	I03_84	I03_85	I03_86	I03_87	I04_10_8	I04_10_9	I04_10_10	I04_10_11	I04_10_12	I04_10_13	I04_10_14	I04_10_15	I04_11_0	I04_11_1	I04_11_2	I04_11_3	I04_11_4	I04_11_5	I04_11_6	I04_11_7
I02_88	I02_89	I02_90	I02_91	I02_92	I02_93	I02_94	I02_95	I03_88	I03_89	I03_90	I03_91	I03_92	I03_93	I03_94	I03_95	I04_11_8	I04_11_9	I04_11_10	I04_11_11	I04_11_12	I04_11_13	I04_11_14	I04_11_15	I04_12_0	I04_12_1	I04_12_2	I04				

## FAN Power Control

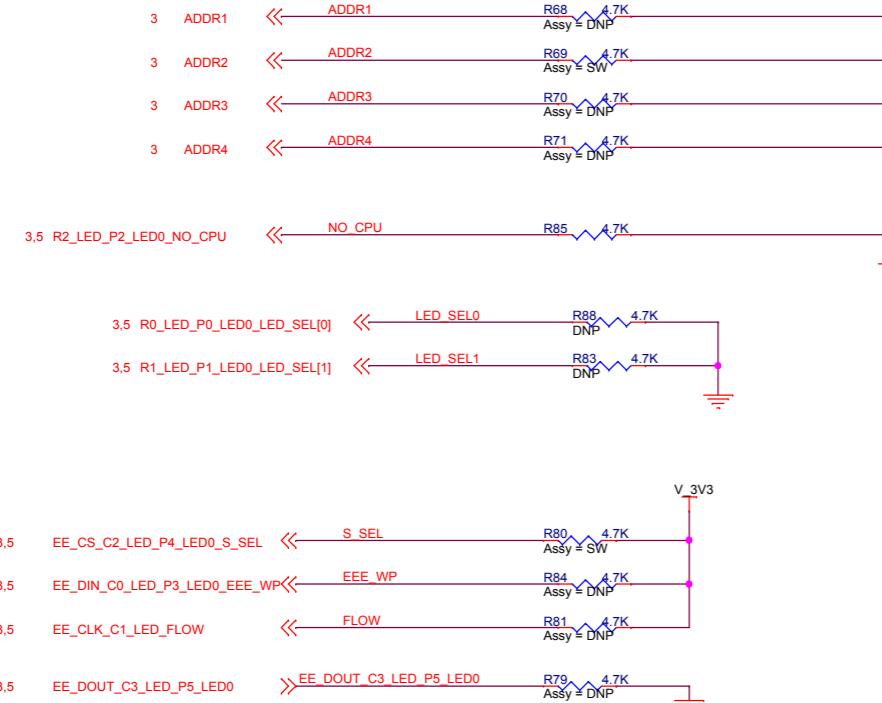


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Size	Title	Rev
A	ClearFog Pro Evaluation Board	
	Date: Wednesday, October 28, 2015	Rev Rev-2.1



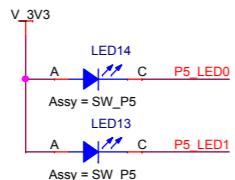
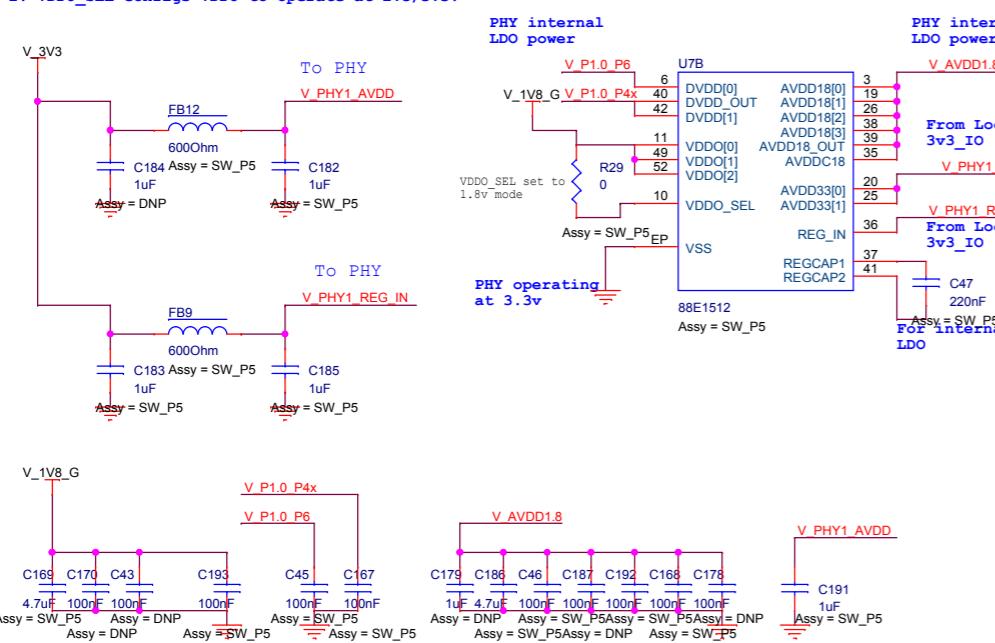
**ADDR0 = always 0x0**  
**SMI ADDRESS is the inverted value = 0x4**



Pin	Name	Functionality	Default	Jumper/ DPR
35	NO_CPU	CPU ATTACHED	PU	PD.NC
34	LED_SEL[1]	LED Functionality	PU	PD.NC
33	LED_SEL[0]	LED Functionality	PU	PD.NC
39	S_SEL	Connect serdes to port 4 or 5	PD	PU
38	FLOW	Advertise auto-neg flow control	PD	PU
36	EEE_WP	Enable energy efficient Ethernet	PD	PU.NC
70	P5_VDDOS[0]	Port 5 power rail select	PU	PD
66	P5_VDDOS[1]	Port 5 power rail select	PU	PU
67,68,69	P5_OUTD[2:0]	0x7 = RGMII	PU	No option
94	P6_VDDOS[0]	Port 6 power rail select	PU	PD
90	P6_VDDOS[1]	Port 6 power rail select	PU	PU
91,92,93	P6_OUTD[2:0]	0x7 = RGMII	PU	No option
85,86,87,88	ADDR[4:1]n	SMI ADDRESS	PU	0x2

## PHY Power configurations

88E1512 power configurations:  
1. using internal lv8 and lv0 regulators.  
2. VDDO SEL configs VDDO to operate at 2v5/3v3.



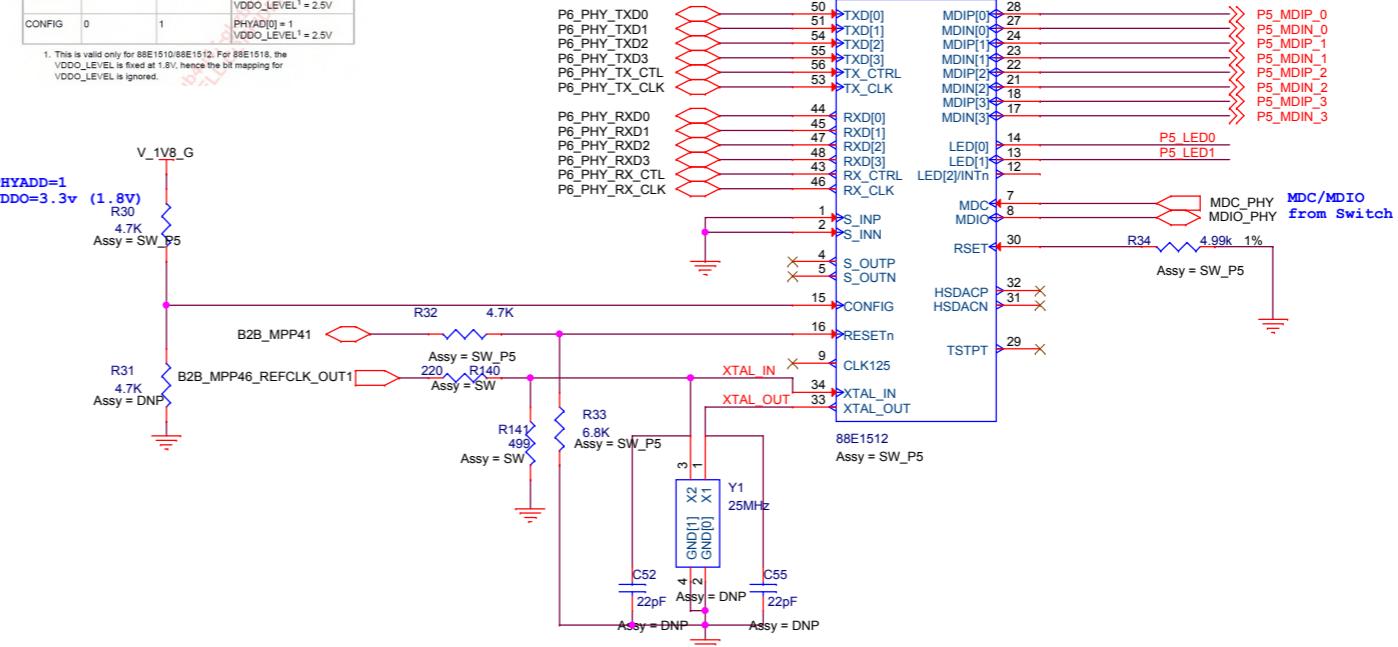
## PHYADD configuration

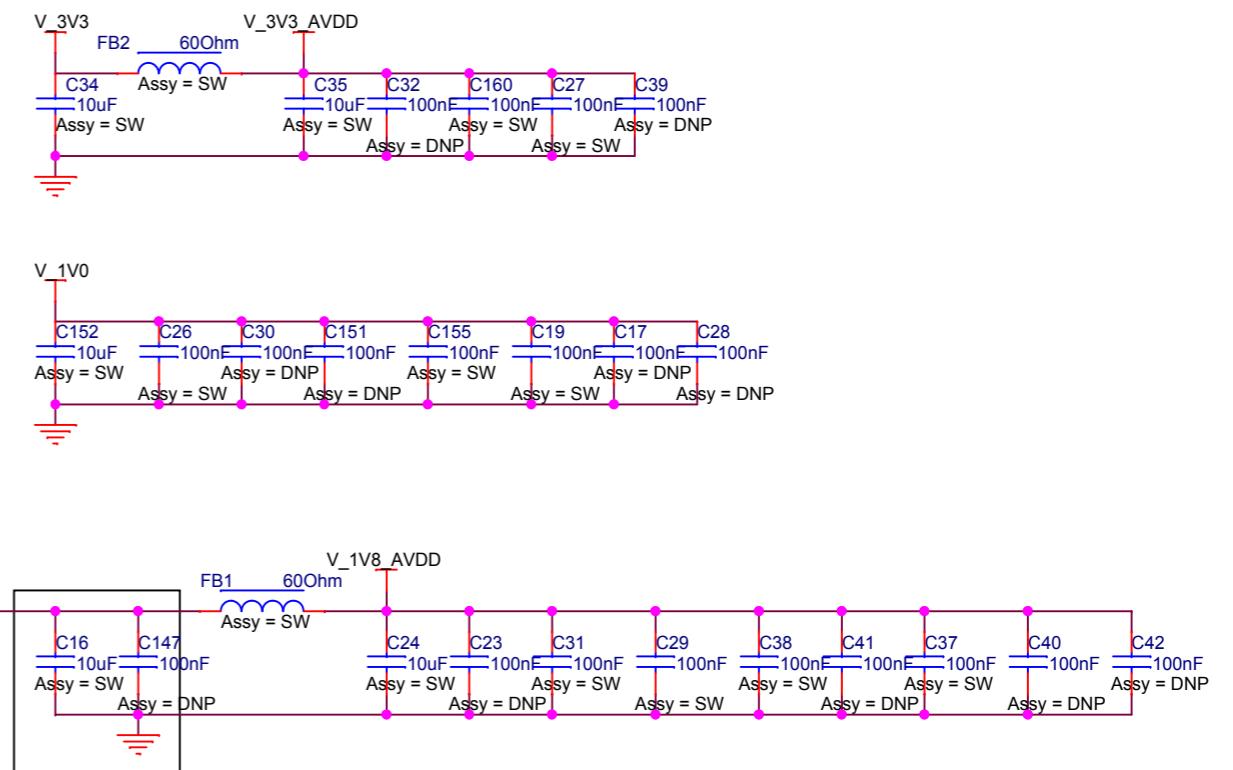
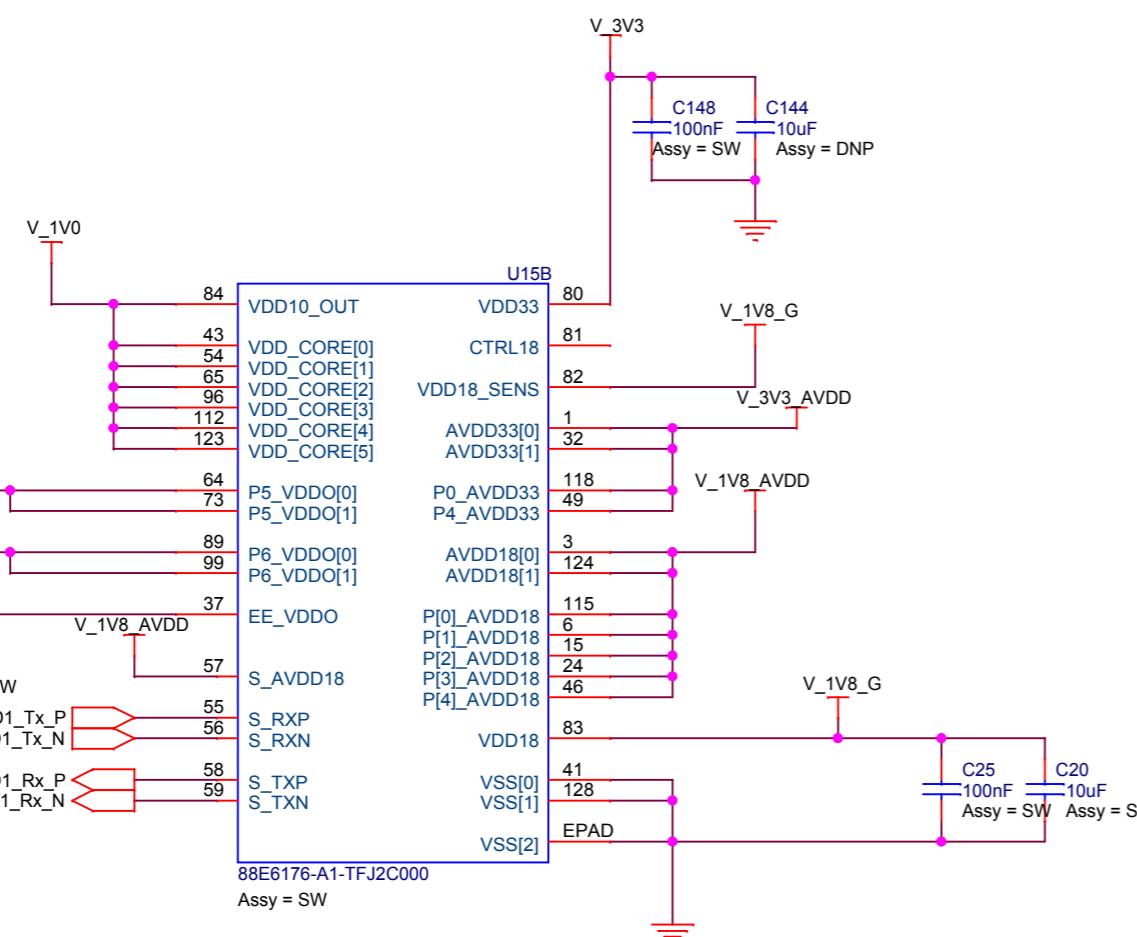
## 88E1512 PHY configuration options:

Table 53: Configuration Mapp

Pin	CONFIG Bit 1	CONFIG Bit 0	Value Assignment
CONFIG	0	0	PHYAD[0] = 0 VDDO_LEVEL = 0
CONFIG	1	1	PHYAD[0] = 1 VDDO_LEVEL = 1
CONFIG	1	0	PHYAD[0] = 0 VDDO_LEVEL = 1
CONFIG	0	1	PHYAD[0] = 1 VDDO_LEVEL = 0

1. This is valid only for 88E1510/88E1512. For 88E1511/VDDO\_LEVEL is fixed at 1.8V, hence the bit n<sub>1</sub> is ignored.

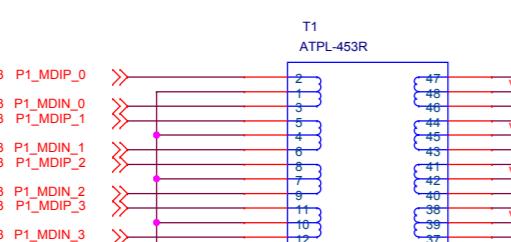




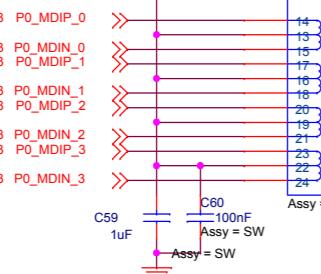
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Size	Title	Rev
B	ClearFog Pro Evaluation Board	Rev Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 18 of 19	

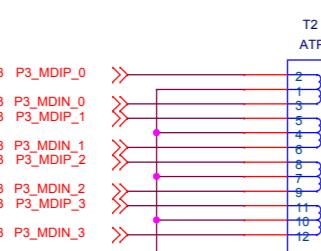
### PORT-1 MDI I/F



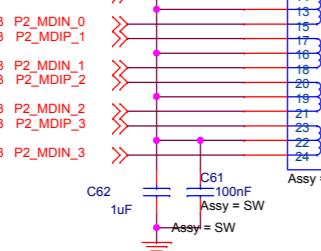
### PORT-0 MDI I/F



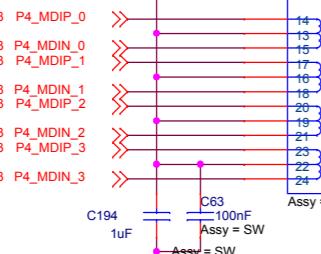
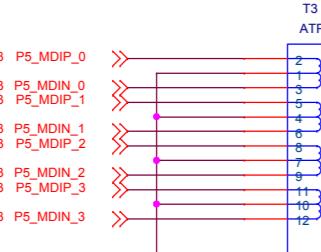
### PORT-3 MDI I/F



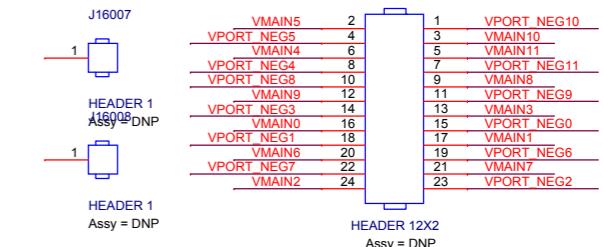
### PORT-2 MDI I/F



### PORT-4 MDI I/F



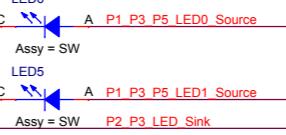
PoE Module connector, including two mechanical pins



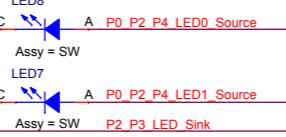
LED1 = Gig Link  
LEDO = Link\Act



LED1 = Gig Link  
LEDO = Link\Act



LED1 = Gig Link  
LEDO = Link\Act



LED1 = Gig Link  
LEDO = Link\Act



LED1 = Gig Link  
LEDO = Link\Act



R2\_LED\_P2\_LED0\_NO\_CPU → R47\_150-R0603\_P4\_P5\_LED\_Sink  
R1\_LED\_P1\_LED0\_LED\_SEL[1] → R48\_150-R0603\_P3\_P4\_LED\_Sink  
R0\_LED\_P0\_LED0\_LED\_SEL[0] → R49\_150-R0603\_P0\_P1\_LED\_Sink

P1\_P3\_P5\_LED1\_Source → EE\_DOUT\_C3\_LED\_P5\_LED  
P0\_P2\_P4\_LED1\_Source → EE\_CS\_C2\_LED\_P4\_LED0\_S\_SEL  
P1\_P3\_P5\_LED0\_Source → EE\_CLK\_C1\_LED\_FLOW  
P0\_P2\_P4\_LED0\_Source → EE\_DIN\_CO\_LED\_P3\_LED\_EEE\_WP

C0 LED	C1 LED	C2 LED	C3 LED
R0 LED	Port 0 LED 0	Port 0 LED 1	Port 1 LED 1
R1 LED	Port 2 LED 0	Port 3 LED 0	Port 2 LED 1
R2 LED	Port 4 LED 0	Port 5 LED 0	Port 4 LED 1