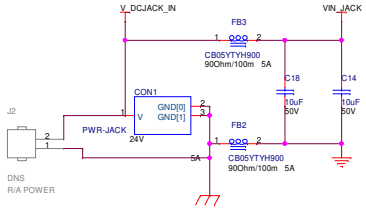
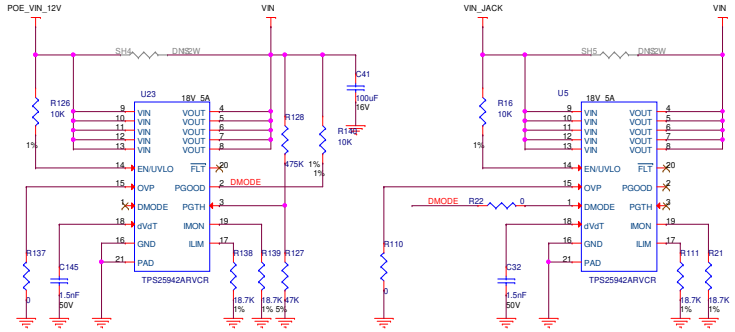
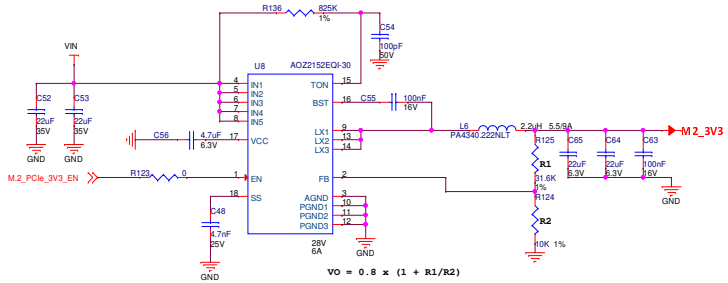


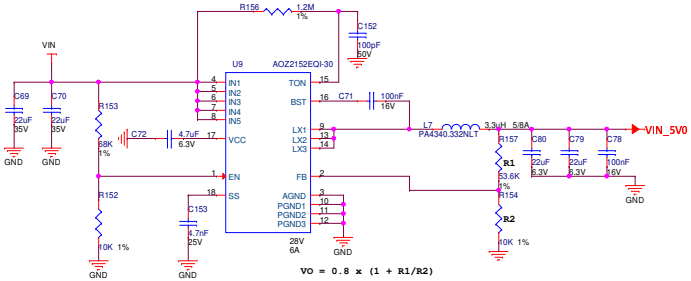
SH4, SH5 bypass U40 and U41 when Vin is a sigle source (Adapter or POE)



3V3/6A powers the M.2 and Mini-PCIe modules



5V/6A powers the SOM and USB power out



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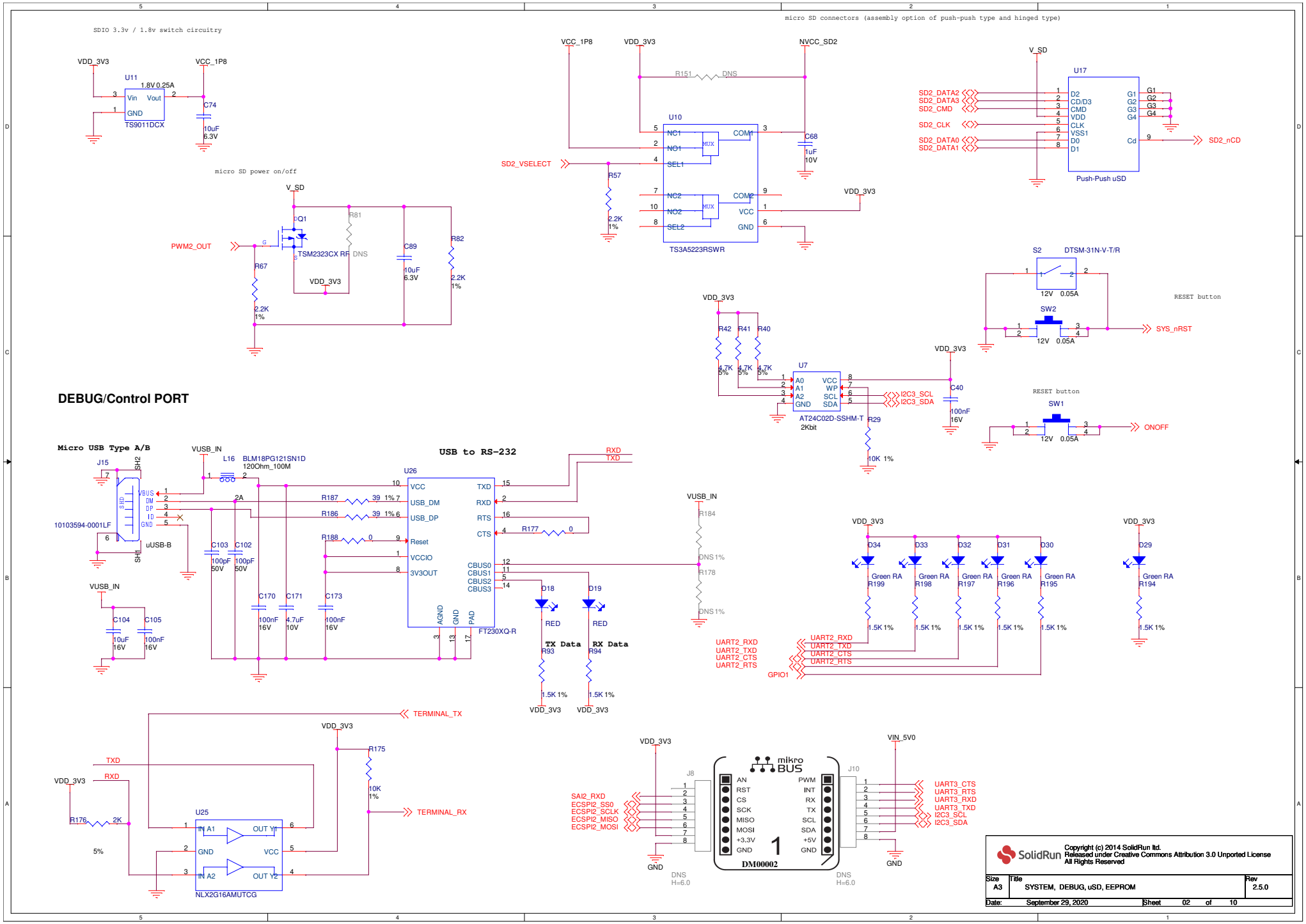
Size	Title	Rev
C	POWER	2.5.0
Date: September 29, 2020	Sheet 01 of 10	


SDIO 3.3v / 1.8v switch circuitry
micro SD connectors (assembly option of push-push type and hinged type)
micro SD power on/off
DEBUG/Control PORT
Micro USB Type A/B
USB to RS-232
RESET button
RESET button
Push-Push uSD
TS3A5223RSWR
AT24C02D-SSHM-T
2Kbit
FT230XQ-R
NLX2G16AMUTCG
TS9011DCX
TSM2323CX RF
DTSM-31N-V-T/R
10103594-0001LF
mikro BUS
DM00002
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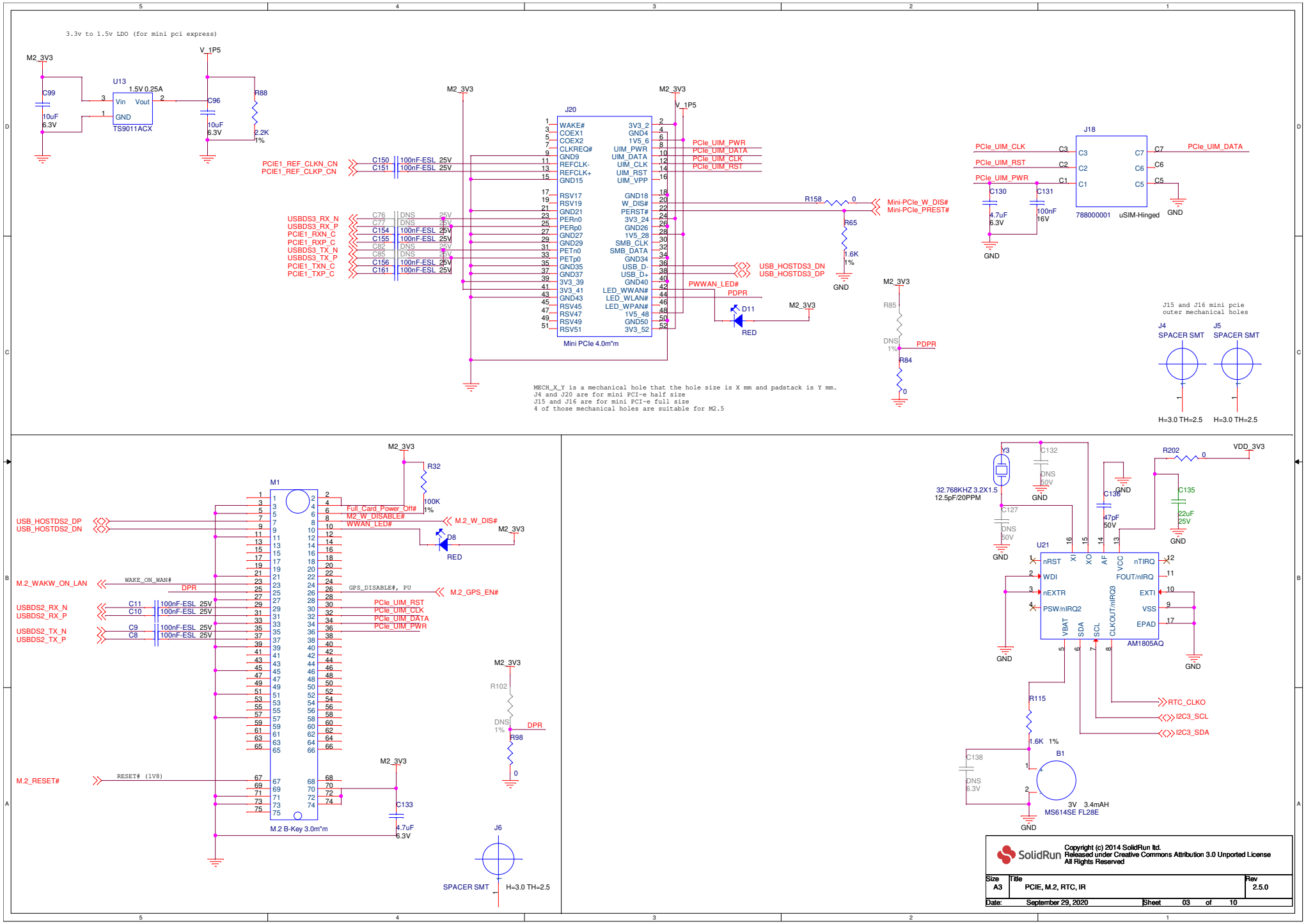
SYSTEM, DEBUG, uSD, EEPROM
September 29, 2020
Sheet 02 of 10
Rev 2.5.0


3.3v to 1.5v LDO (for mini pci express)
M2_3V3
V_1P5
U13
1.5V 0.25A
Vin
Vout
GND
TS9011ACX
C99
10uF
6.3V
C96
10uF
6.3V
R88
2.2K
1%
J20
Mini PCIe 4.0m*m
PCIE1_REF_CLKN_CN
PCIE1_REF_CLKP_CN
C150
C151
100nF-ESL 25V
USBDS3_RX_N
USBDS3_RX_P
PCIE1_RXN_C
PCIE1_RXP_C
USBDS3_TX_N
USBDS3_TX_P
PCIE1_TXN_C
PCIE1_TXP_C
C76
C77
C154
C155
C82
C85
C156
C161
DNS
PCIe_UIM_PWR
PCIe_UIM_DATA
PCIe_UIM_CLK
PCIe_UIM_RST
R158
Mini-PCIe_W_DIS#
Mini-PCIe_PREST#
R65
1.6K
1%
USB_HOSTDS3_DN
USB_HOSTDS3_DP
PWWAN_LED#
PDPR
D11
RED
R85
R84
J18
788000001
uSIM-Hinged
PCIe_UIM_CLK
PCIe_UIM_RST
PCIe_UIM_PWR
PCIe_UIM_DATA
C130
C131
4.7uF
6.3V
100nF
16V
J15 and J16 mini pcie
outer mechanical holes
J4
SPACER SMT
J5
SPACER SMT
H=3.0 TH=2.5
MECH_X_Y is a mechanical hole that the hole size is X mm and padstack is Y mm.
J4 and J20 are for mini PCI-e half size
J15 and J16 are for mini PCI-e full size
4 of those mechanical holes are suitable for M2.5
M1
M.2 B-Key 3.0m*m
R32
100K
1%
Full_Card_Power_Off#
M2_W_DISABLE#
WWAN_LED#
M.2_W_DIS#
D8
RED
USB_HOSTDS2_DP
USB_HOSTDS2_DN
M.2_WAKW_ON_LAN
WAKE_ON_WAN#
DPR
GPS_DISABLE#, PU
M.2_GPS_EN#
USBDS2_RX_N
USBDS2_RX_P
USBDS2_TX_N
USBDS2_TX_P
C11
C10
C9
C8
PCIe_UIM_RST
PCIe_UIM_CLK
PCIe_UIM_DATA
PCIe_UIM_PWR
R102
R98
M.2_RESET#
RESET# (1V8)
C133
4.7uF
6.3V
J6
SPACER SMT
H=3.0 TH=2.5
Y3
32.768KHZ 3.2X1.5
12.5pF/20PPM
C132
C127
C136
47pF
50V
R202
VDD_3V3
C135
22uF
25V
U21
AM1805AQ
nRST
WDI
nEXTR
PSW/nIRQ2
nTIRQ
FOUT/nIRQ
EXTI
VSS
EPAD
VBAT
SDA
SCL
CLKOUT/nIRQ3
R115
1.6K 1%
RTC_CLKO
I2C3_SCL
I2C3_SDA
C138
B1
3V 3.4mAH
MS614SE FL28E
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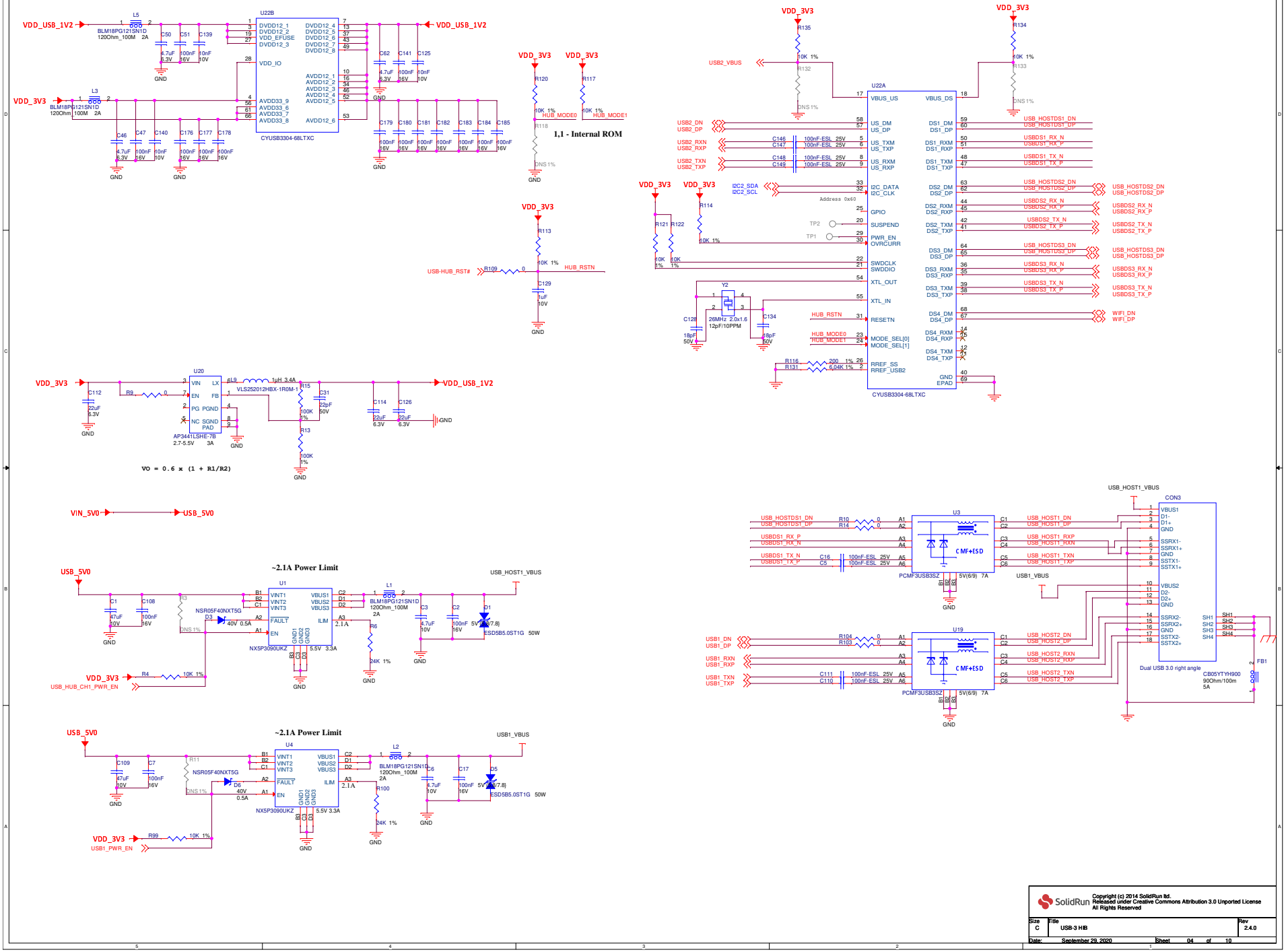
Size A3
Title PCIE, M.2, RTC, IR
Rev 2.5.0
Date: September 29, 2020
Sheet 03 of 10



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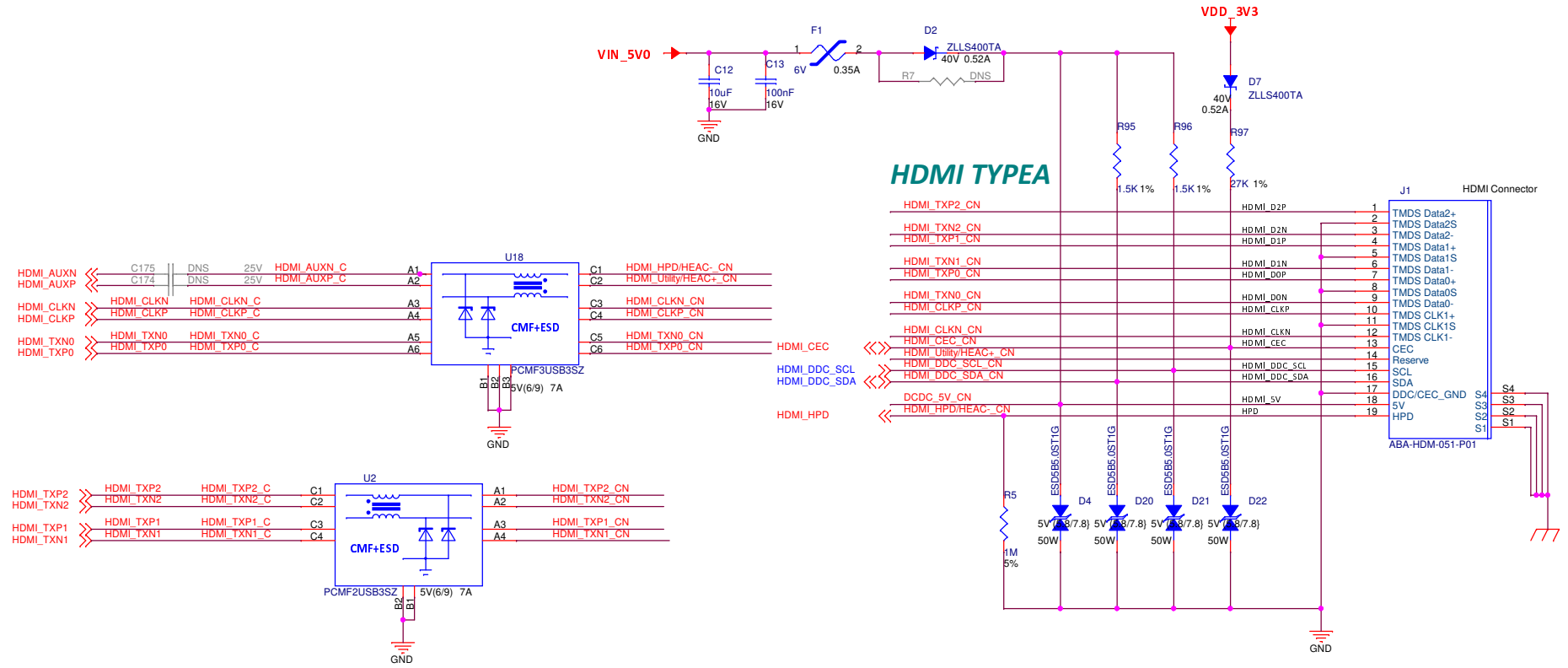
Size	Title	Rev
C	USB-3 HIB	2.4.0
Date: September 29, 2020	Sheet 04 of 10	



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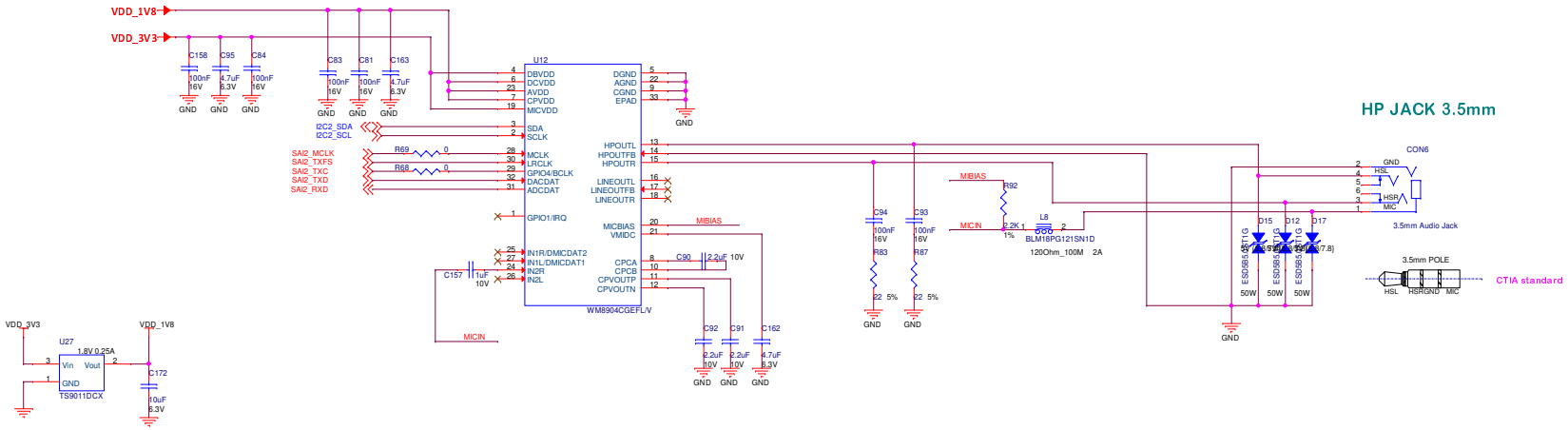
Size	Title	Rev
B	HDMI	2.5.0
Date:	September 29, 2020	Sheet 05 of 10

Audio DAC



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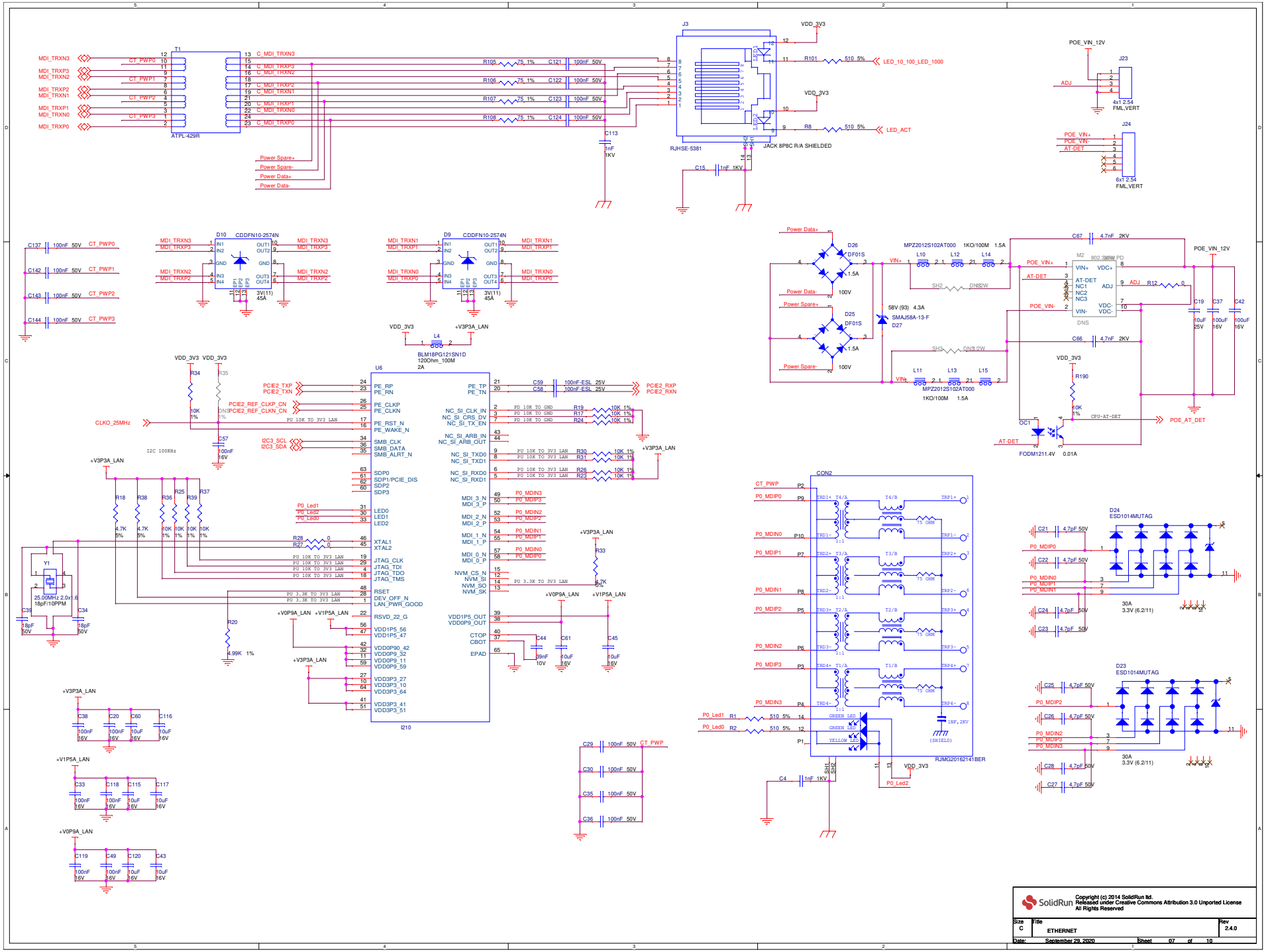
Size	Title	Rev
C	AUDIO	2.5.0

Date: September 29, 2020 Sheet 06 of 10



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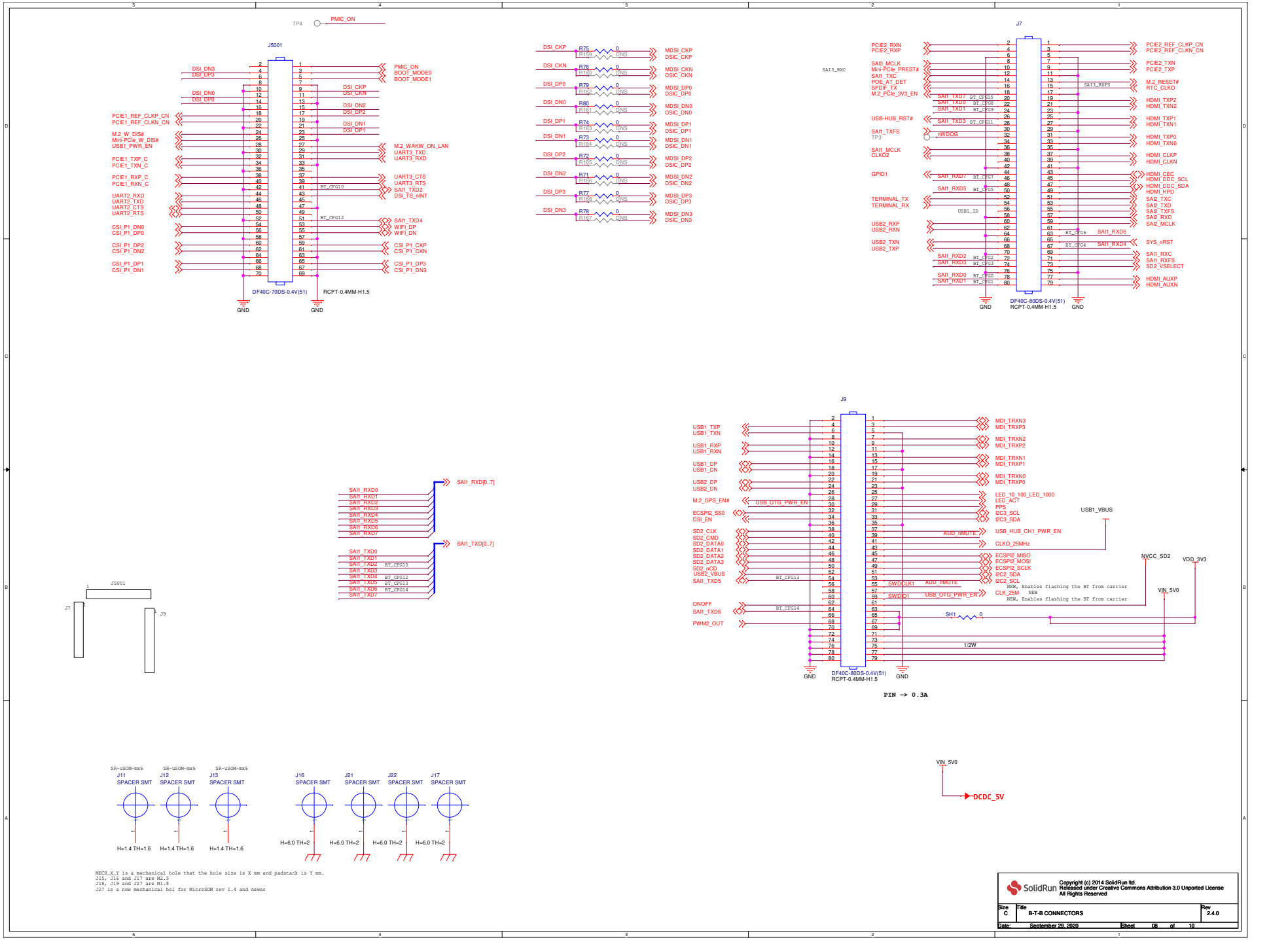
Size	Title	Rev
C	ETHERNET	2.4.0

Date: September 29, 2020 Sheet 07 of 10


TP4
PMIC_ON
J5001
DSI_DN3
DSI_DP3
DSI_DN0
DSI_DP0
PCIE1_REF_CLKP_CN
PCIE1_REF_CLKN_CN
M.2_W_DIS#
Mini-PCIe_W_DIS#
USB1_PWR_EN
PCIE1_TXP_C
PCIE1_TXN_C
PCIE1_RXP_C
PCIE1_RXN_C
UART2_RXD
UART2_TXD
UART2_CTS
UART2_RTS
CSI_P1_DN0
CSI_P1_DP0
CSI_P1_DP2
CSI_P1_DN2
CSI_P1_DP1
CSI_P1_DN1
DSI_CKP
DSI_CKN
DSI_DN2
DSI_DP2
DSI_DN1
DSI_DP1
M.2_WAKW_ON_LAN
UART3_TXD
UART3_RXD
UART3_CTS
UART3_RTS
SAI1_TXD2
DSI_TS_nINT
SAI1_TXD4
WIFI_DP
WIFI_DN
CSI_P1_CKP
CSI_P1_CKN
CSI_P1_DP3
CSI_P1_DN3
PMIC_ON
BOOT_MODE0
BOOT_MODE1
BT_CFG10
BT_CFG12
DF40C-70DS-0.4V(51)
RCPT-0.4MM-H1.5
GND
DSI_CKP
DSI_CKN
DSI_DP0
DSI_DN0
DSI_DP1
DSI_DN1
DSI_DP2
DSI_DN2
DSI_DP3
DSI_DN3
R75
R159
R76
R160
R79
R162
R80
R161
R74
R163
R73
R164
R72
R165
R71
R166
R77
R169
R78
R167
0
DNS
MDSI_CKP
DSIC_CKP
MDSI_CKN
DSIC_CKN
MDSI_DP0
DSIC_DP0
MDSI_DN0
DSIC_DN0
MDSI_DP1
DSIC_DP1
MDSI_DN1
DSIC_DN1
MDSI_DP2
DSIC_DP2
MDSI_DN2
DSIC_DN2
MDSI_DP3
DSIC_DP3
MDSI_DN3
DSIC_DN3
J7
SAI3_RXC
PCIE2_RXN
PCIE2_RXP
SAI3_MCLK
Mini-PCIe_PREST#
SAI1_TXC
PCE_AT_DET
SPDIF_TX
M.2_PCIe_3V3_EN
USB-HUB_RST#
SAI1_TXFS
TP3
nWDOG
SAI1_MCLK
CLKO2
GPIO1
TERMINAL_TX
TERMINAL_RX
USB2_RXP
USB2_RXN
USB2_TXN
USB2_TXP
SAI1_TXD7
SAI1_TXD6
SAI1_TXD1
SAI1_TXD3
SAI1_RXD7
SAI1_RXD5
USB1_ID
SAI1_RXD2
SAI1_RXD3
SAI1_RXD0
SAI1_RXD1
BT_CFG15
BT_CFG8
BT_CFG9
BT_CFG11
BT_CFG7
BT_CFG5
BT_CFG6
BT_CFG4
BT_CFG2
BT_CFG3
BT_CFG0
BT_CFG1
SAI3_RXFS
SAI1_RXD6
SAI1_RXD4
PCIE2_REF_CLKP_CN
PCIE2_REF_CLKN_CN
PCIE2_TXN
PCIE2_TXP
M.2_RESET#
RTC_CLKO
HDMI_TXP2
HDMI_TXN2
HDMI_TXP1
HDMI_TXN1
HDMI_TXP0
HDMI_TXN0
HDMI_CLKP
HDMI_CLKN
HDMI_CEC
HDMI_DDC_SCL
HDMI_DDC_SDA
HDMI_HPD
SAI2_TXC
SAI2_TXD
SAI2_TXFS
SAI2_RXD
SAI2_MCLK
SYS_nRST
SAI1_RXC
SAI1_RXFS
SD2_VSELECT
HDMI_AUXP
HDMI_AUXN
DF40C-80DS-0.4V(51)
RCPT-0.4MM-H1.5
J9
USB1_TXP
USB1_TXN
USB1_RXP
USB1_RXN
USB1_DP
USB1_DN
USB2_DP
USB2_DN
M.2_GPS_EN#
ECSPI2_SS0
DSI_EN
SD2_CLK
SD2_CMD
SD2_DATA0
SD2_DATA1
SD2_DATA2
SD2_DATA3
SD2_nCD
USB2_VBUS
SAI1_TXD5
ONOFF
SAI1_TXD6
PWM2_OUT
MDI_TRXN3
MDI_TRXP3
MDI_TRXN2
MDI_TRXP2
MDI_TRXN1
MDI_TRXP1
MDI_TRXN0
MDI_TRXP0
LED_10_100_LED_1000
LED_ACT
PPS
I2C3_SCL
I2C3_SDA
USB_HUB_CH1_PWR_EN
CLKO_25MHz
ECSPI2_MISO
ECSPI2_MOSI
ECSPI2_SCLK
I2C2_SDA
I2C2_SCL
CLK_25M
NEW, Enables flashing the BT from carrier
SWDCLK1
SWDIO1
AUD_nMUTE
USB_OTG_PWR_EN
BT_CFG13
BT_CFG14
SH1
0
1/2W
USB1_VBUS
NVCC_SD2
VDD_3V3
VIN_5V0
DF40C-80DS-0.4V(51)
RCPT-0.4MM-H1.5
PIN -> 0.3A
SAI1_RXD0
SAI1_RXD1
SAI1_RXD2
SAI1_RXD3
SAI1_RXD4
SAI1_RXD5
SAI1_RXD6
SAI1_RXD7
SAI1_RXD[0..7]
SAI1_TXD0
SAI1_TXD1
SAI1_TXD2
SAI1_TXD3
SAI1_TXD4
SAI1_TXD5
SAI1_TXD6
SAI1_TXD7
SAI1_TXD[0..7]
BT_CFG10
BT_CFG12
BT_CFG13
BT_CFG14
J5001
J7
J9
SR-uSOM-mx6
J11
SPACER SMT
J12
SPACER SMT
J13
SPACER SMT
H=1.4 TH=1.6
J16
SPACER SMT
J21
SPACER SMT
J22
SPACER SMT
J17
SPACER SMT
H=6.0 TH=2
VIN_5V0
DCDC_5V
MECH_X_Y is a mechanical hole that the hole size is X mm and padstack is Y mm.
J15, J16 and J17 are M2.5
J18, J19 and J27 are M1.8
J27 is a new mechanical hol for MicroSOM rev 1.4 and newer
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Size
C
Title
B-T-B CONNECTORS
Rev
2.4.0
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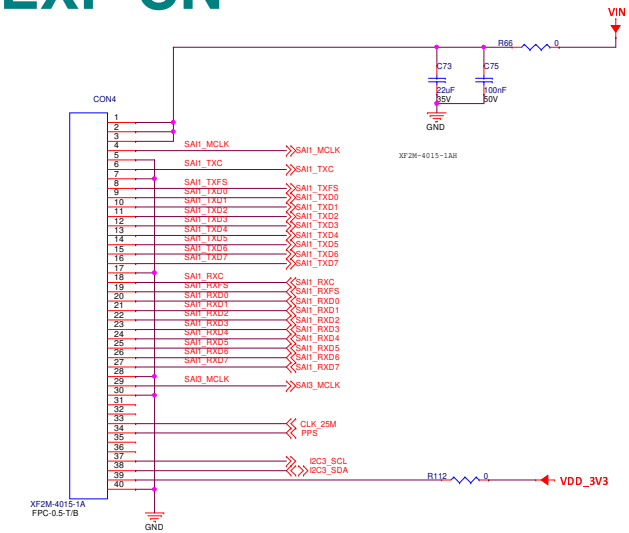
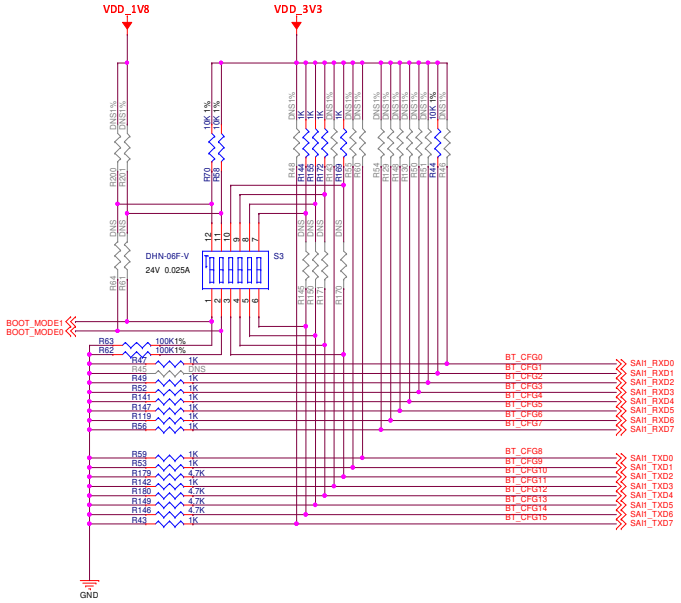
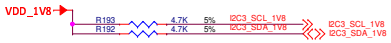
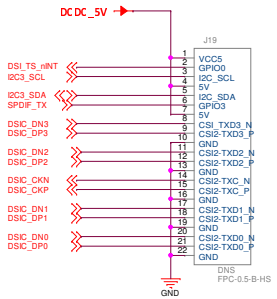
10

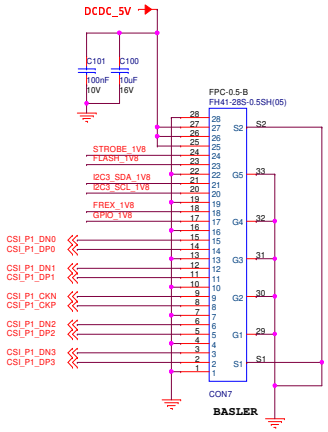
EXP CN

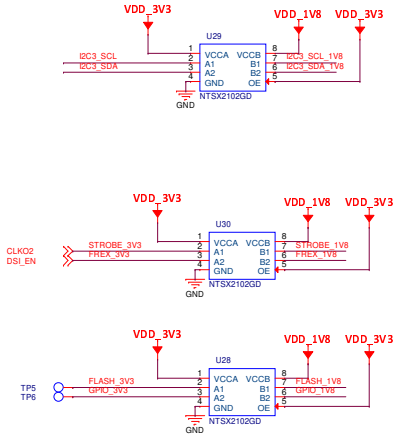












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Size	Title	Rev
C	BOOT, EXP	2.4.0
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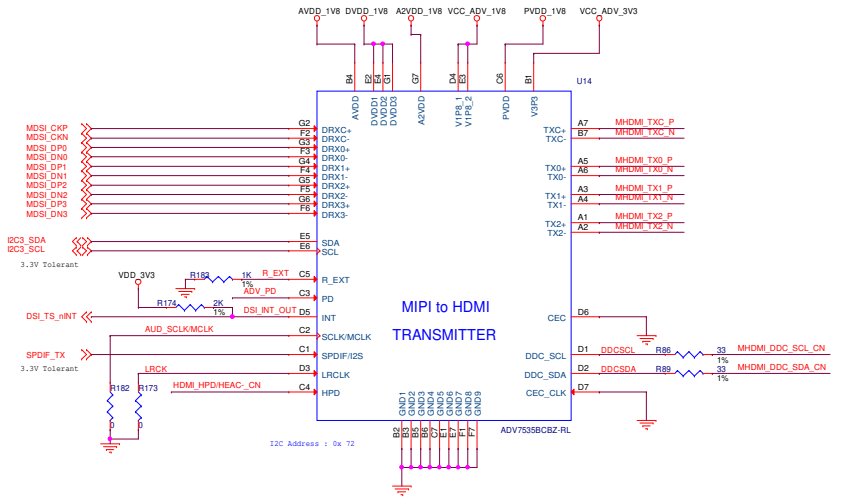

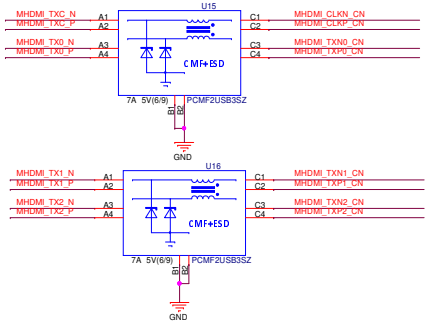

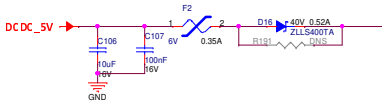

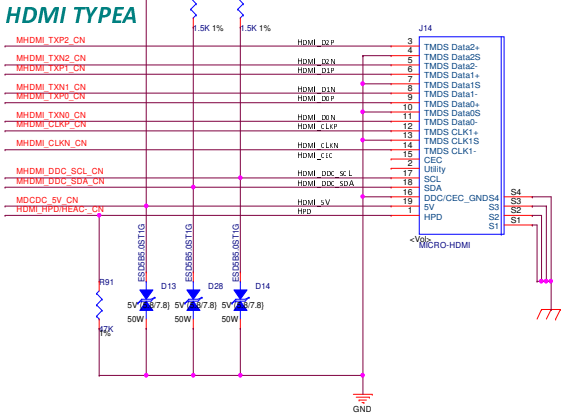

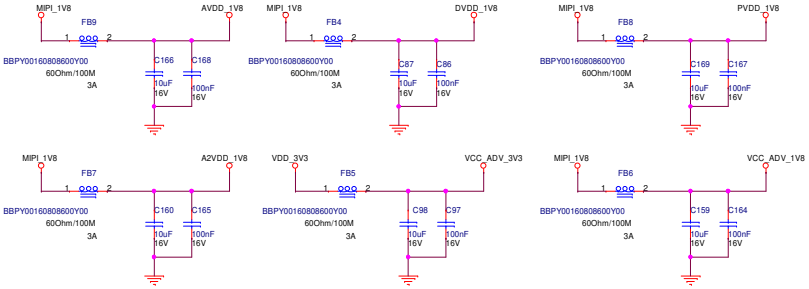

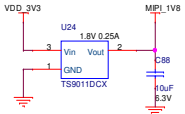

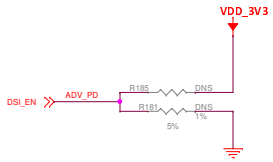

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Size	Title	Rev
C	MIPI-DSI to HDMI	2.4.0
Date: September 29, 2020	Sheet 10 of 10	

Rev. 1.0	Prototype Version
Rev. 2.0	1. Change R257 from 0 Ohm to 100K 2.Adding C297 a 4.7uF on USB Debug 3. Change J35 Routing 4. R23 is assembled instead of R25 to support standalong USB HUB mode 5. Connecting VIN_5V0 to DCDC_5V 6. Cahnging the Power load switch to TPS25942A to support reverse power blocking 7. Changing J5001, J7 and J9 routing to support the new IMX-8 SOM 8. Change the Audio CODEC to WM8904 to suppor IN/OUT 9. Change Y4 from 27MHz to 25MHz
Rev. 2.1	1. Adding R373 and R374 0 Ohm to pull OVP input down for U40 and U41. Taking U37 and U38 out of the BOM and change revision to 2.1.3
Rev. 2.2	New features product
Rev. 2.3	1. Fixing I2C routing on U14 2. Fixing symbols errors on layout - U8, U9 and CON7 3. Changing OC1 position to enable POE module assembly on print side
Rev. 2.3.1	1. R185 is not assembeled
Rev. 2.3.2	1. On HBP ripple adding U27 and C172 to the assembly list to enable VDD_1V8
Rev. 2.4	1. Adding R200 and R201 to enable 1.8V pullup on MODE0 and MODE1 signals (IMX8M-Mini ans IMX8M-Plus) 2. Connecting a reset signal to the Intel NIC. (CLKO_25MHz, J9-41) 3. Changed the B-t-B connector names to J5001, J7 and J9 according to the SOM. 4. Changed J9 to J10 to support item 3.
Rev. 2.5	1. Changed C135 to 100uF in 1210 package 2. Added R202 (1K OHM) between V3V and the RTC power to support slower slew rate on power down. 3. Added C174 and C175 to support IMX8-Plus HDMI 4. Added C176, C177 and C178 to filter USB HUB AVDD power 5. Added C179 - C185 to filter the HUB VDD_USB_1V2 power 6. Placing U18 on CS and changing some of the signals routing to support that 7. Fixing the reset signal to the Intel NIC. (CLKO_25MHz, J9-41) and R35 is not assembled to set reset to "0".

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Size	Title	Rev
B	HISTORY	2.5.0

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