

# 12 MONTHS PROFESSIONAL CERTIFICATION PROGRAM ON

VLSI &  
Semiconductor  
Industry  
Essentials

# TABLE OF CONTENTS

<b>ABOUT THE PROGRAM</b>	<b>01</b>
<b>ABOUT E&amp;ICT ACADEMY IITG</b>	<b>02</b>
<b>ABOUT IIT GUWAHATI</b>	<b>03</b>
<b>KEY FEATURES OF THE PROGRAM</b>	<b>04</b>
<b>ELIGIBILITY CRITERIA &amp; APPLICATION PROCESS</b>	<b>05</b>
<b>TARGET AUDIENCE &amp; PROGRAM OUTCOMES</b>	<b>06</b>
<b>LEARNING PATH VISUALIZATION</b>	<b>07</b>
<b>SEMESTER WISE SYLLABUS</b>	<b>08</b>
<b>CAREER PATHS</b>	<b>18</b>
<b>SAMPLE CERTIFICATES</b>	<b>19</b>
<b>COURSE MENTORS</b>	<b>20</b>
<b>CONTACT US</b>	<b>21</b>

# About the Program

The “VLSI and Semiconductor Essentials” program is an industry-oriented learning track that introduces learners to the fundamentals of foundational Digital Design, Semiconductor Fabrication and Device Design, Hands-on Tool for VLSI and Semiconductor Industry Essentials. It bridges the gap between electronics theory and practical chip design skills, preparing participants for careers in the semiconductor and VLSI industries.

This course is designed for the graduate candidates and will be conducted semester wise where the participants will be introduced to Fundamentals concepts on Digital Design, Semiconductor Fabrication and Device Design, and Hands-on Tool for VLSI. Each semester will last for 3 months (90 hours each semester) and in the final semester Capstone Project and Presentation, Research Methodology and Research Paper Writing will be taught. Also, career counselling with Interview Facing tips and tricks will be taught in the final semester. Thus, this program will be beneficial for the graduate candidates who are interested for further studies and also for those who are interested for career in industry.

The best part of this program is that apart from the theoretical sessions, detailed practical sessions will be conducted in online mode through various platforms like Virtual Labs and tools like MAGIC and SPICE, Xilinx Vivado, Quartus Prime, Questa Sim, Modelsim, NCSIM, VCS/Xcelium, Synopsys DC, FC, ICC Or Cadence Genus, Innovus, CLP or YoSys, OpenRoad Tools and OpenSTA/ PrimeTime/ Tempus. More focus will be on the learning of tools for proper skilling of the participants. The program also emphasizes on industry-relevant skills, including scripting (Python/TCL), automation, and collaborative workflows with version control systems.

Graduates of this program are prepared for roles such as RTL Design Engineer, Verification Engineer, Physical Design Engineer, DFT Engineer, FPGA Engineer, and EDA Tool Specialist across semiconductor companies, fabless design houses, and R&D organizations.

# About E&ICT Academy IIT Guwahati

Electronics & ICT Academy Indian Institute of Technology Guwahati (IIT Guwahati) Academy was setup at IIT Guwahati under the scheme of "Financial Assistance for setting up Electronics and ICT Academies" as an initiative by Ministry of Electronics & Information Technology (MeitY), On 26 March, 2015 the project started at IIT Guwahati and the Academy was inaugurated by Prime Minister Shri. Narendra Modi on 19 January, 2016. The objective of the Academy was aimed to provide specialized training to the faculties of the Engineering colleges in the emerging areas of Electronics & ICT; and training large number of faculties from Arts, Commerce & Science colleges, Polytechnics, etc in the areas of utilisation of IT tools and techniques for application in their respective domain of knowledge / learning / teaching /enhancing productivity, etc by developing state-of-the-art facilities. In the past 7 years the Academy has successfully conducted 400+ Programme through conventional classroom teaching and NKN/virtual classroom mode in different Institute / University of North Eastern States in particular and few in other states of India. Till date the Academy has successfully trained 20000+ participants. The Academy has also signed MoU with Institutes/Universities for hosting the programmes and for conducting hands-on session the Academy collaborated with Industries as Training/Industry Partners. As part of their mandate for self-sustainability, the Academy is also offering online Advance Certification Course in the area of Data Science, Artificial Intelligence & Machine Learning, Big Data, Cloud Computing, Full Stack, UI/UX and VLSI Design and trained 2000+ graduates and working professionals. The Academy has also delivered training to 140+ Assam Police and Indian Navy official on cybercrime concepts and Data Science.



# About IIT Guwahati

Indian Institute of Technology Guwahati, the sixth member of the IIT fraternity, was established in 1994. The academic programme of IIT Guwahati commenced in 1995. At present the Institute has eleven departments, seven interdisciplinary academic centres and five schools covering all the major engineering, science, healthcare, management and humanities disciplines, offering B.Tech., B.Des., M.A., M.Des., M.Tech., M.Sc., MBA and Ph.D. programmes. Within a short period of time, IIT Guwahati has been able to build up world class infrastructure for carrying out advanced research and has been equipped with state-of-the-art scientific and engineering instruments. Besides its laurels in teaching and research, IIT Guwahati has been able to fulfil the aspirations of people of the North East region to a great extent since its inception in 1994. Indian Institute of Technology Guwahati's campus is on a sprawling 285 hectares plot of land on the north bank of the river Brahmaputra around 20 kms from the heart of the city. With the majestic Brahmaputra on one side, and with hills and vast open spaces on others, the campus provides an ideal setting for learning. IIT Guwahati is the only academic institution in India that occupied a place among the top 100 world universities – under 50 years of age – ranked by the London-based Times Higher Education (THE) in the year 2014 and continues to maintain its superior position even today in various International Rankings. IIT Guwahati gained rank 32 globally in the 'Research Citations per Faculty' category and overall 364 rank in the QS World University Rankings 2024 released recently. IIT Guwahati has retained the 7th position among the best engineering institutions of the country in the 'India Rankings 2023' declared by the National Institutional Ranking Framework (NIRF) of the Union Ministry of Education. IIT Guwahati has been also ranked 2nd in the 'Swachhata Ranking' conducted by the Govt. of India. IIT Guwahati has been ranked as the top- ranked University in 2019 for IT developers by HackerRank in the Asia-Pacific region.

Also, IIT Guwahati ranks 6th globally in Sustainable Development Goal 7 (Affordable and clean energy) of the Times Higher Education Impact Rankings 2023. The strategic commitment of IIT Guwahati provides the road map for the journey towards excellence.

These strategies include the Vision, Mission, Goal and Values that would be instrumental in placing IIT Guwahati among the top academic institutions of the world. The strategies will create new opportunities for the faculty and the students for enhancement of knowledge, performing cutting edge research and development of professional skills.

The ultimate aim is to provide the students with an educational training that emphasizes innovation, social awareness, professional ethics and nurture leadership skills. A resourceful environment to promote creativity and entrepreneurship amongst researchers is also being developed while maintaining sustainable goals and upholding the values of highest professional ethics and enrich the lives of humanity.



# Key Features of the Program



Course duration is 12 months with 4 semesters of 3 months each



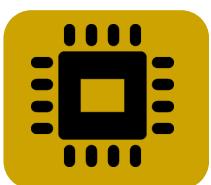
Each Semester will have a Fee Structure of Rs. 30,000/- each



Classes will be delivered in Online Mode by experienced faculty/staff/scholars



Academic masterclasses delivered by insightful IIT Guwahati and Rrookee faculties



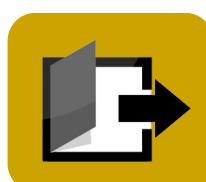
Exposure to Industrial Tools and Software during the Practical Sessions



Exclusive “Ask-me-Anything” live sessions through the online platform



Job and Research Writing Assistance from IIT Guwahati experts



Easy exit criteria from the course after each Semester



Offline orientation and Campus Immersion at the IIT Guwahati Campus



Module/Course Completion Certificates by E&ICT Academy IIT Guwahati

# Eligibility Criteria

For admission to this VLSI and Semiconductor Industry Essentials program, candidates:

- Should have a bachelor's degree with an average of 50% or higher marks
- Having some prior work experience is desired but not mandatory
- With prior coding experience is not required

## How to Enroll

- Visit our website: <https://eict.iitg.ac.in>
- Download the detailed prospectus.
- Attend a free information session (optional).
- Complete the online application.

## Application Process

The Application process consist of the following steps:



### Application Submission



Complete the application including your current resume and all the necessary documents

### Application Review & Test



Your application will be reviewed and all the documents will be verified by the admission panel members & online MCQ test will be conducted

### Admission in the Program



An offer of admission letter will be mailed to qualified candidates after the clearances of admission fee

# Target Audience

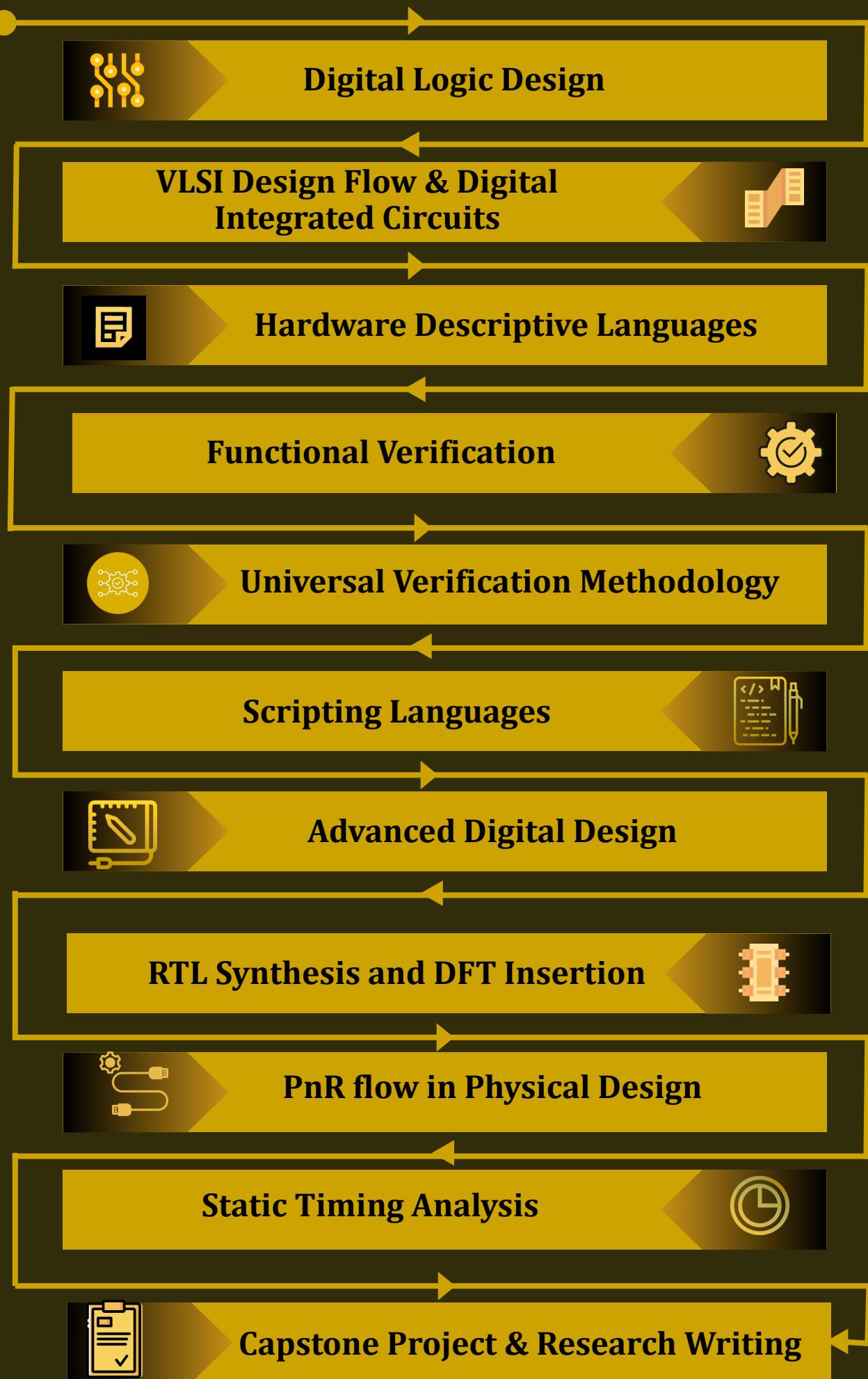
This program is designed for the following:

- **Graduate Students** – Students who have passed degrees in Electronics, Electrical Engineering, Computer Engineering, or related fields who want to specialize in VLSI.
- **Working Professionals** – Engineers in the semiconductor, hardware, or embedded systems industry who want to upskill or transition into VLSI design and verification roles.
- **Researchers and Academics** – Those engaged in advanced studies, research, or teaching in microelectronics, digital design, or integrated circuits.
- **Aspiring Semiconductor Entrepreneurs** – Individuals aiming to work in or start ventures in chip design, fabrication, or EDA (Electronic Design Automation) tools.
- **Tech Enthusiasts** – Learners with a strong interest in understanding how chips and circuits work, particularly those interested in digital logic, processor design, or SoC (System-on-Chip) architectures.

# Program Outcomes

- ▶ Strong Technical Foundation – Apply knowledge of semiconductor physics, digital/analog design, and CMOS technology in VLSI systems.
- ▶ Design & Implementation Skills – Design, model, and implement digital/analog circuits using standard VLSI methodologies and industry EDA tools.
- ▶ Verification & Problem-Solving – Analyze, simulate, and verify complex circuits to ensure functionality, timing, power efficiency, and manufacturability.
- ▶ Industry Readiness & Professional Skills – Demonstrate teamwork, technical communication, and adherence to semiconductor industry practices and standards.
- ▶ Ethics & Lifelong Learning – Recognize professional responsibilities and pursue continuous learning in emerging VLSI technologies, low-power design, and sustainable chip solutions.

# Learning Path Visualization



# Semester wise Syllabus

## Semester I : Foundational Digital Design (Months 1-3)

### Module Code: 101 : Digital Logic Design

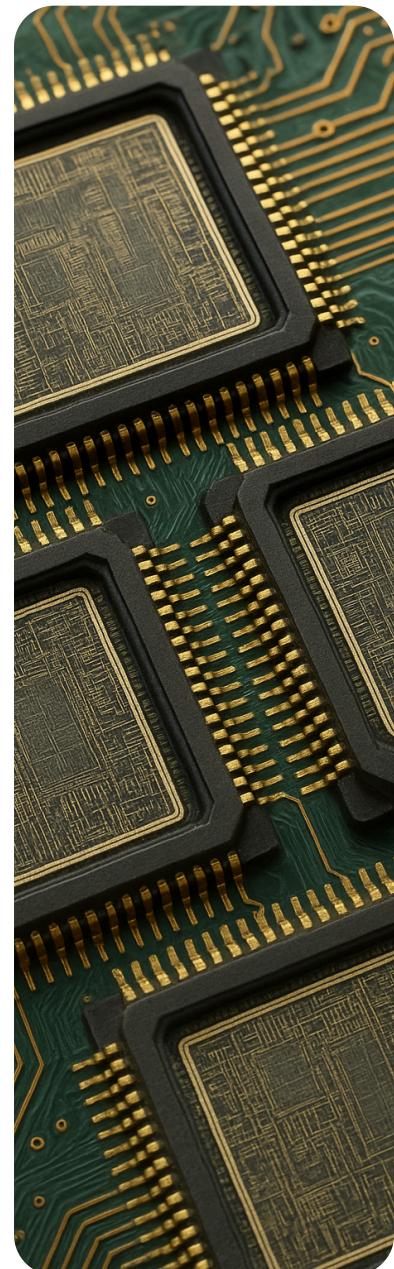
#### Learner's Goal:

- Build a strong foundation in digital logic and number systems.
- Learn how to design and analyze circuits that perform real tasks.
- Practice using tools and languages (like HDL) to bring circuits to life.
- Apply digital logic knowledge to understand computers and modern systems.

#### Learning Outcome:

- Demonstrate understanding of Boolean algebra, number systems, and basic logic operations.
- Design and analyze combinational and sequential circuits using standard techniques.
- Apply digital logic principles to model and solve practical computing problems.

Sr. No.	Topic	Hours
1	Logic Gates (AND, OR, NOT etc.)	1
2	Boolean Algebra	1
3	Gate level combinational circuits: Multiplexer/Demultiplexer	1
4	Encoder/ Decoder	1
5	Adder/ Subtractor	1
6	Comparator	1
7	Parity generators	1
8	Gate level sequential circuits: latches	1
9	Flip-flops (RS, JK, D, T, and Master Slave)	2
10	Registers	1
11	Counters: Ripple and Ring	1
12	Shift Register and Counters	1
13	Design of synchronous sequential finite state machine	3
14	Analysis of synchronous sequential finite state machine	



**Practical Hours = 14 Hours**

**\*\*Note: Digital Electronics Lab can be conducted using Virtual Labs platform in online mode**

**Module Code: 102**

# VLSI Design Flow and Digital Integrated Circuits

## Learner's Goal:

- To learn the device physics of MOS transistor, structure, operation, characteristics, and model.
- To study analog CMOS sub circuits and amplifiers
- To learn various design styles for combinational and sequential logic circuits

## Learning Outcome:

- Understand the models of MOS transistors and its use in circuit simulations.
- Design different CMOS logic circuits covering static and dynamic CMOS designs.
- Design and analyze various CMOS combinational circuits in CAD tools.



Sr. No.	Topic	Hours
1	Key stages in design	1
2	Key stages in Verification	1
3	Synthesis	1
4	Physical Design	2
5	<b>MOS Circuits:</b> MOS transistor operation in linear and saturated regions, MOS transistor threshold voltage, MOS switch and inverter, Latch-up in CMOS inverter	4
6	Sheet resistance and area capacitances of layers	
7	Wiring capacitances	1
8	CMOS inverter	
9	CMOS Gates	
10	Delays	0.5
11	Logical Effort, Electrical Effort, Gate sizing, Buffering	2
15	Asymmetric gate	1
16	Skewed gates	0.5
17	Ratioed logic	1
18	Switching power dissipation	1
19	Stick Diagram	1
20	<b>MOSFET scaling:</b> Constant-Voltage, Constant-field scaling	2
21	<b>Dynamic CMOS design:</b> Steady-state behavior of dynamic gate circuits, Noise considerations in dynamic design, Charge sharing, Cascading dynamic gates, Domino logic, np-CMOS logic, Problems in single-phase clocking, Two-phase non-overlapping clocking scheme	2

**Practical Hours: 09 hours**

**Practical Tools required : MAGIC and SPICE**

# Module Code: 103 :

## Hardware Descriptive Languages (HDLs)

### Learner's Goal:

- To learn the fundamentals of CMOS based sequential circuits.
- To understand the timing constraints of CMOS based digital circuits.
- To learn the realization of finite state machines.

### Learning Outcome:

- Illustrate the use of various delay models and optimize the CMOS circuit delay.
- Design and analyse various CMOS combinational and sequential circuits, data path and memory subsystems.
- Design and analysis of different arithmetic circuits covering adders, multipliers and shifters.

Sr. No.	Topic	Hours
1	Introduction to digital circuit design flow, Verilog Language introduction	1
2	Levels of abstraction, Module, Ports types and declarations, Registers and nets, Arrays	3
3	Identifiers, Parameters, Relational, Arithmetic, Logical, Bit-wise shift Operators	2.5
4	Writing expressions, Behavioral Modeling, Structural Coding, Continuous Assignments	4
5	Procedural Statements, Always, Initial Blocks, begin end, fork join, Blocking and Non-blocking statements	3.75
6	Operation Control Statements, If, case, Loops: while, for-loop, forever, repeat	2
7	Combination and sequential circuit designs, Memory modeling,, state machines, CMOS gate modeling	2.25
8	Writing Tasks and Functions	2.5
9	Compiler directives, Conditional Compilation, System Tasks	3
10	Gate level primitives, User defined primitives, Delays, Specify block, Test benches, modeling, timing checks	3
11	Assertion based verification, Code for synthesis, Advanced topics, Writing reusable code	3



**Practical Tools: Tools Required: Xilinx Vivado, Quartus Prime**

**\*\*Note: Labs will follow the theory in the same duration.**

## Semester II : Semiconductor Fabrication & Device Design (Months 4 - 6)

### Module Code: 201 : Functional Verification

#### Learner's Goal:

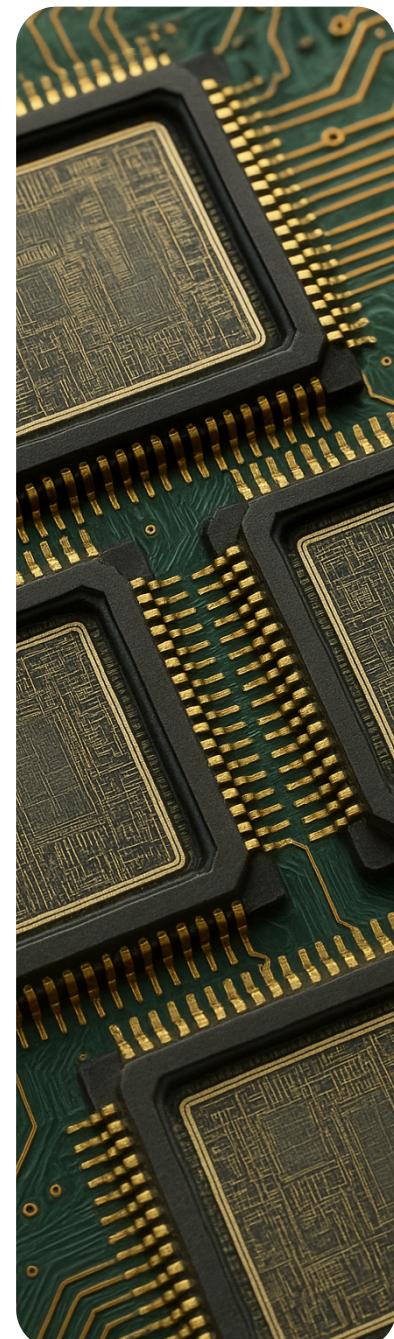
- To know digital building blocks, test benches and verify the functionality using HDL
- To Study the verification concepts using System Verilog
- To learn principles of verification using System Verilog and design test benches

#### Learning Outcome:

- Verify increasingly complex designs more efficiently and effectively
- Interpret flexible and reliable SV verification environment, whose components can be re-used across multiple projects
- Utilize randomization and OOP concepts of SV to build complex digital systems

Sr. No.	Topic	Hours
1	Functional Verification overview	
2	System Verilog Course overview	
3	Operators, Data types (Int,Void,String,Userdefined,Enumeration,class)	
4	Arrays(Fixed Size Array, packed array, unpacked array,Dynamic array ,Associate Array ,Queues)	
5	Procedural Statements and Flow Control (foreach,repeat forever,break and continue,event control,Named block)	
6	Object Oriented Programming Overview	
7	Advanced Data types	
8	Fork join, Inter process synchronization	
9	Project to learn all SV language constructs	
10	Program, Scheduling semantics, Task, Function	
11	Constraints, Randomization	
12	Functional and code coverage	
13	Assertions and Assertion based verification	
14	Direct Programming Interface(DPI)	
15	Configuration libraries, Packages, XMR	
16	Test bench Architecture	

25



Practical will follow the Theory at the same time.

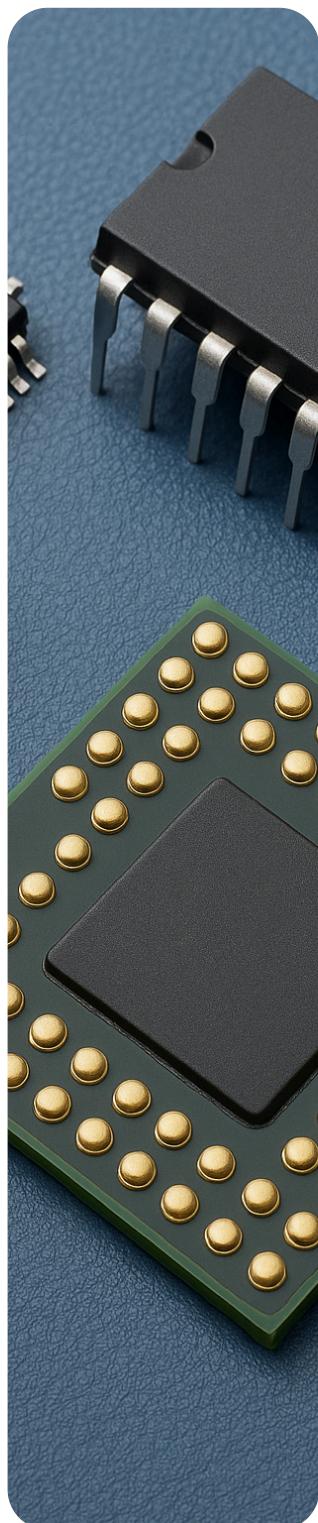
Tools Required: Questa Sim, Modelsim, NCSIM, VCS

**Module Code: 202****Universal Verification Methodology (UVM)****Learner's Goal:**

- Understand Verification Fundamentals
- Learn UVM Architecture & Components
- Develop Practical UVM Testbenches
- Apply Advanced Verification Techniques
- Gain Industry-Relevant Skills

**Learning Outcome:**

- Explain the concepts of functional verification, constrained-random testing, and coverage-driven methodology.
- Design and implement reusable UVM testbenches using System Verilog, incorporating agents, drivers, monitors, sequencers, and scoreboards.



Sr. No.	Topic	Hours
1	UVM Methodology	
2	How UVM evolved?	
3	UVM class library	
4	UVM Class Library, Macros, Utilities	
5	UVM TB Architecture	
6	Command line processor	
7	Reporting classes	
8	Objections	
9	UVM Factory	
10	Configuration DB, Resource DB	25
11	TLM1.0	
12	Simulation Phases	
13	Sequences, Sequencers	
14	Test case development	
15	Configuring TB Environment	
16	Different testbench component coding	
17	Different styles of sequence development	
18	Sequence library	
19	Virtual Sequencer, Virtual sequences	

**Practical will follow the Theory at the same time**  
**Practical Tools required : Questa Sim, Modelsim, NCSIM, VCS**

# Module Code: 203 : Scripting Languages

## Learner's Goal:

- To understand the importance of scripting languages in VLSI Design
- To describe the various TCL & Python concepts used in VLSI design for large data handling
- To understand utilization of TCL in CAD Tools Interfacing

## Learning Outcome:

- Gain fluency in programming with Linux
- Create and run scripts using Python.
- Understand the fundamentals of TCL scripting
- Develop the VLSI scripts for tool automation using TCL
- Learn the advanced programming skills of Python programming.

Sr. No.	Topic	Hours
1	Linux Commands – Hands On	2
2	Vim Editor – Hands On	2
	TCL	
3	Programming Basics	10
4	Data Manipulation	
5	File Handling	
	Python	
6	Programming Basics	11
7	Data Manipulation	
8	File Handling	
9	Basic Statistics	
10	Data Visualization	



**Practical Tools: Tools : Unix/Linux Environment + TCL and Python Utility**

**\*\*Note: Labs will follow the theory in the same duration.**



# Module Code: 204 Advanced Digital Design

## Learner's Goal:

- Gain in-depth knowledge of sequential logic, pipelining, finite state machines (FSMs), and timing optimization.
- Design, model, and verify complex digital systems using Verilog/VHDL/SystemVerilog.
- Employ CAD tools, synthesis, simulation, and FPGA prototyping for practical implementation and testing.

## Learning Outcome:

- Explain advanced digital design principles including pipelining, FSM optimization, and timing analysis.
- Design and implement complex digital systems using Verilog/VHDL/SystemVerilog and industry-standard EDA tools.
- Analyze and optimize digital circuits for performance, power, and area trade-offs.

Sr. No.	Topic	Hours
1	Clock Domain Crossing (CDC): Fundamentals and Metastability issues	
2	Types of CDC signals: Single-bit control and Multi-bit data signals, Handshake-based transfers	5
3	CDC design techniques: 2-flop synchronizer, Pulse synchronizer, Handshake and FIFO-based synchronizer, Timing constraints and STA considerations for CDC	
4	CDC verification techniques: Simulation limitations, Formal verification methods, Static CDC tools	5
5	Reset Domain Crossing (RDC): Fundamentals, Asynchronous vs synchronous resets, Metastability due to reset deassertion	
6	Reset release synchronization methods, Safe reset design practices, Reset tree design in large SoCs, RDC verification and sign-off checks	5
7	Synchronizers: Basics of metastability, Synchronizer design principles	
8	Common synchronizer architectures: 2-flop synchronizer, Multi-flop synchronizer, Muller C-element synchronizer, Gray code synchronizer	5
9	MTBF (Mean Time Between Failure) calculation, Impact of technology scaling on synchronizers,	
10	Best practices for synchronizer placement and physical design	
11	Case studies in synchronizer failures	



**Practical Tools: Tools Required: QuestaSim, VCS, or Xcelium**

**\*\*Note: Labs will follow the theory in the same duration.**

## Semester III : Hands-on Tool for VLSI (Months 7-9)

### Module Code: 301 : RTL Synthesis and DFT Insertion

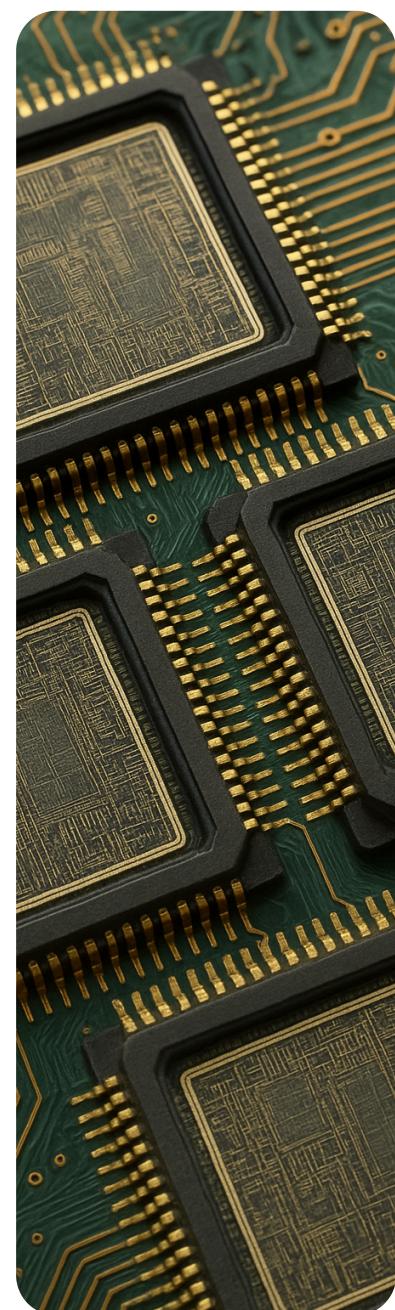
#### Learner's Goal:

- Get familiarized with various files related to RTL Synthesis flow and their contents.
- Differentiate the logical and physical synthesis.
- To know optimization techniques used by tools

#### Learning Outcome:

- Set up the tools flow to carry out the RTL synthesis.
- Debug the errors in flow and correct it.
- Generate synthesized netlist without any errors in design as well as timing.
- Apply the testing concepts to achieve better yield in IC design

Sr. No.	Topic	Hours
1	Introduction, Logical Vs Physical, Timing Models, Inputs required in Details	3
2	Steps in Synthesis: Analyse/Elaborate, Importing Constraints, Importing DEF & UPF, Compile	1
3	Optimization, Scan (DFT) Insertion, Compile incremental, Debugging/Resolving the Errors	1.5
4	Important Commands, Qualifying netlist, Generating outputs	1.5
5	Logical Equivalence Check: Introduction, Need for LEC, Modes, Debuging & Resolving the mismatches in netlists	2
6	Need for testing, DFT Basics, SoC Scan architecture overview, Types of Scan	3
7	ATPG DRC Debug, ATPG Simulation Mismatch Debug, DFT Diagnosis, JTAG	5
8	MemoryBIST, LogicBIST, Scan and ATPG	3.5
9	Test compression techniques, Hierarchical Scan Design	2
10	DFT Compiler: Overview, Flows Supported by DFT Compiler, Scan Insertion Flow, DFT Compiler Flow and supported Commands, Tetramax/Tessent Flow for ATPG, Steps involved in ATPG mode, ATPG models targeted by Tetramax/Tessent	7.5



Practical will follow the Theory at the same time.

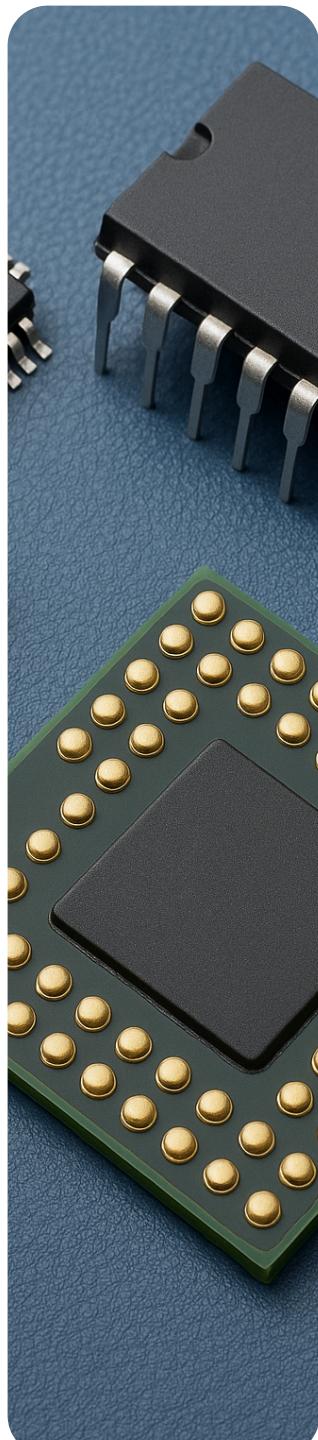
Tools Required: Synopsys DC, FC, FV or Cadence Genus, CLP or YoSys, Tetramax/ Tesson

**Module Code: 302****PnR flow in Physical Design****Learner's Goal:**

- To know VLSI physical design automation
- Get familiarized with various files related to PD flow and their contents.
- To learn concepts related to floor planning, partitioning, placement, CTS & routing.
- Get familiarized with various CAD tools including OpenRoad tool.
- Run whole physical design flow with provided technology files & RTLs to generate the GDS-II at the end of flow.

**Learning Outcome:**

- Identify the input files provided to him.
- Run the whole PnR flow starting with floorplanning to generate the GDS-II file.
- Identify use of Important commands related to tools that learner is using.



Sr. No.	Topic	Hours
1	Floor planning: Inputs of Floorplan, Sanity Checks, Macro Placement Guidelines, Qualifying the Floorplan, Power Planning	10
2	Placement: Standard cell placement, Global routing, Congestion analysis, Timing analysis, Qualifying the placement db	10
3	Clock Tree Synthesis: Specification file, NDR rules, Clock tree build and Balance, CCD Concurrent Clock and Data Optimization, Clock tree optimization, Crosstalk, Timing Analysis	10
4	Routing and Optimization: Overview & goals, Constraints, Pre-route checks, Related terminologies, Types of routing and Optimization, Challenges in routing (DRC/LVS), Timing Analysis, ECO (Engineering Change Order), GDS-II Generation	10

**Practical will follow the Theory at the same time.**  
**Practical Tools required : Synopsys ICC, FC Or Cadence Innovus or OpenRoad Tools**



# Module Code: 303 :

## Static Timing Analysis (STA)

### Learner's Goal:

- To get familiar with terms used in STA flow.
- To learn about various constraints in SDC file.
- To learn the usage of commands related to constraints.
- To know the advance STA topics

### Learning Outcome:

- Know the meaning & usage of each term used in STA flow
- Build the SDC file which includes various constraints.
- Identify and resolve the errors related to constraints file.

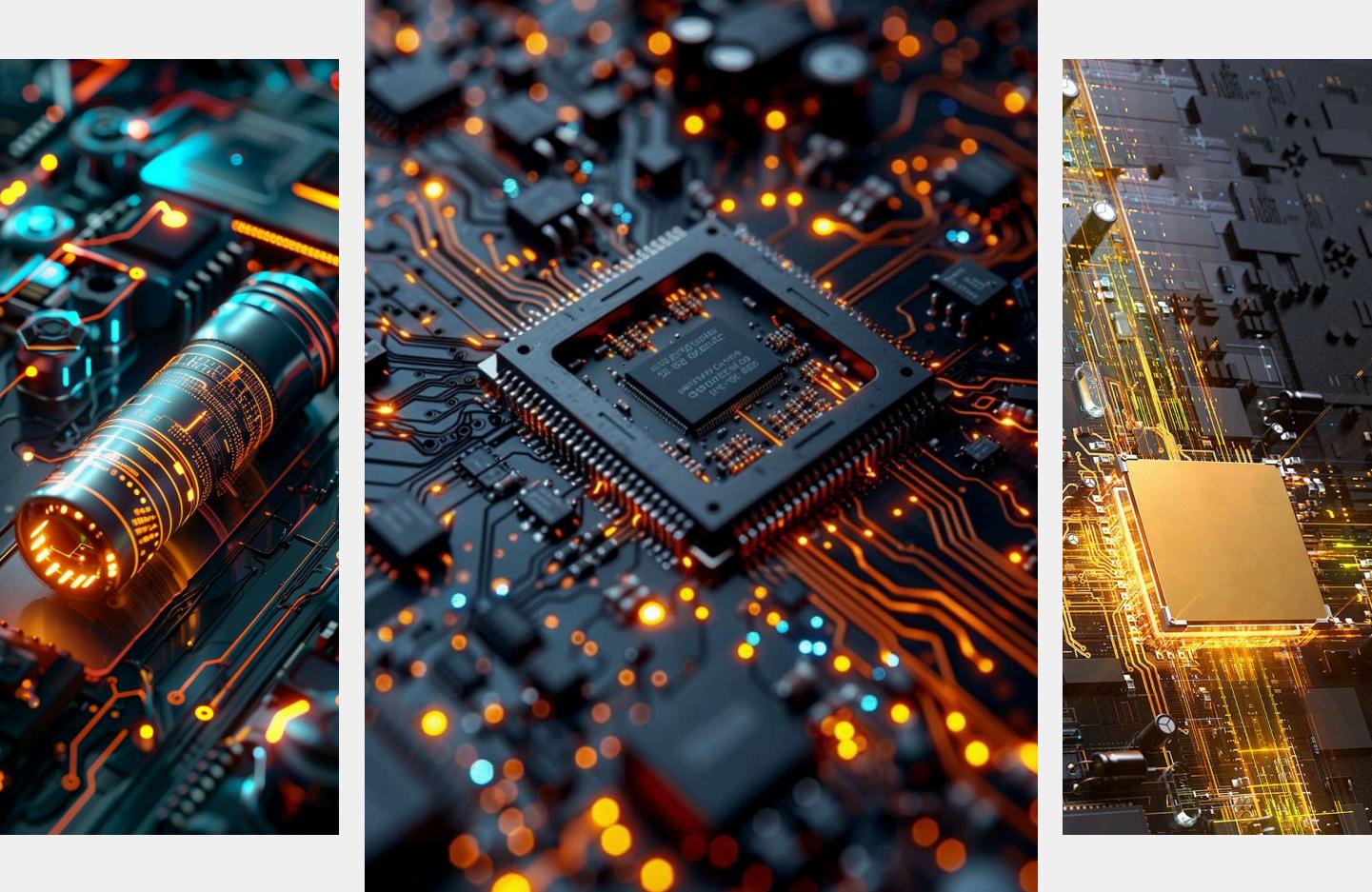
Sr. No.	Topic	Hours
1	Basic Static Timing Analysis Concept, Input to STA tool	1.5
2	Setup Time, Hold Time, Slack, Clock Latencies + Clock Skew	1.5
3	Library Overview, Recovery and Removal Time, Propagation Delay Calculations	4.5
4	Timing Paths, Timing Exception, Asynchronous Path, Clock Gating, STA VS DTA	3
5	Generated Clock, Virtual Clock, Untenses + Functionality, Uncertainty, Jitter	1.5
6	Design Constraints in details: Timing Constraints, Design Rule Constraints, Exceptions, Area Constraints, System Interface constraints, Multi-voltage and power optimization Constraints	6
7	Advance STA Concept: Onchip Variation (OCV), Advance Onchip variation (AOCV), Parametric On chip variation (POCV), Signal Integrity Effects	2



### Semester IV : VLSI and Semiconductor for Industry Essentials (Months 10-12)

Sr. No.	Topic	Hours
1	Module Code: 401: Capstone Project	30
2	Module Code: 402: Final Project Presentation	5
3	Module Code: 403: Research Methodology & Research Writing	35
4	Module Code: 404: Career Counselling	10
5	Module Code: 405: Interview Facing Tips & Tricks	10

# Unlock Exciting Career Paths



Graduates of this program will be equipped for a wide array of roles in the burgeoning VLSI Design landscape, including:

- Physical Design Engineer
- Analog Layout Engineer
- Digital Layout Engineer
- VLSI Application Engineer
- Front-End Design Roles
- Back-End Design Roles
- Mixed Signal Roles
- Validation and Testing Roles
- EDA and CAD Roles
- Architecture and R&D roles

# Sample Certificates

A Certificate of Completion will be provided after successful completion of every Semester and a Course Completion Certificate will be provided after completion of all the four Semesters. This is a globally recognized certificate which can create an immediate impressive career impact.



**Module completion certificate after completion of Semester I on "Foundational Digital Design"**

**Module completion certificate after completion of Semester II on "Semiconductor Fabrication & Device Design"**



**Module completion certificate after completion of Semester III on "Hands-on Tools for VLSI"**



**Module completion certificate after completion of Semester IV on "VLSI and Semiconductor Industry Essentials"**

# Course Designed by



**Prof. Gaurav Trivedi**  
**Professor and Principal  
Investigator, E&ICT Academy  
IIT Guwahati**

**Research Interest:**

Circuit Simulation (Analog, RF & Digital) and VLSI CAD, Electronics System Design, Computer Architecture, Semiconductor Devices, Hardware Security, Embedded Systems and IoT, High Performance Computing, Large Scale Optimization and Machine Learning



**Prof. Anand Bulusu**  
**Professor,  
Department of ECE  
IIT Roorkee**

**Research Interest:**

CMOS digital circuit design methodologies, VLSI device physics, device-circuit interaction, Mixed-signal design methodologies



# Contact Us

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