Analyzing the dynamic accuracy of simultaneous sample-and-hold circuits is straightforward. A wideband scope and a simple mathematical model supply the answers.

In most simultaneous data-acquisition systems a large number of analog input channels are strobed at precise time intervals and then sequentially digitized by an analog-to-digital converter. To check the multichannel sample-and-hold circuits there are some simple tests the user can perform to verify correct circuit operation.

To start the error analysis, several assumptions can safely be made: All static errors have been eliminated—

- The offset error.
- The gain error.
- The hold step error.

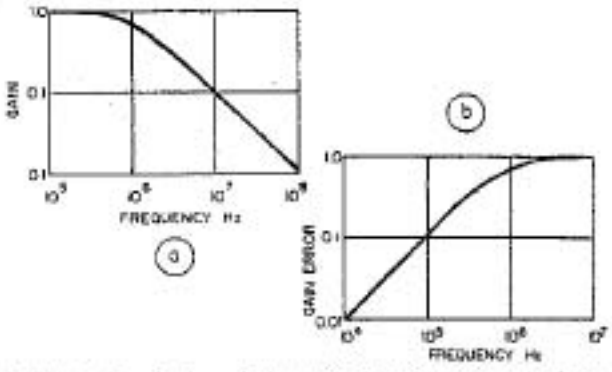
Input voltage, V_{in}, to the sample-and-hold equals the output voltage, V_{out}, from the sample-and-hold. V_{in} is any dc voltage between ±10 V. The offset error is V_{out} when $V_{in} = 0$, while the gain error is the maximum value of the offset error divided by V_{in} maximum (10 V).

Looking at the dynamic errors

Normally, one sample-and-hold circuit is used for each a/d converter with any multiplexing between input channels done previously. However, for a large number of channels this leads to errors due to the different conversion times of the various channels. In a simultaneous sample-and-hold configuration, a number of input analog channels are strobed at a precise time and the held voltages are sequentially converted to digital form.

At this point the most basic test that can be performed is to simultaneously apply the same voltage waveform to all inputs. Now, if we look at the output for each channel, the digital words representing each voltage should be identical. If the system fails this basic test, the user must search the specification sheets and the circuits themselves for the error sources.

The three major sources of dynamic errors can be traced to the following:



1. **Plots of a single pole transfer function** (a) and of the gain-error (b) are shown with a 1-MHz cutoff frequency.

- A change in the gain during the sample mode as a function of frequency.
- A nonzero hold step as a function of frequency (hold-step error).
- A shift in the effective beginning of the hold-step as a function of V_{out}, dV_{out}/dt, or frequency (aperture-shift error).

The aperture-shift error can be caused by a slowly opening switch or by a pole at the unity-gain −3 dB point (f_{co}) of the unity-gain sample amplifier. The error advances the effective time of the switch opening to a time prior to its actually reaching open circuit. For applications of simultaneous sample-and-hold circuits both the f_{co}'s and the switch opening times, must be matched.

The transfer function during sample

Gain in the sample stage can be represented by a linear transfer function—at least for amplitudes small enough that the amplifier slew-rate doesn't affect the results. Thus, a simple low-pass function with a pole at f_{co}, say 1 MHz, can be represented by the following:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + j\frac{f}{10^6}}$$

The graph of this typical low-pass filter is shown in Fig. 1a. It has unity-gain transmission and a

1-MHz −3 dB point.

Usually, though, it proves more useful to plot small deviations from unity gain as shown in Fig. 1b. The formula used for this gain-error plot is

$$\text{Gain error} = \frac{V_{out}}{V_{in}} - 1 = \frac{-j\frac{f}{10^6}}{1 + j\frac{f}{10^6}}$$

While not usually seen in this form, this type of frequency-response plot is quite valid. From the equation we see, for example, that a circuit bandwidth of 1 MHz, an input of 10 V at a frequency of 1 kHz results in an error of 0.001 or 10 mV.

By now finding the response of the circuit to a ramp of K V/sec, we can try to match transfer functions of all the channels of the sample-and-hold stages. The gain-error transfer function is put into the s domain using LaPlace transforms and becomes

$$\text{Gain error} = \frac{-s}{2\pi \times 10^6} \Big/ 1 + \frac{s}{2\pi \times 10^6}$$

The ramp is also transformed, and becomes K/s^2.

The sample-and-hold: What is it and where is it used?

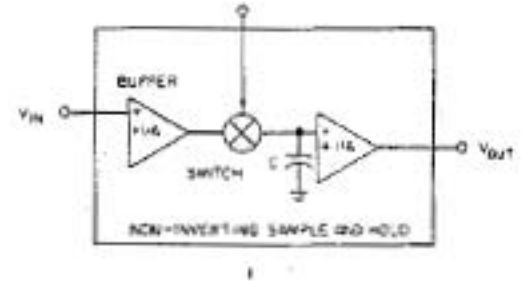
A sample-and-hold (S/H) circuit holds or "freezes" a changing analog input signal voltage. Usually, the voltage thus frozen is then converted into another form, either by a voltage-controlled oscillator, an analog-to-digital (a/d) converter or some other device.

The simplified block diagram of a lossless (ideal) S/H circuit is shown in Fig. 1. Here the amplifiers are assumed to be ideal—with infinite input impedances and bandwidths, zero output impedances and unity gains. The electronic switch is also considered ideal—with infinite speed, zero impedance in the sample position and infinite impedance in the hold position. Also, the sampling capacitor, C, is assumed to have no leakage or dielectric absorption.

Depending upon cost, the user has three basic methods to choose from when setting up a multiple-signal data-acquisition system. The most basic but also the most expensive scheme is the one shown in Fig. 2a. This circuit uses an individual S/H and a/d converter for each sensor line. Fig. 2b is a low cost alternative in which all the sensor lines are first multiplexed and then fed into a single S/H and a/d converter. Another method, falling between those of Figs. 2a and 2b in cost and performance, is shown in Fig. 2c. Here, the sensor signals are first sampled and then multiplexed and sent to a single a/d converter.

If the S/H circuits were ideal, the only significant errors would occur in the multiplexer or the a/d converters. In a real world situation, of course, the S/H circuits introduce some serious errors into the conversion circuit.

The circuits of Figs. 2a and 2c require additional qualities from the S/H circuits that are not needed for the system of Fig. 2b. Precise matching of the aperture delays and bandwidths is required.



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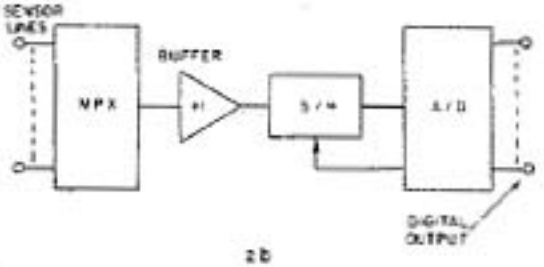
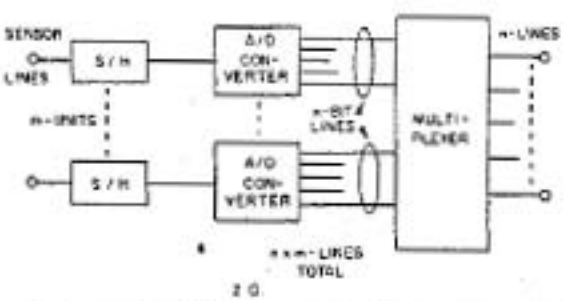
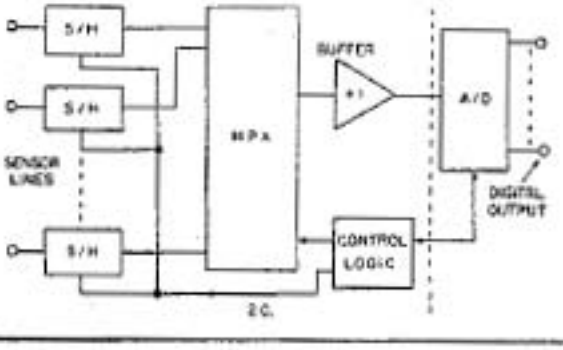


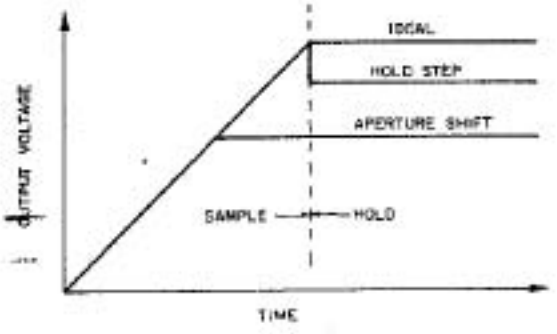
2b



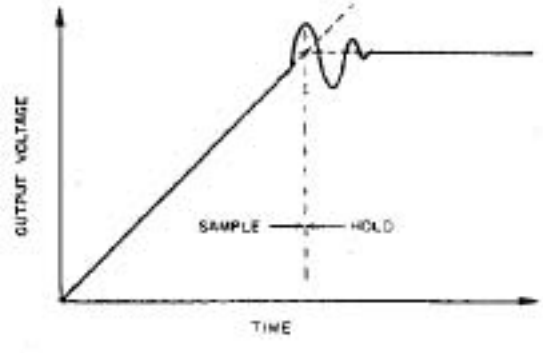
2a



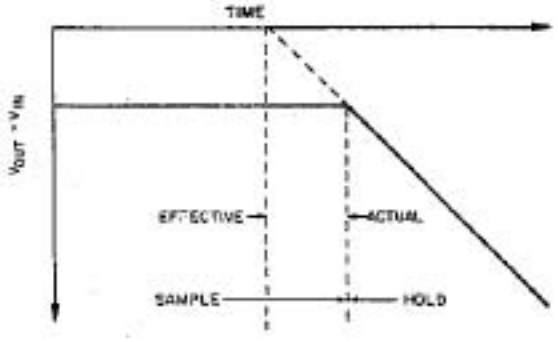
2c



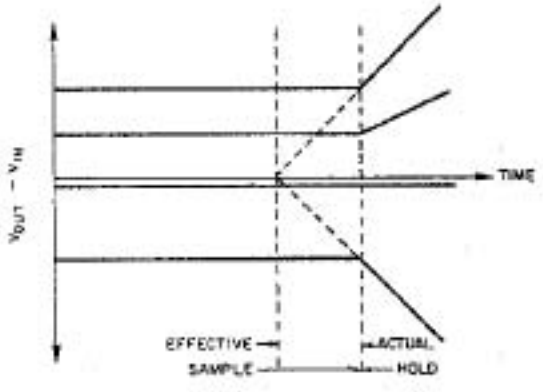
2. **Dynamic errors caused by the hold step** and the aperture shift are hard to distinguish.



3. **By extrapolating** the two straight-line segments to meet each other, you can find the effective time at which the hold period starts.



4. **If you use a different scope input,** the effective point of hold initiation can be found by extrapolating back to the zero point.



5. **The effective start time** for hold is not affected by the slope of the input ramp—for a first-order analysis.

Taking the inverse transform of the product we get

$$\frac{K}{2\pi \times 10^6}[1 + e^{-(2\pi \times 10^6)t}]$$

as the output error for a ramp input.

The two terms in the result represent a gain error. This error is due to the ramp as a constant $K/2\pi f_{-3}$ and a delay of $1/2\pi f_{-3}$ seconds. The delay in the output can be considered as an advance in the transition time of sample-to-hold states—but this is not usually done. The inverse transfer function can always be applied after the data has been digitized. However, for multichannel simultaneous sample-and-hold applications it is unnecessarily complicated to keep track of, say, 32 different transfer functions. The solution to this problem is to match all the transfer functions so that the units will deliver identical outputs for the same input waveform.

Other error sources exist

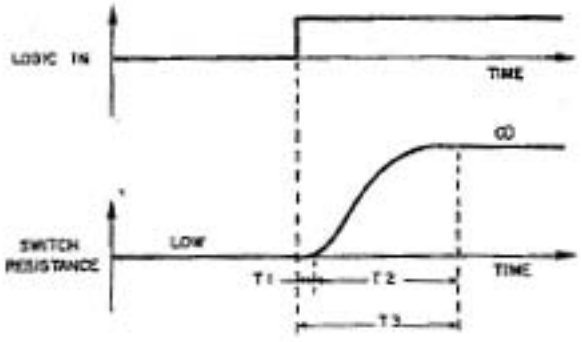
Examination of the output voltage near the time of the sample-to-hold transition shows the errors caused by both a hold step and an aperture shift (Fig. 2).

The hold-step error appears as a sudden change in the sample capacitor voltage at the time of hold. If such an error exists only for a fast ramp input, a probable cause is dielectric absorption in the capacitor.

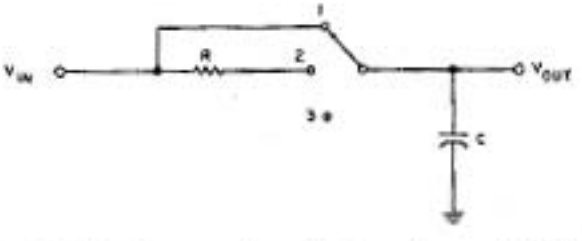
The aperture shift is a variation, in either direction, of the point in time at which hold occurs. It is also known as aperture uncertainty. As a function of input rate it is somewhat difficult to measure.

To measure aperture uncertainty, use an oscilloscope with a sampling amplifier or with a sensitive, wideband input having good recovery. Then observe the sample-and-hold output for an input slope of 0.5 or 1 V/μs. The resulting straight lines can then be extrapolated to a point where they meet, and the effective hold instant can be found, as shown in Fig. 3. A change of this point with the input waveform, or randomly, is called aperture jitter.

A similar type of measurement uses a scope's differential input. All static and dynamic errors, including linear ones, due to the transfer function can be measured by observing $V_{out} - V_{in}$ as shown in Fig. 4. The slope during the hold period can be extrapolated back to zero to find the effec-



6. **A typical analog switch** introduces a delay in the sample-to-hold transition.

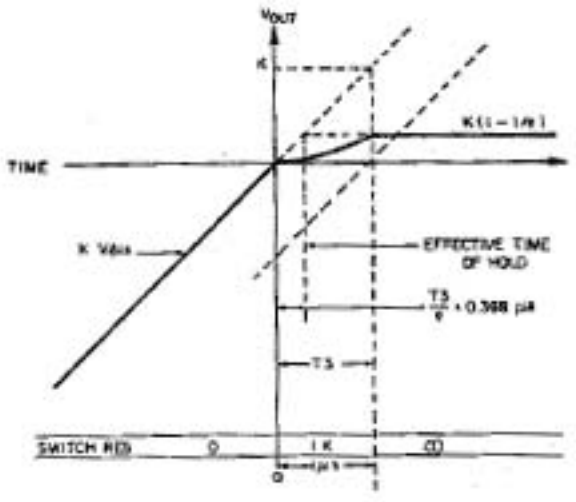


7. **An ideal slow opening switch** can be modeled by using a simple RC network and a three position switch.

tive time when hold starts. With a single-pole transfer function, the value of $V_{out} - V_{in}$ during sample for an input ramp is proportional to the slope of the waveform. But as shown in Fig. 5, to a first-order approximation, the start of hold is unaffected.

But, there is zero aperture uncertainty with the transfer function representation, thus the effective time of hold initiation occurs before the switch opens! The amount of this shift can be determined as a function of bandwidth. A transfer function with an f_{co} of 1 MHz can be represented by an RC low-pass filter with a resistor of 159 Ω and a capacitor of 100 pF. An input ramp of 1 V/s will cause a capacitor current of 1 mA (CV/t) which in turn causes a resistor drop of 159 mV. Thus the effective time of hold occurs 159 mV/V/μs or 159 ns before the actual switch opening.

The two measurements described are difficult to perform without high performance test equipment. Therefore, most manufacturers' specifications of aperture delay and uncertainty tend to be primarily concerned with the variation of switch resistance after the logic input changes to the hold state. Fig. 6 shows a typical logic switch resistance change during the sample-to-hold transition.



8. **The effective time** at which hold commences occurs before the switch is fully opened.

The time T_1 is known as the switching delay or aperture delay and is characteristic of any practical switch. Switching time, T_2, usually is measured from the 10 to 90% points (as for logic circuits) and is sometimes called aperture time. The total switching time, T_3, is also referred to as either the aperture time or aperture delay. If the rise time of the switch varies with the input voltage waveform, or just randomly, the change in T_1 is called the aperture jitter.

To further complicate matters, some definitions do not use switch resistance. Diode-bridge switches are characterized by stored charge and not by changes in resistance. The switch must then be viewed as a black box—apply a ramp voltage to it, open the switch and determine the effective time of opening by observing V_{out} and extrapolating the straight lines as previously described. A second method relying on diode reverse-recovery measurements can be used but is not as accurate.

The example shown in Fig. 7 can demonstrate that the effective switch opening time occurs before the switch resistance reaches infinity. Let V_{in} be a ramp of K V/μs. If, at time t = 0, the switch goes from position 1 to 2, then 1 μs later it goes to position 3, the effective time of hold can be seen from Fig. 8 to occur while the switch is in position 2. The aperture-time advance is fixed for an input ramp but will have jitter for waveforms that have curvature. The effective hold initiation will occur between instants T_1 and T_3. This is why $T_3 - T_1 = T_2$ is often specified as the aperture time. ■■