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INNOVATOR IN ELECTRONICS

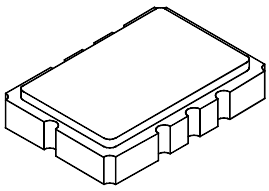
Discontinued

RFM products are now Murata products.

OP4018B1

718.864 MHz Optical Timing Clock

- ***Fundamental-Mode Oscillation at 718.864 MHz***
- ***Quartz SAW Stabilized and Filtered "Diff Sine" Technology***
- ***Voltage Tunable for Phase Lock Loop Operations***
- ***Optical Timing Reference for Forward Error Correction Applications***
- ***Complies with Directive 2002/95/EC (RoHS)***



SMC-8A

The output of this device is generated and filtered by narrow band quartz SAW elements at 718.864 MHz. The configuration of this clock is intended to provide a pure signal for optical timing applications in noisy signal environments. The Q/Qbar differential output swing of ±1 volt about 0 Vdc has symmetry better than ±1% into loads from 40 to 70 ohms; determined by customer application. The long term frequency accuracy is set by an external reference source allowing this device to complete a Phase Lock Loop design without the usual noise and jitter problems associated with PLL's.

Absolute Maximum Ratings

Rating	Value	Units
DC Suppy Voltage	0 to 5.5	Vdc
Tuning Voltage	0 to 5.5	Vdc
Case Temperature	-55 to 100	°C

Electrical Characteristics

Characteristic		Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency	Absolute Frequency	f_O	1, 9		718.863785		MHz
	Tuning Frequency Range		2	±50			ppm
	Tuning Voltage Range		1	1.8	2.4	3	V
	Tuning Linearity		1, 8		±3	±5	%
	Modulation Bandwidth			100			kHz
	Tuning Input DC Resistance			100			KΩ
	Tuning Slope			150	250	350	ppm/volt
Q and $\overline{Q}$ Output	Voltage into 50 Ω (VSWR<1.2)	V_O	1,3	0.6		1.1	V_{P-P}
	Operating Load VSWR		1,3			2:1	
	Symmetry		3, 4, 5	49		51	%
	Harmonic Spurious		3, 4, 6			-15	dBc
	Nonharmonic Spurious		3, 4, 6, 7			-65	dBc
Phase Noise	@100 Hz offset				-70	-65	dBc/Hz
	@1 kHz offset				-100	-95	dBc/Hz
	@10 kHz offset				-125	-120	dBc/Hz
	@100 kHz offset				-140	-135	dBc/Hz
	Noise Floor				-150		dBc/Hz
Jitter	RMS Jitter (10 kHz to 80 MHz)		3, 4, 6, 7			0.5	ps_{P-P}
	200 mV_{P-P} from 1 MHz to ½ f_O on		3			-50	dBc
Output DC Resistance (between Q & $\overline{Q}$)			1, 3	50			KΩ
DC Power Supply	Operating Voltage	V_{CC}	1, 3	3.135	3.300	3.465	Vdc
	Operating Current	I_{CC}	1, 3			70	mA
Operating Ambient Temperature		T_C	1, 3	0		+85	°C
Lid Symbolization (YY=Year, WW=Week)		RFM OP4018B1 YYWW					

CAUTION: Electrostatic Sensitive Device. Observe precautions for handling.
COCOM CAUTION: Approval by the U.S. Department of Commerce is required prior for export of this device.

NOTES:

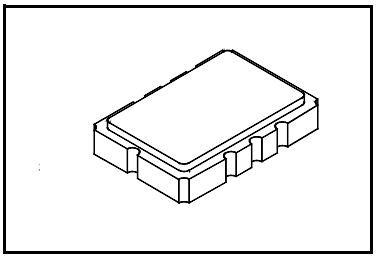
1. Unless otherwise noted, all specifications include any combination of load VSWR, VCC, and TC. In addition, Q and $\overline{Q}$ are terminated into 50 Ω loads to ground.
2. Customer useful tune range in excess of what part requires over temp, aging, pushing, pulling & accuracy.
3. The design, manufacturing process, and specifications of this device are subject to change without notice.
4. Only under the nominal conditions of 50 Ω load impedance with VSWR ≤ 1.2 and nominal power supply voltage.
5. Symmetry is defined as the pulse width (in percent of total period) measured at the 50% points of Q or $\overline{Q}$. (See: Timing Definitions.)
6. Jitter and other spurious outputs induced by externally generated electrical noise on V_{CC} or mechanical vibration are not included in this specification, except where noted. External voltage regulation and careful PCB layout are recommended for optimum performance.
7. Applies to period jitter of Q and $\overline{Q}$. Measurements are made with the Tektronix CSA803 signal analyzer with at least 1000 samples.
8. Linearity is a function of the percentage variation from a permitted linear deviation versus the amount of frequency tune range. *See Linearity Definition.*
9. One or more of the following United States patents apply: 4,616,197; 4,670,681; 4,760,352.

Discontinued

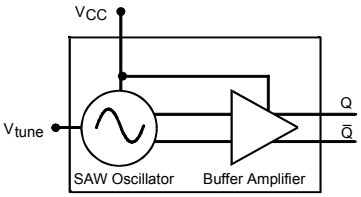
OP Performance Curves and Applicati

See the OP4005B Data Sheet for typical OP performance curves and application information.

SMC-8A 8-Terminal Surface Mount Case

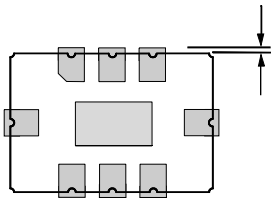


BLOCK DIAGRAM



Typical Printed Circuit Board Land Pattern

A typical land pattern for a circuit board is shown below. Grounding of the metallic center pad is optional.

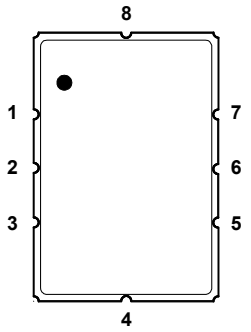


Typically 0.01" to 0.05" or 0.25 mm to 1.25 mm (8 Places)

(The optimum value of this dimension is dependent on the PCB assembly process employed.)

Electrical

Terminal Number	Connection
1	Tune
2	*Enable
3	Ground
4	Ground
5	Q Output
6	$\overline{Q}$ Output
7	V_{CC}
8	Ground
LID	Ground



Case Dimensions

Dimension	mm		Inches	
	MIN	MAX	MIN	MAX
A	13.46	13.97	0.530	0.550
B	9.14	9.66	0.360	0.380
C	1.93 Nominal		0.076 Nominal	
D	1.93 Nominal		0.076 Nominal	
E	2.54 Nominal		0.100 Nominal	
F	1.27 Nominal		0.050 Nominal	

*Enable Sense: Pin 2 Ground-Clock Off