

# SprloT 6UL

## Schematics DevBoard

## Table of Content

<b>Page 1</b>	Cover
<b>Page 2</b>	Block Diagram
<b>Page 3</b>	PWR TREE
<b>Page 4</b>	1DX Module
<b>Page 5</b>	CPU PWR
<b>Page 6</b>	LvDDR3
<b>Page 7</b>	eMMC
<b>Page 8</b>	CPU PERI1
<b>Page 9</b>	CPU PERI2
<b>Page 10</b>	PWR MGR
<b>Page 11</b>	SOM 80x2 Connectors
<b>Page 12</b>	
<b>Page 13</b>	
<b>Page 14</b>	
<b>Page 15</b>	
<b>Page 16</b>	
<b>Page 17</b>	
<b>Page 18</b>	
<b>Page 19</b>	
<b>Page 20</b>	
<b>Page 21</b>	
<b>Page 22</b>	
<b>Page 23</b>	
<b>Page 24</b>	
<b>Page 25</b>	
<b>Page 26</b>	
<b>Page 26</b>	
<b>Page 27</b>	
<b>Page 28</b>	

## Revision History

[illegible]

1. Unless Otherwise Specified:


All resistors are in ohms, 10%, 1/8 Watt, 0603  
All capacitors are in uF, 20%, 50V, 0603  
All voltages are DC  
All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

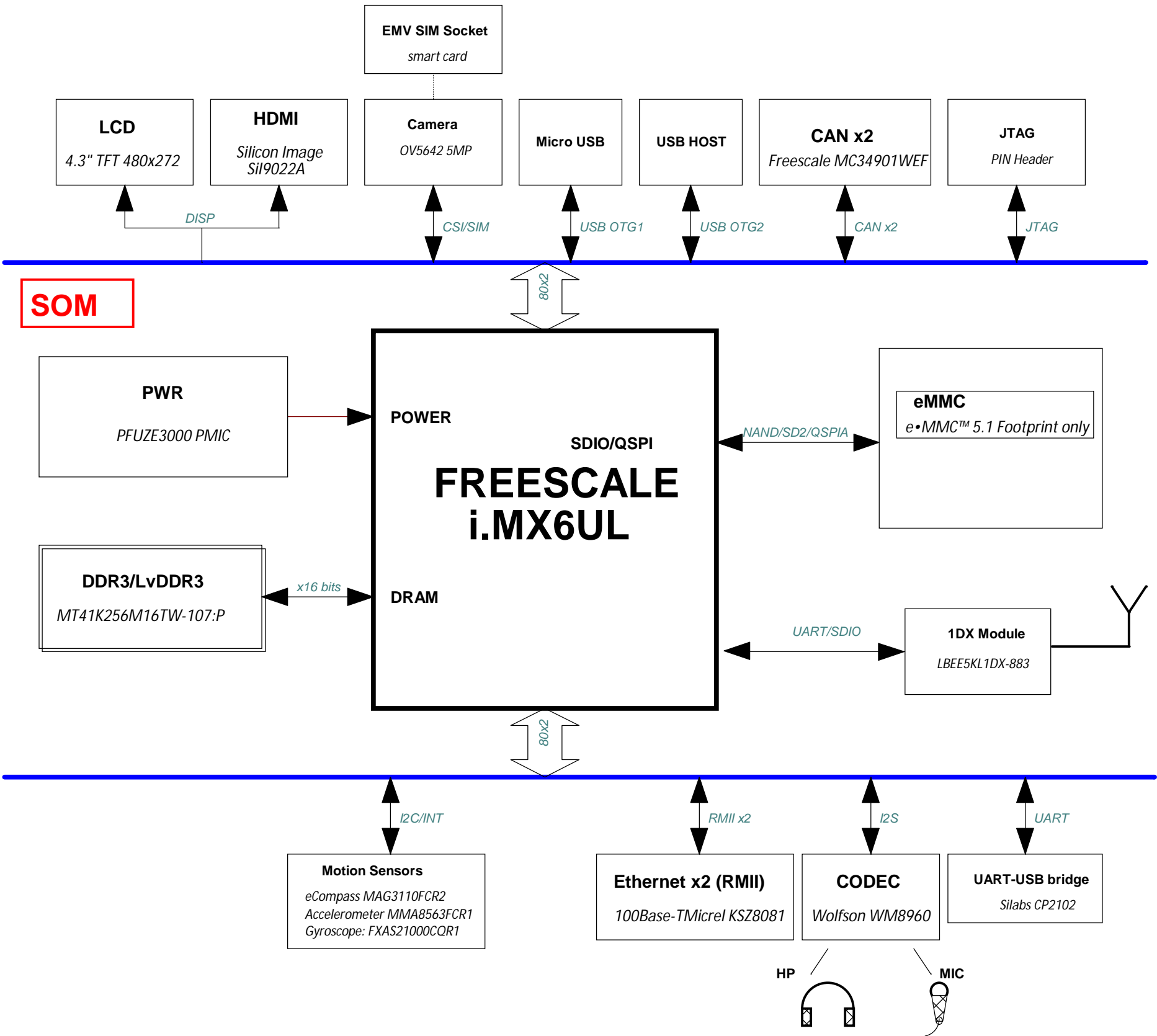
3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:  
   \_B Denotes - Active-Low Signal  
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

		Murata, Inc. 4100 Midway Road, Suite 2050 Carrollton, TX 75007	
Title			
Title and Rev History			
Size	Document Number		Engineer
C	801108		VH
Date:	Tuesday, August 01, 2017	Sheet	1 of 11
			PR

# i.MX6UL-SOM EVK Block Diagram



**SOM PWR TREE**

**WALL Adapter: 5V/3A** → **OVP** → **VSYS**

**PFUZE3000 PMIC**

- V33**: 2.85V-3.3V / 350mA
- SW1A**: 0.7V-1.425V / 1.8V/3.3V / 1A
- SW1B**: 0.7V-1.475V / 1.75A
- SW2**: (1.5V-1.85V) / (2.5V-3.3V) / 1.25A
- SW3**: 0.9V-1.65V / 1.5A
- VLD03(VREFDDR)**: 1.8V-3.3V / 100mA
- VLD04**: 1.8V-3.3V / 350mA
- VSBST**: 5V-5.15V / 600mA
- VLD01**: 1.8V-3.3V / 100mA
- VLD02**: 0.8V-1.55V / 250mA
- VCC\_SD**: (1.8V-1.85V)/(2.85V-3.3V) / 100mA

**LDO**: TLV71333PDBVR, 3.3V/100mA Iq = 4uA

**Breakout board**: 2.8V/300mA

**Breakout board LOAD SW**

**QSPI**: Micron N25Q256

**DCDC\_3V3**: 3.3V/200mA

**VPERI\_3V3**: 3.3V/370mA

**LvDDR3**: MT41K256M16TW-107:P

**eMMC 4GB**: EMMC04G-M627

**1DX MODULE**: LBEE5KL1DX-883

**i.MX6UL CPU**

**SOM**

**VDD\_SNVS\_IN**: 276uA

**VDD\_HIGH\_IN**: 125mA

**VDD\_SOC\_IN**: 900mA

**NVCC\_DRAM**: 50mA

**NVCC\_NAND**

**VDDA\_ADC\_3P3**

**NVCC\_SD**

**NVCC\_CSI**

**USB\_OTG1\_VBUS**: 50mA

**USB\_OTG2\_VBUS**

**VDD\_USB\_CAP**

**VDD\_ARM\_SOC**

**LDO\_ARM\_SOC**

**VDD\_ARM\_CAP**

**VDD\_SOC\_CAP**

**NVCC\_GPIO/NVCC\_ENET/NVCC\_LCDIF**

**NVCC\_DRAM\_2P5**

**LDO\_1P1**

**NVCC\_PLL**

**LDO\_2P5**

**VDD\_HIGH\_CAP**

**VDD\_SNVS\_CAP**

**muRata**

Murata, Inc.  
4100 Midway Road, Suite 2050  
Carrollton, TX 75007

Title: Power Tree

Size: C Document Number: 801108 Engineer: VH Rev: PR2

Date: Monday, March 06, 2017 Sheet: 3 of 11

**SOM PWR TREE**

**WALL Adapter: 5V/3A** → **OVP** → **VSYS**

**LDO**  
TLV71333PDBVR  
3.3V/100mA Iq = 4uA  
Always ON

**PFUZE3000 PMIC**

Component	Input Voltage Range	Current
V33	2.85V-3.3V	350mA
SW1A	0.7V-1.425V	1.8V/3.3V / 1A
SW1B	0.7V-1.475V	1.75A
SW2	(1.5V-1.85V)	(2.5V-3.3V) / 1.25A
SW3	0.9V-1.65V	1.5A
VLD03(VREFDDR)	1.8V-3.3V	100mA
VLD04	1.8V-3.3V	350mA
VSBST	5V-5.15V	600mA
VLD01	1.8V-3.3V	100mA
VLD02	0.8V-1.55V	250mA
VCC_SD	(1.8V-1.85V)/(2.85V-3.3V)	100mA

**Breakout board**  
2.8V/300mA

**Breakout board LOAD SW**

**QSPI**  
Micron N25Q256

**LvDDR3**  
MT41K256M16TW-107:P

**eMMC 4GB**  
EMMC04G-M627

**1DX MODULE**  
LBEE5KL1DX-883

**i.MX6UL CPU**

**SOM**

**Power Tree Details:**

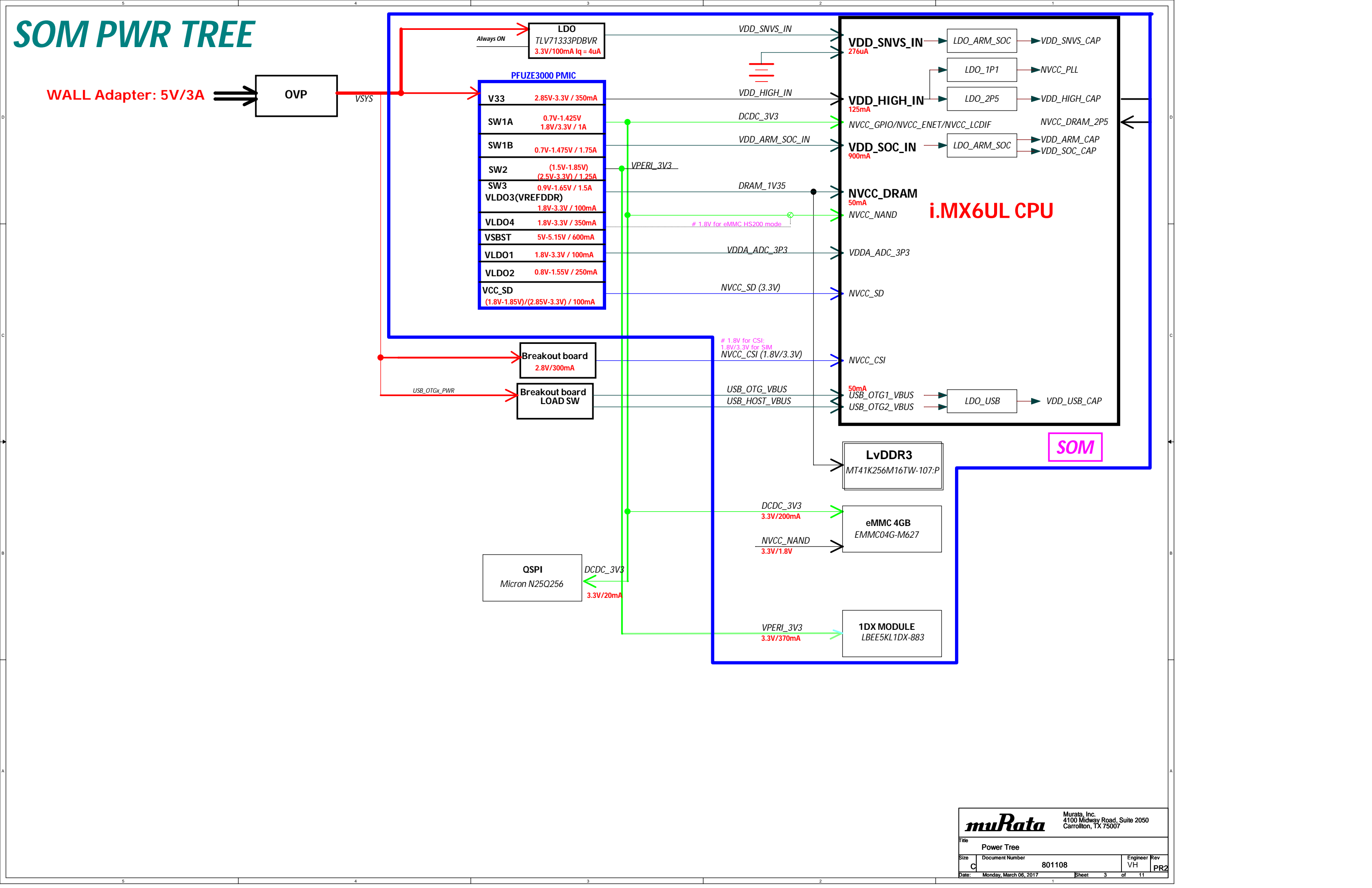
- V33** (2.85V-3.3V / 350mA) → **VDD\_SNVS\_IN** (276uA) → **LDO\_ARM\_SOC** → **VDD\_SNVS\_CAP**
- SW1A** (0.7V-1.425V / 1.8V/3.3V / 1A) → **VDD\_HIGH\_IN** (125mA) → **LDO\_1P1** → **NVCC\_PLL**
- SW1B** (0.7V-1.475V / 1.75A) → **VDD\_ARM\_SOC\_IN** (900mA) → **LDO\_2P5** → **VDD\_HIGH\_CAP**
- SW2** (1.5V-1.85V / 2.5V-3.3V / 1.25A) → **VDD\_ARM\_SOC\_IN** (900mA) → **LDO\_ARM\_SOC** → **VDD\_ARM\_CAP**
- SW3** (0.9V-1.65V / 1.5A) → **VDD\_ARM\_SOC\_IN** (900mA) → **LDO\_ARM\_SOC** → **VDD\_SOC\_CAP**
- VLD03(VREFDDR)** (1.8V-3.3V / 100mA) → **NVCC\_DRAM** (50mA)
- VLD04** (1.8V-3.3V / 350mA) → **NVCC\_NAND**
- VSBST** (5V-5.15V / 600mA) → **VDDA\_ADC\_3P3**
- VLD01** (1.8V-3.3V / 100mA) → **NVCC\_SD** (3.3V)
- VLD02** (0.8V-1.55V / 250mA) → **NVCC\_CSI**
- VCC\_SD** (1.8V-1.85V)/(2.85V-3.3V) / 100mA → **NVCC\_CSI**
- Breakout board** (2.8V/300mA) → **USB\_OTG\_VBUS** (50mA) → **LDO\_USB** → **VDD\_USB\_CAP**
- Breakout board LOAD SW** → **USB\_OTG\_VBUS** (50mA) → **LDO\_USB** → **VDD\_USB\_CAP**
- QSPI** (Micron N25Q256) → **DCDC\_3V3** (3.3V/20mA)
- LvDDR3** (MT41K256M16TW-107:P) → **DCDC\_3V3** (3.3V/200mA)
- eMMC 4GB** (EMMC04G-M627) → **NVCC\_NAND** (3.3V/1.8V)
- 1DX MODULE** (LBEE5KL1DX-883) → **VPERI\_3V3** (3.3V/370mA)

**muRata**  
Murata, Inc.  
4100 Midway Road, Suite 2050  
Carrollton, TX 75007

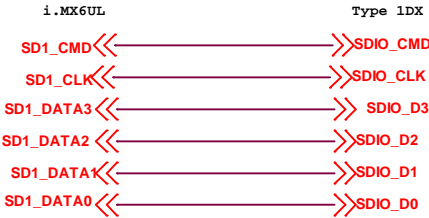
**Power Tree**

Size	Document Number	Engineer	Rev
C	801108	VH	PR2

Date: Monday, March 06, 2017 Sheet 3 of 11



SDIO interface mapping.



WIFI interface mapping.



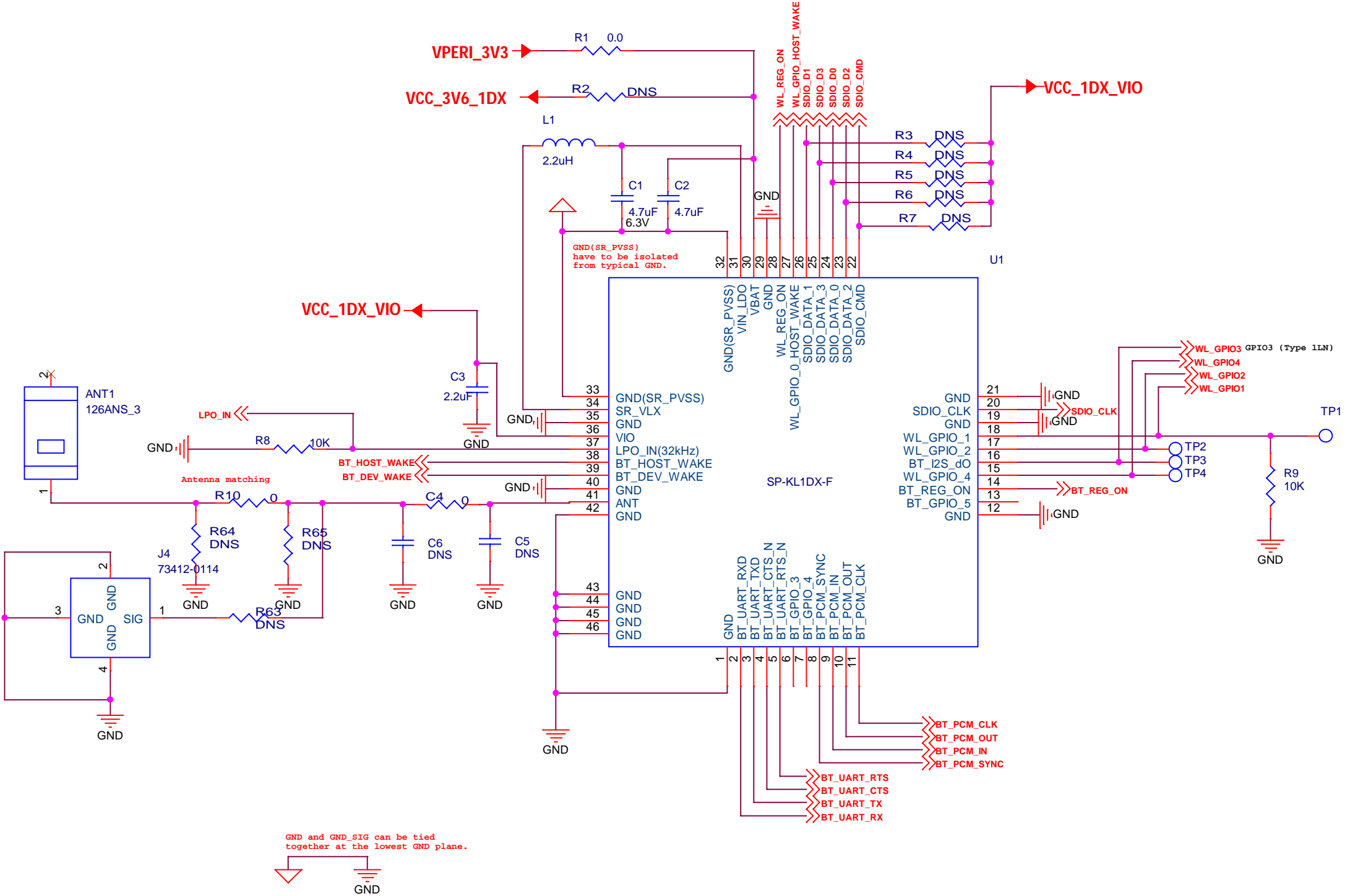
UART interface mapping.



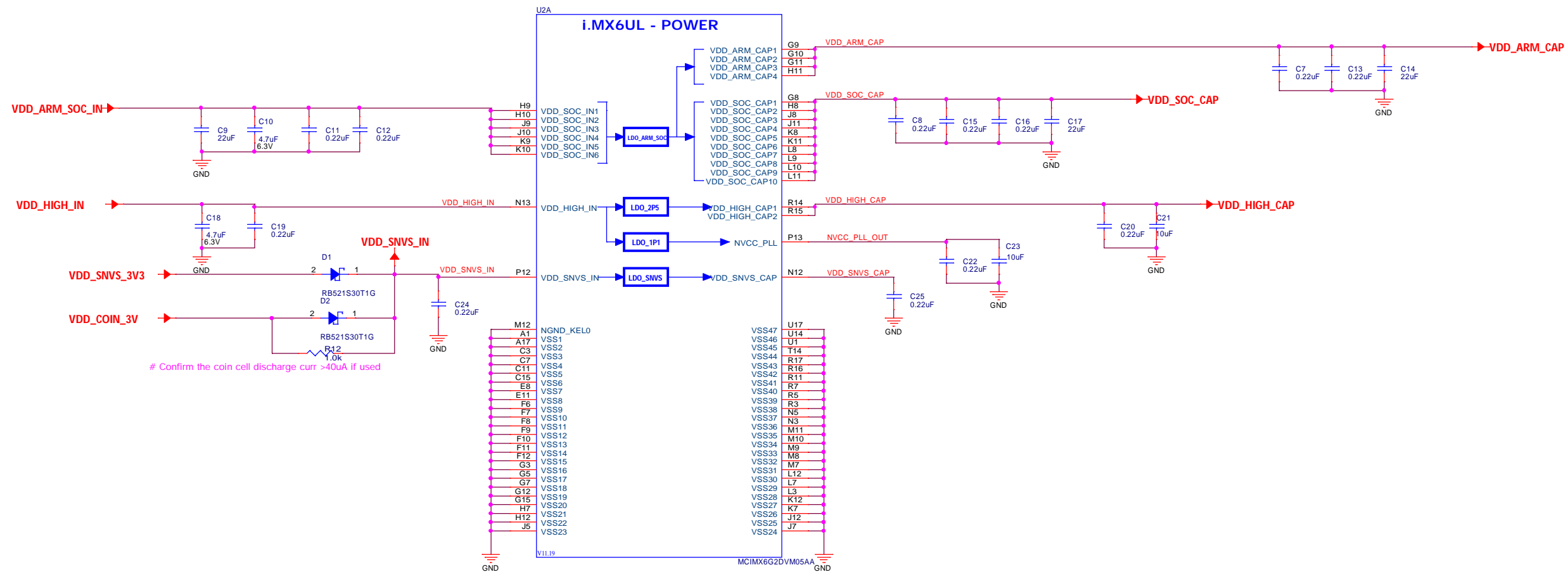
Bluetooth control interface mapping.



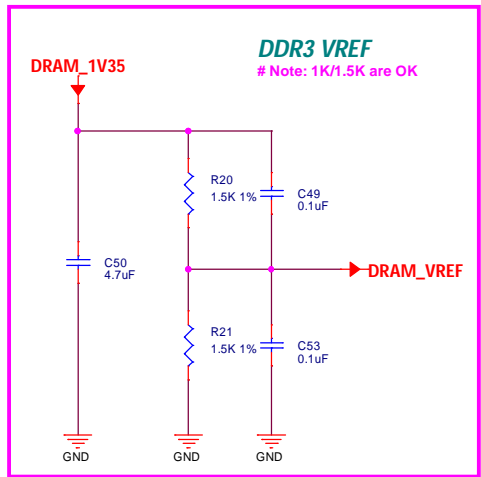
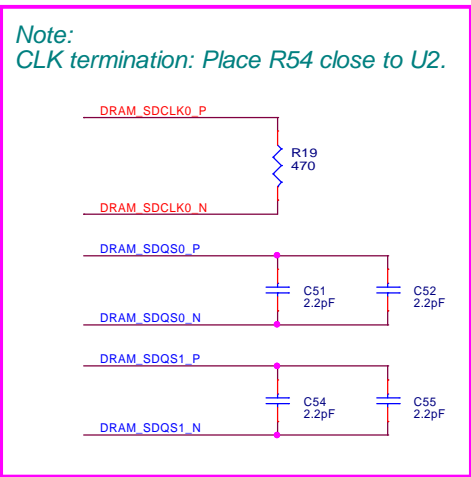
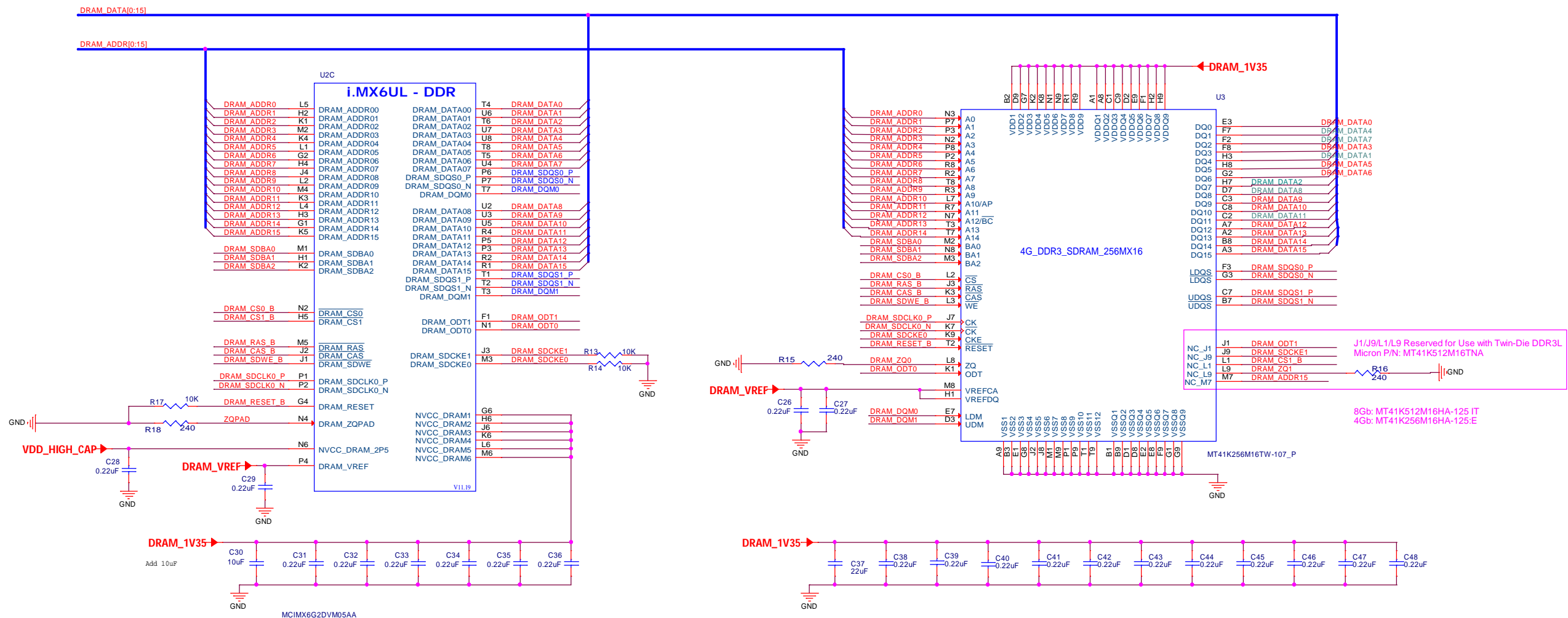
LPO\_IN <-> WB\_LO\_IN



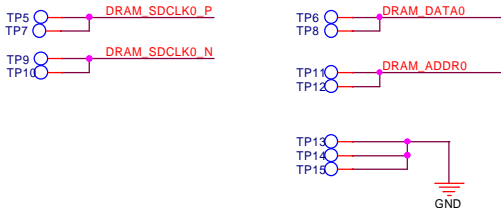
# i.MX6UL PWR



# DDR3/LvDDR3

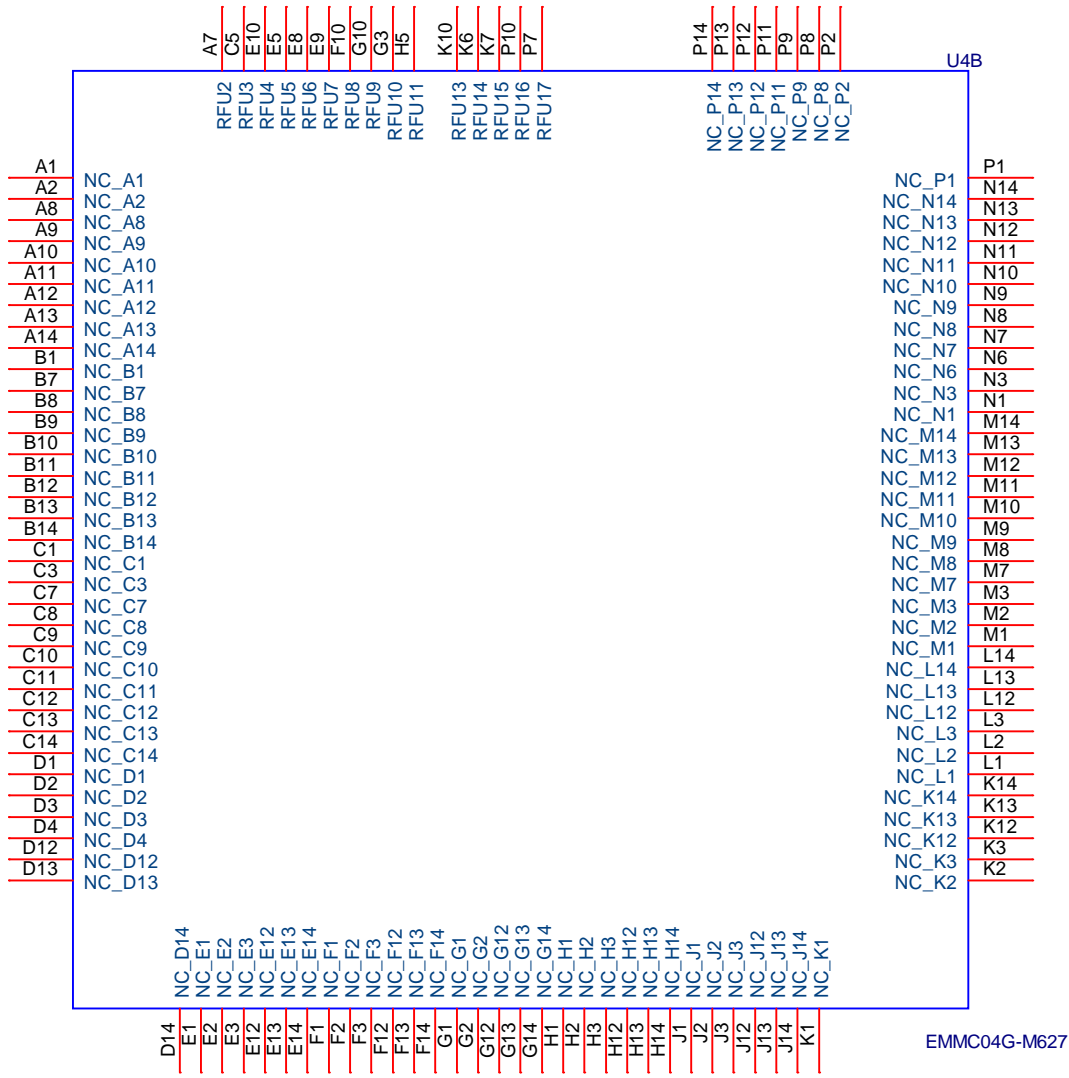
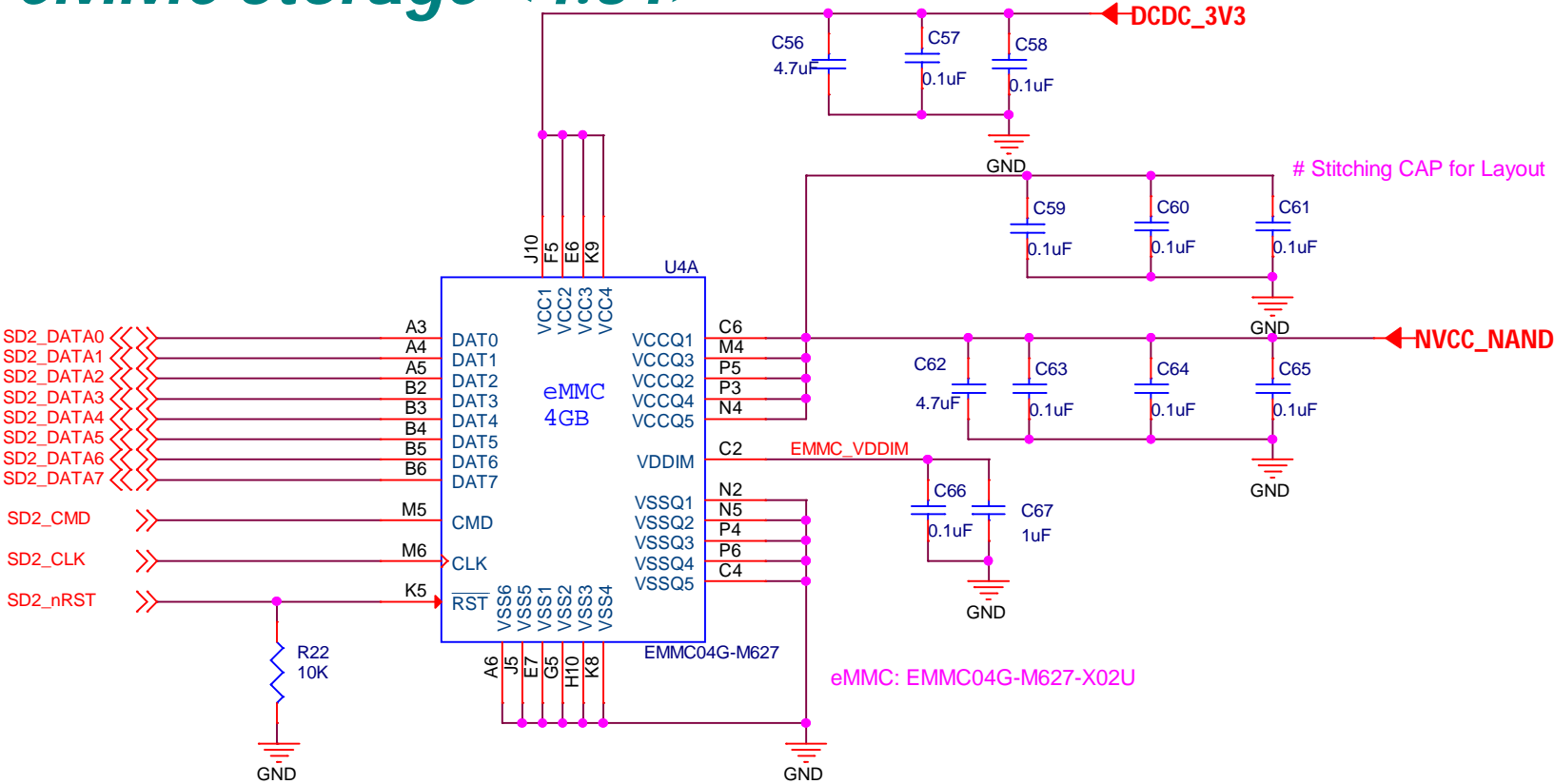


## DRAM Test Points

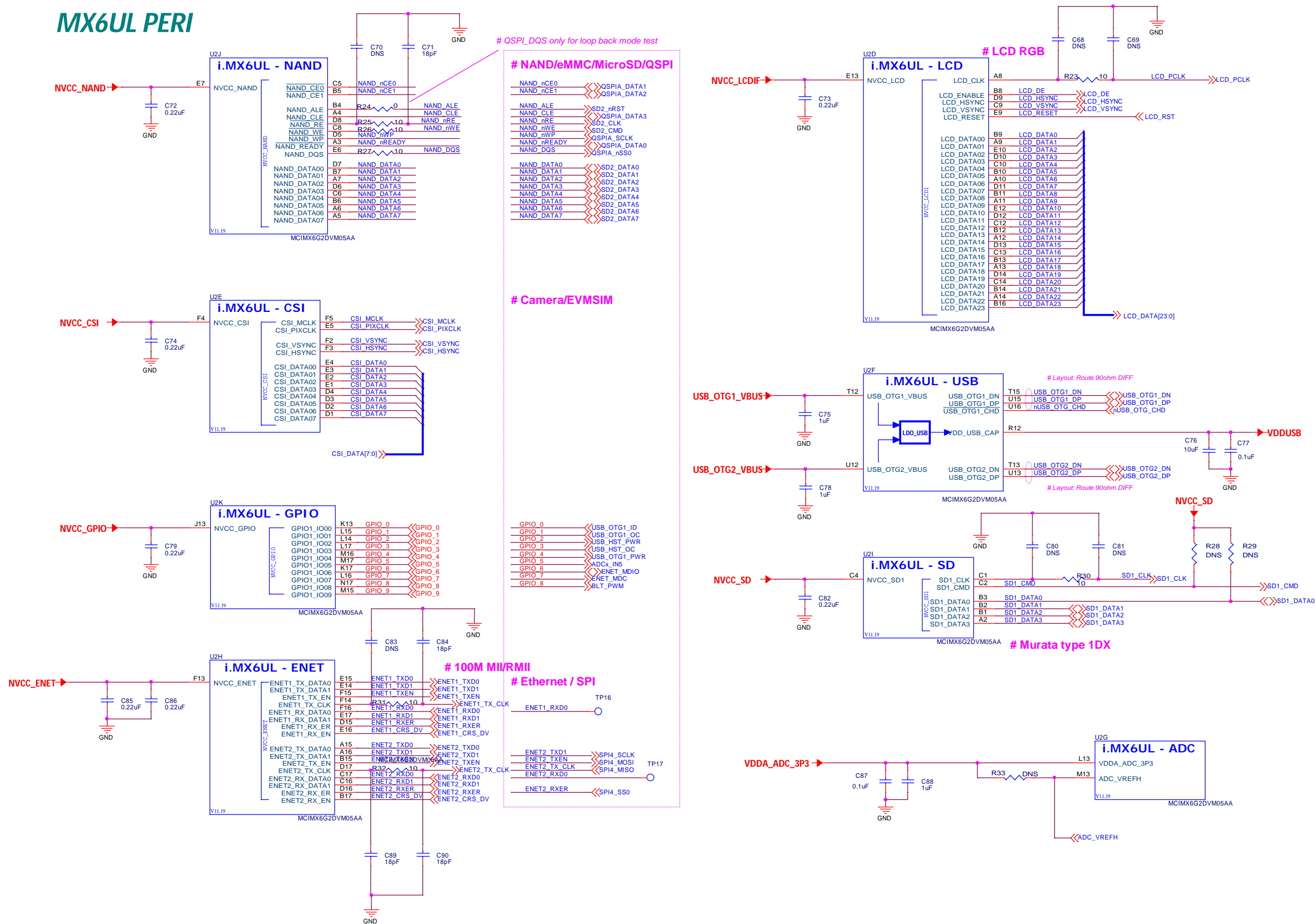


# Note:  
Test points for signal integrity measurement

eMMC Storage <4.51>

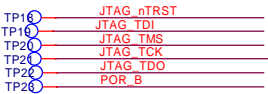


# MX6UL PERI

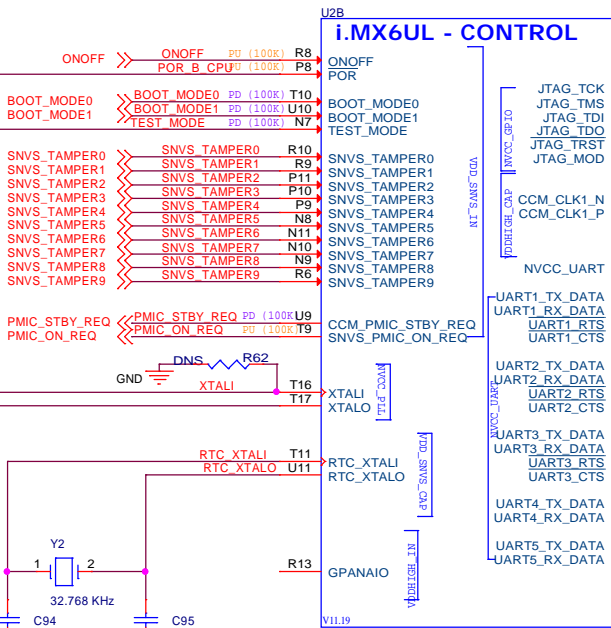
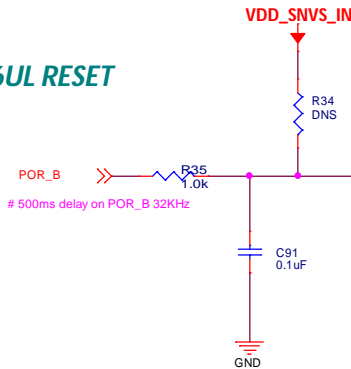




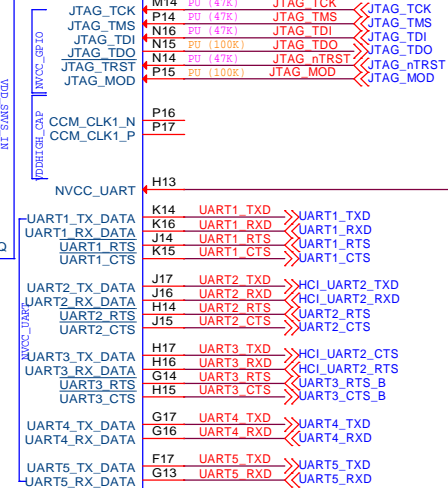
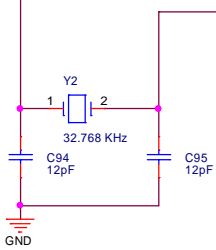
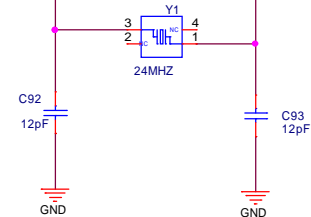
JTAG Debug



i.MX6UL RESET



# VDD\_SNVS\_IN PWR domain, IO CFG is need to prevent leakage. When TAMPER PIN used as GPIO, need to PULL DOWN 1M to GND to give a fixed state to the PIN to reduce the power consumption, Just for TO1.0



JTAG\_MOD SPDIF\_TX

# NVCC\_GPIO (J13) and NVCC\_UART (H13) should share one 0.22uF de-coupling cap. There is no PCB space to fit two caps.

NVCC\_UART

UART2\_RTS CAN2\_RX  
UART2\_CTS CAN2\_TX

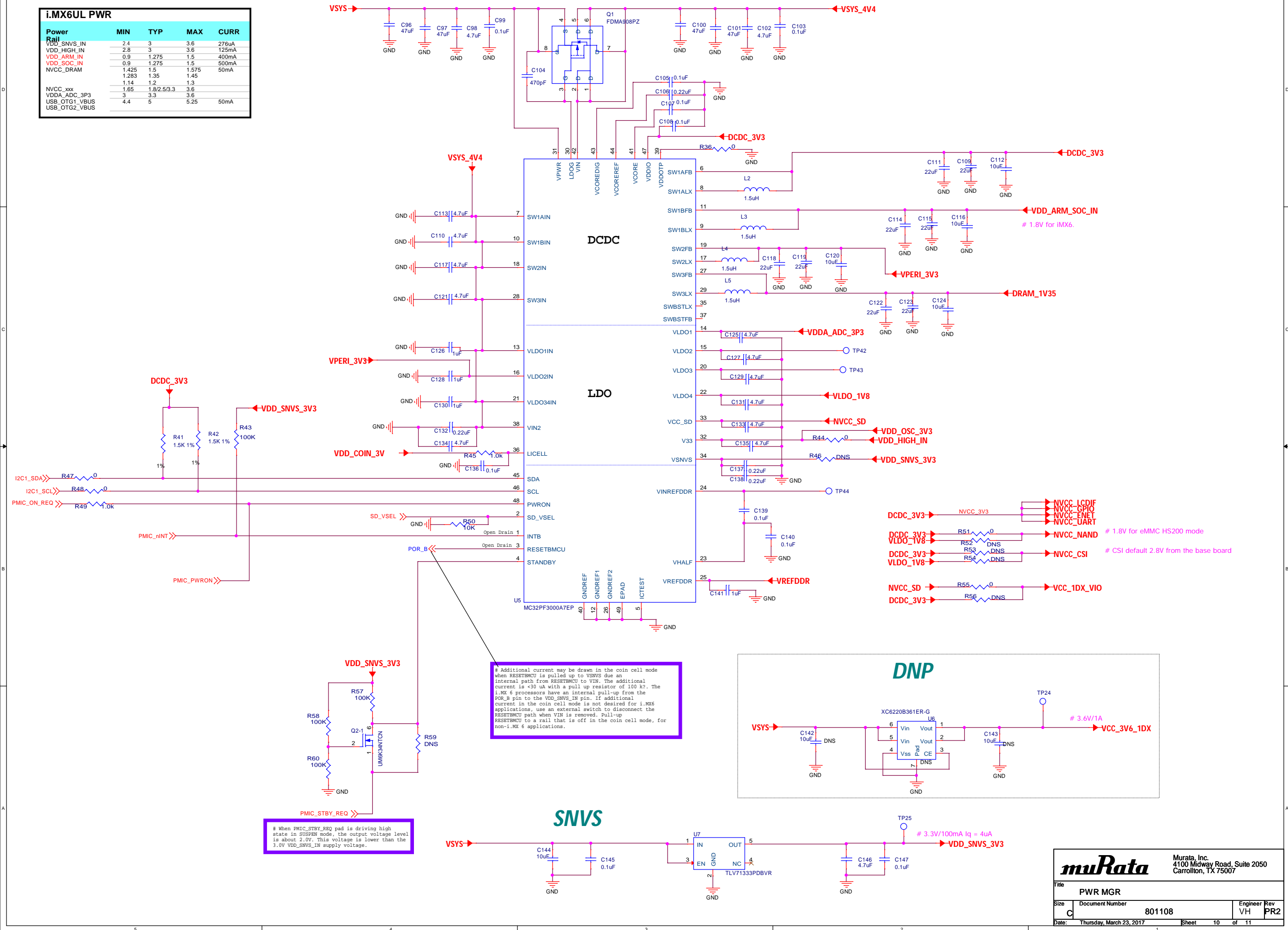
UART4\_TXD X2C1\_SCL  
UART4\_RXD X2C1\_SDA

MCIMX6G2DVM05AA

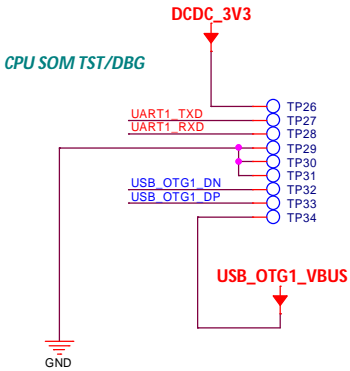
# PFUZE3000 PMIC

## i.MX6UL PWR

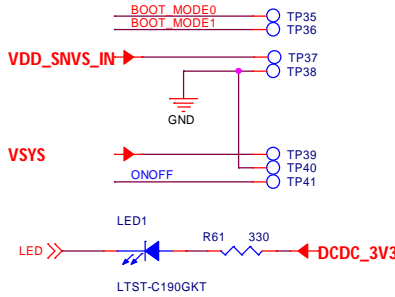
Power Rail	MIN	TYP	MAX	CURR
VDD_SNVS_IN	2.4	3	3.6	276uA
VDD_HIGH_IN	2.8	3	3.6	125mA
VDD_ARM_IN	0.9	1.275	1.5	400mA
VDD_SOC_IN	0.9	1.275	1.5	500mA
NVCC_DRAM	1.425	1.5	1.575	50mA
	1.283	1.35	1.45	
	1.14	1.2	1.3	
NVCC_xxx	1.65	1.8/2.5/3.3	3.6	
VDDA_ADC_3P3	3	3.3	3.6	
USB_OTG1_VBUS	4.4	5	5.25	50mA
USB_OTG2_VBUS				



TP for SOM MFG



BMOD TP for MFG TOOL



SOM 80x2

