Designing with a sample-hold won't be a problem if you use the right circuit

Part 1 of 3

Sample-hold circuits are widely used in analog signal-processing and data-conversion systems to store an analog voltage accurately over periods ranging from less than a microsecond up to several minutes. This capability suits them to numerous applications including data-distribution systems, data-acquisition systems, simultaneous sample-hold systems, a/d converter front ends, sampling oscilloscopes and DVMs, signal reconstruction filters, and analog computation circuits.

Although sample-holds are conceptually simple, their application is full of subtleties. In general, applications that need only slow to moderate speed and moderate accuracy generate few problems, but high-speed, high-accuracy applications are the ones that need careful design. An example of the latter is taking a 10-V sample in one microsecond or less with 0.01% accuracy.

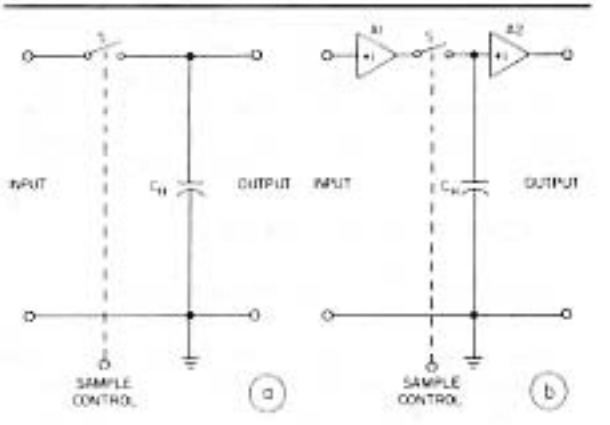
To select the right sample-hold for a particular job, and apply it properly as well, requires understanding the intricacies of its design and operation.

Basically speaking

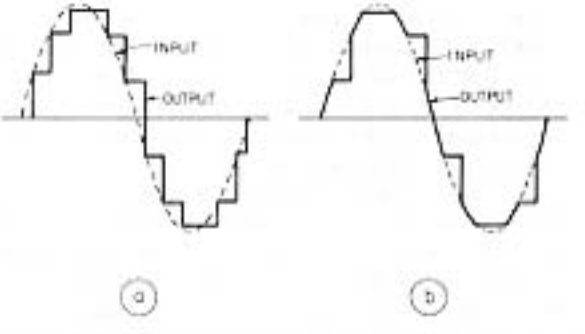
A sample-hold circuit is fundamentally a "voltage memory" device that stores a given voltage on a high-quality capacitor. The circuit can take a voltage sample and then "freeze" it for some specified period, while some other circuit or system uses the voltage.

Fig. 1a shows a sample-hold circuit in conceptual form. An electronic switch is connected to a hold capacitor so that when the switch closes, the capacitor charges to the input voltage. When the switch opens, the capacitor retains this charge and thus holds the desired voltage for a specified period.

There are three important sets of terminals in a sample-hold circuit: the analog input, the analog



1. **In a basic sample-hold circuit (a),** the switch closes to sample the input voltage. When the switch opens, the capacitor holds the voltage. A practical circuit (b) has unity-gain buffers to charge the capacitor without loading the source and to drive normal loads without changing the voltage stored by the capacitor.



2. **A sample-hold can operate in two different ways.** It can take a quick sample of the input and return right back to hold mode (a), or it can track the input for part of the time and hold it for the rest (b).

output, and the sample control terminals. Fig. 1b shows a practical circuit that includes input and output buffer amplifiers and a switch-driver circuit. The sample control input closes the switch for sample mode, or opens it for hold mode.

The sample-hold input terminals are usually the input of a high-impedance buffer amplifier since in most applications, such as operating at the output of an analog multiplexer, the source shouldn't be loaded. Likewise, the output has a low impedance so that the sample-hold can drive a load such as an a/d converter input. The output buffer amplifier must also present a very high input impedance, and very low bias current, to the hold capacitor so that its charge doesn't leak off too rapidly. In virtually all sample-hold designs, therefore, this amplifier has a junction-FET input stage. Similarly, the switch must be fast and have very low off-state leakage.

Sample-hold: An energy storage circuit

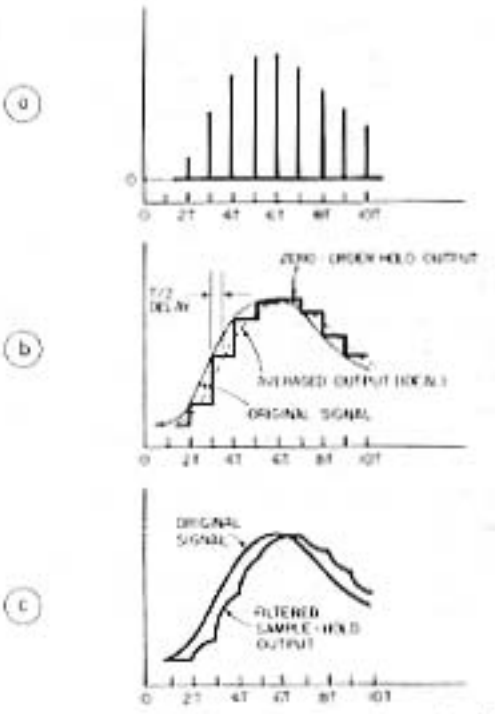
All sample-holds are basically accurate energy storage circuits. Since the hold capacitor is a key component in an accurate sample-hold, a fundamental question to be answered is: Why use a capacitor to store the energy?

It turns out that certain types of capacitors very nearly approach the ideal. They have extremely low leakage, and therefore very high equivalent parallel resistance. This resistance, commonly specified in megohm-microfarads and known as insulation resistance, is the parallel resistance of a one-microfarad capacitor and is numerically equal to the self-discharge time constant of the capacitor in seconds.

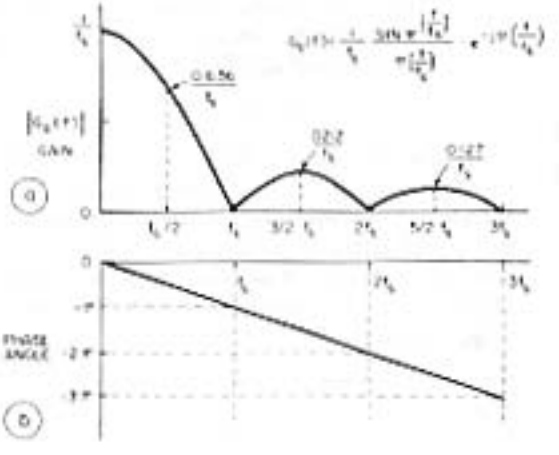
To find the parallel resistance for other capacitor values, divide the insulation resistance in megohm-microfarads by the capacitance in microfarads. Since the parallel resistance can be quite high for smaller value capacitors, most manufacturers specify a maximum "need not exceed" value, generally twice the insulation resistance. This means only that the parallel resistance is not measured or guaranteed by the manufacturer. It may well be as high as calculated.

The self-discharge time constant is the length of time required for an open-circuited capacitor to discharge to 36.8% of its charged voltage. High-quality capacitors used in sample-holds have insulation resistance as high as 10^6 megohm-microfarads, equivalent to a self-discharge time constant of one million seconds, or 11-1/2 days. In other words, this is only 1% droop in almost three hours.

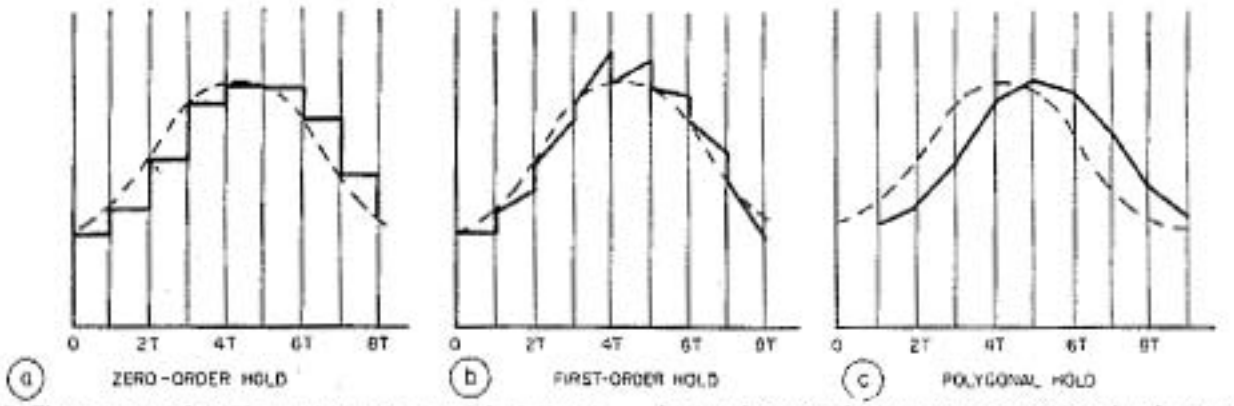
To get back to why capacitors are used for the energy storage, they approach the ideal much more closely than the alternative, which is an inductor. The figure of merit for an energy-storage element is its self-discharge time constant. A high quality short-circuited inductor is hard pressed to give a self-discharge time constant (L/R) as high as 10 seconds, while a capacitor can give a time constant (RC) of 10^6 seconds. (The only exception, a superconducting induc-



3. A zero-order hold reconstructs an analog signal that's been transmitted as a series of pulse samples (a). It does so by holding the amplitude of each pulse to fill in the spaces between them (b). Practical averaging uses a low-pass filter (c) that has more delay than the ideal averaging shown in (b).



4. The gain response of a zero-order hold (a) in terms of the sampling frequency f_s takes the form of the absolute value of (sin x)/x. The phase response (b) is linear because of the constant time delay.



5. Three types of holds reconstruct an original signal (dashed curve) differently. The output of a zero-order hold (a) is steady between samples. A first-order hold (b) extrapolates a new slope that's proportional to the difference between the two most-recent samples. Its output error is zero during constant-slope portions of the signal. The polygonal hold (c) interpolates between the two most recent samples.

tor, would, of course, be better than a high quality capacitor, but it would be difficult to package in an ordinary sample-hold circuit!)

Capacitors of certain types are therefore clearly superior to inductors when it comes to approaching the ideal. Acceptable types of capacitors include polystyrene, polycarbonate, polypropylene, and Teflon. In addition, MOS capacitors are excellent for hybrid circuit sample-holds.

Two other storage elements useful in specialized sample-holds are an electrochemical cell such as the Plessey Electro-Products E-Cell, and a register that holds the voltage digitally.

Sample-hold circuits are variously called zero-order-holds, track-and-holds, or sample-and-hold amplifiers. Although these terms are generally used interchangeably today, some technical distinctions should be pointed out.

Strictly speaking, a sample-hold takes a very fast sample and then goes into the hold mode. This means that the switch closes for only a very short period of time, usually because a pulse transformer drives the switch. A track and hold circuit, on the other hand, can track the input with the switch closed indefinitely and then go into the hold mode upon command.

A zero-order hold may be either a sample-hold or track-and-hold. When a device is called a zero-order hold, that means it's used as a signal recovery filter. There are various types of sample-hold recovery filters such as zero-order holds, first-order holds, fractional-order holds, and polygonal holds.

The term "sample-and-hold amplifier" can refer to either a sample-hold or a track-and-hold, and originates from the fact that operational amplifiers are used to make sample-hold circuits.

Although there's a technical distinction between the terms sample-hold and track-and-hold, it's automatically assumed that both functions are included in the term "sample-hold," as just about all sample-holds can also track and hold. The few circuits that can only sample for a short time, and cannot track the input, are clearly labeled this way.

To appreciate the difference between true sample-hold operation and track-and-hold operation, see Fig. 2. In Fig. 2a, a sample-hold periodically takes a sample of the input, a sinusoid in this case, and holds it for the rest of the time. In Fig. 2b, a track-and-hold tracks the input for part of the time and holds it for the rest. Here, the track time and hold time are equal.

Zero-order hold

An important sample-hold application is reconstructing, or recovering, an analog signal that has been transmitted as a train of pulse samples, like those in Fig. 3a. To reconstruct the original signal waveform, a sample-hold, or zero-order hold, retains the peak value of a sample until the next one arrives, thus filling in the spaces between them, as in Fig. 3b. The result is a reasonable reconstruction of the original signal before it was converted to a pulse train. Ideally, the average of the reconstructed waveform, shown dashed in Fig. 3b, is a near-replica of the original waveform, delayed by half the sampling period, T.

If the staircase waveform of the output is objectionable, a low-pass filter following the zero-order hold will smooth the waveform further. This filter will add further phase delay, but the resulting reconstruction of the original signal is much better, as Fig. 3c shows. The cutoff frequency of this filter must be determined from the sampling rate and the bandwidth of the signal to be recovered. The lower the cutoff frequency, the better the smoothing.

The zero-order hold is a type of filter. As with other types of filters, its gain-phase characteristics are important to know. These gain and phase terms are

plotted in Fig. 4. The zero-order hold is obviously not an ideal filter with its (sinx)/x amplitude response. Nevertheless, it reconstructs signals respectably. Its gain is slightly more than 3 dB down at a frequency of $f_s/2$, and it again goes to zero at integral multiples of the sampling frequency, f_s. There are some undesirable gain peaks at frequencies of $3/2\ f_s$, $5/2\ f_s$, etc. These peaks are frequently attenuated by a low-pass filter following the zero-order hold. A zero-order hold as a filter has a perfectly linear phase response (Fig. 4b), which results in the constant phase delay of T/2 for the output signal.

There are also more-sophisticated recovery filters than the zero-order hold circuit. These higher-order hold circuits, known as first-order holds, second-order holds, etc., reconstruct a signal more accurately than a zero-order hold (Fig. 5). A first-order hold does this by retaining the value of the previous sample as well as the present one. It then extrapolates from existing data to predict the slope to the next sample, which hasn't arrived yet (Fig. 5b). When a new sample comes in, it generates a slope proportional to the difference between this sample and the previous one. If the slope of the original signal hasn't changed much, the resulting error is small; for a constant slope, the error is zero. When the original signal reverses its slope quickly, the output "goes the wrong way," causing a fairly large error for one sample period.

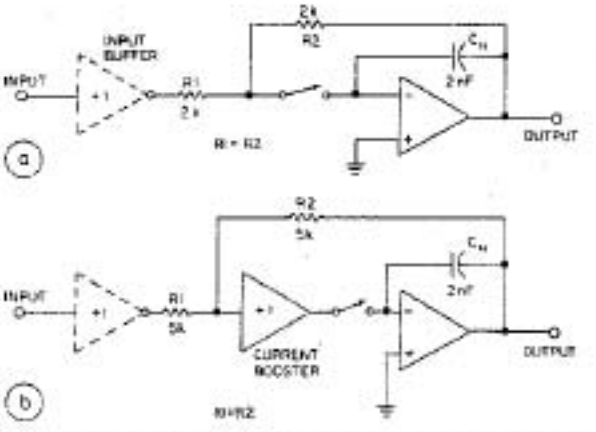
An interpolative first-order hold, also called a polygonal hold, reconstructs the original signal much more accurately. This circuit also generates a line segment with a slope proportional to the difference between consecutive samples, but rather than extrapolate into the future, it interpolates between samples already received. Its accuracy is achieved at the expense of a delay of one sample period, which is necessary because a new sample must arrive before the line segment can be generated by starting from the previous sample.

Lots of circuit variety

Sample-holds come in many different circuit configurations, each suited to different speed and accuracy requirements. It's important to know the common configurations and how they operate to choose the proper type and apply it properly.

One configuration is popular because it's accurate and simple. This circuit, shown in Fig. 6a, has a gain of −1 since $R_1 = R_2$; however, making R_2 larger than R_1 gives inverting gains larger than one. When the switch closes, hold capacitor C_H charges to the negative of the input voltage. The switch opens after the capacitor has acquired this voltage to the desired accuracy.

Although potentially very accurate, this circuit is not a fast sample-hold. The capacitor charges slowly since it has a time constant of R_2C_H; with practical values such as R_2 = 2k and C_H = 2 nF, the time



6. This type of inverting, closed-loop circuit is both accurate and simple. The charge time constant, R_2C_H, of the basic circuit (a) is much too long for some applications. The current booster in (b) speeds up charging considerably. The input resistance, R_1, may be too low for some sources; the buffer raises it a great deal.

constant is 4 μs. To reach a value within 0.01% of the input requires about nine time constants, or in this case, 36 μs.

Speed can be improved considerably, as shown in Fig. 6b, by adding an amplifier with current gain, inside the feedback loop. The operational amplifier must also be able to supply this current to the capacitor. Since these amplifiers have low output resistance, the circuit's time constant is much lower. For example, with the same valued capacitor and an amplifier output resistance of 20 Ω, the time constant is only 40 ns rather than 4 μs. Now, only the amplifiers' output current capability limits charging.

With a maximum output current of 20 mA from this amplifier to charge the capacitor and a 40-ns time constant, the capacitor takes just 1.2 μs to charge to within 0.01% of final value. This is much faster than the 36 μs for the previous circuit. Note that in the latter case, Fig. 6b, R_1 and R_2 can be larger since R_2 no longer determines the charging time constant.

An input buffer amplifier improves this circuit further by boosting the input resistance to a much higher value than that of the input resistor R_1. In fact, the input resistance can be as high as 10^9 to 10^{12} ohms. Such high resistances are required when a sample-hold follows an analog multiplexer. In this case the buffer amplifier must be fast, since its settling time becomes part of the time required to charge the holding capacitor. The buffer can also be added to the circuit of Fig. 6a. Both sample-holds in Fig. 6 are referred to as closed loop, since the capacitor charging takes place within a closed loop circuit.

Fig. 7 shows a noninverting closed-loop sample-hold in which A_1, that is serving as both an input buffer amplifier and an error-correcting amplifier, compares the output voltage to the input voltage, then charges the holding capacitor until this error is reduced to zero.

Amplifier A_2 also gives this circuit a high input resistance.

Thanks to the error-correcting feedback in this sample-hold, A_2 need not be very accurate so long as its gain is roughly unity. Resistor R isolates the output of A_2 from the input of A_1 during hold mode.

This circuit is both fast and accurate; how fast it charges the capacitor depends on the speed of A_1 and its output current capability. Two back-to-back diodes clamp A_1's output to its negative input so that A_1 remains closed-loop stable when the switch is opened. Note that in this circuit the switch must float up and down with the input voltage, whereas in the circuits of Fig. 6 the switch always operates at virtual ground.

Operational transconductance amplifiers

Fig. 8 shows another type of sample-hold circuit, which is versatile and can be operated in a number of closed loop configurations. This circuit is an operational integrator that can be enclosed in the feedback loop of A_1. In this case, however, A_1 is an operational transconductance amplifier; that is, one that produces an output current proportional to its input voltage. The current charges the holding capacitor while the integrator's input remains at virtual ground.

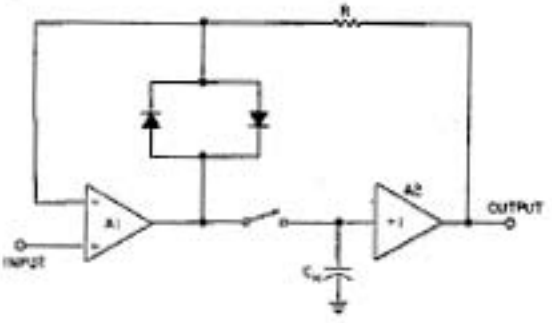
In this circuit, the two switches operate out of phase. Switch S_1 closes to sample, then S_2 closes to reduce hold-mode feedthrough when S_1 opens again.

This circuit can be connected in different ways as a closed-loop sample-hold: Fig. 9a shows the most commonly used connection, a noninverting sample-hold with a gain of +1; Fig. 9b shows the noninverting connection with gain, and Fig. 9c shows the inverting connection with gain.

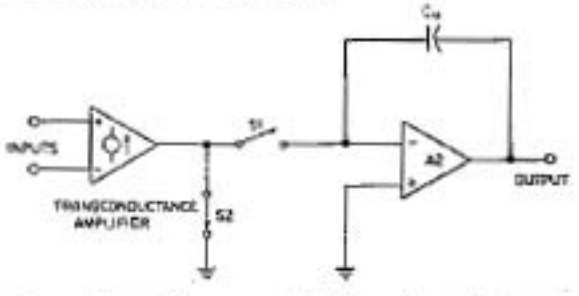
Both of the switches in these circuits operate at virtual ground, an advantage in driving the switch and producing an accurate output voltage. This circuit has been successfully used in monolithic, hybrid, and modular sample-hold devices.

Another popular noninverting, unity-gain circuit is shown in Fig. 10. It's basically the same as the one shown in Fig. 1b, with two unity-gain buffer amplifiers. This type of open-loop sample-hold is commonly used in ultra-fast designs. In this case, a pulse transformer drives a fast diode bridge switch.

Normally, the supply voltage back-biases the diodes. Sampling is done by a fast-rise command pulse that turns on the diodes to charge the hold capacitor from the input buffer. Using ultra-fast buffer amplifiers and an appropriate diode-gate switch, such sample-holds can charge the hold capacitor to a full-scale change in as little as 30 nanoseconds. Because of the open-loop configuration, there is no problem with phase delays from output to input caused by a feedback loop. This means that the circuit is both fast and stable.



7. **Closed-loop sample-holds can also be noninverting.** In this configuration, A_1 is both an input buffer and an error-correcting amplifier. When the switch closes, current from A_1 charges the hold capacitor until the output equals the input. The pair of diodes clamps A_1's output to keep it stable when the switch is open.



8. **Several closed-loop sample-hold configurations** can be built around this circuit, shown without its feedback connections. Basically, it's an operational integrator driven by an operational transconductance amplifier, A_1.

The input buffer in this circuit is difficult to design, for it must be both fast and stable while driving the hold capacitor load. Sampling switches, however, cause no such problems.

The basic sampling switch circuits commonly use junction FETs, MOSFETs, D-MOS FETs, and diode-gate switches. All of these can be both fast and accurate. The FET-type switches have the advantage of zero offset since they are purely resistive in the closed state. The diode-gate switch does have an offset voltage, however, which is minimized by properly matching the diode forward-voltage drops.

The infinite-hold circuit

All sample-hold circuits have the problem that once they are in the hold mode, the charge will gradually leak off the hold capacitor due to switch leakage, capacitor leakage, and output amplifier bias current. It was mentioned previously that a digital register can store a number equivalent to a voltage value as long as necessary.

The "infinite hold" circuit uses this principle to store a voltage value for any required time without any drift due to leakage. The circuit, shown in Fig. 11, is basically a tracking a/d converter, with its output

Know your circuit

Sample-hold: The generic term used for track-and-hold, zero-order hold, or sample-and-hold amplifier, it describes basically a circuit that acquires an analog input voltage and accurately stores it for a specified period of time.

Track-and-hold: A sample-hold circuit that can continuously follow the input signal until switched into the hold mode.

Signal-recovery filter: A circuit that reconstructs an analog signal from a train of analog samples.

Zero-order hold: A sample-hold circuit used as a signal recovery filter. So called because its output represents the first term of a power-series approximation to the input.

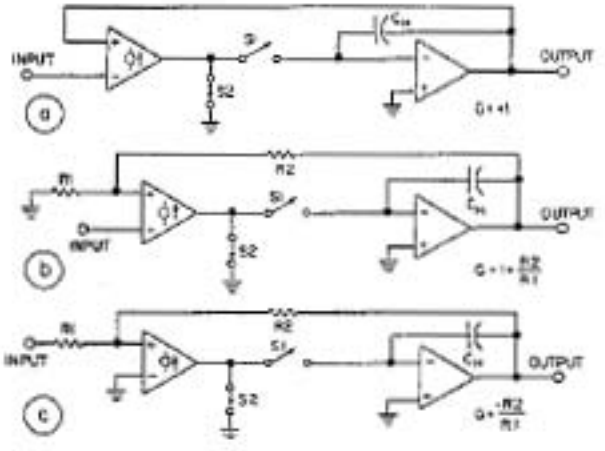
First-order hold, or extrapolative hold: A complex signal-recovery filter that predicts the next sample value by generating an output slope equal to the slope of a line segment connecting previous and present samples. In a sense, it works toward the future.

Polygonal hold, or interpolative hold: A complex signal-recovery filter that generates a straight-line segment output that joins the previous sample value to the present sample. It uses available data to reconstruct the signal more accurately than other hold circuits, but with a one-sample-period delay.

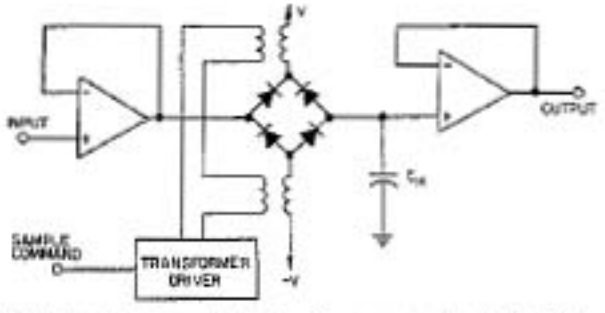
Infinite hold: An analog/digital sample-hold that digitally holds an analog voltage indefinitely without the decay of capacitor storage.

Closed-loop sample-hold: A sample-hold circuit that charges the hold capacitor within a negative feedback loop during sampling to achieve high accuracy.

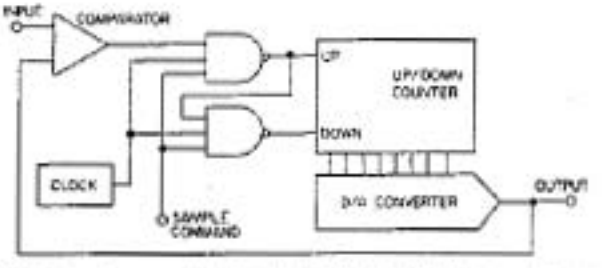
Open-loop sample-hold: A sample-hold circuit that does not enclose the hold capacitor within a feedback loop.



9. Here are three different ways to connect the input and feedback to the partial circuit in Fig. 8. The circuit in (c) has unity gain if the input (R_1) and feedback (R_2) resistors have equal values.



10. Ultra-fast sample-holds often use a circuit like this. It has a diode-bridge switch and operates open-loop. The diodes are biased off until a sample command arrives; then the pulse transformer's output turns on the diodes, which connect the input buffer amplifier to the hold capacitor. A 30-ns full-scale change is possible.



11. Sometimes called an "infinite hold," this circuit can hold a sample indefinitely without the droop that happens with capacitor storage. It's an a/d converter with its output taken from the analog feedback line. A high on the sample command line lets the output follow the input. A low freezes the count inputs, so the count doesn't change.

from the analog feedback line rather than from the counter. It consists of a d/a converter, up-down counter, clock, and analog comparator. The circuit operates by directing clock pulses into the up or down count inputs of the bidirectional binary counter that controls a d/a converter.

An analog comparator tests the output voltage of the d/a converter against the input voltage and directs the clock pulses to the counter so that the converter's output voltage changes toward the input. When the input voltage is reached, the circuit oscillates within one count of the input value. When the sample command goes low, the counter retains its contents indefinitely until the next sample is taken.

This circuit is not particularly fast since it must go to each new value one count at a time until the input voltage is reached. Different counting techniques will speed it up, however. Its accuracy depends on the resolution of the d/a converter; ±0.01% accuracy requires at least 12 bits. ■■