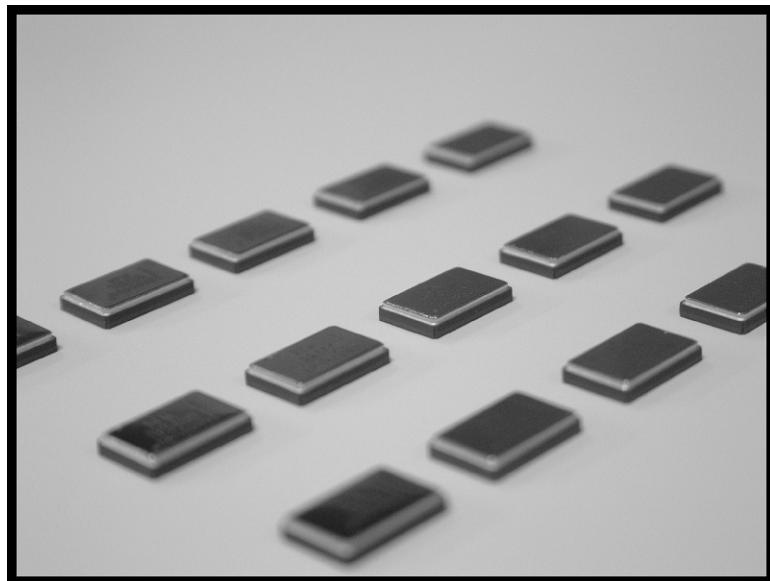




Third-Generation ASH Transceiver Designer's Guide



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1 Introduction

1.1 Short-Range Wireless Data Communications

Short-range wireless systems transmit 0.0001 to 10 mW of RF power on frequencies from 300 to 960 MHz, and operate over distances of 3 to >1000 meters (single hop). Once certified to comply with local communications regulations, they do not require a license or "air-time fee" for operation. Short-range wireless systems can be designed to operate from small batteries for extended periods of time. More than 150 million products will be manufactured this year that utilize short-range wireless for security, control and data transmission. Many new applications are emerging, and Murata estimates that more than 300 million short-range wireless products will be manufactured in 2007.

The classical uses for short-range wireless systems are one-way remote control and alarm links, including garage door openers, automotive "keyless entry" transmitters, and home security systems. Recently, a strong interest has also developed in two-way data communications applications. Short-range wireless data systems are used to eliminate nuisance cables on all types of digital products, much as cordless phones have eliminated cumbersome phone wires.

The following list of example applications demonstrates the diversity of uses for short-range wireless data systems:

- Wireless bar-code and credit-card readers
- Wireless and bar-code label printers and credit-card receipt printers
- Smart ID tags for inventory tracking and identification
- Wireless automatic utility meter reading systems
- Communications links for hand-held terminals, HPCs and PDAs
- Wireless keyboards, joysticks, mice and game controls
- Portable and field data logging
- Location tracking (follow-me phone extensions, etc.)
- Sports and medical telemetry
- Surveying system data links
- Engine diagnostic links
- Polled wireless security alarm sensors
- Authentication and access control tags

Murata's second and third-generation amplifier-sequenced hybrid (ASH) radios are specifically designed for short-range wireless applications. These radios provide robust operation, very small size, low power consumption and low implementation cost. All critical RF functions are contained in the hybrids, simplifying and speeding design-in. ASH radios can be readily configured to support a wide range of data rates and protocol requirements. These radios features excellent suppression of transmitter harmonics and virtually no RF emissions when receiving, making them easy to certify to short-range radio regulations. The third-generation (third-generation) ASH transceiver is the flagship of Murata's third-generation ASH radio product line. While this designer's guide focuses on the third-generation ASH transceiver, most of the information provided is directly applicable to second-generation ASH transmitters, receivers, and transceivers. The exceptions are discussed in section 3.4 of the Appendix.

1.2 Operating Authorities

Low-power wireless products do not have to be individually licensed, but they are subject to regulation. Before low-power wireless systems can be marketed in most countries, they must be certified to comply with specific technical regulations. While these regulations vary from country to country, they follow the same general philosophy of assuring that short-range wireless systems will not significantly interfere with licensed radio systems. Regulations specify limitations on transmitted power, harmonic and spurious emission levels, transmitter frequency stability, and modulation bandwidth. See section 1.4.6 below for additional details.

1.3 Operating Distance

The operating distance of a low-power wireless system depends on transmitter power, receiver sensitivity, choice of antennas, data encoding, data rate, bit error rate (BER) requirements, the communication protocol used, the threshold (squelch) level used, the required fading margin, and especially the propagation environment. A “textbook” approach to estimating operating distance is as follows:

1. Determine the acceptable “clear channel” packet error rate (PER) you would like your system to achieve.
2. Estimate the bit error rate $\text{BER} = \text{PER}/(\text{number of bits per packet})$ based on the protocol used.
3. Estimate the signal-to-noise ratio (per bit) required to achieve the BER.
4. Estimate the needed signal strength at the receiver from the signal-to-noise ratio, receiver noise figure, implementation loss and receiver filter bandwidth.
5. Estimate the allowed path loss by adding the transmitter power (dB) to the transmitter and receiver antenna gains, and subtracting the fading margin and the required receiver signal strength.
6. Estimate the operating distance from the allowed path loss and the propagation characteristics of the local (application) environment.

This procedure is obviously complex, and many factors have to be estimated to make the calculation. The propagation loss of the local environment is especially difficult to estimate. Propagation loss in “free space” is proportional to $1/d^2$, but can be higher than $1/d^4$ in dense cubical office space. In many cases, a better estimate of operating distance can be made by using a Virtual Wire® Development Kit as a propagation survey tool.

An example operating distance calculation based on the above procedure is provided in the Appendix. Informal testing suggests that third-generation products give triple the range estimates over second-generation devices. We stress again that it is very important to conduct “real world” range testing in several locations for your application in making an assessment of operating range.

1.4 Key System Issues

Murata supports hundreds of customers that engineer and manufacture short-range

wireless products. The most successful customers approach their short-range wireless designs from a system point of view. In addition to the choice of radio technology, there are six other key system issues to consider in developing a short-range wireless product:

1.4.1 Fail-safe system design

Most short-range wireless systems operate with few interference problems. However, these systems operate on shared radio channels, so interference can occur at any place and at any time. *Products that incorporate short-range wireless technology must be designed so that a loss of communications due to radio interference or any other reason will not create a dangerous situation, damage equipment or property, or cause loss of valuable data.* The single most important consideration in designing a product that uses any short-range wireless technology is safety.

1.4.2 Antennas and propagation

Antenna choice and location - suitable antennas are crucial to the success of a low-power wireless application. Here are several key points to consider in using antennas in your application:

- Where possible, the antenna should be placed on the outside of the product. Also, try to place the antenna on the top of the product. If the product is "body worn", try to get the antenna away from the body as far as possible.
- Regulatory agencies prefer antennas that are permanently fixed to the product. In some cases, antennas can be supplied with a cable, provided a non-standard connector is used to discourage antenna substitution (these connectors are often referred to as "Part 15" connectors).
- An antenna can not be placed inside a metal case, as the case will shield it. Also, some plastics (and coatings) significantly attenuate RF signals and these materials should not be used for product cases, if the antenna is going to be inside the case.
- Many suitable antenna designs are possible, but efficient antenna development requires access to antenna test equipment such as a network analyzer, calibrated test antenna, antenna range, etc. Unless you have access to this equipment, the use of a standard antenna design or a consultant is recommended.
- A patch or slot antenna can be used in some applications where an external antenna would be subject to damage.

The human body readily absorbs RF radiation in the UHF frequency range, especially above 750 MHz. The signal from a body-worn transmitter can be attenuated 20 to 30 dB in any direction that passes through the user's body. When designing body-worn products, you have to plan for this extra attenuation.

Mounting the antenna close to the user's body will also reduce signal strength in directions away from the user's body. Try not to mount the antenna any closer than 1.5 cm from the user's body, with 2 to 3 cm preferred.

RF Propagation - indoor radio propagation is an issue for special consideration. In most indoor locations, “dead spots” can be found where reception is very difficult. These can occur even if there appears to be a line-of-sight relationship between the transmitter and receiver locations. These “dead spots”, or nulls, are due to multiple transmission paths existing between two points because of reflections off metal objects such as steel beams, concrete rebar, metal door, window and ceiling tile frames, etc. Nulls occur when the path lengths effectively differ by an odd half-wavelength. Deep nulls are usually very localized, and can be avoided by moving slightly. Hand-held applications usually involve some movement, so automatic packet retransmission often succeeds in completing the transmission as hand motion moves the node through the null and back into a good transmission point.

Diversity reception systems - diversity reception techniques are very helpful in reducing indoor null problems. Many short-range wireless systems involve communications between a master and multiple slave units. In this case, the master transmission can be sent twice; first from one master and then again from a second master in a different location. The nulls for each master will tend to be in different locations, so a slave is very likely to hear the transmission from one or the other master. Likewise, a transmission from a slave is likely to be heard by at least one of the masters.

For further information, see Murata’s application note, *Antennas for Low Power Applications*, on Murata’s web site (<http://www.murata.com>). The application note includes test results on eleven types of antennas for short-range wireless applications, along with an introductory tutorial on antennas and techniques for antenna testing and tuning.

1.4.3 Data coding for radio transmission

Data streams must be encoded to add the characteristics needed for efficient radio transmission. As a minimum, encoding must make it possible to AC-couple the transmitted signal. This greatly simplifies the design of a radio system and helps to improve its performance. The encoding technique should also produce frequent transitions in the transmitted signal, which facilitates data clock synchronization and efficient data recovery at the receiver.

Radio transmissions must be bandwidth limited to control the signal-to-noise ratio observed at the receiver, as the noise power added during a radio transmission is proportional to the receiver bandwidth. The bandwidth required to transmit a data stream depends both on its data rate and how it has been encoded. Figure 1.4.3.1 shows three encoding schemes for single bits. Note that although the data rate is the same in each case, the minimum pulse width in the encoded signals vary 3:1. *The minimum bandwidth that can be used in the receiver depends on the minimum pulse (or gap) width in the encoded data stream, not the data rate.* It should be noted that encoding does not have to be done at the bit level, it can be done over a range of bits, such as a byte. Bit level encoding can usually be considered a modulation technique. Encoding over a range of bits is frequently referred to as symbolization.

Bit Coding and Receiver Bandwidth

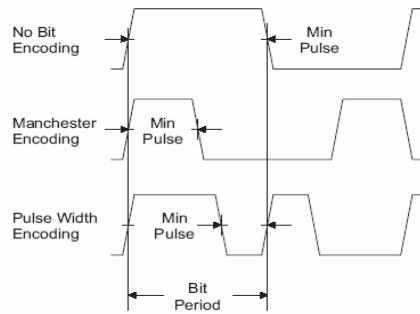


Figure 1.4.3.1

The performance of a radio system depends on how well the data encoding scheme conditions the signal for AC-coupling. The encoding scheme should achieve DC-balance, which means that the encoded signal has a "1" value 50% of the time, and a "0" value 50% of the time. The encoding scheme should also limit the run length, or for how many bit periods the encoded signal remains at a "1" (or a "0") value. *The run length determines the maximum pulse (or gap) width that can occur in the transmitted signal.*

As shown in Figure 1.4.3.2, the way the receiver processes the transmitted signal depends on the minimum and maximum width of the pulses or gaps in the signal, *not the underlying encoded data rate*.

Receiver Signal Processing

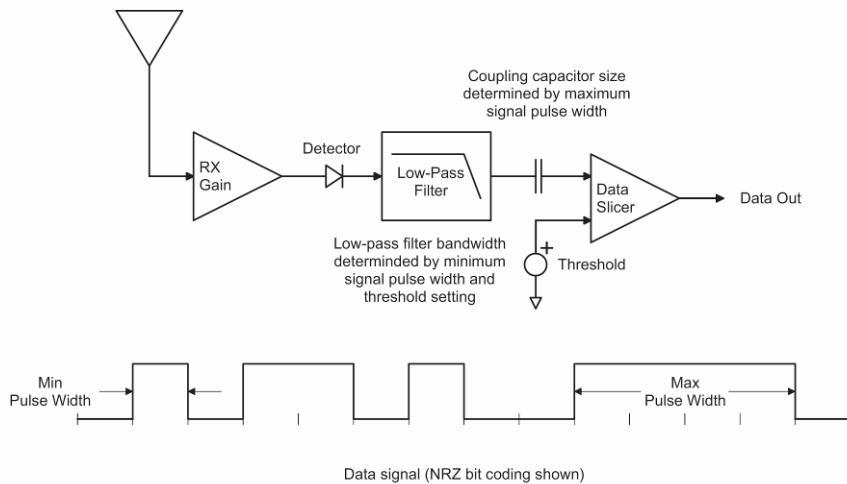


Figure 1.4.3.2

The ASH transceiver is AC-coupled between the receiver base-band output (Pin 5) and the comparator input (Pin 6). For this reason, the data bit stream being received should be encoded or modulated for good DC-balance, as explained above.

DC-balance can be accomplished a number of ways. Two of the most popular techniques for achieving DC-balance are Manchester encoding and symbol conversion. Manchester encoding is accomplished by encoding a “1” bit as a “1” + “0” signal pulse sequence, and encoding a “0” bit as a “0” + “1” pulse sequence. From another point of view, Manchester encoding is a form of BPSK modulation. This encoding scheme is very robust, but doubles the number of data bits that must be transmitted to send a message.

Another popular choice is byte to 12-bit symbol conversion, where each byte of a message is encoded as 12 bits, always with six “1” bits and six “0” bits. This encoding scheme is almost as robust as Manchester encoding, but only increases the number of data bits that must be transmitted to send a message by 50%. Refer to the program DC_BAL.BAS in the Appendix for an example of “byte to 12-bit conversion”. In this example, conversion is done by mapping between nibbles (4 bits) and 6-bit half-symbols, using a lookup table.

Closely related to the need for DC-balance is the need to limit the number of “1” pulses or “0” pulses that occur together (run length), or in high concentration, in the transmitted signal. Note that Manchester encoding does an excellent job, limiting the run length to just two encoded bits. Using the byte to 12-bit symbol conversion technique shown in the Appendix, the run length is limited to 4 bits, which is also satisfactory.

Scrambling algorithms are also used on occasion to encode transmitted data. The advantage of scrambling is that there is no increase in the number of bits transmitted to send a message.

Scrambling does ensure frequent bit transitions and average DC-balance. However, scrambling does not control run length and bit concentration very well. This limits its use as an encoding scheme to applications where data rate is more important than transmission range.

As mentioned above, the reason that data is encoded to provide DC-balance and to control bit concentration and run length is receiver performance. Data encoding provides for maximum noise rejection. DC-balance charges the capacitor between Pin 5 and Pin 6 on the ASH transceiver to a value that makes the comparator “slice” the signal at a voltage halfway between the average value for a “1” and a “0”. This means that the encoded data will be recovered error free so long as the noise level is less than one-half the voltage value between a “1” and a “0” pulse. When a received signal is unbalanced and a strong bias toward a “1” or a “0” value develops, noise rejection is severely reduced.

The value of the capacitor between Pin 5 and Pin 6 must be “tuned” for best receiver performance. It is desirable that this capacitor value not be too large, so that it quickly charges to the correct DC value for best noise performance when it starts receiving a transmission. On the other hand, it has to be large enough to pass the maximum signal run length without developing a strong bias in its slicing level. Thus, the optimum capacitor value depends on the message encoding scheme. Section 2.6.1 below discusses the specifics of selecting the base-band coupling capacitor for the ASH transceiver.

1.4.4 Packet communication protocols

All radio channels are subject to noise, interference and fading. In many cases, radio channels are shared by several users or services. Packet communication protocols are widely used to achieve error-free communications over imperfect and/or shared communication channels. Communication systems that use packet protocols include:

- The Internet
- Local area networks
- PC telephone modems
- Spread spectrum radios and wireless LANs
- Digital cellular phones and cellular modems (CDPD, etc.)
-

Almost all short-range wireless data communications use some form of packet protocol to automatically assure information is received correctly at the correct destination. A packet is a data structure that generally includes a training preamble, a start symbol, routing information (to/from, etc.) a packet ID, all or part of a message and error detection bits. Other information may be included depending on the protocol.

Figure 1.4.4.1 shows one of the packet formats used in Murata's Virtual Wire® Development Kits. The structure begins with a training preamble, which improves weak signal detection at the receiver by "training" the data slicer for best noise immunity, and providing signal transitions to train the clock recovery process. The training preamble usually consists of several bytes of a 1-0-1-0-1-0... sequence. The length of the preamble needed depends on the receiver base-band coupling time constant, t_{BBC} . The time constant, in turn, depends on the data coding scheme used, as discussed in section 1.4.3 above, and section 2.6.1 below. A typical preamble is three to four bytes long.

General Virtual Wire RF Link Packet Format

Preamble	Start Symbol	To Byte	From Byte	Packet Number	Size/Status Byte*	Message	FCS High Byte	FCS Low Byte
<p>↓ (0xE2E2)</p>								

General Virtual Wire Computer Link Packet Format

To Byte	From Byte	Packet Number	Size/Status Byte*	Message
---------	-----------	---------------	-------------------	---------

Figure 1.4.4.1

The preamble is followed by a start symbol (often called a start vector), which is a distinct pattern of bits marking the start of the information section of the packet. The longer the start symbol, the lower the probability that a random noise pattern will match the start symbol and trigger a false packet reception. A 12 to 16 bit start symbol provides reasonable discrimination.

Third-generation devices include clock recovery and an optional start symbol that can be implemented. This takes the burden away from the microprocessor and allows the processor to sleep until awakened by a clock signal from the device. This reduces overall current consumption. The start symbol is 0xE2E2 and is statistically determined not to randomly occur with a moderate receive threshold setting (THLD1). When using internal data and clock recovery, a THLD1 value of 20K is recommended to minimize start vector “nuisance tripping” due to random noise. Testing has shown that the start symbol will occur randomly on an average of every 30 sec with a threshold setting less than 20mV. When active, this function continuously tests for the 16-bit start symbol 0xE2E2 (hex). Data clocking begins in the middle of the first bit following the 16-bit start symbol, and clocking continues. Once all of the bits in the message are received, the host processor resets this function to end data clocking. After the message has been processed, the host processor re-enables the function again to enable detection of the next message. The register and bit settings that control this function are described in section 2.11 below.

The start symbol is followed by “to” and “from” address information. Murata uses 4 bit and 8 bit “to” and “from” addresses in its protocols. It is a common practice to reserve one address for broadcasting to all nodes in a packet system. If a very large number of unique addresses are needed, 48 or more address bits may be used. The packet (ID) number allows specific packets to be identified and their error-free reception to be acknowledged. The packet ID number also makes it possible to assemble a multi-packet message when the packets are received out of sequence. In the Murata protocol, the packet ID is followed by message size or status information.

The message or data payload then follows. The data payload length will vary with each application. The last two bytes of the packet comprise a 16 bit error checking code (frame check sequence), based on the X.25 packet standard (ISO 3309). The error checking code is recomputed at the destination to confirm error-free detection. The ISO 3309 frame check sequence provides very high confidence of error detection for packets up to 256 bytes in length.

In summary, Murata Virtual Wire® protocols provides the following features:

- 16-bit ISO 3309 error detection calculation to test message integrity
- To/from address routing with programmable node addresses
- ASCII or binary message support
- Automatic packet retransmission until an acknowledgment is received; up to 8 retries with semi-random back off plus “acknowledge” and “link failure” alarm messages.

Each byte transmitted by the radio is converted into a 12 bit, DC-balanced symbol. DC-balance promotes good noise immunity by keeping the data slicer threshold set half way between a “1” and “0” value. The DC-balanced symbols used have no more than 4 bits of the same value in a row. This limited “run length” allows the receiver data slicer to be tuned to recover quickly from a heavy noise burst or strong interfering signal.

Further information on data encoding and packet protocols, plus a discussion of software

techniques for clock and data recovery can be found in the ASH Transceiver Software Designer's Guide. The Software Guide includes tutorial source code examples. Also, no-cost source code licenses are available from Murata for several versions of the Virtual Wire® data link layer protocol. Contact Murata's application engineering group for additional information.

1.4.5 Noise control

Short-range wireless systems are especially sensitive to RF noise in the passband of the receiver, because the desired signals are transmitted at relatively low power levels. Commonly encountered internal noise sources include microcontrollers (for both control functions and data functions), brush-type motors and high-speed logic circuits. If the rise times and/or fall times of the clocking in a microcontroller are fast enough to produce harmonics in the frequency range of the receiver input and a harmonics fall directly within the passband of the receiver, special care must be taken to reduce the level of the harmonic at the antenna port of the receiver. If you have the option, choose a microprocessor with the slowest rise and fall time you can use for the application to minimize the generation of harmonics in the UHF band.

If possible, brush-type motors should be avoided in your application, since arcing of the brushes on the commutator makes a very effective spark-gap transmitter. If it is necessary to use a brush-type motor, spark suppression techniques must be used. Brush motors can often be purchased with spark suppression built-in. If the motor does not have built-in spark suppression, bypass capacitors, series resistors and shielding can be employed.

High-speed logic circuits produce noise similar to microprocessors. Once again, you should use logic with the slowest rise and fall times that will work in your application. The items listed below should be considered for an application that has one or more of the above noise sources included. It may not be possible to follow all of these guidelines in a particular application.

- Locate the RF transceiver and its antenna as far from the noise source as possible.
- If the transceiver must be enclosed with the noise source, locate the antenna remotely using a coaxial cable.
- Terminate high-speed logic circuits with their characteristic impedance and use microstrip interconnect lines designed for that impedance.
- Keep line lengths at a minimum that carry high-speed logic signals or supply brush-type motors. Such lines are antennas that radiate the unwanted noise.
- If possible, enclose the noise source in a grounded metal box and use RF decoupling on the input/output lines.
- Avoid using the same power lines for the RF transceiver and the noise source or at least thoroughly filter (RF decouple) the power lines. It is advisable to use separate voltage regulators, if possible.
- If the antenna cannot be remotely located, place it as far from the noise source as possible (on the opposite end of the PC board). Orient the antenna such that its axis is in the same plane with the PC board containing the noise source. Do not run

wires that supply the noise source in close proximity to the antenna.

Microcontroller clock frequency selection - you should check the computer or microcontroller clocks being used in your system to be sure they are not at or near a subharmonic of the receiver operating frequency. (For example, a 30.55 MHz clock would be the 30th subharmonic of 916.5 MHz.) It can be very difficult to suppress RF noise that is a harmonic of a clock being used in a digital system (especially odd harmonics). It is far better to chose a clock frequency that avoids this problem in the beginning.

Many microprocessors and microcontrollers “count down” the clock internally by factors such as 4, 8, 16, etc. If this is the case with the processor you are using, confirm that the “count down” frequency is also not at or near a subharmonic of your RF input frequency.

1.4.6 Regulatory certification

Worldwide, man-made electromagnetic (radio) emissions are controlled by international treaty and the ITU (International Telecommunications Union) committee recommendations. These treaties require countries within a geographical region to use comparable tables for channel allocations and emission limits, to assure that all users can operate with minimum levels of interference.

Recognizing a need to protect their limited frequency resources, most countries have additional local laws, regulations and government decrees for acceptable emission levels from various types of electronic equipment, both military and commercial. By requiring that each model of equipment be tested and an authorization permit issued after the payment of a fee, governmental bodies prevent the sale of poor quality equipment and also create a record of equipment manufacturers.

Technical regulations and enforcement criteria vary from location to location. The USA, Canada and most European countries have adopted ITU tables for their respective radio regions. Australia, Hong Kong and Japan also have extensive rules and regulations for short-range transmitters and receivers, but with significant differences in the tables for their geographic regions. Most other countries have a set of less formal regulations, often modeled on either USA or EU regulations.

Since third-generation devices are capable of +10 dBm peak output power, use of these devices in the USA in the 902-928 MHz band must conform to FCC 47 part 15.247 in order to use peak transmit power in excess of 50,000 µV/m or -1.25 dBm (+0.75 mW). The FCC rules for 15.247 state that frequency hopping or digital modulation must be employed in order to transmit up to 1 Watt of peak output power. The TR8100 is designed specifically for that purpose. The TR8100 device has digital modulation capability in order to meet the spectral requirements of FCC part 15.247. It is recommended to enable the digital modulation function at initial configuration and leave it enabled for operation at +10 dBm peak output power.

To operate third-generation devices under FCC 47 part 15.249, the peak output power must be decreased to 50,000 µV/m or -1.25 dBm (+0.75 mW). FCC part 15.249 allows peak transmit power up to 50,000 µV/m or -1.25 dBm (+0.75 mW). The TXMOD resistor is

used to control the peak output power of the device. Refer to the device data sheets to determine the correct value of the TXMOD resistor in order to conform third-generation devices to FCC 47 part 15.249.

In any country, it is important to contact the Ministry of Telecommunications or Postal Services to determine the local allocations, regulations and required certifications prior to marketing your product there. The mildest penalty is often total loss of your import, export and foreign exchange privileges.

These laws and requirements are applicable to a finished product in the configuration that it will be sold the general public or the end user. OEM components often can not be certified, since they require additional non-standard attachments before they have any functional purpose.

Unless otherwise marked, Murata modules (such as development kits) have not been certified to any particular set of regulations. Each module has suggested countries for use, depending on current allocations and technical limits.

Product certification - general requirements for emissions and ingestions (called electromagnetic susceptibility) are controlled by engineering standards of performance, regulations, and the customer's expectations.

In USA and Canada, for example, you must formally measure your product's emissions, file for and receive a certification or authorization, and affix a permanent marking label to every device prior to retail sale. Regulations allow you to build a small number of products (usually 5 pieces) for testing and in-company use before certification and marketing. Trade shows and product announcements can be a problem for marketing, when the products are advertised without proper disclaimers. With Internet access, go to "www.fcc.org" for USA information or "www.ic.gc.ca" for Canada. The Canadian rules are RCC-210, Revision 2. FCC CFR 47, Parts 2 and 15, contains the needed information for USA sales.

European Union (EU) requirements allow self-certification of some systems but require formal measurement reports for other systems. In all cases, however, the directives demand that a "CE mark" be added to all compliant devices before they can be freely shipped in commerce. In the EU, the EMC Directive also adds various tests and expectations for levels of signal that will permit acceptable operation.

In April of 2000, the Radio Equipment and Telecommunications Terminal Equipment (R&TTE) Directive was issued that greatly simplifies short-range radio certification requirements in Europe. The R&TTE requires manufacturers to take full responsibility for the conformance of their equipment, but it also greatly streamlines the certification process.

A good general discussion of the introduction of the R&TTE Directive is available on the web site of the UK Radiocommunications Agency. The link to this discussion is:

<http://www.radio.gov.uk/document/misc/rtte/rtteman/rtteman.htm>

Additional information can be found on the European Radiocommunications Office (ERO) web site at:

<http://www.ero.dk>

Murata recommends you check these sites frequently as some additional changes to the ETSI short-range device specifications and EMC specifications are expected in the near future.

Certification testing

The emissions are measured in a calibrated environment defined by the regulations. USA and Canada use an “open field” range with 3 meters between the device under test (DUT) and the antenna. The range is calibrated by measurement of known signal sources to generate range attenuation (correction) curves in accordance with ANSI C63.4-1992.

EU measurement rules are based on a similar arrangement, but a “standard dipole” antenna is substituted for the DUT to calibrate the range attenuation. Since the EU measurements are comparison or substitution rules, they are often easier to follow for informal pre-testing by the designer. ETSI-300-220 has drawings to completely describe a typical test configuration.

The USA and Canadian requirements are contained in ANSI C63.4-1992, including a step-by-step test calibration and measurement procedure. Since these rules include range attenuation factors, one must make twice the measurements of the EU test method. Other countries follow one of these two techniques, with exception for a 10 meter range (separation) measurement or a different group of test frequencies.

Each of the listed contacts will have resources to provide current regulations and certification forms. They can also suggest sources for your formal tests, either commercial labs or the government testing office. Unless you want to invest in a qualified radiated signals test range, the commercial labs can help you with preliminary measurements and some expertise in correcting any difficulties that are noted. Contacts for further information and current test facilities listings:

ANSI
Institute of Electrical & Electronics Engineers,
345 East 47th Street, New York, NY 10017 USA
<http://www.ansi.org>

ETSI
European Telecommunications Standard Institute
F-06921 Sophia Antipolis Cedex FRANCE
<http://www.etsi.fr>

FCC
Federal Communications Commission
Washington DC 20554 USA
<http://www.fcc.gov>

Canada DOC
Industrie Canada
Attn: Certification, Engineering and Operations Section,
1241 Clyde Avenue, Ottawa K1A 0C8 CANADA
<http://info.ic.gc.ca>

UNITED KINGDOM
Radiocommunications Agency
Waterloo Bridge House, Waterloo Road
London SE1 8UA
<http://www.open.gov.uk/radiocom>

JATE
Japan Approvals Institute (JATE)
Isomura Bldg, 1-1-3 Toranomon
Minato-ku Tokyo JAPAN
<http://www.mpt.go.jp>
Please refer to Murata's web site at <http://www.murata.com> for additional information on regulatory agencies.

2.0 Third-Generation ASH Transceiver Set-Up

2.1 Theory of Operation

The third-generation ASH transceiver's unique feature set is made possible by its system architecture. The heart of the transceiver is the amplifier-sequenced receiver section, which provides more than 100 dB of stable RF and detector gain without any special shielding or decoupling provisions. Stability is achieved by distributing the total RF gain over time. This is in contrast to a superheterodyne receiver, which achieves stability by distributing total RF gain over multiple frequencies.

Figure 2.1.1 shows the basic block diagram and timing cycle for an amplifier-sequenced transceiver. Note that the bias to RF amplifiers RFA1 and RFA2 are independently controlled by a pulse generator, and that the two amplifiers are coupled by a surface acoustic wave (SAW) delay line, which has a typical delay of 0.5 μ s.

ASH Receiver Block Diagram & Timing Cycle

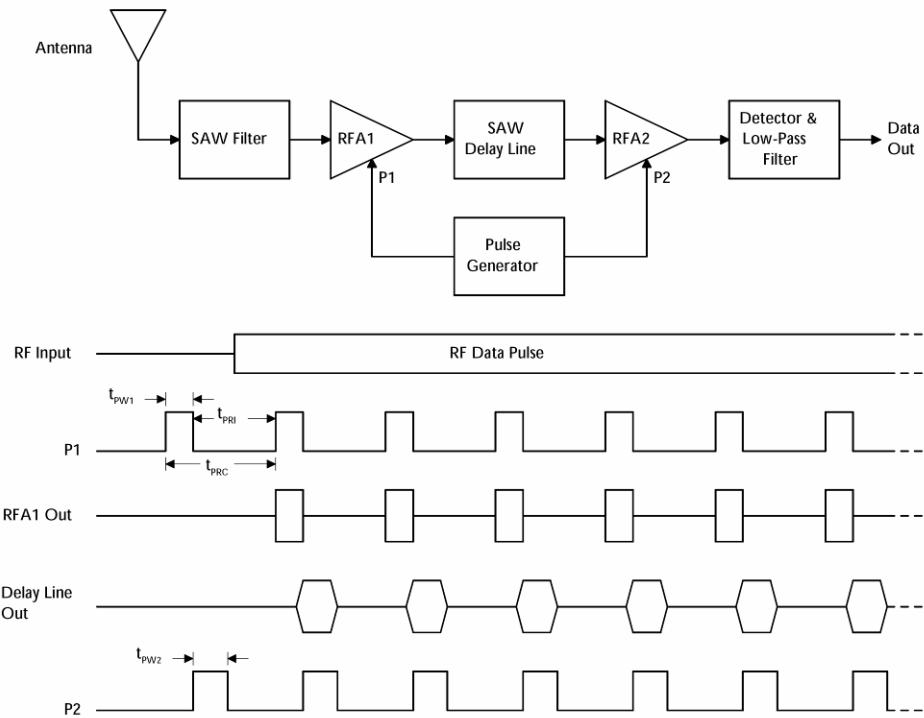


Figure 2.1.1

An incoming RF signal is first filtered by a narrow-band SAW filter, and is then applied to RFA1. The pulse generator turns RFA1 ON for $0.814 \mu s$. The amplified signal from RFA1 emerges from the SAW delay line at the input to RFA2. RFA1 is now switched OFF and RFA2 is switched ON for $0.814 \mu s$, amplifying the RF signal further. As shown in the timing diagram, RFA1 and RFA2 are never on at the same time, assuring excellent receiver stability. Note that the narrow-band SAW filter eliminates sampling sideband responses outside of the receiver passband, and the SAW filter and delay line act together to provide very high receiver ultimate rejection.

Amplifier-sequenced receiver operation has several interesting characteristics that can be exploited in system design. The RF amplifiers in an amplifier-sequenced receiver can be turned on and off almost instantly, allowing for very quick power-down (sleep) and wake-up times. Also, both RF amplifiers can be off between ON sequences to trade-off receiver noise figure for lower average current consumption. The effect on noise figure can be modeled as if RFA1 is on continuously, with an attenuator placed in front of it with a loss equivalent to $10 * \log_{10}(\text{RFA1 duty factor})$, where the duty factor is the average amount of time RFA1 is ON (up to 50%). Since an amplifier-sequenced receiver is inherently a sampling receiver, the overall cycle time between the start of one RFA1 ON sequence and the start of the next RFA1 ON sequence should be set to sample the narrowest RF data pulse at least 10 times. Otherwise, significant edge jitter will be added to the detected data pulse.

Figure 2.1.3 is the overall block diagram of the third-generation ASH transceiver, and Figure 2.1.2 is the pin-out diagram. Please refer to these figures for the following discussions.

3G Transceiver Pin Out

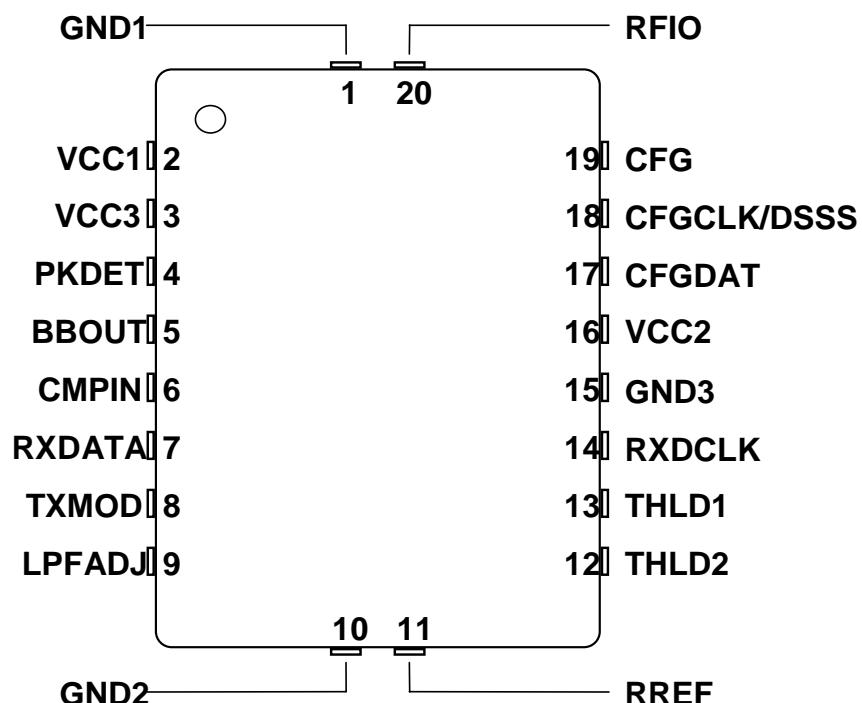


Figure 2.1.2

3G ASH Transceiver Block Diagram

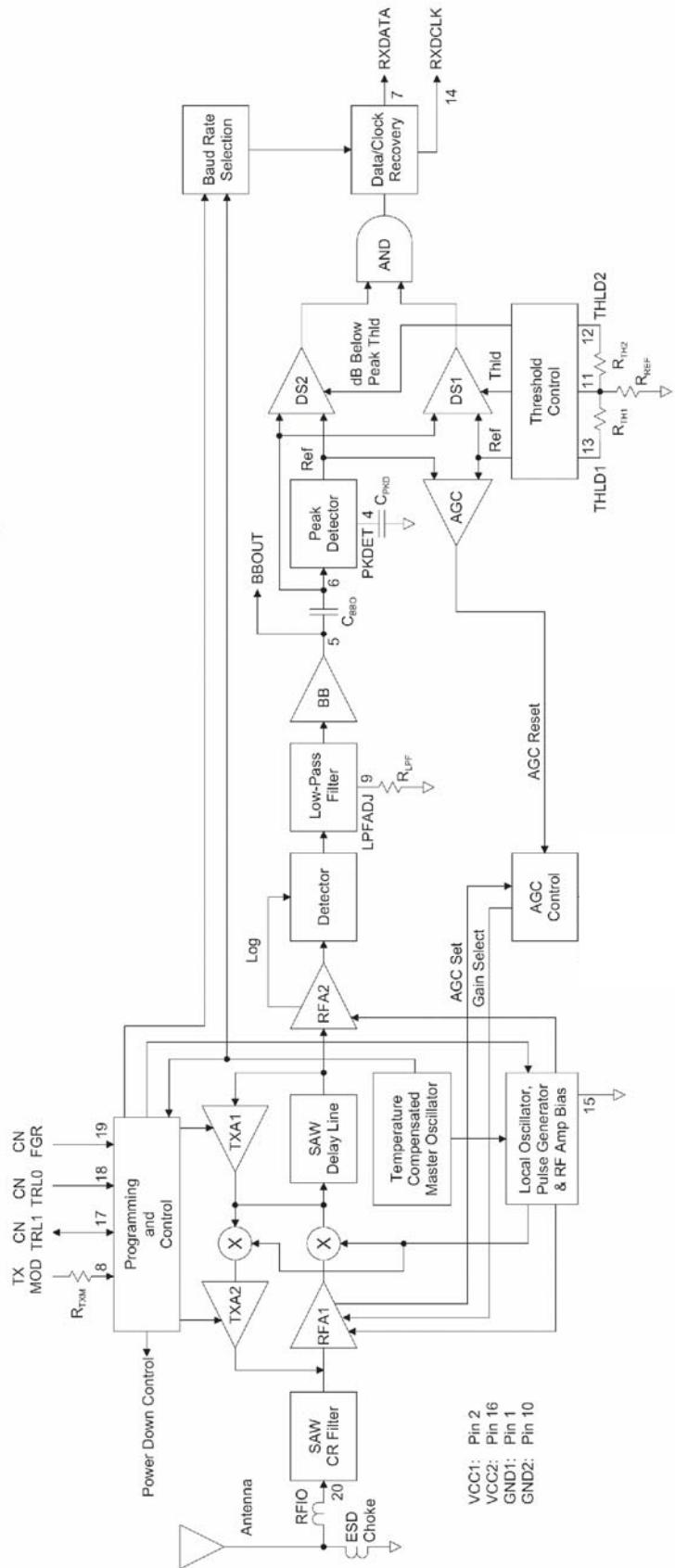


Figure 2.1.3

Antenna port - The only external RF components needed for the transceiver are the antenna and its matching components. Antennas presenting an impedance in the range of 35 to 72 ohms resistive can be satisfactorily matched to the RFIO pin with a series matching coil and a shunt matching/ESD protection coil. Other antenna impedances can be matched using two or three components. For some impedances, two inductors and a capacitor will be required. A DC path from RFIO to ground is required for ESD protection.

Receiver chain - the SAW RF filter has a nominal insertion loss of 3.5 dB, a 3 dB bandwidth of 600 kHz, and an ultimate rejection of 55 dB. The output of the SAW filter drives amplifier RFA1. This amplifier includes provisions for detecting the onset of saturation (AGC Set), and for switching between 35 dB of gain and 5 dB of gain (Gain Select). AGC Set is an input to the AGC Control function, and Gain Select is the AGC Control function output. ON/OFF control to RFA1 (and RFA2) is generated by the Pulse Generator & RF Amp Bias function. The output of RFA1 drives the low-loss SAW delay line, which has a nominal delay of 0.5 μ s, an insertion loss of 6 dB, and an ultimate rejection of 50 dB. Note that the combined out-of-band rejection of the SAW RF filter and SAW delay line provides excellent receiver ultimate rejection.

The second amplifier, RFA2, provides 51 dB of gain below saturation. The output of RFA2 drives a square law detector with 19 dB of threshold gain. The onset of saturation in each section of RFA2 is detected and summed to provide a logarithmic response. This is added to the output of the square law detector to produce an overall detector response that transitions into a log response for high signal levels. This combination provides excellent threshold sensitivity and more than 70 dB of detector dynamic range. In combination with the 30 dB of AGC range in RFA1, more than 100 dB of receiver dynamic range is achieved.

The detector output drives a gyrator filter. The filter provides a three-pole, 0.05 degree equiripple low-pass response with excellent group delay flatness and minimal pulse ringing. The 3 dB bandwidth of the filter can be set from 4.5 kHz to 1.8 MHz with an external resistor.

The filter is followed by a base-band amplifier which boosts the detected signal to the BBOUT pin. The BBOUT signal changes about 10 mV/dB, with a peak-to-peak signal level of up to 450mV. The detected signal is riding on a 1.5 Vdc level that varies somewhat with supply voltage, temperature, etc. BBOUT is coupled to the CMPIN pin or to an external data recovery process (DSP, etc.) by a series capacitor.

When an external data recovery process is used with AGC, BBOUT must be coupled to the external data recovery process and CMPIN by separate series coupling capacitors. The AGC reset function is driven by the signal applied to CMPIN.

Data Slicers - The CMPIN pin drives two data slicers, which convert the analog signal from BBOUT back into a digital stream. The best data slicer choice depends on the system operating parameters. Data slicer DS1 is a capacitor-coupled comparator with provisions for an adjustable threshold. DS1 provides the best performance at low signal-to-noise conditions. The threshold, or squelch, offsets the comparator's slicing level from

0 to 90 mV, and is set with a resistor between the RREF and THLD1 pins. This threshold allows a trade-off between receiver sensitivity and output noise density in the no-signal condition. For best sensitivity, the threshold should be set to zero, however, 9mV minimum should be used for proper AGC operation. In this case, noise is output continuously when no signal is present. This, in turn, requires the circuit being driven by the RXDATA pin to be able to process noise (and signals) continuously. This can be a problem if RXDATA is driving a circuit that must sleep when data is not present to conserve power, or when it is necessary to minimize false interrupts to a multitasking processor. In this case, noise can be greatly reduced by increasing the threshold level, but at the expense of sensitivity. The best 3 dB bandwidth for the low-pass filter is also affected by the threshold level setting of DS1. The bandwidth must be increased as the threshold is increased to minimize data pulse-width variations with signal amplitude.

DS2 is a “dB-below-peak” slicer. The peak detector charges rapidly to the peak value of each data pulse, and decays slowly in between data pulses (1:1000 ratio). The DS2 slicer trip point can be set from 0 to 120 mV below this peak value with a resistor between RREF and THLD2.

DS2 is best for ASK modulation where the transmitted waveform has been shaped to minimize signal bandwidth. However, DS2 can be temporarily “blinded” by strong noise pulses, which causes burst data errors. Note that DS1 is active when DS2 is used, as RXDATA is the logical AND of the DS1 and DS2 outputs. DS2 can be disabled by leaving THLD2 disconnected. Note that a non-zero DS1 threshold is required for proper AGC operation.

Data and Clock Recovery – RXDATA is the receiver data output pin. The signal on this pin can come from one of two sources. The default source is directly from the output of the compound data slicer circuit. The alternate source is from the radio’s internal data and clock recovery circuit. When the internal data and clock recovery circuit is used (CFG0, Bit 0 ‘high’), the signal on RXDATA is switched from the output of the data slicer to the output of the data and clock recovery circuit when a packet start symbol is detected.

When the radio’s internal data and clock recovery circuit is not used, RXDCLK is a steady low value. When the internal data and clock recovery is used, RXDCLK is low until a start symbol is detected at the output of the data slicer. Each bit following the start symbol is output at RXDATA on the rising edge of a RXDCLK pulse, and is stable for reading on the falling edge of the RXDCLK pulse. Once RXDCLK is activated by the detection of a start symbol, it remains active until CFG0 Bit 0 is reset low. Normally RXDCLK is reset by the host processor as soon as a packet is received.

AGC Control - The output of the Peak Detector also provides an AGC Reset signal to the AGC Control function through the AGC comparator. The purpose of the AGC function is to extend the dynamic range of the receiver, so that two transceivers can operate close together when running ASK and/or high data rate modulation. The AGC also prevents receiver saturation by a strong in-band interfering signal, allowing operation to continue at short range in the presence of the interference. The onset of saturation in the output stage of RFA1 is detected and generates the AGC Set signal to the AGC Control function. The

AGC Control function then selects the 5 dB gain mode for RFA1. The AGC Comparator will send a reset signal when the Peak Detector output (multiplied by 0.8) falls below the threshold voltage for DS1 (note that the DS1 threshold must be greater than zero for correct AGC operation), thus, the peak detector is required to be functioning for proper AGC reset action.

An AGC capacitor is not needed for third-generation ASH devices. There is provided enough delay within the device to mitigate AGC “chattering” during the time it takes for the signal to propagate through the low-pass filter and charge the peak detector. Pin 3 on third-generation devices is a VCC pin (see Figure 2.1.2).

Receiver pulse generator and RF amplifier bias - The receiver amplifier-sequenced operation is controlled by the Pulse Generator & RF Amplifier Bias module. The receiver RF amplifiers operate at a 50%-50% duty cycle of 614kHz. Both receiver RF amplifiers are turned off by the Power Down Control Signal, which is invoked in the Sleep and transmit modes.

Transmitter chain - The transmitter is capable of generating +10dBm of output power. The transmitter chain consists of a SAW delay line oscillator, followed by an OOK/ASK modulated buffer amplifier. The SAW filter suppresses transmitter harmonics to the antenna. Note that the same SAW devices used in the amplifier sequenced receiver are reused in the transmit modes. Transmitter operation supports two modulation formats, on-off keyed (OOK) modulation, and amplitude-shift keyed (ASK) modulation. When OOK modulation is chosen, the transmitter output turns completely off between “1” data pulses. When ASK modulation is chosen, a “1” pulse is represented by a higher transmitted power level, and a “0” is represented by a lower transmitted power level. OOK modulation provides compatibility with second and third generation ASH technology, and provides for power conservation. ASK modulation must be used for high data rates (data pulses less than 30 μ s). ASK modulation also reduces the effects of some types of interference and allows the transmitted pulses to be shaped to control modulation bandwidth. Some devices, such as the TR8100, have the capability of providing a digitally modulated, spread spectrum output. This allows the user to output 10mW and meet FCC regulations in the 902-928MHz ISM band.

The modulation format is chosen by the state of bit 5 of the CFG0 configuration word. Refer to section 2.11 for a detailed discussion of the control and configuration registers. When either modulation format is chosen, the receiver RF amplifiers are turned off. In the OOK mode, the delay line oscillator amplifier TXA1 and the output buffer amplifier TXA2 are turned off when the voltage to the TXMOD input falls below 220 mV. In the OOK mode, the data rate is limited by the turn-on and turn-off times of the delay line oscillator, which are 12 and 6 μ s respectively. In the ASK mode TXA1 is biased ON continuously, and the output of TXA2 is modulated by the TXMOD input current. Minimum output power occurs in the ASK mode when the modulation driver sinks about 10 μ A of current from the TXMOD pin. The transmitter RF output power is proportional to the input current to the TXMOD pin. A resistor in series with the TXMOD pin is used to adjust the peak transmitter output power. 10 mW of output power requires about 315 μ A of input current.

Transceiver operating modes – Transmitter operation supports two modulation formats, on-off keyed (OOK) modulation, and amplitude-shift keyed (ASK) modulation. These are configured by three pins: Pin 17 (CFGDAT), Pin 18 (CFGCLK), and Pin 19 (CFG). When DC power is applied to the device with Pin 19 held low, the functions of Pins 17 and 18 default to the “2G ASH” definition. This allows the device to be used with existing second-generation ASH PCB layouts and protocol software. Note that for default 2G operation, Pin 15 is grounded (zero ohm resistor) and Pin 14 is left unconnected.

When Pin 19 is first set to a logic 1 after DC power is applied, the functionality of Pins 17 and 18 change from the 2G control mode to the third-generation serial control mode. This change persists until a power reset. After serial control is invoked, Pins 17, 18 and 19 are used to write data to and read from three 8-bit configuration control registers in the radio. To begin a write or read sequence, Pin 19 is set to logic 1. Data is then clocked into or out of Pin 17 on the rising edge of each clock pulse applied to Pin 18. Configuration data clocked into Pin 17 is transferred to a control register every eight bits. Bits clocked into Pin 17 when Pin 19 is a logic 0 are ignored. Also, if Pin 19 is reset to logic 0 before a complete group of eight data bits is received, the incomplete group is ignored.

If a power output of 10mW is desired in the 902-928MHz ISM band, a device, such as the TR8100, must be used in the “Digital Modulation” (ISS) mode. To do this it is necessary to change the power-on default values of several bits in CFG0 and CFG1 registers before the transceiver will comply with FCC 15.247 regulations. The advantage of the FCC 15.247 “digital modulation” rules is that the device can transmit its full rated RF power. See section 2.9.4 for a detailed description of “Digital Modulation” (ISS Mode).

2.2 Power Supply Requirements

As shown in Figure 2.1.2, pin 2 is the supply voltage pin for the transmit output amplifier. Pin 3 is the supply voltage pin for the receiver baseband circuitry and the transmit oscillator. Pin 2 is usually connected to the positive supply through a ferrite RF decoupling bead which is bypassed by an RF capacitor on the *supply side*. Pin 3 may be connected directly to VCC at the bypass capacitor. The ferrite bead eliminates the possibility of RF feedback from the antenna to Pin 2 and should be used, except for specific (300 - 400 MHz) “EMI robust” layouts. VCC2 (Pin 16) is the positive supply voltage pin for the receiver and transmitter RF sections and the digital baseband circuitry. Pin 16 must be bypassed with an RF capacitor, and must also be bypassed with a 1 to 10 μ F tantalum or electrolytic capacitor. The power supply voltage range for standard operation is characterized from 2.2 to 3.7 Vdc. **Power supply ripple must be less than 10 mV peak-to-peak.**

2.2.1. Low voltage set-up

Third-generation ASH radios were characterized for operation from 2.2 to 3.7 Vdc over the temperature range of -40 to +85 °C in 2006 (see section 3.8 in the Appendix). Where transmitter output power stability is important over this extended voltage range, the TXMOD input (Pin 8) should be driven from a true current source rather than a voltage source through a relatively large resistor. When using a current source, an RF isolation

resistor of at least 220 ohms should be used between Pin 8 and the current source.

2.3 RF Input/Output

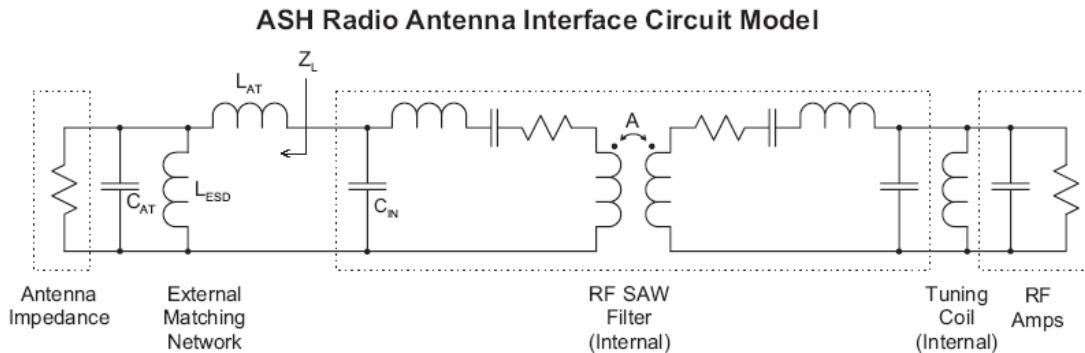


Figure 2.3.1

Pin 20 (RFIO) is the RF input/output pin. This pin is connected directly to the input transducer of a high-Q quartz SAW filter, as shown in Figure 2.3.1. The antenna impedance must be transformed by a matching network to present a specific impedance Z_L to the SAW filter for proper operation. *Connecting Pin 20 directly to a 50 ohm antenna will result in poor performance.*

2.3.1 Antenna matching

Referring to Figure 2.3.1 again, the RF SAW filter can be modeled as a two-pole band-pass filter with acoustic coupling between the two sections of the filter. The right section of the filter is internally matched to the receiver input amplifier and transmitter power amplifier by a shunt tuning coil. When the proper impedance Z_L is presented to the left side of the filter, the correct RF filter response, receiver match for low noise figure, transmitter output match, and other RF parameters are automatically achieved.

Transforming a 50 ohm antenna impedance to the correct Z_L for an third-generation ASH radio can usually be accomplished using a series chip inductor and a shunt chip inductor on the antenna side. The values for these impedance matching components are listed in Table 2.3.1.1. However, many applications will involve interfacing an ASH radio to an antenna whose impedance is not 50 ohms. To accomplish this task, first measure the input impedance of the antenna using a network analyzer. Next, determine the matching network to transform the antenna impedance to 50 ohms. Cascade this antenna matching network with the impedance transformation network from Table 2.3.1.1 to get the overall matching network. Finally, combine component values where possible to simplify the overall matching network.

Let's consider an example. Assume we are working with a monopole antenna, either a simple length of wire or a copper trace on a PC board. If the length of the antenna is less than one-fourth of a wavelength at the frequency of interest, the network analyzer will in-

d dictate that the impedance is of the form, $R - jX$, or that the impedance is equivalent to a resistor in series with a capacitor. This antenna can be matched by using a series inductor whose reactance is equal to the reactance X of the capacitor. This results in a matched antenna impedance of R . For such an antenna, the value of R is usually some where between 35 and 72 ohms. This is close enough to 50 ohms to avoid significant impedance mismatch loss. Once the antenna matching inductance value has been determined, the overall matching network is developed by combining the antenna matching inductance value with the matching component values listed in Table 2.3.1.1. In most cases, this allows using two chip inductors to transform the antenna impedance to the required Z_L .

Table 2.3.1.1

Third-Generation ASH Radio Matching Component Values for a 50 ohm Antenna						
Part Number	Frequency	L_{AT}^*	L_{ESD}	C_{AT}	$R + jX$	Y_L
	MHz	nH	nH	pF	Ohms (Ω)	mho (Ω^{-1})
TR8100	916.50	15	100	-	43 - j21	.0188 +j0.0092
TR8000	916.50	15	100	-	43 - j21	.0188 +j0.0092
TR8001	868.35	10	100	-	30.5 - j12.3	.0282 + j0.0114
TR7000	433.92	56	220	-	40 + j7.66	.0241 - j0.0046

* Q of at least 50

Another example is matching a monopole antenna whose length is greater than $\frac{1}{4}$ of a wavelength. The impedance of such an antenna will be of the form $R + jX$, indicating that the impedance is equivalent to a resistor in series with an inductor. This antenna can be matched by using a series capacitor whose reactance is equal to the reactance X of the inductor, resulting in a matched antenna impedance of R . Once again, the value of R will usually be close enough to 50 ohms to avoid significant mismatch loss. The negative reactance of this matching capacitor can then be combined with the reactance of the matching components listed in Table 2.3.1.1 to obtain the reactance of the matching components that will match the antenna to the ASH radio. Of course, if the resulting reactance is negative, the matching components will include a capacitor rather than an inductor.

For more information (plus examples) on developing matching networks starting with the component values for matching an ASH radio to a 50 ohm antenna, see the *ASH Transceiver Antenna Impedance Matching* paper in the application notes section of Murata's website at www.murata.com.

Table 2.3.1.1 also lists the Z_L impedance values and corresponding Y_L admittance values for all standard third-generation ASH radios. These values can be transferred directly to a Smith Chart or RF CAD package to support the design and evaluation of various antenna matching network topologies. Note that it is desirable to use a matching network topology that includes a series inductor L_{AT} in the matching network. L_{AT} and the RF SAW filter input capacitance C_{IN} (Figure 2.3.1) form a low-pass filter above the operating frequency of the ASH radio, providing additional high-side signal rejection. Also, a shunt inductor across the antenna must be present in the matching network for ESD protection, as

discussed in section 2.3.2 below.

2.3.2 ESD protection

The SAW input transducer (Pin 20) is static sensitive and must be protected by a shunt RF choke to GND1 (Pin 1). The ESD choke may also function as part of the antenna tuning network as shown in Table 2.3.1.1. To provide further ESD protection, externally mounted antennas should have an insulating jacket. The ESD choke should have a very low series resistance (less than 0.1 ohm) to be fully effective.

2.4 Pulse Generator

2.4.1 Fixed Sequence

Third-generation ASH devices use an internal 50% duty cycle Pulse Generator signal to sequence the receive RF amplifiers, as opposed to the variable sequencing available with second-generation devices.

The receiver amplifier-sequence operation is controlled by the Pulse Generator & RF Amplifier Bias module and the Sleep Control Signal from the Modulation & Bias Control function. The Pulse Generator runs a 50%-50% duty cycle at 614kHz. RFA1 is on for .814 μ s and RFA2 is off, then RFA2 is on for .814 μ s and RFA1 is off. The pulse rate is sufficient to provide ample oversampling of data up to 115kbps. Both receiver RF amplifiers are turned off by the Sleep Control Signal, which is invoked in the Sleep and transmit modes.

2.5 Low-Pass Filter

The low-pass filter used in the third-generation ASH transceiver is a three-pole, 0.05 degree equiripple design which features excellent group delay flatness and minimal pulse ringing.

2.5.1 3 dB bandwidth adjustment

Pin 9 is the receiver low-pass filter bandwidth adjust. The filter bandwidth is set by a resistor R_{LPF} between this pin and ground. The resistor value can range from 510 kilohms to 820 ohms, providing a filter 3 dB bandwidth f_{LPF} from 4.5 kHz to 1.8 MHz. The resistor value is determined by:

$$R_{LPF} = (.0006 * f_{LPF})^{-1.069} \text{ where } R_{LPF} \text{ is in kilohms, and } f_{LPF} \text{ is in kHz}$$

A $\pm 5\%$ resistor should be used to set the filter bandwidth. This will provide a 3 dB filter bandwidth between f_{LPF} and $1.3 * f_{LPF}$ with variations in supply voltage, temperature, etc. R_{LPF} cannot be larger than 510 kilohms (4.5 kHz bandwidth). For low data rate operation a simple external R-C filter can be added at Pin 5 to further improve receiver sensitivity. See Figure 4.2 in the ASH Transceiver Software Designer's Guide for additional details.

2.5.2 Bandwidth selection

When using data slicer DS2 or data slicer DS1 with no threshold, the recommended 3 dB bandwidth of the filter for DC-balanced data (12-bit symbol or Manchester encoding) is:

$$f_{LPF} = 750/SP_{MIN}, \text{ where } f_{LPF} \text{ is in kHz and minimum signal pulse width } SP_{MIN} \text{ is in } \mu\text{s}$$

The recommended 3 dB bandwidth when using DS1 (only) with a mild threshold is:

$$f_{LPF} = 1000/SP_{MIN}$$

The recommended 3 dB bandwidth when using DS1 (only) with a strong threshold is:

$$f_{LPF} = 2500/SP_{MIN}$$

2.6 Base-Band Coupling

Pin 5 is the receiver base-band output pin (BBOUT). This pin drives the CMPIN (Pin 6) through coupling capacitor C_{BBO} for internal data slicer operation. The time constant t_{BBC} for this connection is:

$$t_{BBC} = 0.1 * C_{BBO}, \text{ where } t_{BBC} \text{ is in } \mu\text{s and } C_{BBO} \text{ is in pF}$$

A $\pm 10\%$ ceramic capacitor should be used between BBOUT and CMPIN. The time constant can vary between t_{BBC} and $1.8 * t_{BBC}$ with variations in supply voltage, temperature, etc. The optimum time constant in a given circumstance will depend on the data rate, data run length, and other factors as discussed in section 2.6.1 below.

The minimum value of C_{BBO} that will work with the data stream should be used to minimize the receiver recovery time after power-down or transmit.

2.6.1 Base-band coupling capacitor selection

The correct value of the base-band coupling capacitor depends on the maximum pulse width (or gap) that can occur in the signal. The maximum pulse width, in turn, depends on the data stream encoding, the data rate, and the maximum run length that occurs in the data. If no data stream encoding is used, the maximum pulse width is equal to a bit period multiplied by the maximum run length. If byte to 12-bit symbol encoding is used, the maximum pulse width is four encoded bit periods. For Manchester encoding, the maximum pulse width is two encoded bit periods.

Time constant t_{BBC} should be chosen so that the signal “droops” no more than 50% during a maximum pulse width event, or:

$$t_{BBC} = 1.12 * SP_{MAX}, \text{ where } t_{BBC} \text{ and maximum signal pulse width } SP_{MAX} \text{ are in } \mu\text{s}$$

$$C_{BBO} = 10 * t_{BBC}, \text{ where } t_{BBC} \text{ is in } \mu\text{s and } C_{BBO} \text{ is in pF, or}$$

$$C_{BBO} = 11.2 * SP_{MAX}, \text{ where } SP_{MAX} \text{ is in } \mu\text{s and } C_{BBO} \text{ is in pF}$$

It takes a packet training preamble equal to 1.6 times t_{BBC} to train C_{BBO} to a voltage of 80% of its optimum slicing value. Using Manchester encoding, this equates to nominally two AA hex bytes. Using byte to 12-bit symbolization, this equates to four AA hex bytes. Attempting to transmit data with an SP_{MAX} of 16 bits or more requires an impractically long training preamble. This is one reason that data encoding is important.

2.6.2 Base-band output signal levels

BBOUT can also be used to drive an external data recovery process (DSP, etc.) with the receiver RF amplifiers operating at a 50%-50% duty cycle. The BBOUT signal changes about 10 mV/dB, with a peak-to-peak signal level of up to 450 mV. The detected signal is riding on a 1.5 Vdc level that varies somewhat with supply voltage, temperature, etc. BBOUT is coupled to the CMPIN pin or to an external data recovery process by a series capacitor. The nominal output impedance of this pin is 1 K. A load impedance of 50 K to 500 K in parallel with no more than 10 pF is recommended.

When an external data recovery process is used with AGC, BBOUT must be coupled to the external data recovery process and CMPIN by separate series coupling capacitors. The AGC reset function is derived from the Peak Detector Circuit which is driven by the signal applied to CMPIN (Pin 6).

2.7 Data Slicers

CMPIN (Pin 6) drives two data slicers, which convert the analog signal from BBOUT back into a digital stream. The best data slicer choice depends on the system operating parameters. Data slicer DS1 is a capacitor-coupled comparator with provisions for an adjustable threshold. DS1 provides the best performance at low signal-to-noise conditions. The threshold, or squelch, offsets the comparator's slicing level from 0 to 90 mV, and is set with a resistor between the RREF and THLD1 pins. This threshold allows a trade-off between receiver sensitivity and output noise density in the no-signal condition. For best sensitivity, the threshold is set to 0. In this case, noise is output continuously when no signal is present. This, in turn, requires the circuit being driven by the RXDATA pin to be able to process noise (and signals) continuously.

This can be a problem if RXDATA is driving a circuit that must "sleep" when data is not present to conserve power, or when it is necessary to minimize false interrupts to a multitasking processor. In this case, noise can be greatly reduced by increasing the threshold level, but at the expense of sensitivity. A threshold of 50 mV provides a good trade-off between excessive false interrupts and excessive loss of sensitivity for a filter bandwidth of 48 kHz (19.2 kbps NRZ data rate). If you are using a different filter bandwidth, start with a threshold value of:

$$V = 7.2 * (f_{LPF})^{1/2} \text{ where } V \text{ is in mV and } f_{LPF} \text{ is in kHz}$$

Thresholds of 60 to 90 mV may be required to suppress hash from some computers. Note

that the best 3 dB bandwidth for the low-pass filter is affected by the threshold level setting of DS1, as discussed in section 2.5.2. Also, note that the AGC reset operation requires a non-zero threshold on DS1.

DS2 is a “dB-below-peak” slicer. The peak detector charges rapidly to the peak value of each data pulse, and decays slowly in between data pulses (1:1000 ratio). The DS2 slicer trip point can be set from 0 to 120 mV below this peak value with a resistor between RREF and THLD2. A threshold of 60 mV is the most common setting, which equates to “6 dB below peak”. Slicing at the “6 dB-below-peak” point reduces the signal amplitude to data pulse-width variation allowing shaping of the transmitted waveform to minimize signal bandwidth, thus, DS2 is used with high data rate ASK modulation and/or to reject weak interference. However, DS2 can be temporarily “blinded” by strong noise pulses, which causes burst data errors. Note that DS1 is active when DS2 is used, as RXDATA is the logical AND of the DS1 and DS2 outputs. When DS2 is used, the DS1 threshold is usually set to less than 60 mV (25 mV typical). DS2 is disabled by leaving THLD2 disconnected. Figure 2.6.1 shows the data slicer threshold levels with reference to a DC-balanced signal.

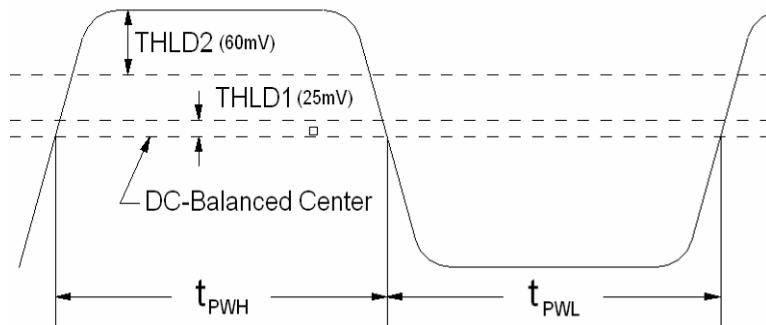


Figure 2.6.1

2.7.1 Data slicer 1 threshold selection (THLD1)

RREF is the external reference resistor pin. A 100 K reference resistor is connected between this pin and ground. A $\pm 1\%$ resistor tolerance is recommended. It is important to keep the total capacitance between ground, Vcc and this node to less than 5 pF to maintain current source stability. If THLD1 and/or THLD2 are connected to RREF through resistor values less than 1.5 K, their node capacitance must be added to the RREF node capacitance and the total should not exceed 5 pF.

The THLD1 pin sets the threshold for the standard data slicer through a resistor R_{TH1} to RREF. The threshold is increased by increasing the value of the resistor. Connecting this pin directly to RREF provides zero threshold. R_{TH1} is given by:

$$R_{TH1} = 1.11 * V, \text{ where } R_{TH1} \text{ is in kilohms and the threshold } V \text{ is in mV}$$

For the case that THLD2 is used, the acceptable range for the THLD1 resistor is 0 to 200 K, again providing a THLD1 range of 0 to 90 mV. The resistor value is given by:

$R_{TH1} = 2.22*V$, where R_{TH1} is in kilohms and the threshold V is in mV

A $\pm 1\%$ resistor tolerance is recommended for the THLD1 resistor.

2.7.2 Data slicer 2 threshold selection (THLD2)

The operation of data slicer 2 and the AGC depend on the peak detector circuit. Pin 4 controls the peak detector operation. A capacitor between this pin and ground sets the peak detector attack and decay times, which have a fixed 1:1000 ratio. For most applications, these time constants should be coordinated with the base-band time constant.

For a given base-band capacitor C_{BBO} , the capacitor value CPKD is:

$$C_{PKD} = 2.0*C_{BBO}, \text{ where } CPKD \text{ and } CBBO \text{ are in pF}$$

A $\pm 10\%$ ceramic capacitor should be used at this pin. This time constant will vary between 1:1 and 1.5:1 with variations in supply voltage, temperature, etc. The capacitor is driven from a 200 ohm “attack” source, and decays through a 200 K load. The peak detector is used to drive the “dB-below-peak” data slicer and the AGC release function. Where low data rates and OOK modulation are used, the “dB-below-peak” data slicer is optional. In this case the THLD2 pin can be left unconnected. The peak detector capacitor is discharged in the receiver power-down mode and in the transmit modes.

THLD2 is the “dB-below-peak” data slicer threshold adjust pin. The threshold is set by a 0 to 200 K resistor R_{TH2} between this pin and RREF. Increasing the value of the resistor decreases the threshold below the peak detector value (increases difference) from 0 to 120 mV. For most applications, this threshold should be set at 6 dB below peak, or 60 mV for a 50%-50% RF amplifier duty cycle. The value of the THLD2 resistor is given by:

$$R_{TH2} = 1.5*V, \text{ where } R_{TH2} \text{ is in kilohms and the threshold V is in mV.}$$

A $\pm 1\%$ resistor tolerance is recommended for the THLD2 resistor. Leaving the THLD2 pin open disables the dB-below-peak data slicer operation.

2.8 AGC

The AGC is an internal function for the third-generation ASH device, as opposed to the second-generation ASH devices. Second-generation devices required an AGC capacitor to avoid AGC “chattering” for long runs of 0’s in the data stream. The AGC capacitor provided a delay for AGC reset. The AGC control loop in the third-generation ASH devices has sufficient delay that an AGC capacitor is not necessary.

The purpose of the AGC function is to extend the dynamic range of the receiver, so that two transceivers can operate close together when running ASK and/or high data rate

modulation. The AGC also allows limited-range operation when using either ASK or OOK modulation in the presence of strong interference that would otherwise saturate the receiver.

The AGC circuit operates by the Peak Detector providing a reset signal to the AGC Control function through the AGC comparator. The onset of saturation in the output stage of RFA1 is detected and generates the AGC Set signal to the AGC Control function. The AGC Control function then selects the 5 dB gain mode for the first RX amplifier RFA1. The AGC Comparator will send a reset signal when the Peak Detector output (multiplied by 0.8) falls below the threshold voltage for DS1 (the DS1 threshold must be greater than zero for proper AGC operation). A *capacitor is not necessary at Pin 3 for third-generation devices*. Note that AGC operation requires the peak detector to be functioning, even if DS2 is not being used.

2.9 Transmitter Modulation

The transmitter chain consists of a SAW delay line oscillator followed by a modulated buffer amplifier. The SAW filter suppresses transmitter harmonics to the antenna. Note that the same SAW devices used in the amplifier-sequenced receiver are reused in the transmit modes.

Transmitter operation supports three modulation formats, on-off keyed (OOK) modulation, amplitude-shift keyed (ASK) modulation, and OOK/ASK “Digital Modulation”. When OOK modulation is chosen, the transmitter output turns completely off between “1” data pulses. OOK modulation provides compatibility with first-generation ASH technology, and provides for power conservation. When ASK modulation is chosen, a “1” pulse is represented by a higher transmitted power level, and a “0” is represented by a lower transmitted power level. ASK modulation must be used for high data rates (data pulses less than 30 μ s). ASK modulation also reduces the effects of some types of interference and allows the transmitted pulses to be shaped to control modulation bandwidth. When “Digital Modulation” is selected the user may apply a custom spreading code onto pin 18, or choose the “ISS” or Internal Spread Spectrum mode, which internally applies a fixed spreading code of alternating 1’s and 0’s at 460.8 kHz. This spreading code is designed to meet FCC 15.247 transmitter spectral density criteria for the 902-928 MHz band. When using the device in third-generation mode (USA only) it is recommended to operate the device with this feature enabled. Without enabling this feature it is not possible to comply with FCC 15.247 regulations. In this case, the output power must be adjusted to comply with FCC 15.249 regulations. For European operation the device may transmit at full output power and the ISS mode is not necessary.

The modulation format is chosen by the state of the CFGDAT (pin 17) and the CFGCLK (pin 18) pins when operating in 2G mode, and by writing the internal configuration registers when operating in third-generation mode. When any modulation format is chosen, the receiver RF amplifiers are turned off. In OOK mode, the delay line oscillator amplifier TXA1 and the output buffer amplifier TXA2 are turned off when the voltage to the TXMOD input falls below 220 mV. The data rate is limited by the turn-on and turn-off times of the delay line oscillator, which are 12 and 6 μ s respectively . In ASK mode TXA1 is

biased ON continuously, and TXA2 is modulated by the TXMOD input current.

2.9.1 OOK/ASK selection

On-off keyed (OOK) modulation should be chosen when compatibility with Murata's TX-series transmitters and RX-series receivers is desired. OOK modulation also provides some power savings in the transmit mode, and can be used when the minimum pulse width in the transmitted signal is 30 μ s or greater.

Amplitude-shift keyed (ASK) modulation should be chosen when the minimum pulse width in the transmitted signal is less than 30 μ s. ASK modulation should also be used when the transmitted signal has been shaped for spectrum bandwidth control and/or when a specific modulation depth is required.

Section 2.11 details how to configure the device for OOK or ASK modulation depending on the operating mode of the chip.

2.9.2 Transmitter power adjustment

Transmitter output power is proportional to the input current to TXMOD (Pin 8). Figures 2.9.2.1 and 2.9.2.2 show this relationship in several of the third-generation devices. A series resistor is used to adjust the peak transmitter output power. Maximum saturated output power requires 250 to 320 μ A of input current depending on operating frequency. In the ASK mode, minimum output power occurs when the modulation driver sinks about 10 μ A of current from this pin. Figure 2.9.2.1 shows the relationship between V_{TXM} and I_{TXM} . Figure 2.9.2.2 shows the relationship between P_o and I_{TXM} .

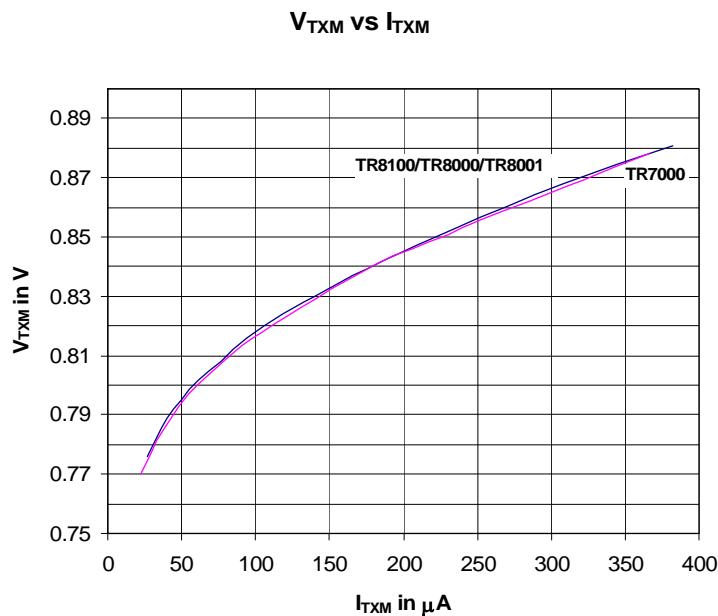


Figure 2.9.2.1

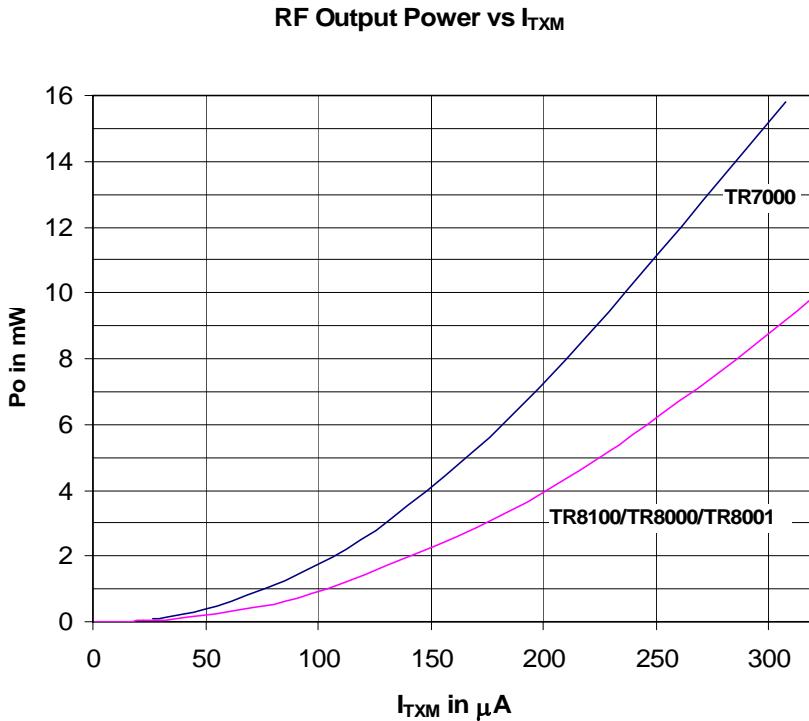


Figure 2.9.2.2

Peak transmitter output power P_o for a 3 Vdc supply voltage is:

$$P_o = 101 * (I_{TXM})^2 \text{ for } 916.5 \text{ MHz operation, where } P_o \text{ is in mW, and the peak modulation current } I_{TXM} \text{ is in mA}$$

$$P_o = 180 * (I_{TXM})^2 \text{ for } 433 \text{ MHz operation, where } P_o \text{ is in mW, and the peak modulation current } I_{TXM} \text{ is in mA}$$

A $\pm 5\%$ resistor is recommended. Peak transmitter output power varies somewhat with supply voltage. Products operating from batteries should be adjusted for peak output power using a “fresh” battery to assure regulatory compliance. Supply voltage regulation should be used in systems where maximum operating range must be maintained over the operating life of the battery. In the OOK mode, the TXMOD pin is usually driven with a logic-level data input (unshaped data pulses). OOK modulation is practical for data pulses of 30 μs or longer. In the ASK mode, the TXMOD pin accepts analog modulation (shaped or unshaped data pulses). As discussed above, ASK modulation is used for data pulses shorter than 30 μs . Note that the TXMOD input must be low in the power-down (sleep) mode.

2.9.3 ASK modulation depth adjustment

If the ASK transmitter mode is being used to allow the transmission of data pulses shorter than 30 μs , the same simple resistor calculation described above can be used to set peak transmitter output power. When the signal to the TXMOD resistor is brought close to

0 volts, maximum modulation depth is obtained. The modulation depth is usually greater than 45 dB, and is determined by the OFF isolation of TXA2.

The ASK modulation depth can be controlled over a range of 30 dB with relatively simple circuitry, as shown in Figure 2.9.3.1. Limiting ASK modulation depth is useful in improving system performance when certain types of weak interference are constantly present on an operating channel. Refer to Murata's application note, *Comparison of OOK, ASK and FSK Modulation*, at <http://www.murata.com> for further information on this topic.

ASK Modulation Depth Control Circuit

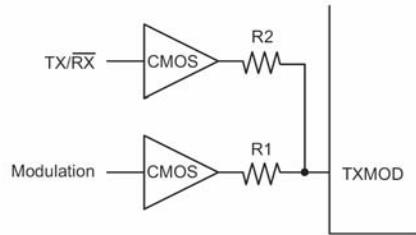


Figure 2.9.3.1

Referring to Figure 2.9.3.1, to control ASK modulation depth it is necessary to provide one TXMOD input current level (I_{MAX}) for peak output power, and a second input level (I_{MIN}) for the minimum output power. One approach to achieving this uses two CMOS buffers. The "TX/RX" buffer is held at a logic '1' during transmit and at a logic '0' during receive. The "Modulation" buffer is driven high and low by the transmit pulse stream. When the modulation buffer output is low, the transmitter output power is determined by the current through R1 minus the current going back into R2. The peak transmitter power is determined by the sum of the currents supplied by both gates through R1 and R2. The values of R1 and R2 are calculated as follows. Using the peak output power P_o from 2.9.2 above as the high power level:

$$I_{MAX} = (V_{TXH} - V_{TXMH})/R_{TXM}, \text{ so } G_{TXM} = G1 + G2 = I_{MAX}/(V_{TXH} - V_{TXMH}),$$

where I_{MAX} is in mA, G_{TXM} , $G1$ and $G2$ are in millimho, and V_{TXH} is the logic 1 voltage, and V_{TXMH} is the V_{TXM} voltage for I_{MAX} .

Next, choose the low output power level:

$$I_{MIN} = (P_{MIN} / 101)^{0.5}, \text{ where } P_{MIN} \text{ is in mW and } I_{MIN} \text{ is in mA}$$

$$G2 = (I_{MIN} - (I_{MAX} * ((V_{TXL} - V_{TXML}) / (V_{TXH} - V_{TXML})))) / (V_{TXH} - V_{TXL}),$$

where V_{TXL} is the logic 0 voltage level (0.2 V typical), V_{TXML} is the V_{TXM} voltage for I_{MIN} , and conductances are in millimhos and

$$G1 = ((I_{MAX} / (V_{TXH} - V_{TXMH})) - G2)$$

$R_1 = 1/G_1$, and $R_2 = 1/(G_2)$, where R_1 and R_2 are in kilohms

The above calculation provides starting point resistor values for a modulation depth of 30 dB or less. Figure 2.9.2.1 allows V_{TXMH} and V_{TXML} to be estimated for I_{MAX} and I_{MIN} .

2.9.4 Digital Modulation (TR8100 only)

In order to operate >0 dBm (+1 mW) output power in the U.S. the FCC requires the device to be capable of frequency hopping or digital spread spectrum modulation according to FCC 47 part 15.247. In this mode the TR8100 device is configured for single channel Spread Spectrum (SS) operation. The mixer in the transmitter is used to provide spread spectrum operation using binary phase shift keying (BPSK) to spread the transmitter output spectrum. Figure 2.9.4.1 shows the transmitter spectrum when using the internal spread spectrum mode (ISS).

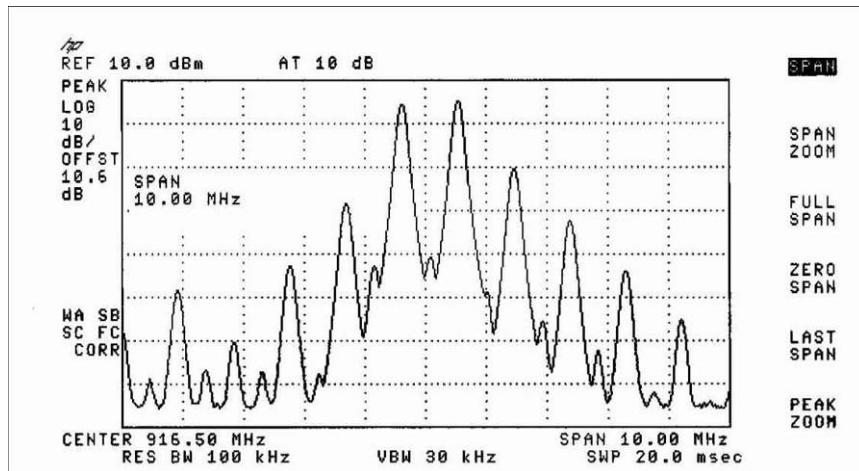


Figure 2.9.4.1

One of the mixers in the TX image reject mixer is shut down to form a simple double balanced mixer. The internal 460.8 kHz square wave spreading code causes BPSK modulation of the RF carrier from the TX RF oscillator.

The transmitter function in OOK or ASK mode is the same. The data is superimposed on the BPSK signal using either OOK or ASK modulation.

When internal spread spectrum mode is enabled, the receiver RF amplifiers are sequenced at the internal 614kHz rate. To receive the ISS signal, the receiver is put in the "Fixed Sequence" mode and simply demodulates the OOK/ASK modulation on the BPSK signal.

2.10 Data Output and Clock Recovery

RXDATA (Pin 7) is the receiver data output pin. This pin is a CMOS output with high drive capability. The signal on this pin can come from one of two sources. The default source is directly from the output of the data slicer circuit. The alternate source is from the radio's internal data and clock recovery circuit. Data and clock recovery are only available in third-generation mode. When the internal data and clock recovery circuit is enabled, the signal on RXDATA is switched from the output of the data slicer to the output of the data and clock recovery circuit when a packet start symbol is detected. Each recovered data bit is then output on the rising edge of a RXDCLK pulse (Pin 14), and is stable for reading on the falling edge of the RXDCLK pulse. When clock recovery is not used, RXDCLK is continuously 'low'. Once RXDCLK is activated by the detection of a start symbol, it remains active until the Start Vector Enable (SVEN) bit is reset. See section 1.4.4 for a detailed discussion of the start symbol. Normally RXDCLK is reset by the host processor as soon as a packet is received. Use of the clock recovery circuit reduces the burden on the microprocessor and allows a reduction in current consumption. The microprocessor can normally be in sleep mode and wake up only when a valid clock is provided.

2.11 Mode Control and Timing

The third-generation ASH transceiver may operate in 2 modes – 2G mode and third-generation mode. Second-generation (2G) mode is backward compatible for designs currently using the second-generation devices, such as TR1000, RX6000, etc. third-generation mode incorporates all of the second-generation modes plus new enhancements to the transmitter and receiver functions such as Digital Spread Spectrum Modulation, increased peak output power to +10mW, receive clock recovery, and 2-wire serial interface programming. The patented methods of using SAW stabilized oscillators and input SAW filtering remain at the heart of the third-generation ASH operation.

The four, second-generation transceiver operating modes – receive, transmit ASK, transmit OOK and power-down (sleep) - are controlled by the Modulation & Bias Control function, and are selected with the CNTRL1 (Pin 17) and CNTRL0 (Pin 18) inputs. Refer to Table 2.11.1.1 for mode control line settings. CFG (Pin 19) selects the mode of operation at power-up. CNTRL1 and CNTRL0 are CMOS compatible. These inputs must be held at a logic level and should not be left floating. The voltage to these pins should rise with the power supply voltage at turn on.

2.11.1 Mode control lines

CNTRL0 (pin 18) and CNTRL1 (pin 17) perform two functions based on the state of CFG pin 19. On power-up, if CFG pin 19 is 'low' the device defaults into second-generation mode. The CFG (pin 19) pin must be maintained low to operate in 2G mode. CNTRL0 (pin 18) and CNTRL1 (pin 17) are used to select the mode of operation just as the second-generation devices are used. If CFG pin is 'high' at power-up, or is brought 'high' at any time after power-up, the device configures into third-generation mode. In third-generation mode CNTRL0 (pin 18) and CNTRL1 (pin 17) function as the CFGCLK

(pin 18) and CFGDAT (pin 17) pins, respectively. These make up the 2-wire interface used to configure the internal registers for third-generation mode functions. After the CFG (pin 19) pin has been pulled ‘high’, it is not possible to configure back into 2G mode. To configure back into 2G mode, power must be cycled and the CFG (pin 19) pin held low on power-up.

For second-generation mode, setting CNTRL1 and CNTRL0 both high place the unit in the receive mode. Setting CNTRL1 high and CNTRL0 low place the unit in the ASK transmit mode. Setting CNTRL1 low and CNTRL0 high place the unit in the OOK transmit mode. Setting CNTRL1 and CNTRL0 both low place the unit in the power-down (sleep) mode. Note that the resistor driving TXMOD (Pin 8) must be low in the receive and sleep modes. Figure 2.11.1.1 shows the second-generation ASH transceiver mode and the state of CNTRL0 (pin 18) and CNTRL1 (pin 17).

2G Default OOK/ASK Configuration

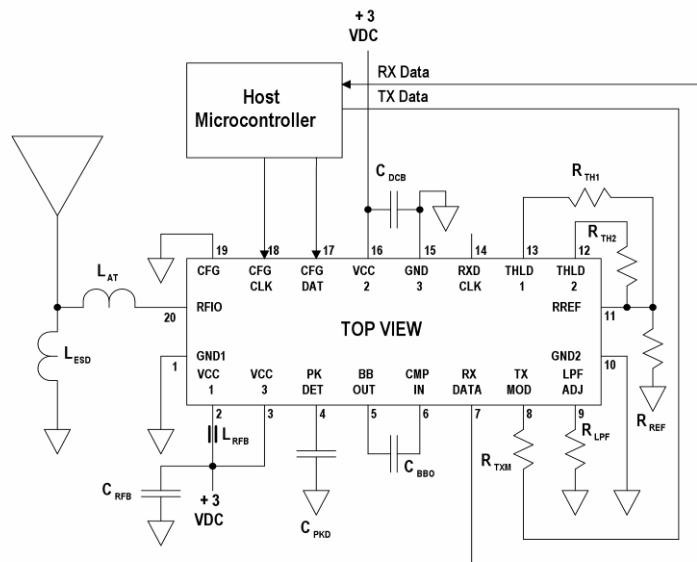


Figure 2.11.1.1

Pin 17	Pin 18	Mode
1	1	Receive
0	0	Sleep
0	1	Transmit OOK
1	0	Transmit ASK

Table 2.11.1.1

NOTE: It is not possible to comply with FCC 15.247 regulations using the default 2G control mode. In this case, the output power must be adjusted to comply with FCC 15.249 regulations.

After power-up, pulling CFG (pin 19) ‘high’ configures the device for operation in third-generation mode using the enhanced features mentioned in section 2.11. At this point CNTRL0 (pin 18) and CNTRL1 (pin 17) function as CFGCLK and CFGDAT,

respectively. CFGCLK (pin 18) is the 2-wire clock signal used to read and write configuration bytes to one of the three internal registers. The 2-wire interface will accept a maximum clock rate of 5.5MHz. A single configuration byte may be written in under 1.45usec. This allows for very little processor overhead when changing between different functions of the device. Each data bit is latched on the rising edge of the CFGCLK pin. The CFG (pin 19) pin should be held ‘high’ during the entire write cycle in order for the device to recognize it as a valid data write. Clocking data bits in when the CFG pin is ‘low’ will cause the data byte to be ignored. If the CFG pin is returned ‘low’ before all 8 bits are received, the entire byte is ignored.

Each configuration register may be addressed and written separately, or may be sequentially written back-to-back. The address of the initial register to be written should be applied first. Keeping the CFG pin ‘high’ through the entire write will cause the internal address counter to increment automatically to the next register address. When address register 2 is written, the internal counter will automatically roll over from address 2 to address 0. Figure 2.11.1.2 shows the third-generation ASH transceiver mode using CFGCLK (pin 18) and CFGDAT (pin 17) with a processor to configure the internal registers by the serial port.

3G ASH Transceiver Application Circuit

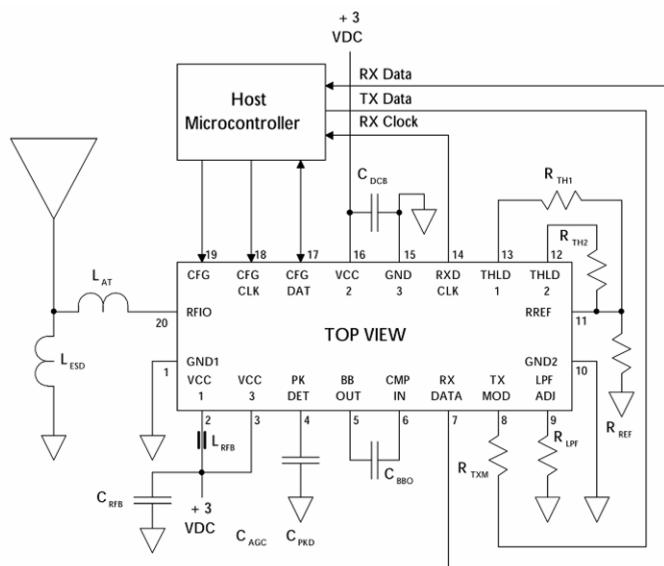


Figure 2.11.1.2

The contents of each register may also be read back. A bit read sequence is performed on the second falling edge following the last address bit clocked into the device. For a read sequence, the bit is latched on the first rising edge after the last address bit and the bit may be read on the falling edge of each CFGCLK thereafter. Figure 2.11.1.3 and Figure 2.11.1.4 show the read and write sequence of the serial port. Serial port timing is given in Table 2.11.1.3. The bits in the configuration registers are summarized in Table 2.11.1.2. Refer to the device data sheet for detailed descriptions of each bit function.

Configuration Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	CFG0	Sleep	TX/RX	ASK/OOK	-	Mode 1	Mode 0	-	SVEn (TR8100 only)
1	CFG1	-	-	ISSMod (TR8100 only)	-	BR3	BR2	BR1	BR0
2	LoSyn	Test	LOSyn6	LOSyn5	LOSyn4	LOSyn3	LOSyn2	LOSyn1	LOSyn0

Table 2.11.1.2

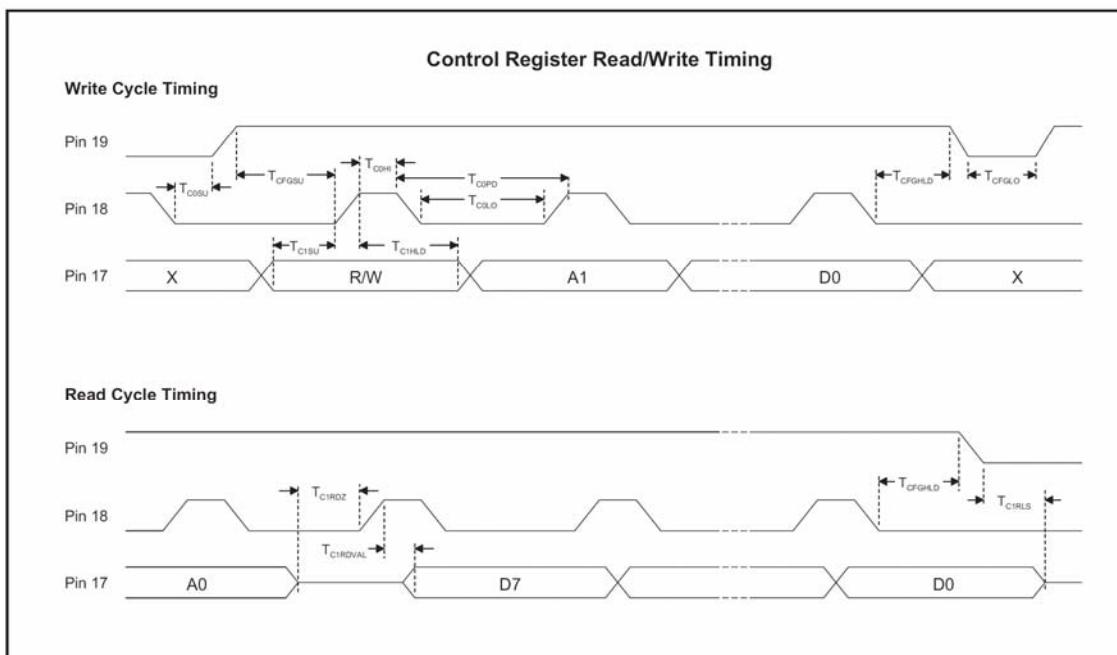


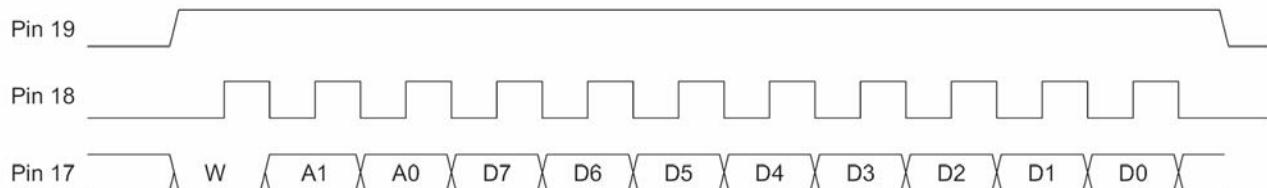
Figure 2.11.1.3

Symbol	Characteristic	Min	Typ	Max	Units	Conditions
T_{C0HI} , T_{C0LO}	Serial Port CLOCK (CFGCLK)			5.5	MHz	
T_{C0SU}	CFGCLK (18) low setup time to CFG (19) rising edge	45			ns	
T_{C0HI}	CFGCLK (18) high time	90			ns	
T_{C0LO}	CFGCLK (18) low time	90			ns	
T_{C0PD}	CFGCLK (18) period – rising edge to rising edge	190			ns	
T_{CFGSU}	CFG (19) setup time – active modes	90			ns	all modes except sleep
T_{CFGSU}	CFG (19) setup time – sleep mode	1000			ns	sleep mode
T_{C1SU}	CFGDAT (17) setup time to CFGCLK (18) rising edge	45			ns	
T_{C1HLD}	CFGDAT (17) hold time to CFGCLK (18) rising edge	90			ns	
T_{CFGLO}	CFG (19) low time between transfers	90			ns	
T_{C1RDZ}	CFGDAT (17) high impedance setup time on data read	20			ns	
$T_{C1RDVAL}$	CFGDAT (17) time to valid data output on read			90	ns	
T_{C1RLS}	CFGDAT (17) time to high impedance on end of transfer			20	ns	

Control Register Read/Write Detail

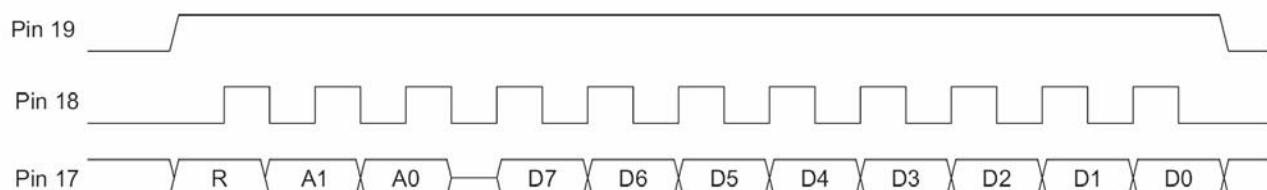
Single Byte Write Sequence

The write, address and data bits are clocked into the radio (left to right) on the rising edge of the clock input to Pin 18.



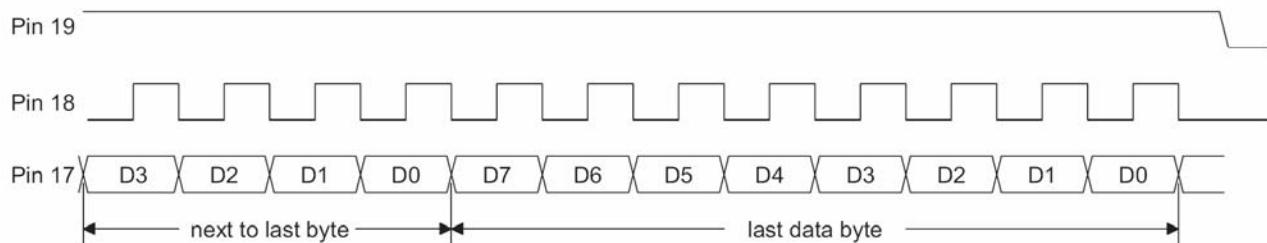
Single Byte Read Sequence

The read and address bits are clocked into the radio on the rising edge of the clock input to Pin 18; data is output on the rising edge of the clock and should be read into the host on the falling edge of the clock.



Multi-byte Write Sequence

Address increments automatically and rolls over from address 2 to address 0.



Multi-byte Read Sequence

Address increments automatically and rolls over from address 2 to address 0.

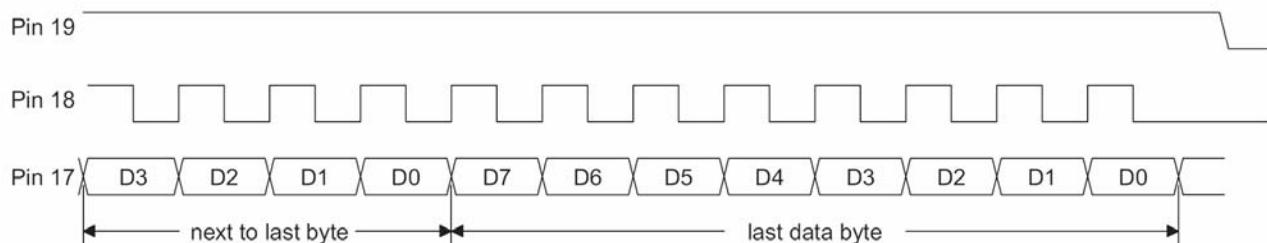


Figure 2.11.1.4

2.11.2 Turn-on timing

The maximum time t_{PR} required for the receive function to become operational at turn on is influenced by two factors. All receiver circuitry will be operational 1 ms after the supply voltage reaches 2.2 Vdc. The BBOUT-CMPIN coupling-capacitor is then DC stabilized in 4 time constants. The total turn-on time t_{PR} to stable receiver operation for a 10 ms power supply rise time is $15 \text{ ms} + 4*t_{BBC}$, where t_{BBC} is the coupling capacitor time constant (see section 2.6).

The maximum time required for either the OOK or ASK transmitter mode to become operational is 5 ms after the supply voltage reaches 2.2 Vdc (switch from receive mode).

2.11.3 Transmit-to-Receive timing

The maximum time required to switch from the OOK or ASK transmit mode to the receive mode is $4*t_{BBC}$, where t_{BBC} is the BBOUT-CMPIN coupling-capacitor time constant.

2.11.4 Receive-to-Transmit timing

After turn-on stabilization, the maximum time required to switch from receive to either transmit mode is 12 μs . Most of this time is the start-up of the transmitter oscillator.

2.11.5 Power-down and Wake-up Timing

The maximum transition time from the receive mode to the power-down (sleep) mode t_{RS} is 10 μs . The maximum transition time from either transmit mode to the power-down mode (t_{TOS} and t_{TAS}) is 10 μs .

The maximum transition time t_{SR} from the sleep mode to the receive mode is $4*t_{BBC}$, where t_{BBC} is the BBOUT-CMPIN coupling-capacitor time constant.

The maximum time required to switch from the sleep mode to either transmit mode (t_{STO} and t_{STA}) is 16 μs . Most of this time is due to the start-up of the transmitter oscillator.

2.12 Application Circuits

The third-generation ASH transceiver can be tailored to a wide variety of application requirements, allowing emphasis to be placed on simplicity or high performance. The most common application circuit configurations are presented in sections 2.12.1-2.12.4.

2.12.1 Minimum OOK configuration

The minimum OOK configurations are shown in Figures 2.12.1.1 and 2.12.1.2. This circuit is suitable for transmitting data with a minimum pulse width of 30 μs . Data slicer DS1 is implemented with threshold. Data slicer DS2 is not implemented. Only 13 external components are required to implement this transceiver configuration. This configuration is compatible with second-generation technology.

Second-generation Compatible Transceiver Application Circuit Minimum OOK Configuration

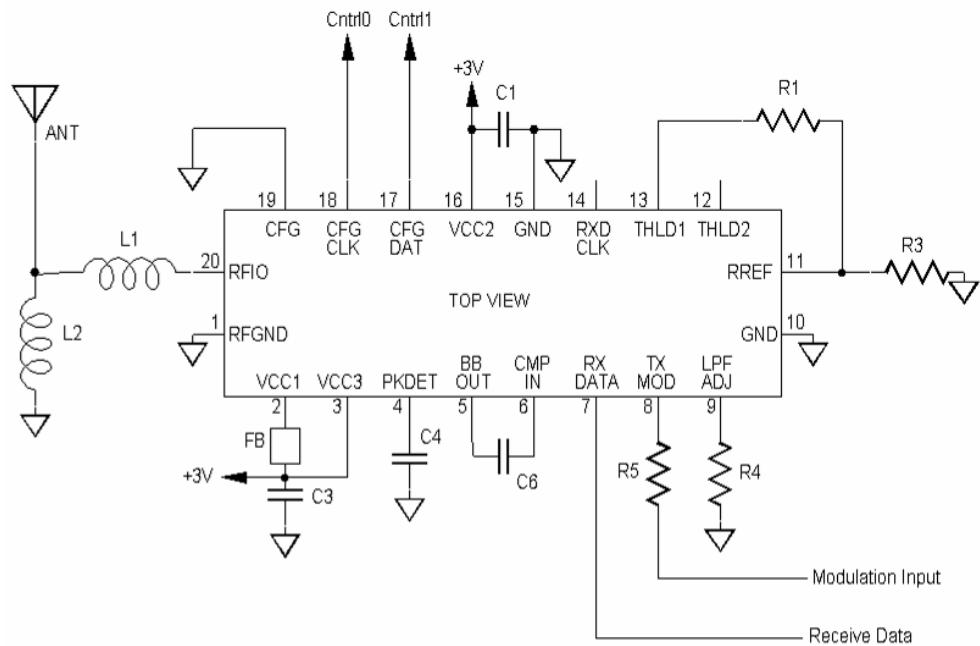


Figure 2.12.1.1

Third-generation ASH Transceiver Application Circuit Minimum OOK Configuration

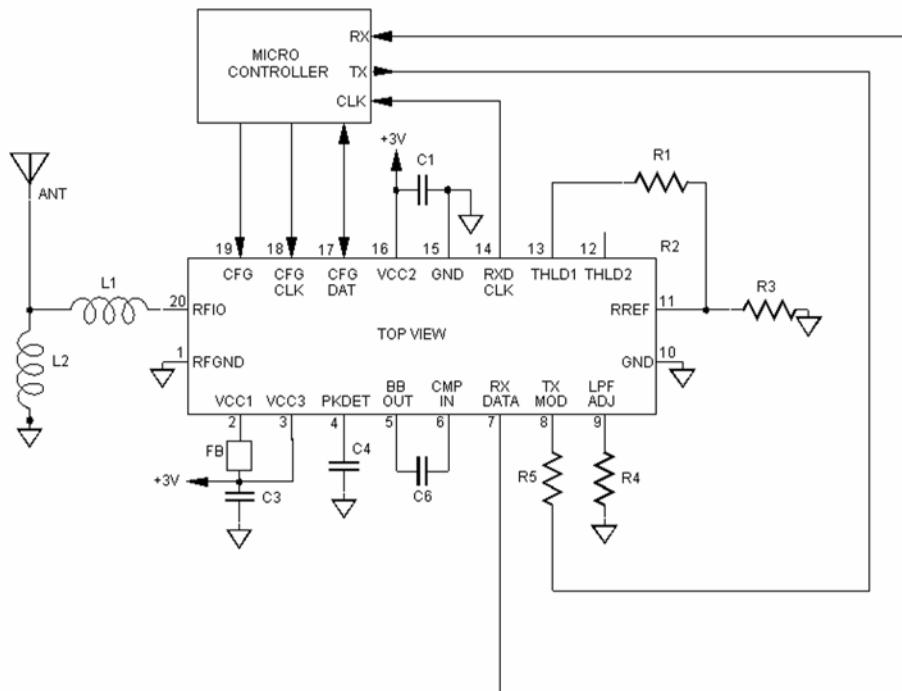


Figure 2.12.1.2

2.12.2 Standard OOK/ASK configuration

The standard OOK/ASK configurations are shown in Figures 2.12.2.1 and 2.12.2.2. This circuit is suitable for transmitting OOK data with a minimum pulse width of 30 µs, or ASK data at any data rate supported by the ASH transceiver being used.

For backward compatible second-generation mode both control lines to the transceiver can be toggled, allowing for the selection of receive, power-down, OOK transmit and ASK transmit with pin 19 connected to ground. Data slicer DS2 is implemented for good performance at higher data rates if the transmitted signal is bandwidth limited. AGC is also implemented for high dynamic range ASK operation, and to support limited-range OOK or ASK operation in the presence of strong interference. Thirteen external components, including a processor, are required to implement this flexible configuration.

**Second-generation Compatible Transceiver Application Circuit
Standard OOK/ASK configuration**

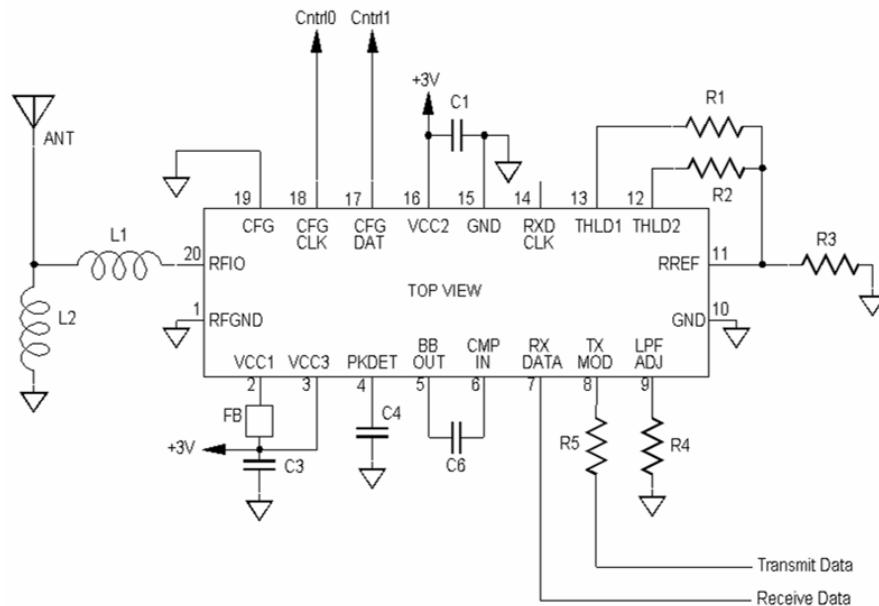


Figure 2.12.2.1

Third-generation ASH Transceiver Application Circuit Standard OOK/ASK Configuration

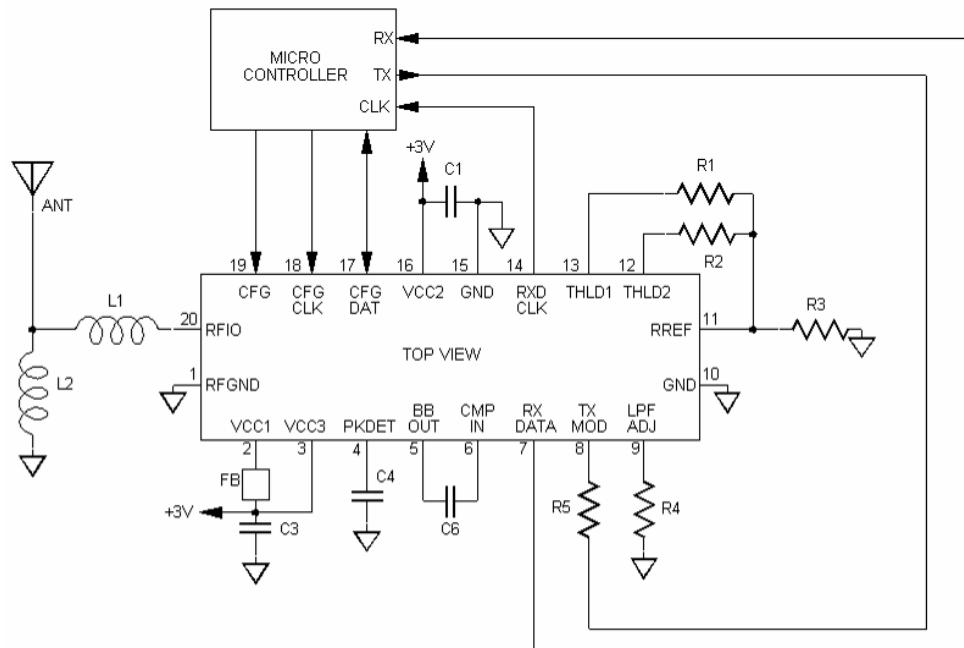


Figure 2.12.2.2

2.12.3 Receive-only configuration (OOK)

Figures 2.12.3.1 and 2.12.3.2 show the receive-only OOK configuration. It can be used with either a third-generation transceiver or second-generation ASH receiver. Receive and sleep modes are implemented using a single control line, which can be tied to Vcc for continuous operation. Data slicer DS1 is implemented with threshold. Data slicer DS2 is not implemented. Only eleven external components are required to implement the OOK receive-only configuration. For ASK reception, install a resistor at R2 (shaded below R1) if the transmitted signal is bandwidth limited.

Second-generation Compatible Transceiver Application Circuit Receive-Only configuration (OOK)

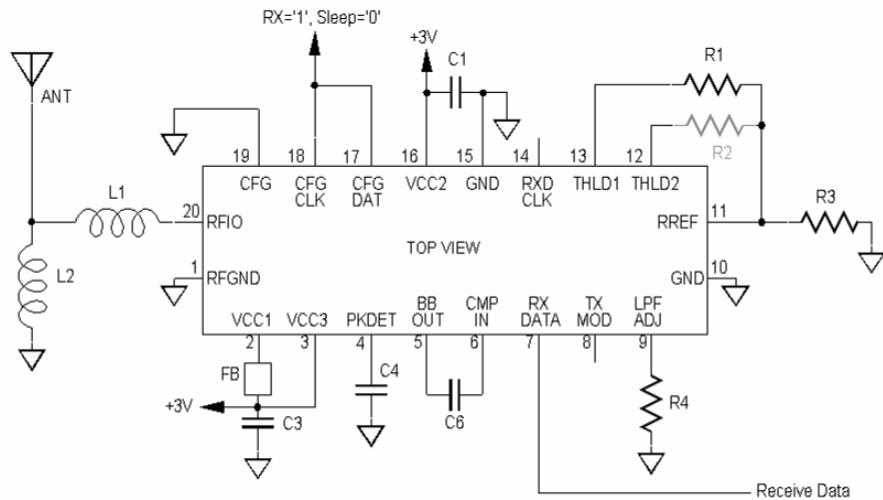


Figure 2.12.3.1

Third-generation ASH Transceiver Application Circuit Receive-Only configuration (OOK)

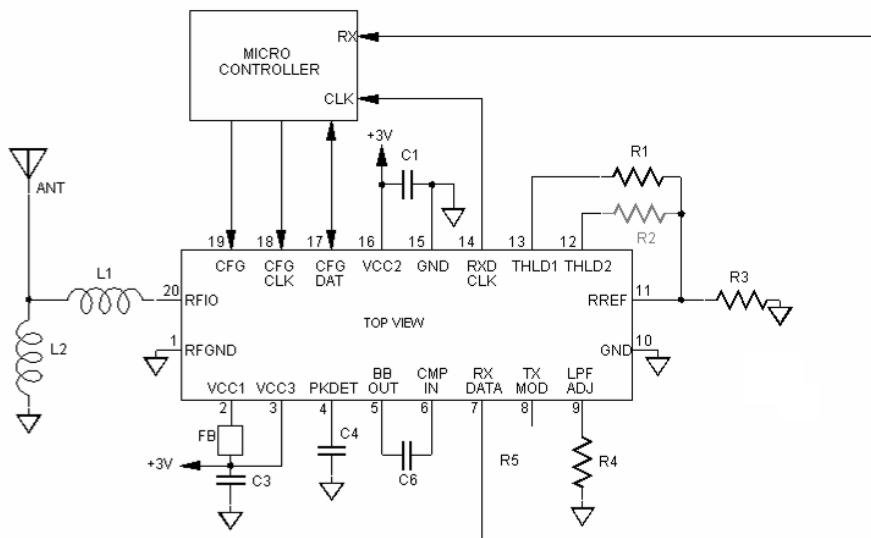


Figure 2.12.3.2

2.12.4 Transmit-only configuration (OOK)

Figures 2.12.4.1 and 2.12.4.2 show the transmit-only configuration (OOK). It can be used with either a third-generation transceiver or second-generation ASH transmitter. Only

eight external components are required to implement this configuration. The modulation input line must hold below 220 mV between transmissions to minimize transmitter current consumption. Modulation resistor values for R5 using second-generation devices will differ from third-generation devices.

Second-generation Compatible ASH Transceiver Application Circuit Transmit -Only configuration (OOK)

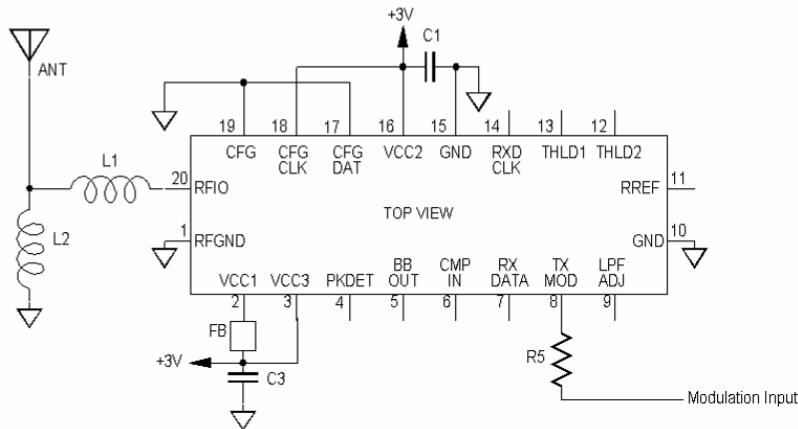


Figure 2.12.4.1

Third-generation ASH Transceiver Application Circuit Transmit-Only configuration (OOK)

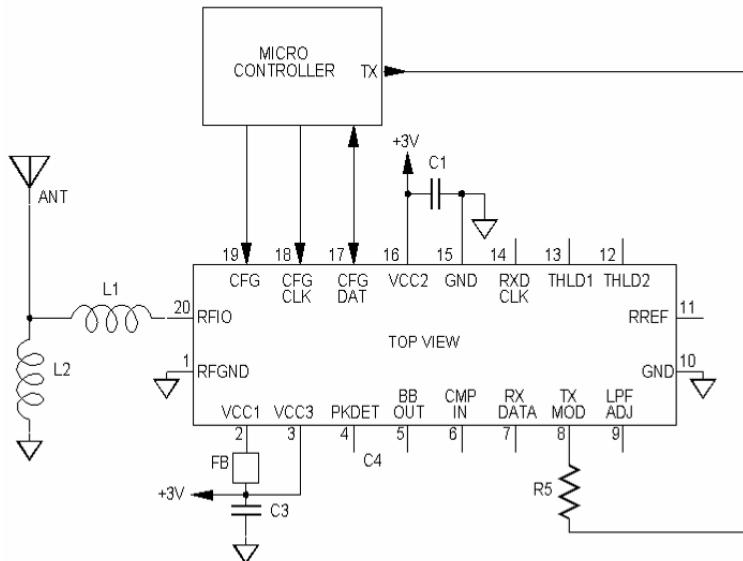


Figure 2.12.4.2

2.12.5 Set-up tables

Tables 2.12.5.1-2.12.5.4 provide component values for the above configurations at three standard data rates. Component values for other data rates can be computed using the formulas provided above and in the third-generation ASH transceiver data sheets.

TR8100 Transceiver Set-up, 3.0V, -40 to +85°C

Item	Symbol	OOK	OOK	OOK	ASK	Units	Notes
Encoded Data Rate	DRNOM	2.4	4.8	19.2	115.2	kb/s	see pages 1 & 2
Minimum Signal Pulse	SPMIN	416.66	208.32	52.08	8.68	μs	single bit
Maximum Signal Pulse	SPMAX	1666.66	833.28	208.32	34.72	μs	4 bits of same value
PKDET Capacitor	C4	.047	.022	.0056	820 pF	μF	±10% ceramic
BBOUT Capacitor	C6	.022	0.01	0.0027	390 pF	μF	±10% ceramic
TXMOD Resistor	R5	6.2	6.2	6.2	6.2	K	±5%, for 10 dBm output
LPFADJ Resistor	R4	470	470	160	24	K	±5%
RREF Resistor	R3	100	100	100	100	K	±1%
THLD2 Resistor	R2	-	-	-	*100	K	±1%, typical values
THLD1 Resistor2	R1	20	20	20	20	K	±1%, typical values
DC Bypass Capacitor	C1	4.7	4.7	4.7	4.7	μF	tantalum
RF Bypass Capacitor	C3	27	27	27	27	pF	±5% NPO
Series Tuning Inductor	L1	15	15	15	15	nH	50 ohm antenna
Shunt Tuning/ESD Inductor	L2	100	100	100	100	nH	50 ohm antenna
RF Bypass Bead	FB	Fair-Rite	Fair-Rite	Fair-Rite	Fair-Rite		2506033017YO or equivalent

* if the transmitted signal is bandwidth limited

Table 2.12.5.1

TR8000 Transceiver Set-up, 3.0V, -40 to +85°C

Item	Symbol	OOK	OOK	OOK	ASK	Units	Notes
Encoded Data Rate	DRNOM	2.4	4.8	19.2	115.2	kb/s	see pages 1 & 2
Minimum Signal Pulse	SPMIN	416.66	208.32	52.08	8.68	μs	single bit
Maximum Signal Pulse	SPMAX	1666.66	833.28	208.32	34.72	μs	4 bits of same value
PKDET Capacitor	C4	.047	.022	.0056	820 pF	μF	±10% ceramic
BBOUT Capacitor	C6	.022	0.01	0.0027	390 pF	μF	±10% ceramic
TXMOD Resistor	R5	6.2	6.2	6.2	6.2	K	±5%, for 10 dBm output
LPFADJ Resistor	R4	470	470	160	24	K	±5%
RREF Resistor	R3	100	100	100	100	K	±1%
THLD2 Resistor	R2	-	-	-	*100	K	±1%, typical values
THLD1 Resistor2	R1	20	20	20	20	K	±1%, typical values
DC Bypass Capacitor	C1	4.7	4.7	4.7	4.7	μF	tantalum
RF Bypass Capacitor	C3	27	27	27	27	pF	±5% NPO
Series Tuning Inductor	L1	15	15	15	15	nH	50 ohm antenna
Shunt Tuning/ESD Inductor	L2	100	100	100	100	nH	50 ohm antenna
RF Bypass Bead	FB	Fair-Rite	Fair-Rite	Fair-Rite	Fair-Rite		2506033017YO or equivalent

* if the transmitted signal is bandwidth limited

Table 2.12.5.2

TR7000 Transceiver Set-up, 3.0V, -40 to +85°C

Item	Symbol	OOK	OOK	OOK	ASK	Units	Notes
Encoded Data Rate	DRNOM	2.4	4.8	19.2	115.2	kb/s	see pages 1 & 2
Minimum Signal Pulse	SPMIN	416.66	208.32	52.08	8.68	μs	single bit
Maximum Signal Pulse	SPMAX	1666.66	833.28	208.32	34.72	μs	4 bits of same value
PKDET Capacitor	C4	.047	0.022	0.0056	820 pF	μF	±10% ceramic
BBOUT Capacitor	C6	.022	0.01	0.0027	390 pF	μF	±10% ceramic
TXMOD Resistor	R5	6.2	6.2	6.2	6.2	K	±5%, for 10 dBm output
LPFADJ Resistor	R4	470	470	160	24	K	±5%
RREF Resistor	R3	100	100	100	100	K	±1%
THLD2 Resistor	R2	-	-	-	*100	K	±1%, typical values
THLD1 Resistor1	R1	20	20	20	20	K	±1%, typical values
DC Bypass Capacitor	C1	4.7	4.7	4.7	4.7	μF	tantalum
RF Bypass Capacitor	C3	27	100	100	100	pF	±5% NPO
Series Tuning Inductor	L1	15	56	56	56	nH	50 ohm antenna
Shunt Tuning/ESD Inductor	L2	100	220	220	220	nH	50 ohm antenna
RF Bypass Bead	FB	Fair-Rite	Fair-Rite	Fair-Rite	Fair-Rite		2506033017YO or equivalent

* if the transmitted signal is bandwidth limited

Table 2.12.5.3

TR8001 Transceiver Set-up, 3.0V, -40 to +85°C

Item	Symbol	OOK	OOK	OOK	ASK	Units	Notes
Encoded Data Rate	DRNOM	2.4	4.8	19.2	115.2	kb/s	see pages 1 & 2
Minimum Signal Pulse	SPMIN	416.66	208.32	52.08	8.68	μs	single bit
Maximum Signal Pulse	SPMAX	1666.66	833.28	208.32	34.72	μs	4 bits of same value
PKDET Capacitor	C4	.047	0.022	0.0056	820 pF	μF	±10% ceramic
BBOUT Capacitor	C6	.022	0.01	0.0027	390 pF	μF	±10% ceramic
TXMOD Resistor	R5	6.2	6.2	6.2	6.2	K	±5%, for 10 dBm output
LPFADJ Resistor	R4	470	470	160	24	K	±5%
RREF Resistor	R3	100	100	100	100	K	±1%
THLD2 Resistor	R2	-	-	-	*100	K	±1%, typical values
THLD1 Resistor1	R1	20	20	20	20	K	±1%, typical values
DC Bypass Capacitor	C1	4.7	4.7	4.7	4.7	μF	tantalum
RF Bypass Capacitor	C3	27	100	100	100	pF	±5% NPO
Series Tuning Inductor	L1	15	10	10	10	nH	50 ohm antenna
Shunt Tuning/ESD Inductor	L2	100	100	100	100	nH	50 ohm antenna
RF Bypass Bead	FB	Fair-Rite	Fair-Rite	Fair-Rite	Fair-Rite		2506033017YO or equivalent

* if the transmitted signal is bandwidth limited

Table 2.12.5.4

2.13 PCB Layout and Assembly

Figure 2.13.1 is the schematic of the DR8100 data radio board. The following discussions will use the DR8100 as an example. Note that the board is designed to allow testing of both OOK and ASK modulation, and to allow pulse generator operation in either the low data rate or high data rate mode. Depending on which modulation and pulse generator set-up is chosen, some resistors may be left off the board or replaced with “zero ohm” jumper resistors.

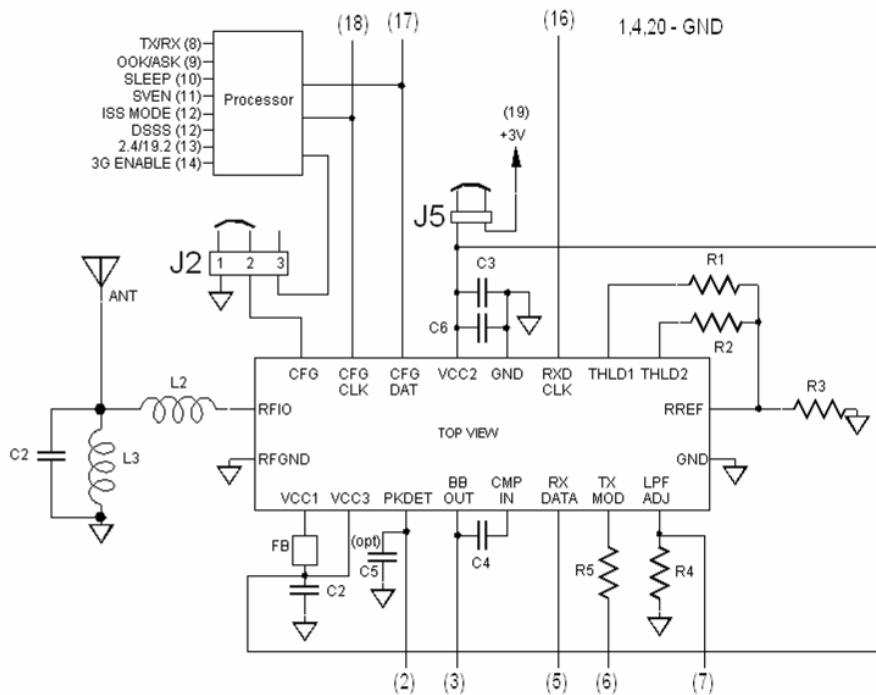


Figure 2.13.1

2.13.1 PCB layout

Figures 3.2.1 and 3.2.2 show the outline drawing and suggested pad layout of the SM3-20H package and figures 3.6.2 and 3.6.3 show the DR8100 printed circuit board (PCB) layout. The DR8100 layout is done on a two-layer printed circuit board. The bottom of the board is a solid ground plane. Ground connections are made from the top of the circuit board to the ground plane using plated-through holes. Note the special care used in the layout to keep all PCB traces as short as possible. The power supply pin to VCC1 is decoupled with a ferrite bead. The L3 component shown on the layout is an optional ESD protection diode for severe ESD environments. The C8 component shown in the layout is an optional RF capacitor that can be used to tune reactive antennas.

2.13.2 PCB Assembly

Figures 2.13.2.1 and 2.13.2.2 show the recommended temperature profile for reflow soldering leaded and lead-free third-generation ASH radio hybrids. The hybrid package consists of a ceramic base with a metal lid. The transceiver package is hermetic and the solder seal must not be compromised with excessive heat in assembly. It is critical that the transceiver package is never heated above 250°C. It is recommended that the transceiver package be heated no higher than 240°C for no more than 10 seconds.

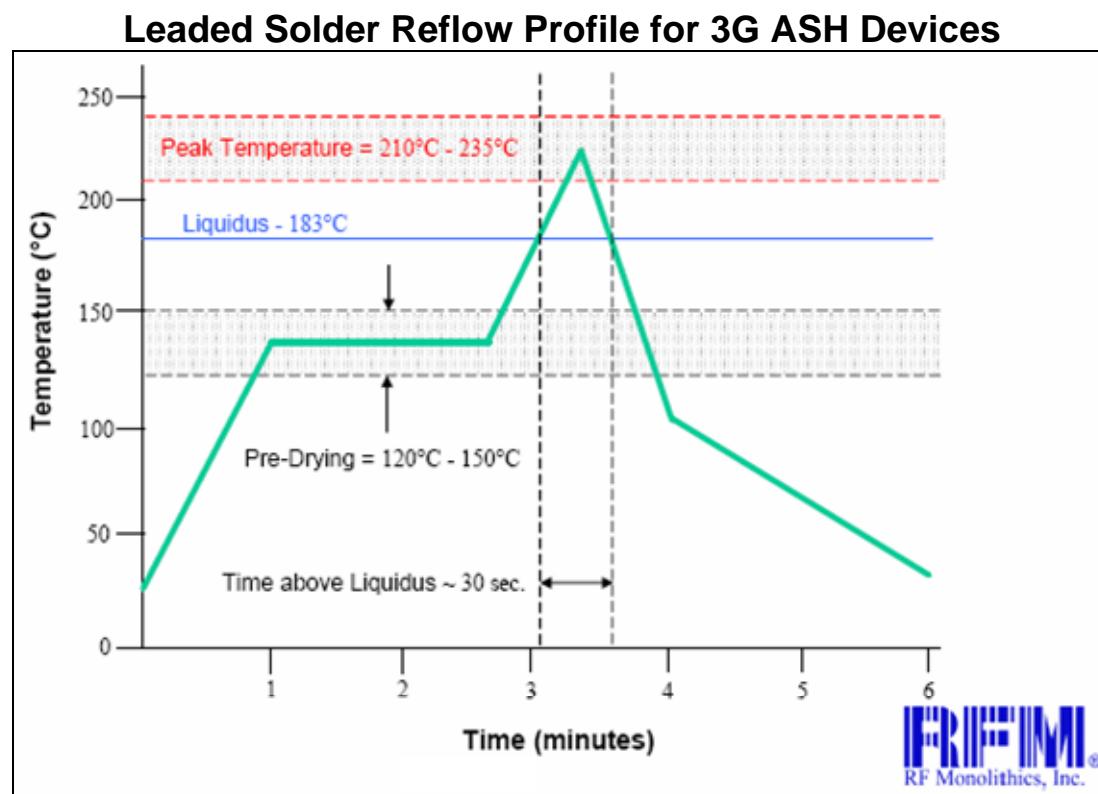


Figure 2.13.2.1

Lead-Free Solder Reflow Profile for 3G ASH Devices

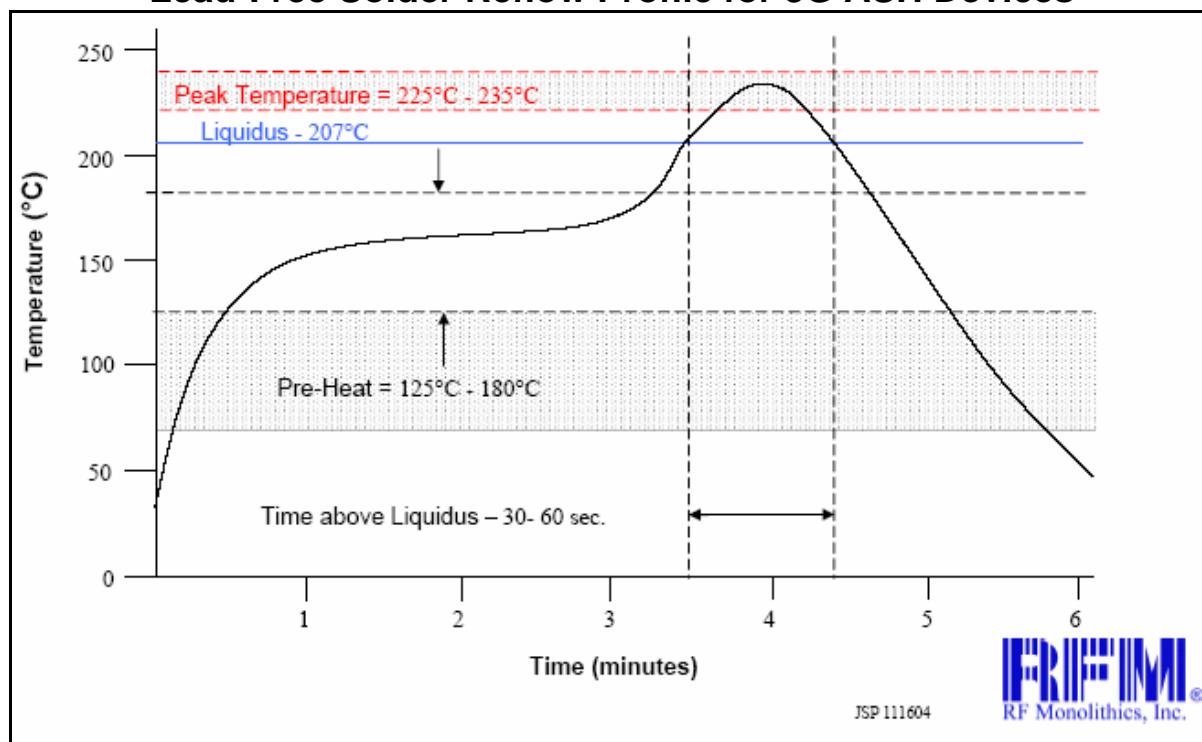


Figure 2.13.2.2

3 Appendices

3.1 Example Operating Distance Calculation

This example estimates the operating distance of a short-range wireless system transmitting 12-bit encoded data at 19.2 kbps using OOK modulation and no threshold at the receiver. A 3 dB filter bandwidth of 14.4 kHz is used (noise BW = 1.25 * 3 dB BW). Average transmitter output power is -9 dBm. A receiver noise figure of 7.5 dB is assumed. Antennas with 1 dB of gain are used. A 20 dB fade margin is chosen (99% Rayleigh probability). Packets are 38 bytes long (excluding preamble), or 456 bits. The system goal is to achieve 90% packet reads on the first try. The operating frequency is 916.5 MHz. Estimate the interference-free operating range:

A single bit error will result in a packet error. Only one bit error in 10 packets can be accepted or:

$$\text{BER} = 1/(456*10) = 2.193\text{E-}4$$

The required signal-to-noise ratio to achieve this BER using non-coherent detection of OOK modulation is:

$$10*\log_{10}(-2*\ln(2*\text{BER})) = 12 \text{ dB}$$

adding 7.5 dB for receiver noise figure, 3 dB for sampling loss and 7 dB for implementation loss:

$$12 + 17.5 = 29.5 \text{ dB}$$

The detected noise power (double sideband) through the 14.4 kHz filter is:

$$N = -174 \text{ dBm} + 10*\log_{10}(2*1.25*14400) = -128.4 \text{ dBm}$$

The signal level required is then:

$$-128.4 + 29.5 = -98.9 \text{ dBm}$$

The allowed path loss is:

$$L_{\text{PATH}} = P_O + G_{\text{ATX}} + G_{\text{ARX}} - L_{\text{FADE}} - S_{\text{RX}}$$

where P_O is the transmitter peak output power, G_{ATX} is the transmitter antenna gain (over isotropic), G_{ARX} is the receiver antenna gain, L_{FADE} is the fade margin, and S_{RX} is the required received signal strength. Assuming a 20 dB fade margin:

$$L_{\text{PATH}} = -9 \text{ dBm} + 1 \text{ dB} + 1 \text{ dB} - 20 \text{ dB} - (-98.9 \text{ dBm}) = 71.9 \text{ dB}$$

Now comes the trickiest part of the estimate. For ideal free space propagation, path loss is directly proportional to the square of the distance, or $20\log_{10}(D)$, and is also directly proportional to the square of the operating frequency, or $20\log_{10}(f)$. The equation for distance in meters is:

$$L_{PATH} = -27.6 \text{ dB} + 20\log_{10}(f) + 20\log_{10}(D),$$

where f is in MHz and D is in m $71.9 = -27.6 \text{ dB} + 59.2 + 20\log_{10}(D)$; $D = 103.5$ meters, or 339.4 feet.

Again, this range can only be achieved under ideal free space conditions, approximated by mounting your equipment at the top of two 100 meter towers spaced 103.5 meters apart. Down on the ground, and especially in dense cubical office space where propagation loss can be higher than $1/d^4$, the practical operating range is much less. One of the more commonly used propagation models for near ground and/or indoor use is the simplified Keenan-Motley (IBM Zurich) equation:

$$L_{PATH} = -27.6 \text{ dB} + 20\log_{10}(f) + N \cdot 10\log_{10}(D),$$

where N is 2 or greater, f is in MHz and D is in m.

As before, $N = 2$ for free space propagation. $N = 2.5$ is typical for UHF propagation 1.5 meter above the ground in an open field or large, open indoor space. $N = 3$ is typical for indoor open office and retail space, and $N = 4$ is typical of dense cubical office space.

For $N = 2.5$, $N = 3$ and $N = 4$ our estimated operating distance is:

$N = 2.5$:

$$71.9 = -27.6 \text{ dB} + 59.2 + 25\log_{10}(D); D = 40.9 \text{ meters, or } 134.1 \text{ feet}$$

$N = 3$:

$$71.9 = -27.6 \text{ dB} + 59.2 + 30\log_{10}(D); D = 22.0 \text{ meters, or } 72.2 \text{ feet}$$

$N = 4$:

$$71.9 = -27.6 \text{ dB} + 59.2 + 40\log_{10}(D); D = 10.2 \text{ meters, or } 33.0 \text{ feet}$$

These range estimates are generally less than "real world" observations made using Murata Virtual Wire Development Kits as propagation survey tools. This is due to the conservative choice of a 20 dB fade margin, and the stringent packet error rate performance criteria used in these calculations.

3.2 PCB Pad Layouts

Figure 3.2.1 and 3.2.2 show the SM3-20H package and the dimensions of the recommended PCB layout for the SM3-20H package.

SM3-20H Package

Top View Bottom View

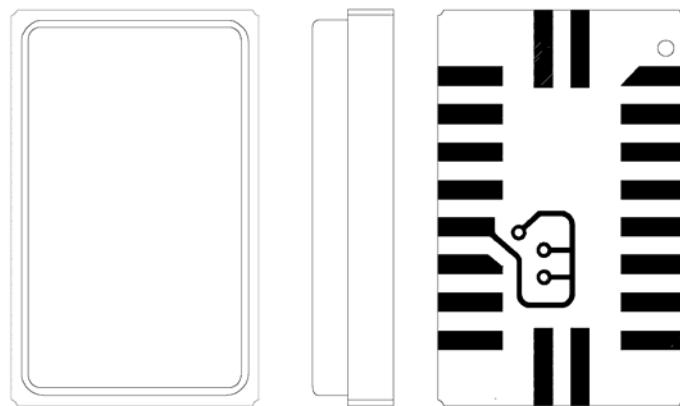
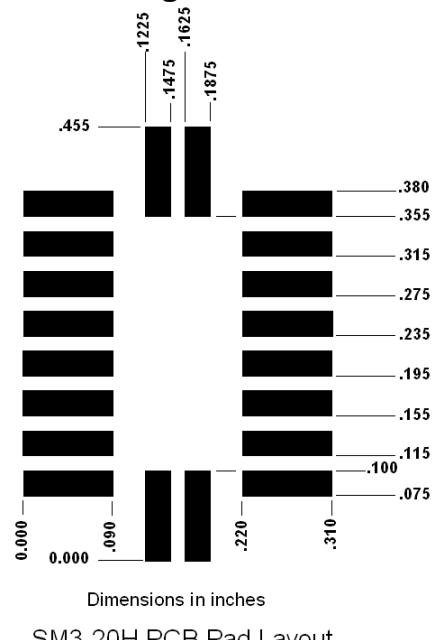


Figure 3.2.1



SM3-20H PCB Pad Layout

Figure 3.2.2

3.3 Byte to 12-Bit DC-Balanced Symbol Conversion

The QuickBasic program below is an example of DC-balanced encoding and decoding. Encoding and decoding are done by mapping between nibbles (4 bits) and 6-bit half-symbols using a look-up table.

```
' DC_BAL.BAS 2000.12.22 @ 10:00 CST
' Copyright 2000, RF Monolithics, Inc.
' Converts any 4-bit pattern to 6-bit DC-balanced pattern

SCREEN 0
WIDTH 80
CLS

DEFINT A-Z          ' 16 bit integers
DIM BTbl(0 TO 15)   ' BTbl holds 6-bit patterns
GOSUB BldTbl        ' build symbol BTbl

DO
    INPUT "Input nibble (0 to 15): ", N      ' get test nibble
    IF (N < 0) OR (N > 15) THEN EXIT DO      ' exit if out of range
    S = BTbl(N)                            ' get half-symbol from table
    PRINT
    PRINT N; "maps to"; S; "("; HEX$(S); " Hex)" ' print nibble and half-symbol
    GOSUB GetNibl                          ' now get nibble back from half-symbol
    PRINT
    PRINT S; "maps back to"; NN; "("; HEX$(NN); " Hex)"
    PRINT

LOOP

PRINT
PRINT "Input out of range"

END

GetNibl:

Q = 0              ' zero table index
DO                ' nibble look-up loop
    IF S = BTbl(Q) THEN      ' look-up test
        EXIT DO            ' got match so exit
    END IF
    Q = Q + 1            ' else increment index
    IF Q > 15 THEN        ' if not in table
        PRINT " Not in table!"
        END                ' print warning
    END IF
    LOOP
    NN = Q              ' Q is decoded nibble

RETURN

BldTbl:

BTbl(0) = 13      ' 0D hex
BTbl(1) = 14      ' 1E hex
BTbl(2) = 19      ' 13 hex
BTbl(3) = 21      ' 15 hex
BTbl(4) = 22      ' 16 hex
BTbl(5) = 25      ' 19 hex
BTbl(6) = 26      ' 1A hex
BTbl(7) = 28      ' 1C hex
BTbl(8) = 35      ' 23 hex
BTbl(9) = 37      ' 25 hex
BTbl(10) = 38     ' 26 hex
```

BTbl(11) = 41	' 29 hex
BTbl(12) = 42	' 2A hex
BTbl(13) = 44	' 2C hex
BTbl(14) = 50	' 32 hex
BTbl(15) = 52	' 34 hex

RETURN

3.4 Sample SPI Assembly code for writing ASH configuration registers

This is part of the code that is used on the DR evaluation boards that takes advantage of the on-board SPI port to update the registers when configured for 3G mode. Even though the ASH device does not implement a standard SPI interface, the SPI can be used successfully to write the internal configuration registers through a little programming trickery.

Three, bit addressable registers, REG1, REG2, and REG3, are created in memory to hold the state of each bit. Each bit is assigned in accordance with section 2.11.1 (also refer to the specific device data sheet). When a bit is changed, the subroutine below is called and the registers are updated. Note that the R/nW bit and the two address bits, A0 and A1, are included in the register configuration, but are not a valid bit in the configuration registers. When all three registers are written, the last register is 5 bits short. When CFG (pin 19) is brought 'High', CFG register 2 is totally ignored and remains in its default state since the CFG pin is brought 'High' before 8 bits are clocked in.

3G Configuration Registers (ex. TR8100)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	CFG0	Sleep	TX/RX	ASK/OOK	-	Mode 1	Mode 0	-	SV En
1	CFG1	-	-	ISS	-	BR3	BR2	BR1	BR0
2	CFG2	Test	0	0	0	0	0	0	0

Memory Registers

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
REG1	R/nW	A1	A0	Sleep	TX/RX	ASK/OOK	-	Mode 1
REG2	Mode 0	-	SV En	-	-	ISS	-	BR3
REG3	BR2	BR1	BR0	0	0	0	0	0

Dummy Bits

```

CLR  RW      ;CLEAR BIT FOR WRITE
CLR  A0      ;ADDRESS '00' CONFIG REG 0
CLR  A1      ;" "
SETB SS      ;PULL PIN 19 HIGH TO WRITE TO SPI

;** BEGIN SPI SEND CONFIG **
MOV   SPI0DAT, REG1      ;LOAD SPI REGISTER
WAIT_TX1:
JNB   SPIF, WAIT_TX1    ;WAIT FOR SPI TO XFER,LOOP IF STILL BUSY
CLR   SPIF
MOV   SPI0DAT,REG2      ;LOAD SPI REGISTER
WAIT_TX2:
JNB   SPIF, WAIT_TX2    ;WAIT FOR SPI TO XFER,LOOP IF STILL BUSY
CLR   SPIF
MOV   SPI0DAT, REG3      ;LOAD SPI REGISTER
WAIT_TX3:
JNB   SPIF, WAIT_TX3    ;WAIT FOR SPI TO XFER,LOOP IF STILL BUSY
CLR   SPIF
CLR   SS      ;PULL PIN 19 LOW
CLR   P0.3     ;PULL CFGDAT PIN 'LOW'
CLR   P0.7     ;PULL CFGCLK PIN 'LOW'
LJMP  START      ;GO TO BEGINNING

```

3.5 Third-Generation ASH Transceivers

The same technology developed for the second-generation ASH transceiver is used in the third-generation ASH transceiver hybrids to support demanding one-way control and telemetry applications. All third-generation ASH radios utilize a standardized 20 pin layout. Pins related to the transmit and receive functions are in the same location and have the same input/output electrical characteristics on third-generation ASH transceivers. This makes it possible to do a single PCB layout and build it as a transmitter, receiver or transceiver.

Please refer to the individual product data sheets for further information.

3.6 EMI Robust ASH Radio PCB Layouts

Electromagnetic compatibility (EMC) testing is required prior to marketing short-range wireless devices in Europe, and for certain industrial applications worldwide. EMC testing is done by applying an RF field of a specific strength (measured in V/m) to confirm the product's operation is not disrupted due to electromagnetic interference (EMI). The minimum field strength used in EMC testing is 3 V/m. EMC testing is typically done over a range of frequencies from 10 MHz to 1 GHz, except for an exclusion band around the operating frequency of the radio.

ASH radios have been specifically developed for EMI robustness. For best results, however, these radios must be used in application circuits and PCB layouts designed for robust EMI performance. Figure 3.6.1 shows the schematic of an EMI robust application circuit, and Figures 3.6.2 and 3.6.3 show EMI robust PCB layouts for the SM3-20H ASH radio packages. The Gerber files for these layouts are located on Murata's web site, <http://www.murata.com>, under Application Notes.

Referring to Figures 3.6.2 and 3.6.3, note the special Vcc routing for the SM3-20H ASH radio package and the Vcc RF decoupling capacitors on both sides of the radio package. Also note the heavy use of ground plane on the top of the PCB, connected directly to the solid ground plane underneath.

**Third-generation ASH RADIO Application Circuit Schematic
EMI Robust Configuration**

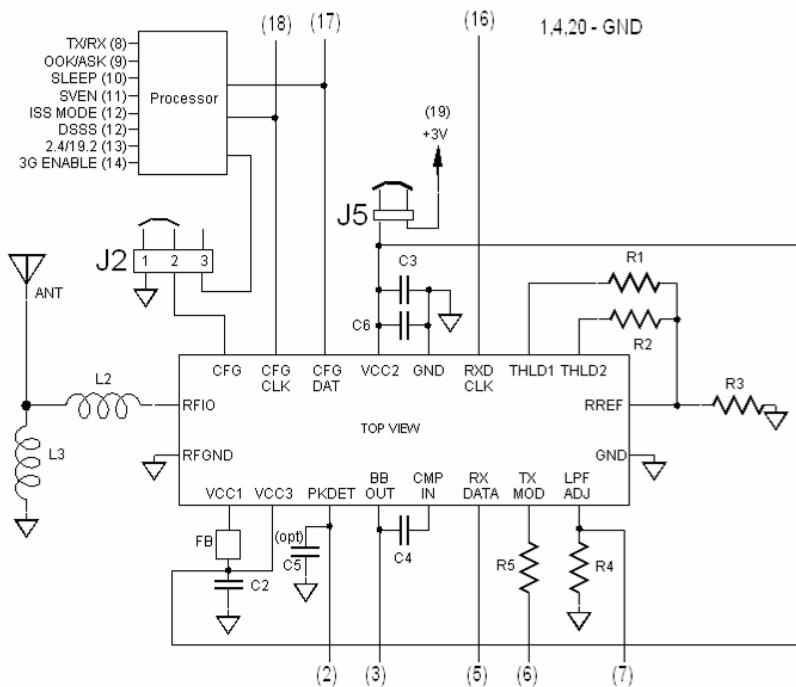


Figure 3.6.1

For EMC testing at 3 V/m, special grounding of the ASH radio hybrid lid is not usually required. But for higher field strengths, it may be necessary to ground the lid with a small clip or wire, or cover the top of the PCB with a small “tin plate” shield.

The strong RF fields used in EMC testing can disrupt the operation of op-amps, regulators, analog-to-digital converters and even logic circuits. It is important to use compact PCB layouts and adequate RF decoupling in the electronics throughout the product. *It is especially important to decouple RF from the Vcc supply to the ASH radio.*

EMI Robust ASH Radio PCB Layout, Top View, SM3-20H Package

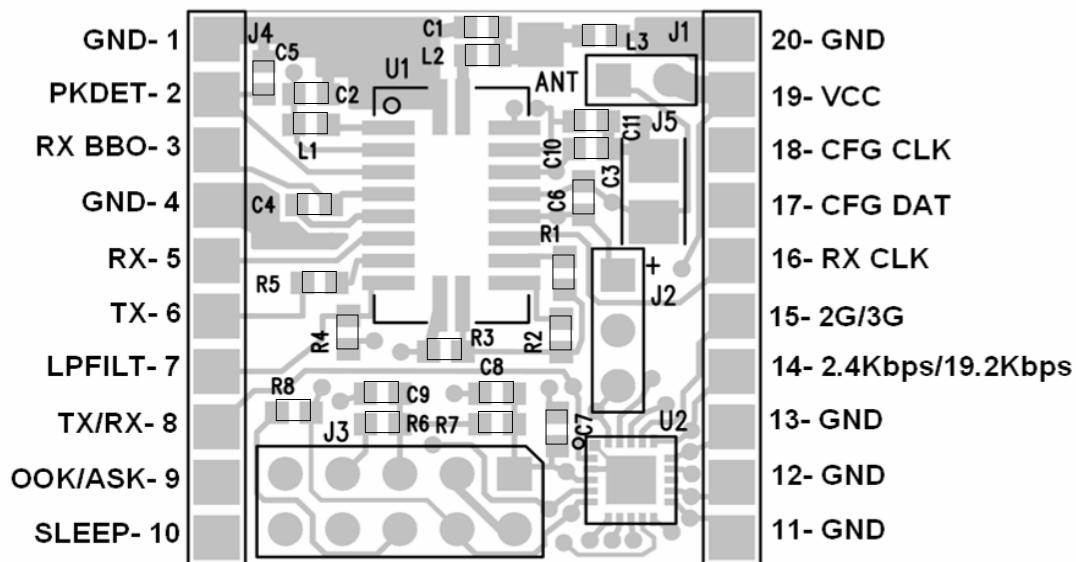


Figure 3.6.2

**EMI Robust ASH Radio PCB Layout,
Bottom View, SM3-20H Package**

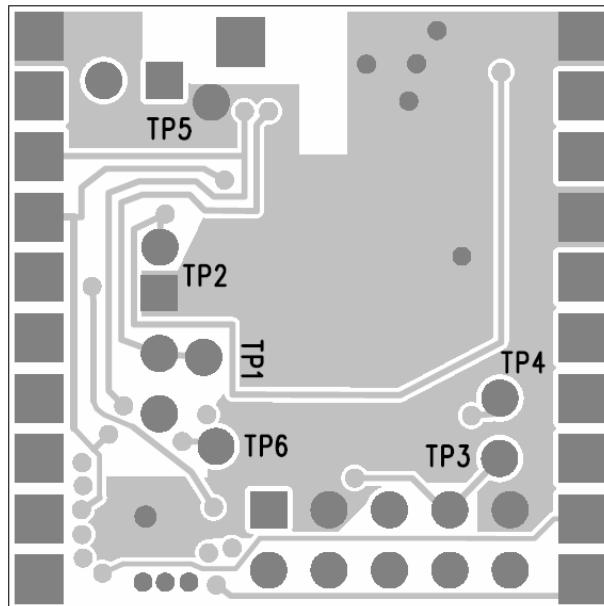


Figure 3.6.3

Bill of Material, TR8100/TR8000, 916.50 MHz, 4.8kbps

Item	Reference	Description	Value	Qty
1	C2	Capacitor SMT 0603	27pF	1
2	C4	Capacitor SMT 0603	.01uF	1
3	C5	Capacitor SMT 0603	.022uF	1
4	C6	Capacitor SMT 0603	100pF	1
5	C7	Capacitor SMT 0603	0.1uF	1
6	C8	Capacitor SMT 0603	0.1uF	1
7	C9	Capacitor SMT 0603	0.1uF	1
8	C3	Capacitor Tantalum EIA-B	4.7uF	1
9	L1	Fair-rite Bead 0603	2506033017YO	1
10	L2	Inductor Chip 0603	15nH	1
11	L3	Inductor Chip 0603	100nH	1
12	R1	Resistor Chip 0603	20K	1
13	R2	-	-	1
14	R3	Resistor Chip 0603	100K	1
15	R4	Resistor Chip 0603	470K	1
16	R5	Resistor Chip 0603	6.2K	1
17	R6	Resistor Chip 0603	1.0K	1
18	R8	Resistor Chip 0603	1.0K	1
19	R7	Resistor Chip 0603	10K	1
20	U2	C8051F330 SILICON LABS Microcontroller		1
21	U1	IC, TR8100 or TR8000		1

Bill of Material, TR8001, 868.35 MHz, 4.8kbps

Item	Reference	Description	Value	Qty
1	C2	Capacitor SMT 0603	100pF	1
2	C4	Capacitor SMT 0603	.01uF	1
3	C5	Capacitor SMT 0603	.022uF	1
4	C6	Capacitor SMT 0603	100pF	1
5	C7	Capacitor SMT 0603	0.1uF	1
6	C8	Capacitor SMT 0603	0.1uF	1
7	C9	Capacitor SMT 0603	0.1uF	1
8	C3	Capacitor Tantalum EIA-B	4.7uF	1
9	L1	Fair-rite Bead 0603	2506033017YO	1
10	L2	Inductor Chip 0603	10nH	1
11	L3	Inductor Chip 0603	100nH	1
12	R1	Resistor Chip 0603	20K	1
13	R2	-	-	
14	R3	Resistor Chip 0603	100K	1
15	R4	Resistor Chip 0603	470K	1
16	R5	Resistor Chip 0603	6.2K	1
17	R6	Resistor Chip 0603	1.0K	1
18	R8	Resistor Chip 0603	1.0K	1
19	R7	Resistor Chip 0603	10K	1
20	U2	C8051F330 SILICON LABS Microcontroller		1
21	U1	IC, TR8001		1

Bill of Material, TR7000, 433.92 MHz, 4.8kbps

Item	Reference	Description	Value	Qty
1	C2	Capacitor SMT 0603	100pF	1
2	C4	Capacitor SMT 0603	.01uF	1
3	C5	Capacitor SMT 0603	.022uF	1
4	C6	Capacitor SMT 0603	100pF	1
5	C7	Capacitor SMT 0603	0.1uF	1
6	C8	Capacitor SMT 0603	0.1uF	1
7	C9	Capacitor SMT 0603	0.1uF	1
8	C3	Capacitor Tantalum EIA-B	4.7uF	1
9	L1	Fair-rite Bead 0603	2506033017YO	1
10	L2	Inductor Chip 0603	56nH	1
11	L3	Inductor Chip 0603	220nH	1
12	R1	Resistor Chip 0603	20K	1
13	R2	-	-	
14	R3	Resistor Chip 0603	100K	1
15	R4	Resistor Chip 0603	470K	1
16	R5	Resistor Chip 0603	6.2K	1
17	R6	Resistor Chip 0603	1.0K	1
18	R8	Resistor Chip 0603	1.0K	1
19	R7	Resistor Chip 0603	10K	1
20	U2	C8051F330 SILICON LABS Microcontroller		1
21	U1	IC, TR7000		1

3.7 Modulation Bandwidth Control

To comply with ETSI EN 300 220-1 regulations, SRD transmitter modulation sidebands must be suppressed to at least 250 nW (-36 dBm) outside of the band or sub-band of operation (see EN 300 220-1 Section 8.6 for test details). The modulation bandwidth of an ASH transmitter or transceiver can be controlled by low-pass filtering the signal to the TXMOD input (Pin 8). For transmitted data rates up to 20 kbps (data pulses 50.0 μ s or greater), the simple low-pass filter shown in Figure 3.7.1 below can be used to meet ETSI requirements under most circumstances. The filter in Figure 3.7.1 can be used with either

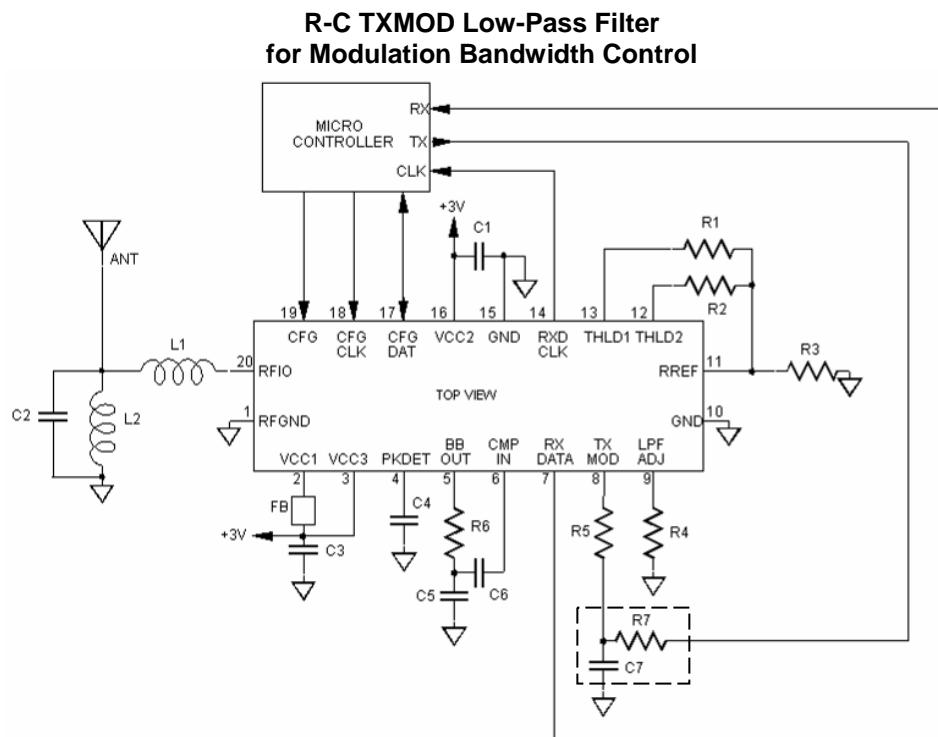


Figure 3.7.1

OOK or ASK modulation. When designing a low-pass filter, note that the dynamic input impedance of the TXMOD Pin is about 300 ohms. This value will vary some with temperature and drive level. For consistent filter behavior, a resistor of several kilohms is used between the capacitor in the low-pass filter and the TXMOD Pin. Table 3.7.1 provides starting-point filter values for a range of data rates. The driving point impedance of the data source will influence the component values used in the low-pass filter. If the driving point impedance is relatively high, the value of C7 in Table 3.7.1 will need to be reduced. Note that the driving point voltage, driving point impedance, and the values of resistors R5 and R7 set the peak TXMOD current. Refer to the individual ASH radio data sheets for recommended peak TXMOD current values.

Table 3.7.1

ASH Radio	Data Rate, bps	SP _{MIN} , μ s	R7	C7	R5
TR8100/TR8000/TR8001	1200	833.3	2.4 K	0.1 μ F	3.9 K
TR8100/TR8000/TR8001	2400	416.7	2.4 K	0.056 μ F	3.9 K
TR8100/TR8000/TR8001	4800	208.3	2.4 K	0.027 μ F	3.9 K
TR8100/TR8000/TR8001	9600	104.2	2.4 K	0.015 μ F	3.9 K
TR8100/TR8000/TR8001	19200	52.1	2.4 K	0.0068 μ F	3.9 K
TR7000	1200	833.3	4.3 K	0.056 μ F	3.9 K
TR7000	2400	416.7	4.3 K	0.027 μ F	3.9 K
TR7000	4800	208.3	4.3 K	0.015 μ F	3.9 K
TR7000	9600	104.2	4.3 K	0.0068 μ F	3.9 K

For data rates above 20 kbps, a more sophisticated low-pass filter may be required for some ETSI bands (868.00 -868.60 MHz, etc.), such as the filter shown in Figure 3.7.2. In this example, an active RC filter is used to implement a 4-pole Bessel low-pass filter. The component values given are for a 26.8 kHz 3 dB bandwidth, which is suitable for a 50 kbps data rate. The Bessel transfer function is chosen because of its relatively flat group delay. The ASH radio must be operated in the ASK transmit mode at this data rate. R8 should be chosen for the peak transmit output power desired. See the individual device data sheets for recommended resistance values.

**Active R-C TXMOD Low-Pass Filter,
4 Pole Bessel, 26.6 kHz 3 dB BW,
50 kbps Data Rate**

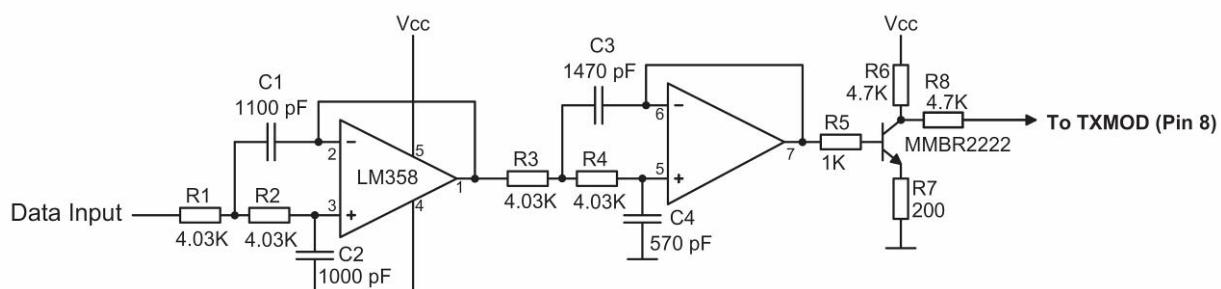


Figure 3.7.2

3.8 ASH Radio RSSI Circuits

A received signal strength indication (RSSI) can be readily derived from Pin 5 of an ASH receiver or transceiver. Under no-signal conditions, the DC value at Pin 5 is about 1.5 volts. When a signal is received, the voltage at Pin 5 increases 10 mV/dB. When DC-balanced data encoding is used, a 5mV/dB DC change will be observed by low-pass filtering the received data stream at the output of Pin 5. The log detector driving Pin 5

saturates at about 450 mV, providing a 225 mV “full scale” DC change at the output of the low-pass filter.

Figure 3.8.1 shows the basic ASH radio RSSI circuit. The best R-C time constant depends on the data rate, packet length and the analog-to-digital converter (ADC) input impedance. If the ADC input impedance is high and your shortest transmitted packet has at least 100 bits including the CBBO training preamble, start with an R-C time constant 20% to 35% of the transmission time of your shortest transmitted packet. Make the RSSI measurement at or near the end of the packet, so that the DC value at the output of the low-pass filter has maximum time to settle. If you are sending packets shorter than 100 bits, set the R-C time constant for the best trade-off between the residual ripple from the data pattern and the DC transient settling time of the filter. Resistor R should not be less than 50 kilohms, with a value of 100 kilohms to 470 kilohms preferred.

Basic ASH Radio RSSI Circuit

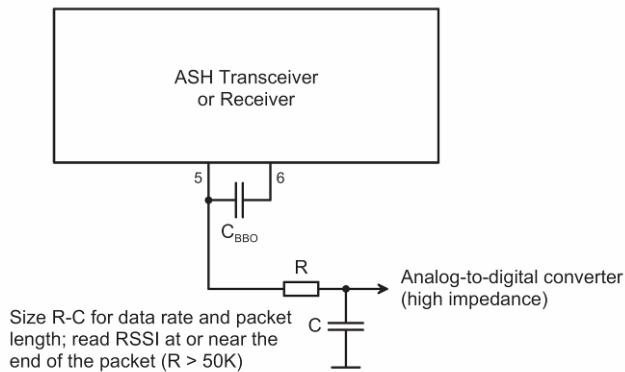


Figure 3.8.1

The no-signal DC value at Pin 5 can vary ± 250 mV due to unit-to-unit variations, temperature drift and supply voltage drift. When using the circuit in Figure 3.8.1, the RSSI software routine must track the no-signal DC value at Pin 5 for calibration purposes. Unless packet activity is very dense, the no-signal DC value will be the lowest DC value seen at the output of the low-pass filter over several hundred R-C time constants.

Figure 3.8.2 shows an op amp RSSI circuit implementation. The no-signal DC value seen at the cathode of D1 is close to 24.4% of the DC supply voltage. If the supply voltage is

Op Amp ASH Radio RSSI Circuit

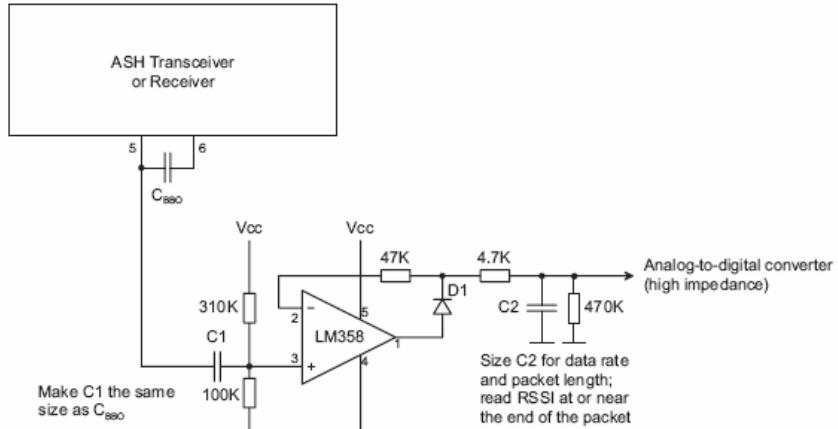


Figure 3.8.2

regulated, the requirement for the RSSI software to track the no-signal DC value is relaxed. The op amp circuit acts as a fast attack/slow decay peak detector. The attack time constant is close to $4.7K \times C_2$, and the decay time constant is close to $470K \times C_2$. Again the RSSI measurement should be made at or near the end of the received packet to allow the transients in the circuit to settle. The decay time constant must be short enough to allow the preamble training transient at C1 to settle before the ADC measurement. This is usually not an issue unless the decay time constant is very large or the packet payload is very small.

Note that since the receiver includes AGC, the detected signal level at Pin 5 will “fall back” when the AGC engages at approximately -50dBm input.

3.9 ASH Radio Performance Curves

Third-generation ASH radios are capable of operating over a supply voltage range of 2.2 to 3.7 Vdc from -40 to +85 °C. Typical performance curves for operation from 2.2 to 3.7 Vdc are presented in this section. Curves in Figures 3.9.2 – 3.9.7 are given for transmitter and receiver performance for encoded data rates of 4.8, 19.2 and 115.2 kbps. Transmitter output power for levels of modulation drive current are also given.

Refer to Figure 3.9.1 for details of the test circuits schematic used for characterization. Note that receiver sensitivity is given for a bit error rate (BER) of 10E-3, which is the most commonly used sensitivity reference for short-range radio applications. Two test methods are in common use for making short-range radio sensitivity measurements, the “100% AM” (or 99% AM) test method, and the “OOK Pulse” test method. The “100% AM” test method starts with a unmodulated (CW) signal level and then applies the data to the signal with amplitude modulation. The modulation swings the signal voltage almost $\pm 100\%$ of the CW level. The “OOK Pulse” test method starts with a CW signal level and “chops” the signal with the data stream. The signal voltage swings between the CW level

and almost zero. For both test methods a “0” bit swings the signal voltage to almost zero. However, the “100% AM” test method swings the signal voltage to almost twice the CW level for a “1” bit in contrast to the “OOK Pulse” method which sets the signal voltage to just the CW level. For this reason, the “100% AM” test method will make any OOK/ASK receiver look 6 dB more sensitive than the “OOK Pulse” test method. The “100% AM test” method is more commonly used because many RF signal generators do not include provisions for pulse modulation.

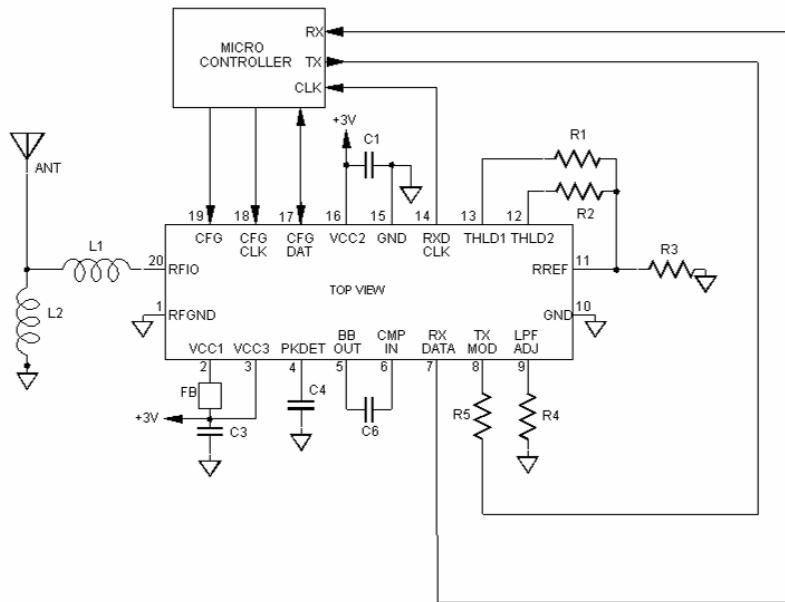


Figure 3.9.1

TR8100/TR8000 Transceiver Set-Up, 3.0 Vdc, -40 to +85 °C

Item	Symbol	OOK	OOK	OOK	ASK	Units	Notes
Encoded Data Rate	DRNOM	2.4	4.8	19.2	115.2	kb/s	see pages 1 & 2
Minimum Signal Pulse	SPMIN	416.66	208.32	52.08	8.68	μs	single bit
Maximum Signal Pulse	SPMAX	1666.66	833.28	208.32	34.72	μs	4 bits of same value
PKDET Capacitor	C4	.047	.022	.0056	820 pF	μF	±10% ceramic
BBOUT Capacitor	C6	.022	0.01	0.0027	390 pF	μF	±10% ceramic
TXMOD Resistor	R5	6.2	6.2	6.2	6.2	K	±5%, for 10 dBm output
LPFADJ Resistor	R4	470	470	160	24	K	±5%
RREF Resistor	R3	100	100	100	100	K	±1%
THLD2 Resistor	R2	-	-	-	*100	K	±1%, typical values
THLD1 Resistor	R1	20	20	20	20	K	±1%, typical values
DC Bypass Capacitor	C1	4.7	4.7	4.7	4.7	μF	tantalum
RF Bypass Capacitor	C3	27	27	27	27	pF	±5% NPO
Series Tuning Inductor	L1	15	15	15	15	nH	50 ohm antenna
Shunt Tuning/ESD Inductor	L2	100	100	100	100	nH	50 ohm antenna
RF Bypass Bead	FB	Fair-Rite	Fair-Rite	Fair-Rite	Fair-Rite		2506033017YO or equivalent

*if transmitted signal is bandwidth limited

TR8000/8001/8100 Transmitter Performance

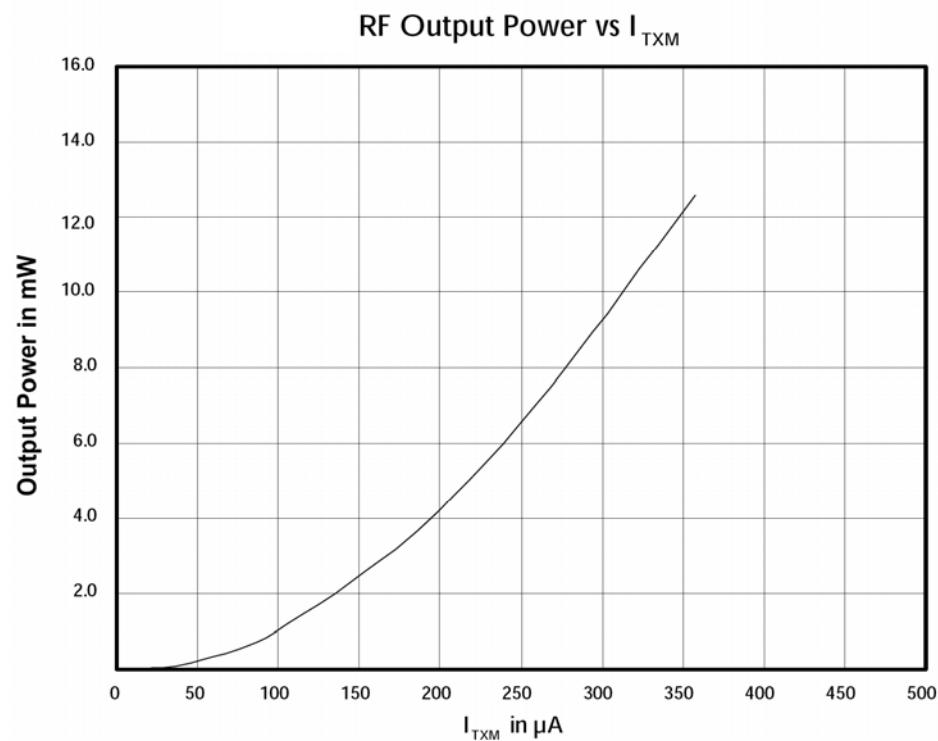


Figure 3.9.2

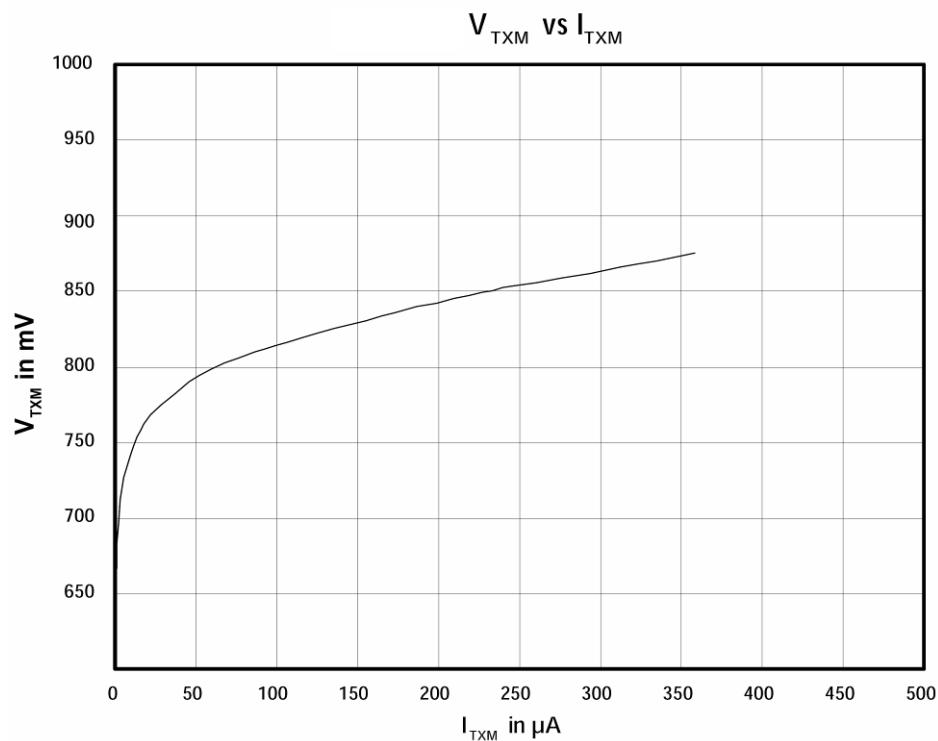


Figure 3.9.3

TR7000 Transmitter Performance

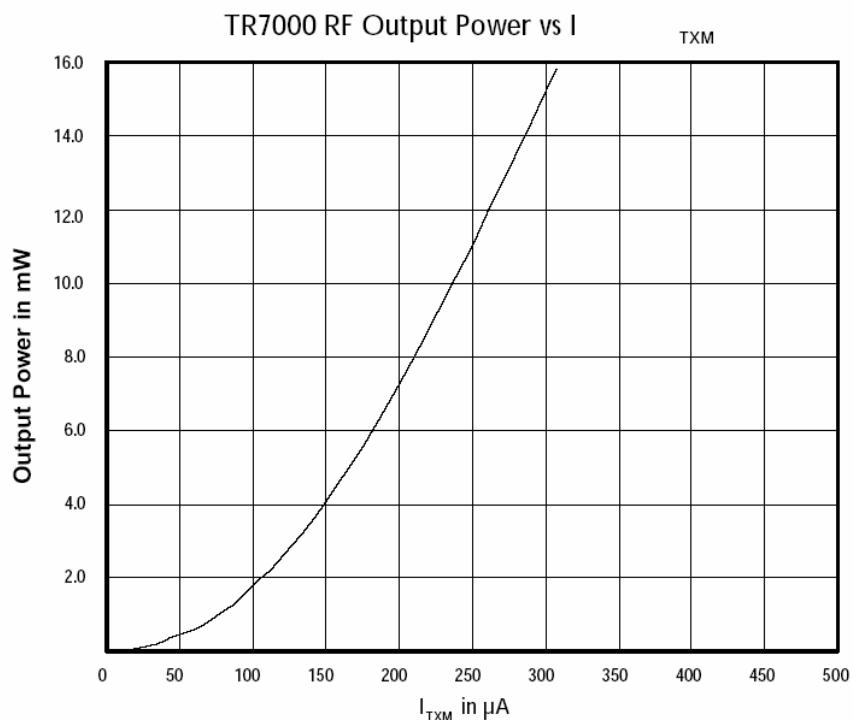


Figure 3.9.4

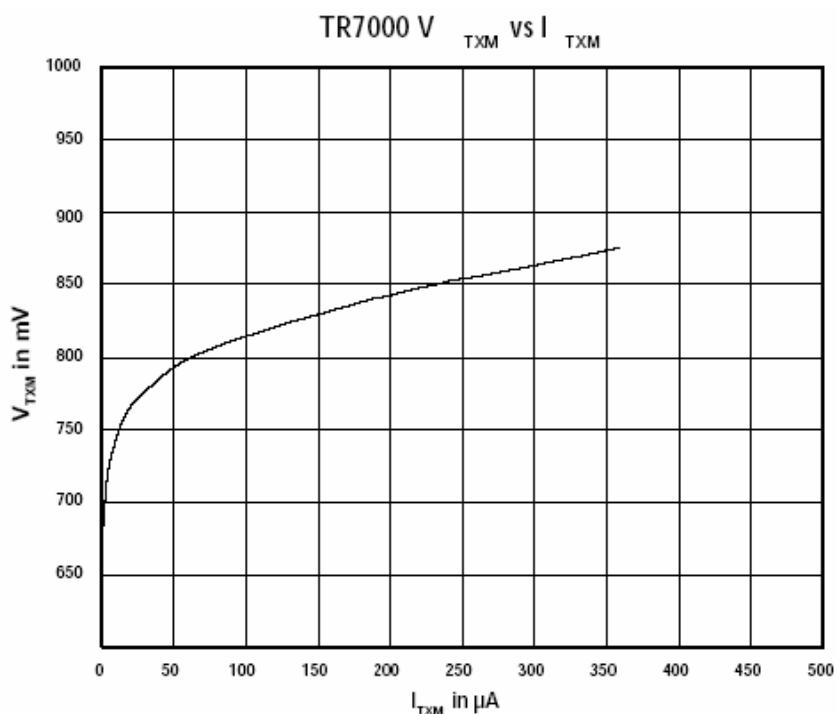


Figure 3.9.5

TR8000/8001/8100/7000 Receiver Performance

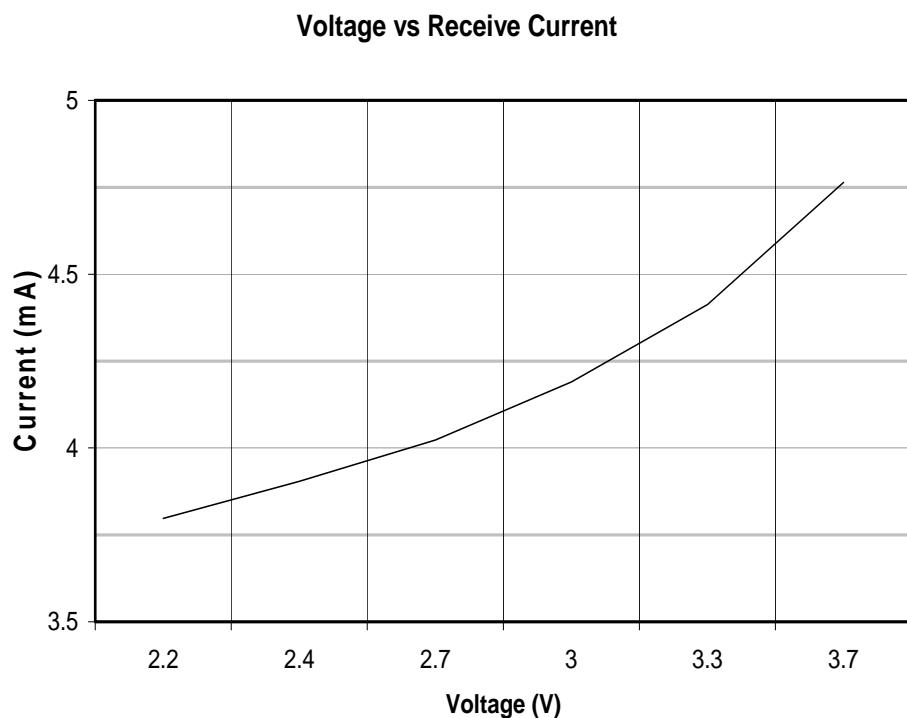


Figure 3.9.6

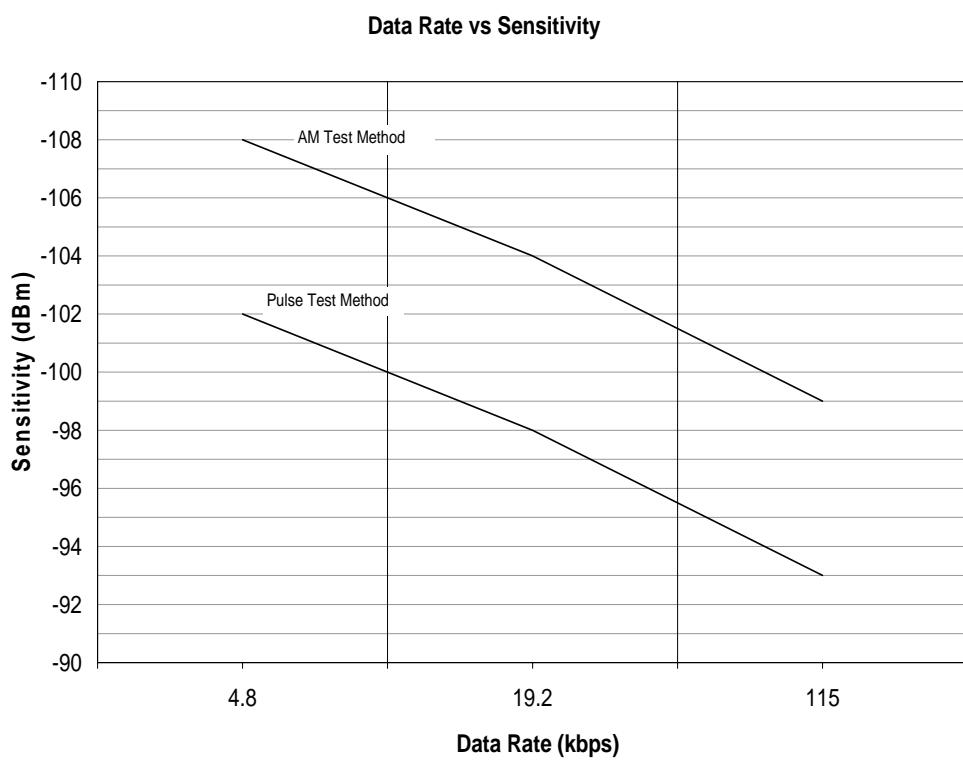


Figure 3.9.7

4.0 FCC/ETSI Field Strength Conversion Formulas

uV/m to dBm = $10 \log (3xE^2) - 100$ [dBm] (with E in uV/m)

dBuV to dBm = dBuv – 107 [dBm]

dBm to dBuV = dBm + 107 [dBuV]

-50000uV/m = -1.25 dBm = 750uW

-1mW = 0dBm = 57735 uV/m

mW to dBm = $10 \log (XmW/1mW)$ [dBm]

dBm to mW = $10^{(dBm/10)}$ [mW]

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Revision History

Rev	Date	Description
-	2/13/2007	Initial Release