INTERPRETATION OF DATA CONVERTER ACCURACY SPECIFICATIONS

Cognizance of accuracy factors involved when interfacing data converters into system applications permits designers to meet overall error budget constraints. Transfer functions; quantization noise; offset, gain, and linearity errors; and temperature effects must be interpreted to satisfy specification requirements

Analog-to-digital and digital-to-analog converters are widely utilized to interface between the physical world of analog measurements and the computational world of digital computers. Dating from the early 1950s, the application of data converters has increased enormously as the use of minicomputers and microcomputers has grown. Typical applications of data converters involve the areas of process control and measurement where the inputs and outputs of the system must be in analog form, yet the computation and control functions are performed digitally. In such a system, input variables such as temperature, flow, pressure, and velocity must be converted into electrical form by a transducer, then amplified and converted into digital form by an analog-to-digital converter for the computer to process.

Since the computer not only measures and determines the state of a process, but also controls it, its computations must be employed to close the loop around the system. This is done by causing the computer to actuate inputs to the process itself, thus controlling its state. Because the actuation is done by analog control parameters, the output of the digital computer must be converted into analog form by a digital-to-analog converter. Such a closed loop feedback control system is shown in Fig 1.

Interfacing by analog-to-digital (A-D) and digital-to-analog (D-A) converters performs a vital role. At the present time, it is estimated that at least 15% of all microcomputers function in such control and measurement applications where data converters are required; this percentage is expected to grow to about 40% within a few years. For the designer of such computer controlled systems, it is fortunate that a broad choice of data converters exists. In fact, a virtual supermarket of A-D and D-A converters of all prices, sizes, and performance specifications is available. This spectrum of converters encompasses those from simple 8-bit monolithic devices costing a few dollars, through better performing hybrid devices with higher resolution, to higher cost discrete module converters with the best performance characteristics.

Design selection involves not only price and size, but also many facets of performance: resolution, linearity, temperature coefficient, speed, and various self-contained options. In the realm of A-D converters (ADCs), there is also the choice between basic conversion methods, such as successive approximation, dual-slope integrating, and parallel (or flash) techniques. Furthermore, there exists a choice between three competing technologies: monolithic, hybrid, and modular, each with its own specific advantages. Since A-D and D-A converters are basically analog circuits that have digital inputs or outputs, the computer systems engineer who may be mostly familiar with digital techniques must become familiar

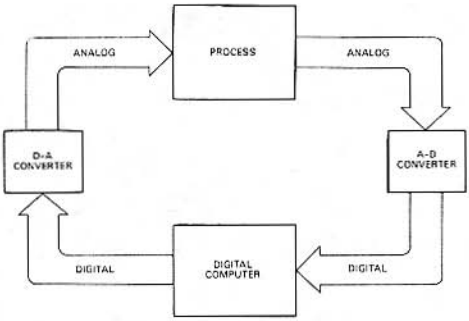

Fig 1 Computer controlled feedback control system. Computer closes loop around process to control its state. However, two interfaces are required: A-D converter and D-A converter

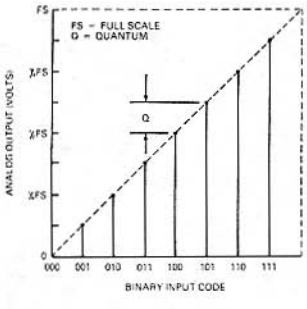

Fig 2 Ideal DAC transfer function. This I/O graph is shown for 3-bit DAC which has one-to-one correspondence between input and output

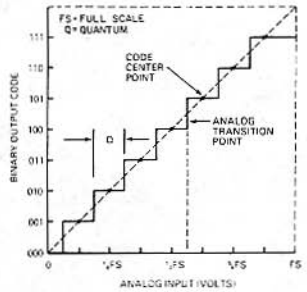

Fig 3 Ideal ADC transfer function. I/O graph illustrates 3-bit ADC which has quantized characteristic

with the many analog specifications describing data converter performance in order to choose the correct converter for a specific requirement.

Data Converter Transfer Functions

Fig 2 shows the transfer function of an ideal 3-bit D-A converter (DAC). This converter is assumed to be of the parallel type, as are virtually all DACs in use today. A parallel DAC responds simultaneously to all digital input lines whereas a serial DAC responds sequentially to each digital input. The transfer function representing a 3-bit DAC is a discontinuous function; its analog output voltage or current changes only in discrete analog steps, or quanta, rather than continuously. However, a one-to-one correspondence exists between the binary input code and the analog output value. For each input code there is one, and only one, possible output value. Analog step magnitude, or quantum, is shown as Q.

The horizontal axis is the input binary code, in this case a 3-bit code, increasing from 000 to 111. The number of output states, or quanta, is 2^n, where n is the number of bits in the code. For a 3-bit DAC, the number of states is 2^3 or 8; for a 12-bit DAC, the number of states is 2^{12} or 4096.

Fig 3 illustrates the transfer function for an ideal 3-bit ADC. This transfer function is also discontinuous but without the one-to-one correspondence between input and output. An ADC produces a quantized output from a continuously variable analog input. Therefore, each output code word corresponds to a small range (Q) of analog input values. The ADC also has 2^n output states and $2^n - 1$ transition points between states; Q is the analog difference between these transition points.

For both ADCs, Q represents the smallest analog difference that the converter can resolve. Thus, it is the resolution of the converter expressed in analog units. Resolution for an A-D or D-A converter, however, is commonly expressed in bits, since this defines the number of

TABLE 1

Summary of Data Converter Characteristics

Resolution (n)	States (2^n)	Binary Weight (2^{-n})	Q for 10 V FS	S/N Ratio (dB)	Dynamic Range (dB)	Max Output for 10 V FS (V)
4	16	0.0625	0.625 V	34.9	24.1	9.3750
6	64	0.0156	0.156 V	46.9	36.1	9.8440
8	256	0.00391	39.1 mV	58.9	48.2	9.9609
10	1024	0.000977	9.76 mV	71.0	60.2	9.9902
12	4096	0.000244	2.44 mV	83.0	72.2	9.9976
14	16384	0.0000610	610 μV	95.1	84.3	9.9994
16	65536	0.0000153	153 μV	107.1	96.3	9.9998

states of the converter. A converter with a resolution of 12 bits, then, ideally resolves 1 part in 4096 of its analog range.

For an ideal ADC or DAC, Q has the same value anywhere along the transfer function. This value is $Q = FSR/2^n$, where FSR is the converter's full-scale range—the difference between the maximum and minimum analog values. For example, if a converter has a unipolar range of 0 to 10 V or a bipolar range of −5 to 5 V, FSR in both cases is 10 V. Q is also referred to as one least significant bit (LSB), since it represents the smallest code change the converter can produce, with the last bit in the code changing from 0 to 1 or 1 to 0.

Notice in the transfer functions of both A-D and D-A converters that the output never reaches full scale. This results because full scale is a nominal value that remains the same regardless of the resolution of the converter. For example, assume that a DAC has an output range of 0 to 10 V; then 10 V is nominal full scale. If the converter has an 8-bit resolution, its maximum output is 255/256 x 10 V = 9.961 V. If the converter has 12-bit resolution, its maximum output voltage is 4095/4096 x 10 V = 9.9976 V.

In both cases, maximum output is one bit less than indicated by the nominal full-scale voltage. This is true because analog zero is one of the 2^n converter states; therefore, there are only $2^n - 1$ steps above zero for either an A-D or D-A converter. To actually reach full scale would require $2^n + 1$ states, necessitating an additional coding bit. For simplicity and convenience then, data converters always have the analog range defined as nominal full scale rather than actual full scale for the particular resolution implemented.

In the transfer functions of Figs 2 and 3, a straight line is passed through the output values in the case of the DAC and through the code center points in the case of the ADC. For the ideal converter, this line passes precisely through zero and full scale. Table 1 summarizes the characteristics of the ideal A-D or D-A converter for the most commonly applied resolutions.

Quantization Noise and Dynamic Range

Even an ideal A-D or D-A converter has an irreducible error, which is quantization uncertainty or quantization noise. Since a data converter cannot distinguish an analog difference less than Q, its output at any point may be in error by as much as $\pm Q/2$.

Fig 4(a) shows an ideal ADC and an ideal DAC that digitize and then reconstruct an analog slow-voltage ramp signal. The ADC and output register are both triggered together so that the DAC is updated in synchronism with the A-D conversions. The DAC output ramp is identical with the analog input ramp except for the discrete steps in its output (not counting time delay). If the output ramp is subtracted from the input ramp as shown, the difference is the quantization noise—a natural result of the conversion process. This noise [Fig 4(b)] is simply the difference between the transfer function and the straight line shown in Fig 3. Quantization noise from an ideal conversion is therefore a triangular waveform with a peak-to-peak value of Q.

As with most noise sources, the average value is zero, but the rms value is determined from the triangular shape to be E_n (rms) $= Q/\sqrt{12}$. Thus, a data conversion system can be thought of as a simple signal processor that adds noise to the original signal by virtue of the quantization process. Since this noise is an inherent part of the conversion process, it cannot be eliminated except with a converter of infinite resolution. The best that can be done, even with ideal converters, is to reduce it to a level consistent with desired system accuracy. This is done by using a converter with sufficiently high resolution.

In many computerized signal processing applications, it is necessary to determine the signal-to-noise (S/N) ratio, which is a power ratio expressed in decibels. It can be found from the ratio of peak-to-peak signal to rms noise as follows.

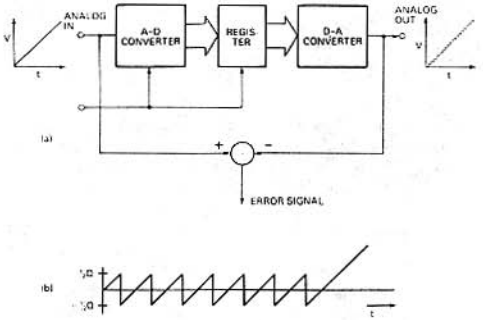

Fig 4 Signal digitization and reconstruction (a) and quantization noise (b). Quantization noise is shown as difference between input and output for ideal data conversion system

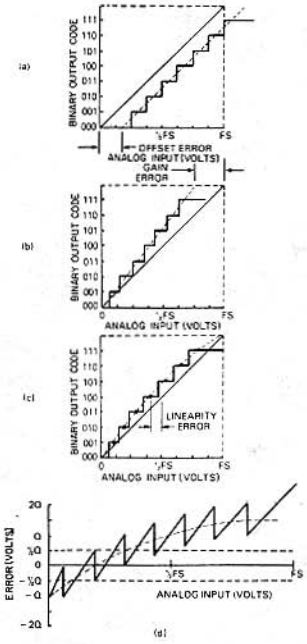

Fig 5 Errors in nonideal A-D converters. Transfer functions are shown for ADCs with offset error (a), gain error (b), and linearity error (c). ADC with all three errors present will have quantization error as shown in (d)

$$\text{S/N Ratio (dB)} = 10 \log \left[\frac{2^n Q}{Q/\sqrt{12}}\right]^2 = 20 \log 2^n + 20 \log \sqrt{12}$$
$$= 6.02n + 10.8 \qquad (1)$$

The S/N ratio increases by a factor of about 6 dB for each additional bit of resolution.

Dynamic range of a data converter, another useful term, is found from the ratio of FSR to Q. This ratio is the same as the number of converter states.

$$\text{Dynamic Range (dB)} = 20 \log 2^n = 20n \log 2 = 6.02n \qquad (2)$$

Therefore, simply multiplying the number of bits of resolution by 6 dB gives the dynamic range. S/N ratio and dynamic range are summarized for the most popular resolutions in Table 1.

Nonideal Data Converters

Real A-D and D-A converters exhibit a number of departures from the ideal transfer functions just described. These departures include offset, gain, and linearity errors (Fig 5), all of which appear simultaneously in any given data converter. In addition, the errors change with both time and temperature. In Fig 5(a), the ADC transfer function is shifted to the right from the ideal function. This offset error is defined as the analog value by which the transfer function fails to pass through zero; it is generally specified in millivolts or in percent of full scale.

In Fig 5(b), the converter transfer function has a slope difference from the ideal function. This gain, or scale factor, error is defined as the difference in full-scale values between the ideal and actual transfer functions when the offset error is zero; gain error is expressed in percent.

An ADC transfer function in Fig 5(c) exhibits linearity error, a curvature from the ideal straight line. Linearity error, or nonlinearity, is the maximum deviation of the transfer function from a straight line drawn between zero and full scale; it is expressed in percent or in LSBs (such as ±½ LSB). Fig 5(d) shows the total error of a nonideal

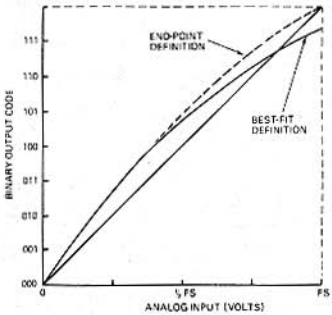

Fig 6 Comparison of linearity error definitions. Curves illustrate end-point and best-fit definitions of linearity error in an ADC

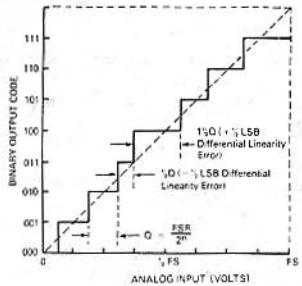

Fig 7 Definition of differential linearity error. This transfer function illustrates ±½ LSB differential linearity errors. Differential linearity error of zero means that every step in transfer function has size of precisely Q

ADC, which contains offset, gain, nonlinearity, and quantization errors. Compare this curve with that of Fig 4(b).

Fortunately, most A-D and D-A converters on the market today have provision for trimming out the initial offset and gain errors. By means of two simple external potentiometer adjustments, the offset and gain errors can be virtually reduced to zero or within the limits of measurement accuracy. Then, only the linearity error remains.

Nonlinearity

Linearity error is the most difficult error to deal with since it cannot be eliminated by adjustment. Like quantization error, it is an irreducible error. Basically, there are just two methods to reduce linearity error, both of which are expensive: either use a higher quality converter with better linearity, or perform a digital error correction routine on the data using a computer. The latter, of course, may not be feasible in many applications. There is some merit in using a more expensive converter, however. For example, suppose that an ultralinear 8-bit ADC is required. Most good quality converters have linearity errors specified to less than ±½ LSB. If a more expensive 12-bit ADC is employed with only 8 output bits used, then its linearity error of ±½ LSB out of 12 bits is the same as ±1/32 LSB out of 8 bits. This converter, therefore, becomes an ultralinear 8-bit ADC and probably at not too great an additional cost.

Actually, two types of linearity errors existing in A-D and D-A converters are integral linearity error and differential linearity error. Integral linearity error in Fig 5(c) is due to the curvature of the transfer function, resulting in departure from the ideal straight line. The definition given for integral linearity error as the maximum deviation of the transfer function from a straight line between zero and full scale is a conservative one used by most data converter manufacturers. It is an "end-point" definition, as contrasted with the normal definition of linearity error as the maximum deviation from the "best-fit" straight line.

Since determining the best-fit straight line for data converters can be a tedious process when calibrating the device, most manufacturers have opted for the more conservative definition. This means that the converter must be aligned accurately at zero and at full scale to realize the specified linearity. The end-point definition can mean a linearity that is twice as good as a best-fit definition, as illustrated in Fig 6. Notice that the curvature may be twice as great with the best-fit straight line definition.

Differential linearity error is the amount of deviation of any quantum from its ideal value. In other words, it is the deviation in the analog difference between two adjacent codes from the ideal value of $FSR/2^n$. If a data converter has ±½ LSB maximum differential linearity error, then the actual size of any quantum in its transfer function is between ½ LSB and 1½ LSB; each analog step is 1 ±½ LSB. Fig 7 illustrates the definition. The first two steps shown are the ideal value $Q = FSR/2^n$. The next step is only ½Q, and above this is 1½Q. These two steps are at the limit of the specification of ±½ LSB maximum differential linearity error. Most data converters today are specified in terms of both integral and differential linearity error. In production testing of data converters, quanta sizes are measured over the converter's full-scale range.

Two other important terms are commonly used in conjunction with the differential linearity error specification. The first is monotonicity, which applies to DACs. A monotonic DAC has an analog output that is a continuously increasing function of the input. The DAC transfer function shown in Fig 8(a) is monotonic even though it has a large differential linearity error. The transfer

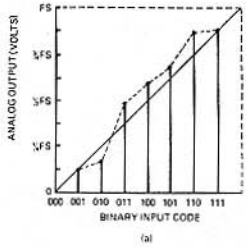

Fig 8 Monotonic (a) and nonmonotonic (b) DAC outputs. Monotonicity means output is continuously increasing function of input

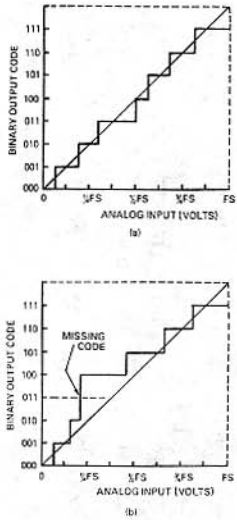

Fig 9 No missing code (a) and missing code (b) in ADC output. Differential linearity error of less than ±1 LSB assures that there are no missing codes in transfer function

function of Fig 8(b), on the other hand, is nonmonotonic since the output actually decreases at one point. In terms of differential linearity error, a DAC may go nonmonotonic if the differential linearity error is greater than ±1 LSB at some point; if the differential linearity error is less than ±1 LSB, it assures that the output is monotonic.

The term missing, or skipped, code applies to ADCs. When the differential linearity error of an ADC is greater than ±1 LSB, the output may have a missing code; if the differential linearity error is less than ±1 LSB, it assures that there are no missing codes. Fig 9(a) shows the transfer function of an ADC with a large differential linearity error but with no missing codes. In Fig 9(b), however, the differential linearity error causes a code to be skipped in the output.

For ADCs, the linearity characteristic depends on the technique of A-D conversion used; each converter type exhibits its own specific nonlinearity characteristic. Fig 10 illustrates the nonlinearity characteristics of the two most popular types of ADCs: successive approximation and dual-slope integrating. With the successive approximation ADC, and also with other feedback type ADCs that use a parallel input DAC in the feedback loop, differential linearity error is the dominant type of nonlinearity. This is due to the parallel input DAC, which is made up of weighted current sources. The worst differential linearity errors occur at the major code transitions, such as ¼, ½, and ¾ scale. If these differential linearity errors are small, then the integral linearity error will also be small.

The difficulty at the major transition points is that, for example, the most significant bit current source is turning on while all other current sources are turning off. This subtraction of currents must be accurate to ±½ LSB and is a severe constraint in high resolution DACs. This means that the weighted current sources must be precisely trimmed in manufacturing. The most difficult transition is at ½ scale, where all bits change state (eg, for an 8-bit converter, 01111111 to 10000000), and the worst differential linearity error generally occurs here.

The next most difficult transitions occur at ¼ scale and ¾ scale, where all but one of the bits change state (eg, for an 8-bit converter, 00111111 to 01000000 and 10111111 to 11000000, respectively). Relatively smaller differential linearity errors may also occur at the ⅛, ⅜, ⅝, and ⅞ scale transitions, and so on. Fig 10(a) shows a successive approximation ADC transfer function, illustrating exaggerated differential linearity errors at ¼, ½, and ¾ scale. If these errors are properly trimmed out in manufacturing, then both differential and integral linearity errors will be less than ±½ LSB.

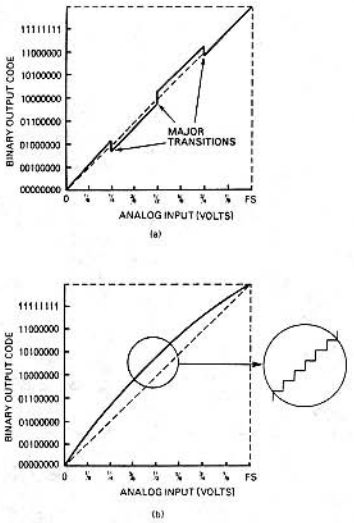

Fig 10 Linearity characteristic of successive approximation (a) and dual slope integrating (b) ADCs. Transfer function of successive approximation converter exhibits mostly differential linearity error while that of integrating converter shows mostly integral linearity error

Fig. 10(b) shows a dual-slope integrating ADC transfer function. In this case, the predominant nonlinearity is the integral linearity error; differential linearity error is almost nonexistent in integrating type ADCs, which also includes charge balancing ADCs. The curvature of the transfer function is caused by a nonideal integrator circuit. Differential linearity is determined by the time between clock pulses in the converter, and this is constant within any conversion cycle.

Temperature Induced Errors

Ambient temperature changes cause variations in offset, gain, and linearity errors. If a converter is operated at a constant temperature within its specified operating temperature range, offset and gain errors can be zeroed by external adjustment at that temperature. But if the converter must operate with changing ambient temperature, then the problem becomes acute.

Offset change with temperature is generally specified in microvolts per degree Celsius, or in parts per million of full scale per degree Celsius. Gain temperature coefficient is specified in parts per million per degree Celsius, and linearity error change with temperature is expressed in parts per million of full scale per degree Celsius.

Effective aproaches to minimizing gain and offset changes with temperature are available. If a converter operates most of the time at a given temperature, then its offset and gain should be zeroed at that temperature. If, however, the ambient temperature varies between two temperatures, the converter should be calibrated midway between those two temperatures. Another approach to minimizing changes with temperature is to use a converter with a low temperature coefficient to meet the desired specification. Data converters with low temperature coefficients are, of course, more expensive, but this may be the most economical solution to the problem when all design factors are considered. Another method of minimizing gain error is based on the fact that many data converters with internal references have provision for connecting an external reference. In such a case, it is possible to connect a lower temperature coefficient external reference to the converter. This can be particularly effective where a number of converters are used together and one reference is used for all of them.

Linearity error temperature coefficient is the most troublesome specification, since it resists correction. In many applications, it is desired that the converter be

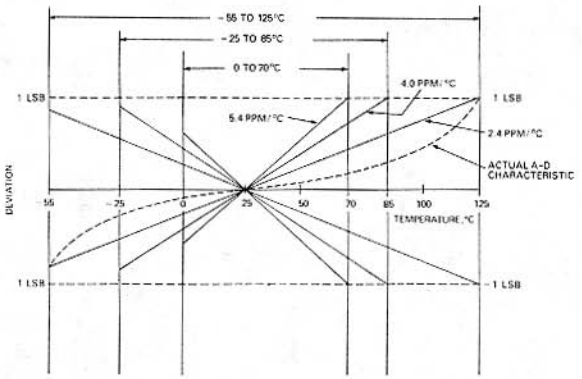

Fig 11 Butterfly gain tempco characteristic for 12-bit ADC with ±1 LSB maximum gain error. Converter is calibrated for zero gain error at 25 °C. Limits shown are for ±1 LSB error out of 12 bits over designated temperature range

monotonic, or have no missing codes, over the desired operating temperature range. From the converter differential linearity temperature coefficient, it is useful to determine the temperature range over which the converter will have guaranteed monotonicity or no missing codes. Using a conservative approach, it is assumed that the converter has a maximum initial differential linearity error of ±½ LSB. Then, if the differential linearity error changes by not more than an additional ½ LSB, a DAC will remain monotonic and an ADC will have no missing codes.

With a 12-bit ADC for example, ½ LSB is equal to 120 ppm. If the operating temperature range is 0 to 70 °C and the converter is calibrated at 25 °C, the maximum temperature change is 70 °C − 25 °C, or 45 °C. To guarantee no missing codes, the differential linearity temperature coefficient must be 120 ppm/45 °C = 2.7 ppm/°C of full scale, maximum. An even lower differential linearity temperature coefficient is required to assure no missing codes if the operating temperature range is the full −55 °C to 125 °C military range. Performing a similar computation gives 120 ppm/100 °C = 1.2 ppm/°C of full scale, maximum, for the differential linearity temperature coefficient.

Gain temperature coefficient is commonly specified by the butterfly limits shown in Fig 11. All the lines pass through zero at 25 °C, where it is assumed that the initial measurement is made. The graph of Fig 11 shows the maximum gain temperature coefficient required for a ±1 LSB gain error for a 12-bit A-D or D-A converter over three different temperature ranges. Observe that the gain deviation curve must be within the bounds shown to meet the specification of ±1 LSB maximum change. The dotted curve shows an actual converter gain deviation that would qualify as a gain temperature coefficient of ±2.4 ppm/°C over the −55 to 125 °C operating temperature range. This represents a very low temperature coefficient for an actual converter since most available devices fall in the range of 5 to 50 ppm/°C.

Error Budget Summary

A common mistake in specifying data converters is to assume that the relative accuracy of a converter is determined only by the number of resolution bits. In fact, achievable relative accuracy is likely to be far different from the implied resolution, depending on the converter specifications and operating conditions. This simply means that the last few resolution bits may be meaningless in terms of realizable accuracy.

The best way to attack this design problem is with a systematic error budget. An error budget partitions all possible errors by source to arrive at a total error. In a given system, this must be done not only for the A-D or D-A converter, but also for the other circuits, such as transducer, amplifier, analog multiplexer, and sample and hold.

As an example, using the accuracy specifications for a typical 12-bit ADC (Table 2), an error budget can be determined based on the following assumptions: operating temperature range of 0 °C to 50 °C, maximum

TABLE 2

Accuracy Specifications for 12-Bit ADC

Characteristic	Value
Resolution	12 Bits
Differential Linearity Error	±½ LSB max
Differential Linearity Tempco	±2 ppm/°C of FSR max
Gain Tempco	±20 ppm/°C max
Offset Tempco	±5 ppm/°C of FSR max
Power Supply Sensitivity	0.002%/%

TABLE 3

Error Budget for 12-Bit ADC

Specification	Error (%)
Quantization Error (±½ LSB)	0.012
Differential Linearity Error (±½ LSB)	0.012
Differential Linearity Error over Temp (2 ppm/°C x 25)	0.005
Gain Change over Temp (20 ppm/°C x 25)	0.05
Zero Change over Temp (5 ppm/°C x 25)	0.0125
Change with Power Supply (1 x 0.002%)	0.002
Long Term Change	0.02
Total Error, Worst Case	0.1135
Total Statistical (rms) Error	0.0581

power supply voltage change of 1% with time and temperature, and maximum converter change of 0.02% with time. Table 3 shows the resulting error budget with a total worst case error of 0.1135%. It is improbable that the errors will all add in one direction. Statistical (rms) addition of the errors yields a lower value of 0.0581%; this, on the other hand, may be too optimistic since the number of error sources is small. At any rate, the maximum error will be somewhere between 0.0581% and 0.1135%, a significant difference from what might be assumed as a 12-bit or 0.024% converter. The ideal relative accuracy has been degraded by one to two resolution bits.

In applying data converters, best results are achieved by reading the data sheet carefully for accuracy specifications, computing total error by the error budget method, and then carefully aligning and testing the converter in its actual application.