




RFIC Design Assistant 4.0 User's Guide





Overview

The RFM RF Design Assistant (RFDA) includes all the functional features of the following RFIC Evaluation Boards:

- DR-TRC101/102-315
- DR-TRC101/102-433
- DR-TRC101/102-868-915
- DR-TRC103-868 
- DR-TRC103-915 
- DR-TRC104-2400 
- DR-RXC101-315
- DR-RXC101-433
- DR-RXC101-868-915
- DR-TXC101-315
- DR-TXC101/102-433
- DR-TXC101/102-868-915

Key Features

- Comprehensive Evaluation of RFIC's
- Individual Parameter Selection
- RS-232 Communication Setup
- Device Selection
- Band Selection
- Center Frequency Setup
- Transmitter Parameter Setup
- Receiver Parameter Setup
- One Click Configuration
- Calibration
- Sleep/Power Down Setup
- Status Register Read
- Example Code Setup
- Load & Save Configurations

Note: The RFDA does not currently include software programmable features for the DR-TXC100-315 and DR-TXC100-433 products. However, the listing for reference schematic and output matching values are included.



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Installation

Go to <http://rfm.com/products/rfic.shtml> and click on the RFDA download link at the bottom of the page. The software will install automatically.

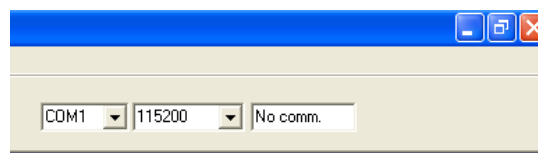
Getting Started

Double click on the RFDA icon and the RF Design Assistant will open to the below screen.

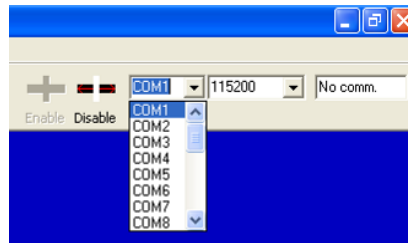


RS-232 Communication Setup

Before continuing, the COM port must be set for communication with the evaluation board. The COM port and Baud Rate selection are located at the top right corner. When the software is first executed, the COM port is automatically connected. To change COM ports simply click on the COM1 drop-down and select the COM port desired. The RFDA automatically disconnects from the current COM port and connects with the new selection. An error message is displayed if the selected COM port is not available.

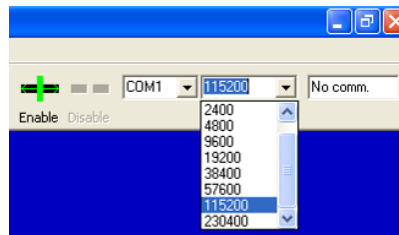


The COM port may be selected from the drop-down box. Select the COM port and it automatically connects. If there is an error with the COM port, an error box will display.



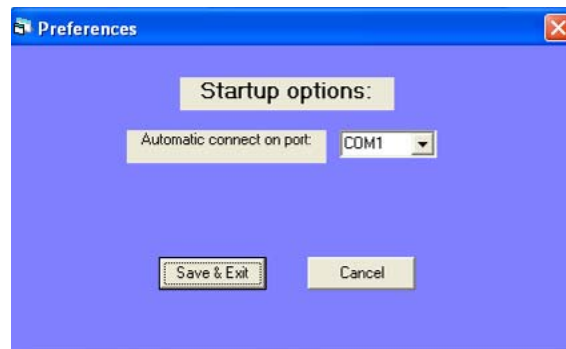
NOTE: The COM port number assignment is limited to a maximum of 16.

The COM port speed may also be configured. Version 1.0 boards operate at 19.2 kb/s. Version 2.0 and later boards all operate at 115.2 kb/s COM rate. Except for the TRC104. To change the COM port speed, select the speed from the drop-down box.



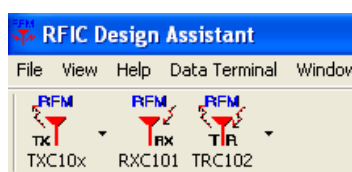
Preferences

The RFDA may be configured to start up and connect to a specific COM port each time the software is executed. COM port startup can be found by clicking File>Preferences.

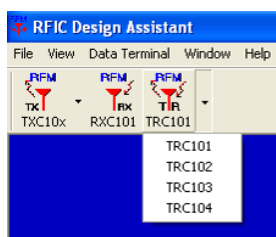


Device Selection

After establishing the correct COM port settings you will need to select the device you wish to evaluate. There are three choices for evaluation: Transmitter (TXC10x), Receiver (RXC101), and Transceiver (TRC10x).

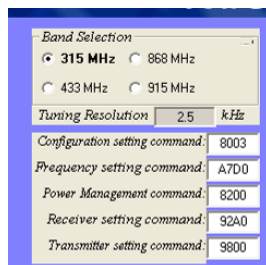


The device is selected by clicking on the arrow to the right of the Toolbar icon and selecting the device from the drop-down box. The TXC100 does not have software programmable features, but is included in the listing for reference schematic and output matching values for the two standard frequency bands.



Band Selection (TXC101/102, RXC101, TRC101/102)

The band of interest must be chosen for the selected evaluation board. Each evaluation board is designed for a particular band of frequencies. If a band is chosen for a board that is not tuned for that band, the performance will suffer.



Note that for the TXC102 and TRC102 there is no 315 MHz Band available.



Center Frequency and Transmit/Receive Parameters Setup

After setting the frequency band, the center frequency can be set. Other parameters related to the transmitter or receiver may be chosen. For the transmitter the modulation bandwidth (FSK deviation), the modulation polarity, or the output power may be set.

For the receiver the base-band bandwidth, LNA gain, or digital RSSI level may be set. Refer to the respective datasheet for detailed information on the individual functions of the transmitter or receiver.



The control above allows changing the frequency on-the-fly. Click the Automatic Update button to enable the new frequency value to be sent to the device without having to click on the Update button at the bottom. This is beneficial for evaluating frequency alignment. Each click of the arrow will move the frequency one resolution tick.

Center frequency	433.92 MHz	<div>↑ ↓</div> <div>Automatic Update</div>
Crystal load	10.0 pF	
LNA gain	max.	
DRSSI	-103 dBm	
Baseband bandwidth	67 kHz	
Valid Data Detector	Slow	
FSK Deviation (Δf)	15 kHz	
Pout	Pmax	
Polarity of mod	fo + df	
Synch Char. Byte	D4	
Clock Buffer Slew	>5 MHz	

Enable Functions

Once the initial parameters have been set, the desired function may be enabled.

<input type="checkbox"/> Enable the receiver <input type="checkbox"/> Enable receiver baseband <input type="checkbox"/> Enable the wake-up timer <input type="checkbox"/> Enable the low battery detector <input type="checkbox"/> Disable the clock output <input type="checkbox"/> Enable the synthesizer <input type="checkbox"/> Enable the oscillator <input type="checkbox"/> Enable the transmitter <input type="checkbox"/> Enable TX Register <input type="checkbox"/> Enable RX FIFO <hr/> Fm8 function <input checked="" type="radio"/> Interrupt input <input type="radio"/> Data Detector output <hr/> <input type="checkbox"/> Xal Low Power on <input type="checkbox"/> PLL Dithering <input type="checkbox"/> PLL BW/Data Rate >90Kbs
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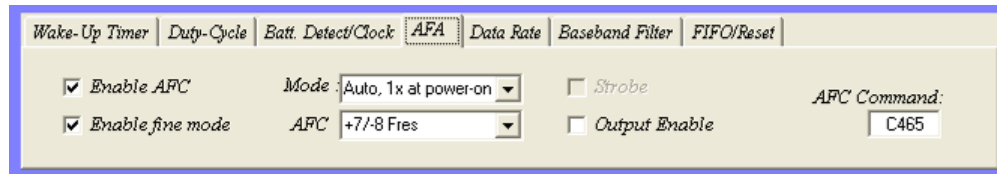
Send Configuration Data - One Click Configuration

To send the configuration packet to the RFIC, simply click on the Update button. After an update, a calibration must be performed to lock in the PLL and synthesizer functions.

NOTE: A calibrate must be performed after every frequency band change.

Update needed >>>	Update	Calibrate >>> (after update)	Calibrate Synthesizer
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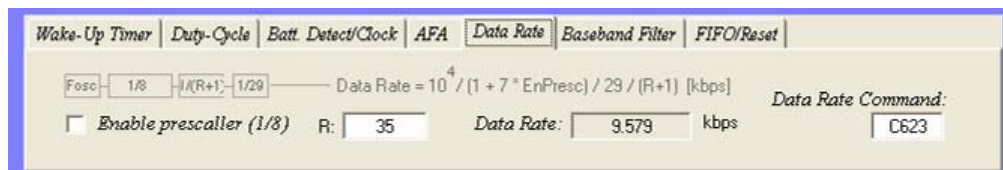
The AFA setup tab configures the offset between the receiver center frequency and the remote transmitter center frequency.



The screenshot shows the 'AFA' tab selected. It contains the following controls:

- ☒ Enable AFC
- Mode: Auto, 1x at power-on
- ☐ Strobe
- ☒ Enable fine mode
- AFC: +7/-8 Fres
- ☐ Output Enable
- AFC Command: C465


The data rate configuration tab allows for easy setting of the expected data rate. This may be used to quickly find the correct digital value for the associated data rate.



The screenshot shows the 'Data Rate' tab selected. It contains the following controls:

- Fosc: 1/8
- 1/(R+1): 1/29
- Data Rate = $10^4 / (1 + 7 * \text{EnPresc}) / 29 / (R+1)$ [kbps]
- ☐ Enable prescaler (1/8)
- R: 35
- Data Rate: 9.579 kbps
- Data Rate Command: C623

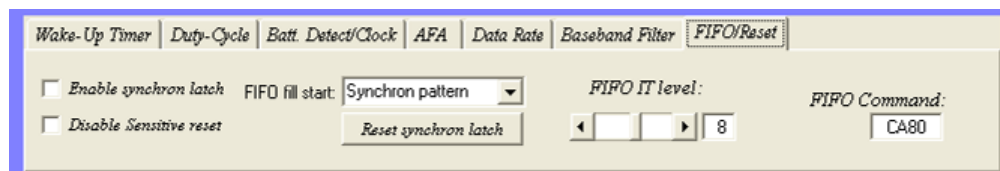
The base-band data filter configuration tab sets the type of filter to be used for base-band reception. The clock recovery is also included in this command word, as well as the data quality detector threshold parameter.



The screenshot shows the 'Baseband Filter' tab selected. It contains the following controls:

- Clock Recovery: Slow
- Filter type: Digital LPF
- DQD parameter: 4
- Data filter Command: C22C

The receive FIFO tab configures the FIFO fill condition and fill interrupt level. The receiver FIFO is enabled/disabled thru this tab. Included in this command word is the Reset Mode. It is advised that the reset mode be disabled (box checked). This eliminates the possibility of a reset on a supply line glitch.

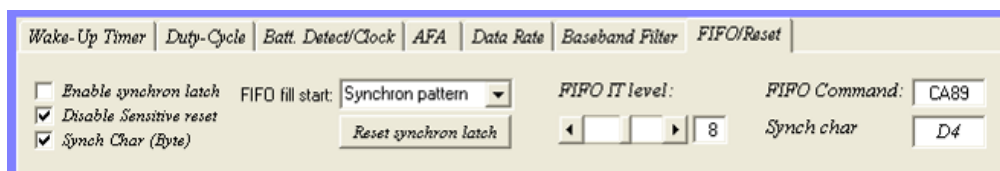


The screenshot shows the 'FIFO/Reset' tab selected. It contains the following controls:

- ☐ Enable synchron latch
- FIFO fill start: Synchron pattern
- ☒ Disable Sensitive reset
- Reset synchron latch
- FIFO IT level: 8
- FIFO Command: CA80

TRC101

The TRC102 has the added feature of the programmable sync character. The sync character may also be assigned as byte long (shown below) or word long.



The screenshot shows the 'FIFO/Reset' tab selected. It contains the following controls:

- ☐ Enable synchron latch
- FIFO fill start: Synchron pattern
- ☒ Disable Sensitive reset
- ☒ Synch Char (Byte)
- Reset synchron latch
- FIFO IT level: 8
- FIFO Command: CA89
- Synch char: D4

TRC102

The Low Battery Detector tab configures the threshold for a low battery indication. The buffered crystal clock frequency may also be set with the command.

Wake-Up Timer	Duty-Cycle	Batt. Detect/Clock	AFA	Data Rate	Baseband Filter	FIFO/Reset
The Low Battery Detector can be enabled by the Power Management command.			$V_{lb} = 2.2 + V \cdot 0.1 [V]$		Low Battery Detector C' Clock Divider	
μC CLK: 1 MHz	V: 0	V_{lb} : 2.2 V	C000			

Sleep/Power Down Setup

The wake-up timer may be configured through the wake-up timer tab. This may serve as a convenient way to determine the digital values to set the desired wake-up time. Clicking on Status Read after a wake-up period will show the interrupt asserted indicating a wake-up interrupt.

NOTE: When the wake-up timer is enabled and the wake-up time period expires, the wake-up timer must first be disabled, updated, and then re-enabled (and updated) to initiate another wake-up period.

Wake-Up Timer	Duty-Cycle	Batt. Detect/Clock	AFA	Data Rate	Baseband Filter	FIFO/Reset
The Wake-up timer can be enabled by the Power Management command.			$Time = M \cdot 2^R [ms]$		Wake-Up Timer Command:	
M: 150	R: 1	Time: 0.3 sec	E196			

The low duty cycle tab configures the on-time of the receiver after a wake-up period has expired. This may serve as a convenient way to determine the digital values to set the desired duty cycle time.

Wake-Up Timer	Duty-Cycle	Batt. Detect/Clock	AFA	Data Rate	Baseband Filter	FIFO/Reset
<input type="checkbox"/> Enable Low Duty-cycle operation			$Duty\ cycle = (D \cdot 2 + 1) / M \cdot 100 [\%]$		Duty-Cycle Command:	
M: 150	D: 7	Duty cycle: 10 %	C80E			

Status Register Read

Clicking the Read Status button reads the status bytes via the SPI interface from the IC and sets the status bits. If a logic '1' is read the indicator turns yellow, otherwise it remains grey. If a bit is active low, the bit will stay yellow to indicate no activity.

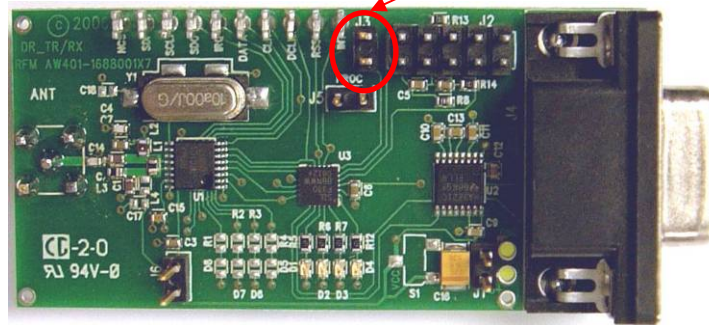
Read Status	RGIT	POR	RGUR	WK-UP	EXT	LBD	Transmitter-receiver carrier frequency offset:			
Status: FF EM	ATS	DQD	CRL	ATGL	SGN	OF3	OF2	OF1	OF0	kHz

Note that for the TRC101 transceiver IC, when you enable the receiver, the related status bits change automatically. Observe the differences in the transmitter status bit names above versus the receiver status bit names below.

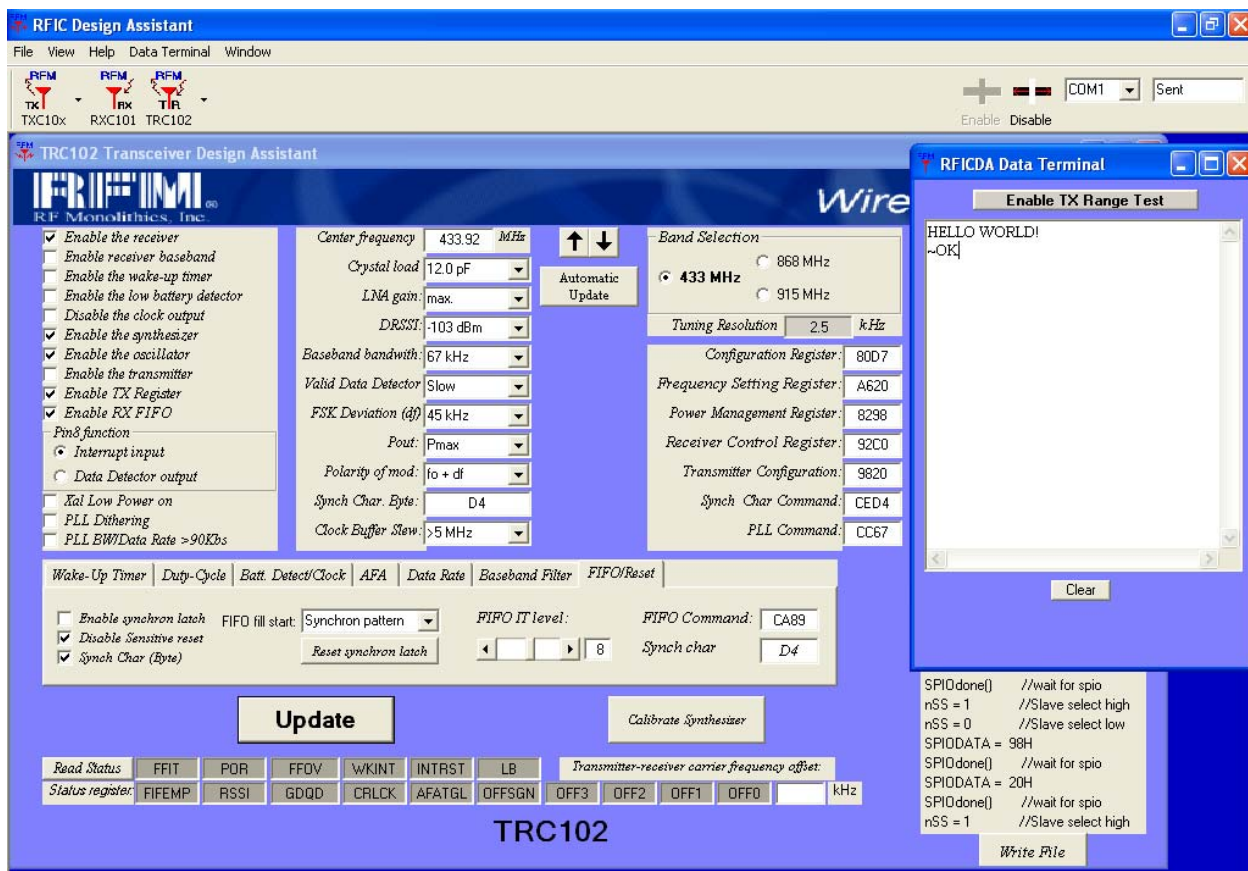
Read Status	FFIT	POR	FFOV	WK-UP	EXT	LBD	Transmitter-receiver carrier frequency offset:			
Status: FF EM	RSSI	DQD	CRL	ATGL	SGN	OF3	OF2	OF1	OF0	kHz

Data Terminal

Install jumper J3 and re-apply power.

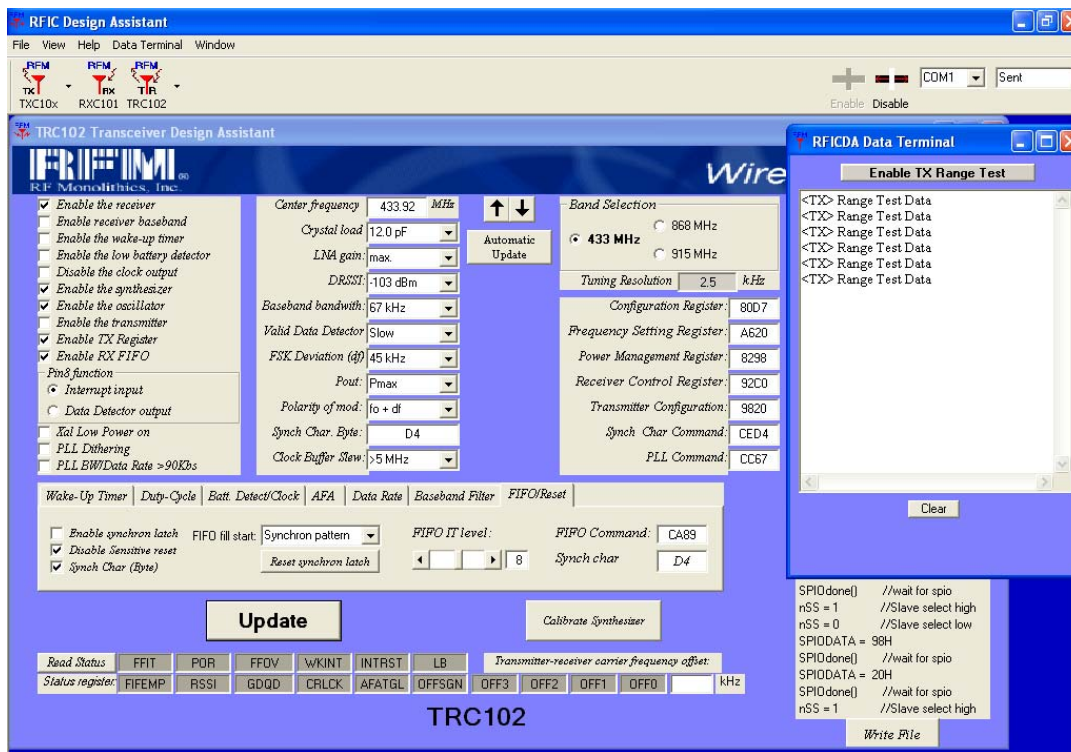


NOTE: No jumper needed for TXC10x DR boards

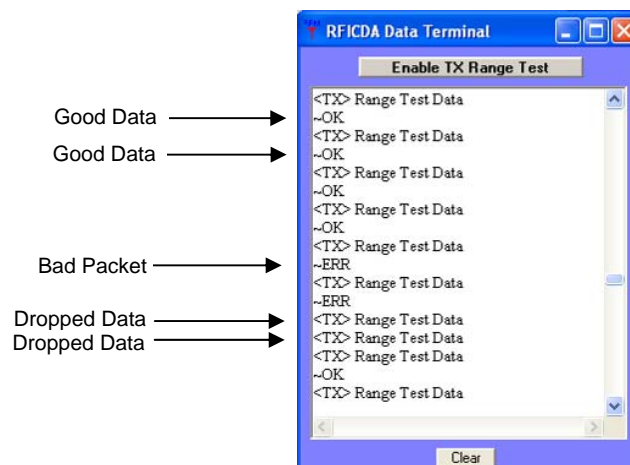


The Data Terminal may be used to transmit short packets of data to another evaluation unit. The data packets are limited to 32 bytes. Packets may be sent with data rates up to 50 kbps.

Range Test



The evaluation unit can be coupled with another unit to conduct a range test. One unit may be configured as a stationary device with the RFDA. The other unit may be configured as a mobile device which can be relocated. The mobile device receives a packet, verifies the packet, then transmits an ACK (~OK) or NACK (~ERR) signal back to the stationary device.





Quick Start for Data Terminal or Range Test (TRC10x & RXC101)

This will require two DR evaluation boards and two PC's.

- 1) Install the jumper at J3.
- 2) Connect board to +3 V and the RS232 cable.
- 3) Start the RFDA software and select the device to configure.
- 4) Configure both boards as follows:

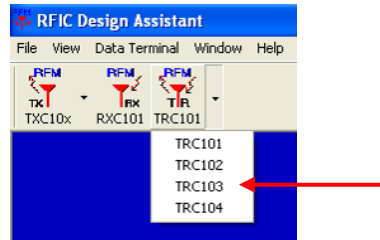
Enable Receiver
Enable TX Register
Enable RX FIFO
Crystal Load = 12 pF
LNA Gain = max
Baseband BW = 67 kHz
Valid Data Detect = Slow
FSK Deviation = 45 kHz
Polarity of Mod = fo + df
AFC:
Enable AFC
Enable Fine Mode
Output Enable
Mode = Auto, drop Foffset
AFC = +15/-16*Fres
Data Rate:
Enable Prescaler
R = 17 (2.4 kbps)
Data Filter: (use defaults)
FIFO Buffer:
Enable Synch Latch
Disable Sensitive Reset
FIFO Fill Start = Sync Pattern
FIFO IT level = 8

- 5) Click the "Update" button and "Calibrate" button.
- 6) Configure the other board as above.
- 7) Open the Data Terminal Window on both PC's.
- 8) When both are configured and calibrated, press the "Enter" key a couple of times on either PC and observe an "~OK" in the terminal window. This shows the units are aligned and ready to transfer data.

NOTE: If the units do not align or excessive errors are shown, move the center frequency a few hundred kilohertz if a nearby interfering signal is suspected or increase the FSK deviation by one step.

TRC103 Device Selection

After establishing the correct COM port settings, click the arrow for the drop-down box and select **TRC103**.

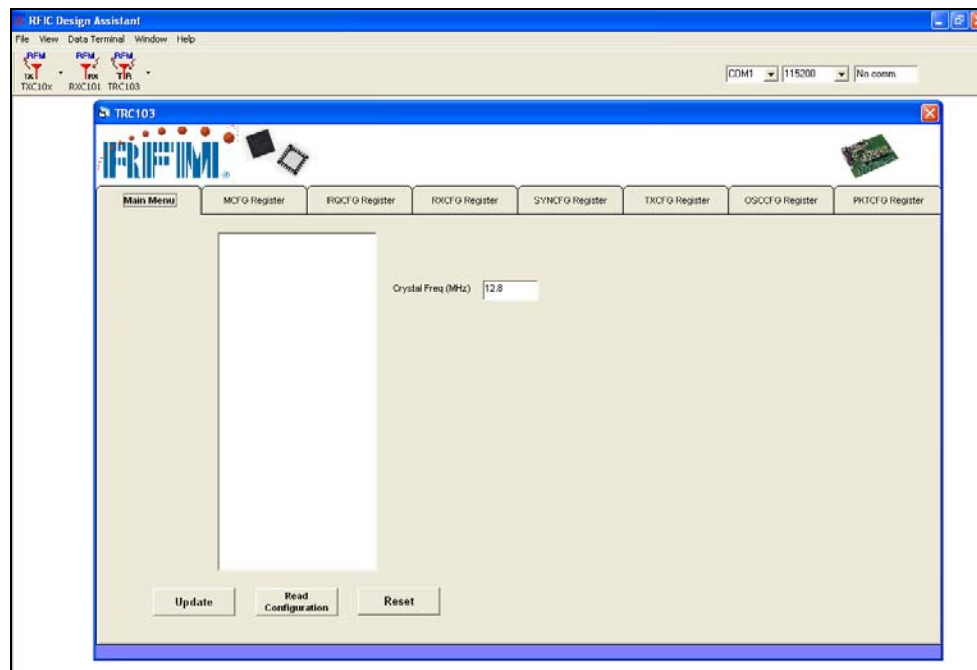


Each configuration tab follows the TRC103 datasheet. The name of the configuration register as well as its hex address is given at the top of each frame for quick reference. The current register setting value, the "Register Bits" label, is also given at the bottom right corner of each register. When a function is changed, the register setting value is updated with the new value. All register setting values are displayed in hex.

Each register setting name corresponds directly with the TRC103 datasheet. For example, when changing the Bit Rate (Config 3 0x03) the "D value" is also the same value name referenced in the datasheet. This makes correlation between RFDA and datasheet effortless.

The Update button in ALL configuration tabs sends all 32 registers to the TRC103, not just that page of values.

Main Menu

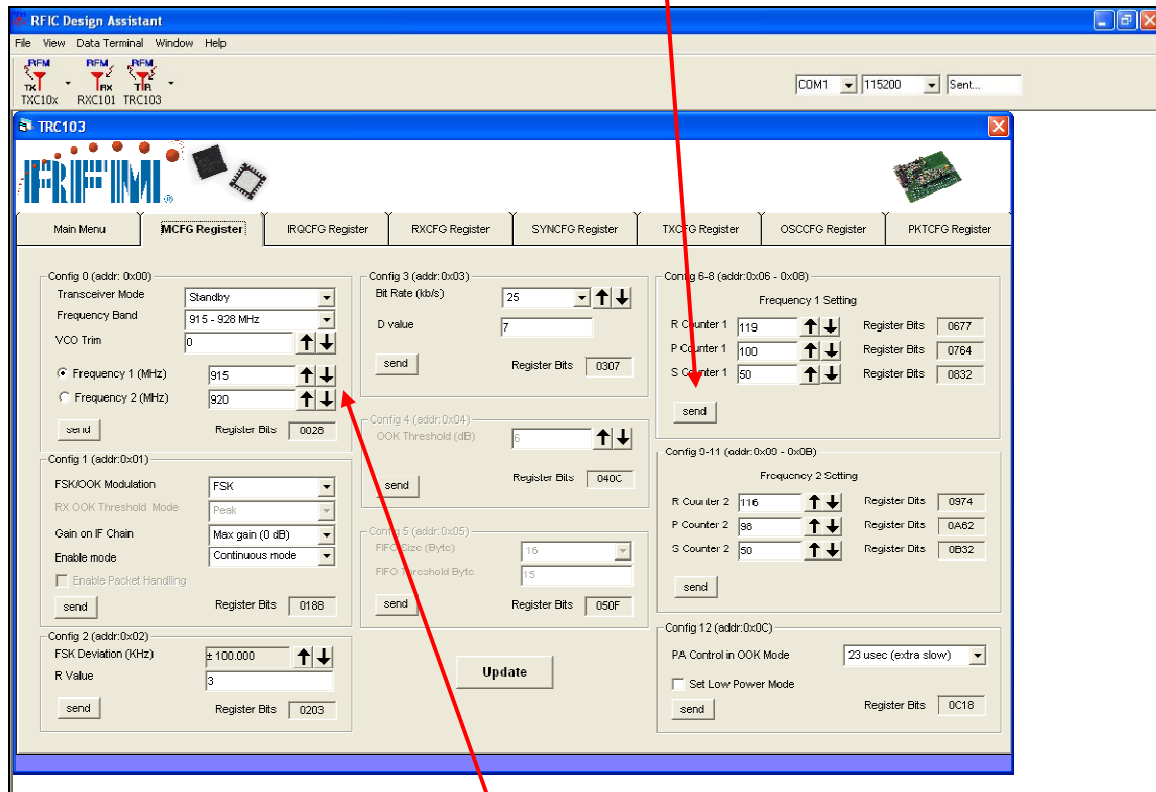


The main menu allows you to select the crystal frequency that will be used with the TRC103. The standard crystal frequency that is used for device characterization and for which the datasheet values are given is 12.8 MHz. Using other crystal frequencies, while permissible, will affect other critical parameter settings. Parameter setting changes in other registers are reflected when the crystal frequency is changed.

The Reset button reloads the default settings of all registers when selected.


The Read Configuration button reads the current values of all registers of the TRC103 and displays them in the window. The Update button sends the configuration for all registers to the TRC103. All registers allow you to update only that particular setting. Each register has a SEND button that will only send that register's value to the TRC103.

MCFG Register [0x00 – 0x0C]



The screenshot shows the RFIC Design Assistant software interface. The main window is titled 'TRC103' and contains several tabs for different registers: Main Menu, MCFG Register, IRQCFG Register, RXCFG Register, SYNCFG Register, TXCFG Register, OSCCFG Register, and PKTCFG Register. The MCFG Register tab is currently selected. It displays a grid of configuration parameters for various registers (Config 0 to Config 12). Each parameter has a text input field, a 'send' button, and a 'Register Bits' label. A red arrow points from the 'Update' button at the bottom of the MCFG Register section to the 'Update' button in the main window.

Frequency Setting

It is advised to allow the RFDA to calculate the R, P, and S register settings for the frequency. However, the user can manually adjust these values if desired and the re-calculated freq is displayed in the Config0 frame. Values for R, P, and S are entered in decimal form (0 to 255) and its hex value is calculated and displayed in the Register Bits label. Exact frequency value can be entered in the frequency box and the R,P,S value is calculated after pressing "Enter". Use the  arrows the fine tune the settings. Each click of the arrow will automatically send the new value for that register to the development board (MCFG Register ONLY).

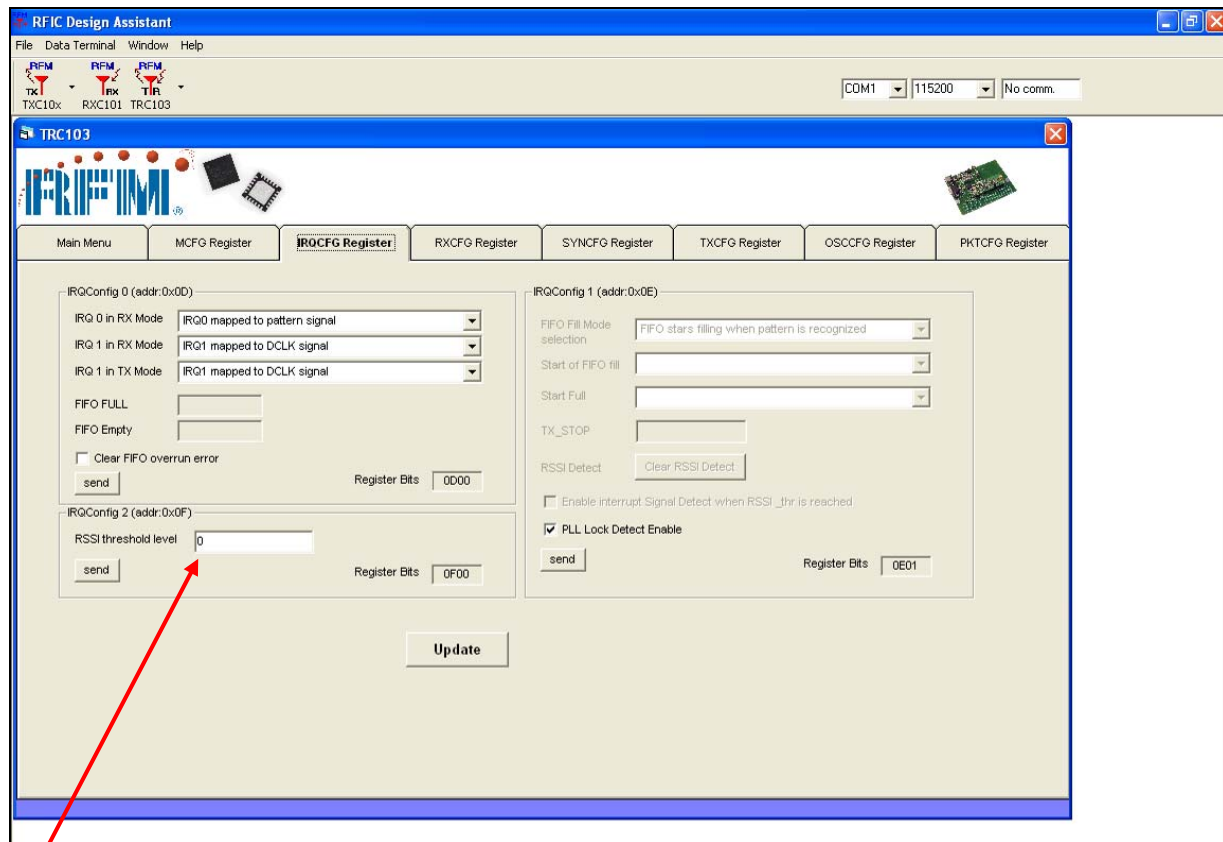
Individual Register Update

There are select registers that allow you to update only that register setting value. These are identified by having the "Send" button available in each individual frame. Clicking on the Send button sends **ONLY** that register value to the TRC103.

Individual register updates for MCFG are:

1. Bit (Data) Rate
2. R, P, S values for Frequency 1 Setting
3. R, P, S values for Frequency 2 Setting

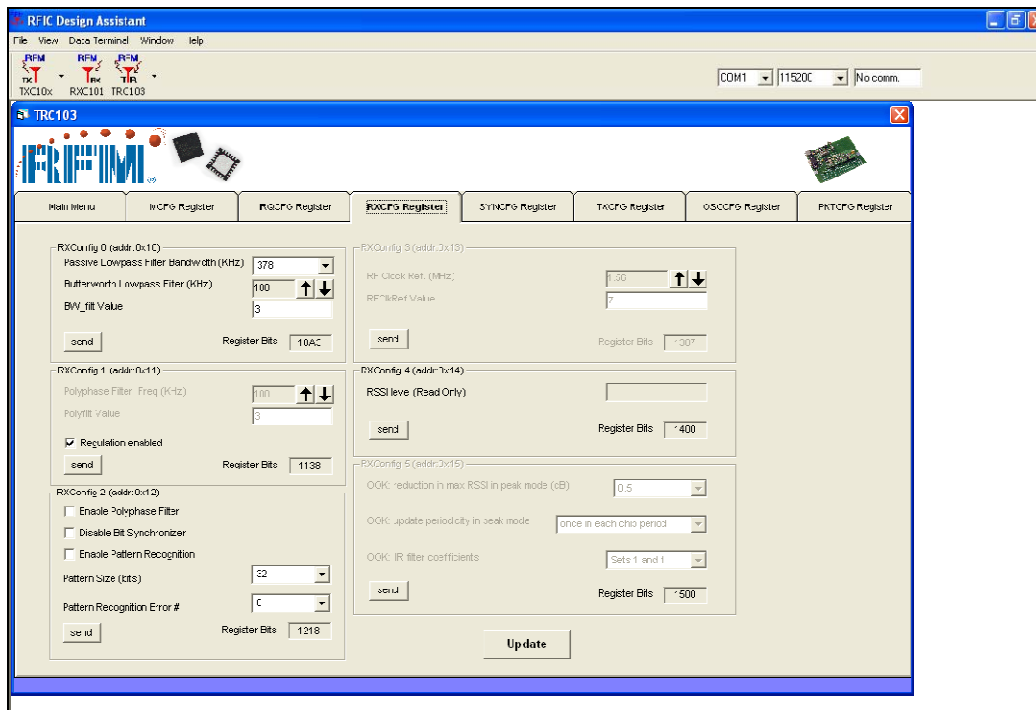
IRQCFG Register [0x0D – 0x0F]



The IRQCFG tab allows for configuration of the interrupt request mapping and FIFO usage. Depending on the mode of operation, continuous versus buffered, the selections for interrupt mapping will automatically change to remain consistent with the correct operating mode.

RSSI threshold level value should be entered as decimal. The hex equivalent is displayed in the Register value label. Read Only bits are grayed out.

RXCFG Register [0x10 – 0x15]



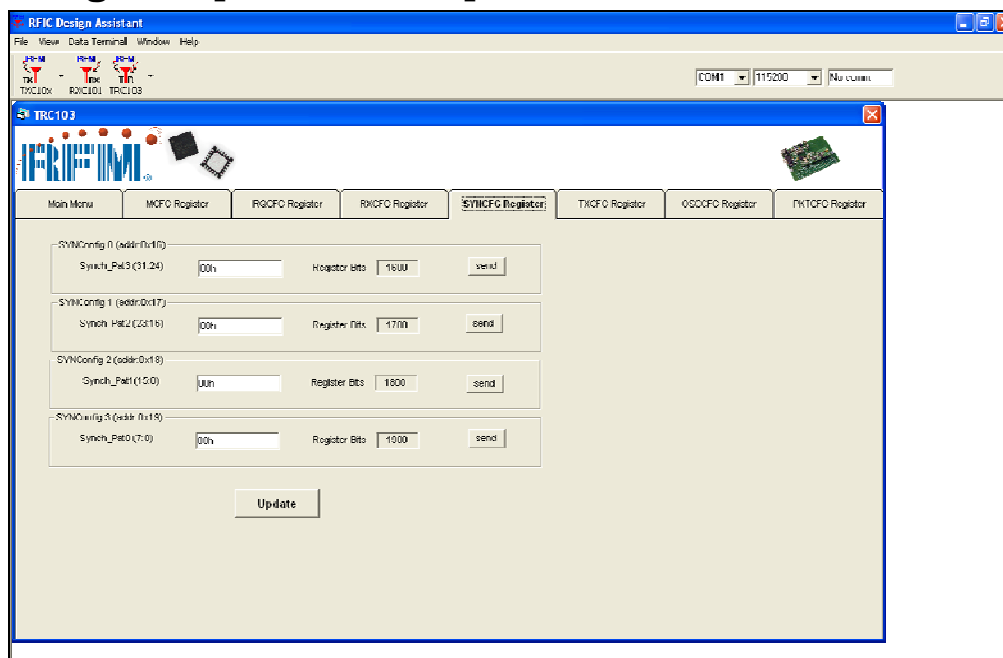
The screenshot shows the 'RXCFG Register' configuration window in the RFIC Design Assistant. The window is titled 'TRC103' and contains several tabs: Main Menu, RXCFG Register, TXCFG Register, SYNCFG Register, OSCCFG Register, and PNTCFG Register. The RXCFG Register tab is active, showing five configuration sections for registers 0 through 5. Each section includes a 'send' button and a 'Register Bits' label.

- RXConfig 0 (addr: 0x10)**: Passive Lowpass Filter Bandwidth (KHz) set to 378, Bufferwidth Lowpass Filter (KHz) set to 100, BW_Fit Value set to 3. Register Bits: 10AC.
- RXConfig 1 (addr: 0x11)**: Polyphase Filter Freq (KHz) set to 100, Polyfill Value set to 3, Regulation enabled (checked). Register Bits: 1138.
- RXConfig 2 (addr: 0x12)**: Enable Polyphase Filter (unchecked), Disable Bit Synchronizer (unchecked), Enable Pattern Recognition (unchecked), Pattern Size (bits) set to 22, Pattern Recognition Error # set to C. Register Bits: 1218.
- RXConfig 3 (addr: 0x13)**: RF Clock Rate (MHz) set to 1.30, RF's Ref Value set to 7. Register Bits: 1307.
- RXConfig 4 (addr: 0x14)**: RSSI level (Read Only). Register Bits: 1400.
- RXConfig 5 (addr: 0x15)**: OOK: reduction in max RSSI in peak mode (dB) set to 0.5, OOK: update period city in peak mode set to once in each chip period, OOK: IR filter coefficients set to Sets 1 and 1. Register Bits: 1500.

An 'Update' button is located at the bottom right of the configuration area.

All RXCFG Register settings are entered as decimal. The hex equivalent is displayed in the Register value label.

SYNCFG Register [0x16 – 0x19]



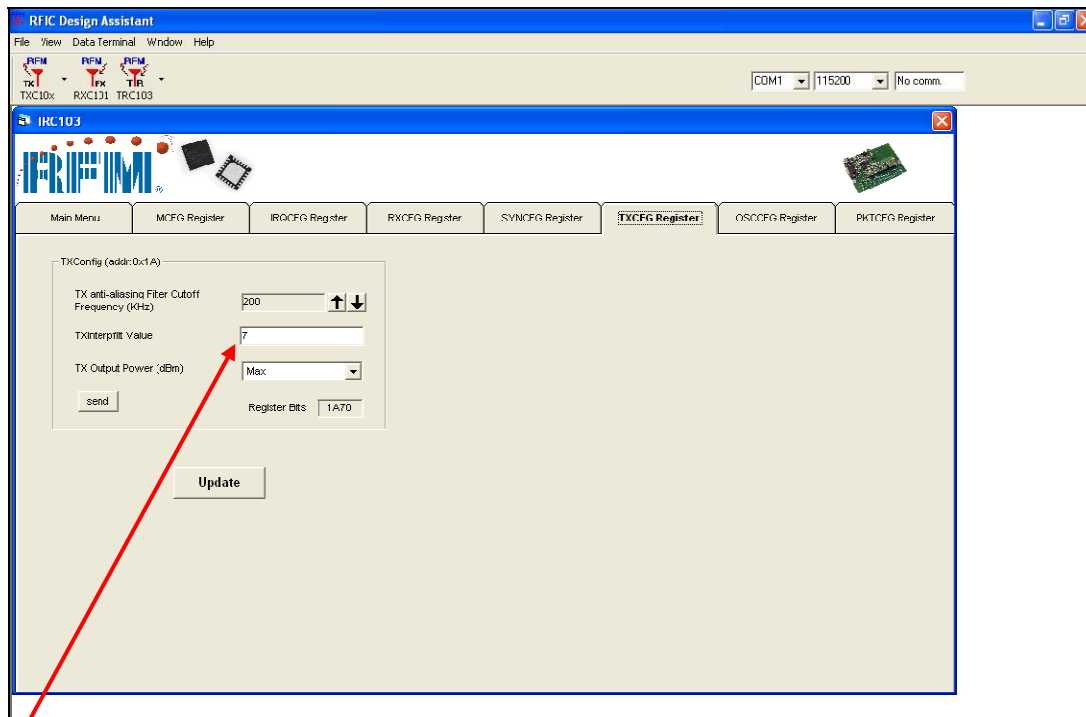
The screenshot shows the 'SYNCFG Register' configuration window in the RFIC Design Assistant. The window is titled 'TRC103' and contains several tabs: Main Menu, RXCFG Register, TXCFG Register, SYNCFG Register, OSCCFG Register, and PNTCFG Register. The SYNCFG Register tab is active, showing four configuration sections for registers 0 through 3. Each section includes a 'send' button and a 'Register Bits' label.

- SYNConfig 0 (addr: 0x16)**: Synch_Pat0 (31:24) set to 00h. Register Bits: 1600.
- SYNConfig 1 (addr: 0x17)**: Synch_Pat1 (23:16) set to 00h. Register Bits: 1700.
- SYNConfig 2 (addr: 0x18)**: Synch_Pat2 (15:0) set to 00h. Register Bits: 1800.
- SYNConfig 3 (addr: 0x19)**: Synch_Pat3 (7:0) set to 00h. Register Bits: 1900.

An 'Update' button is located at the bottom center of the configuration area.

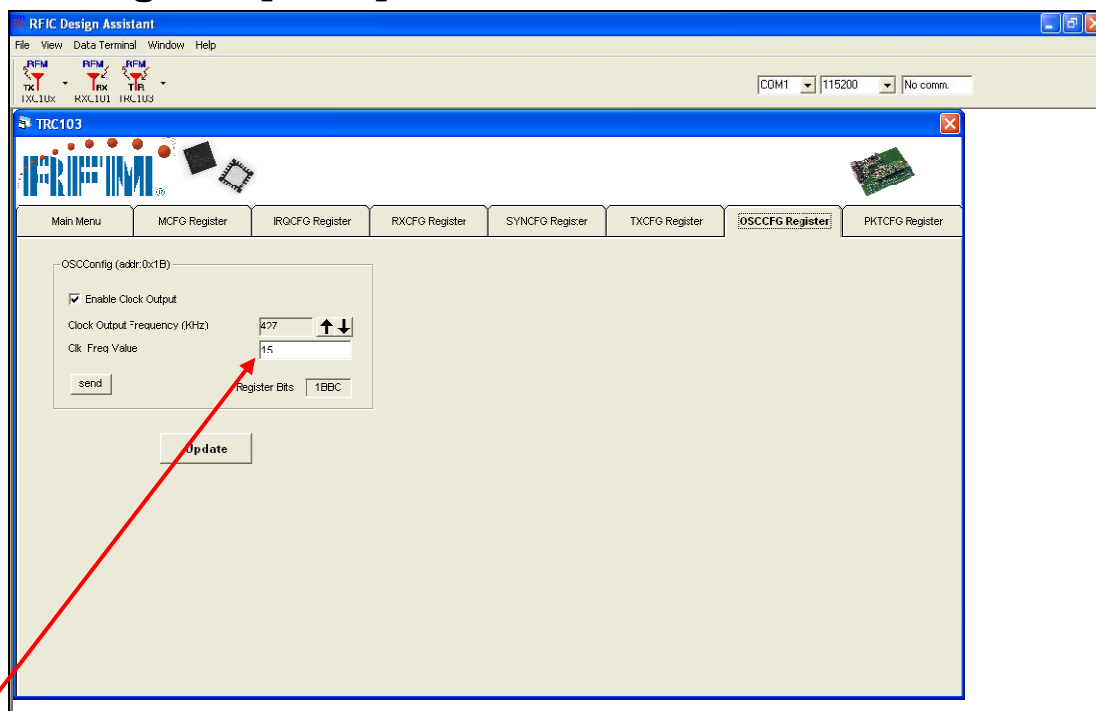
Register values for the sync bytes should be entered as hex. The 'h' need not be added.

TXCFG Register [0x1A]



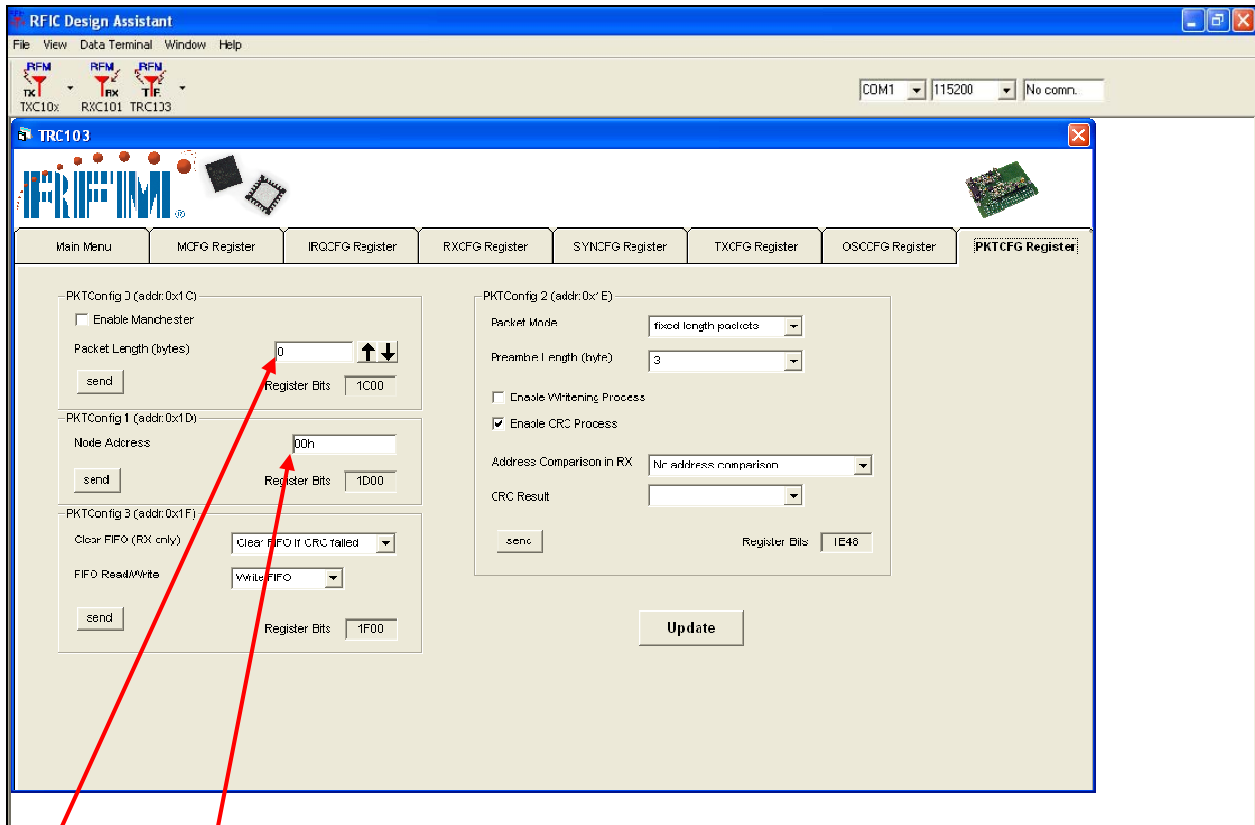
TXInterfilt value should be entered as decimal. The hex equivalent is displayed in the Register value label.

OSCCFG Register [0x1B]



Clk_Freq value should be entered as decimal. The hex equivalent is displayed in the Register value label.

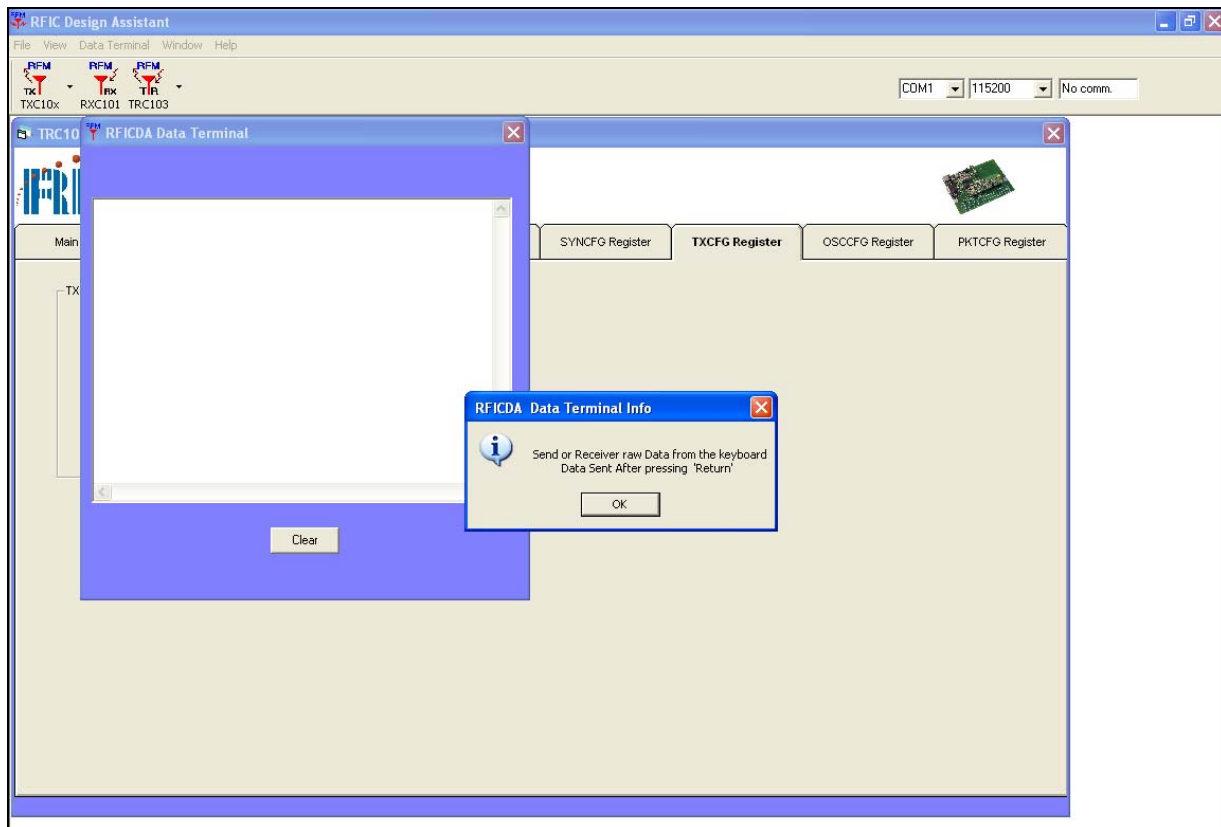
PKTCFG Register [0x1C - 1F]



The node address value should be entered as hex. The 'h' does not need to be added.

Packet Length value (dependent upon Packet Mode) should be entered as decimal. The hex equivalent is displayed in the Register value label. **NOTE: Be sure that the FIFO size is configured correctly (MCFG Register Config5).**

COMLink Data Terminal



To perform a point-to-point terminal com link, click on the Data Terminal Menu selection at the top of the screen. Click on OK to begin terminal use.

Data packets of up to 128 characters (2 x 64 bytes) may be sent using the integrated data terminal. Data packets greater than 128 bytes are truncated. The packet structure is as follows:

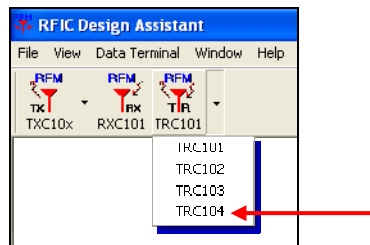
Preamble	Synch Word	Length byte	Start of Text	Character Data	End of Text	CRC
(4 bytes)	(4 bytes)	(Up to 64)	0x02	(Up to 64 bytes)	0x03	(2 bytes)
	0xE2E2					

The development board inserts Start of Text (0x02) and End of Text (0x03) characters for use by the onboard microprocessor to know where the packet starts and stops. The TRC103 automatically inserts the preamble, synch word, and CRC when it transmits a packet. The TRC103 will break the packet into two transmissions if the packet length is greater than the FIFO size (64 bytes max).

The Data Terminal requires no special characters or sequence, thus it may be used for general data transfer.

TRC104 Device Selection

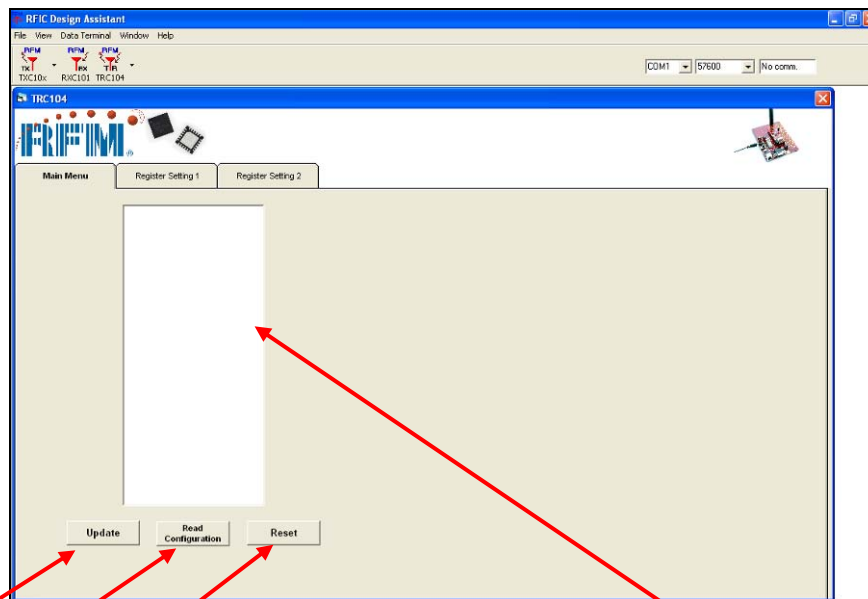
After establishing the correct COM port settings, click the arrow for the drop-down box and select **TRC104**.



The name of the configuration register and its hex address is given at the top of each frame for quick reference. The current register setting value, labeled "Register Bits", is also given at the bottom right corner of each register. When a function is changed, the register setting value is updated with the new value. All register setting values are displayed in hex. Each register setting name corresponds directly with the TRC104 datasheet. This makes correlation between RFDA and datasheet effortless. The Update button in ALL configuration tabs updates all registers to the TRC104, not just that page of values.

Main Menu

The main menu allows you to read the current configuration of the internal registers, update all registers with the current settings defined in Register 1 and Register 2 tabs, and reset the settings defined in Register 1 and Register 2 to the power-up default configuration.

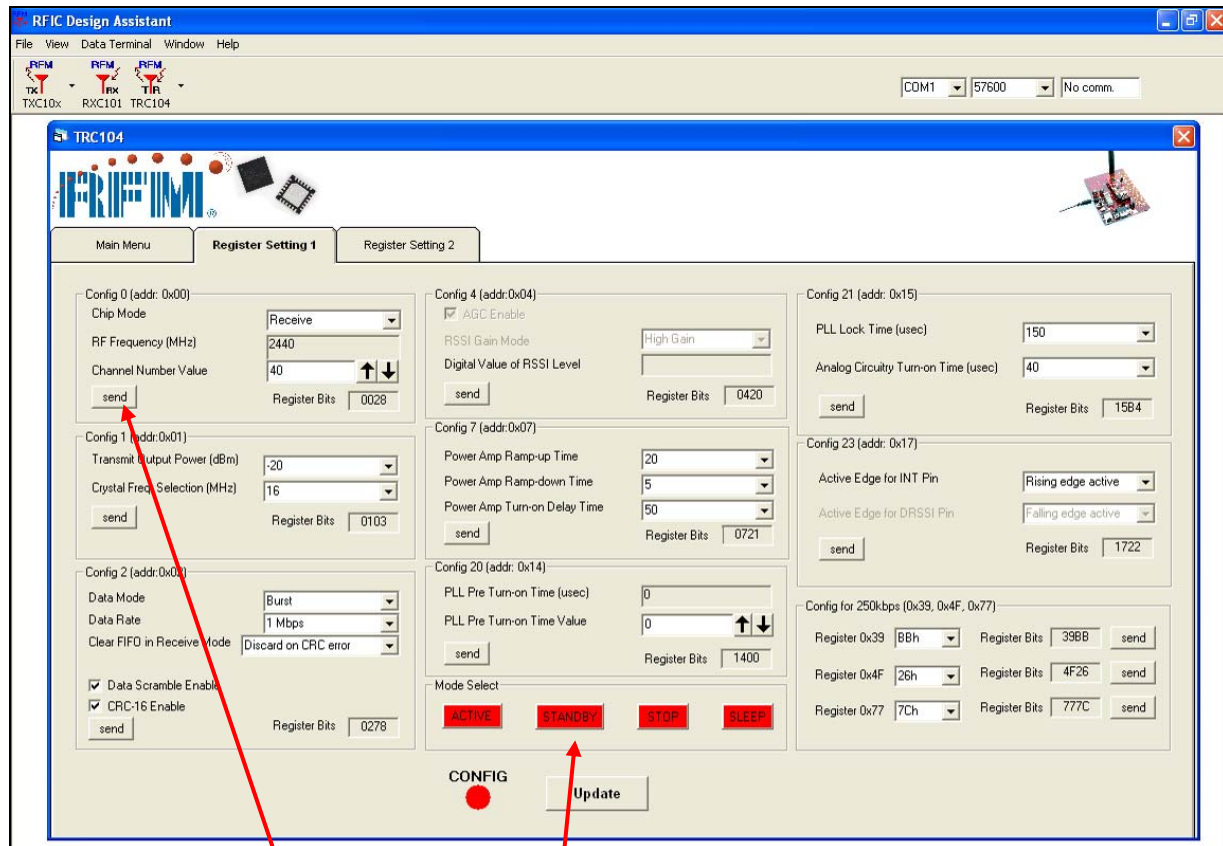


The Update button sends the configuration for all registers to the TRC104. There are select registers that allow you to update only that particular setting and these will be described in the individual tab descriptions.

The Read Configuration button reads the current values of all registers of the TRC104 and displays them in this window.

The Reset button reloads the default settings of all registers when selected.

Register Setting 1



RFIC Design Assistant

File View Data Terminal Window Help

TXC10x RXC101 TRC104

COM1 57600 No comm.

TRC104

Main Menu Register Setting 1 Register Setting 2

Config 0 (addr: 0x00)

Chip Mode: Receive

RF Frequency (MHz): 2440

Channel Number Value: 40

send

Register Bits: 0028

Config 1 (addr: 0x01)

Transmit Output Power (dBm): -20

Crystal Freq. Selection (MHz): 16

send

Register Bits: 0103

Config 2 (addr: 0x02)

Data Mode: Burst

Data Rate: 1 Mbps

Clear FIFO in Receive Mode: Discard on CRC error

☒ Data Scramble Enable

☒ CRC-16 Enable

send

Register Bits: 0278

Config 4 (addr: 0x04)

☒ AGC Enable

RSSI Gain Mode: High Gain

Digital Value of RSSI Level:

send

Register Bits: 0420

Config 7 (addr: 0x07)

Power Amp Ramp-up Time: 20

Power Amp Ramp-down Time: 5

Power Amp Turn-on Delay Time: 50

send

Register Bits: 0721

Config 20 (addr: 0x14)

PLL Pre Turn-on Time (usec): 0

PLL Pre Turn-on Time Value: 0

send

Register Bits: 1400

Config 21 (addr: 0x15)

PLL Lock Time (usec): 150

Analog Circuitry Turn-on Time (usec): 40

send

Register Bits: 1584

Config 23 (addr: 0x17)

Active Edge for INT Pin: Rising edge active

Active Edge for DRSSI Pin: Falling edge active

send

Register Bits: 1722

Config for 250kbps (0x39, 0x4F, 0x77)

Register 0x39: 8Bh Register Bits: 39B8 send

Register 0x4F: 26h Register Bits: 4F26 send

Register 0x77: 7Ch Register Bits: 777C send

Mode Select

ACTIVE STANDBY STOP SLEEP

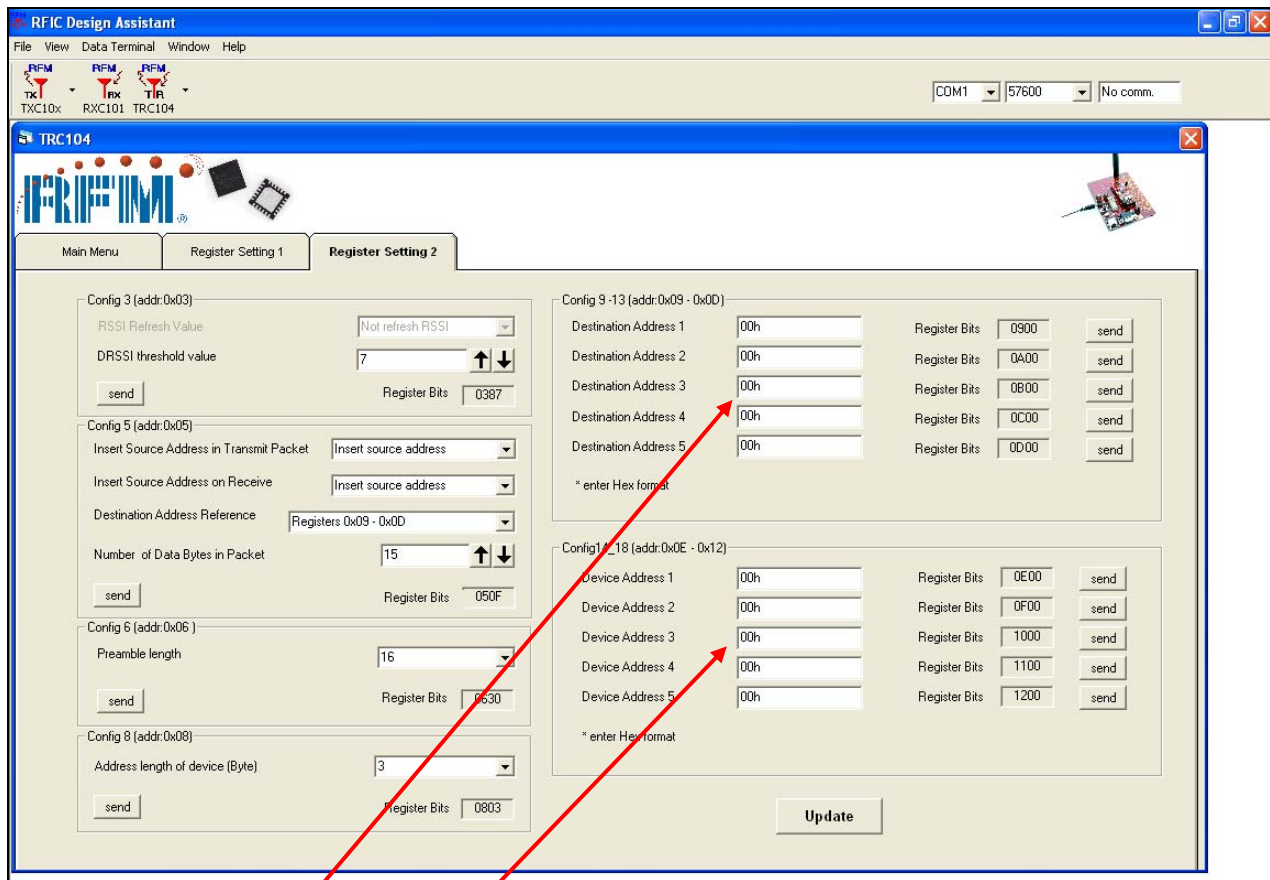
CONFIG

Update

Each register has its own SEND button that allows you to update the settings for that register only. The UPDATE button will update ALL registers.

To enable the three low power modes, there are four buttons located at the bottom of the Register Setting 1 screen. At the time the RFDA is launched, all four buttons will be RED by default. A RED button signifies that state to be inactive. A GREEN button signifies an active state. To set the TRC104 into any one of these operation modes, click on the desired button. A command is sent to the DR board to set the device to the desired mode. When performing an UPDATE or SEND, the TRC104 will revert to the STANDBY mode. See the TRC104 datasheet for details on STANDBY mode.

Register Setting 2



RFIC Design Assistant

File View Data Terminal Window Help

TXC10x RXC101 TRC104

COM1 57600 No comm.

TRC104

Main Menu Register Setting 1 Register Setting 2

Config 3 (addr:0x03)

RSSI Refresh Value Not refresh RSSI

DRSSI threshold value 7

send Register Bits 0387

Config 5 (addr:0x05)

Insert Source Address in Transmit Packet Insert source address

Insert Source Address on Receive Insert source address

Destination Address Reference Registers 0x09 - 0x0D

Number of Data Bytes in Packet 15

send Register Bits 050F

Config 6 (addr:0x06)

Preamble length 16

send Register Bits 0630

Config 8 (addr:0x08)

Address length of device (Byte) 3

send Register Bits 0803

Config 9-13 (addr:0x09 - 0x0D)

Destination Address 1 00h Register Bits 0900 send

Destination Address 2 00h Register Bits 0A00 send

Destination Address 3 00h Register Bits 0B00 send

Destination Address 4 00h Register Bits 0C00 send

Destination Address 5 00h Register Bits 0D00 send

* enter Hex format

Config 14-18 (addr:0x0E - 0x12)

Device Address 1 00h Register Bits 0E00 send

Device Address 2 00h Register Bits 0F00 send

Device Address 3 00h Register Bits 1000 send

Device Address 4 00h Register Bits 1100 send

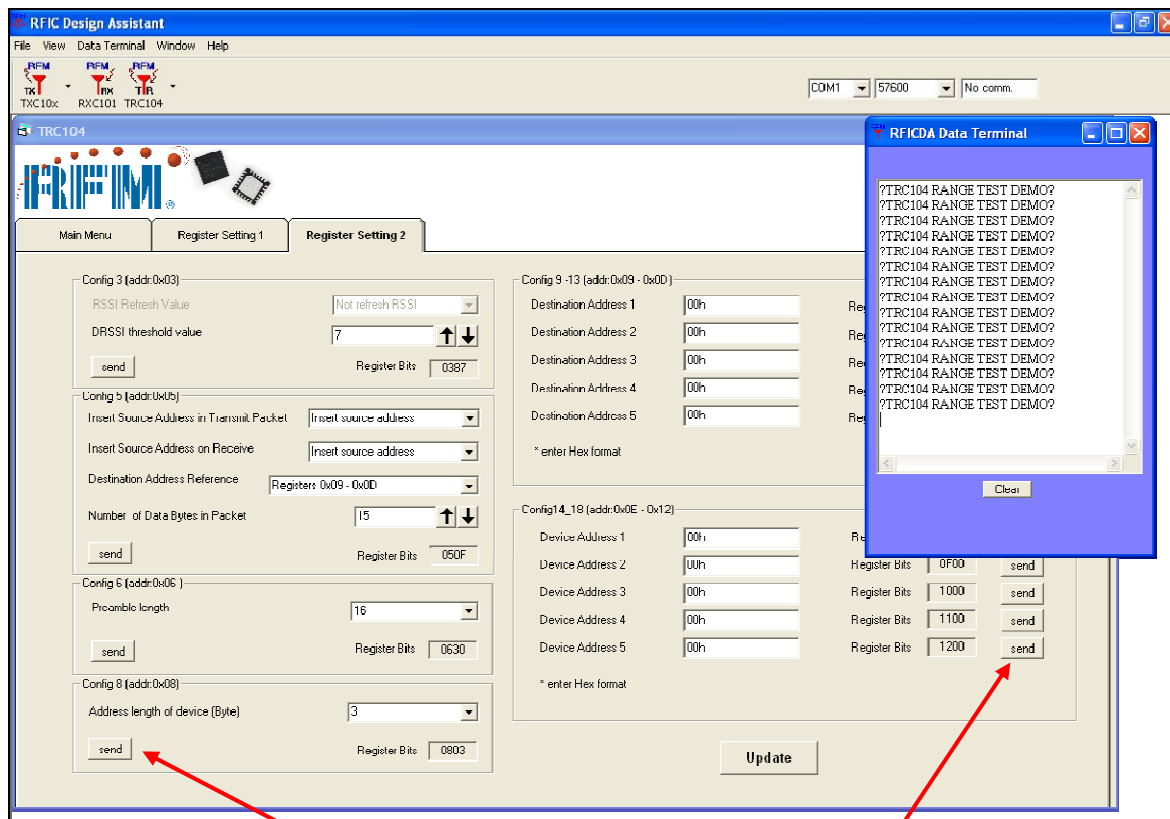
Device Address 5 00h Register Bits 1200 send

* enter Hex format

Update

When configuring the Destination or Device (Sender) address, the value(s) should be entered in hex format. It is not required to add the 'h' at the end. The address length (Config 8) defines the number of active bytes for both the Destination and Device address setting. The Destination and Device address MUST be configured for the same length.

COMLink Data Terminal

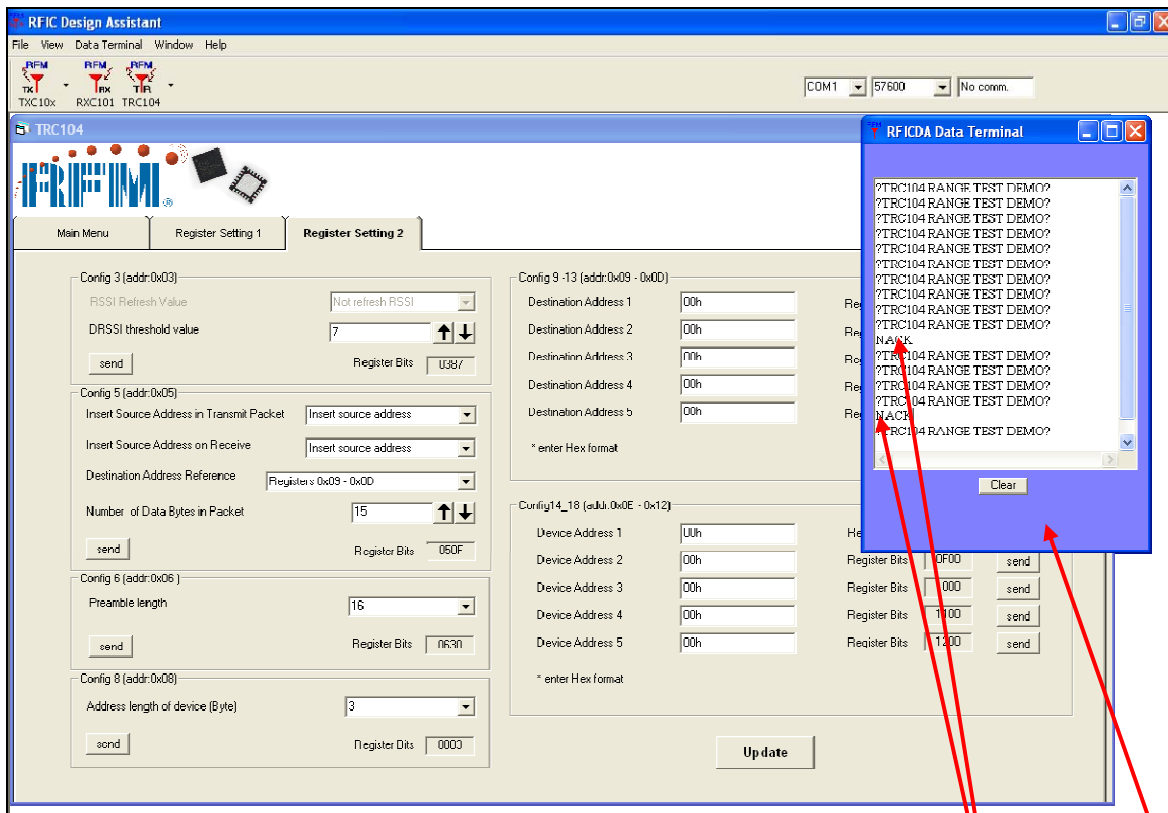


The Data Terminal allows you to monitor the data transferred during a Range Test or to setup a terminal link between two PC's. Contents typed in the Data Terminal are sent upon pressing the ENTER key. An LED will flash indicating a successful transmission.

The receiving terminal will display the sent data and the GREEN LED will flash indicating a successful transfer and CRC check.

When using the COMLink Data Terminal, use the individual SEND buttons to modify the configuration registers individually, since the development boards are preconfigured. See the DR-TRC104-DK User Guide for details on the configuration register settings.

The Data Terminal requires no special characters or sequence, thus it can be used for general data transfer.



When using the COMLink Data Terminal, specifically during a Range Test, the received data is displayed in the terminal window. If a packet is missed, the development board will respond with a NACK response in the terminal window indicating that there was no response from the remote unit for that packet. Good packets will be displayed in the terminal window.