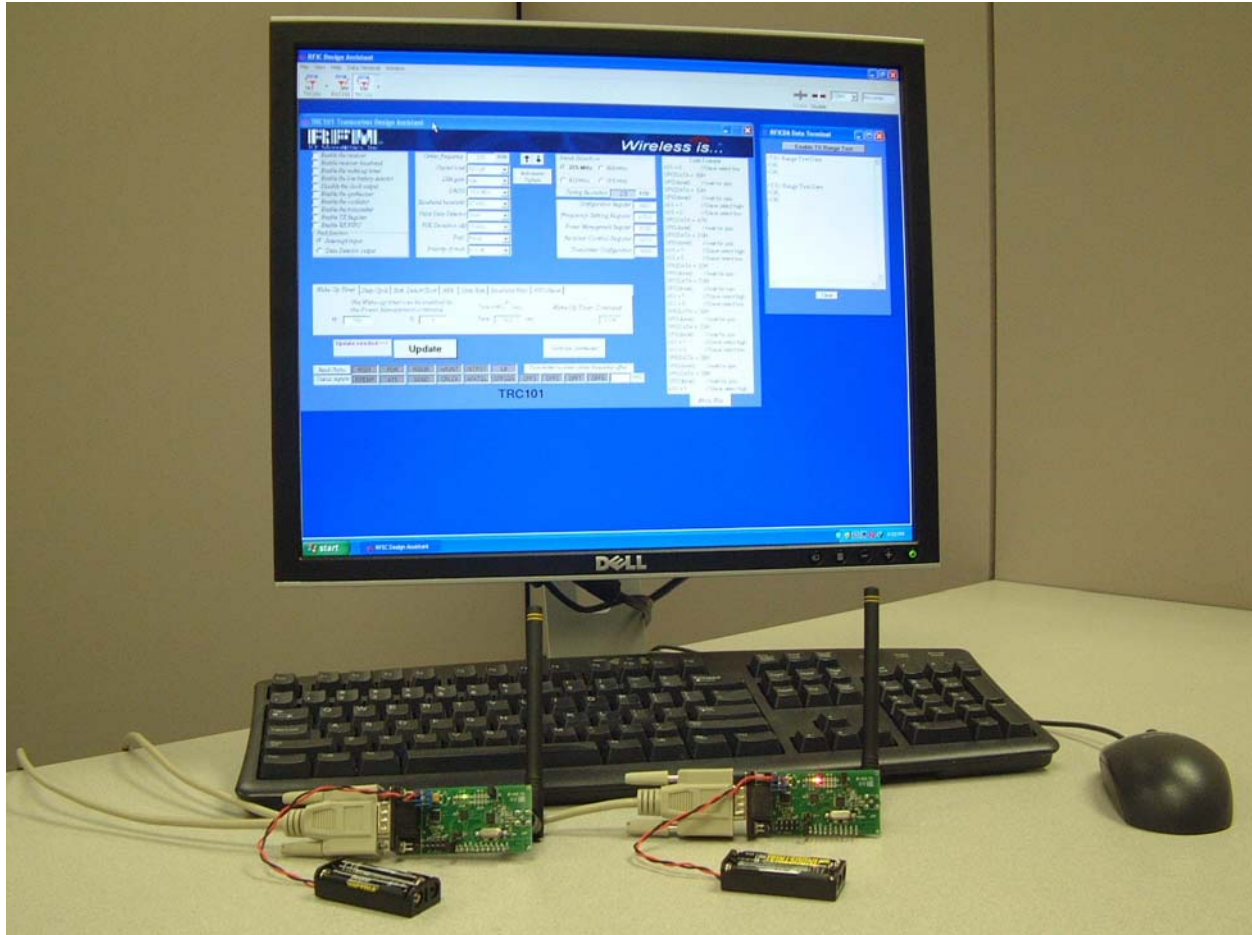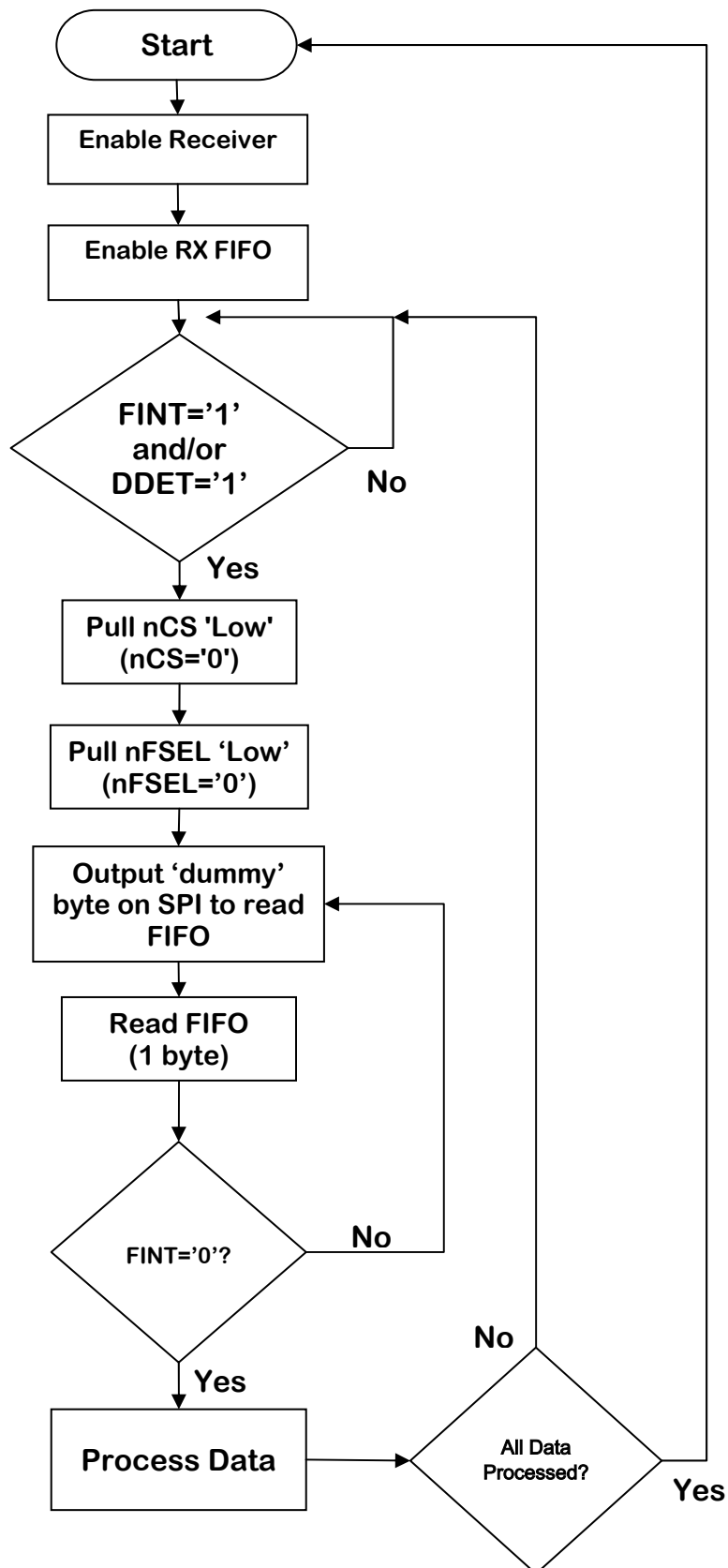# RFIC TX/RX Configuration

RXC101 Configuration

When the RXC101 is configured in microcontroller mode, data can be received in three ways; directly from the Data pin (6), through the internal receive FIFO, or through a Status Register read. The best method that requires minimal effort would be to use the internal FIFO for data reception.

The FIFO can be read by use of the SPI port pins nCS, SDO, SDI, and SCK as well as the nFSEL pin (6) and FINT pin (7). nFSEL is only used if the internal FIFO is enabled (*FIFO Configuration Register* bit 0) and must be pulled "Low" for the entire access time of the FIFO. nFINT may be used as a "FIFO Full" interrupt to wake a processor or may be periodically polled by the processor. The nFINT pin (7) will go "High" after the FIFO has filled to the preprogrammed limit written to the FINT[7..4] bits of the *FIFO Configuration Register*. After the SPI port is enabled, by pulling nCS low, a clock is applied to the SCK line and the data may be read out one bit at a time on the SDO line every rising edge of SCK. **The maximum SCK freq for reading the FIFO is Fxtal/4, or 2.5 MHz for a 10 MHz xtal freq**. Attempting to read the FIFO faster than this will result in read data errors.

The recommended method for reading the FIFO is given below. This is also summarized on page 23 of the RXC101 datasheet.
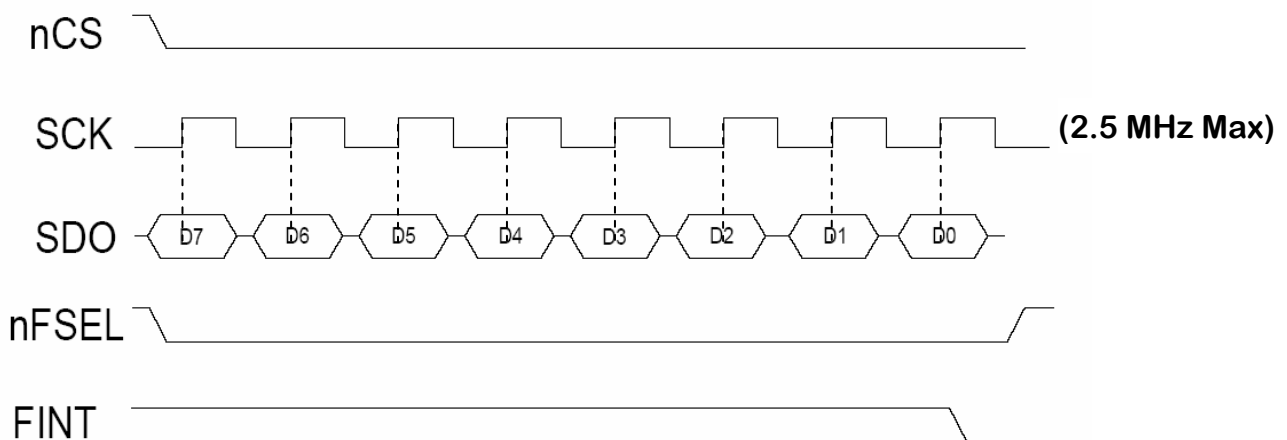
The following flowchart may be used as a guide to writing application code for reading the FIFO.

```
                        ┌──────────────┐
                        │    Start     │◄──────────────────────┐
                        └──────┬───────┘                       │
                               │                               │
                      ┌────────▼────────┐                      │
                      │ Enable Receiver │                      │
                      └────────┬────────┘                      │
                               │                               │
                      ┌────────▼────────┐                      │
                      │  Enable RX FIFO │                      │
                      └────────┬────────┘                      │
                               │◄──────────────────┐          │
                               │                    │          │
                          ◇────▼────◇               │          │
                         ╱ FINT='1'  ╲     No       │          │
                        ◇  and/or     ◇─────────────┘          │
                         ╲ DDET='1'  ╱                         │
                          ◇────┬────◇                          │
                               │ Yes                           │
                      ┌────────▼────────┐                      │
                      │ Pull nCS 'Low'  │                      │
                      │    (nCS='0')    │                      │
                      └────────┬────────┘                      │
                               │                               │
                      ┌────────▼────────┐                      │
                      │ Pull nFSEL 'Low'│                      │
                      │   (nFSEL='0')   │                      │
                      └────────┬────────┘                      │
                               │                               │
                      ┌────────▼────────┐                      │
                      │ Output 'dummy'  │◄──────────┐          │
                      │ byte on SPI to  │           │          │
                      │   read FIFO     │           │          │
                      └────────┬────────┘           │          │
                               │                    │          │
                      ┌────────▼────────┐           │          │
                      │   Read FIFO     │           │          │
                      │   (1 byte)      │           │          │
                      └────────┬────────┘           │          │
                               │                    │          │
                          ◇────▼────◇       No       │          │
                         ╱           ╲──────────────┘          │
                        ◇  FINT='0'?  ◇                        │
                         ╲           ╱                         │
                          ◇────┬────◇                          │
                               │ Yes                No          │
                      ┌────────▼────────┐      ◇────▼────◇     │
                      │  Process Data   │─────╱ All Data  ╲    │
                      └─────────────────┘    ◇ Processed? ◇────┘
                                              ╲           ╱  Yes
                                               ◇─────────◇
```

Minimum Configuration (Polled)

The minimum configuration for the RXC101 uses only 5 connections. These connections are summarized below.
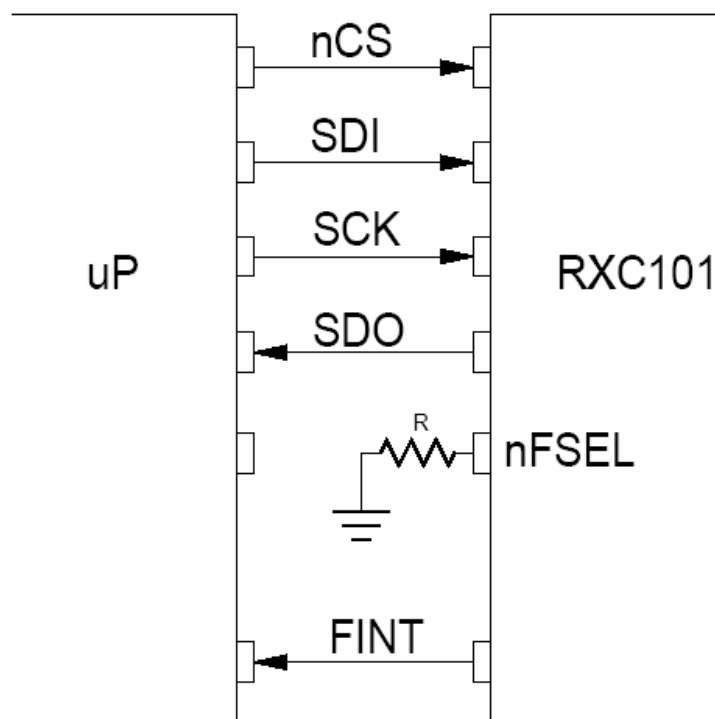
nFSEL is used to select the internal FIFO if the FIFO is enabled. If the internal FIFO will always be used to receive data, this pin can be permanently pulled "High" with an external 10KΩ pull-up resistor, thereby saving the use of an additional processor pin. The FINT pin can be used as an interrupt to determine when the FIFO is ready to be read. This allows for a processor to sleep or run other tasks until the FINT pin indicates a FIFO ready condition.

Interrupt-based Configuration

The interrupt based configuration uses nIRQ to notify when to read status bits. The status of the internal FIFO is given by the nIRQ pin going "Low". Upon reading the status bits, the first bit indicates whether the FIFO has reached the preprogrammed limit.
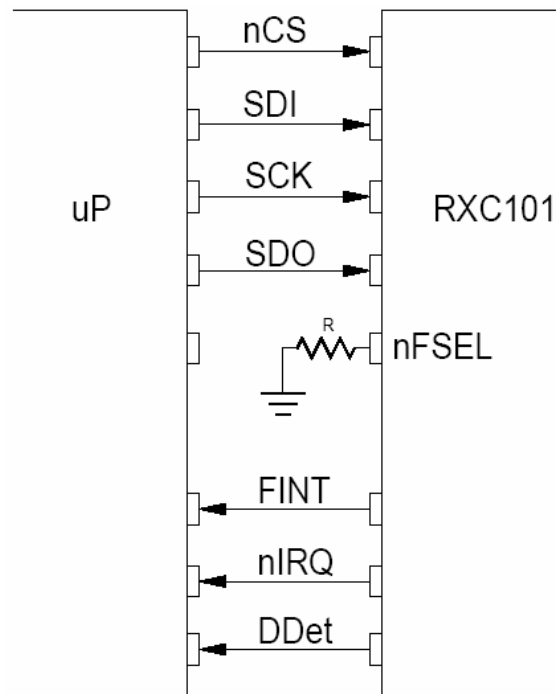
TRC10x Receive Configuration

When the TRC10x is configured in microcontroller mode, data can be received in three ways; directly from the Data pin (6), through the internal receive FIFO, or through a Status Register read. The best method that requires minimal effort would be to use the internal FIFO for data reception.
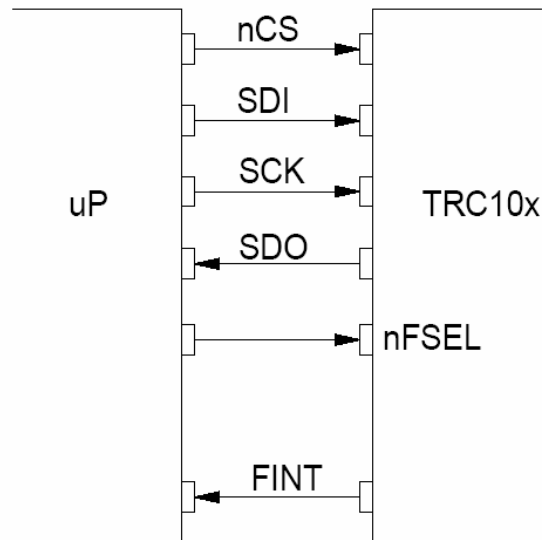
The TRC10x receive configuration follows the RXC101 configuration. The pinout and FIFO function of the device is identical EXCEPT for the state of the nCS pin.
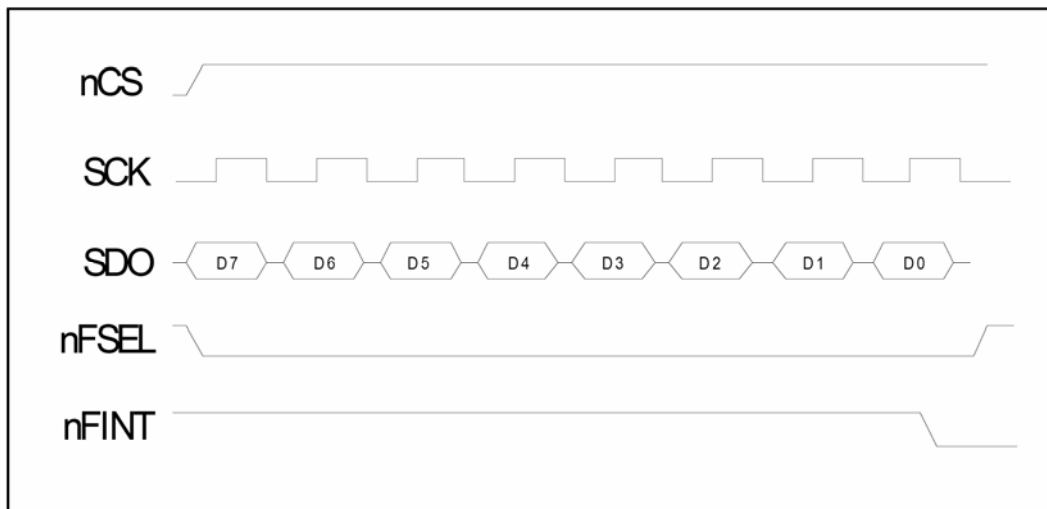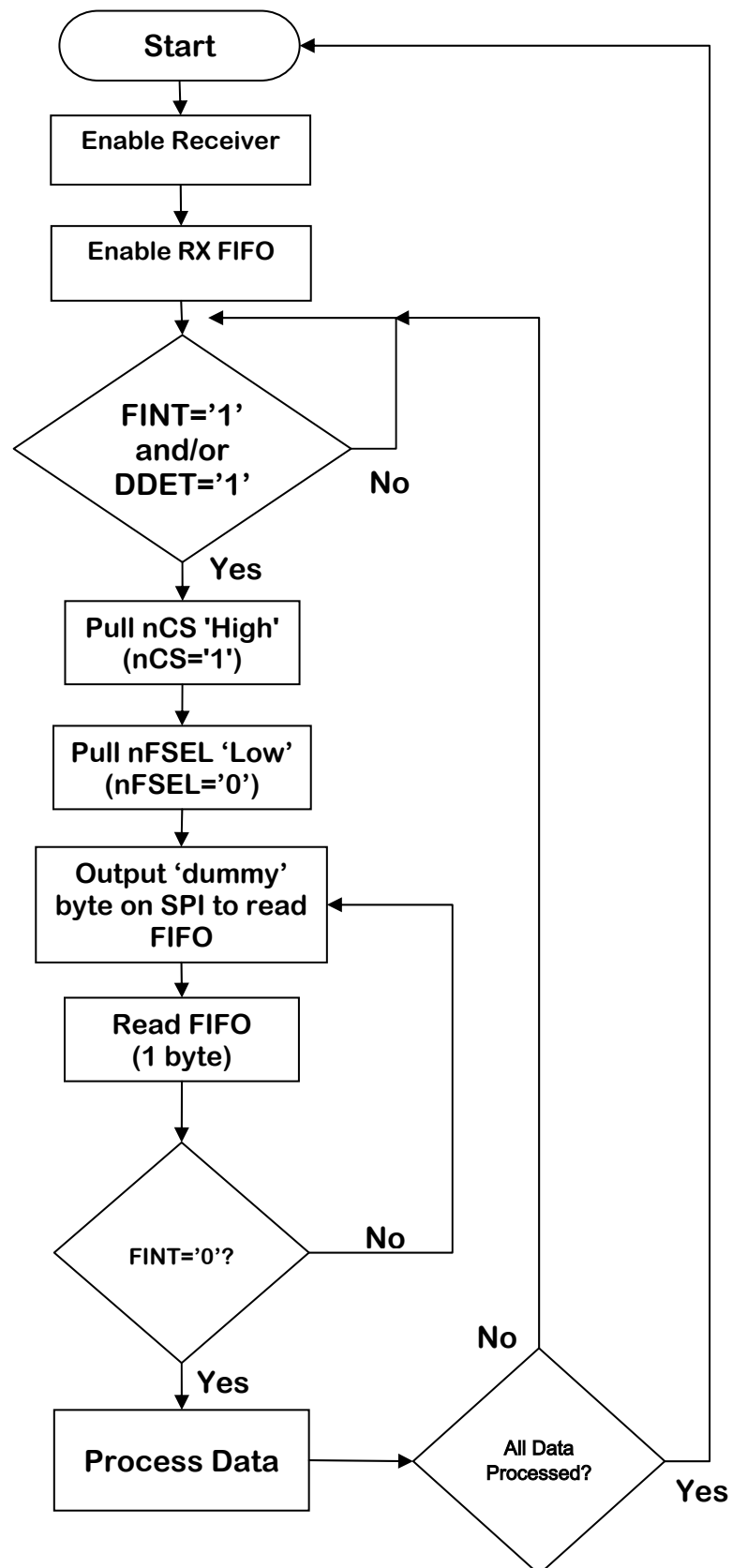

When accessing the FIFO directly, and not through the the FIFO Read Register, the nCS state is "High" through the entire read process. On each rising edge of SCK the state of the received bit is applied to the SDO pin. A read of the SDO pin after each rising edge will give the state of that bit.

The nFSEL pin is used to enable the internal FIFO for receive (*Configuration Register* bit 6 **SET**), or the transmit register for transmit (*Configuration Register* bit 7 **SET**). Both bits may be set at the same time to enable fast switching between modes. Pulling nFSEL "Low" enables the internal receive FIFO for receive. Pulling nFSEL "High"
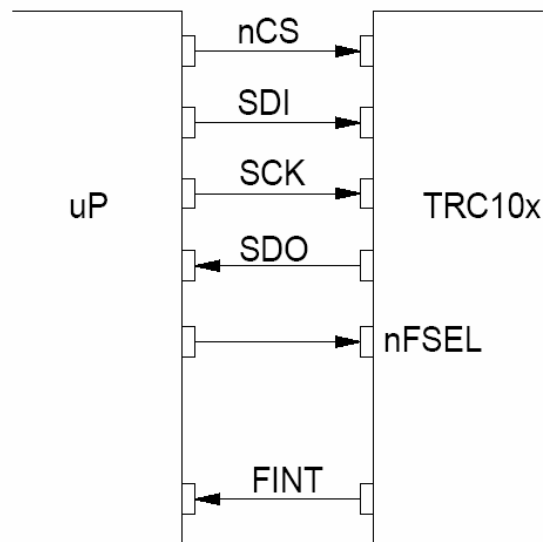
enables the transmit register for transmitting data. nFSEL must be kept "Low" for the entire duration of the data transaction.

The following flowchart may be used as a guide to writing application code for reading the FIFO.

```
                    ┌──────────────────┐
                    │      Start       │◄────────────────────────┐
                    └──────────────────┘                         │
                             │                                   │
                    ┌──────────────────┐                         │
                    │ Enable Receiver  │                         │
                    └──────────────────┘                         │
                             │                                   │
                    ┌──────────────────┐                         │
                    │  Enable RX FIFO  │                         │
                    └──────────────────┘                         │
                             │                  ┌────────────────┤
                             ▼                  │                │
                         ╱╲                     │                │
                        ╱    ╲                  │                │
                       ╱ FINT=              No  │                │
                      ╱  '1' and/or ╲───────────┘                │
                       ╲ DDET='1' ╱                              │
                        ╲        ╱                               │
                         ╲      ╱                                │
                          ╲╱  Yes                                │
                             │                                   │
                    ┌──────────────────┐                         │
                    │ Pull nCS 'High'  │                         │
                    │    (nCS='1')     │                         │
                    └──────────────────┘                         │
                             │                                   │
                    ┌──────────────────┐                         │
                    │ Pull nFSEL 'Low' │                         │
                    │   (nFSEL='0')    │                         │
                    └──────────────────┘                         │
                             │                                   │
                    ┌──────────────────┐                         │
                    │ Output 'dummy'   │◄──────────┐             │
                    │ byte on SPI to   │           │             │
                    │   read FIFO      │           │             │
                    └──────────────────┘           │             │
                             │                      │             │
                    ┌──────────────────┐            │             │
                    │    Read FIFO     │            │             │
                    │    (1 byte)      │            │             │
                    └──────────────────┘            │             │
                             │                      │             │
                         ╱╲                         │             │
                        ╱    ╲        No            │             │
                       ╱ FINT= ╲──────────────────┘             │
                       ╲ '0'? ╱                                  │
                        ╲    ╱                                    │
                         ╲╱  Yes                                  │
                          │                    No                │
                          ▼              ╱╲                      │
              ┌──────────────────┐      ╱    ╲                   │
              │  Process Data    │─────╱  All   ╲────────────────┘
              └──────────────────┘     ╲  Data  ╱  Yes
                                        ╲Processed?╱
                                         ╲      ╱
                                          ╲╱
```

TRC10x Transmit Configuration

When the TRC10x is configured in microcontroller mode, data can be sent in two ways; directly from the Data pin (6), or through the internal transmit register. The best method that requires minimal effort would be to use the internal transmit register. The TRC10x keeps track of bit timing and sends each bit at the appropriate time according to the data rate set by the Data Rate Setup Register.


The nFSEL pin is used to enable either the internal FIFO for receive, or the transmit register for transmit. Pulling nFSEL "Low" enables the internal receive FIFO for receive. Pulling nFSEL "High" enables the transmit register for transmitting data. nFSEL must be kept "High" for transmit for the entire duration of the data transaction.

The *Transmit Register* holds the 8 bits to be transmitted. Bit [7] of the Configuration Register must be set "High" in order to use this. When bit [5] of the *Power Management Register* is set, transmission begins immediately. The SDO pin(4) may be monitored to see when the next byte of data may be written to the register (SDO is logic '1').
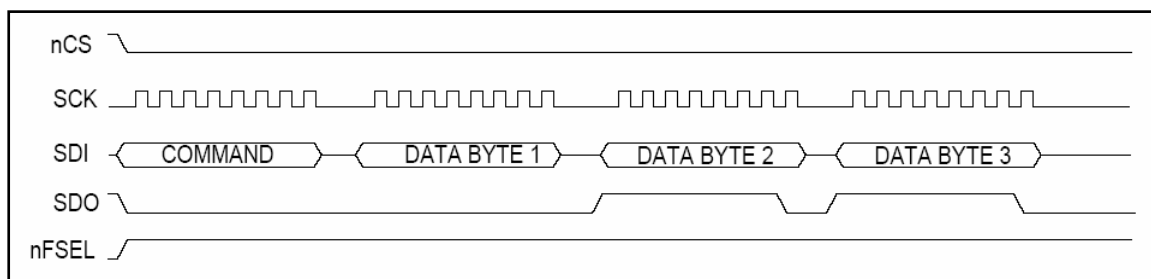
The transmit register may be continuously accessed by holding the nCS pin (3) 'Low' for the duration of the data stream. On the first falling edge of nCS the register command should be issued as normal. Sequential byte writes to the register afterwards will load the transmit register directly without having to reissue the command byte. The SDO pin (4) may be used as a "Transmit Register Empty" flag to write the next byte.

The following flowchart may be used as a guide to writing application code for writing the transmit register to send data.
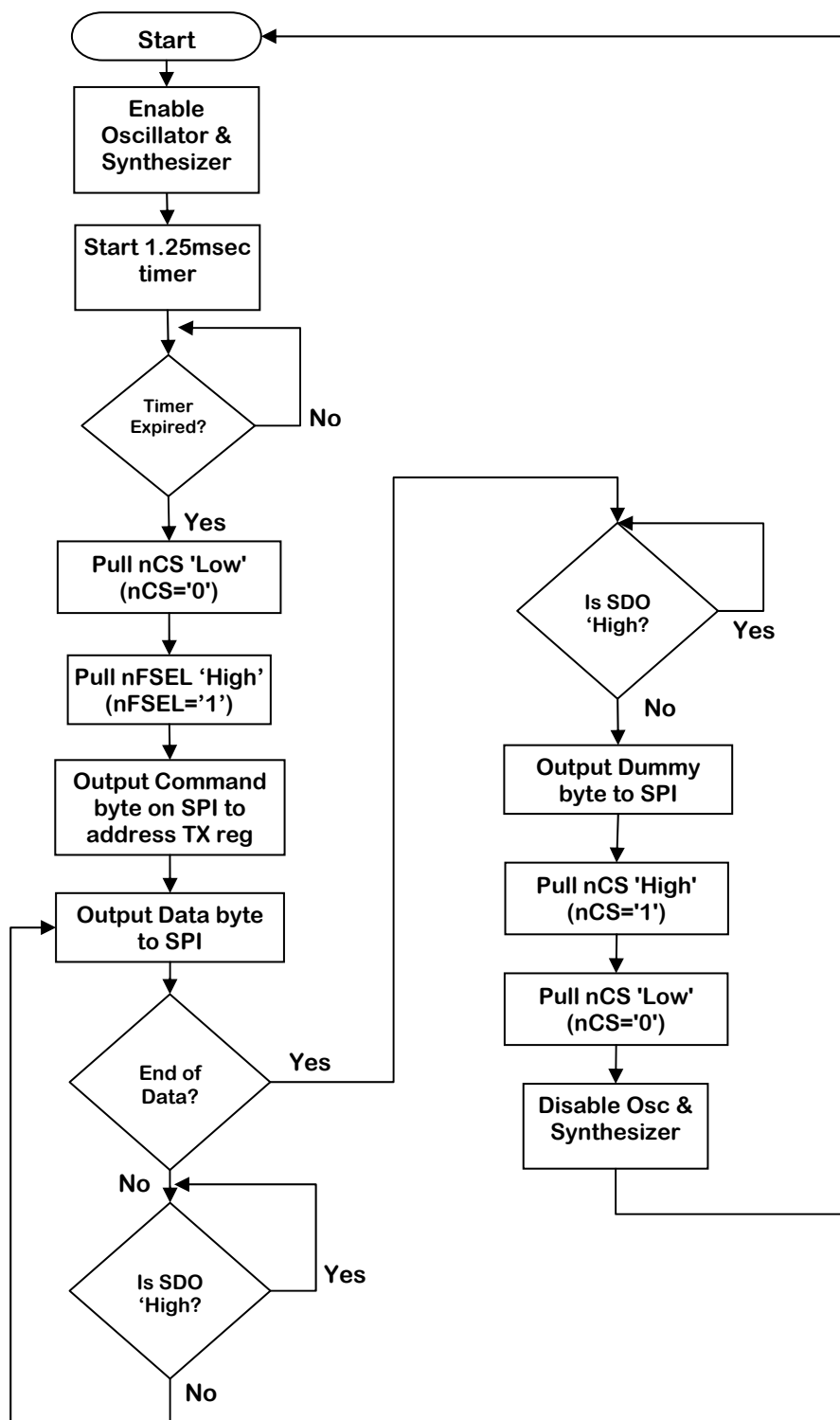
RFIC Calibration

The RF VCO in the PLL performs automatic calibration on startup, which requires only a few microseconds. Calibration always occurs when the synthesizer begins. If temperature or supply voltage changes significantly, VCO recalibration can be initiated at any time by switching the synthesizer off and back on again. Calibration is also recommended when switching from one frequency band to another.