Pick sample-holds by accuracy and speed and keep hold capacitors in mind

Part 3 of 3

When it comes to selecting a sample-hold device, fortunately there's a fine assortment available: monolithic, hybrid and modular types can all give good performance. There are different degrees of good performance, of course, and for the most part the sample-hold that's finally selected will depend on the degree of speed and accuracy needed. Depending on the type of sample-hold and its application, it may need an external hold capacitor. This capacitor should be chosen with as much care as the sample-hold itself, for its quality directly affects the performance of the sample-hold. There will be more about selecting hold capacitors, but first, it's a good idea to consider error analysis, which is vital in appraising the total error contribution of a sample-hold to a system.

In a given system, of course, the sample-hold is but one of the many sources of error that may also include an amplifier, filter, multiplexer, and a/d converter. Achieving total system accuracy on the order of 0.01% is by no means a trivial task, but quite the opposite. It pays to take a somewhat pessimistic approach in adding up the errors, and follow this by thorough testing of the sample-hold's accuracy in the system. In many cases the results will be a pleasant surprise, because a conservatively-specified device has been chosen. In other cases, it won't be a shock to discover that the analysis is about right because the sample-hold that was selected has been specified right at the edge of its performance.

The best way to handle error analysis is with a systematic listing like the one in Table 1, which gives errors for a fast, accurate system with 0.01% error as a design goal. The errors are computed for an assumed operating temperature range of 0 to 50 C and take into account all of the specifications discussed in this series.

What seems to be a large total error in Table 1 shouldn't be alarming. The sample-hold evaluated, designed for use in 12-bit systems, has been conservatively specified. If all the errors add in the same direction, the total error is ±0.036%, but this is an unlikely possibility. Adding the errors statistically (RMS) gives a better figure of ±0.017%, which is a good bit closer to the goal. Since most of the errors are specified as maximums, the typical statistical error is actually close to 0.01%.

Speed and accuracy are the two foremost considerations in choosing a sample-hold, and the key to proper selection is an error analysis that takes the desired sampling rate into account. The circuit configuration, a subject discussed in Part 1 of this series, affects performance in certain applications, so it should be kept in mind as well.

Consider monolithics first

In general, a monolithic device should be considered first, since it will result in the lowest-cost design if moderate performance is acceptable. Moderate performance implies about 4 μs acquisition time to 0.1% and 5 to 25 μs to 0.01%. Monolithic devices use external hold capacitors, so one will need to be selected.

Hybrid microcircuit sample-holds offer a step up in performance without a major increase in size. Acquisition times of 5 μs down to 1 μs, to 0.01% accuracy are available, and even faster acquisition times for 0.1% can be obtained. Most hybrid sample-holds include an internal hold capacitor, so there's no need to select one unless additional capacitance is needed. Many hybrids use MOS-type hold capacitors which offer exceptionally good performance.

Both the newer monolithic as well as hybrid devices equal or surpass the performance of many of the early low-cost modular sample-holds, but they can't match the newer, high-performance modular types. These new modules offer some difficult-to-achieve speed and accuracy specifications such as 350-ns maximum ac-

Table 1. Error analysis of an accurate, high speed sample-hold

Source of error	Error contribution	Comments
Acquisition error	0.01%	Maximum error specified for rated acquisition time.
Gain error	0.00	Externally adjustable to zero.
Offset error	0.00	Externally adjustable to zero.
Nonlinearity	0.005%	Maximum specified.
Droop error	0.01%	For 10 μs hold time. Using 25 C droop of 20 μV/μs max. and multiplying by 10 to give droop of 1 mV at 50 C. This is 0.01% for 10 V full scale.
Gain change	0.004%	Using specified 15 ppm/°C max., X maximum temperature change of 25 C.
Offset change	0.008%	Using specified 30 μV/°C max., X max. temperature change of 25 C.
Dielectric absorption	0.003%	Estimated error voltage during hold time using curve of Fig. 2.
Total	0.036%	
RMS Total	0.017%	

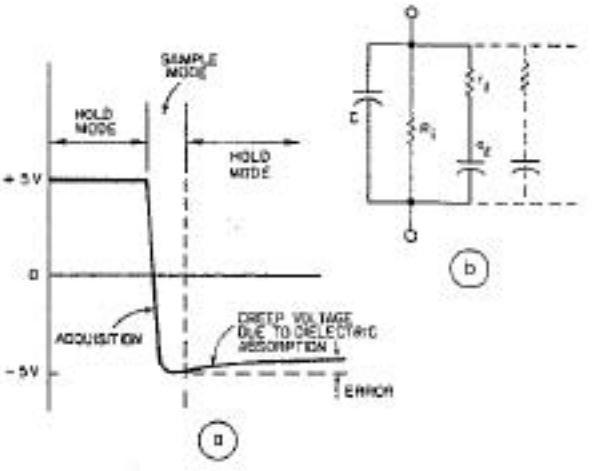
quisition time to 0.01%, or 50 ns to 0.1%.

Once a sample-hold has been selected, it may need a hold capacitor. These capacitors have somewhat unusual requirements. Some parameters, such as tempco of capacitance, matter very little, while others, such as dielectric absorption, are very important. Dielectric absorption affects the accuracy of the held voltage, although insulation resistance is quite important as well, for the same reason.

When high accuracy is needed, the range of satisfactory capacitor dielectrics narrows down to those in Table 2, which gives the important specs for them. Note that insulation resistance, which is quite high at 25 C, drops drastically at higher temperatures, such as 125 C. That's because insulation resistance decreases exponentially with temperature.

It won't stay put

If a capacitor is charged to a given voltage, discharged by shorting it, and then open-circuited again, its voltage will begin to creep up from zero toward the original voltage. The capacitor exhibits a "voltage memory" characteristic known as dielectric absorption, which occurs because the dielectric material



1. **In this example of dielectric absorption error,** the hold capacitor has been sitting at +5 V for some time. Although given enough time to settle completely during sampling, in hold mode, the capacitor's voltage creeps back toward +5 V (a). An imperfect capacitor with dielectric absorption can be modeled (b) by a perfect capacitor, C, the insulation resistance, R_i, and the long-time-constant components r_d and c_d, which simulate dielectric absorption.

doesn't polarize instantaneously—molecular dipoles need time to align themselves in an electric field. As a result, not all the energy stored in a charged capacitor can be quickly recovered upon discharge.

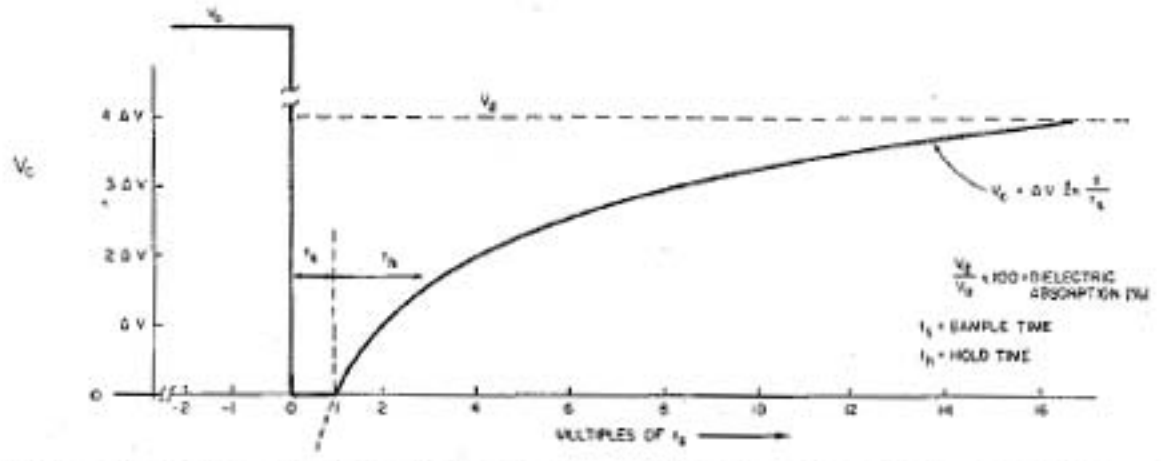
One way to measure dielectric absorption is to charge the capacitor to some voltage for 5 minutes, discharge it through a 5-Ω resistor for 5 seconds, then disconnect it. Measure the capacitor voltage five minutes later. The ratio of the measured voltage to the charging voltage, expressed in percent, is the dielectric absorption.

Even though the time scale in a sample-hold is usually far shorter than 5 min, dielectric absorption is still a source of error and should be taken into account. Assume the hold capacitor has been resting at a given voltage V_a when a different voltage is sampled and held. Once hold mode begins, the voltage on the capacitor will begin to creep back toward V_o. Thus, the dielectric absorption causes an error as illustrated in Fig. 1a.

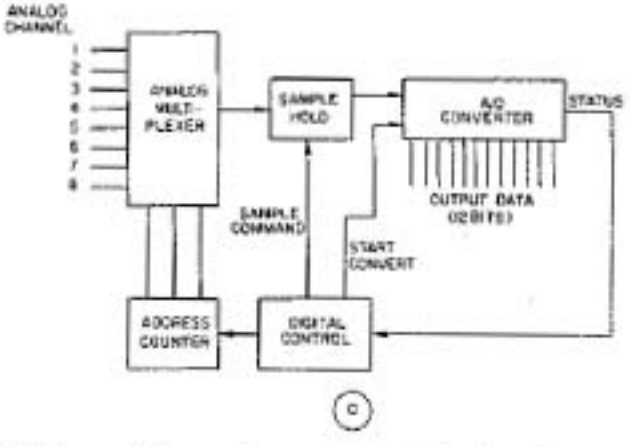
Fig. 1b shows a first-order approximation model of an imperfect capacitor, emphasizing dielectric absorption. Resistor R_i represents the insulation resistance and r_d and c_d represent the source of the dielectric absorption. (Actually, to model the absorption accurately, there should be a number of additional, parallel r_dc_d circuits with different values.)

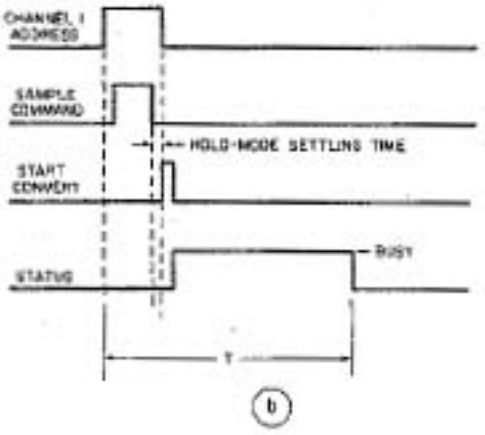
After capacitor C in the model has been rapidly discharged from a previous voltage and then open-circuited, the long time constant of r_dc_d causes some of the charge on c_d to transfer slowly to C, which develops a small voltage.

An accurate approximation to this "creep" voltage



2. A natural log function of time is an accurate approximation to the voltage creep caused by dielectric absorption. Before sampling, the capacitor has been holding a voltage V_o. A new sample charges the capacitor to a new voltage (zero, in this case, for simplicity), for period t_s. Once in hold mode, the capacitor reaches a voltage ΔV at time $2t_s$ and continues to creep toward V_o according to the logarithmic expression.





3. A data-acquisition system scans a number of analog inputs and converts them, one at a time, to digital form (a). The sample-hold provides an unchanging input to the converter until its conversion is complete. When it's finished, the STATUS line goes low to permit the next input in sequence to be converted (b).

caused by dielectric absorption is shown in Fig. 2. The curve is a natural log function of the shorting time, or sampling time (t_s). If the output creep voltage is measured at time $2t_s$, the voltage will be ΔV. If it is measured at $4t_s$, it will be $2\ \Delta V$ and at $8t_s$, $3\ \Delta V$. The equation for the curve is

$$V_c = \Delta V \ln \frac{t}{t_s}$$

where t_s is the sample time and t is the total time, or sample time plus hold time ($t_s + t_h$).

This equation is a good model, providing $V_c \ll V_o$. It does not hold for extremely long time periods, however, since V_c goes to infinity for infinite time. As shown, V_d represents the voltage measured to determine dielectric absorption at a specific time, which is a large multiple of t_s.

Capacitors can be measured and fitted to this curve. First, determine the value of ΔV from the measured dielectric absorption. The standard tests for dielectric absorption normally specify $t_h \gg t_s$, which is the correct way to make them. Since the equation is logarithmic, there is no asymptote to the curve, which continues to rise. For all practical purposes, however, a hold time much longer than the sample time will give a value for dielectric absorption that's far out on the curve.

Assume that the dielectric absorption is measured as 0.02% for a point at which $t_h = 15t_s$ or $t = 16t_s$. Then

$$\Delta V = \frac{2 \times 10^{-4}\ V_o}{\ln 16}$$

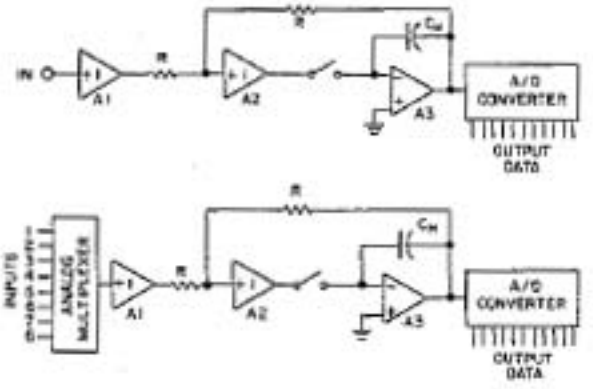
$$= 7.21 \times 10^{-4}\ V_o$$

where the dielectric absorption is defined as V_c/V_o at $t = 16t_s$. The resulting equation for creep voltage is

Table 2. Sample-hold capacitor characteristics

Type	Operating temperature range (°C)	Insulation resistance at 25 C (Megohm-microfarads)	Insulation resistance at 125 C (Megohm-microfarads)	Dielectric absorption
Polycarbonate	−55 to +125	5×10^6	1.5×10^4	0.05%
Metallized polycarbonate	−55 to +125	3×10^3	4×10^2	0.05%
Polypropylene	−55 to +105	7×10^3	5×10^2 (1)	0.03%
Metallized polypropylene	−55 to +105	7×10^3	5×10^2 (1)	0.03%
Polystyrene	−55 to +85	1×10^6	7×10^4 (2)	0.02%
Teflon	−55 to +200	1×10^6	1×10^6	0.01%
Metallized Teflon	−55 to +200	5×10^3	2.5×10^2	0.02%

(1) At 105 C
(2) At 85 C



4. **In a single-channel system, the settling time of the input buffer amplifier,** A_1, isn't critical because the amplifier can follow changes in the signal (a). With multiplexed inputs (b), however, the input buffer may take additional time to settle to the new value at the multiplexer's output when it switches channels.

$$V_e = 7.21 \times 10^{-5}\, V_o \ln \frac{t}{t_o}$$

Two factors reduce considerably the error due to dielectric absorption in typical applications of a sample-hold. First, the dielectric absorption measurement assumes a long initial charging time, say 5 minutes, whereas in a sample-hold a new voltage is held for a relatively short time. Second, the dielectric absorption is specified for a long open-circuit time compared with the shorting time, whereas in a sample-hold the hold time may be only slightly longer than the sample time.

The amount of creep voltage can also be reduced by remaining in the sample mode as long as possible relative to the hold time. The result of these factors is that a capacitor with a dielectric absorption of 0.02%, for instance, may contribute 0.005% or less error to the sample-hold, as the curve in Fig. 2 shows.

At this point, there may be reason to wonder if all the care and time needed to select a sample-hold is worth it. It certainly is. There's an abundance of applications for these devices.

Take a sample

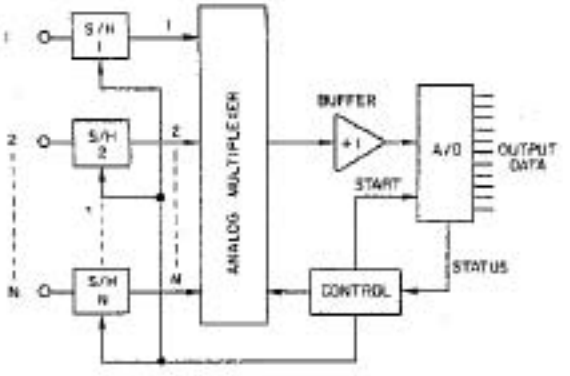
Undoubtedly one of the most common applications for a sample-hold is in data acquisition systems. A representative system would have an 8-channel multiplexer followed by a sample-hold and a 12-bit a/d converter (see Fig. 3a).

A logic-control circuit steps an address counter to sequence the analog multiplexer through the eight channels of analog data. For each channel the sample-hold acquires the input signal and switches into the hold mode.

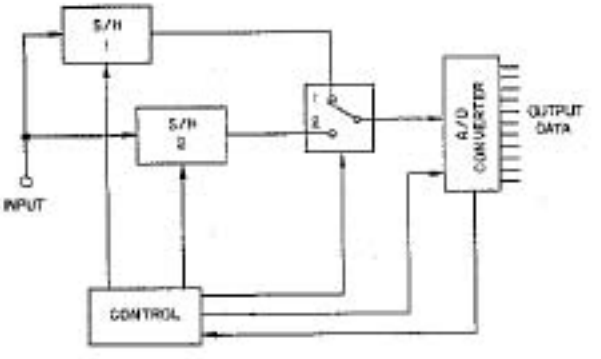
After allowing for the hold-mode settling time, a start-convert pulse initiates the a/d conversion, which is performed by successive approximation. After the conversion, the a/d converter's status output goes low.

When the conversion of this channel is finished, the analog multiplexer switches to the next channel while the output register of the a/d converter holds the digital word from the completed conversion. This word is then transferred out to a computer data bus. The sampling and conversion process is repeated for each analog channel in sequence.

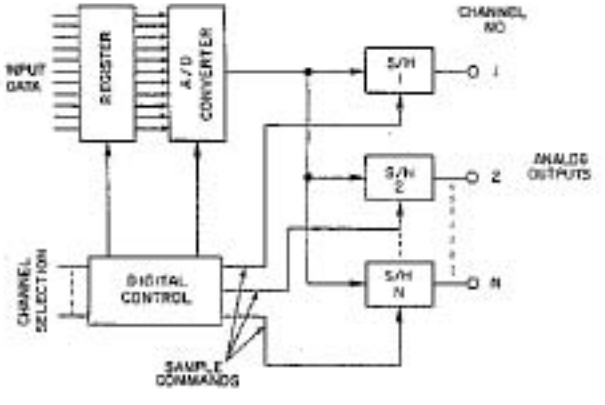
From Fig. 3b, T is the time required for the multiplexer and sample-hold to acquire the signal and for the a/d to convert it. Then 1/T gives the throughput rate, or the fastest rate at which the analog channels can be scanned. The rates for practical 12-bit data acquisition systems may vary from about 20 kHz up to 250 kHz corresponding to values of T that range from 50 μs down to 4 μs.



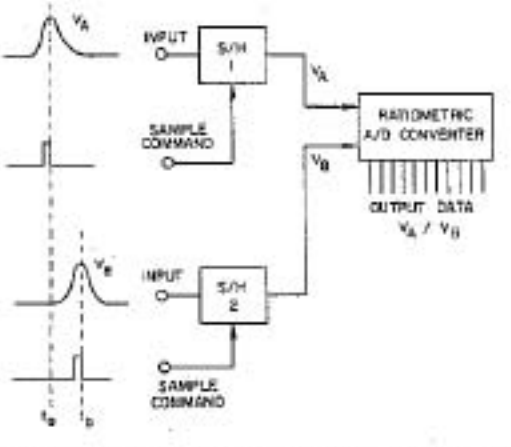
5. **A simultaneous sample-hold system** such as this samples all analog inputs at the same time and holds the samples for conversion. While one of the held voltages is being converted, the others mustn't droop too much.



7. **In an ultrafast a/d conversion system,** acquisition time in a sample-hold takes up a sizable part of the cycle. Interleaving two sample-holds like this lets one of them acquire while the other one's output is being converted.



6. **Multiplexed digital data** destined for a number of analog channels are reconstructed and distributed by a system like this one. Once the data for a channel have been converted, the sample-hold for that channel samples the d/a's output and retains it until the next data word for that channel comes in for conversion.



8. **Sample-holds can serve as temporary analog signal-storage devices.** The first sample-hold retains signal V_A's peak value so the converter can divide it by the peak value of input V_B, which comes by later.

Indeed, considering the many applications for sample-holds, a good number are used in conjunction with a/d converters. This is because the sample-hold greatly reduces the converter's aperture time.

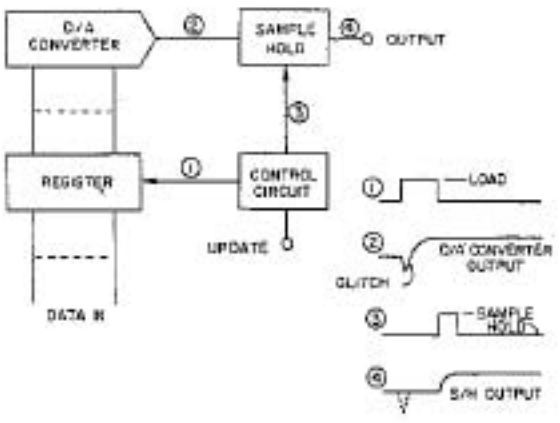
There are two important ways to use a sample-hold with an a/d converter, and each imposes a different requirement for the acquisition time. Fig. 4a shows a fast inverting sample-hold used ahead of an a/d converter, which converts just one input signal. The sample-hold continuously tracks the input signal until is goes into the hold mode.

Even while in the hold mode, input-buffer amplifier A_1 continues to track the input signal and only A_2 and A_3 affect the acquisition time. Acquisition is very fast because A_1 doesn't have to settle to a new voltage for every sample.

The same sample-hold can also follow an analog multiplexer, as in Fig. 4b. The required acquisition time will be longer here since A_1 must settle to a new voltage every time the multiplexer switches to a new channel. This means that the settling time of A_1 is now part of the acquisition time.

These two situations are significant because A_1's settling time may be larger than the acquisition time of the rest of the circuit. If it is, there'll be a great difference between the acquisition times of single-channel and multichannel acquisition systems.

Another important consideration in a data-acquisition system is interfacing the sample-hold to the a/d converter. A successive-approximation a/d converter, without an input buffer amplifier (which adds to the conversion time), has a resistor input that goes to an analog comparator's input terminal. Since the comparator is changing state during the successive-approximation conversion, the input impedance to the a/d changes. Since this happens at high speed, there



9. An output developed by many d/a converters for certain input-code transitions temporarily goes the wrong way. This transient, or "glitch," is undesirable in some applications and can be removed by sampling the converter's output after the glitch has gone by.

may be errors if the sample-hold's high-frequency output impedance isn't low enough. Furthermore, most sample-holds have higher output impedance in the hold mode than in the sample mode.

Sample all at once

Another way to use sample-holds in a data-acquisition system is illustrated in the simultaneous sample-hold system of Fig. 5. Here, data must be taken from all analog inputs at precisely the same time. To do this, the system requires a sample-hold per channel ahead of the analog multiplexer.

All the sample-holds are given the hold command simultaneously; then the multiplexer sequentially switches to each sample-hold output while the a/d converter converts it into digital form. Notice that a high-impedance buffer amplifier is required between the multiplexer and the a/d converter.

For this application, select sample-hold devices that are identical and have very small aperture-uncertainty times. In addition, the aperture delay times should be adjusted so that they all go into hold mode simultaneously. Another important criterion is that the droop rate be relatively low, since the last sample-hold in the system must hold its voltage until all the other outputs have been converted.

In an application which is the reverse of data acquisition, sample-holds can send signals from a channel to many destinations in a data-distribution system. Such a system (see Fig. 6) uses a single d/a converter and storage register together with a number of sample-holds to distribute data to a series of analog channels. As digital data are transferred into the d/a converter and its output changes, the appropriate sample-hold samples the new output voltage and then, once the converter's output has settled, switches into hold mode.

Each sample-hold circuit is updated in sequence as new data arrive, and holds its voltage until all the other sample-holds have been updated and the sequence returns to the first one. The sample-holds used must be chosen for the required acquisition time, which depends on the rate of updating each output, and for the desired droop error between updates.

Table 3. Sample-hold comparison

	Accuracy	Acquisition time	Price
Monolithic	0.1%	4 to 20 μs	$5 to $21
	0.01%	5 to 25 μs	
Hybrid	0.1%	25 ns	$35 to $135
	0.01%	1 to 10 μs	
Modular	0.1%	30 to 200 ns	$43 to $208
	0.01%	0.25 to 5 μs	

Back on the other side of the coin, ultrafast a/d converters can benefit from working with sample-holds. Interleaving two of them, as in Fig. 7, will eliminate acquisition time delay in many applications.

In such systems, the sample-hold's acquisition time can be a significant portion of the system's cycle time. With interleaved sample-holds, however, system cycle time depends only on the time required for a/d conversion.

Acquisition-time delay is eliminated by having one sample-hold acquire the next sample while the a/d is converting the output of the other sample-hold. The a/d converter, therefore, is simply switched from the output of one sample-hold to the other. The only dead time between conversions is the small delay in the analog switch.

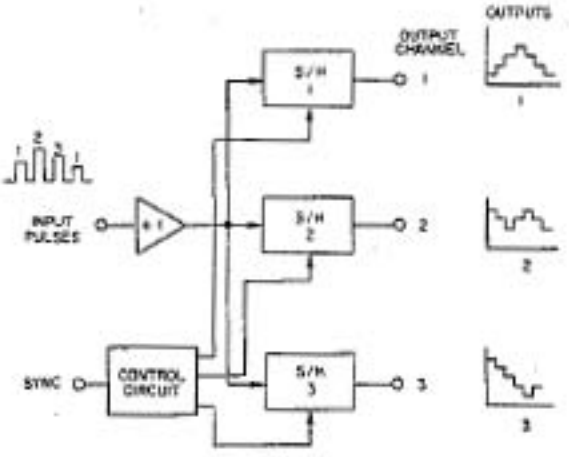
Conversion time can be decreased further, but doing it requires a second a/d converter, with one a/d operating off each sample-hold. The sample-holds then are operated sequentially, and the outputs of the a/d's have to be digitally multiplexed. In this way the throughput time is reduced to half the conversion time of either a/d converter.

In yet another a/d application, a sample-hold can delay or "freeze" analog data that exist only briefly; this information can then be combined with later data. This circuit (see Fig. 8) computes the ratio of two peaks that occur at different times, t_a and t_b.

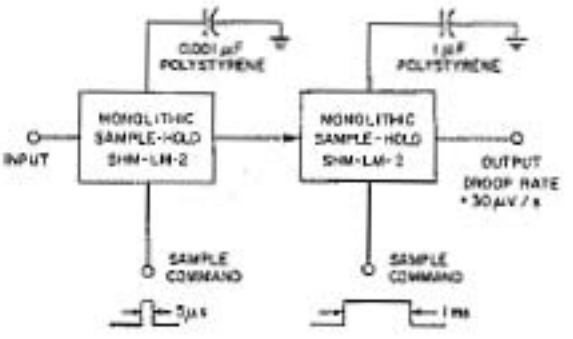
The first sample-hold stores the peak of signal V_A so that its value will still be available to the ratiometric a/d converter when the peak of signal V_B comes by. The second sample-hold stores the peak while the ratio is being converted to digital form.

Sample-holds deglitch

The list of conversion applications for sample-holds seems almost endless. Even big problems can be solved. For example, major code transitions in a d/a converter can cause unwanted voltage spikes as large as half the full-scale output voltage. These spikes,



10. **When analog signals are encoded** by pulse-amplitude modulation and then multiplexed, they can be sorted out and reconstructed by a set of sample-holds with properly timed sample commands. The time scale of the input is shorter than that of the outputs.



11. **Cascaded sample-holds acquire a signal quickly** and hold it for a long time with little droop. The first one needs to hold a signal only long enough for the second to acquire it. Typical acquisition would be 5 μs to 0.1%, with a droop rate of 30 μV/s.

commonly called glitches, are caused by switches in the converter that take longer to turn off than to turn on, or vice versa. The point is, in many d/a converter applications such as CRT displays and automatic testing, the converter output voltage should make a smooth, monotonic transition when it goes from one output voltage to the next.

This can be done by processing the d/a converter output with a sample-hold as shown in Fig. 9. First, a digital control circuit transfers the digital data from the register to the d/a converter. With this information at its input, the d/a converter generates a new output containing glitches. Once the glitches have settled, the sample-hold takes a sample of the new analog data and returns to hold mode before the d/a output changes again. The output of the sample-hold now has a smooth, monotonic transition between the old and the new levels.

Keeping up with high-speed analog d/a outputs generally requires ultrafast sample-holds for deglitching. Usually an inverting, current-input sample-hold follows the d/a converter to permit the highest possible operating speed. In fact, some specially designed d/a converters have self-contained sample-holds for deglitching, and not surprisingly, are called deglitched d/a converters.

Putting it all together

Data conversions aren't the only applications to benefit from sample-holds. As Part 1 of this series pointed out, a zero-order hold makes an excellent data-reconstruction filter and is commonly used in pulse-amplitude modulated (PAM) systems such as the one in Fig. 10. Here, time-division multiplexing is used to send a train of amplitude-modulated pulses over a transmission system, each pulse in sequence being the sample from one analog channel.

To demodulate this pulse train, the control circuit synchronously switches on each sample-hold in sequence as the pulse arrives, then returns it to hold mode until the next pulse from that channel arrives. Pulse by pulse, the output of each sample-hold becomes the reconstructed analog signal of the appropriate channel. A low-pass filter can also be added to each sample-hold output to smooth the reconstructed signals further.

In some analog-circuit applications, sampling should be quick, yet the sampled value should hold steady for a long time. Such conflicting needs produce conflicting requirements on the sample-hold. The best solution to the problem is to use two cascaded sample-hold devices, as in Fig. 11. The first sample-hold is a fast unit that acquires the input rapidly and accurately, while the second unit is a slow device with a very long hold time (low droop rate), perhaps on the order of minutes.

Basically, the first sample-hold must acquire the signal quickly and then hold the result long enough for the second sample-hold to acquire it. The errors need to be calculated carefully to be sure of meeting the accuracy requirements. In many cases two monolithic sample-holds in cascade might do the trick. External hold capacitors can then be chosen to give the desired performance.

For example, a 0.001-μF polystyrene capacitor would be a good choice for the first sample-hold to give an acquisition time of 5 μs to 0.1%. For the second one, a 1.0-μF capacitor would give an acquisition time of 10 ms but a hold time of 300 s to 0.1% accuracy. The resulting droop rate would be only 30 μV/s, which is quite low, indeed.■■