Seeing is Believing – Analog to Digital Converters make the difference in imaging applications

Introduction

Electronic image capture and digitization is one of the most subjective of all electronics disciplines. Its subjectivity is rooted in the unique interaction between the signal-processing capabilities of circuit hardware and the signal-processing capabilities of human physiology. Subtle, often insignificant, shortcomings in signal-processing hardware can easily cause image artefacts that are easily detected by the highly specific and extremely powerful skills of the human vision system. Understanding these interactions, especially in relation to an analog-to-digital converter (ADC), makes for a better image.

The need is universal

Virtually every application in which electronic images are digitally captured, stored, transmitted and manipulated requires the use of an ADC to transform the analog output of the system's photodetector into its digital equivalent. High-end imaging applications including medical, commercial graphic, photo-CD workstations and many forms of scientific imaging continue their insatiable demand for higher-resolution (12 to 18 bits), higher-speed (1 to 20 MHz) ADCs. In achieving image quality at this level, ADCs have become second in importance only to the photodetectors themselves.

Improving the speed/resolution product of ADCs requires performance trade-offs, and most ADC manufacturers are not making those trade-offs in favour of imaging. In response to the decreasing costs of digital computing power and the proliferation of digital signal processing (DSP) techniques, ADC manufacturers are often designing, testing and specifying new products with DSP applications in mind. Total harmonic distortion (THD), for example, is a DSP-based specification many manufacturers seek to optimise. It is however irrelevant to most imaging applications. Electronic image capture is not a DSP application. It is a traditional, time-domain, data-acquisition application.

Human trade-offs

The human visual system, impressive as it is, exhibits many trade-offs. While, due to an abundance of cones at the centre of our retinas, we are great at perceiving colours, our night vision is poor. The dynamic range of light intensities (brightness) we can detect is at least 100,000 to 1 (100 dB); however, the accuracy with which we perceive brightness is terrible. We all know when a light is bright, yet without the aid of scientific instruments we cannot determine exactly how bright it is. We are great at deciding which of two lights is brighter - especially in low-light conditions, but we are unable to tell how much brighter. Nor can we accurately determine when one light is two or three times as bright as another. Our vision system lacks absolute accuracy and is very non-linear.

Optimised for edges

Along with perceiving colour and detecting motion, the human visual system has been optimised for detecting edges; i.e., for detecting discontinuities. This ability is hardware-based and derives from the spatial density of visual receptors on our retinas. ADC converters, by their very nature, create discontinuities. They quantize or round off signals into predetermined levels. Improperly selected ADCs in imaging applications can create discontinuities/edges where they do not otherwise exist, or eliminate subtle edges that do exist. Because our eyes are optimised for detecting such things, we can spot these artefacts instantly.

The big specification

The single most important ADC specification for imaging applications is differential linearity error (also called differential non-linearity or DNL). In the case of the analog input / digital output transfer function of

a 4-bit ADC with associated photodetector, there are 16 output codes and 15 transitions at which the output increments from each code to the next. For the ideal ADC, each incremental step is exactly one least significant bit (LSB) wide. Each time the analog input increases by an amount equal to one LSB, the output counts up to the next code. An ADC exhibits a DNL error when it requires greater or less than the ideal increment in input signal to produce an increment in output code. hile the DNL specification focuses on each individual step in an ADC's transfer function, integral linearity error (INL) relates to the overall linearity of the device's Input/0utput transfer function over its full range.

In certain situations, sequential, relatively benign DNL errors can accumulate to produce significant INL errors. However, so long as the curve resulting from the analog input / digital output relationship remains comparatively smooth this is not disastrous in an imaging application. This is because human vision is not very linear; our visual linearity is less than ±1 percent, a level of performance normally associated with 6 to 7-bit ADCs.
Conversely, small numbers of moderately large DNL errors, because they result in sharp discontinuities, can have little effect on the overall INL of a converter yet cause havoc in imaging applications. This creates what is commonly referred to as a continuous tone wedge - a gradual linear excursion of grey tones from white to black. Precise, continuous tone wedges are often used to test or calibrate electronic imaging equipment.

If the tone wedge is digitised by a linear photodetector married to a perfect 4-bit ADC and then reconstructed on a good CRT or photographic paper, the result will be a step wedge with 16 distinct levels in its grey scale, corresponding to the 16 different output codes of the 4- bit ADC. Because our ideal ADC has perfect DNL, the incremental brightness is the same from step to step.

If the ADC has a series of cumulative negative DNL errors followed by a series of positive DNL errors, the result, as discussed, can be a rather severe positive INL bowing. The opposite condition results in negative bowing. In both cases, the calculated INL (using the endpoint definition) is equal to 1 LSB (6.6 percent of full scale). While this magnitude of INL error is detectable by the human vision system, neither of the two non-linear step wedges is particularly offensive. A moderately large positive DNL error at mid-scale, followed immediately by an equally large negative DNL error, results in respectable overall INL. But in this case our ability to detect edges makes the discontinuities stand out, even though the overall transfer function has better INL than the scenario previously described. (Where a series of cumulative negative DNL errors is followed by series of positive DNL errors or the opposite condition).

ADCs for imaging applications must have excellent DNL. As a minimum, the specified maximum DNL error should not exceed +½ LSB. Many contemporary ADCs list ±1 LSB as a maximum DNL error, others meanwhile list only typical values and rely more heavily on their FFT specifications. Recently introduced imaging-specific devices from C&D Technologies guarantee ±¼ LSB maximum DNL errors.

Photo noise
Most imaging systems seek to have overall system noise limited by the photodetector and not the signal-processing electronics. In the context of this article, ADC noise can be thought of as instantaneous DNL errors that are random in both space and time. If given incident light conditions are expected to yield a given digital output code, ADC noise can easily result in the next higher or lower code.
A straightforward manner in which to narrow the selection of ADCs is to apply a DC input signal to a continuously converting device and observe the number of different output codes appearing. Practitioners of this approach commonly describe devices as having two codes of noise or three codes of noise, etc. For this test, widely known in the industry as the 'DC noise measurement of the ADC' test, it is common to use a grounded input. - All ADC products from C&D Technologies are tested for the DC Noise parameter.
Virtually all of today's high-resolution ADCs exploit the so-called subranging architecture, and for these devices, the noisiest code transitions do not occur around zero. A good set-up must be able to vary the ADC input throughout its full range and perform the DC noise test.

Additional critical capabilities

Full-scale step response and overvoltage recovery time are two relevant ADC specs that are easily understood in the context of scanned imaging systems employing CCDs. In these systems, it is possible to encounter a full-scale change between adjacent pixels. A good imaging ADC must be able to sequentially acquire and accurately convert both signal extremes.

Because most of today's sampling ADCs do not bring the output of their sampling front-end to a device pin, listed specifications for large-signal bandwidth, small-signal band-width, sample/hold (S/H) slew rate and S/H acquisition time are difficult to verify and can be misleading. ADCs that do not specify how they will perform under the above conditions need to be carefully evaluated.

The test for full-scale step response is straightforward. Immediately after the S/H front-end goes into hold, the ADC section begins converting. This event is usually controlled by a timing signal brought out to a device pin. Once the conversion has begun, the input can be changed without affecting its results. In the step test, the ADC first converts a static signal at one extreme of its input range. When the S/H goes into hold, the input is driven to its other extreme. When the S/H is released back into signal-acquisition mode, it sees the new input and is forced to slew its full range and settle in order to accurately acquire the new input (see Figure 1).

Overvoltage recovery time

Whether caused by greater-than-expected light intensities or longer-than-appropriate exposure/integration times, imaging photodetectors can quickly saturate and become non-linear. Saturation conditions can ripple through subsequent analog-signal-processing circuitry, and it is not uncommon for ADCs to experience input voltages that exceed their nominal ranges. Though most ADCs will saturate under these conditions (driving their output to all 1s or all Os), the important question is how quickly they recover from an overvoltaged input. Manufacturers frequently specify an overvoltage recovery time with the implication that users should wait before continuing to collect accurate data. This stop-and-wait approach is inappropriate for imaging. It's more appropriate to simply note how many conversions should be discarded, or at least flagged, before continuing with accurate data.

Overvoltage recovery times can vary widely with the magnitude and/or the duration of the infraction. ADC manufacturers typically specify an overvoltage recovery time for a 10 percent overvoltage. The same specs may not apply for a 20 percent overvoltage.

The best advice is to test any ADCs that you may be considering under conditions appropriate to your application. Ideally, the ADC you select should be able to perform accurately on the very next conversion following the removal of the overvoltage condition. If it cannot, appropriate clamping, assuming it does not slow things down, is always a good idea.

For years, C&D Technologies has been offering high resolution ADC that are optimised for imaging applications. Recently, the company has introduced a new line of products that integrate a correlated double sampler (CDS), a high resolution ADC, plus other supporting circuits in a single package. This ADCDS product family provides a complete solution that guarantees all the specification and parameters that are required for imaging applications.

Figure 1: When testing a sampling ADC for full-scale response, the input signal can begin to change as soon as the front-end sample / hold goes into 'hold'.