Hardware User Guide

AQUILA 6UL SOM

Revision History

Revision	Date	Author	Change Description
0.1	05/02/2017	RF PD	Preliminary version
1.0	05/05/2017	RF PD	Add PCB landing pattern

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1. Introduction

This document describes setting up and using the Evaluation Kit for the AQUILA 6UL System-On-Module (SOM). AQUILA 6UL SOM is compatible with Android Things™ and Linux applications.

1.1 References

[1] Murata, “SP-KL1DX-F: W-LAN+Bluetooth Combo Module Data Sheet for 802.11b/g/n + Bluetooth 4.1/EDR”, June19, 2015.
[2] NXP, “IMX6ULRM: i.MX 6UltraLite Applications Processor Reference Manual”, April 2016
[3] NXP, “IMX6ULCEC : i.MX 6UltraLite Applications Processors for Consumer Products datasheet”, April 2016
[4] Kingston, “Embedded Multi-Media Card (e•MMC™ 5.1) EMMC04G-M627-X01U”
[5] Micron, “DDR3L SDRAM : MT41K256M16TW-107P datasheet”, April 2016
[6] NXP, “MC32PF3000A7EP: Power management integrated circuit (PMIC) for i.MX 7 & i.MX 6SL/SX/UL”, March 2016
[7] NXP, “MCIMX6UL-BB schematics: SPF-28616”, October 18, 2016
[8] Hirose Electric Co., *DF40C-80DP-0.4(51) Specification Sheet*, August 2008
[9] Hirose Electric Co., *DF40 Series 0.4mm Pitch, 1.5 to 4.0mm Height, Board-to-Board and Board-to-FPC Connectors,* Dec 2016

2. AQUILA 6UL SOM Evaluation Kit

The AQUILA 6UL SOM Evaluation Kit (SOM-EVK) provides a platform for evaluating and developing applications on the AQUILA 6UL SOM for Android Things™ and Linux.

Figure 1 AQUILA 6UL SOM EVK

The SOM evaluation kit contains a complete hardware setup out-of-the-box, including a 5V DC supply plug, a micro-USB cable, a SOM mounted on an interposer carrier board and an iMX6ULEVK-BB board.

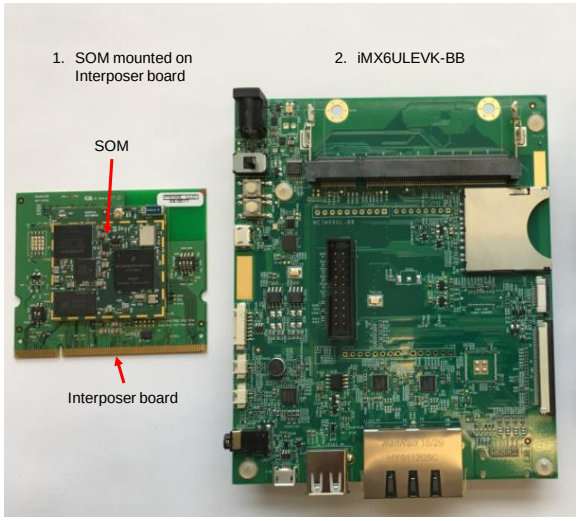


Figure 2 Key out-of-box kit components

2.1 SOM overview

The AQUILA SOM is a turnkey platform for Internet-of-Things (IoT) devices with integrated onboard antenna, Wi-Fi/BT, i.MX6UL application processor, DDR3L memory, eMMC and PMIC. The SOM provides 3.3V supplies and exports a rich selection of communication interfaces through 2 high speed Hirose 80-pins board-to-board connectors. These interfaces and the internal functions of the SOM are detailed in Section 3.

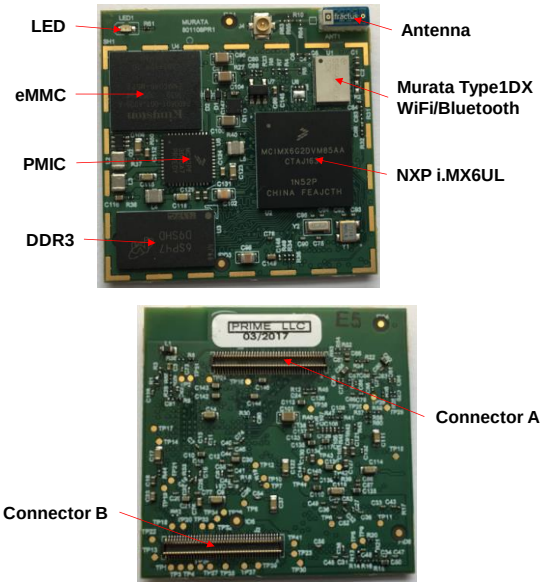


Figure 3 SOM top and bottom views

2.2 iMX6ULEVK-BB

The iMX6ULEVK-BB connects the SOM to the peripherals and networking interfaces supplied by the iMX6ULEVK. This baseboard is the same one as that used for the iMX6ULEVK, the details of which can be obtained from the NXP website for the i.MX6UltraLite Evaluation Kit.

- Power Switch: connects/disconnects the 5 V power supply to the SOM-EVK
- System Reset button may be pressed to reset the system and begin a new boot sequence
- USB OTG port may be used for flashing image to the SOM
- Debug USB port may be used as a debug serial console for the application

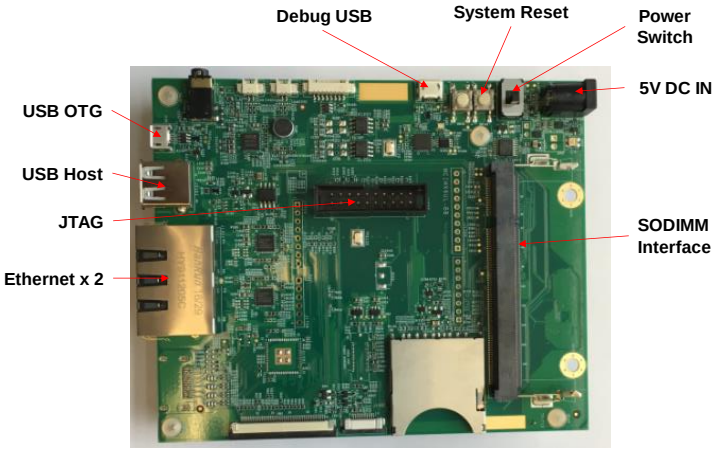


Figure 4 iMX6ULEVK-BB

2.3 Interposer carrier board

The Interposer board is a carrier board that bridges the signals of the SOM's board-to-board connectors to the SODIMM connector of the iMX6ULEVK-BB. It also contains two switches for selecting the boot mode and the boot device in the SOM as well as the boot configuration resisters. By default, the SOM is configured to boot from eMMC at power up.

WARNING: It is important that the SOM be placed properly on the Interposer board. The white rectangle on the Interposer board indicating the proper orientation and position of the SOM should be used to ensure the correct alignment.

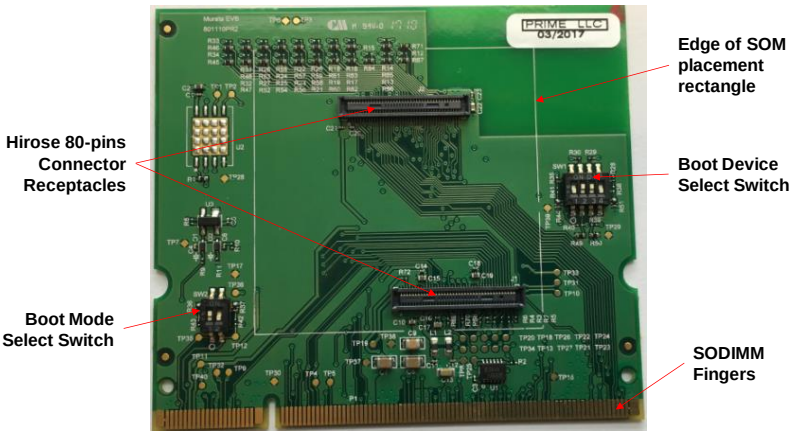


Figure 5 Interposer board

D1/BOOT_MODE1	D2/BOOT_MODE0	Boot mode
OFF	ON	Serial downloader
ON	OFF	Internal Boot (default)

Table 1 SW2 Boot mode settings

D1	D2	D3	D4	Boot device
OFF	ON	ON	OFF	eMMC boot (default)

Table 2 SW1 Boot device settings

2.4 Assemble the SOM-EVK

Carefully remove the SOM-EVK components from their respective protective bags and assemble the EVK as follows:

- The SOM should already be properly mounted on the Interposer board. Otherwise, do the following to connect the SOM to the Interposer:
  - Align the SOM over the corresponding white placement rectangle drawn on the Interposer board
  - Gently press down on the sides of the SOM PCB to insert the module. Avoid pressing on any ICs to help prevent damaging those components.
- Insert the Interposer carrier board into the SODIMM connector on the iMX6ULEVK-BB.
  - Ensure that the SOM is facing up
  - Align the notch on the finger of the Interposer board and the SODIMM connector
  - The properly inserted Interposer board should be held in place by the clips on the SODIMM connector, as shown in Figure 6.
- Ensure that the Power Switch in the iMX6ULEVB-BB is in the OFF position which is the defaut setting. The switch is located next to the 5V power supply connector. When OFF, its position is toward the SODIMM connector and away from the edge of the board.
- Connect the 5V power adapter to the power supply connector on the iMX6ULEVK-BB.
- Connect the micro-USB connector to USB OTG connector on the iMX6ULEVK-BB.

- Turn the Power Switch to ON and the SOM should powerup into the fastboot mode if the default SOM configuration and boot switches have not been changed.

A snapshot of the SOM EVK setup is shown below; the SOM is mounted on an Interposer board which in turn is connected to the iMX6ULEVK-BB through the SODIMM interface.

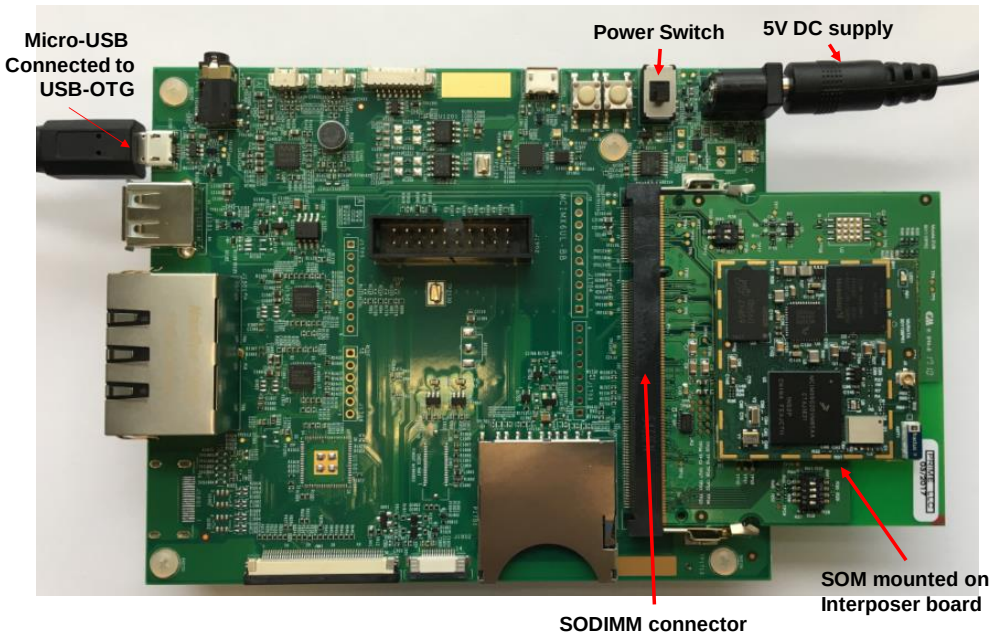


Figure 6 Assembled SOM-EVK

3. AQUILA 6UL System-on-Module (SOM)

The AQUILA 6UL System-on-Module (SOM) is a turnkey platform for Internet-of-Things (IoT) devices with integrated onboard antenna, Wi-Fi/BT, application processor, DDR3L memory, eMMC and PMIC. The SOM is powered by 5V DC; it provides 3.3V supplies and a rich set of communication interfaces through 2 high speed 80-pins board-to-board connectors. A block diagram of the SOM module is shown in Figure 7.

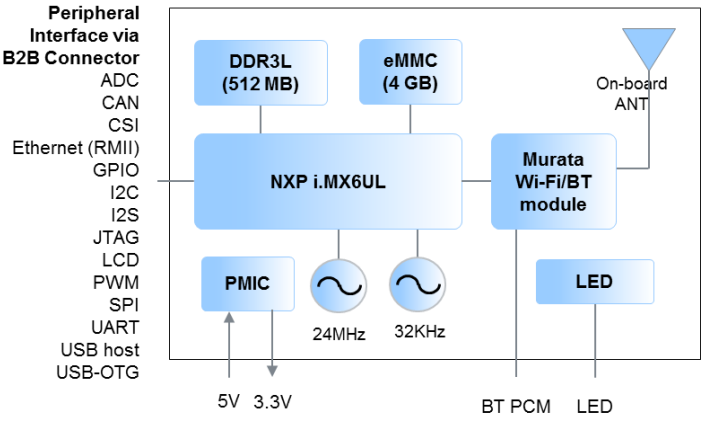


Figure 7 AQUILA 6UL SOM block diagram

3.1 Key components

The AQUILA SOM is powered by a high performance, ultra-efficient NXP i.MX 6UltraLite ([2][3]) processor with an advanced implementation of an ARM® Cortex®-A7 core. Detailed datasheet, reference manual and application notes can be obtained from the NXP i.MX 6UltraLite website. A block diagram of the i.MX6UL is shown below.

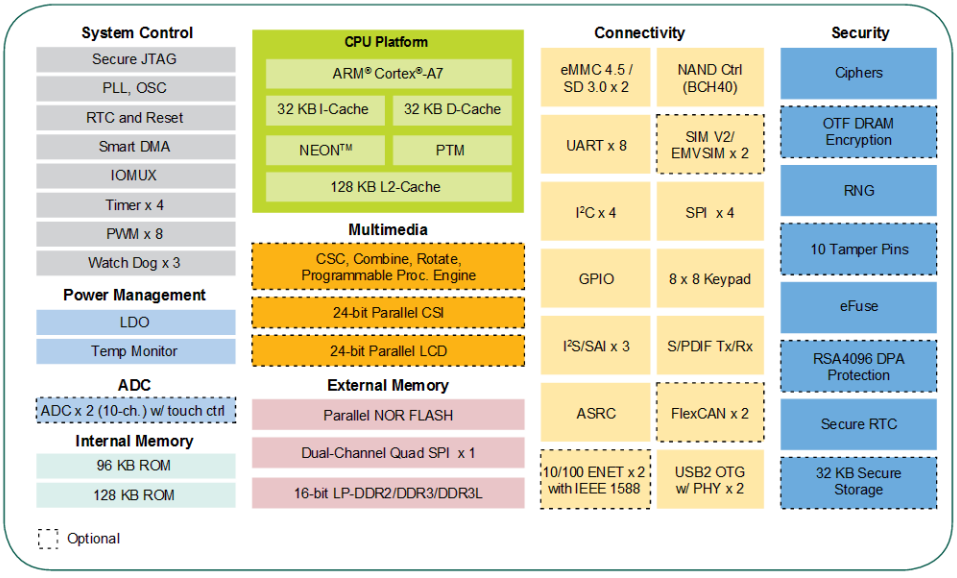


Figure 8 i.MX 6UltraLite applications processor block diagram

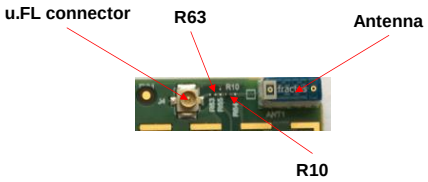
Besides the i.MX6UL processor, the following components are mounted on the SOM:

- Murata Type1DX 802.11b/g/n WiFi/BT 4.1 module based on Cypress BCM4343W [1]
- NXP MC32PF3000A7EP power management IC [6]

- Kingston EMMC04G-M627-A01 4GB eMMC flash [4]
- Micron MT41K256M16TW-107P 512 MB DDR3L [5]

3.2 RF interface

The out-of-box configuration of the SOM uses the onboard antenna for WiFi and Bluetooth; there is also an u.FL connector for RF evaluation. Antenna selection is based on the configurations shown below.



Selection	R63	R10	Description
Onboard antenna	open	0Ω	Default configuration
u.FL connector	0Ω	open	RF testing usage

Figure 9 Antenna selection options

3.3 Internal interfaces

SOM supports the following internal interfaces between its different subsystems.

- Clock interface: 24 MHz and 32KHz crystals for i.MX6UL
- SDIO interface between Type1DX and i.MX6UL for WiFi control
- UART interface: between Type1DX and i.MX6UL for BT control
- GPIOs control interface: between Type1DX and i.MX6UL
- eMMC interface between eMMC flash and i.MX6UL for code and data storage
- MMDC interface: between i.MX6UL and DDR3L
- I2C interface: between i.MX6UL and PMIC

3.3.1 Clock interfaces

The i.MX6UL is supplied with a 24MHz high speed clock connected to XTALI and XTALO.

There is also a 32KHz clock connected to RTC_XTALI and RTC_XTALO.

3.3.2 WiFi and Bluetooth interfaces

The i.MX6UL connects to the Type1DX via SDIO and UART interfaces and a set of GPIOs for control. The following internal SOM connections are made between the i.MX6UL and the Type1DX. These interfaces use only 3.3V signals.

Type1DX	i.MX6UL		Description
	Pad	ALT function	
WL_REG_ON	SNVS_TAMPER1	GPIO5_IO01	Take WLAN core in and out of reset
WL_GPIO_0_HOST_WAKE	SNVS_TAMPER3	GPIO5_IO03	WLAN out-of-band interrupt (OOB IRQ)
SDIO_CMD	SD1_CMD	SD1_CMD	SDIO_CMD

SDIO_CLK	SD1_CLK	SD1_CLK	SDIO_CLK
SDIO_DATA_3	SD1_DATA3	SD1_DATA3	SDIO_DATA_3
SDIO_DATA_2	SD1_DATA2	SD1_DATA2	SDIO_DATA_2
SDIO_DATA_1	SD1_DATA1	SD1_DATA1	SDIO_DATA_1
SDIO_DATA_0	SD1_DATA0	SD1_DATA0	SDIO_DATA_0
BT_UART_RXD	UART2_TX_DATA	UART2_TX_DATA	BT_UART_RXD
BT_UART_TXD	UART2_RX_DATA	UART2_RX_DATA	BT_UART_TXD
BT_UART_CTS_N	UART3_TX_DATA	UART2_CTS_B	BT_UART_CTS
BT_UART_RTS_N	UART3_RX_DATA	UART2_RTS_B	BT_UART_RTS
BT_REG_ON	UART3_RTS_B	GPIO1_IO27	Take Bluetooth core in and out of reset
BT_HOST_WAKE	SNVS_TAMPER6	GPIO5_IO6	Take i.MX6 out of sleep mode
BT_DEV_WAKE	UART3_CTS_B	GPIO1_IO26	Take Bluetooth core out of sleep mode

Table 3 Type1DX-i.MX6UL interface (SOM internal)

The PCM and slow clock interface for the Type1DX are brought out to the SOM connector as listed below:

SOM pad	Type1DX	Description
BT_PCM_OUT	BT_PCM_OUT	PCM Data from BT
BT_PCM_CLK	BT_PCM_CLK	PCM Clock
BT_PCM_SYNC	BT_PCM_SYNC	PCM Sync
BT_PCM_IN	BT_PCM_IN	PCM Data to BT
WB_LO_IN	LPO_IN	External sleep clock input (32.768kHz). Tie to GND if not used.

Table 4 Type1DX interface exported to board-to-board connector

3.3.3 eMMC flash interface

The SOM incorporates a 4GB Kingston eMMC flash memory ([4]). The following connections are made between eMMC interface of i.MX6UL and the flash. The eMMC flash only supports 3.3V operation.

eMMC flash	i.MX6UL		Description
	Pad	ALT function	
RST_n	NAND_ALE	SD2_nRST	Hardware Reset
CMD	NAND_WE_B	SD2_CMD	Command
CLK	NAND_RE_B	SD2_CLK	Clock
DAT7	NAND_DATA07	SD2_DATA7	Data (8-bit width)
DAT6	NAND_DATA06	SD2_DATA6	

DAT5	NAND_DATA05	SD2_DATA5	
DAT4	NAND_DATA04	SD2_DATA4	
DAT3	NAND_DATA03	SD2_DATA3	
DAT2	NAND_DATA02	SD2_DATA2	
DAT1	NAND_DATA01	SD2_DATA1	
DAT0	NAND_DATA00	SD2_DATA0	

Table 5 i.MX6UL and eMMC flash connections

3.3.4 DRAM interface

The SOM contains a 512MB DDR3L SDRAM from Micron [5]. The MMDC interface for the i.MX6UL is used to communicate with the DDR.

3.4 Power supply interface

The SOM is powered by an external 5V power supply which drives the PMIC and an onboard LDO, as follows:

- The PMIC provides power to the SOM for i.MX6UL, DDR, eMMC, Type1DX and external IOs.
- The PMIC provides power to external peripherals (up to 500mA and 10 mA, respectively, through VIO_3V3 and DCDC_3V3).
- The LDO provides the 3.3V supply for VDD_SNVS_3V3.

The following signals are exported from the SOM. They may be used to perform reset and power on control of the PMIC and i.MX6UL application processor.

SOM	PF3000	i.MX6UL pad	Description
PMIC_ON_REQ	PWRON	SNVS_PMIC_ON_REQ	Power ON/OFF input from i.MX or button to turn on/off PMIC
MCU_ONOFF	-	ONOFF	Power ON/OFF i.MX
MCU_nPOR	RESETBMCU	POR_B	PMIC open drain reset output to i.MX
PMIC_nINT	INTB	-	Open drain interrupt signal from PMIC

Table 6 On/Off and Reset control

3.4.1 Input constraint

Each Hirose connector pin has 300mA current rating[8]. The application should provide power through all nine (9) VSYS pins to limit the current through each individual VSYS pins.

3.4.2 Power management integrated circuit (PMIC) interface

The SOM uses the NXP PMIC MC32PF3000A7EP [6]. The following connections are made between PMIC interface of i.MX6UL and the PMIC.

PF3000	i.MX6UL		Description
	Pad	ALT function	
PWRON	SNVS_PMIC_ON_REQ	PMIC_ON_REQ	Power ON/OFF input from i.MX or button
RESETBMCU	POR_B	POR_B	Open drain reset output to i.MX
STANDBY	CCM_PMIC_STBY_REQ	-	i.MX signal to PMIC standby signal
SD_VSEL	-	-	Pulldown via 10KΩ to select VCC_SD = 2.85 to 3.3V
SCL	UART4_TX_DATA	I2C1_SCL	I2C clock
SDA	UART4_RX_DATA	I2C1_SDA	I2C data

Table 7 PMIC-i.MX6 control interface mapping

3.5 Signals reserved for SOM

The following lists the i.MX6UL signals used by the module and the function mapping must not be changed by the customer application. The “SOM only” signals are not brought out to the connectors.

Components	i.MX6UL	Actual signal	SOM only
WiFi	SD1_CMD	SDIO_CMD	×
	SD1_CLK	SDIO_CLK	×
	SD1_DATA3	SDIO_DATA_3	×
	SD1_DATA2	SDIO_DATA_2	×
	SD1_DATA1	SDIO_DATA_1	×
	SD1_DATA0	SDIO_DATA_0	×
	SNVS_TAMPER1	WL_REG_ON	×
	SNVS_TAMPER3	WL_HOST_WAKE	×
Bluetooth	UART2_TX_DATA	BT_UART_RXD	×
	UART2_RX_DATA	BT_UART_TXD	×
	UART3_TX_DATA	BT_UART_CTS	×
	UART3_RX_DATA	BT_UART_RTS	×
	UART3_RTS_B	BT_REG_ON	×
	SNVS_TAMPER6	BT_HOST_WAKE	×
	UART3_CTS_B	BT_DEV_WAKE	×
eMMC	NAND_ALE	SD2_nRST	×
	NAND_WE_B	SD2_CMD	×
	NAND_RE_B	SD2_CLK	×
	NAND_DATA07	SD2_DATA7	×
	NAND_DATA06	SD2_DATA6	×

	NAND_DATA05	SD2_DATA5	×
	NAND_DATA04	SD2_DATA4	×
	NAND_DATA03	SD2_DATA3	×
	NAND_DATA02	SD2_DATA2	×
	NAND_DATA01	SD2_DATA1	×
	NAND_DATA00	SD2_DATA0	×
PMIC	SNVS_PMIC_ON_REQ	PWRON	
	POR_B	RESETBMCU	
	CCM_PMIC_STBY_REQ	STANDBY	×
	UART4_TX_DATA	I2C1_SCL	
	UART4_RX_DATA	I2C1_SDA	
DDR3L	*	All MMDC pins	×

Table 8 SOM internal i.MX6UL signals

3.6 Board-to-board connectors

The SOM provides both 3.3V supplies and a rich selection of communication and control interfaces through two (2) high-speed Hirose DF40C-80DP-0.4V(51) 80-pins board-to-board connectors [8]. A compatible mating receptacle is the Hirose DF40C-80DS-0.4V(51) with height of 2.0mm or more [9].

3.6.1 Power for external peripherals

The SOM provides 3.3V to the external peripherals through the following pins:

- VIO_3V3 (2 pins): up to 500mA
- DCDC_3V3: up to 10mA

3.6.2 Indication LED

SOM has an LED onboard which can be connected to a GPIO for indication purposes. The LED is powered by the DCDC_3V3 supply through a 330Ω resister.

LED	Description
LED	On when LED pad is driven low

Table 9 LED control mapping

3.6.3 Peripheral control

The SOM simplifies IoT development by integrating the DDR3, eMMC, PMIC and WiFi/BT with the i.MX6UL processor. Apart for the pins dedicated for those interfaces, the SOM exports other signals from the i.MX6UL and provides the following interfaces for external device communication and control.

- UART interface
- USB-OTG interface
- USB host interface
- SPI interface
- QSPI interface
- PWM interface

- LCD interface
- JTAG interface
- I2S interface
- I2C interface
- GPIO interface
- Ethernet interface (RMII)
- CSI interface
- CAN interface
- ADC interface

Subject to the constraints described in Section 3.5, the application may choose the specific IO MUX as detailed in the i.MX6UL reference manual [2].

3.6.4 SOM pinout summary

The SOM connector pinout is summarized below. The location of Connector A and Connector B are shown in Figure 10.

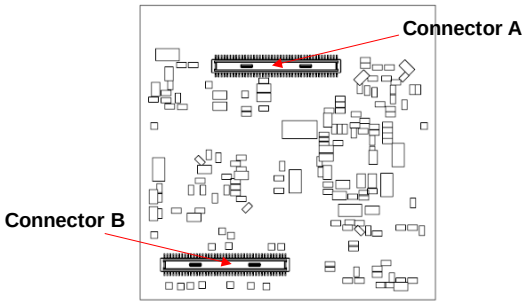


Figure 10 SOM board-to-bard connectors

Pin number	Pin name	iMX/1DX/PMIC pad		Pin number	Pin name	i.MX6 pad
A1	VSYS	5V to PMIC		A2	GND	GND
A3	VSYS	5V to PMIC		A4	GND	GND
A5	VSYS	5V to PMIC		A6	ADC_VREFH	ADC_VREFH
A7	VSYS	5V to PMIC		A8	GND	GND
A9	VSYS	5V to PMIC		A10	USB_HST_PWR	GPIO1_IO02
A11	VSYS	5V to PMIC		A12	GND	GND
A13	VSYS	5V to PMIC		A14	USB_HST_DP	USB_OTG2_DP
A15	VSYS	5V to PMIC		A16	USB_HST_DN	USB_OTG2_DN
A17	VSYS	5V to PMIC		A18	GND	GND
A19	VIO_3V3	PMIC VPERI_3V3		A20	USB_HST_VBUS	USB_OTG2_VBUS
A21	VIO_3V3	PMIC VPERI_3V3		A22	USB_HST_OC	GPIO1_IO03
A23	DCDC_3V3	PMIC DCDC_3V3		A24	USB_OTG_CHD	USB_OTG1_CHD
A25	VDD_SNVS_3V3	VDD_SNVS_IN		A26	GND	GND

Pin number	Pin name	iMX/1DX/PMIC pad		Pin number	Pin name	i.MX6 pad
A27	GND	GND		A28	ADCx_IN9	GPIO1_IO09
A29	WB_LO_IN	Type1DX.37		A30	BLT_PWM	GPIO1_IO08
A31	RESERVED			A32	ADCx_IN5	GPIO1_IO05
A33	PMIC_PWRON	PMIC PWRON		A34	I2C3_SCL	ENET2_RX_DATA0
A35	MCU_ONOFF	ONOFF		A36	I2C3_SDA	ENET2_RX_DATA1
A37	MCU_nPOR	POR_B		A38	I2C4_SCL	ENET2_RX_EN
A39	BOOT0	BOOT_MODE0		A40	I2C4_SDA	ENET2_TX_DATA0
A41	BOOT1	BOOT_MODE1		A42	SPI4_MOSI	ENET2_TX_EN
A43	LED	User LED control		A44	SPI4_MISO	ENET2_TX_CLK
A45	CAN2_TX	UART2_CTS		A46	SPI4_NSS	ENET2_RX_ER
A47	CAN2_RX	UART2_RTS		A48	SPI4_SCK	ENET2_TX_DATA1
A49	I2C1_SCL	UART4_TX_DATA		A50	GND	GND
A51	I2C1_SDA	UART4_RX_DATA		A52	USB_OTG_DN	USB_OTG1_DN
A53	UART1_TXD	UART1_TX_DATA		A54	USB_OTG_DP	USB_OTG1_DP
A55	UART1_RXD	UART1_RX_DATA		A56	GND	GND
A57	UART1_CTS	UART1_CTS		A58	USB_OTG_VBUS	USB_OTG1_VBUS
A59	UART1_RTS	UART1_RTS		A60	USB_OTG_ID	GPIO1_IO00
A61	PMIC_nINT	PMIC INTB		A62	USB_OTG_OC	GPIO1_IO01
A63	RESERVED			A64	USB_OTG_PWR	GPIO1_IO04
A65	RESERVED			A66	UART5_TXD	UART5_TX_DATA
A67	RESERVED			A68	UART5_RXD	UART5_RX_DATA
A69	RESERVED			A70	JTAG_TMS	JTAG_TMS
A71	BT_PCM_OUT	Type1DX.10		A72	JTAG_TCK	JTAG_TCK
A73	BT_PCM_CLK	Type1DX.11		A74	JTAG_TDI	JTAG_TDI
A75	BT_PCM_SYNC	Type1DX.8		A77	JTAG_TDO	JTAG_TDO
A77	BT_PCM_IN	Type1DX.9		A78	JTAG_nTRST	JTAG_TRSTB
A79	GND	GND		A80	GND	GND

Table 10 SOM Connector A pinout

Pin number	Pin name	i.MX6 pad		Pin number	Pin name	i.MX6 pad
B1	NVCC_CSI	NVCC_CSI		B2	GND	GND
B3	CSI_VSYNC	CSI_VSYNC		B4	LCD_ENABLE	LCD_ENABLE
B5	CSI_HSYNC	CSI_HSYNC		B6	LCD_CLK	LCD_CLK
B7	GND	GND		B8	GND	GND
B9	CSI_MCLK	CSI_MCLK		B10	LCD_HSYNC	LCD_HSYNC
B11	GND	GND		B12	LCD_VSYNC	LCD_VSYNC

Pin number	Pin name	i.MX6 pad		Pin number	Pin name	i.MX6 pad
B13	CSI_PIXCLK	CSI_PIXCLK		B14	LCD_RESET	LCD_RESET
B15	GND	GND		B16	GND	GND
B17	CSI_DATA07	CSI_DATA07		B18	LCD_DATA00	LCD_DATA00
B19	CSI_DATA06	CSI_DATA06		B20	LCD_DATA01	LCD_DATA01
B21	CSI_DATA05	CSI_DATA05		B22	LCD_DATA02	LCD_DATA02
B23	CSI_DATA04	CSI_DATA04		B24	LCD_DATA03	LCD_DATA03
B25	CSI_DATA03	CSI_DATA03		B26	LCD_DATA04	LCD_DATA04
B27	CSI_DATA02	CSI_DATA02		B28	LCD_DATA05	LCD_DATA05
B29	CSI_DATA01	CSI_DATA01		B30	LCD_DATA06	LCD_DATA06
B31	CSI_DATA00	CSI_DATA00		B32	LCD_DATA07	LCD_DATA07
B33	QSPI_nSS0	NAND_DQS		B34	LCD_DATA08	LCD_DATA08
B35	QSPI_DATA0	NAND_READY_B		B36	LCD_DATA09	LCD_DATA09
B37	QSPI_DATA1	NAND_CE0_B		B38	LCD_DATA10	LCD_DATA10
B39	QSPI_DATA2	NAND_CE1_B		B40	LCD_DATA11	LCD_DATA11
B41	QSPI_DATA3	NAND_CLE		B42	LCD_DATA12	LCD_DATA12
B43	QSPI_SCLK	NAND_WP_B		B44	LCD_DATA13	LCD_DATA13
B45	GND	GND		B46	GND	GND
B47	GPIO5_IO5	SNVS_TAMPER5		B48	LCD_DATA14	LCD_DATA14
B49	GPIO5_IO8	SNVS_TAMPER8		B50	LCD_DATA15	LCD_DATA15
B51	GPIO5_IO7	SNVS_TAMPER7		B52	LCD_DATA16	LCD_DATA16
B53	GPIO5_IO9	SNVS_TAMPER9		B54	LCD_DATA17	LCD_DATA17
B55	GPIO5_IO4	SNVS_TAMPER4		B56	LCD_DATA18	LCD_DATA18
B57	ETH_MDIO	GPIO1_IO06		B58	LCD_DATA19	LCD_DATA19
B59	ETH_MDC	GPIO1_IO07		B60	LCD_DATA20	LCD_DATA20
B61	ETH_RDATA0	ENET1_RX_DATA0		B62	LCD_DATA21	LCD_DATA21
B63	ETH_RDATA1	ENET1_RX_DATA1		B64	LCD_DATA22	LCD_DATA22
B65	ETH_RX_EN	ENET1_RX_EN		B66	LCD_DATA23	LCD_DATA23
B67	ETH_RX_ER	ENET1_RX_ER		B68	GND	GND
B69	ETH_TX_EN	ENET1_TX_EN		B70	SPDIF_TX	JTAG_MOD
B71	ETH_TDATA0	ENET1_TX_DATA0		B72	GPIO5_IO0	SNVS_TAMPER0
B73	ETH_TDATA1	ENET1_TX_DATA1		B74	GPIO5_IO2	SNVS_TAMPER2
B75	GND	GND		B77	GND	GND
B77	ETH_TX_CLK	ENET1_TX_CLK		B78	VDD_COIN_3V	PMIC LICELL
B79	GND	GND		B80	GND	GND

Table 11 SOM Connector B pinout

3.7 Mechanical Specification

3.7.1 Dimension

Parameter	Typical	Unit
Dimension (L x W x H)	40.0 ±0.2 x 40.0 ±0.2 x 5.5	mm

Table 12 Module dimensions

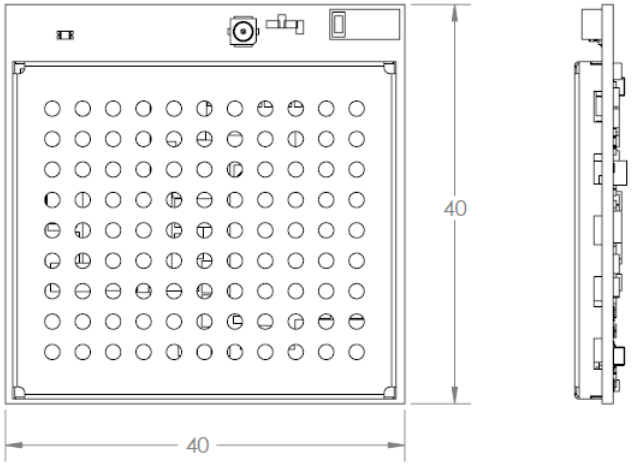


Figure 11 Module top and side view (dimension unit: mm)

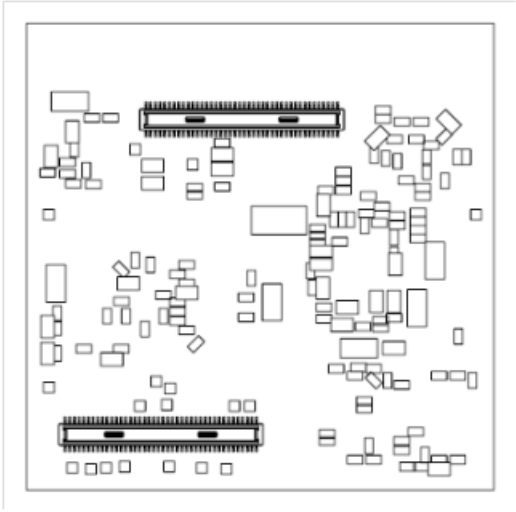


Figure 12 Module bottom view

3.7.2 Example host board footprint

The example below shows the host board landing pattern with 2.0mm receptacles. A compatible receptacle is the Hirose DF40C-80DS-0.4V(51) with height of 2.0mm or more [9].

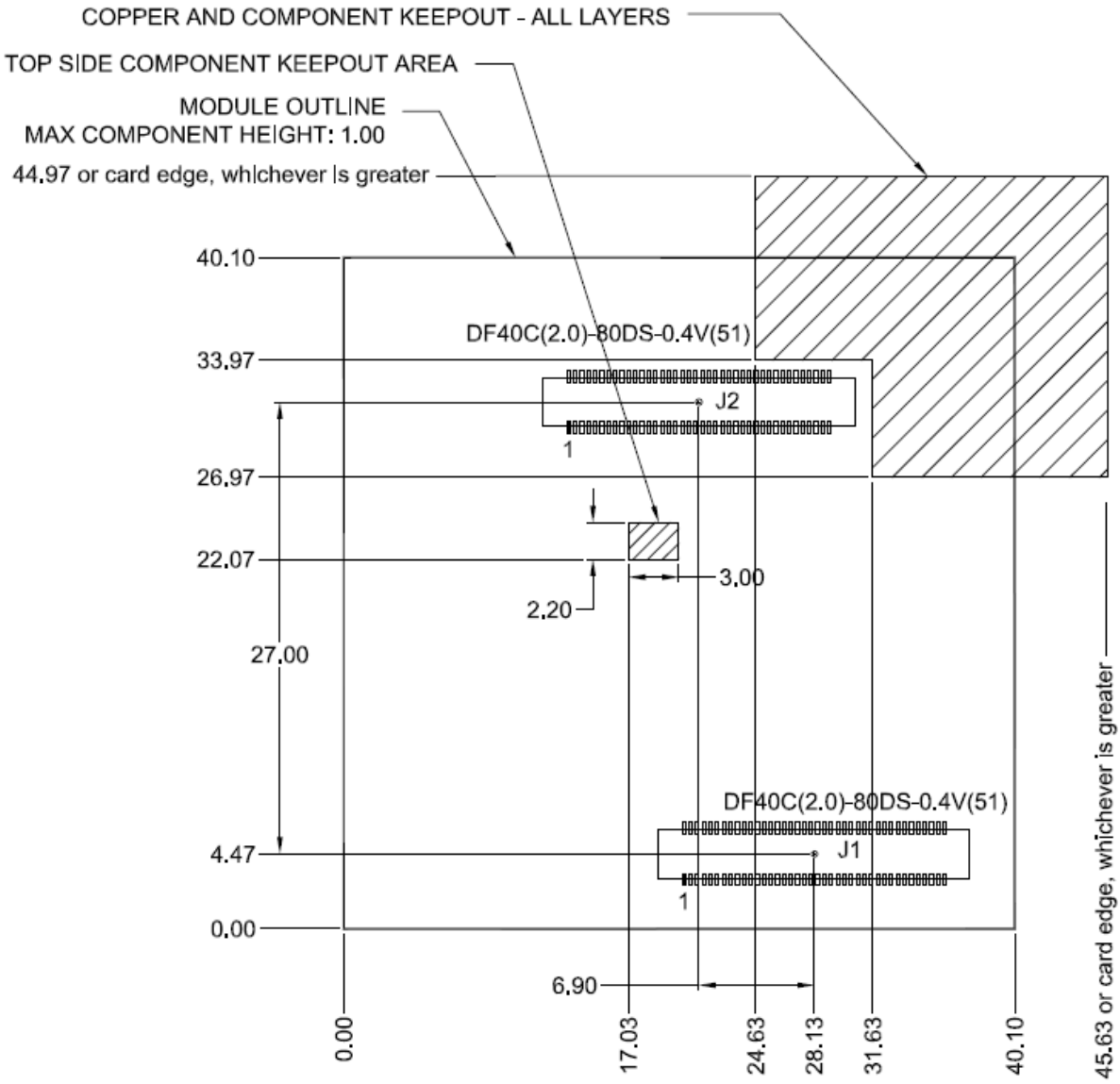


Figure 13 Example host PCB footprint (top view)

4. Technical Support Contact

Contact Wireless module application support at modules@murata.com

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