Keep track of a sample-hold from mode to mode to locate error sources

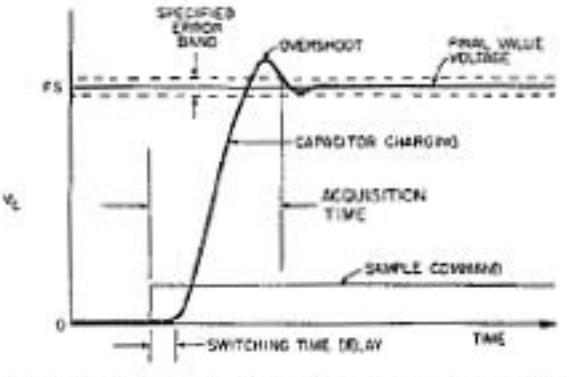
Part 2 of 3

A complicated process begins when a sample-hold takes a sample. The complications increase when it switches into the hold mode. To this bumper crop of complications, add the actual sample-to-hold transition itself, which, as a complex and important event, must not be overlooked. Understanding the intricate workings of this process is the basis for understanding the sources of error in the system and how to minimize them.

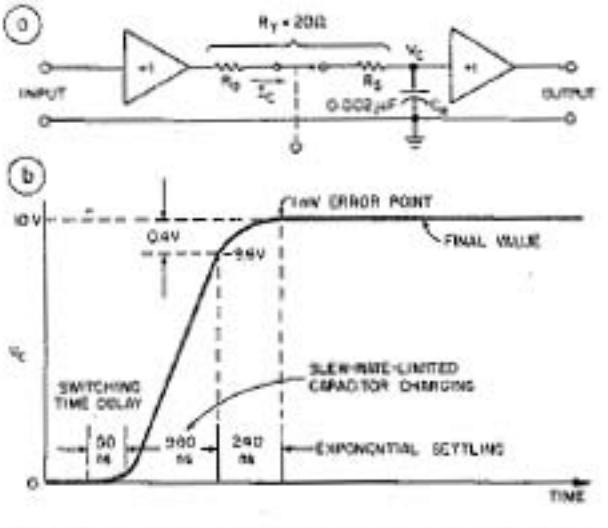
In the sample mode, the sampling switch closes and the circuit charges the hold capacitor to the input voltage. With the capacitor charged, the circuit tracks the input signal as it changes. However, tracking is possible only if the signal doesn't exceed the bandwidth or slew rate limit of the sample-hold. The term "sample mode" applies regardless of how long tracking continues.

The operating parameters that apply to the sample-hold in the sampling mode are specified in the same way as an operational amplifier's. Offset voltage, expressed in millivolts, may be referred to either the input or output, and is usually adjustable to zero with an external potentiometer. Dc gain, the ratio of output to input voltage at dc, is commonly either +1 or −1. With some sample-holds, adding external feedback resistors provides other gains, and some allow trimming external gain to precisely +1 or −1.

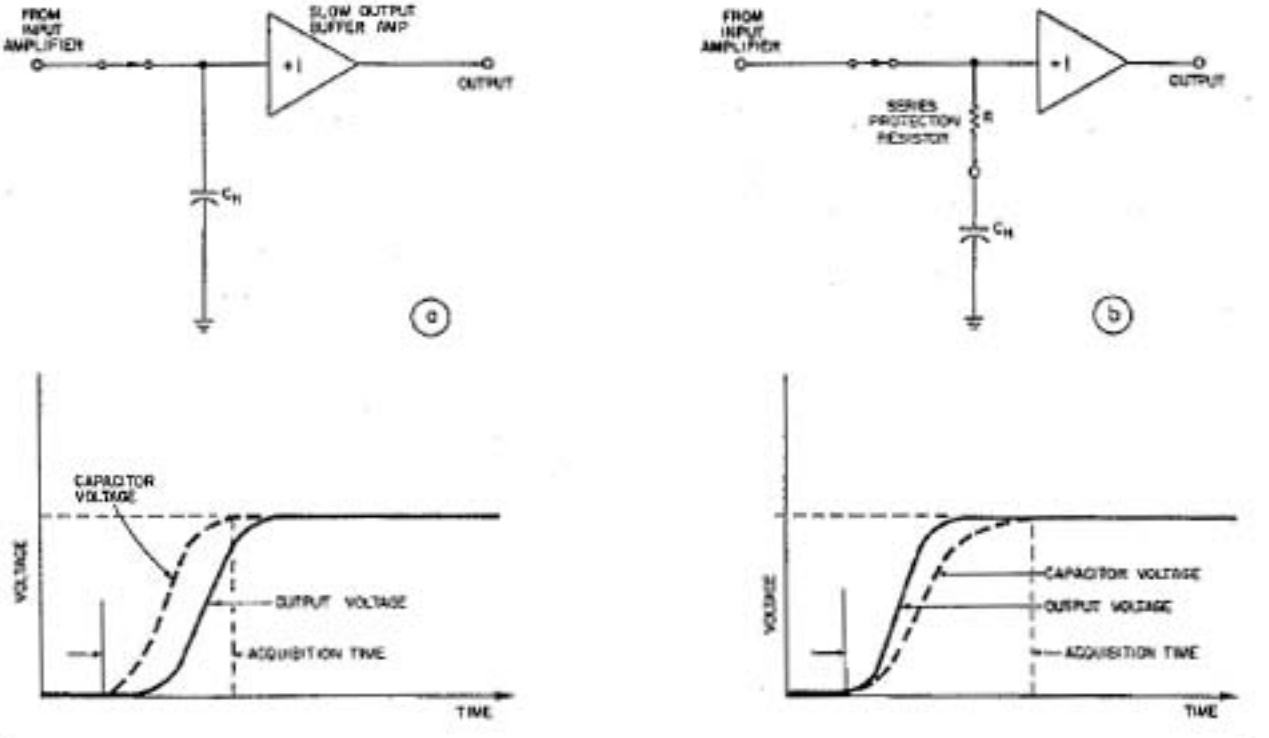
Bandwidth, the sinusoidal frequency at which gain is down by 3 dB from its dc value, is measured with a small-signal sine wave below the slew rate limit. The slew rate is the fastest rate at which the sample-



1. **Acquisition time of a sample-hold** starts with the sample command and ends when the voltage on the hold capacitor enters and stays in the error band. Acquisition time is defined for a full-scale voltage change, measured at the hold capacitor.



2. **This equivalent circuit for determining acquisition time** (a) shows the importance of the charging time constant, $R_T C_H$. Acquisition time is the sum of the various delays incurred in charging the hold capacitor to its final value (b), and is dominated by slew-limited charging.



3. **Acquisition time** may be less than or greater than the time it takes the output voltage to settle to its final value. In (a), the capacitor reaches its final value before the output amplifier catches up. In (b), the protective resistor permits the output to settle before the capacitor reaches its final voltage.

hold output can change. Specified in volts per microsecond, slew rate is generally determined by the charging rate of the hold capacitor.

Acquisition time counts

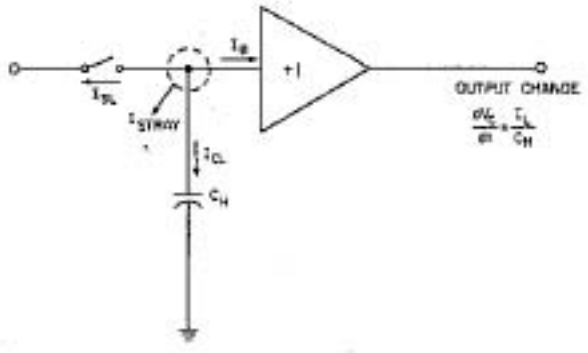
The most important specification of the sample-hold in the sample mode is acquisition time—the time required, after the sample command is given, for the hold capacitor to charge to a full-scale voltage change and remain within a specified error band about its final value.

As illustrated in Fig. 1, the definition applies to the capacitor voltage, not the output voltage of the circuit. The reason for this will become clear shortly. The figure shows an initial switching delay following the sample command. After this delay, the hold capacitor charges at a maximum rate which is determined by its charging current.

Initially, as the capacitor voltage attempts to enter the final value error band, it slightly overshoots the band, but then enters and remains within it. The amount of overshoot, generated by a wideband input amplifier driving a capacitive load, depends on this amplifier's stability. Acquisition time is therefore measured from the beginning of the sample command transition to the point where the signal enters the error band and stays there.

Another useful definition of acquisition time is the amount of time following the sample command transition that the hold command can be given so that the hold capacitor retains the voltage change to the required accuracy. The full-scale voltage change is usually specified as a 10-V change, although other magnitudes may be specifically stated. The error band is commonly specified from 0.2% down to 0.005%, with other values possible. Within this range there are sample-holds available that provide acquisition times from about 10 μs down to 20 ns. Basically, acquisition time determines the maximum sampling rate at which a sample-hold can be operated.

Several circuit limitations determine the achievable acquisition time for a sample-hold: the speed of the input amplifier with a capacitive load, the current available to drive the hold capacitor, the source resistance driving the hold capacitor (both amplifier output and switch), and the value of the hold capacitor. Either the input amplifier or the switch may limit



4. **Hold-mode droop is caused by currents** that charge or discharge the hold capacitor. These include switch-leakage, stray-leakage, amplifier-bias currents and leakage within the hold capacitor itself.

the current available to drive the hold capacitor.

Fig. 2 shows the relationship between the acquisition time, the current available to charge the capacitor, and the time constant associated with the hold capacitor. For example, to determine the acquisition time for a 10-V change to within 1 mV, or a 0.01% error band, assume a maximum charging current from the amplifier and switch of 20 mA and a capacitor value of 0.002 μF. The rate of change of capacitor voltage dV_C/dt is

$$\frac{I_C}{C_H} = \frac{20 \times 10^{-3}}{2 \times 10^{-9}} = 10^7 = 10\ V/\mu s, \qquad (1)$$

where I_C is the charging current and C_H is the capacitance of the hold capacitor. After a 50-ns switching delay, the capacitor begins to charge at a constant rate of 10 V/μs until it approaches final value and maximum charging current is no longer required. This happens when

$$V_C = 10 - (I_C R_T) = 9.6\ V. \qquad (2)$$

R_T, the total resistance in the hold capacitor's charging path, is also the sum of the amplifier output resistance (R_O) and the switch series resistance (R_S).

The capacitor charges exponentially over the final 400 mV with a time constant of

$$T = R_T C_H = 20 \times 2 \times 10^{-9} = 40\ ns. \qquad (3)$$

Since the final value error band is specified as 1 mV, it takes six time constants to reduce the 400 mV error to 1 mV, or 0.25%. Six time constants give a 240-ns exponential settling time. The acquisition time is then the sum of the three times that are indicated in Fig. 2b, or 0.05 + 0.96 + 0.24 = 1.25 μs.

This illustrates a fast sample-hold that acquires to 0.01% accuracy and shows as well that the charging current to the capacitor must be high and the hold capacitor time constant must be low. The same acquisition time limitations apply to the other sample-hold circuits shown in Part 1 of this series, which is why a current booster amplifier is required in one case.

Direct measurement of a sample-hold's acquisition time is not always possible since in some cases the capacitor voltage is not accessible externally. If a sample-hold has an operational integrator output stage, acquisition time can be measured, but in other circuits it may not be possible because the capacitor is inside the circuit.

The two interesting cases in Fig. 3 illustrate why the acquisition time is defined in terms of the hold capacitor. In Fig. 3a, the output buffer has a slower response time than the input amplifier and capacitor. This lag means that when the capacitor acquires a new voltage, its final value is reached before the output of the sample-hold. The switch can be opened when the capacitor voltage has entered the specified error band even though the output voltage has not. Slightly afterward, the output amplifier settles to the correct output voltage.

Fig. 3b shows the output stage of one of the popular monolithic sample-hold circuits that has a resistor in series with the hold capacitor. This resistor provides short circuit protection to the capacitor terminal. The resistor, however, causes a lag in the capacitor voltage, which means that the capacitor is not fully charged when the sample-hold output voltage has reached final value. To allow the capacitor to charge completely, the sampling switch in this circuit must remain closed longer than indicated by the output voltage. The acquisition time in this case must be measured by starting with a long sample time and then gradually reducing this time until the output starts to show an error. These cases underscore the fact that acquisition time is properly defined at the capacitor rather than at the sample-hold's output.

Then there's hold mode

The second mode of operation for a sample-hold, when the sampling switch is open, is the hold mode. Two important specifications that characterize hold mode are hold mode droop, or voltage decay, and hold-mode feedthrough.

Hold-mode droop, defined as the output voltage change per unit of time while in the hold mode, is commonly specified in volts per second, microvolts per microsecond, or other convenient quantities. Hold-mode droop originates as leakage from the hold capacitor (see Fig. 4). The four leakage components consist of capacitor insulation leakage I_{CL}, switch leakage current I_{SL}, output amplifier bias current I_B and stray leakage I_{STRAY} from the common terminal connection. The rate of voltage change on the capacitor dV/dt is the ratio of the total leakage current, I_L, to hold capacitance C_H

$$\frac{dV_C}{dt} = \frac{I_L}{C_H} \qquad (4)$$

If all the leakage currents don't have the same

Terminology

Acquisition time: How long it takes after the sample command is given, for the hold capacitor to be charged to a full-scale voltage change and to remain within a specified error band around its final value.

Aperture delay time: The time elapsed from the hold command to the opening of the switch.

Aperture jitter: Also called "aperture uncertainty time," it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture time: The averaging time of a sample-hold during the sample-to-hold transition.

Bandwidth: The frequency at which the gain is down 3 dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Effective aperture delay: The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure of merit: The ratio of the available charging current during sample mode to the leakage current during hold mode.

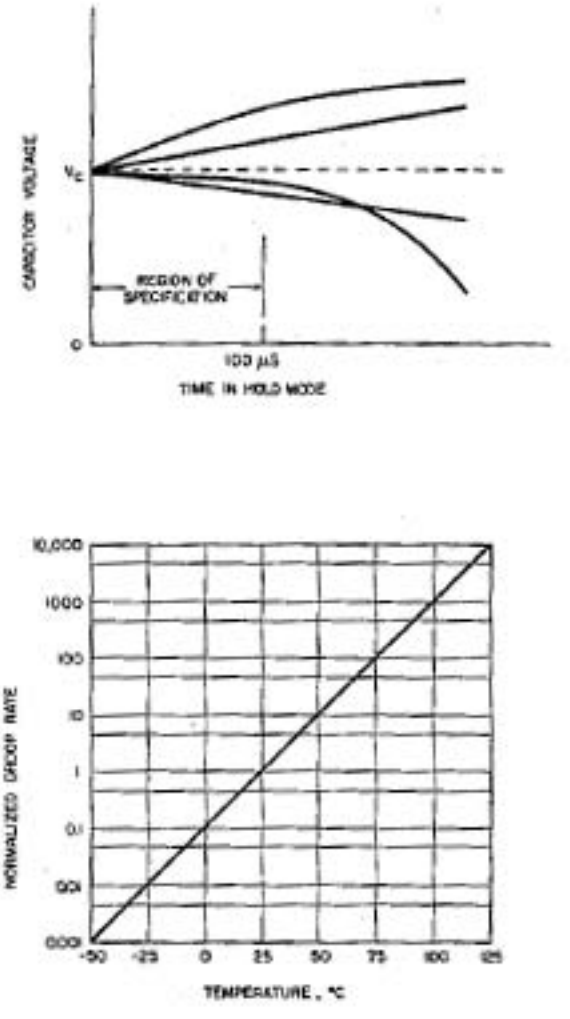
Hold-mode droop: The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold-mode feedthrough: The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold-mode settling time: The time from the hold-command transition until the output of the sample-hold has settled within the specified error band. It includes aperture delay time.

Sample-to-hold offset error: The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor from the switch as it opens.

Slew rate: The fastest rate at which the sample-hold output can change. It's specified in V/μs.



5. **Droop in hold mode** can be positive or negative-going, and may not be linear with time (a). Since most leakage current comes from silicon devices, droop as a function of temperature is predictable (b).

polarity, the result is a somewhat lower droop rate.

To measure hold-mode droop, simply acquire a given voltage and then while watching the output voltage on an oscilloscope, switch into the hold mode. The droop may be positive or negative and is not necessarily linear with time (See Fig. 5a). Several possible droop rates are illustrated. The value measured, which appears on data sheets, is the slope right after initiation of the hold mode when the output voltage feeds an a/d converter or other circuit.

In addition, hold-mode droop changes exponentially with temperature. Most of the leakage that causes this droop comes from silicon devices. Since a device's leakage approximately doubles for every 10 C increase in temperature, hold-mode droop shares this characteristic. Fig. 5b shows a normalized plot of hold-mode droop vs. temperature for virtually any sample-hold. Droop rate is specified on a data sheet at 25 C. To consider an example, a sample-hold with a droop rate of 100 μV/ms at 25 C will have a rate of 3.2 mV/ms at 75 C and a rate of 102 mV/ms at 125 C.

For a given operating temperature, droop rate must be determined based on the required hold time in order to know the resulting error. Of course, below 25 C, droop rate improves by a factor of two for every 10 C. In cases where better droop rate is required, an extra hold capacitor must be added or a better sample-hold selected. Additional capacitance also increases the acquisition time of the circuit.

In the case of monolithic sample-holds, the hold-mode leakage is specified on the data sheet so that the required capacitor value can be figured from the

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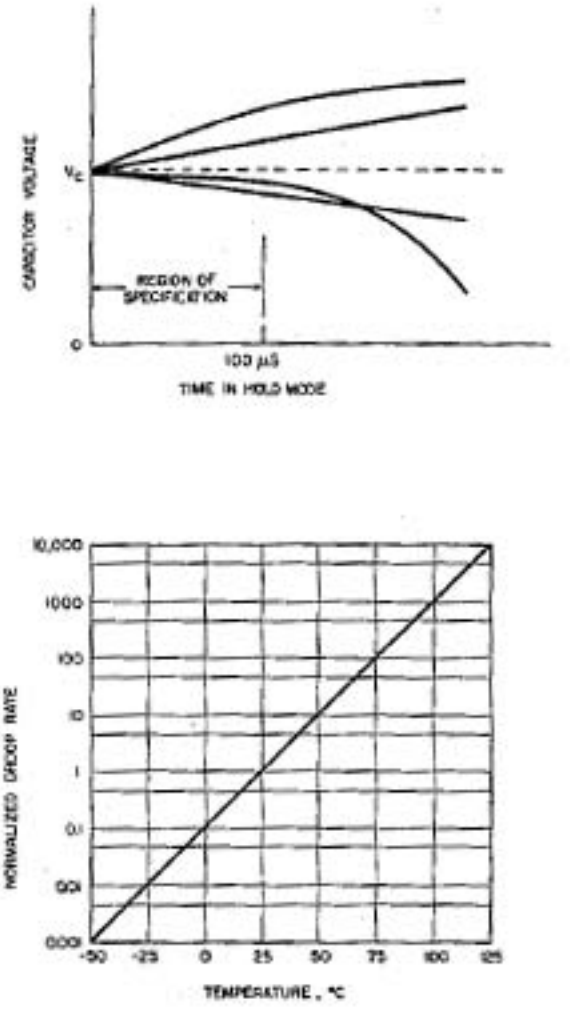

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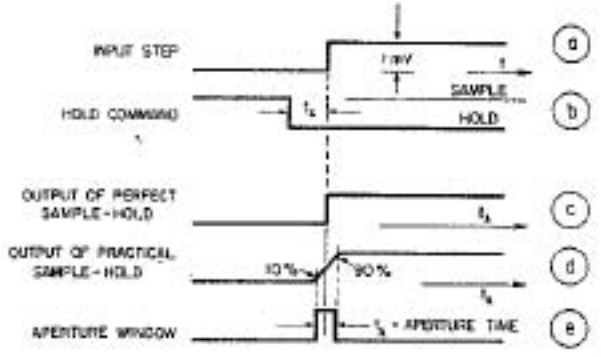
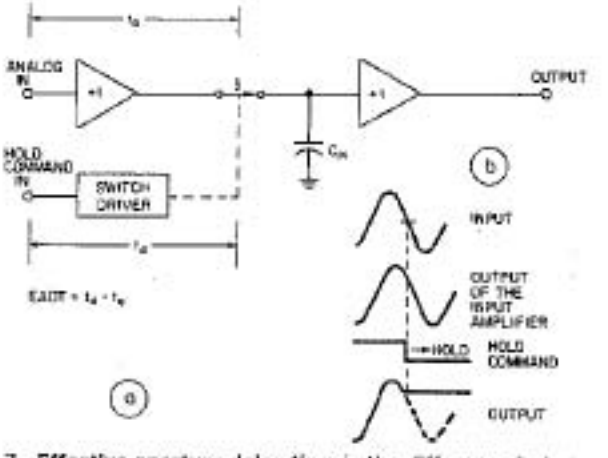


6. **Aperture time can be measured** by repeatedly feeding a tiny step (a) to the sample-hold's input and repeatedly shifting from sample to hold (b) with a varying delay, t_a. A perfect sample-hold would have an output like (c) as a function of delay time t_a, but a real sample-hold averages this step over t_A.



7. **Effective aperture delay time** is the difference between the input amplifier time delay, t_a, and the delay between the hold command and the time when the switch opens (t_d). EADT may be positive, zero, or negative. If t_a is greater than t_d, the hold capacitor sees a delayed version of the input (b), which results in holding an input voltage that occurred before the hold command.

relationships in equation 4.

Since the hold capacitor directly affects both speed and accuracy of a sample-hold, it's useful to have a figure of merit for sample-holds. Increasing the hold capacitance decreases the droop rate, but increases acquisition time. Likewise, decreasing the capacitance increases the droop rate although it does decrease the acquisition time.

The figure of merit is a ratio that measures the improvement in both acquisition time and droop rate together. It is a dimensionless quantity and may have values of 10^6 or more for a high quality sample-hold.

A useful figure of merit sometimes used with sample-holds is the ratio of the current available to charge the capacitor (I_C) to the leakage current from the capacitor (I_L). This ratio is approximately equal to the ratio of slew rate to droop rate:

$$\text{Figure of Merit} = \frac{I_C}{I_L} \approx \frac{\text{Slew Rate}}{\text{Droop Rate}} \qquad (5)$$

A source of error in the hold mode, hold-mode feedthrough, or simply feedthrough, is the second specification that characterizes hold mode. This parameter is the percentage of an input sinusoidal signal that's measured at the output of a sample-hold in the hold mode.

To measure feedthrough, apply a 20-V peak-to-peak sinusoid to the input of a sample-hold while it is in the hold mode. A greatly attenuated version of the input shows up at the output, passing through switch capacitance and stray coupling capacitance. The resulting feedthrough can be measured easily with an oscilloscope. Typical values of feedthrough for a well-designed sample-hold are from 0.05% down to 0.005% of the input. Feedthrough is sometimes expressed in dB of attenuation.

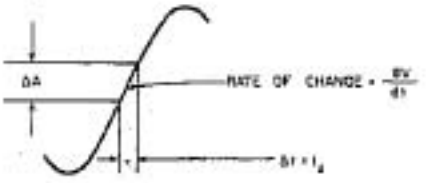
Hold-mode feedthrough may vary with frequency, either increasing or decreasing at higher frequencies depending on the particular design of the sample-hold. Feedthrough is a most important specification when a sample-hold follows an analog multiplexer that switches between many different channels. Note that feedthrough can also be measured with a square-wave input rather than a sinusoid, since the square wave contains many harmonic frequencies.

A critical parameter

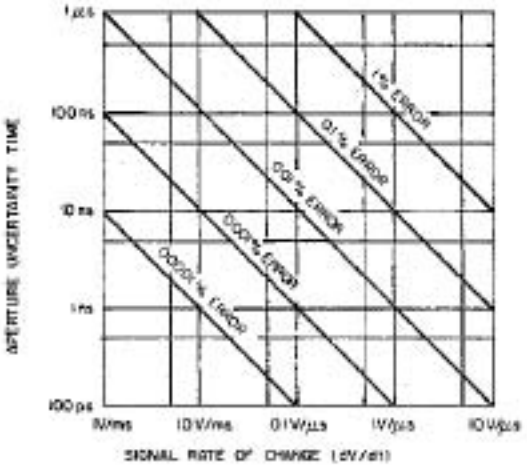
The most critical part of sample-hold operation is during the short sample-to-hold transition when the sampling switch opens. It's during this transition period that the real subtleties of sample-hold operation appear, including one of the most important parameters associated with this period, called aperture time.

Aperture time is the most misunderstood of all sample-hold specifications. There are actually several related parameters which use the word aperture as part of the specification.

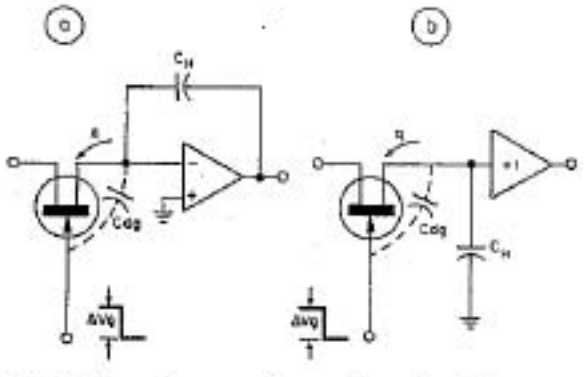
The concept of aperture time in electronics relates closely to the root meaning of aperture: an opening, or hole. In electronic measurements aperture is the "opening" or "window" of time during which a signal is averaged or measured. For example, in an a/d converter, the conversion time is the time required to measure the input signal and is also known as the aperture time of the converter. In fact, a sample-hold is the device that reduces the aperture time of an a/d converter by replacing the converter's time window with the sample-hold's much shorter window.



8. **Timing uncertainty in the switch** and driver circuit produces uncertainty in the held voltage, which for a given period of time, increases with the rate of change of the signal voltage.



9. **To obtain the error due to aperture uncertainty time** for a given signal rate of change, a full-log plot is helpful. This plot assumes a 10-V full-scale signal.



10. **Drain-to-gate capacitance,** C_{dg}, transfers some charge, q, when a FET sampling switch opens. The resulting voltage step on the hold capacitor, C_H, is small if C_H is large. The switch in the first circuit (a) operates at virtual ground.

Ideally, a sample-hold takes a point sample of the input signal, that is, an accurate sample in zero time. Since this is impossible, the sample is actually taken in the short period of time when the switch opens, during which the signal is averaged. The aperture time therefore occurs after the signal has been acquired, when the switch rapidly opens.

Aperture time is frequently, but mistakenly, defined as the turn-off time of the switch. If this were true, aperture times would be extremely small since the switch opens very quickly. The confusion stems from the fact that the switch follows a band-limited input amplifier which, even if the switch opening were instantaneous, averages the result over a small period of time.

To interpret aperture time, as in Fig. 6, assume the sample-hold receives a 1-mV input step (Fig. 6a). The hold command transition (Fig. 6b) can be adjusted to occur before, with or after the input step. The timing difference between the two, designated t_x, can be positive, zero, or negative. (For simplicity, assume no delay between the hold command and the opening of the sampling switch.) To make the measurement, feed the sample-hold with repeated input steps and hold commands while slowly varying t_x. As the hold command transition effectively scans across the input step, the sample-hold's output in hold mode changes. Ideally, when hold-mode output is plotted against t_x, it should look like Fig. 6c. Such an output, a perfect sample with no averaging, requires an infinite-bandwidth input amplifier in addition to an infinitely-fast switch.

Since this is not possible, the input step is averaged, or filtered, by both the switch with a non-zero opening time, and by the input amplifier, which has limited bandwidth. The actual waveform therefore looks like Fig. 6d. The filtering action of the switch and input amplifier slows the rise-time of the step to t_A, which is the aperture time or aperture window of the sample-hold as shown in Fig. 6e. Mathematically convolving the input step (Fig. 6a) with the aperture window (Fig. 6e) gives the actual output (Fig. 6d).

In practice, because of amplifier and switch speed limitations, it is extremely difficult to achieve true aperture times less than a few nanoseconds.

Delayed window

Aperture delay time, another frequently used term concerning the sample-to-hold transition, is generally defined as the elapsed time between the hold command and the opening of the switch. Aperture delay time, a pure time delay, can be compensated out by advancing or delaying the hold command. Furthermore, this specification is difficult to measure, if not impossible, since the precise time when the switch turns off cannot be determined directly.

A more useful specification might be called effective aperture delay, and defined as the time difference between the hold command and the time at which the

input signal and the held voltage were equal. In other words, effective aperture delay relates the hold command to the point on the input signal which was held (see Fig. 7).

Effective aperture delay really points out the difference between the two delay times shown in Fig. 7. The first is the analog delay through the input amplifier, while the second is the digital delay to the switch opening (Fig. 7a). Effective aperture delay (EAD) is then equal to $(t_s - t_a)$.

Notice that either a positive, negative, or zero value may be obtained depending on which delay is larger. Fig. 7b illustrates negative effective aperture delay. In this instance, time lag in the input amplifier has resulted in holding an input voltage which occurred before the hold command. Knowing effective aperture delay time then is more useful than knowing aperture delay time.

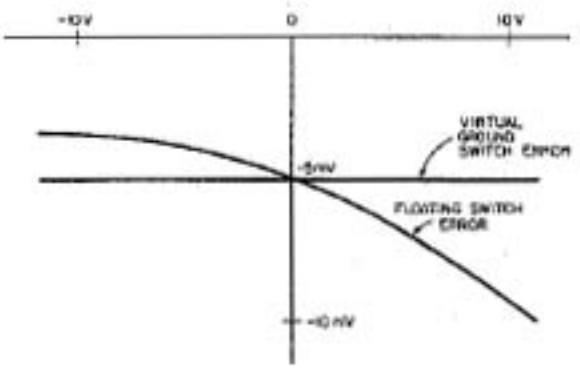
A related specification, aperture uncertainty time, or aperture jitter, is the uncertainty in the time at which the switch opens. Actually, it's the time variation in aperture delay time. If the sampling switch receives the hold command for a series of samples at the same point on a waveform, it will hold slightly different values each time.

Aperture uncertainty time originates in the digital driver circuit and switch. The hold command has a finite risetime and must pass through one or more logic thresholds that have voltage noise. These transitions therefore generate time uncertainties. The significance of aperture uncertainty time is that it causes an amplitude uncertainty in the held output of the sample-hold. This amplitude error, ΔA, shown in Fig. 8, equals the product of the rate of change of the input signal dV/dt, and the aperture uncertainty t_u.

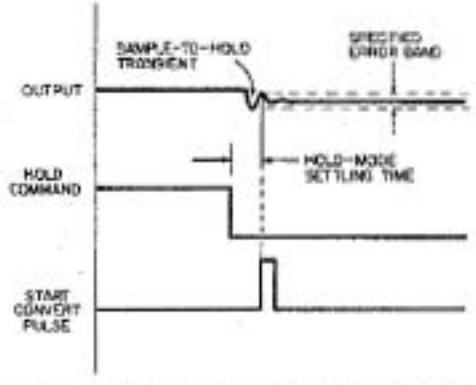
This product is the basis of a graph (Fig. 9) that gives aperture uncertainty vs. signal rate of change for various accuracies. The accuracy is based on 10-volt full scale signals. The surprising fact is that moderate speed signals produce relatively large errors even with small aperture uncertainties. For example, if the aperture uncertainty is 10 ns and the input signal rate of change is 1V/μs, the amplitude error is 0.1% for 10 V full scale. Reducing this error to 0.01% means that the aperture uncertainty time has to be reduced to just 1 ns.

Aperture uncertainty time is generally quite small in well-designed sample-holds since it's possible to achieve values of a few nanoseconds down to tens of picoseconds. As a rough rule of thumb, the aperture uncertainty tends to be 10% or less of the aperture delay time; in some designs it can be as low as 0.1%.

Sample-to-hold offset error develops when the switch opens, as a direct result of a phenomenon called charge dumping or charge transfer.



11. **Sample-to-hold offset error varies** with input signal voltage if the sampling switch floats with the signal, but is unaffected by variations in signal voltage if the switch operates at virtual ground.



12. **When an a/d converter follows a sample-hold,** the start-conversion pulse must be delayed until the output of the sample-hold has had enough time to settle within the error band and stay there.

There are two types of sample-hold switches; one operates at virtual ground (Fig. 10a), while the other operates at the signal voltage (Fig. 10b). Every electronic switch has a capacitance associated with it. In this case it is C_{dg}, the drain-to-gate capacitance of the junction FET switches shown. This capacitance couples the switch-control voltage on the gate to the hold capacitor.

Since the switch-control voltage must generally be rather large, a significant charge transfers from the hold capacitor to the gate-drive circuit when the switch is turned off. This charge is

$$q = C_{dg}\,\Delta V_g \qquad (6)$$

where ΔV_g is the change in gate voltage. The error this produces on the hold capacitor is then

$$V_e = \frac{q}{C_H} = \frac{C_{dg}}{C_H}\,\Delta V_g. \qquad (7)$$

This error typically might be 10 mV assuming 2 pF for C_{dg}, a 10-V ΔV_g, and a 0.002 μF hold capacitor.

Sample-to-hold offset error is one of the un-

desirable, inherent characteristics of sample-hold circuits. It should be looked for and recognized. The charge transfer that causes this error is expressed in picocoulombs and in practical circuits it may vary from 50 pC down to 0.1 pC. Since monolithic sample-hold circuits require external hold capacitors, their voltage error must be determined by equation 7. Sample-holds with internal capacitors have a specified sample-to-hold offset voltage. This offset, of course, can be decreased by adding an external capacitor to increase the total hold capacitance.

Note that the two switch configurations in Fig. 10 have somewhat different charge transfer characteristics. In the virtual ground switch the charge transfer is constant regardless of the signal voltage, since the gate voltage change is always the same. In the other switch, however, the gate voltage change varies with the signal voltage. This causes the charge transfer to vary with signal level. Furthermore, the drain-to-gate capacitance also varies with the signal voltage, so that the charge transfer itself is nonlinear and even has a "gain error."

Some have curved errors

The output error caused by charge transfer differs for the two types of switches (Fig. 11). The virtual ground switch produces a constant offset error vs. signal voltage, while the floating switch produces a nonlinear error vs. signal voltage. Charge transfer is obviously a limiting factor in a high-accuracy, high-speed sample-hold. It works against attaining both these characteristics simultaneously. Some sample-holds have unique switch designs that minimize or compensate for this charge transfer. In some of them, an externally-adjustable compensation circuit minimizes the charge transfer. If the sample-to-hold offset error is constant with signal voltage, then the error is relatively easy to handle since it can be zeroed with a simple offset adjustment.

Another effect of the sample-to-hold transition is a small transient in the output just after going into the hold mode—the hold mode settling time (Fig. 12b). This is the time it takes the output of the sample-hold to settle within the specified error band after the hold command transition. Notice that the hold mode settling time includes aperture delay time. Fig. 12 shows the small output transient caused by the rapid switch turn-off at the input to the buffer amplifier.

This transient occurs after the output settles to a new value that includes the sample-to-hold offset. Hold mode settling time may be a few nanoseconds to a microsecond or so, depending on the particular sample-hold. It is an important specification because an a/d conversion that follows sampling and holding cannot begin until hold-mode settling is complete without causing a conversion error. As Fig. 12 shows, the pulse that starts the converter is generated after the sample-hold output has settled within the specified error band.■■