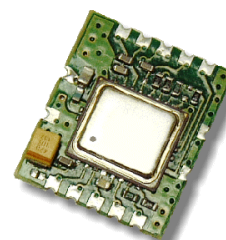


DR5103

303.825 MHz Receiver Module



- **Designed for Short-Range Wireless Data Communications**
- **Supports up to 19.2 kbps Encoded Data Transmissions**
- **3 V, Low Current Operation plus Sleep Mode**
- **Ready to Use OEM Module**

The DR5103 receiver module is ideal for short-range wireless data applications where robust operation, small size and low power consumption are required. The DR5103 utilizes Murata's RX5003 amplifier-sequenced hybrid (ASH) architecture to achieve this unique blend of characteristics. The receiver RX5003 is sensitive and stable. A wide dynamic range log detector provides robust performance in the presence of on-channel interference or noise. Two stages of SAW filtering provide excellent receiver out-of-band rejection. The DR5103 includes the RX5003 plus all configuration components in a ready-to-use PCB assembly excellent for prototyping and intermediate volume production runs.

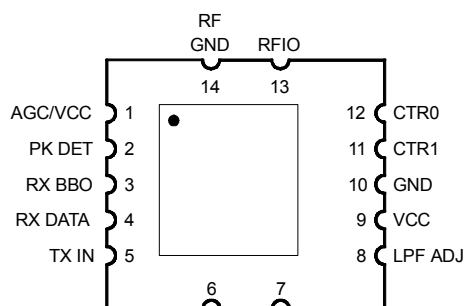
Absolute Maximum Ratings

Rating	Value	Units
Power Supply and All Input/Output Pins	-0.3 to +4.0	V
Non-Operating Case Temperature	-50 to +100	°C
Soldering Temperature (10 seconds)	230	°C

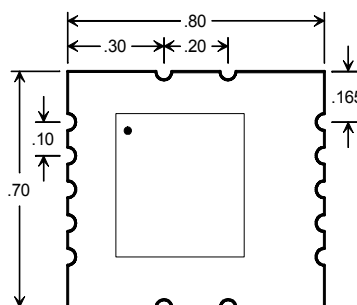
Electrical Characteristics, 2.4 kbps On-Off Keyed

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency	fO		303.625		304.025	MHz
Modulation Type			OOK			
Data Rate				2.4	19.2	kbps
Receiver Performance (OOK @ 2.4 kbps)						
Input Current, 3 Vdc Supply	I _R				1.8	mA
Input Signal for 10 ⁻⁴ BER, 25 °C				-100		dBm
Rejection, ±30 MHz	R _{REJ}		55			dB
Sleep to Receive Switch Time(100 ms sleep, -85 dBm signal)	t _{SR}	3		200		μs
Sleep Mode Current	I _S				5	μA
Power Supply Voltage Range	VCC		2.7		3.5	Vdc
Operating Ambient Temperature	T _A		-20		+65	°C

DR5103 Pin Out



DR5103 Outline Drawing



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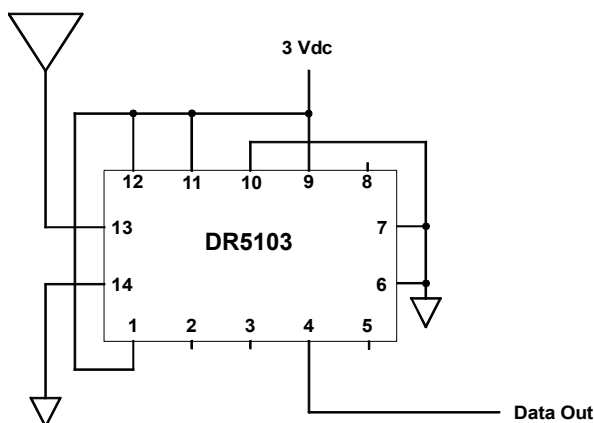
Pin Descriptions

Pin	Name	Description
1	AGC/VCC	<p>This pin is connected directly to the receiver AGCCAP pin. To disable AGC operation, this pin is tied to VCC. To enable AGC operation, a capacitor is placed between this pin and ground. This pin controls the AGC reset operation. A capacitor between this pin and ground sets the minimum time the AGC will hold-in once it is engaged. The hold-in time is set to avoid AGC chattering. For a given hold-in time t_{AGH}, the capacitor value C_{AGC} is:</p> $C_{AGC} = 19.1 \cdot t_{AGH}, \text{ where } t_{AGH} \text{ is in } \mu\text{s and } C_{AGC} \text{ is in pF}$ <p>A $\pm 10\%$ ceramic capacitor should be used at this pin. The value of C_{AGC} given above provides a hold-in time between t_{AGH} and $2.65 \cdot t_{AGH}$, depending on operating voltage, temperature, etc. The hold-in time is chosen to allow the AGC to ride through the longest run of zero bits that can occur in a received data stream. The AGC hold-in time can be greater than the peak detector decay time, as discussed below. However, the AGC hold-in time should not be set too long, or the receiver will be slow in returning to full sensitivity once the AGC is engaged by noise or interference. The use of AGC is optional when using OOK modulation with data pulses of at least 30 μs. Active or latched AGC operation is required for ASK modulation and/or for data pulses of less than 30 μs. The AGC can be latched ON once engaged by connecting a 150 K resistor between this pin and ground, instead of a capacitor. AGC operation depends on a functioning peak detector, as discussed below. The AGC capacitor is discharged in the receiver power-down (sleep) mode. Note that provisions are made on the circuit board to install a jumper between this pin and the junction of C2 and L3. Installing the jumper allows either this pin or Pin 9 to be used for the Vcc supply when AGC operation is not required.</p>
2	PK DET	<p>This pin is connected directly to the receiver PKDET pin. This pin controls the peak detector operation. A capacitor between this pin and ground sets the peak detector attack and decay times, which have a fixed 1:1000 ratio. For most applications, the attack time constant should be set to 6.4 ms with a 0.027 μF capacitor to ground. (This matches the peak detector decay time constant to the time constant of the 0.1 μF coupling capacitor C3.) A $\pm 10\%$ ceramic capacitor should be used at this pin. The peak detector is used to drive the "dB-below-peak" data slicer and the AGC release function. The AGC hold-in time can be extended beyond the peak detector decay time with the AGC capacitor, as discussed above. Where low data rates and OOK modulation are used, the "dB-below-peak" data slicer and the AGC are optional. In this case, the PKDET pin can be left unconnected, and the AGC pin can be connected to VCC to reduce the number of external components needed. The peak detector capacitor is discharged in the receiver power-down (sleep) mode. See the description of Pin 3 below for further information.</p>
3	RX BBO	<p>This pin is connected directly to the receiver BBOUT pin. On the circuit board, BBOUT also drives the receiver CMPIN pin through C3, a 0.1 μF coupling capacitor ($t_{BBC} = 6.4 \text{ ms}$). RX BBO can also be used to drive an external data recovery process (DSP, etc.). The nominal output impedance of this pin is 1 K. The RX BBO signal changes about 10 mV/dB, with a peak-to-peak signal level of up to 675 mV. The signal at RX BBO is riding on a 1.1 Vdc value that varies somewhat with supply voltage and temperature, so it should be coupled through a capacitor to an external load. A load impedance of 50 K to 500 K in parallel with no more than 10 pF is recommended. Note the AGC reset function is driven by the signal applied to CMPIN through C3. When the receiver is in power-down (sleep) the output impedance of this pin becomes very high, preserving the charge on the coupling capacitor(s). The value of C3 on the circuit board has been chosen to match typical data encoding schemes at 2.4 kbps. If C3 is modified to support higher data rates and/or different data encoding schemes and PK DET is being used, make the value of the peak detector capacitor about 1/3 the value of C3.</p>
4	RX DATA	<p>RX DATA is connected directly to the receiver data output pin, RXDATA. This pin will drive a 10 pF, 500 K parallel load. The peak current available from this pin increases with the receiver low-pass filter cutoff frequency. In the power-down (sleep) or receive mode, this pin becomes high impedance. If required, a 1000 K pull-up or pull-down resistor can be used to establish a definite logic state when this pin is high impedance (do not connect the pull-up resistor to a supply voltage higher than 3.5 Vdc or the receiver will be damaged). This pin must be buffered to successfully drive low-impedance loads.</p>
5	NC	
6, 7	GND	

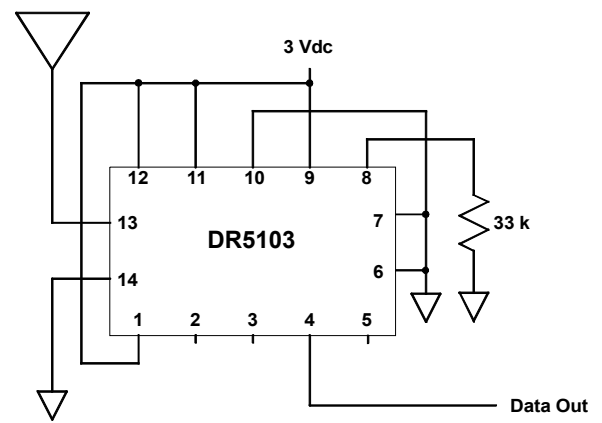
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8	LPF ADJ	<p>This pin is the receiver LPFADJ pin. R6 on the circuit board (330 K) is connected between LPFADJ and ground will be in parallel with any external resistor connected to LPF ADJ. The filter bandwidth is set by the parallel resistance of R6 and the external resistor (if used). The equivalent resistor value can range from 330 K to 820 ohms, providing a filter 3 dB bandwidth f_{LPF} from 4.4 kHz to 1.8 MHz. The 3 dB filter bandwidth is determined by:</p> $f_{LPF} = 1445 / (330 * R_{LPF} / (330 + R_{LPF})), \text{ where } R_{LPF} \text{ is in kilohms, and } f_{LPF} \text{ is in kHz}$ <p>A $\pm 5\%$ resistor should be used to set the filter bandwidth. This will provide a 3 dB filter bandwidth between f_{LPF} and $1.3 * f_{LPF}$ with variations in supply voltage, temperature, etc. The filter provides a three-pole, 0.05 degree equiripple phase response. The peak drive current available from RXDATA increases in proportion to the filter bandwidth setting. As shipped, the receiver module is set up for nominal 2.4 kbps operation. An external resistor can be added between Pin 8 and ground to support higher data rates. Preamble training times will not be decreased, however, unless C3 is replaced with a smaller capacitor value (see the descriptions of Pins 2 and 3 above). Refer to sections 1.4.3, 2.5.1 and 2.6.1 in the ASH Transceiver Designer's Guide for additional information on data rate adjustments.</p>
Pin	Name	Description
9	VCC	This is the positive supply voltage pin for the module. The operating voltage range is 2.7 to 3.5 Vdc. It is also possible to use Pin 1 as the Vcc input. Please refer to the Pin 1 description above.
10	GND	This is the supply voltage return pin.
11	CTR1	CTR1 is connected to the CNTRL1 control pin on the receiver. CTR1 and CTR0 select the transceiver operating modes. CTR1 and CTR0 both high place the unit in the receive mode. CTR1 and CTR0 both low place the unit in the power-down (sleep) mode. CTR1 is a high-impedance input (CMOS compatible). This pin must be held at a logic level; it cannot be left unconnected. At turn on, the voltage on this pin and CTR0 should rise with VCC until VCC reaches 2.7 Vdc (receive mode). Thereafter, any mode can be selected.
12	CTR0	CTR0 is connected to the CNTRL0 control pin on the receiver. CTR0 is used with CTR1 to control the operating modes of the receiver. CTR0 is a high-impedance input (CMOS compatible). This pin must be held at a logic level; it cannot be left unconnected. At turn on, the voltage on this pin and CTR1 should rise with VCC until VCC reaches 2.7 Vdc (receive mode). Thereafter, any mode can be selected.
13	RFIO	RFIO is the RF input/output pin. A matching circuit for a 50 ohm load (antenna) is implemented on the circuit board between this pin and the receiver SAW filter transducer.
14	RF GND	This pin is the RF ground (return) to be used in conjunction with the RFIO pin. For example, when connecting the transceiver module to an external antenna, the coaxial cable ground is connected this pin and the coaxial cable center conductor is connected to RFIO.

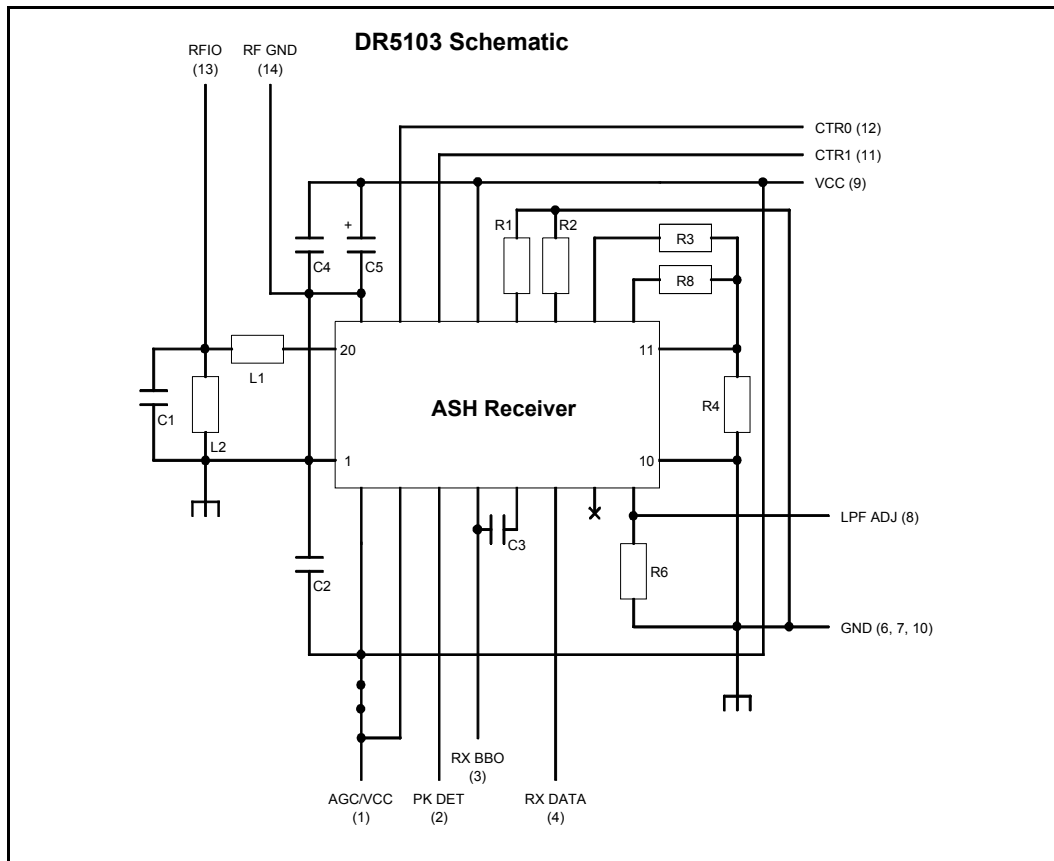
2.4 kbps Application Circuit



19.2 kbps Application Circuit



Discontinued



Note: Preliminary specifications, subject to change without notice.