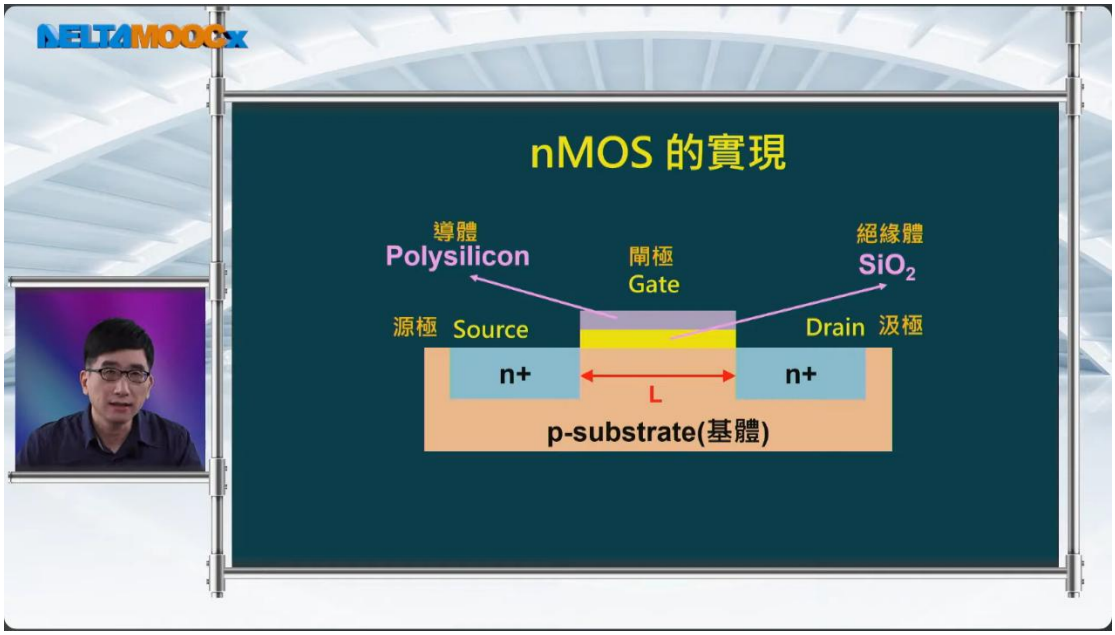
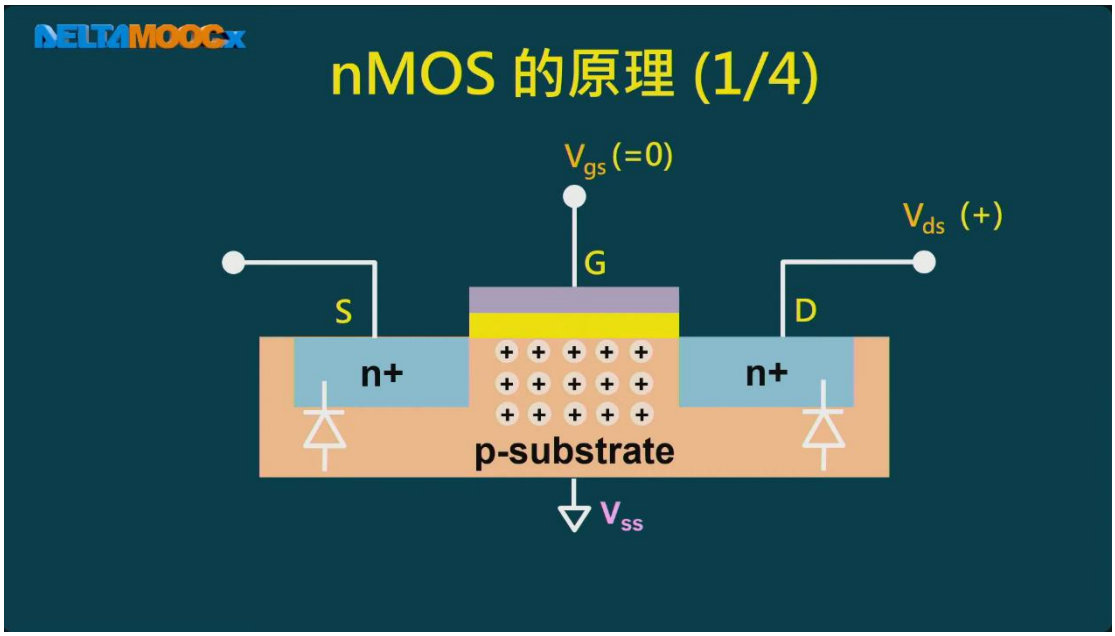
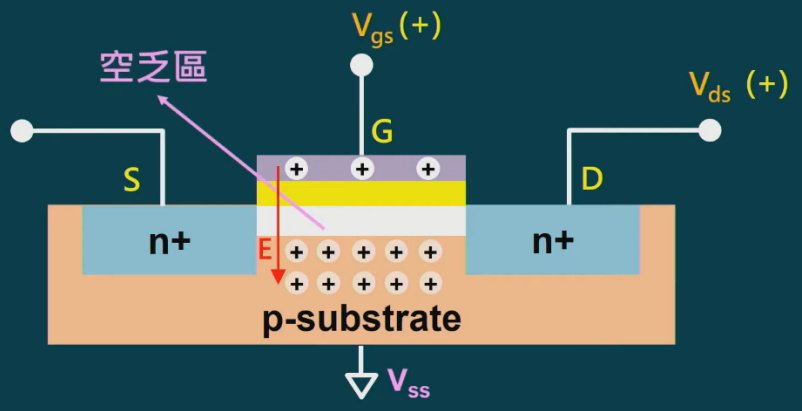
L 也就是我們常說的幾納米

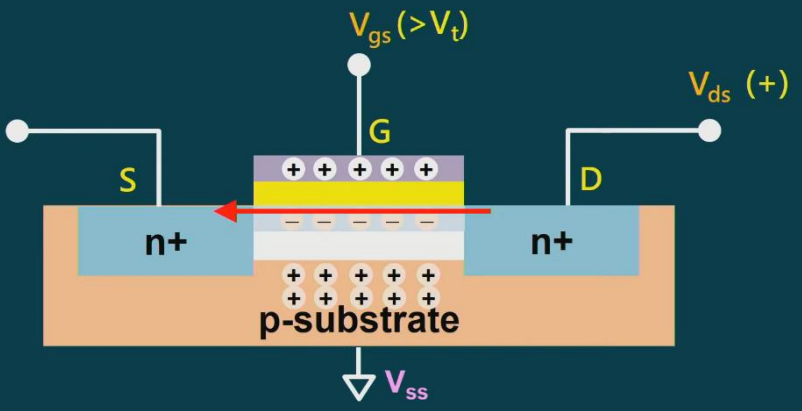




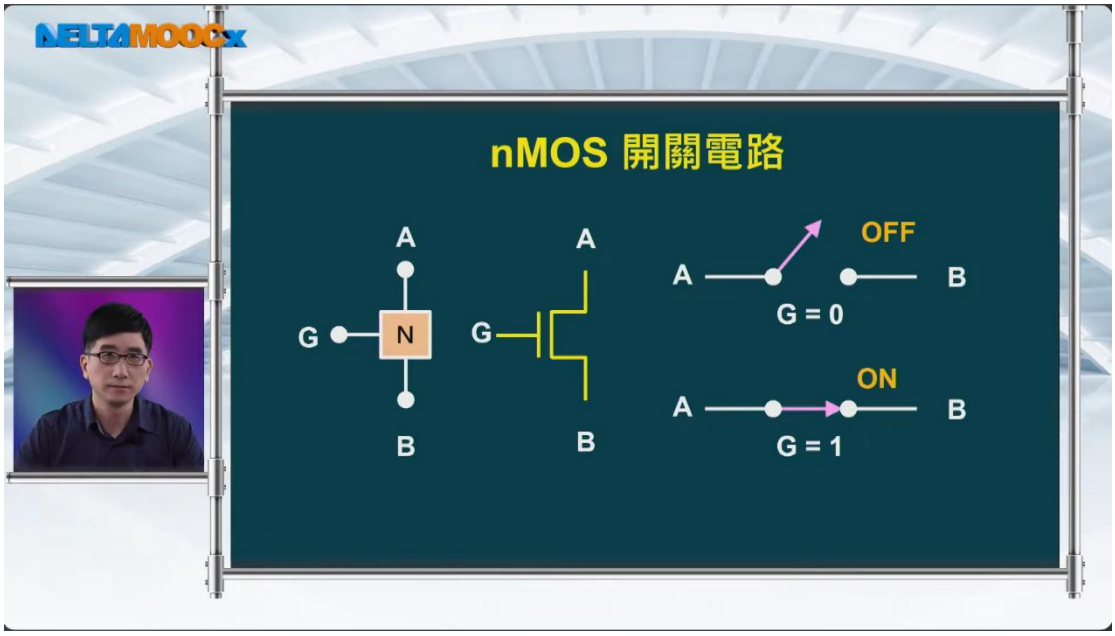
nMOS 的原理 (2/3)

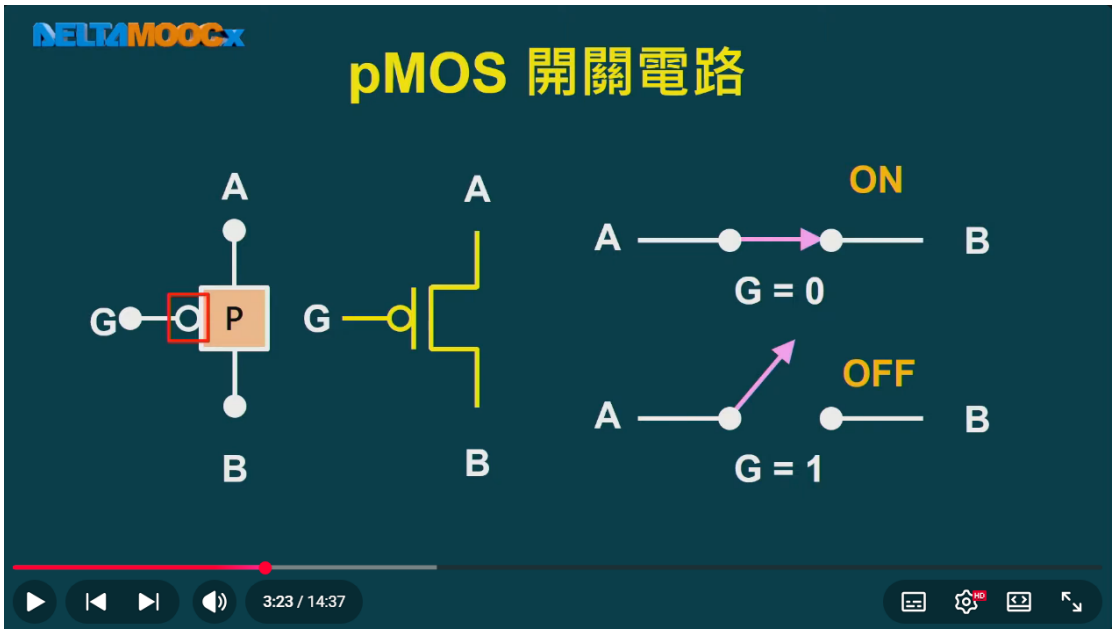


nMOS 的原理 (3/3)

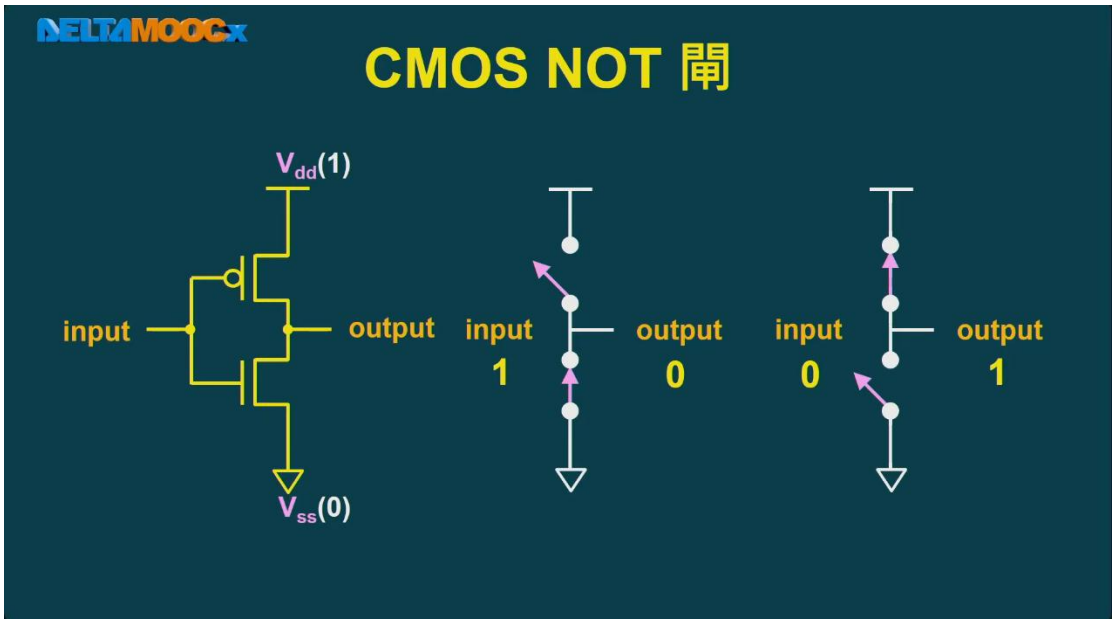


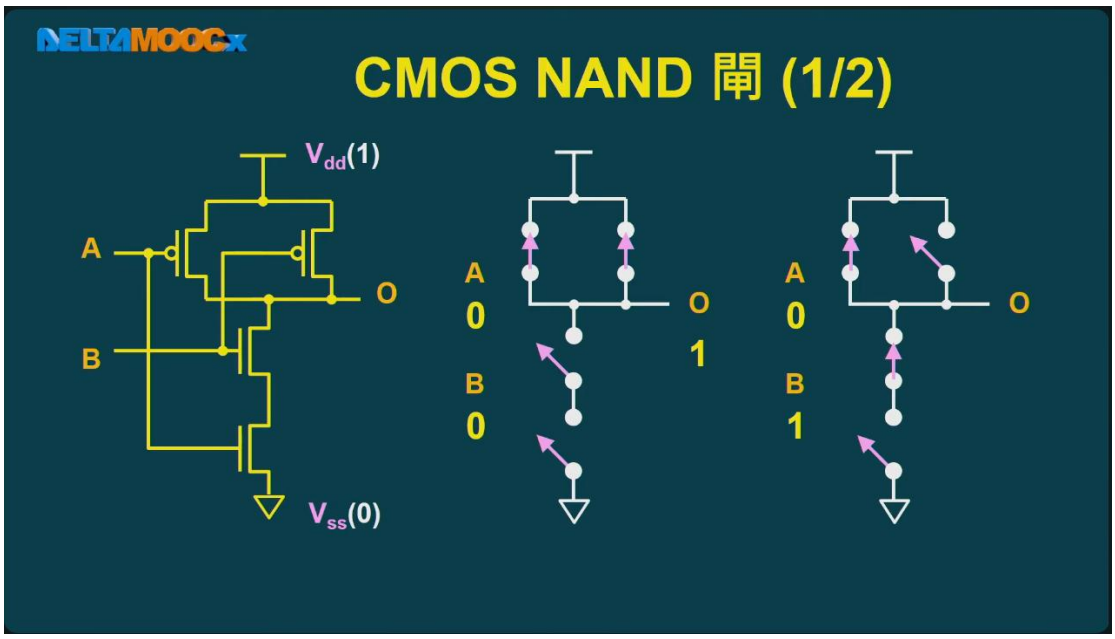
MOS 當 Switch 來用



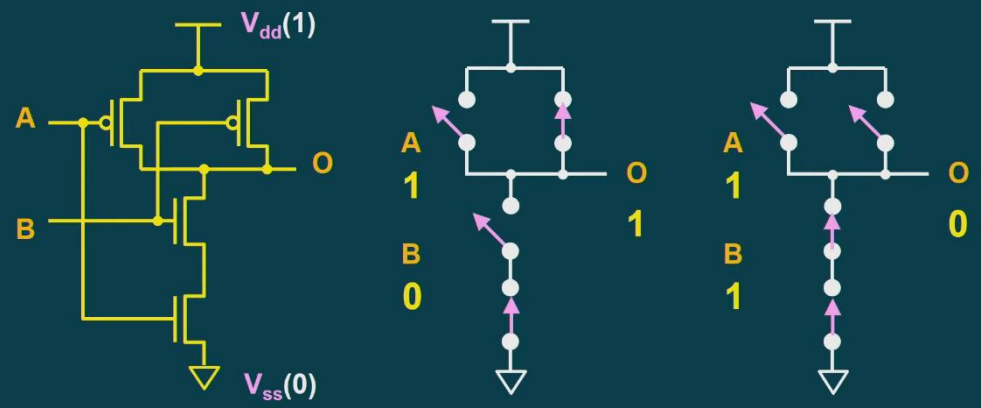


Complementary MOS，這裡的 Complementary 代表就叫做互補式的一種結構，它會同時運用到 N MOS 以及 P MOS 的電晶體來實現它

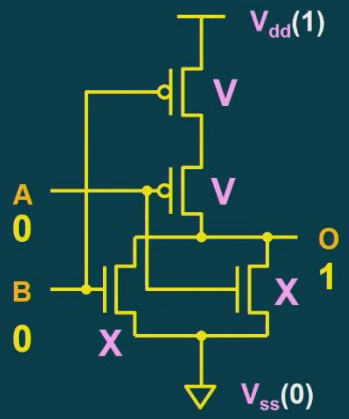




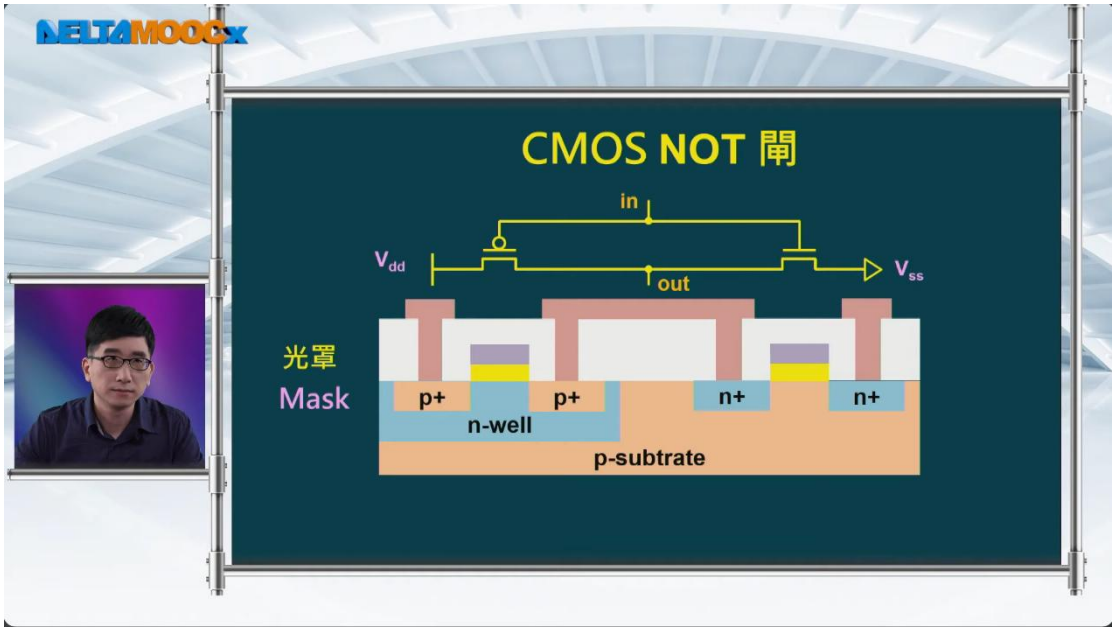
CMOS NAND 閘 (2/2)

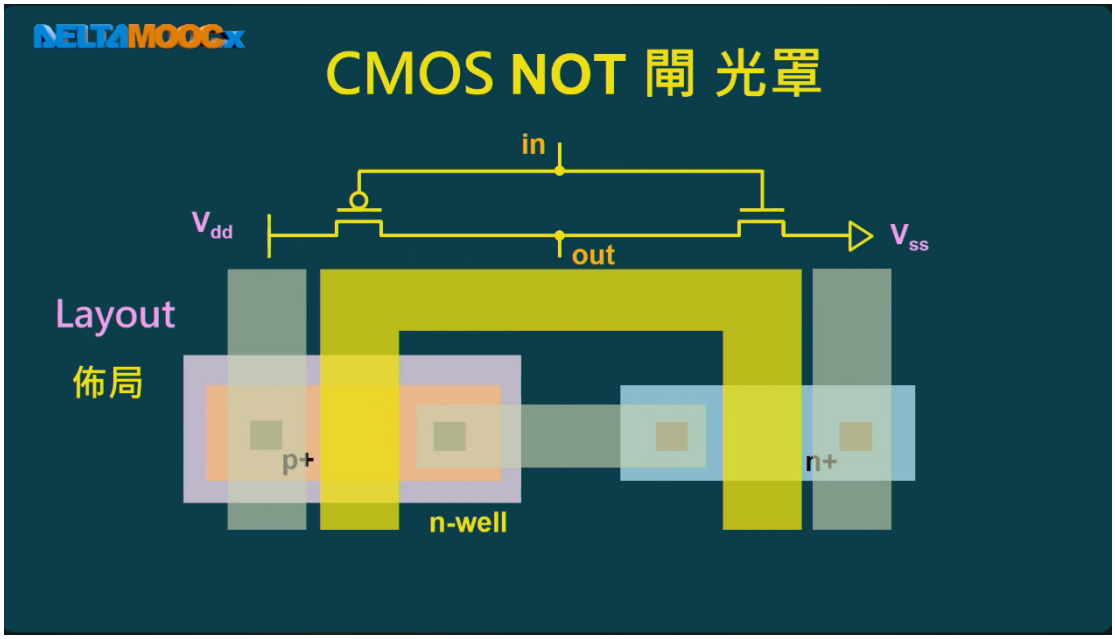


CMOS NOR 閘



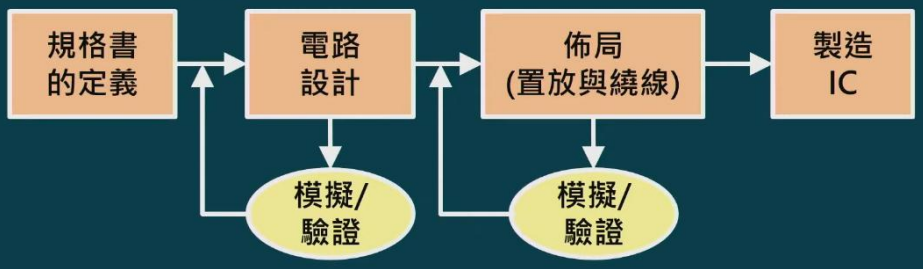
A	B	O
0	0	1
0	1	0
1	0	0
1	1	0

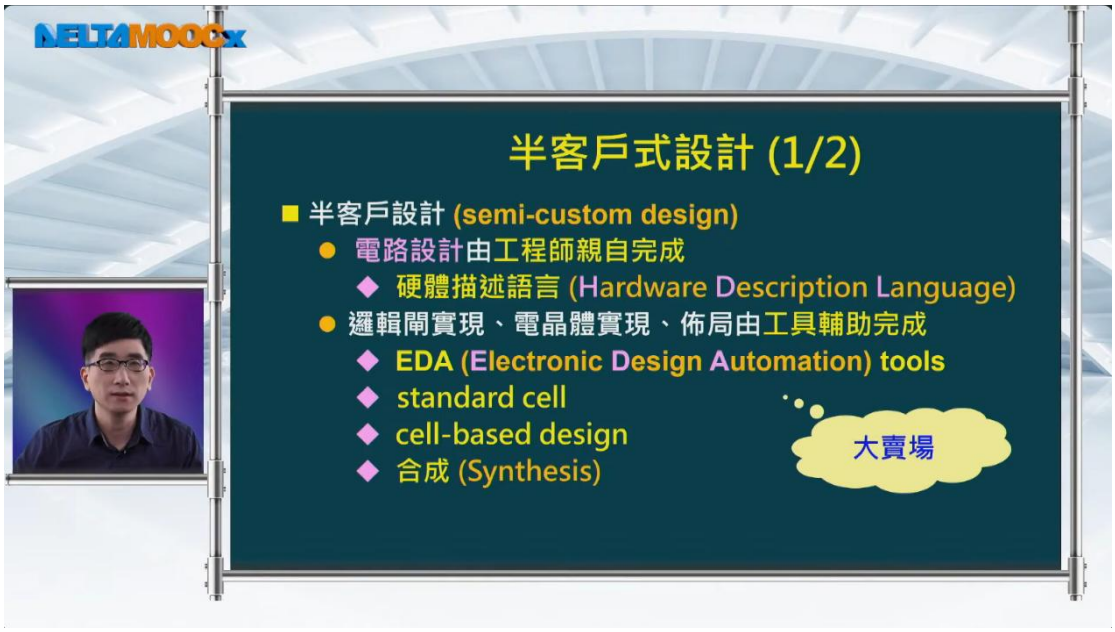

CMOS NOT 閘
in
V_{dd}
out
V_{ss}
光罩
Mask
p+
p+
n+
n+
n-well
p-subtrate


CMOS NOT 閘 光罩
in
V_{dd}
out
V_{ss}
Layout
佈局
p+
n+
n-well

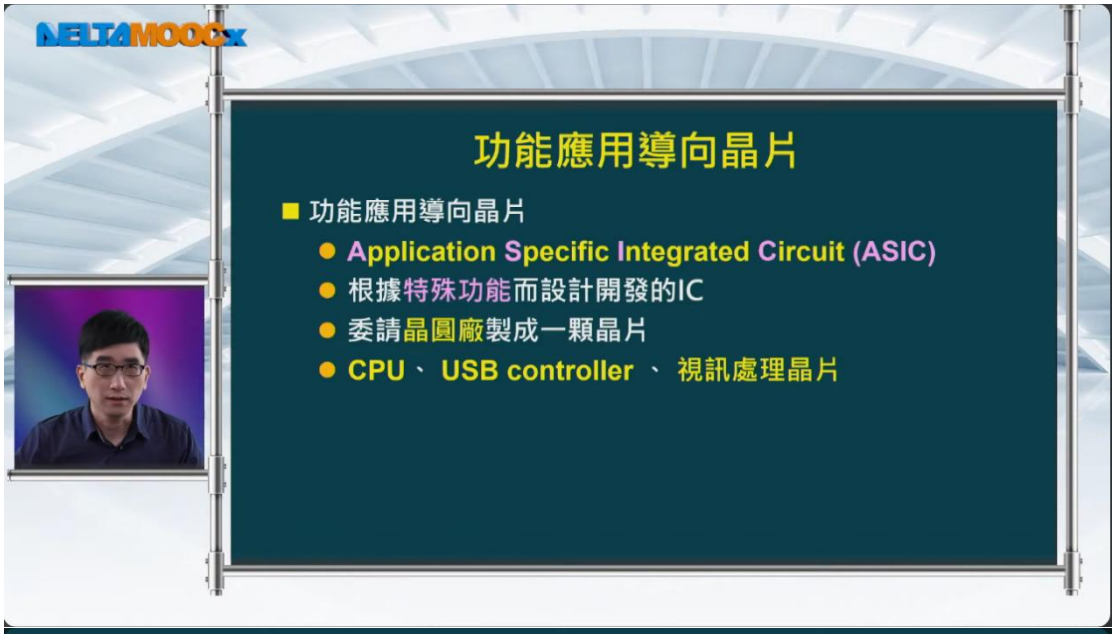
IC 設計流程

- IC 的設計流程
  - 全客戶式設計 (full custom design)
  - 半客戶式設計 (semi-custom design)




DELTAMOOCx
半客戶式設計 (1/2)
半客戶設計 (semi-custom design)
電路設計由工程師親自完成
硬體描述語言 (Hardware Description Language)
邏輯閘實現、電晶體實現、佈局由工具輔助完成
EDA (Electronic Design Automation) tools
standard cell
cell-based design
合成 (Synthesis)
大賣場


DELTAMOOCx
半客戶式設計 (2/2)
半客戶設計 (semi-custom design)
優點: 設計時程較為快速
缺點: 電路的最佳化有限
EDA 工具開發廠商
Cadence 、 Synopsys
IP 廠商
大型數位電路、SoC



FPGA / CPLD 實現電路

- Field Programmable Gate Array (FPGA)
  - 現場可程式規劃邏輯閘陣列
- Complex Programmable Logic Device (CPLD)
  - 複合式可程式規劃邏輯元件
- 半客戶式設計
  - 電路模型建立 (電路圖、HDL)
  - EDA tools 進行合成、模擬與驗證
  - 燒錄(program)到 FPGA/CPLD


DELTAMOOCx
ASIC 與 FPGA
ASIC
優點：面積較小、速度較快、功耗較低、單顆成本低
缺點：開發成本高、時程較長、修改不易
量產、成熟產品
FPGA / CPLD
優點：開發成本低、時程較短、修改容易
缺點：面積較大、速度較慢、功耗較高、單顆成本高
少量 、 驗證雛形、搶攻市場