IC Design Contest
Local Binary Patterns

王偉丞

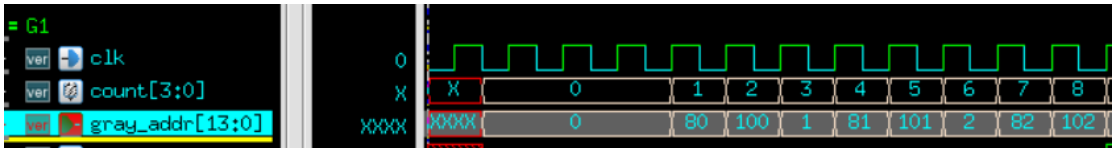
E94071217

國立成功大學工程科學系

gray_addr:

0 1 2
↓ ↓ ↓
128 129 130
↓ ↓ ↓
256 257 258

reset 後，gray_addr 設為 0，之後開始加 128 或減 255，一直做下去。



gray_addr 波形圖

存取 gray_data 之方式:

宣告 g0~g7 及 gc 之暫存器，存取九宮格內之 gray_data。當九宮格之暫存器存滿時就會開始左移。

g0 <= **g1** <= **g2** <= gray_data (if count%3==0)
g3 <= **gc** <= **g4** <= gray_data (if count%3==1)
g5 <= **g6** <= **g7** <= gray_data (if count%3==2)

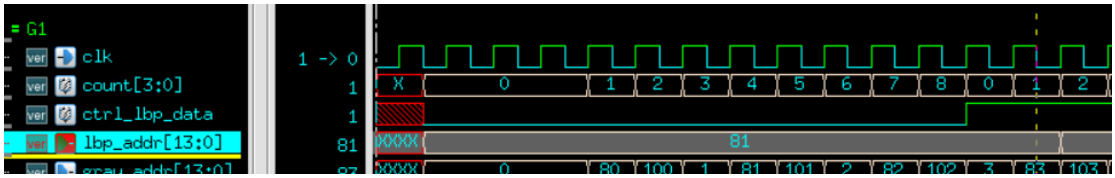
lbp_data:

此訊號會跟著時脈正緣做改變，將 gc 和 g0~g7 做比較，算出 lbp_data，但是隨著時脈做變動，一定會有錯誤之 lbp_data，所以需要控制 lbp_valid 來確保 Host 接收到對的資料。

lbp_addr:

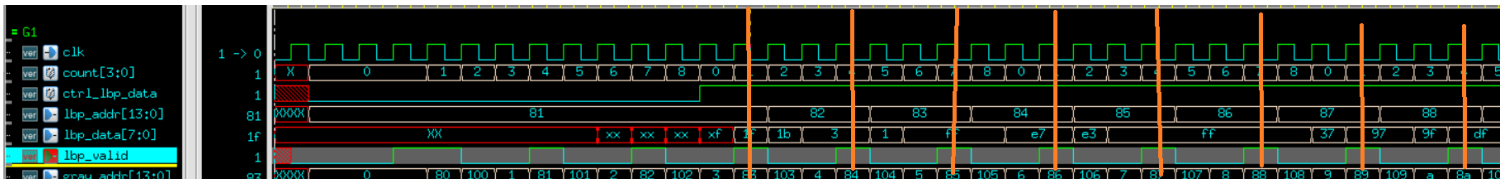
最一開始要讓 g0~g7、gc 暫存器都存取好資料並比較出 lbp_data 後才能開始改變 lbp_addr 的值，所以我設置了一個 **ctrl_lbp_data** 訊號，當此訊號拉高時，lbp_addr 才能改變。

改變的方式為過 3 個 cycle 就加一(用 **count** 控制)，但這樣會有邊界值，所以也需要 lbp_valid 確保 Host 接收到對的資料。



lbp_valid:

為了要取到對的 lbp_data，所以當 count%3==0 時，lbp_valid 才能拉高。然後要避免取到邊界的 lbp_addr，所以 lbp_addr%128==0 或 127 時，lbp_valid 要設為 low。



橘線部分為負緣時 Host 端接收到正確之 lbp_addr 及 lbp_data。

finish:

當 lbp_addr==16254 且 lbp_valid 為 high 時，finish 拉高。

模擬結果

RTL Simulation:

```
Output pixel: 0 ~        3000 are correct!
Output pixel: 0 ~        4000 are correct!
Output pixel: 0 ~        5000 are correct!
Output pixel: 0 ~        6000 are correct!
Output pixel: 0 ~        7000 are correct!
Output pixel: 0 ~        8000 are correct!
Output pixel: 0 ~        9000 are correct!
Output pixel: 0 ~       10000 are correct!
Output pixel: 0 ~       11000 are correct!
Output pixel: 0 ~       12000 are correct!
Output pixel: 0 ~       13000 are correct!
Output pixel: 0 ~       14000 are correct!
Output pixel: 0 ~       15000 are correct!
Output pixel: 0 ~       16000 are correct!
Output pixel: 0 ~       16383 are correct!
--------------------------------------------------

Congratulations! All data have been generated successfully!

-------------------------PASS-------------------------

Simulation complete via $finish(1) at time 604900 NS + 0
./testfixture.v:128       #(`CYCLE/2); $finish;
ncsim> exit
```

Gate level 合成:

```
Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
LBP                tsmc13_wl10           slow

Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.50       0.50
count_reg[2]/CK (DFFRX1)                 0.00       0.50 r
count_reg[2]/Q (DFFRX1)                  1.04       1.54 r
U396/Y (AND2X1)                          0.44       1.99 r
U387/Y (MXI2X1)                          0.59       2.58 r
U381/Y (OAI2BB1X1)                       0.42       3.00 r
U386/Y (MXI2X1)                          0.61       3.60 r
U383/Y (OAI2BB1X1)                       0.43       4.03 r
U388/Y (MXI2X1)                          0.60       4.64 r
U270/Y (NOR2X1)                          0.42       5.06 f
U371/Y (CLKBUFX3)                        0.45       5.51 f
U272/Y (NOR2X1)                          0.83       6.34 r
U373/Y (CLKBUFX3)                        0.86       7.19 r
g3_reg[0]/E (EDFFX1)                     0.00       7.19 r
data arrival time                                   7.19

clock clk (rise edge)                   10.00      10.00
clock network delay (ideal)              0.50      10.50
clock uncertainty                       -0.10      10.40
g3_reg[0]/CK (EDFFX1)                    0.00      10.40 r
library setup time                      -0.65       9.75
data required time                                  9.75
-----------------------------------------------------------
data required time                                  9.75
data arrival time                                  -7.19
-----------------------------------------------------------
slack (MET)                                         2.56
```

```
design_vision> uplevel #0 { report_area }

****************************************
Report : area
Design : LBP
Version: P-2019.03
Date   : Mon Oct 11 01:45:19 2021
****************************************

Library(s) Used:

    slow (File: /usr/cad/CBDK/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                          78
Number of nets:                          532
Number of cells:                         414
Number of combinational cells:           283
Number of sequential cells:              129
Number of macros/black boxes:              0
Number of buf/inv:                        60
Number of references:                     50

Combinational area:               2860.118986
Buf/Inv area:                      685.749608
Noncombinational area:            4163.722252
Macro/Black Box area:                0.000000
Net Interconnect area:           53853.607056

Total cell area:                  7023.841238
Total area:                      60877.448293
```

timing path　　area

Gate level Simulation:

```
Output pixel: 0 ~        3000 are correct!

Output pixel: 0 ~        4000 are correct!

Output pixel: 0 ~        5000 are correct!

Output pixel: 0 ~        6000 are correct!

Output pixel: 0 ~        7000 are correct!

Output pixel: 0 ~        8000 are correct!

Output pixel: 0 ~        9000 are correct!

Output pixel: 0 ~       10000 are correct!

Output pixel: 0 ~       11000 are correct!

Output pixel: 0 ~       12000 are correct!

Output pixel: 0 ~       13000 are correct!

Output pixel: 0 ~       14000 are correct!

Output pixel: 0 ~       15000 are correct!

Output pixel: 0 ~       16000 are correct!

Output pixel: 0 ~       16383 are correct!

--------------------------------------------------

Congratulations! All data have been generated successfully!

-------------------------PASS-------------------------

Simulation complete via $finish(1) at time 604887500 PS + 0
./testfixture.v:128       #(`CYCLE/2); $finish;
ncsim> exit
```

$604887.5\ ns * 7023.84 = 4.24*10^{9} < 1.2*10^{10}$

等級 A