113 學年度

國立中山大學

課程名稱：硬體描述語言

題目：Adder/Subtractor/
Multiplier Designs:
Non-Pipelined versus
Pipelined

作業/成果報告/專題

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一、Automatic verification

利用 testbench 內軟體計算預期答案，去對比 module 輸出之答案，若沒有 error，則會輸出 all test data correct，另外也有輸出 200 筆之 input/output 去對比。

1. nonpipeline

```
All test data correct!
$finish called from file "/home/B103040021 HDL/HW2/pre sim/nonpipeline/pre syn testbench.v", line 62.
```

2. pipeline

```
All test data correct !
$finish called from file "/home/B103040021_HDL/HW2/pre_sim/pipeline/pre_syn_testbench.v", line 81.
```

3. clockgating

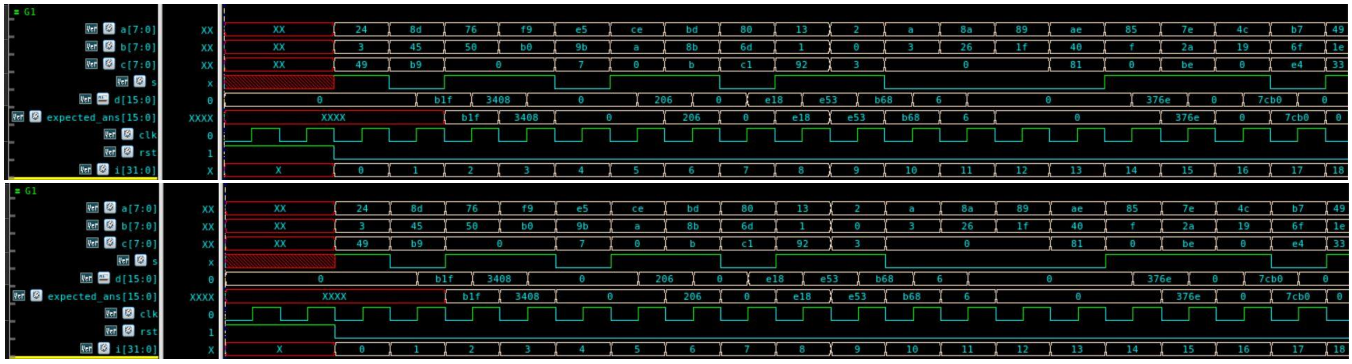
```
All test data correct !
$finish called from file "/home/B103040021_HDL/HW2/pre_sim/clockgating/pre_syn_testbench.v", line 81.
```

二、波形圖

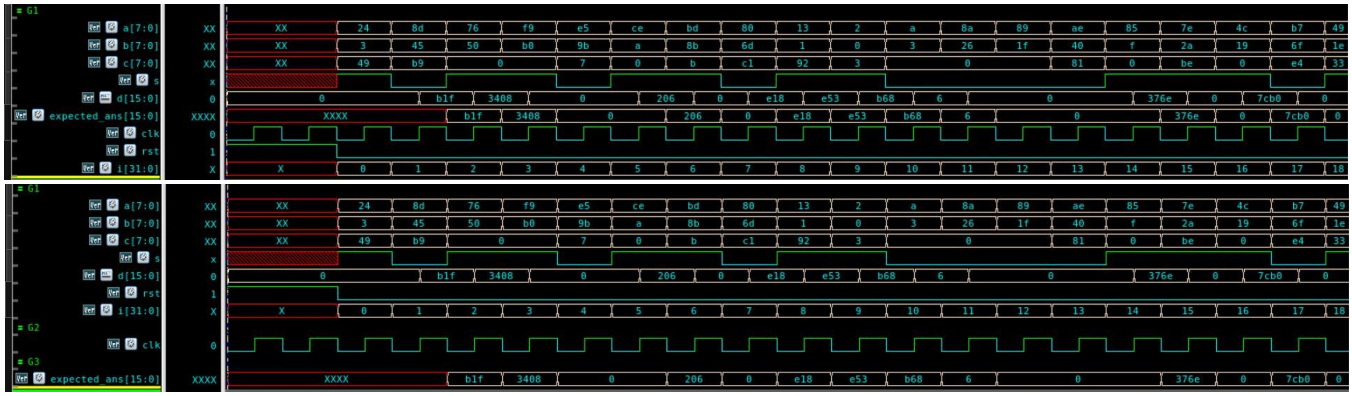
跟 hw1 時一樣，pre-sim 與 post-sim 之波形圖會長一樣，不同的是 nonpipe 與 pipe、clock-gate 之差別，因為 Pipe 與 clock-gate 有引入 clk 與 rst，所以一開始 value 會是 unknown，直到 rst 是 1，而 module 之 output d 會在 clk=1 時才會輸出。

1. nonpipeline

2. pipeline



3. clockgating



三、DC 的 area、timing、power

1. nonpipeline

i. Timing

```
max_delay                                                  0.26       0.26
output external delay                                      0.00       0.26
data required time                                                    0.26
--------------------------------------------------------------------------
data required time                                                    0.26
data arrival time                                                    -0.26
--------------------------------------------------------------------------
slack (MET)                                                           0.00
```

ii. Area

```
Combinational area:                343.077126
Buf/Inv area:                       22.498561
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                   343.077126
Total area:                 undefined
```

iii. Power

```
Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  = 833.4792 uW   (55%)
  Net Switching Power  = 672.8365 uW   (45%)
                         ---------
Total Dynamic Power    =   1.5063 mW  (100%)

Cell Leakage Power     = 352.7029 nW
```

2. pipeline

i. timing

```
clock clk (rise edge)                                  0.27       0.27
clock network delay (ideal)                            0.00       0.27
result_stage2_reg_reg_15_/CP (DFCNQD2BWP16P90LVT)      0.00       0.27 r
library setup time                                    -0.01       0.26
data required time                                                0.26
--------------------------------------------------------------------------
data required time                                                0.26
data arrival time                                                -0.26
--------------------------------------------------------------------------
slack (MET)                                                       0.00
```

ii. area

```
Combinational area:                175.322884
Buf/Inv area:                       18.299520
Noncombinational area:              37.946881
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area

Total cell area:                   213.269765
Total area:                 undefined
```

iii. Power

```
Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  = 581.7757 uW   (74%)
  Net Switching Power  = 200.0770 uW   (26%)
                         ---------
Total Dynamic Power    = 781.8527 uW  (100%)

Cell Leakage Power     = 186.6517 nW
```

3. clockgating

i. timing

```
clock clk (rise edge)                                   0.28       0.28
clock network delay (ideal)                             0.00       0.28
d_reg_13_/CP (DFCNQD2BWP16P90LVT)                       0.00       0.28 r
library setup time                                     -0.01       0.27
data required time                                                 0.27
-------------------------------------------------------------------------
data required time                                                 0.27
data arrival time                                                 -0.27
-------------------------------------------------------------------------
slack (MET)                                                        0.00
```

ii. area

```
Combinational area:                172.627204
Buf/Inv area:                       16.018560
Noncombinational area:              47.589122
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                   220.216325
Total area:                 undefined
```

iii. power

```
Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  = 614.6285 uW   (76%)
  Net Switching Power  = 194.6323 uW   (24%)
                         ---------
Total Dynamic Power    = 809.2607 uW  (100%)

Cell Leakage Power     = 180.5618 nW
```

四、數據表格

	Area (um^2)			Delay	Latency	Power (W)		
	CL	SL	Total	(ns)	(ns)	dynamic	leakage	total
Non-pipelined (DC)	343.077126	0	343.077126	0.26	0.26	1.5063	352.7029	354.2092
Non-pipelined (PrimeTime)				0.26	0.26	3.69e-04	3.5e-07	3.69e-04
Pipelined (DC)	115.32288	39.946881	213.269761	0.27	0.54	181.8527	186.6519	968.5044
Pipelined (PtimeTime)				0.27	0.54	8.99e-05	1.92e-07	8.99e-05
Clock-gated (DC)	172.627204	49.589122	220.216326	0.28	0.56	809.2609	180.5618	989.8225
Clock-gated (PrimeTime)				0.28	0.56	6.53e-05	2.22e-07	6.55e-05

五、Pipeline delay

由各階 pipeline 之 delay 可以看出 pipeline 與 clockgating 之 critical path 皆為 stage2。

1. pipeline
   i. stage1

```
clock clk (rise edge)                                    0.27       0.27
clock network delay (ideal)                              0.00       0.27
result_stage1_reg_reg_7_/CP (DFCNQD2BWP16P90LVT)         0.00       0.27 r
library setup time                                      -0.01       0.26
data required time                                                  0.26
-------------------------------------------------------------------------
data required time                                                  0.26
data arrival time                                                  -0.24
-------------------------------------------------------------------------
slack (MET)                                                         0.02
```

ii. stage2

```
clock clk (rise edge)                                    0.27       0.27
clock network delay (ideal)                              0.00       0.27
result_stage2_reg_reg_15_/CP (DFCNQD2BWP16P90LVT)        0.00       0.27 r
library setup time                                      -0.01       0.26
data required time                                                  0.26
-------------------------------------------------------------------------
data required time                                                  0.26
data arrival time                                                  -0.26
-------------------------------------------------------------------------
slack (MET)                                                         0.00
```

2. clockgating

i. stage1

```
clock clk (rise edge)                                    0.28       0.28
clock network delay (ideal)                              0.00       0.28
result_stage1_reg_reg_7_/CP (DFCNQD2BWP16P90LVT)         0.00       0.28 r
library setup time                                      -0.01       0.27
data required time                                                  0.27
-------------------------------------------------------------------------
data required time                                                  0.27
data arrival time                                                  -0.24
-------------------------------------------------------------------------
slack (MET)                                                         0.03
```

ii. stage2

```
clock clk (rise edge)                                    0.28       0.28
clock network delay (ideal)                              0.00       0.28
d_reg_13_/CP (DFCNQD2BWP16P90LVT)                        0.00       0.28 r
library setup time                                      -0.01       0.27
data required time                                                  0.27
-------------------------------------------------------------------------
data required time                                                  0.27
data arrival time                                                  -0.27
-------------------------------------------------------------------------
slack (MET)                                                         0.00
```

六、PT power

1. nonpipeline

Hierarchy	Int Power	Switch Power	Leak Power	Total Power	%
hw2_nonpipe	2.11e-04	1.58e-04	3.50e-07	3.69e-04	100.0
add_6 (hw2_nonpipe_DW01_add_2)	1.13e-05	1.07e-05	3.93e-08	2.21e-05	6.0
mult_6_2 (hw2_nonpipe_DW_mult_uns_6)	9.99e-05	7.26e-05	1.36e-07	1.73e-04	46.8
mult_6 (hw2_nonpipe_DW_mult_uns_7)	8.46e-05	5.97e-05	1.19e-07	1.44e-04	39.1
sub_6 (hw2_nonpipe_DW01_sub_2)	1.23e-05	1.46e-05	4.69e-08	2.70e-05	7.3

2. pipeline

Hierarchy	Int Power	Switch Power	Leak Power	Total Power	%
hw2_pipe	5.55e-05	3.42e-05	1.92e-07	8.99e-05	100.0
s1 (stage1)	4.44e-06	1.81e-06	1.31e-08	6.27e-06	7.0
add_46 (stage1_DW01_add_0)	1.97e-06	6.50e-07	4.56e-09	2.62e-06	2.9
sub_48 (stage1_DW01_sub_0)	2.14e-06	9.58e-07	5.46e-09	3.10e-06	3.5
s2 (stage2)	4.09e-05	3.12e-05	1.50e-07	7.23e-05	80.4
mult_61 (stage2_DW_mult_uns_1)	4.09e-05	3.12e-05	1.50e-07	7.23e-05	80.4

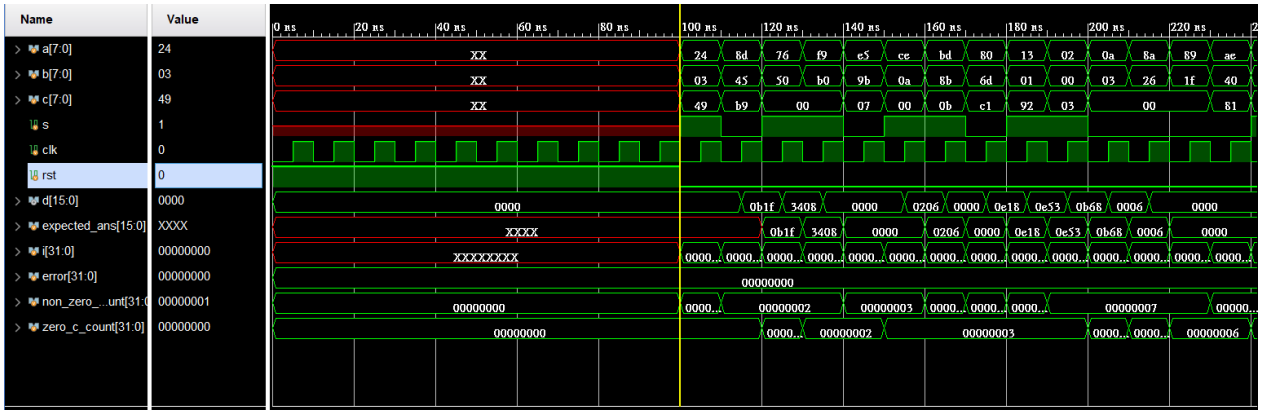
3. clockgating

Hierarchy	Int Power	Switch Power	Leak Power	Total Power	%
hw2_clock_gate	4.23e-05	2.30e-05	2.22e-07	6.55e-05	100.0
clk_gate_C128 (SNPS_CLOCK_GATE_HIGH_hw2_clock_gate)	1.87e-07	2.76e-07	7.78e-12	4.63e-07	0.7
s1 (stage1)	4.52e-06	1.84e-06	1.31e-08	6.37e-06	9.7
add_51 (stage1_DW01_add_0)	2.05e-06	6.81e-07	4.56e-09	2.73e-06	4.2
sub_53 (stage1_DW01_sub_0)	2.13e-06	9.54e-07	5.45e-09	3.09e-06	4.7
s2 (stage2)	2.69e-05	1.97e-05	1.65e-07	4.68e-05	71.4
mult_66 (stage2_DW_mult_uns_1)	2.69e-05	1.97e-05	1.65e-07	4.68e-05	71.4

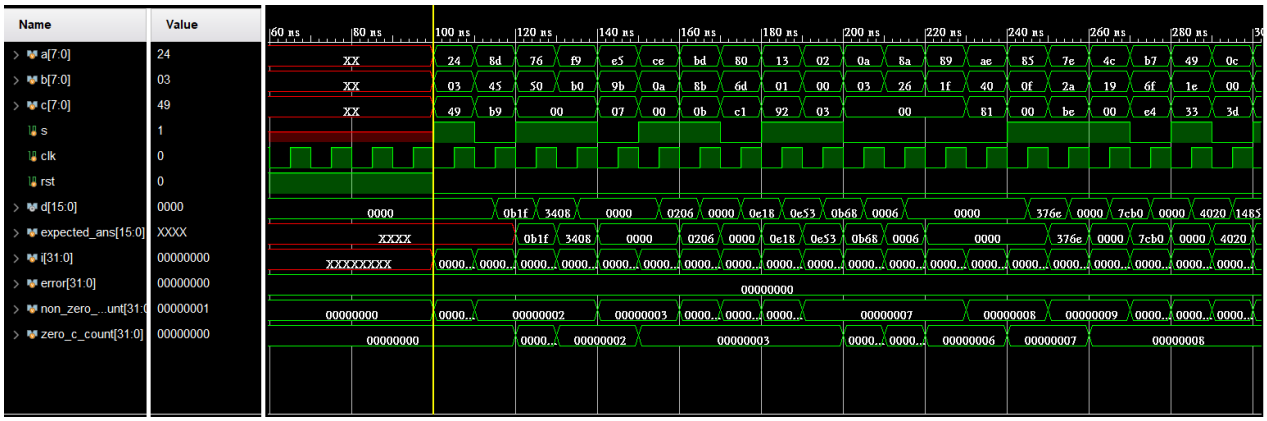
七、Vivado 波形圖

與 RTL 跟 gate-level 波形圖相似，pre-sim 與 post-imp 之波行長的一樣。

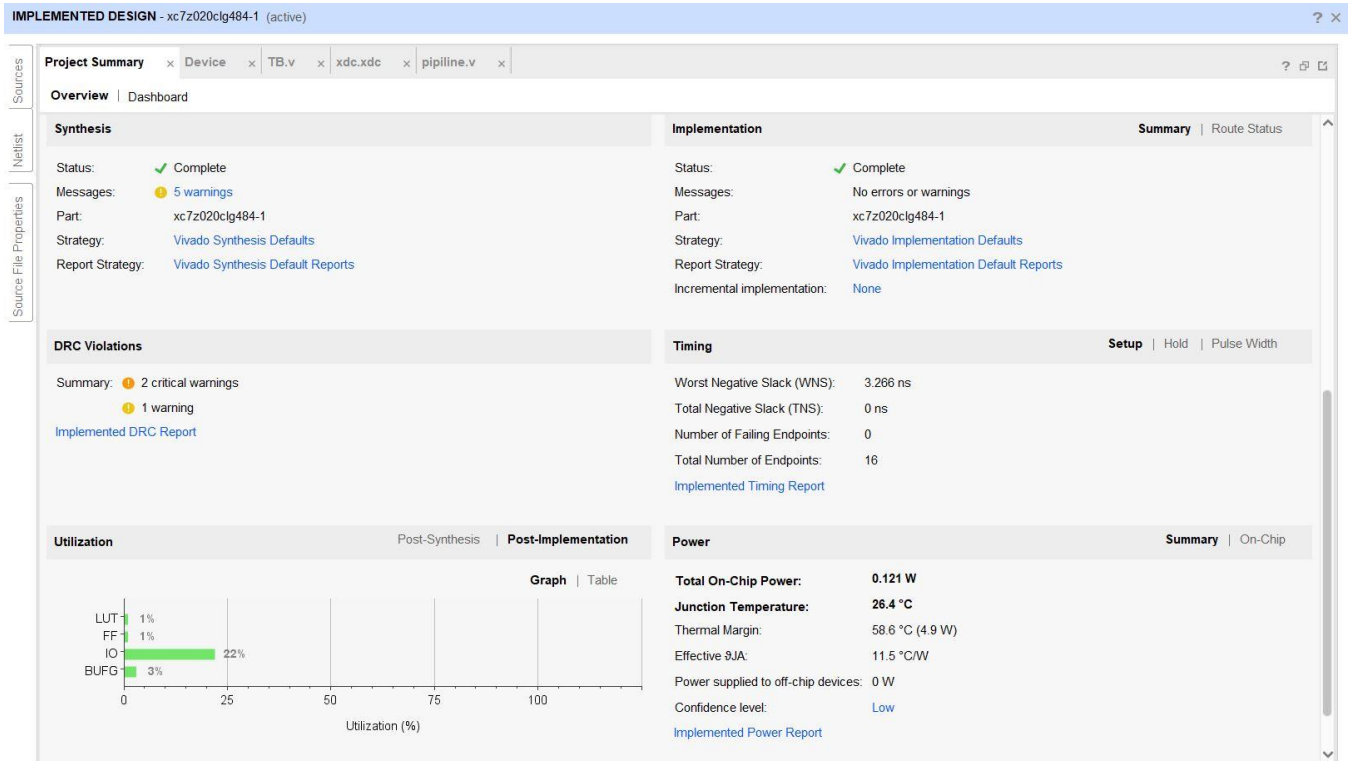
1. pre-sim



2. post-imp



八、Vivado summary



九、心得

這次作業 2 我遇到最多問題的地方是在設置 clockgating 時，一開始不太知道到底是要設在計算進行時或是存到暫存器時，後來透過 trial and error 才發現是要設在存到暫存器時，而且因為我們這次只有兩階 pipeline，所以只有辦法在第一階 pipeline 存到 register 時設置 clockgating，因為若設在第二階 pipeline 的話，這樣只要 c=0 時，output d 就不會被改到，從而導致答案錯誤。