UFE412 4.2.1 1875 Release Known Issues

Issue No. 1: July 2013

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Revision History

Issue No.	Issue Date	Details of Change
1	July 2013	Initial version

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1 About this document

The following is a list of known issues in UFE412 software,GA release 4.3.2.
All issues confirmed as known issues by PMC-Sierra Inc. are listed, regardless of whether or not a fix or patch is yet available. A description of the defect, as well as any known workarounds, is provided, along with the current status, and the modules or protocols affected (No customer-specific information will be divulged in the known issues list).
Defects related to proprietary customer features are not listed, as these would not be applicable to general customers. Also not listed are those issues still under investigation, for which the root cause may or may not be determined to be known issues.

2 Open Issues

The following issues have been confirmed as open issues in WDDS release 4.2.1:

#	Affected Component	Title	Issue
1.	HW FRAMER (UFE)	Data errors when setting the UFE4 to E1 framed PCM31CRC mode while enabling deep line loopback.	007153

Status: OPEN
Description:
When the UFE4 is set E1 framed PCM31CRC mode while enabling deep line loopback, the test equipment detects data errors.

#	Affected Component	Title	Issue
2.	HW FRAMER (UFE)	Sync mapping not supported in UFE412	007070

Status: OPEN
Description:
sync mapping is not supported currently in UFE412. The only mapping which is supported is WPX_UFE_FRAMER_CLIENT_MAPPING_BIT_ASYNC for E1/T1 facilities.

#	Affected Component	Title	Issue
3.	SW CORE (UFE)	One bit ECC when running data unit sizes which are less than 16 Bytes with UFE412	005513

Status: OPEN
Description:
UFE412 WUFE_EVENT_FM_RX_ECC_ONE_BIT event is constantly raised when UFE412 transparent Rx phy is configured with data unit size less than 16 bytes. The data integrity is not affected and this event can be treated as false alarm.

#	Affected Component	Title	Issue
4.	SW FRAMER (UFE)	Using Trace identifier in 16 byte mode- The UFE412 will pad the string with spaces till 15 byte length string	007297

Status: OPEN
Description:
When using trace identifer in 16 byte mode and configuring an expected or transmittted string which is shorter then 15 bytes, the UFE will pad the string with spaces instead of NULL characters - Note that in case that a String with NULL characters was passed to the expected/transmitted set API, the function will replace the NULL characters with spaces

#	Affected Component	Title	Issue
5.	SW WDDI/DPS (UFE)	UFE PWE3 CESoPSN does not work when located over UPI2	006801

Status: OPEN
Description:
When locating UFE3 or UFE4 over UPI the CES protocol may not work. The UFE Phy would constantly report WAIT. WAIT should never occur for transparent phy.

#	Affected Component	Title	Issue
6.	SW WDDI/DPS (UFE)	DPS UPI Rx threads can get stuck if Extended ATM statistics are disabled	006458

Status: OPEN
Description:
The DPS UPI Rx will stop responding with all threads being stuck when Extended ATM statistics are disabled. Invalid bus accesses can be seen via the winutil CLI function: "winutil tast"
Workaround:
Enable Extended PHY statistics when creating UPI Port: WP_port_upi.atm_ext->atm_characteristics |= WP_ATM_EXT_PHY_STATS_ENABLE.

#	Affected Component	Title	Issue
8.	HW OTHERS (UFE)	Phy time slots modification does not work well for UFE412	007420

Status: OPEN
Description:

There are 2 issues:

1. When changing PHY 0 slots assignment – for example 23 slots instead of 24 there is no decrease in throughput on PHY 0.

2. When changing the slot assignment on PHY n (n not 0), both Phy n and Phy 0 are affected.

#	Affected Component	Title	Issue
9.	HW OTHERS (UFE)	DS3 PM counters values are not accurate.	007530

Status: OPEN
Description:

DS3 PM counters values are not accurate.

#	Affected Component	Title	Issue
10.	HW OTHERS (UFE)	ATM protocol on DS3/E3 connections has throughput degradation when provisioning more than two connections	007639

Status: OPEN
Description:

When provisioning more than two connections of DS3/E3 in ATM protocol, there is a significant degradation in the traffic rate.

3 Restrictions

Following is a list of modes and configurations not supported or with limited support in UFE412 release 4.2.1:

#	Affected Component	Title	Issue
1.	HW FRAMER (UFE)	UFE412 does not support IDLE alarm for DS3	006959

Description:
IDLE alarm for DS3 is not supported

#	Affected Component	Title	Issue
2.	HW FRAMER (UFE)	Signal Degrade and Signal fail can't be configured to the same threshold simultaneously	007020

Description:
for a specific facility/port and byte (B1/B2/B3) the signal fail and signal degrade cannot be configured both to 10E5.

#	Affected Component	Title	Issue
3.	HW FRAMER (UFE)	There is no support in the HW for J1 trace length of 64 bytes in TU3 facility	007252

Description:
For TU3 facility there is no support for J1 mode of 64 bytes. Only 16 bytes trace length is available.

#	Affected Component	Title	Issue

#	Affected Component	Title	Issue
4.	HW FRAMER (UFE)	No downstream AIS consequent action occurs for E3/DS3 mode	007253

Description:
In E3/DS3 mode there is no support for downstream AIS consequent action in result to HO path alarms.

#	Affected Component	Title	Issue
5.	HW FRAMER (UFE)	Pointer adjustment not occurring in full bandwidth	005966

Description:
Byte/Bit Synchronous mapping mode is not supported for UFE412.

#	Affected Component	Title	Issue
6.	HW MAC-HDLC-TX (UFE)	Graceful disable must be enforced in the Tx direction when disabling UFE412 HDLC Phy	005790

Description:
HDLC Phy disable must be done after packet transmission is complete. That is the disable should not be done in the middle of packet transfer from the WP to the UFE.

Workaround:
The safe sequence is:
1) Disable the classifier rule that lead to HDLC Tx.
2) Build the iw_system
3) Wait till the transmit packets FIFO will be empty (can be verified by calling the API function WP_ChannelQDepth. Note that return value 1 means that the FIFO is empty).
4)Disable the Tx channel
5)Disable the Tx direction in the device.
6)Disable the UFE phy. When enabling, enable first the UFE phy, and afterwards the WP device.

#	Affected Component	Title	Issue

#	Affected Component	Title	Issue
7.	HW OTHERS (UFE)	Delays in T1 framed multiple PW per line Adaptive Clock Recovery mode.	005961

Description:
In E1\T1 framed multiple PW per line Adaptive Clock Recovery mode, if trying to create more than 2 PW per line over more than 100 lines, big delays (up to 250us) in the transfer of the Data units may occasionally rise. This may cause performance issues in the ACR algorithm (PSN2TDN)and raise under-run conditions in CES shaping mode(TDM2PSN).

#	Affected Component	Title	Issue
8.	SW CORE (UFE)	UFE supports only WP id equals to 0.	007273

Description:
UFE supports only WP id equals to 0.

#	Affected Component	Title	Issue
9.	SW CORE (UFE)	CR ACR CES shaping requires differential clock to be connected to BRGin	005765

Description:
In ACR mode, the CES shaping mode requires the differential reference clock to be connected to one of the BRG inputs in the TDM2PSN system.

#	Affected Component	Title	Issue
10.	SW FRAMER (UFE)	In Dual EMPHY, releasing UFE0 before UFE1 causes data access error	006257

Description:
In the DUAL EMPHY configuration UFE0 need to be connected to UPI1 and UFE1 connected to UPI3. Calls to WUFE_UfeRelease performed in the order (1) release UFE0 on UPI1, then (2) release UFE1 on UPI3 cause a MIPS data access error when attempting to reference

memory of the second UFE.

Workaround:
Calls to WUFE_UfeRelease must be performed in the order (1) release UFE1 on UPI3, then (2) release UFE0 on UPI1.

#	Affected Component	Title	Issue
11.	SW WDDI/DPS (UFE)	Clock Recovery Debug DCOs not working on second UFE4	006282

Description:
The debug DCOs on the second UFE in a Dual UFE4 system is not functioning.

Workaround:
Output the desired lines (First and second UFE) frequencies through the first UFE's DCOs.

#	Affected Component	Title	Issue
12.	SW WDDI/DPS (UFE)	UFE4 ACR Rx channel disable requires delay	006382

Description:
UFE4 ACR PW delete scenario requires a delay between UPI Rx channel disable and the TDM2PSN IW flow aggregation delete. The UPI Rx channel delete should only be called after the IW Flow aggregation delete. The delay should be bigger than the time it takes to receive the packet from the TDM interface.

Workaround:
Apply delay between the channel disable and the IW flow disable/delete calls. (WP_ChannelDisable & WP_IwFlowAggregationDelete)

#	Affected Component	Title	Issue
13.	SW WDDI/DPS (UFE)	UFE initialization must be done after UPI port create and enable.	006912

Description:
The WUFE_UfeInit() function should be called only after calling the function WP_PortEnable()

of the relevant UPI port which is configured to EMPHY mode.

#	Affected Component	Title	Issue
14.	SW WDDI/DPS (UFE)	ATM BYPASS can't be supported on UFE ATM device	006410

Description:
UPI ports configured to work with UFE do not support the following ATM VP/VC look-up modes: WP_ATM_LOOKUP_BYPASS_HASH_UNI
WP_ATM_LOOKUP_BYPASS_HASH_NNI
WP_ATM_LOOKUP_BYPASS_VP_AND_HASH_UNI
WP_ATM_LOOKUP_BYPASS_VP_AND_HASH_NNI

#	Affected Component	Title	Issue
15.	SW FRAMER (UFE)	Deletion and creation of the PDH facility result in LP-TIM and LP-UNEQ alarms	007051

Description:
When deleting and creating a PDH facility there will be LP-TIM and LP-UNEQ alarms caused by mismatch in the V5 octet in the J2 string value Workaround: After deletion and creation of a PDH facility, need to call again to the APIs setting the V5 value and the J2 string value

#	Affected Component	Title	Issue
16.	SW FRAMER	HP-LOM alarm category should be disabled unless there are E1/T1 connections under the HO path	007580

Description:
HP-LOM alarm is relevant only for HO paths under which there are E1/T1 connections.

For all other modes (E3/T3 or clear channel) the HP-LOM alarm category should be disabled.

#	Affected Component	Title	Issue
17.	SW FRAMER	User must provide a 64 byte length string when calling the J2 set/get API's	007603

Description:

When the user calls the J2 string set/get API's, he must provide as parameter a 64 bytes length string, since the framer driver pads with NULL character the string starting from offset 16 till offset 64.

4 Fixed / Closed Issues

The following issues have been resolved since WDDS release 4.3.1:

#	Affected Component	Title	Issue
1.	HW FRAMER (UFE)	Data corruption on the DDR3 interface due to jitter clock	007289

Status: CLOSED
Description:
We have detected a high DDR3 clock jitter value when UFE412 full chip is configured and traffic is running at maximum bandwidth. In some cases the high clock jitter can result in a data corruption on the DDR3 data bus (see note a). A clock-balancing modification was implemented in the UFE412 and is included in this WDDS4.3.2 release significantly reducing the maximum detected jitter. With this improvement all data corruption issues have been resolved.

Notes:

a. DDR3 Data integrity issues are detected by ECC events on the UFE interrupt bus.

b. Data corruption was not found on all boards.

#	Affected Component	Title	Issue
2.	HW FM (UFE)	ATM in STM4 - Clear channel does not reach full bandwidth	006809

Status: CLOSED
Description:
STM4/ OC12 does not reach full rate with ATM due to reduce number of parallel threads.

#	Affected Component	Title	Issue
3.	HW FRAMER (UFE)	AIS_P wrong indication might occur after changing configuration between channelized and clear channel	007088

Status: CLOSED

Description:
in board to board configuration SONET OC12 E1(or T1) mode (Or SDH VC3 E1/T1), delete all the E1 facilities and STS1 on one board, create 4 STS3C CC facilities, then delete the CC facilities and re-create all the STS1/E1 facilities AIS_P alarm might appear for some of the STS1 facilities.

#	Affected Component	Title	Issue
4.	HW FRAMER (UFE)	the EXC and DEG alarms need to configured with thresholds E3-E5	006759

Status: CLOSED
Description:
EXC and DEG alarms cannot work with threshold E6-E9

#	Affected Component	Title	Issue
5.	HW FRAMER (UFE)	incorrect ingress de-mapping of T1 on VC11	007030

Status: CLOSED
Description:
The UFE4 framer might suffer bit losses (slip errors) in the ingress direction when working with VC-11 (T1). The issue is seen only when working with particular ADMs, or SONET multiplexors for example RAD's FCD-155. When PDH TX timing is set to "RX timing" (loop timing), the egress direction is also affected. Does not affect VC-12 (E1).

#	Affected Component	Title	Issue
6.	HW FRAMER (UFE)	Uncontrolled accesses into the framer DDR when an invalid H4 byte is received	007131

Status: CLOSED
Description:
Upon heavy load of reports, alarms and PMs are enabled on the Overhead Pre-processor, the Overhead Pre-processor memory in the DDR might get corrupted. This causes an unrecoverable

failure in Overhead processing mechanism.

#	Affected Component	Title	Issue
7.	HW FRAMER (UFE)	When the UFE detects PDH_LOF in the RX the upstream RAI injection might be not stable - when working in T1 ESF mode	007018

Status: CLOSED
Description:
In T1 ESF mode, When the UFE detects PDH_LOF in the RX direction the consequent action of sending upstream PDH_RAI is not constant. The RAI upstream will toggle in and out.

#	Affected Component	Title	Issue
8.	HW FRAMER (UFE)	False indications of TU_AIS and TU_LOP may be reported to user application due to overflow in pointers FIFO	007069

Status: CLOSED
Description:
in very rare cases, once every 5 runs of a stress scenario which enable/disable all the lines, sporadic TU_AIS and TU_LOP alarm might raise to the application by mistake.

#	Affected Component	Title	Issue
9.	HW FRAMER (UFE)	There is deviation in the 1 second counting of the PM	007260

Status: CLOSED
Description:
Inaccuracy in the 1 second toggling mechanism for PM information

#	Affected Component	Title	Issue

#	Affected Component	Title	Issue
10.	HW OTHERS (UFE)	UFE412 Clear Channel change from 4XOC3 to 1XOC12 fails	005831

Status: CLOSED
Description:
Changing the mode from 4xOC3 to 1xOC12 in clear channel configuration (from VC4/STS3 to VC4_4C/STS12) will cause the VC4_4C/STS12 mode to fail. This is because the FLEXMUX framer still has some STM1/OC3 configurations on the RX side. Additional problem is when moving from STM4/OC12 to 1xSTM1/OC3, the line 0 must always be configured first.

#	Affected Component	Title	Issue
11.	SW CORE (UFE)	WUFE_SfpWrite function works only for sfp_id=0	007073

Status: CLOSED
Description:
the sfp_id parameter was not set correctly by the function and therefore all writes were directed to SFP 0.

#	Affected Component	Title	Issue
12.	SW FRAMER (UFE)	When bringing up the UFE412 system, a false LOS alarm indication might appear.	007026

Status: CLOSED
Description:
When bringing up the UFE412 system, a false LOS alarm indication might appear for the UFE412, which has during the bring-up an optical cable connected. This false indication is only for the first port.

#	Affected Component	Title	Issue
13.	SW FRAMER (UFE)	false TU-LOP alarm might raise for a new LO facility	006916

Status: CLOSED

Description:
false TU-LOP alarm is raised if a new LO facility is created and there is TU-AIS present. once the TU-AIS will be cleared the wrong TU-LOP will NOT be cleared

#	Affected Component	Title	Issue
14.	SW FRAMER (UFE)	deletion of one low order VT might cause loss of data on another VT	006915

Status: CLOSED
Description:
When deleting a low order VT (VC11, VC12, VT15, VT2) a wrong VT is AISed downstream causing loss of data

#	Affected Component	Title	Issue
15.	SW FRAMER (UFE)	HP-RDI and LP-RDI are not injected as result of HP-UNEQ, HP-PLM or HP-TIM detection	006613

Status: CLOSED
Description:
HP-RDI and LP-RDI will not be injected to far end as a result of HP-UNEQ, HP-PLM or HP-TIM detection in the RX direction.

#	Affected Component	Title	Issue
16.	SW FRAMER (UFE)	The enabling of the PLM-P alarm in sonet mode does not affect to get the alarm	007050

Status: CLOSED
Description:
The enabling of the PLM-P alarm does not make the relevant change in the firmware in order to get the alarm status to the application. Therefore the alarm won't be enabled even if the user calls the API to enable PLM-P alarm category.

#	Affected Component	Title	Issue
17.	SW FRAMER (UFE)	Deleting port of sonet will set the port mode to sdh mode causing failure when trying to create again the sonet port.	006957

Status: CLOSED
Description:
When creating, deleting and creating again one port on sonnet mode, an error will be retrieved on the WPX_FRMR_SONET_SDH_PORT_SetRate API, announcing that the device does not support the port rate.

#	Affected Component	Title	Issue
19.	SW FRAMER (UFE)	AU_AIS alarm not cleared after raised when working with instruments that send NDF when go out of AU_AIS	007013

Status: CLOSED
Description:
when the UFE412 detect AU_AIS, if the first pointer that the UFE will detect will include the NDF flag then no clear AU_AIS message will be send to the application. Note: the consequent action of sending HP_RDI upstream and AIS the data downstream will behave correctly.

#	Affected Component	Title	Issue
20.	SW FRAMER (UFE)	J1 not working in 64 bytes mode	007014

Status: CLOSED
Description:
when setting the J1 mode to 64 bytes only the RX configuration are correct in the HW, and therefore the TX will remain in 16 Bytes mode

Affected	Title	Issue

#	Component		
21.	SW FRAMER (UFE)	Change configuration from 1 VC4_4C clear channel to VC4 Clear Channel cause Tx requests to be stopped	007019

Status: CLOSED
Description:
When working in 1xOC12 build personality and changing the configuration of the first port from a single VC4_4C clear channel to 4 VC4s Clear Channels the TX threads are stuck.

#	Affected Component	Title	Issue
22.	SW FRAMER (UFE)	TIM_V message not raised to the user application	007068

Status: CLOSED
Description:
TIM_V alarm is not raise to the user application. When the received j2 byte is not equal to the expected j2 byte the HW will detect TIM_V and if necessarily a consequent action of upstream RDI_V and downstream AIS will occur but the user will not receive a message of TIM_V alarm.

#	Affected Component	Title	Issue
23.	SW FRAMER (UFE)	upstream LP_RDI insertion will be stopped once one of LP_UNEQ/LP_TIM alarms are clear	007089

Status: CLOSED
Description:
when the UFE412 detects LP_UNEQ or LP_TIM alarm it will insert LP_RDI upstream as consequent action. When the UFE412 detects that one of the alarms (LP_TIM/LP_UNEQ) has been cleared it will stop the insertion of LP_PLM upstream without checking that both of the alarms are cleared.

#	Affected Component	Title	Issue

#	Affected Component	Title	Issue
24.	SW FRAMER (UFE)	No Port level alarms available on the second port in 2+2 build personality. Both working and protected port.	007163

Status: CLOSED
Description:
No Port level alarms available on the second port in 2+2 build personality. Both working and protected port.

#	Affected Component	Title	Issue
25.	SW FRAMER (UFE)	PM data storage corruption.	007165

Status: CLOSED
Description:
The PM mechanism will override data, causing a false PMs statistics data.

#	Affected Component	Title	Issue
26.	SW WDDI/DPS (UFE)	Loss of Cell Delineation (LCD) status not passed to IMA layer.	006584

Status: CLOSED
Description:
Loss of Cell Delineation (LCD) status not passed to IMA layer.

#	Affected Component	Title	Issue
27.	SW WDDI/DPS (UFE)	UFE4 WP_DEVICE_HSPOS device handles incorrectly CRC, and conflicts with buffer chaining	006639

Status: CLOSED
Description:
UFE4 WP_DEVICE_HSPOS device handles incorrectly CRC, and conflicts with buffer chaining UFE4 POS fast layer2 which is created with WP_DeviceCreate (...WP_DEVICE_HSPOS...) is set to work with CRC32 only. Appose to regular Ethernet it does

not remove the FCS, therefore the device should not be configured to work with buffer chaining (i.e. Qnode.buffer _size >= (maxsdu+IWSystem.gap_offset) There is no API to configure the TDM traffic to be CRC 16 even with correct setting of the UFE phy would cause data corruption.

#	Affected Component	Title	Issue
28.	SW WDDI/DPS (UFE)	HEC error cells would pass to the ATM address look-up module. may cause DPS locking issue	006815

Status: CLOSED
Description:
Cells received with HEC/Parity errors over UFE/IMA links are not always dropped and may lead to stuck threads.

#	Affected Component	Title	Issue
29.	HW EMPHY (UFE)	when configure the ufe to mixed mode of ATM and another protocol the data might get stuck	007021

Status: CLOSED
Description:
When running a configuration mixed mode of ATM and other protocol (CES/HDLC/POS)the TX threads might get stuck and all data is corrupted. possible events:
WUFE_EVENT_EMPHY_EGRESS_PHY_NOT_VALID
WUFE_EVENT_FM_TX_DDR_UNDERRUN

#	Affected Component	Title	Issue
30.	HW FRAMER (UFE)	M1 counter doesn't get the expected results	007099

Status: CLOSED
Description:

M1 PM counter doesn't get the expected results. Caused by incorrect accumulation in the framer HW. Fixed in release 4.3.2

#	Affected Component	Title	Issue
31.	HW FRAMER (UFE)	The 1-second counter counted 0.999897 s	007096

Status: CLOSED
Description:
The Performance monitoring mechanism is inaccurate due inaccurate HW counter. The "1-second" HW measurement is incorrect by +/-0.1% and this leads to inaccurate performance reporting at all the SDH/SONET/PDH levels. The issue is fixed in release 4.3.2

#	Affected Component	Title	Issue
32.	SW WDDI/DPS (UFE)	DPS UPI Rx threads can get stuck if Extended ATM statistics are disabled	006458

Status: CLOSED
Description:
The DPS UPI Rx will stop responding with all threads being stuck when Extended ATM statistics are disabled. Invalid bus accesses can be seen via the winutil CLI function: "winutil tast"

#	Affected Component	Title	Issue
33.	SW FRAMER (UFE)	MS_AIS will be raise during start-up in case MS_RDI is detected	007313

Status: CLOSED
Description:
If the UFE412 detect MS_RDI in the RX when enabling the alarm category it will raise MS_AIS alarm instead of MS_RDI.

#	Affected Component	Title	Issue
34.	HW MAC-POS-TX (UFE)	During Pos Tx machine operation, rare cases will cause the machine to freeze and stop asserting Tx requests to the Winpath	007315

Status: CLOSED
Description:
There are two cases which will cause the POS TX machine to get stuck and stop asserting TX requests.

1. When the machine is in Inter-Frame state and transmits FLAG or IDLE octets, and the incoming buffer descriptor does NOT contain Start of Frame indication (SOP)

2. When the machine suffered Underrun condition and the incoming buffer descriptor does NOT contain Start of Frame indication.

These cases can be causes by various scenarios, for example when the Winpath transmits long frames and the UFE Phy is being Enabled/Disabled, without disabling the channel in Winpath.

#	Affected Component	Title	Issue
35.	SW FRAMER (UFE)	Error may return when creating the DS3 line in reverse order	007507

Status: CLOSED
Description:

Creating DS3 line in reverse order may return the error of "WPX_UFE_FRAMER_ERROR_FACILITY_BLOCKED_BY_PEER"

#	Affected Component	Title	Issue
36.	HW FRAMER (UFE)	Synchronization errors occur in E3 mode, when the framer configured to master in the PDH & SONET level	007488

Status: CLOSED
Description:

Configuring the UFE412 framer to E3 master mode (in both SDH & PDH level) will cause synchronization errors.

There will be LSS in the test equipment and buffer underrun or overrun events will be raised in the WP statistics.

#	Affected Component	Title	Issue
37.	HW FRAMER (UFE)	When a single VTG of VT1.5 (TUG2 of TU11) contains both Framed and Unframed T1 tributaries, all the four T1 are stuck in LOF state	007502

Status: CLOSED
Description:

On the the Near End (SONET/SDH receive direction), when a certain VT-Group of four VT1.5 (or single TUG2 of four TU11) contains at least one Unframed T1, all the tributaries in this VT-group fail to find framing and remain in LOF state.

#	Affected Component	Title	Issue
38.	HW FRAMER (UFE)	False PDH AIS may be detected in E1 framed mode when the payload is all 1's	007328

Status: CLOSED
Description:

When working in E1 framed mode.

If the PDH payload is all 1's and the E1 national bits are set, the UFE412 framer may detect false AIS condition.

The probability for the false detection increases if the RAI bit is also asserted.

#	Affected Component	Title	Issue
39.	SW FRAMER (UFE)	UFE412 DS3\E3 PDH facilities must be created in incremental order	007507

Status: CLOSED
Description:

Creating DS3\E3 framer PDH facilities in reverse order may return the error of "WPX_UFE_FRAMER_ERROR_FACILITY_BLOCKED_BY_PEER"

#	Affected Component	Title	Issue
40.	HW FRAMER (UFE)	False PDH alarms may be reported if multiple PDH connections change state simultaneously	007528

Status: CLOSED
Description:

When a change occur in the PDH state (LOS, LOF, RAI, RFI)for a large amount of PDH facilities simultaneously, it may cause for several PDH alarm to get stuck in wrong state.

#	Affected Component	Title	Issue
41.	HW FRAMER (UFE)	Failure to switch to E3/DS3 framed mode	007314

Status: CLOSED
Description:

When configured to DS3/E3, the framer may occasionally fail to switch to the requested state

and may remain in unframed mode in the ingress direction. As a result, the data at the output will be corrupted and the appropriate RDI bit (X for DS3, A for E3) will be asserted at the egress direction.

#	Affected Component	Title	Issue
42.	HW FRAMER (UFE)	AU-AIS might not be asserted during loss of signal in the port level	007532

Status: CLOSED
Description:
When there is no signal in the SONET/SDH level the AU-AIS alarm might not be raised

#	Affected Component	Title	Issue
43.	SW FRAMER (UFE)	False HP/LP-PLM alarm might be raised when the UNEQ alarm is enabled and the PLM disabled	007551

Status: CLOSED
Description:
When enabling the UNEQ alarm and the PLM alarm is disable for an HO/LO facility in some rare cases the PLM alarm will be raised and will cause consequent action of up-stream RDI and down-stream AIS

#	Affected Component	Title	Issue
44.	SW CORE (UFE)	UFE4 clear channel OC12 ATM Cell transmitted only when the next cell arrived from the Winpath.	006395

Status: CLOSED

Description:
When using UFE412 as OC12 clear channel, the last cell provided by the WinPath is held

(stuck) in the UFE transmit FIFO. This cell is transmitted when the next cell arrived from the Winpath. This behavior increases the latency of the ATM OC12 Clear Channel.

#	Affected Component	Title	Issue
45.	HW FRAMER	E1 Defframer will no sync in a case of multiple FAS patterns in E1 bit stream	007579

Status: CLOSED

Description:
When Injecting multiple FAS pattern on the ingress bit stream, the E1 ingress framer might not synchronize, and will cause an assertion of PDH LOF alarm.

#	Affected Component	Title	Issue
46.	SW FRAMER	It is not possible to multiplex DS3\E3 with T1\E1 connections on the same optical port in UFE412	007603

Description:
It is not possible to have combinations of E3s with E1s on the same optical port or a similar

#	Affected Component	Title	Issue
47.	HW OTHERS (UFE)	TU-LOP/TU-AIS alarms may get stuck if the port optical signal is toggling in high frequency	007529

Description:
When the port rx optical signal is toggling in high frequency (a change each ~500usec), few low order facilities may be stuck in TU-LOP/TU-AIS mode.