Morteza Baradaran

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Overview

My interests lie broadly in Computer Architecture and Domain Specific Accelerators. I'm interested in exploring novel hardware and software techniques to enhance the performance, energy efficiency, and programmability of domain specific accelerators.

Highlights of my research experience: During my Ph.D., I developed high-performance accelerators and tools for data-intensive workloads, including TriPIM (triangle counting on UPMEM PIM) and PARMIK (fast, memory-efficient genomic aligner). I designed a PIM-enabled architecture to accelerate a hybrid Transformer-CNN model (e.g., SAM2) by addressing memory bottlenecks. I collaborated on PIMeval/PIMbench for PIM simulation and benchmarking, as well as Sangam (chiplet-based PIM for LLM inference).

Education

University of Virginia, Charlottesville, USA — Sep. 2021 - Now
Ph.D., Computer Science (Advisor: Prof. Kevin Skadron) — (GPA: 3.95)

Sharif University of Technology, Tehran, Iran — Sep. 2010 - June 2012
M.Sc., Computer Architecture (Advisor: Prof. H. Sarbazi-Azad)

Shahed University, Tehran, Iran — Sep. 2006 - June 2010
B.Sc., Computer Engineering

Notable Projects

Accelerating Computer Vision Tasks using Processing-in-Memory (**Language:** *C/C++, Python*)
Goal: Accelerating hybrid Transformer-CNN architectures (e.g., SAM2) through Processing-in-Memory techniques.

Sangam: A Chiplet-Based DRAM-PIM Accelerator with CXL Integration for LLM Inferencing (**Language:** *C/C++, Python*)
Goal: Accelerating LLM inferencing through Chiplet-Based Processing-in-Memory techniques.

PARMIK: PArtial Read Matching with Inexpensive K-mers (**Language:** *C/C++, Python*)
Goal: A fast and memory-efficient tool for identifying the "Partial Match" region between two genomic sequences.
Links: GitHub | Paper

PIMeval simulator and PIMbench suite (**Language:** *C/C++, Python*)
Goal: A PIM simulation and benchmark framework.
Links: GitHub | Paper

Swift: A Multi-FPGA Framework for Scaling Up Accelerated Graph Analytics (**Language:** *C/C++, Python*)
Goal: A scalable FPGA-based graph accelerator framework to handle large graphs efficiently.
Links: Paper

TriPIM: Exact Triangle Counting on UPMEM Processing-in-Memory for Graph Analytics (**Language:** *C/C++, Python*)
Goal: Efficient Triangle Counting Powered by Binary Search and In-Memory Processing (UPMEM).
Links: GitHub

ECG: Expressing Locality and Prefetching for Optimal Caching in Graph Structures (**Language:** *C/C++, Python*)
Goal: Enriching graph data with cache optimizations to improve prefetching and replacement policies in graph analytics.
Links: GitHub | Paper

HashMem: PIM-based Hashmap Accelerator (**Language:** *C/C++*)
Goal: A PIM-based Hashmap Accelerator.
Links: GitHub | Paper

Energy Consumption Analysis of Instruction Cache Prefetching (**Language:** *C/C++*, **Framework:** *ChampSim, CACTI-7*)
Goal: Evaluating the energy consumption of instruction cache prefetching techniques.
Links: GitHub | Paper

Banking Integrated Card Personalization System (IPS) (**Language:** *C/C++, Java*)
Goal: A Banking Card Personalization System Capable of Acquiring Customers' data and Personalizing it for Banking Cards.

Automatic Train Control Systems for Metro and Urban Railway (**Language:** *C++*)
Goal: Developing and Analyzing Metro & Urban Railway Signalling and Telecommunication Systems (i.e., ATC, ATP, etc).

Publications

- **M. Baradaran**, K. Kiyawat, A. Shekar, A. T. Mughrabi, and K. Skadron, "TriPIM: Exact Triangle Counting on UPMEM Processing-in-Memory for Graph Analytics," in *International Symposium on Memory Systems (MEMSYS)*, 2025

- K. Kiyawat, Z. Fan, Y. Seneviratne, **M. Baradaran**, A. Shekar, Z. Xia, M. Kang, and K. Skadron, "Sangam: A Chiplet-Based DRAM-PIM Accelerator with CXL Integration for LLM Inferencing," 2025. In submission
- **M. Baradaran**, R. Layer, and K. Skadron, "PARMIK: PArtial Read Matching with Inexpensive K-mers," 2025. Submitted to Bioinformatics
- W. Jaiyeoba, A. T. Mughrabi, **M. Baradaran**, B. Gul, and K. Skadron, "Swift: A Multi-FPGA Framework for Scaling Up Accelerated Graph Analytics," in *International Conference on Field Programmable Technology (FPT)*, 2024
- F. A. Siddique, D. Guo, Z. Fan, M. Gholamrezaei, **M. Baradaran**, A. Ahmed, H. Abbot, K. Durrer, K. Nandagopal, E. Ermovick, K. Kiyawat, B. Gul, A. Mughrabi, A. Venkat, and K. Skadron, "Architectural Modeling and Benchmarking for Digital DRAM PIM," in *International Symposium on Workload Characterization (IISWC)*, 2024
- A. T. Mughrabi, **M. Baradaran**, A. Samara, and K. Skadron, "ECG: Expressing Locality and Prefetching for Optimal Caching in Graph Structures," in *International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, 2024
- **M. Baradaran**, A. Ansari, M. Sadrosadati, and H. Sarbazi-Azad, "Energy Consumption Analysis of Instruction Cache Prefetching," in *International Symposium on Computer Architecture and High Performance Computing Workshops (SBAC-PADW)*, 2023
- A. Shekar, **M. Baradaran**, S. Tajdari, and K. Skadron, "HashMem: PIM-based Hashmap Accelerator," in *International Workshop on Domain-Specific System Architecture at ISCA, Orlando, Florida*, 2023
- **M. Baradaran** and M. Zarei, *Theory of Automata and Machine Language*. National Library of Iran, 2013. Published between 2012-2013

Work Experience

Informatics Services Corp, Tehran, Iran — Sep. 2018 - Aug. 2021
Senior Software Development Engineer: Design and Development of Debit and Credit Card Personalization Systems

TOSAN Group Corp, Tehran, Iran — June 2017 - Apr. 2018
Lead Software Engineer: POS Development for ticketing system of Tehran Metro (QR, contactless cards)

MAHARAN Co, Tehran, Iran — May 2015 - Feb. 2017
Software Engineer: Design & development of Automatic Train Control (ATC) and intermediate block system

National-ID Co, Tehran, Iran — Jul 2012 - Dec. 2013
Hardware Specialist: Smart Card OS Design and Implementation including Memory management, File system, and I/O

Professional Services

The Journal of Supercomputing (JS) - Peer reviewer — 2024-present

International Conference on Computer Design (ICCD) - Peer co-reviewer — 2023

Presentations

TECHCON (presentation) — Sep 2024
Title: TriPIM: Efficient Triangle Counting on PIM Technologies — A Binary Search Approach

Genome Informatics (poster) — Dec 2023
Title: Enhancing pandemic preparedness—A novel partial matching approach for identifying similar genetic material from diverse sources for pathogen surveillance

Teaching Experience

Teaching Assistant, CS3130: Undergraduate Computer Systems & Organization 2 — Fall 2024
University of Virginia

Teaching Assistant, CS4414: Undergraduate Operating System — Fall 2023
University of Virginia

Teaching Assistant, CS4414: Undergraduate Operating System — Fall 2022
University of Virginia

Skills

Programming Languages/APIs: C/C++, CUDA, Java, Python, Verilog, Bash, Assembly

Simulation Tools: Gem5, SniperSim, DRAMsim3, ChampSim, CACTI, Synopsys Design Compiler, UPMEM Functional Sim

Performance & Benchmarking: SPEC/PARSEC Benchmarks, GAP Benchmark, prim-benchmarks, Gunrock, Ligra, InSituBench

References

Three references will be made available upon request.