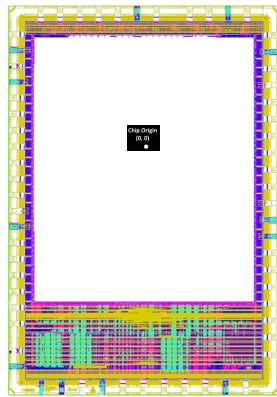
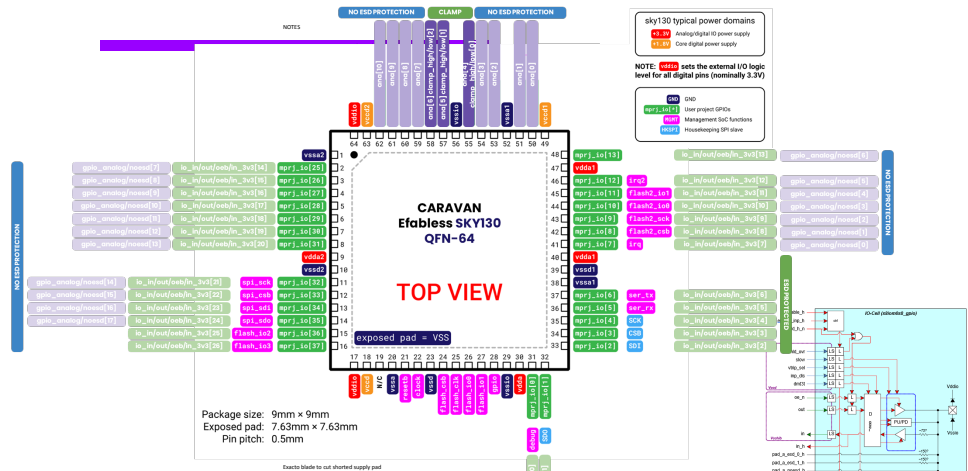
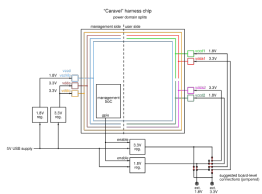


ESD		https://www.gst.com/technical-info/resources/Support%201%20-%20New%20guide.html																	
North																			
Prod Pad	#	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49		
ESD		NO ESD						CLAMP				NO ESD							
Chip Pad	#																		
Pad Choice																			
enables VIO pin				NFC_Ana	NFC_Ana	NFC_Ana	NFC_Ana	NFC_Ana	NFC_Ana			NFC_Ana	NFC_Ana	NFC_Ana			NFC_Ana	Wrapper	
				mpr1_n[24]	mpr1_n[25]	mpr1_n[22]	mpr1_n[21]	mpr1_n[20]	mpr1_n[19]			mpr1_n[18]	mpr1_n[17]	mpr1_n[16]			mpr1_n[15]	mpr1_n[14]	
pin type				Analog (in)	Analog (in)	Analog (in)	Analog (in)	Analog (in)	Analog (in)			Analog (in)	Analog (in)	Analog (in)			Analog (in)	Analog (in)	
										Clamp High		Clamp High							
										Clamp Low		Clamp Low							
												No							
												No							
conversion pin name		noconv	noconv	no_conv[0]	no_conv[1]	no_conv[2]	no_conv[3]	no_conv[4]	no_conv[5]	noconv	no_conv[6]	no_conv[7]	no_conv[8]	noconv	no_conv[9]	no_conv[10]	noconv		
Clamp High										clamp_high[0]		clamp_high[1]							
Clamp Low										clamp_low[0]		clamp_low[1]							
NFC Use				NFC_Ana_TSD_EXT (DEMOD_ENA_MTXL...)	ANA_MUX_OUT_2_EXT	FS_EXT	MSST_EXT	VBSST_EXT	VSD_EXT	noconv	VBSST_OUT_EXT	AMT_FDS_EXT	AMT_MIS_EXT			ANA_MUX_OUT_EXT			
Wrapper Use																		clock_source	
enables aux																			
signal choice		noconv	noconv	TSD_EXT (DEMOD_ENA...)	ANA_MUX_OUT_2_EXT	FS_EXT	MSST_EXT	VBSST_EXT	VSD_EXT	noconv	VBSST_OUT_EXT	AMT_FDS_EXT	AMT_MIS_EXT	noconv	ANA_MUX_OUT_EXT	clock_source	noconv		
Coordination	X																		
	Y																		

[illegible][illegible]

Pin	ESD	Chip Pin	Pin Description	relatives I/O pin	pin type	current pin name	IOs	MCU type	Wrapper I/O	relatives aux	ESD device	Coordination	
46	NO ESD RESISTOR - ESD DIODES ONLY		NFC-Dig	mpr1_mn1[1]	GPIOD (out 3v3)	ts_mn0[11]	ts_mn0[11]	tsm2		tsm2	X	Y	ESD
47													
46		Wrapper	mpr1_mn1[12]	GPIOD (inout 1v8)	ts_mn0[12]	ts_mn0[12]	ts_mn0_1	tsm2	tsm2_1				
45		Wrapper	mpr1_mn1[11]	GPIOD (inout 1v8)	ts_mn0[11]	ts_mn0[11]	ts_mn0_0	tsm2_0	tsm2_0				
44		Wrapper	mpr1_mn1[10]	GPIOD (inout 1v8)	ts_mn0[10]	ts_mn0[10]	tsm1_1	tsm2_1	tsm2_1				
43		Wrapper	mpr1_mn0[9]	GPIOD (inout 1v8)	ts_mn0[9]	ts_mn0[9]	tsm1_0	tsm2_0	tsm2_0				
42		Wrapper	mpr1_mn0[8]	GPIOD (inout 1v8)	ts_mn0[8]	ts_mn0[8]	tsm1_0	tsm2_0	tsm2_0				
41		Wrapper	mpr1_mn0[7]	GPIOD (out 3v3)	ts_mn0[7]	ts_mn0[7]	tsm1_0	tsm2_0					
40	ESD RESISTOR ("150ohm" + ESD DIODE)												ESD
39													
38													
37		Wrapper	mpr1_mn0[6]	GPIOD (out 3v3)	ts_mn0[6]	ts_mn0[6]	tsm1_mn_0	tsm1_mn_0					
36		Wrapper	mpr1_mn0[5]	GPIOD (inout 1v8)	ts_mn0[5]	ts_mn0[5]	tsm1_mn_0	tsm1_mn_0					
35		Wrapper	mpr1_mn0[4]	GPIOD (inout 1v8)	ts_mn0[4]	ts_mn0[4]	tsm1_mn_1	tsm1_mn_1					
34		Wrapper	mpr1_mn0[3]	GPIOD (out 3v3)	ts_mn0[3]	ts_mn0[3]	tsm1_TSD	tsm1_TSD					
33		Wrapper	mpr1_mn0[2]	GPIOD (in 1v8)	ts_mn0[2]	ts_mn0[2]	tsm1_TSD	tsm1_TSD					



Please put chip layout data showing top metal layers.

