DISCRETE SEMICONDUCTORS

DATA SHEET

BFM520Dual NPN wideband transistor

Product specification Supersedes data of 1995 Sep 04 File under Discrete Semiconductors, SC14





Dual NPN wideband transistor

BFM520

FEATURES

- · Small size
- Temperature and h_{FE} matched
- · Low noise and high gain
- High gain at low current and low capacitance at low voltage
- Gold metallization ensures excellent reliability.

APPLICATIONS

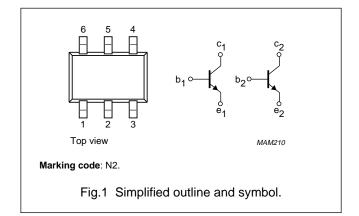
- · Oscillator and buffer amplifiers
- · Balanced amplifiers
- LNA/mixers.

DESCRIPTION

Dual transistor with two silicon NPN RF dies in a surface mount 6-pin SOT363 (S-mini) package. The transistor is primarily intended for wideband applications in the GHz-range in the RF front end of analog and digital cellular phones, cordless phones, radar detectors, pagers and satellite TV-tuners.

PINNING - SOT363A

| PIN | SYMBOL | DESCRIPTION |
|-----|----------------|-------------|
| 1 | b ₁ | base 1 |
| 2 | e ₁ | emitter 1 |
| 3 | c ₂ | collector 2 |
| 4 | b ₂ | base 2 |
| 5 | e ₂ | emitter 2 |
| 6 | C ₁ | collector 1 |



QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
|-------------------------|----------------------------------|---|------|------|------|------|--|
| Any single | Any single transistor | | | | | | |
| C _{re} | feedback capacitance | I _e = 0; V _{CB} = 3 V; f = 1 MHz | _ | 0.4 | _ | pF | |
| f _T | transition frequency | $I_C = 20 \text{ mA}; V_{CE} = 3 \text{ V}; f = 900 \text{ MHz}$ | _ | 9 | _ | GHz | |
| $\left s_{21}\right ^2$ | insertion power gain | I_{C} = 20 mA; V_{CE} = 3 V; f = 900 MHz; T_{amb} = 25 °C | 13 | 14.5 | _ | dB | |
| G _{UM} | maximum unilateral power gain | I _C = 20 mA; V _{CE} = 3 V; f = 900 MHz; T _{amb} = 25 °C | _ | 15 | _ | dB | |
| F | noise figure | $I_C = 5 \text{ mA}; V_{CE} = 3 \text{ V};$ $f = 900 \text{ MHz}; \Gamma_S = \Gamma_{opt}$ | _ | 1.2 | 1.6 | dB | |
| R _{th j-s} | thermal resistance from junction | single loaded | _ | _ | 230 | K/W | |
| | to soldering point | double loaded | _ | _ | 115 | K/W | |

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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT | |
|------------------|---------------------------|---------------------------------------|------|------|------|--|
| Any single | Any single transistor | | | | | |
| V _{CBO} | collector-base voltage | open emitter | _ | 20 | V | |
| V _{CEO} | collector-emitter voltage | open base | _ | 8 | V | |
| V _{EBO} | emitter-base voltage | open collector | _ | 2.5 | V | |
| I _C | DC collector current | | _ | 70 | mA | |
| P _{tot} | total power dissipation | up to T _s = 118 °C; note 1 | _ | 1 | W | |
| T _{stg} | storage temperature | | -65 | +175 | °C | |
| Tj | junction temperature | | _ | 175 | °C | |

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---------------------|----------------------------------|---------------|-------|------|
| R _{th j-s} | thermal resistance from junction | single loaded | 230 | K/W |
| | to soldering point; note 1 | double loaded | 115 | K/W |

Note to the Limiting values and Thermal characteristics

1. T_s is the temperature at the soldering point of the collector pin.

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CHARACTERISTICS

 $T_j = 25$ °C unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------------------|---|--|------|------|------|------|
| DC charac | DC characteristics of any single transistor | | | | | |
| V _{(BR)CBO} | collector-base breakdown voltage | $I_C = 2.5 \mu\text{A}; I_E = 0$ | 20 | _ | _ | V |
| V _{(BR)CEO} | collector-emitter breakdown voltage | $I_C = 10 \mu A; I_B = 0$ | 8 | _ | _ | V |
| V _{(BR)EBO} | emitter-base breakdown voltage | $I_E = 2.5 \mu\text{A}; I_C = 0$ | 2.5 | _ | _ | V |
| I _{CBO} | collector-base leakage current | V _{CB} = 6 V; I _E = 0 | _ | _ | 50 | nA |
| h _{FE} | DC current gain | $I_C = 20 \text{ mA}; V_{CE} = 6 \text{ V}$ | 60 | 120 | 250 | |
| DC charac | teristics of the dual transistor | | | | | |
| Δh_{FE} | ratio of highest and lowest DC current gain | $I_{C1} = I_{C2} = 20 \text{ mA};$ $V_{CE1} = V_{CE2} = 6 \text{ V}$ | 1 | 1.2 | _ | |
| ΔV_{BEO} | difference between highest and lowest base-emitter voltage (offset voltage) | $I_{E1} = I_{E2} = 30 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$ | 0 | 1 | _ | mV |
| AC charac | teristics of any single transistor | | | | | |
| f _T | transition frequency | $I_C = 20 \text{ mA}; V_{CE} = 3 \text{ V}; f = 1 \text{ GHz}$ | _ | 9 | _ | GHz |
| C _c | collector capacitance | $I_E = i_e = 0$; $V_{CB} = 3 \text{ V}$; $f = 1 \text{ MHz}$ | _ | 0.5 | _ | pF |
| C _{re} | feedback capacitance | $I_C = 0$; $V_{CB} = 3 \text{ V}$; $f = 1 \text{ MHz}$ | _ | 0.4 | _ | pF |
| G _{UM} | maximum unilateral power gain; note 1 | $I_C = 20 \text{ mA}; V_{CE} = 3 \text{ V};$ $T_{amb} = 25 ^{\circ}C; f = 900 \text{ MHz}$ | - | 15 | - | dB |
| | | $I_C = 20 \text{ mA}; V_{CE} = 3 \text{ V};$ $T_{amb} = 25 ^{\circ}\text{C}; f = 2 \text{ GHz}$ | - | 9 | - | dB |
| s ₂₁ ² | insertion power gain | $I_C = 20 \text{ mA}; V_{CE} = 3 \text{ V};$ f = 900 MHz; $T_{amb} = 25 ^{\circ}\text{C}$ | 13 | 14.5 | _ | dB |
| F | noise figure | I_C = 5 mA; V_{CE} = 3 V; f = 900 MHz; Γ_S = Γ_{opt} | _ | 1.2 | 1.6 | dB |
| | | I_C = 20 mA; V_{CE} = 3 V; f = 900 MHz; Γ_S = Γ_{opt} | _ | 1.7 | 2.1 | dB |
| | | $I_C = 5 \text{ mA}; V_{CE} = 3 \text{ V};$ $f = 2 \text{ GHz}; \Gamma_S = \Gamma_{opt}$ | - | 1.9 | - | dB |

Note

Note $\text{1. } G_{UM} \text{ is the maximum unilateral power gain, assuming } s_{12} \text{ is zero. } G_{UM} = 10 \log \frac{\left|s_{21}\right|^2}{(1-\left|s_{11}\right|^2) \; (1-\left|s_{22}\right|^2)} \; \text{dB}$

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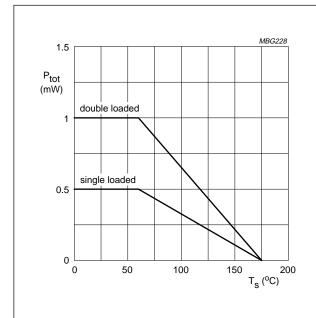


Fig.2 Power derating as a function of soldering point temperature; typical values.

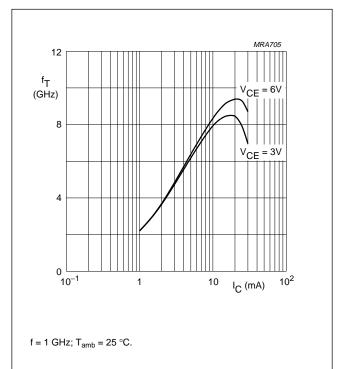


Fig.3 Transition frequency as a function of collector current; typical values.

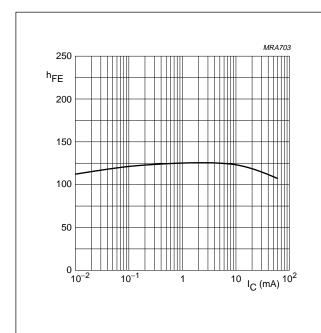
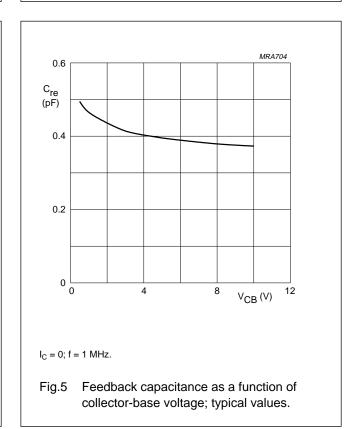


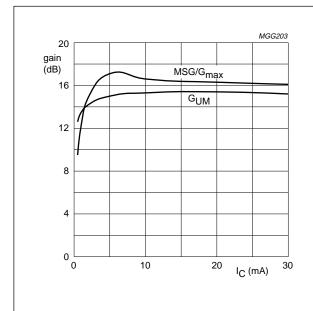
Fig.4 DC current gain as a function of collector current; typical values.

 $V_{CE} = 6 V.$



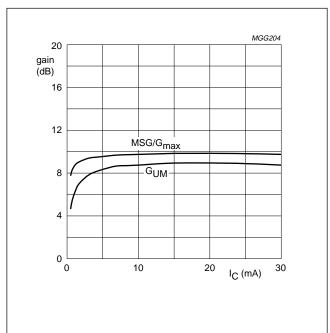
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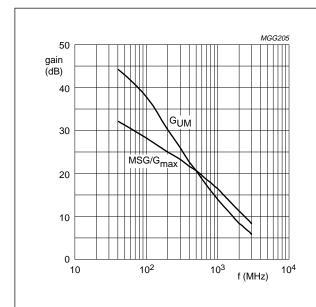
f = 900 MHz; V_{CE} = 3 V.

Fig.6 Gain as a function of collector current; typical values.



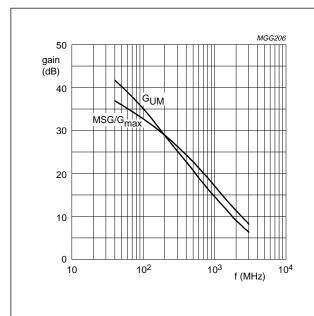
 $f = 2 GHz; V_{CE} = 3 V.$

Fig.7 Gain as a function of collector current; typical values.



 I_C = 5 mA; V_{CE} = 3 V.

Fig.8 Gain as a function of frequency; typical values.



 I_C = 20 mA; V_{CE} = 3 V.

Fig.9 Gain as a function of frequency; typical values.

 G_{ass}

15

10

Dual NPN wideband transistor

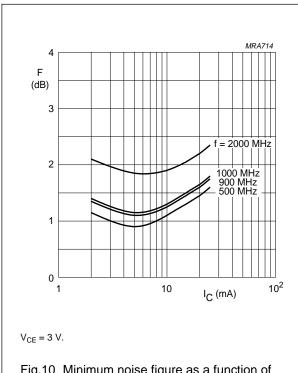
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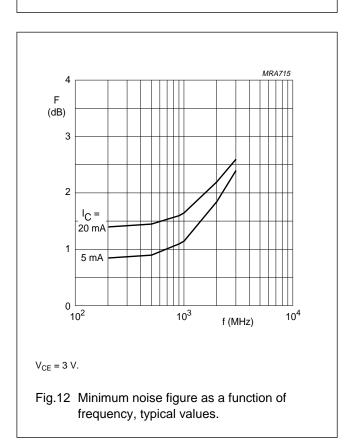
1000 MHz

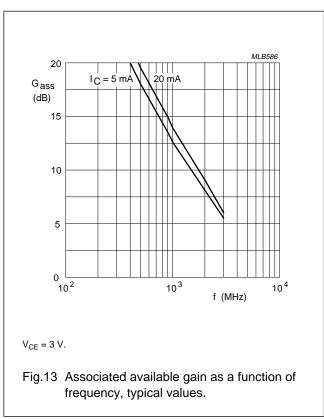
2000 MHz

10²



5 0 I_C (mA) $V_{CE} = 3 V.$ Fig.10 Minimum noise figure as a function of Fig.11 Associated available gain as a function of collector current, typical values. collector current, typical values.





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APPLICATION INFORMATION

SPICE parameters for any single BFM520 die

| SEQUENCE No. | PARAMETER | VALUE | UNIT |
|-------------------|-----------|-------|------|
| 1 | IS | 1.016 | fA |
| 2 | BF | 220.1 | _ |
| 3 | NF | 1.000 | _ |
| 4 | VAF | 48.06 | V |
| 5 | IKF | 510.0 | mA |
| 6 | ISE | 283.0 | fA |
| 7 | NE | 2.035 | _ |
| 8 | BR | 100.7 | _ |
| 9 | NR | 0.988 | _ |
| 10 | VAR | 1.692 | V |
| 11 | IKR | 2.352 | mA |
| 12 | ISC | 24.48 | аА |
| 13 | NC | 1.022 | _ |
| 14 | RB | 10.00 | Ω |
| 15 | IRB | 1.000 | μΑ |
| 16 | RBM | 10.00 | Ω |
| 17 | RE | 0.775 | Ω |
| 18 | RC | 2.210 | Ω |
| 19 ⁽¹⁾ | XTB | 0.000 | _ |
| 20 ⁽¹⁾ | EG | 1.110 | eV |
| 21 ⁽¹⁾ | XTI | 3.000 | _ |
| 22 | CJE | 1.245 | pF |
| 23 | VJE | 600.0 | mV |
| 24 | MJE | 0.258 | _ |
| 25 | TF | 8.616 | ps |
| 26 | XTF | 6.788 | _ |
| 27 | VTF | 1.414 | V |
| 28 | ITF | 110.3 | mA |
| 29 | PTF | 45.01 | deg |
| 30 | CJC | 447.6 | fF |
| 31 | VJC | 189.2 | mV |
| 32 | MJC | 0.071 | _ |
| 33 | XCJC | 0.130 | _ |
| 34 | TR | 543.7 | ps |
| 35 ⁽¹⁾ | CJS | 0.000 | F |
| 36 ⁽¹⁾ | VJS | 750.0 | mV |
| 37 ⁽¹⁾ | MJS | 0.000 | _ |
| 38 | FC | 0.780 | _ |

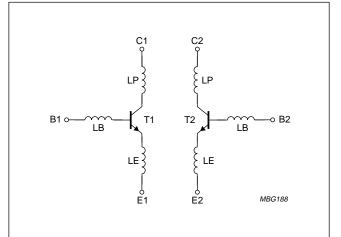
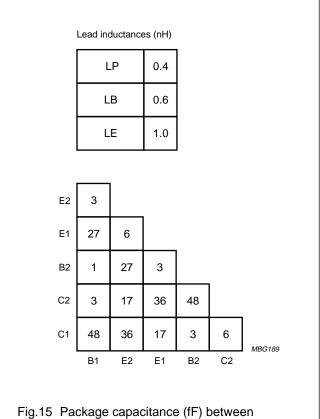


Fig.14 Package equivalent circuit SOT363A (inductance only).



000 – indicated nodes.

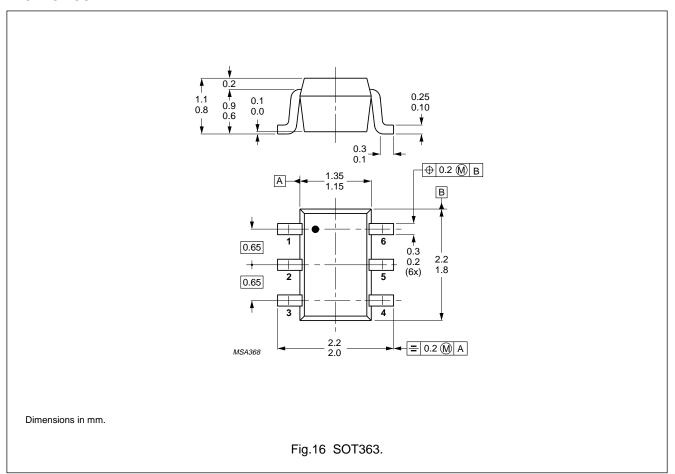
Note

1. These parameters have not been extracted, the default values are shown.

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PACKAGE OUTLINE



Product specification Philips Semiconductors

Dual NPN wideband transistor

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DEFINITIONS

| Data sheet status | | | | |
|---|--|--|--|--|
| Objective specification This data sheet contains target or goal specifications for product development. | | | | |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. | | | |
| Product specification | This data sheet contains final product specifications. | | | |
| Short-form specification | The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook. | | | |
| Limiting values | | | | |

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.