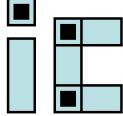


MOSbius – Tutorial

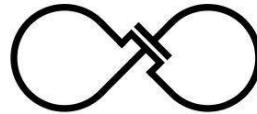
Peter Kinget

Analog & RF  Design Research

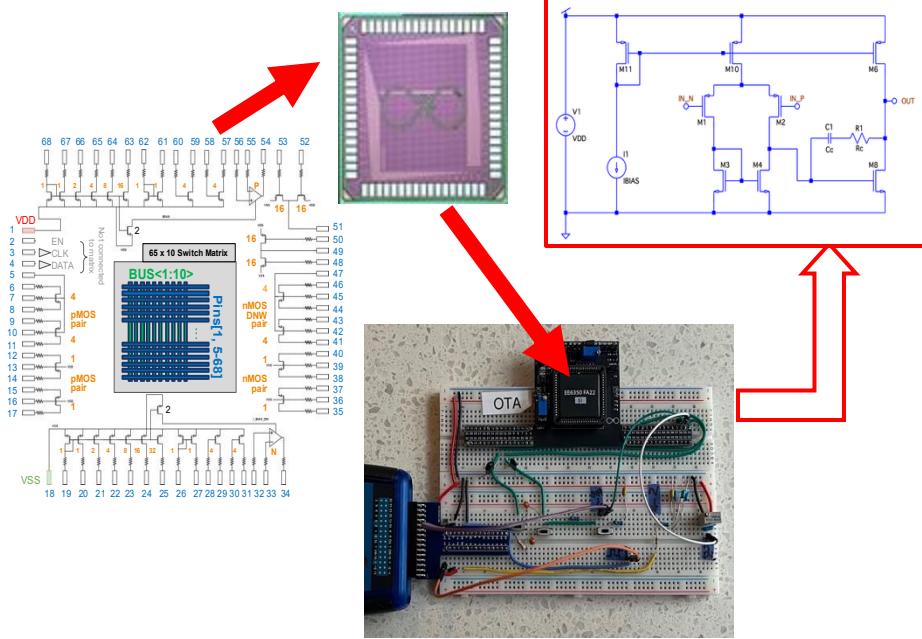
Columbia Integrated Systems Laboratory



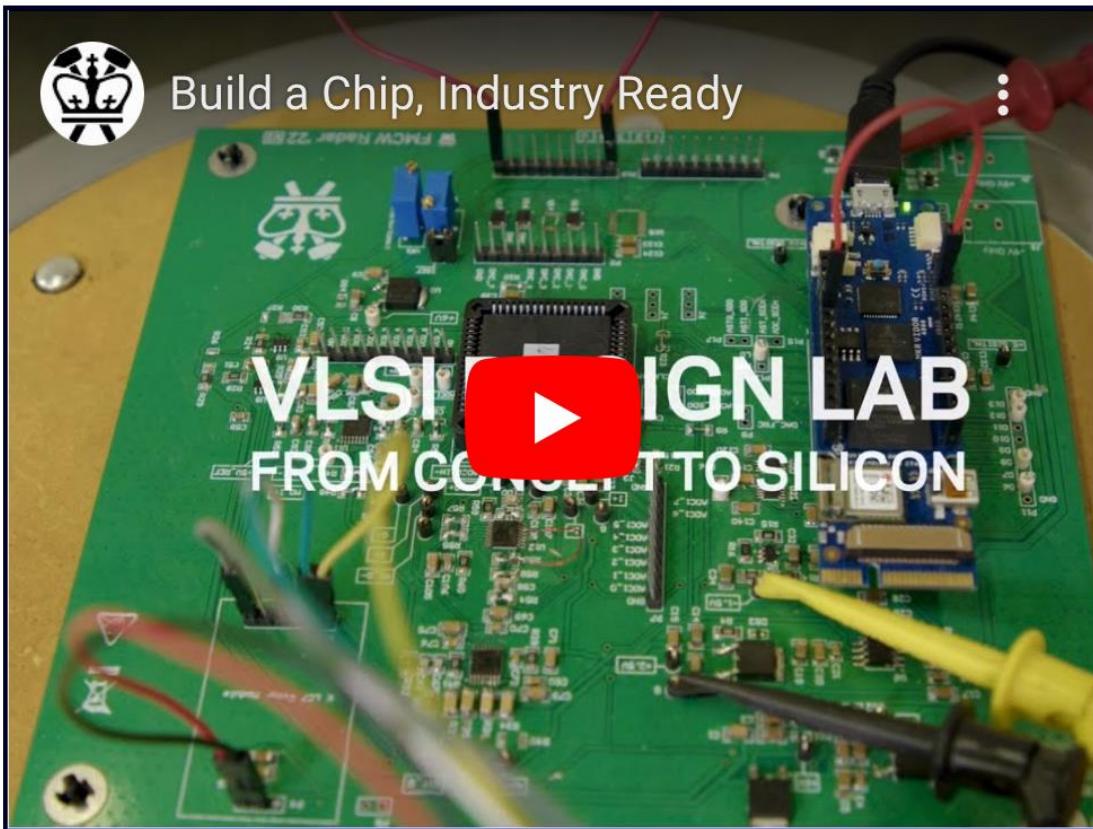
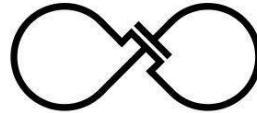
<http://www.cisl.columbia.edu>



MOSbius Track

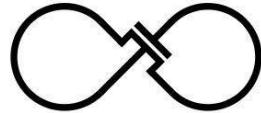


<https://sscs.ieee.org/technical-committees/tc-ose/sscs-pico-design-contest/>



Many detailed chip designs: Class-D Amplifiers, PPGs, ECG, Sensor I/Fs, AM Receiver, WWVB Atomic Clock, FM Receiver, SAR ADCs, Digital Clocks, FPGA, RISC-V Processor, NPU, Ultrasonic Rangers, ...

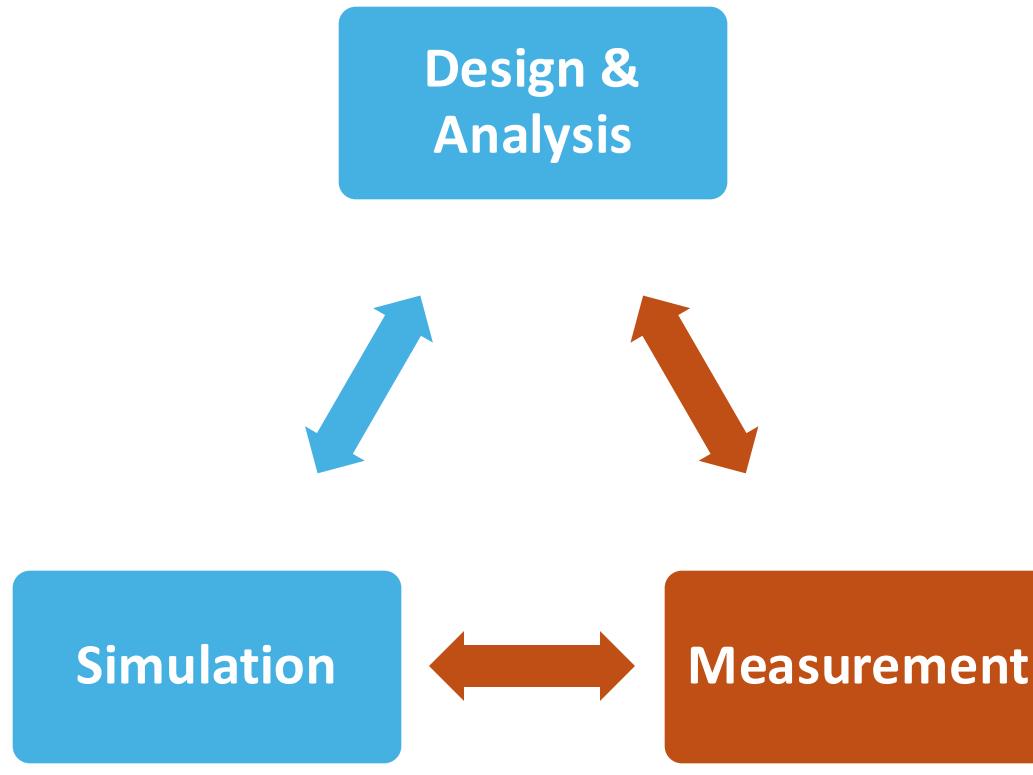
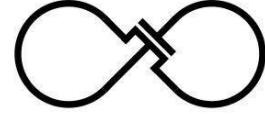
MOSbius Mission



Make it easy for learners to experiment with CMOS
transistors in circuits **relevant to IC design**

<https://mosbius.org>

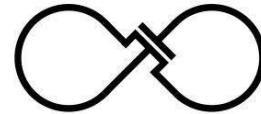
Motivation: Learning IC Design



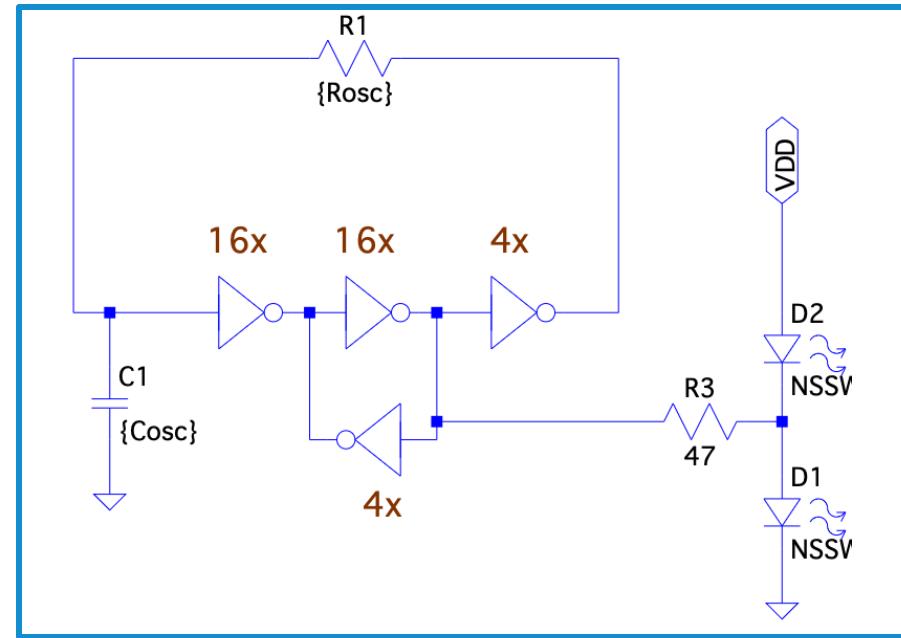
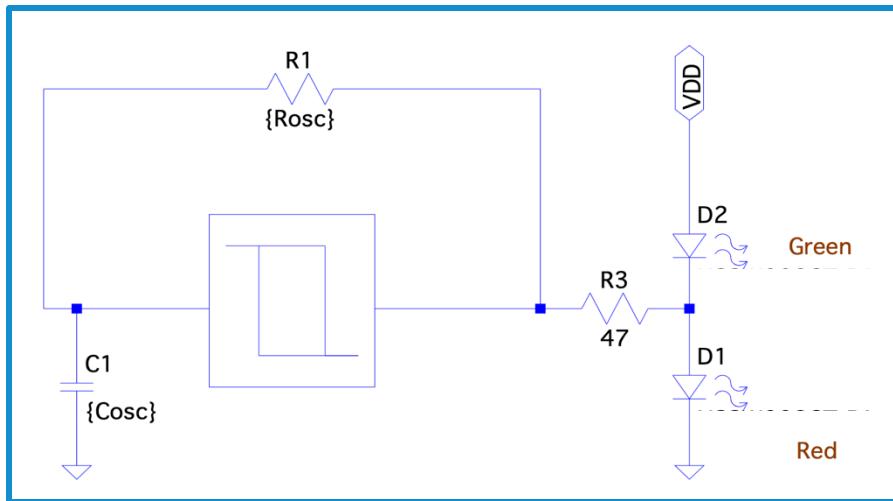
Simulators only answer the
questions you ask them ...
What questions should you be
asking?

Silicon does what *it* wants to do, not
always what **you** want it to do ...

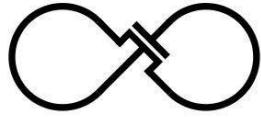
A First Example: Blinky



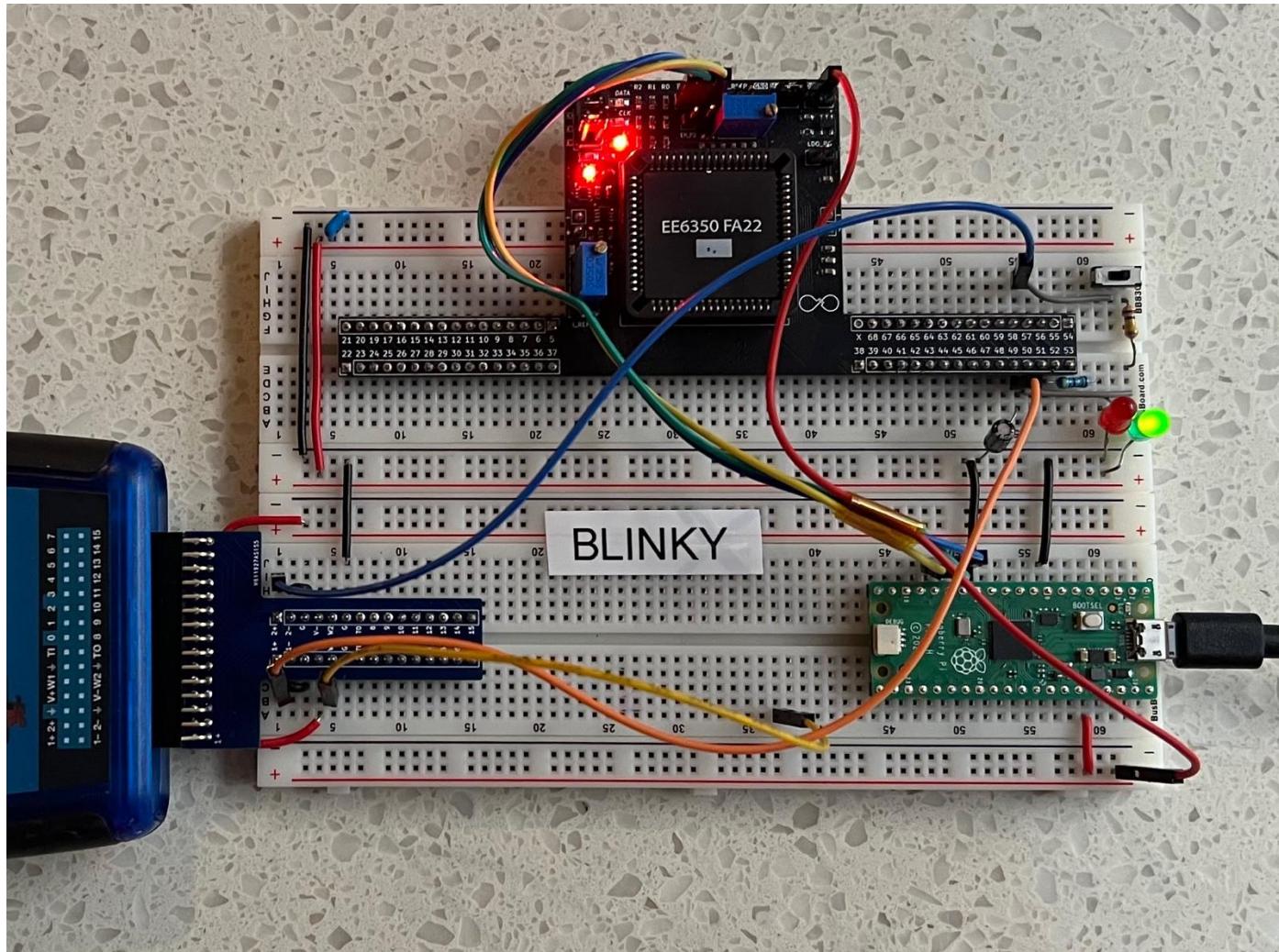
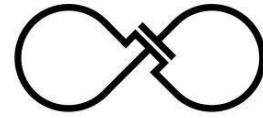
Schmitt-Trigger based Relaxation Oscillator



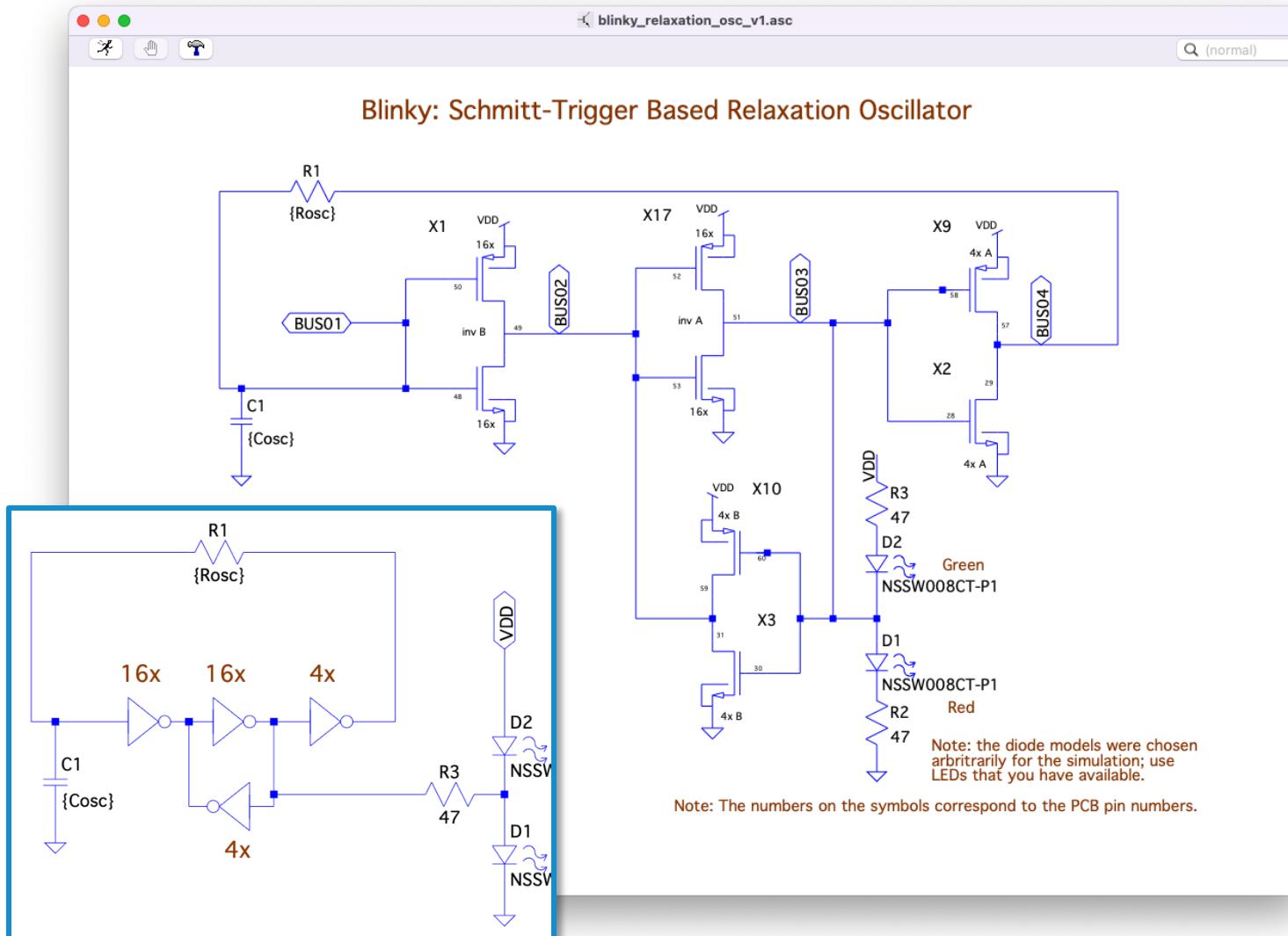
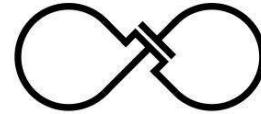
Positive Feedback → Hysteresis



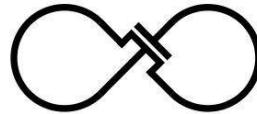
A demo is worth a thousand words



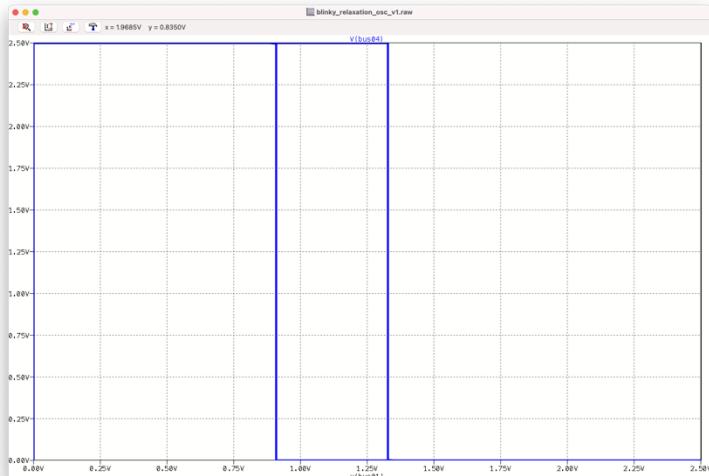
Blinky Spice Schematic



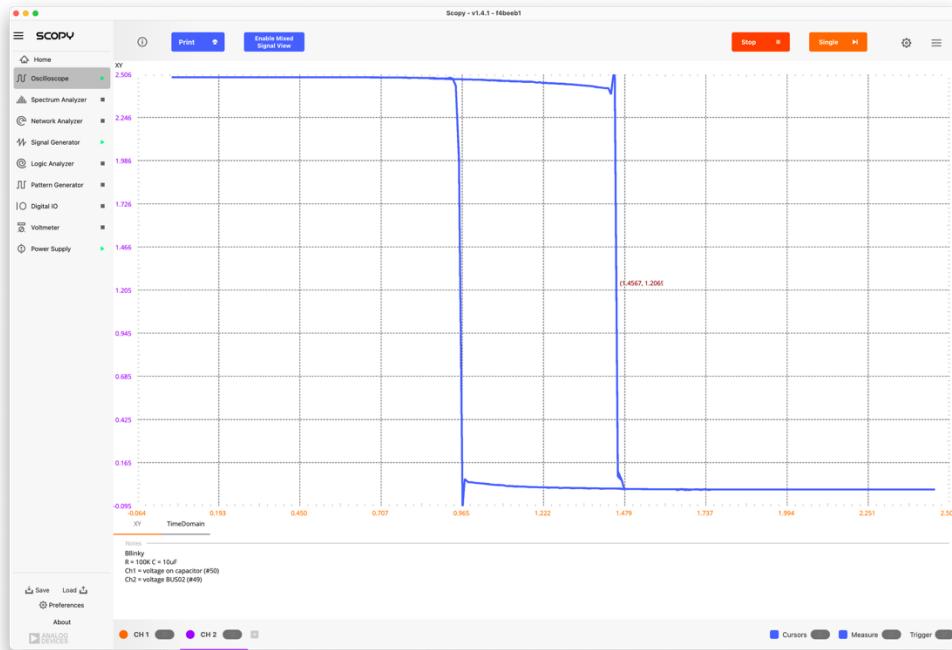
Blinky Schmitt Trigger Simulation



Simulation



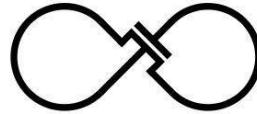
Measurement



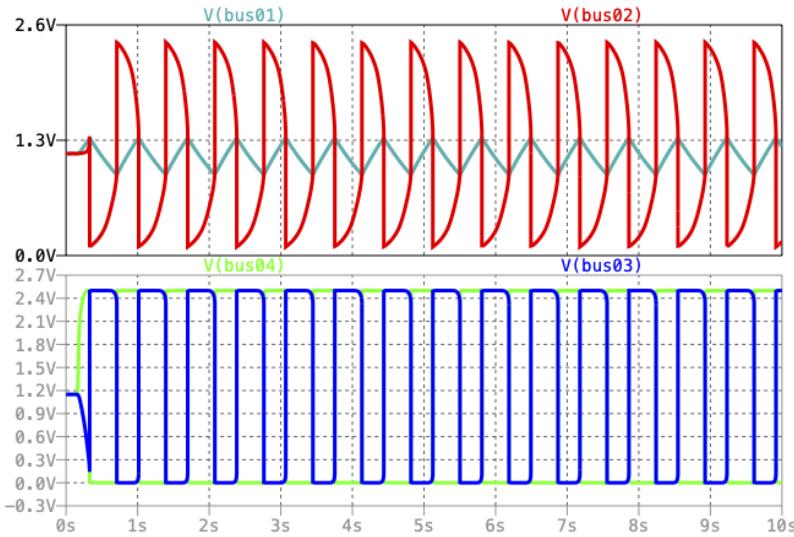
$$\Delta V = 418mV$$

$$\Delta V = 505mV$$

Blinky



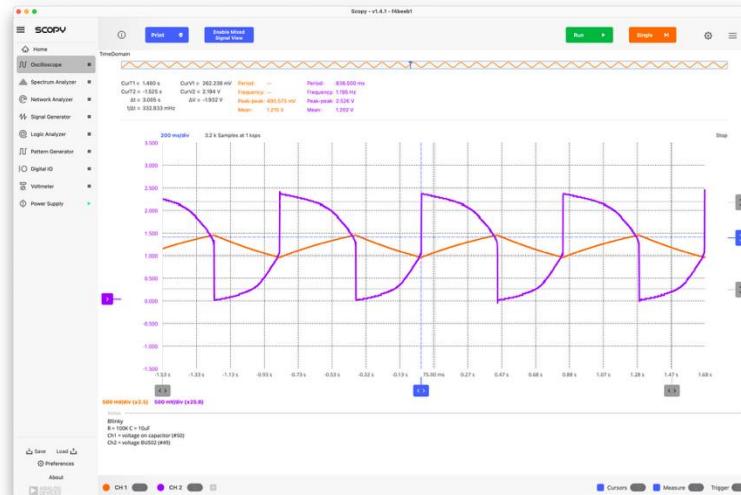
Simulation



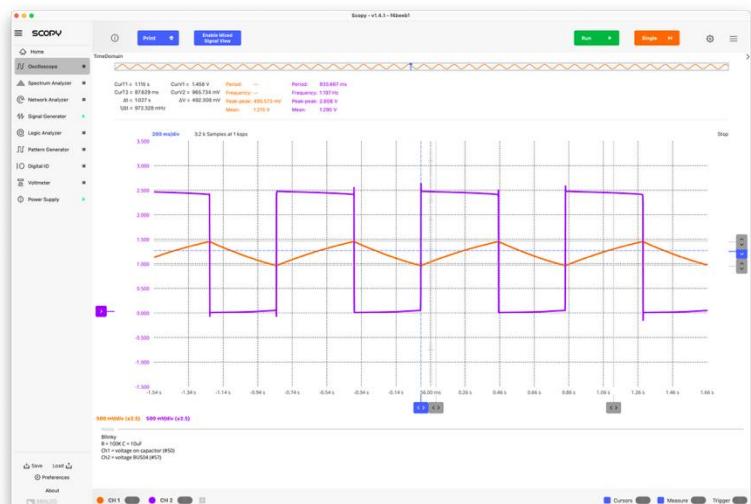
$$\Delta V = 0.411 \text{ V}$$

$$T = 682 \text{ ms}$$

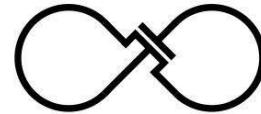
Measurement



$$\Delta V = 0.496 \text{ V}$$
$$T = 837 \text{ ms}$$



Blinky



$$C \frac{\Delta V}{\Delta T} = I_{ch} \approx \frac{V_{DD} - V(BUS01)_{avg}}{R}$$
$$\Delta T \approx RC \frac{\Delta V}{V_{DD} - V(BUS01)_{avg}}$$

$$\Delta V = 0.5 \text{ V} \Rightarrow \Delta T \approx 400 \text{ ms}$$

$$T = 2\Delta T = 800 \text{ ms}$$

Design & Analysis

$$\Delta V = 0.411 \text{ V}$$
$$T = 682 \text{ ms}$$

Simulation

Measurement

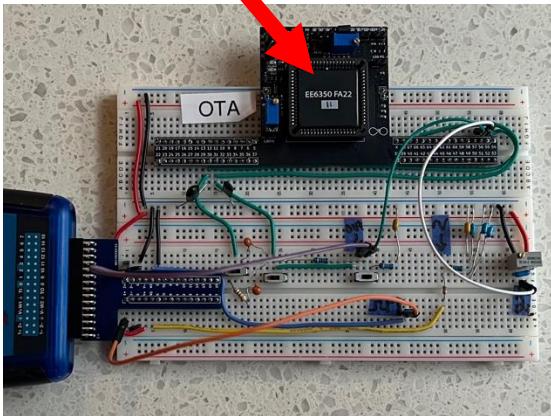
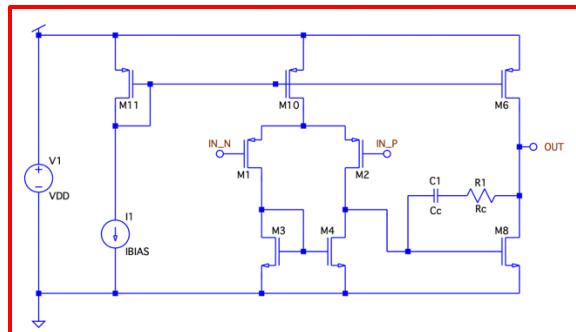
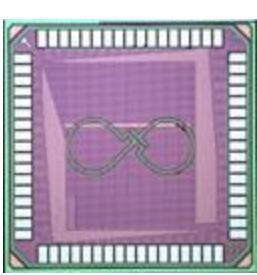
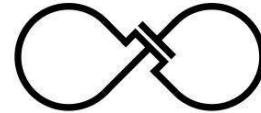
Note:

$$682 \times \frac{496}{411} = 823$$

$$\Delta V = 0.496 \text{ V}$$
$$T = 837 \text{ ms}$$

Main difference in ΔV due to device modeling inaccuracies
in public model card

What is MOSbius, so far?

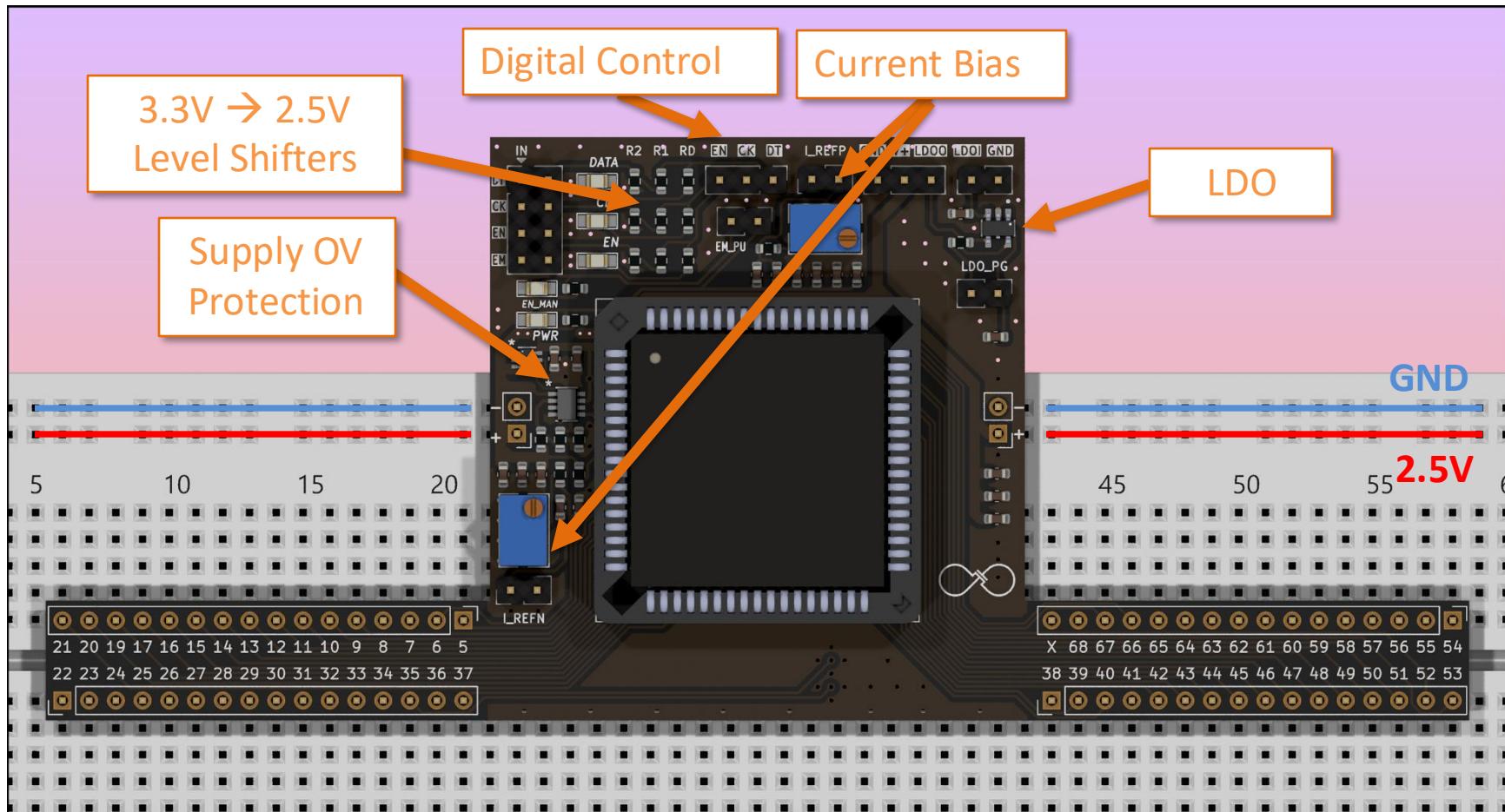
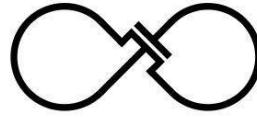


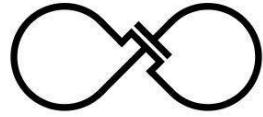
Current version: focus
on transistor-level
analog design

- Website
- Programming support
- Simulation support

<https://mosbius.org>

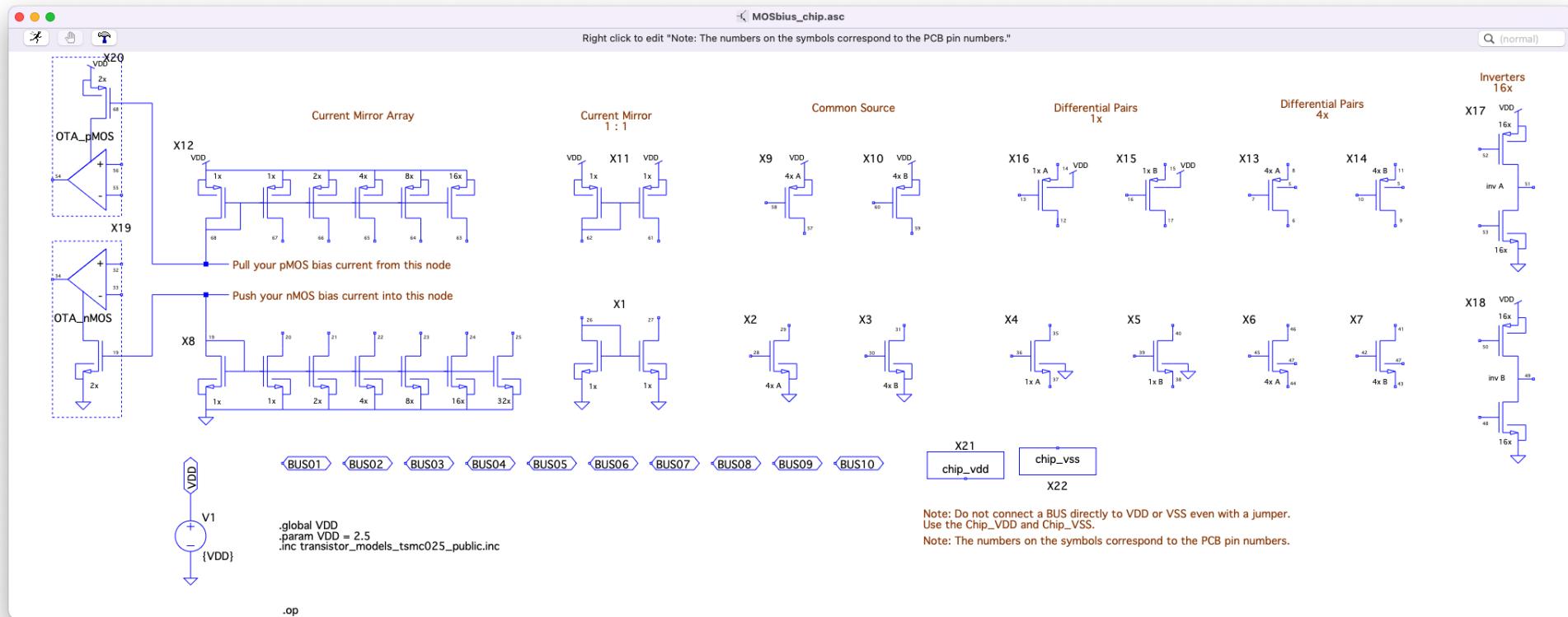
Breadboard Adapter PCB





Spice Simulations

- Custom LTspice Symbol Library

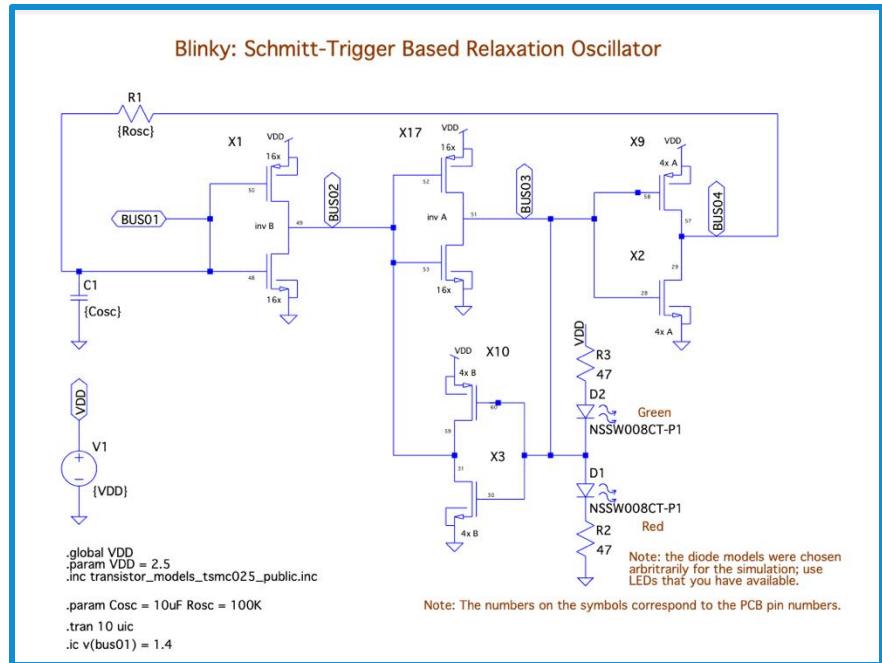


- Public domain BSIM3 transistor model card
- Can easily be ported to ngspice, commercial simulators, ...

MOSbiusTools



Schematic

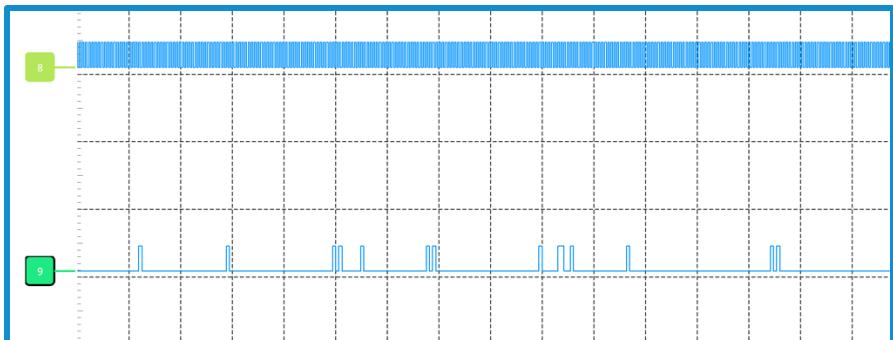


connections.json

```
{ "1": [48, 50],  
  "2": [31, 49, 52, 53, 59],  
  "3": [28, 30, 51, 58, 60],  
  "4": [29, 57] }
```

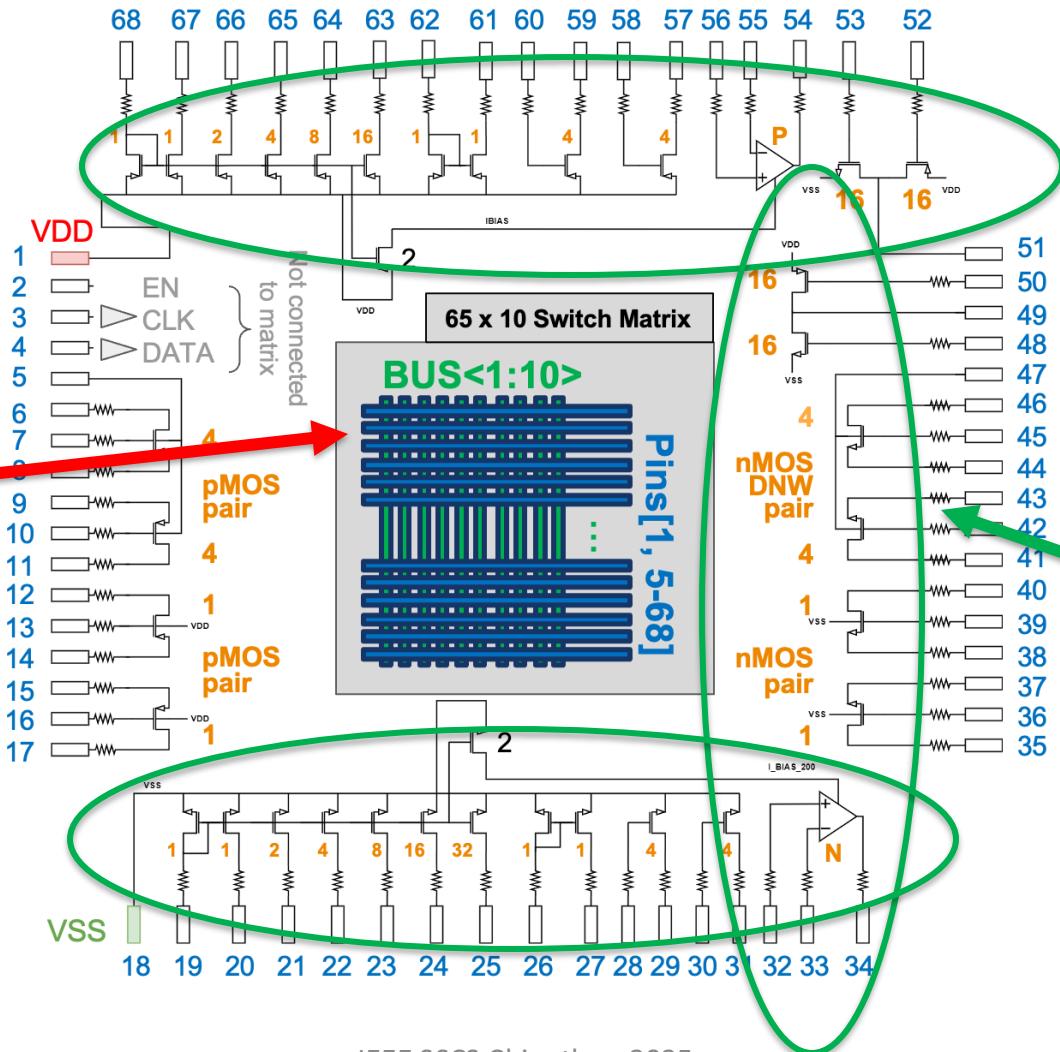
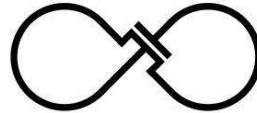


Bitstream

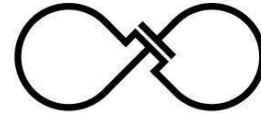


```
pip3 install -i https://test.pypi.org/simple MOSbiusTools
```

What is MOSbius, so far?



MOSbius in the Classroom



- Fall 2024:
 - ***ELEN E4312 Analog Electronic Circuits***
 - 92 students (seniors/1st year graduate students)
- Six labs

[3.1.1. Lab 1: Basic Measurements](#)

[3.1.2. Lab 2: Current Mirrors](#)

[3.1.3. Lab 3: Differential Pair DC Response](#)

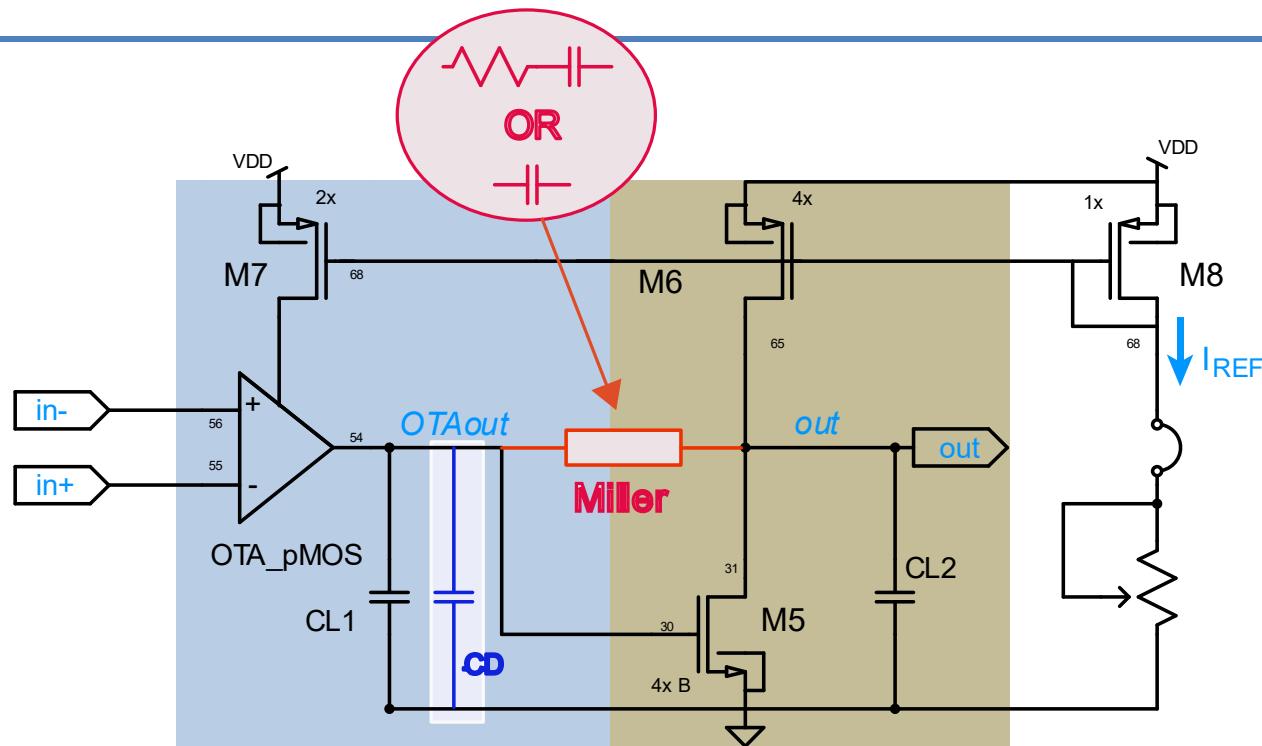
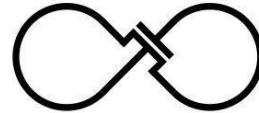
[3.1.4. Lab 4: Differential Pair AC Response](#)

[3.1.5. Lab 5: One-stage OTA and Common-Source Amplifier](#)

[3.1.6. Lab 6: Frequency Compensation of a Two-Stage OTA](#)

Enthusiastic feedback from the students!!

Lab 6: Compensate Two-Stage OTA

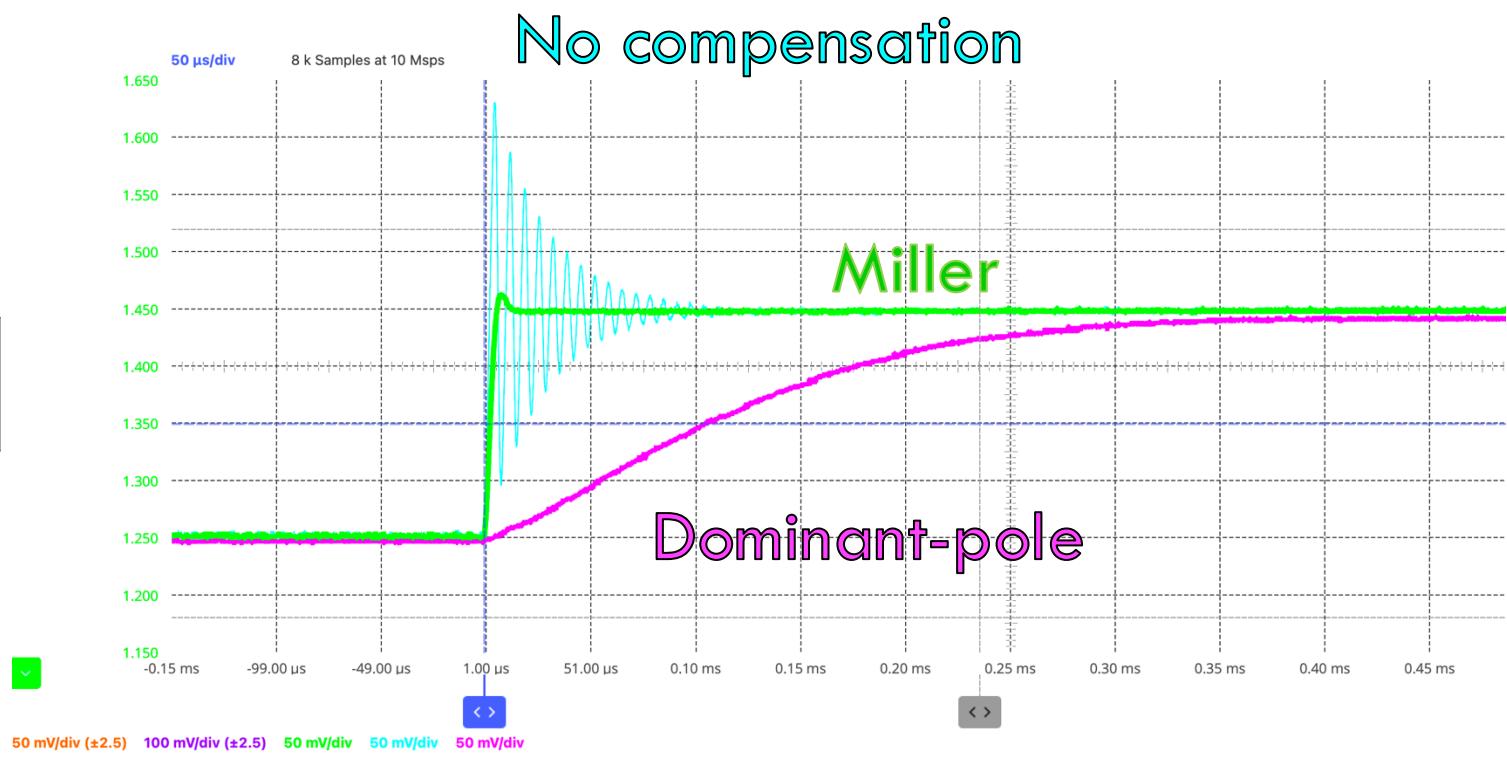
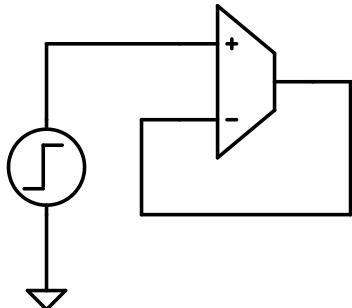
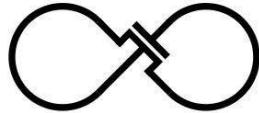


Dominant-Pole Compensation CD

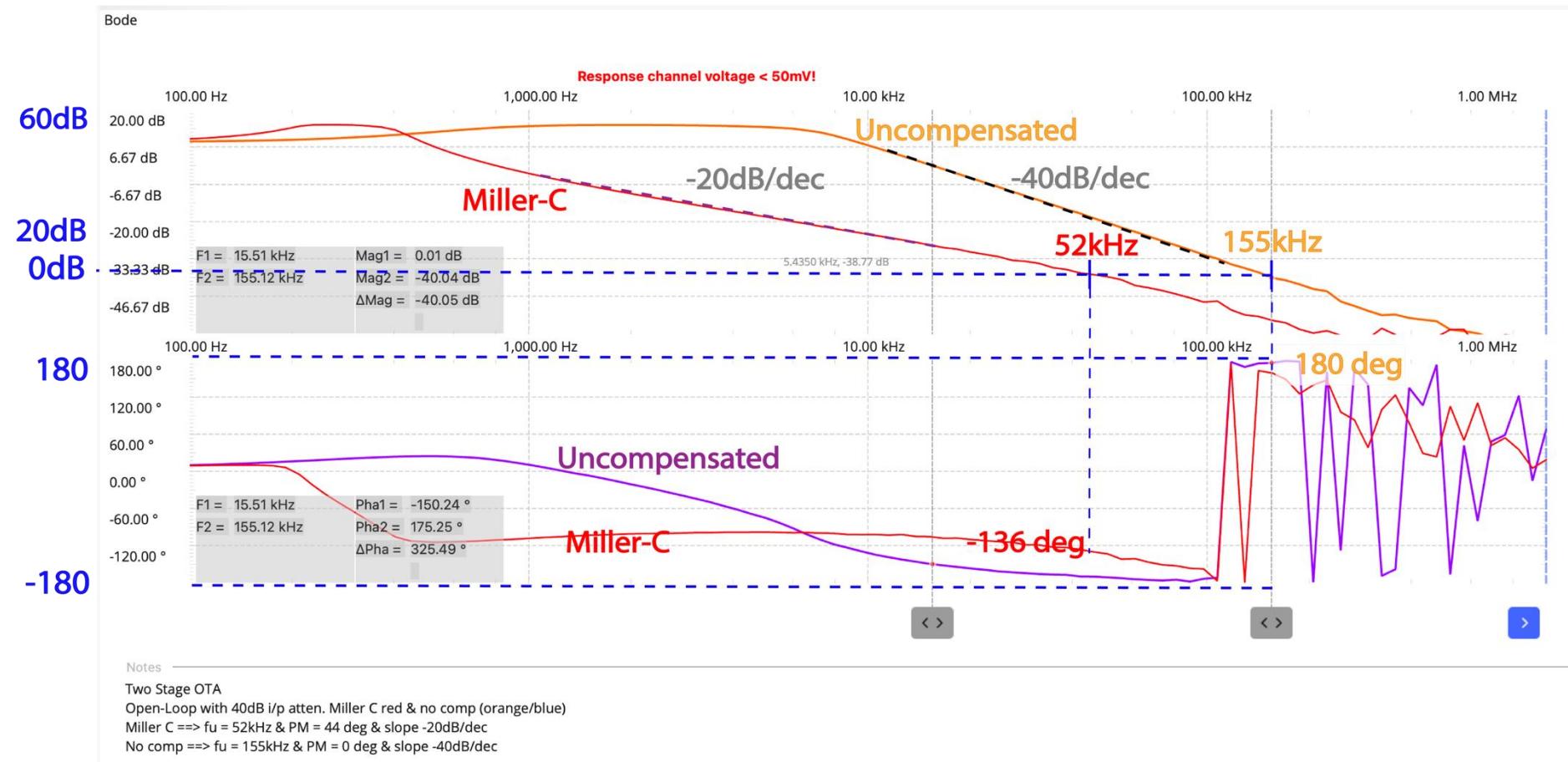
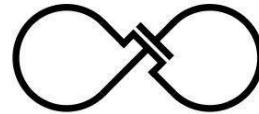
OR

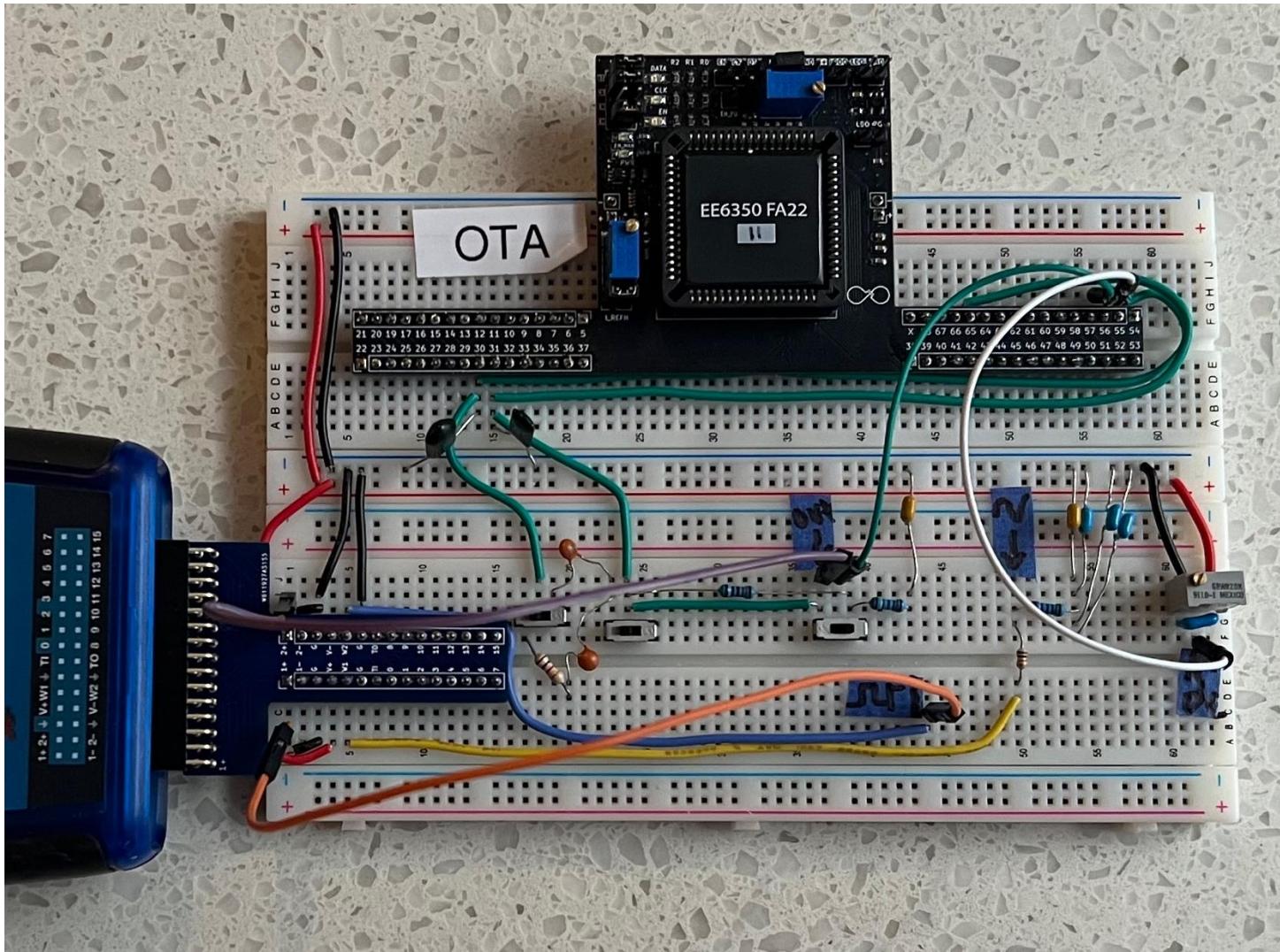
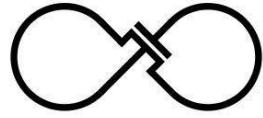
Miller Compensation: C_C & $R_C - C_C$

Unity-Gain Step Response

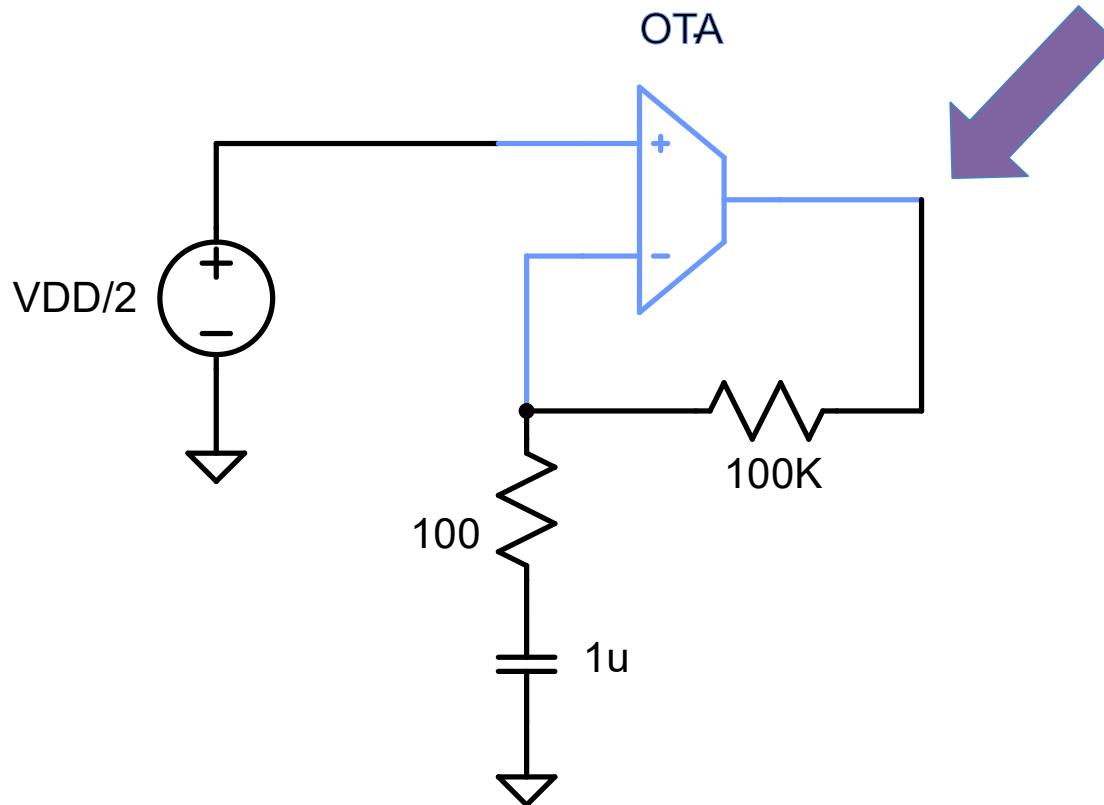
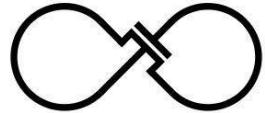


Loop Response: No C vs Miller-C

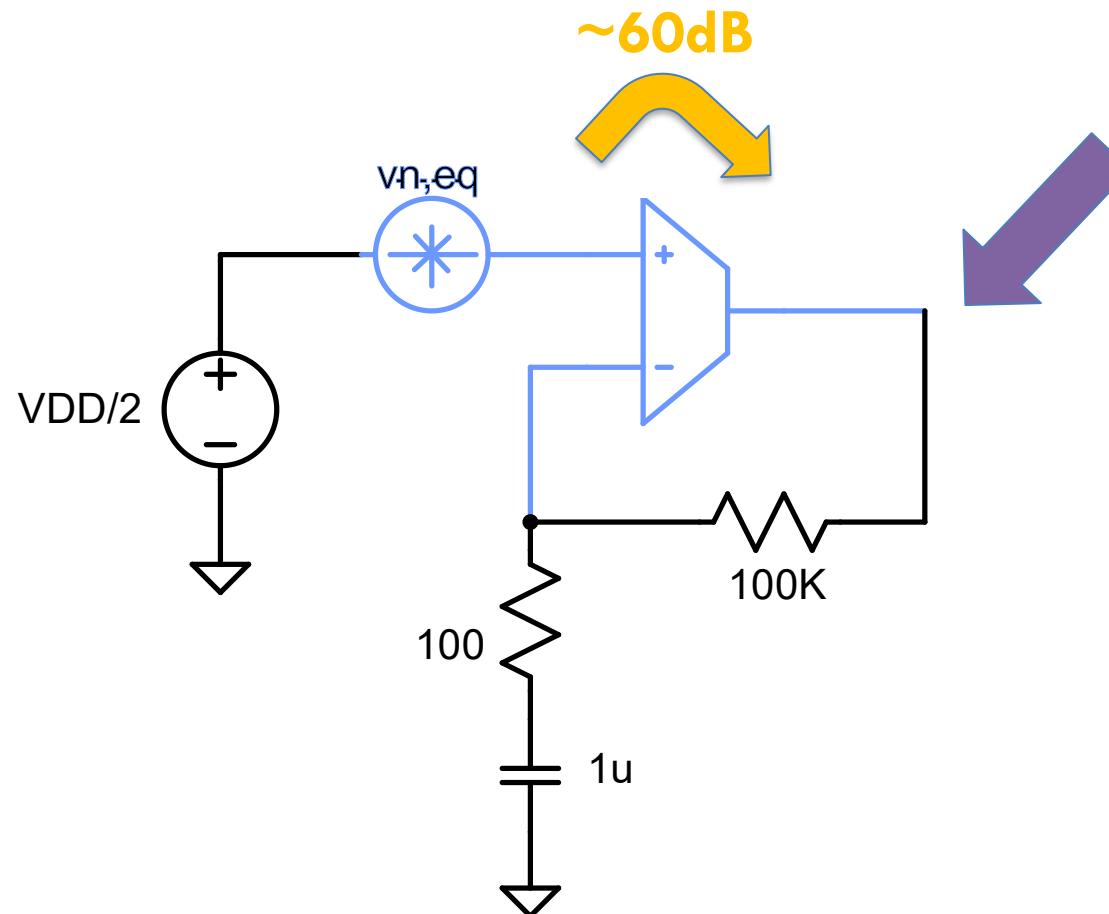
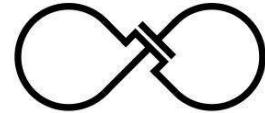




OTA in AC Open-Loop



OTA in AC Open-Loop

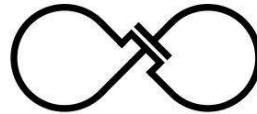


Video Interview with Matt Venn



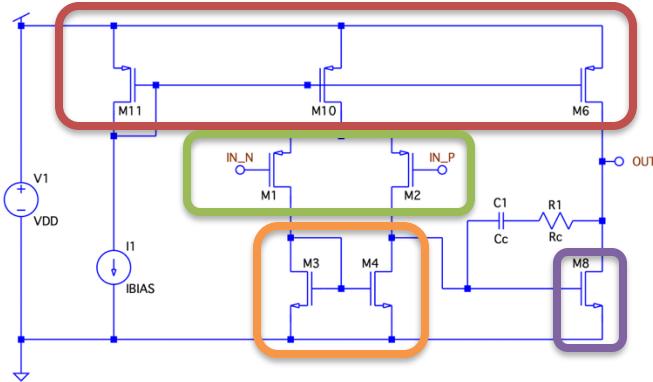
- Zero to ASIC Course
- June 25, 2025
- [MOSbius - A field programmable transistor array for chip designers - interview with Peter Kinget](#)
 - [One-Bit Delta-Sigma Converter Demo](#)

How was MOSbius architected?



- Started from two-stage OTA

- pMOS input diff. pair



- nMOS input diff. pair → dashed boxes

- Provided all components for a fully differential two-stage OTA

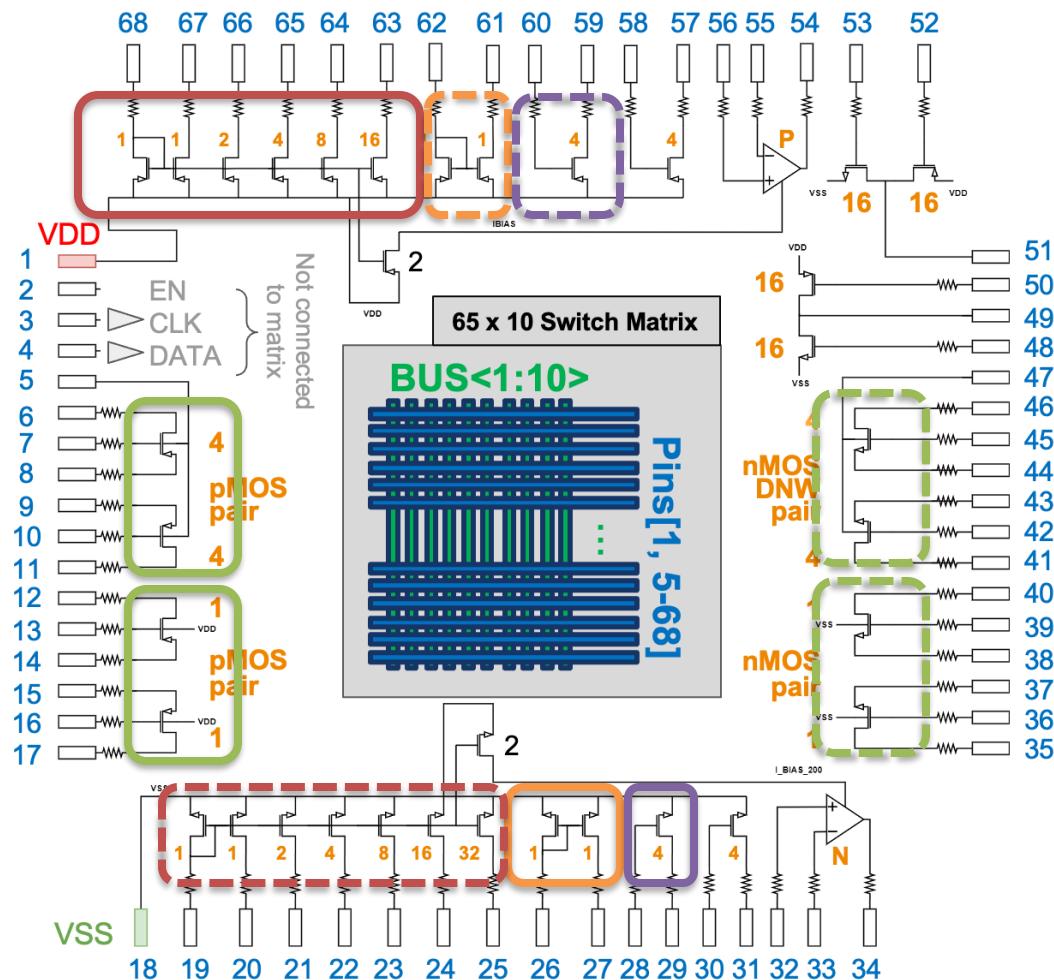
- Added other blocks like:

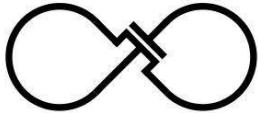
- One-stage OTAs
- Inverter output stages

- Added Switch Matrix

- 10 BUSes
- CLK, DATA, EN pins

Note: Even though we started from a two-stage OTA, many other circuits have been built with these basic transistor assemblies

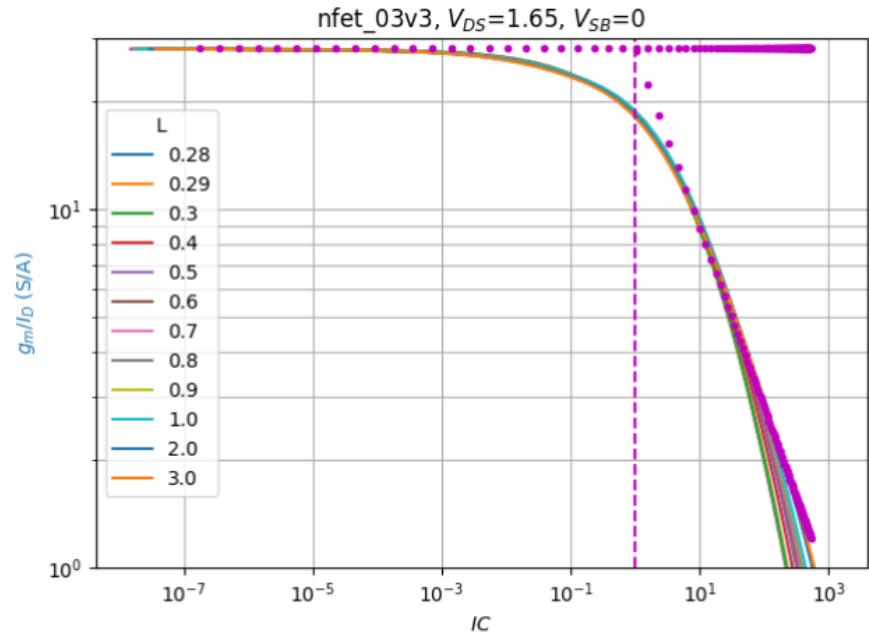
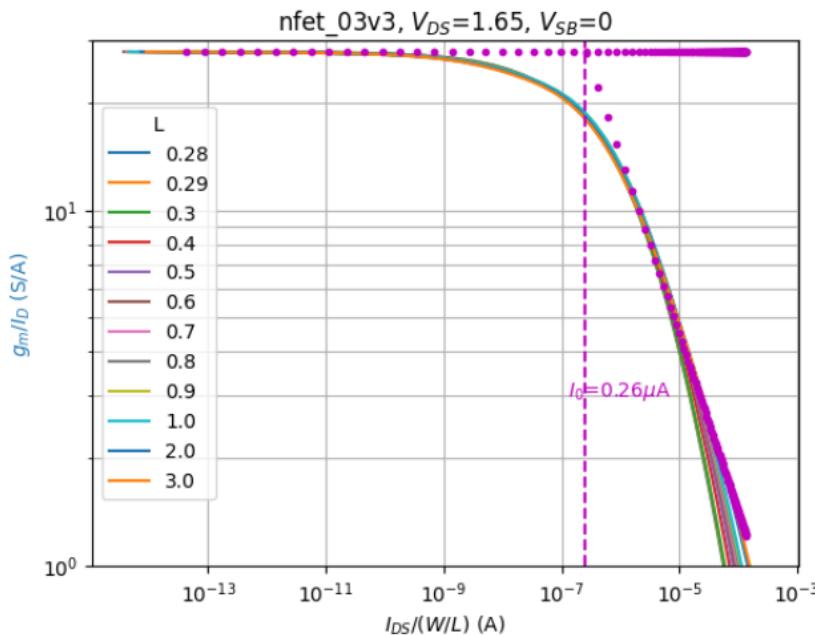




Transistor Bias Point Selection

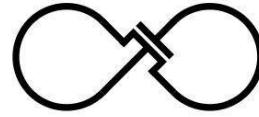
- Used a gm/ID approach and found the W/L so that:
 - $I_C = 10 \text{ & } I_{DS} = 100\mu\text{A} \text{ & } V_{OV} \simeq 200\text{mV} \text{ & } (gm/I) \simeq 9$
- In GF180, for 3.3V nMOS
 - $I_0 = 0.26\mu\text{A} \rightarrow IC = 10 \text{ & } gm/I \simeq 10 \text{ S/A}$
 - for $IDS = 2.6\mu\text{A} \text{ & } W/L = 1$,
 - for $IDS = 26\mu\text{A} \text{ & } W/L = 10$, etc.

- Double Check yourself!!
- What is it for PMOS??
- Choose your own bias point

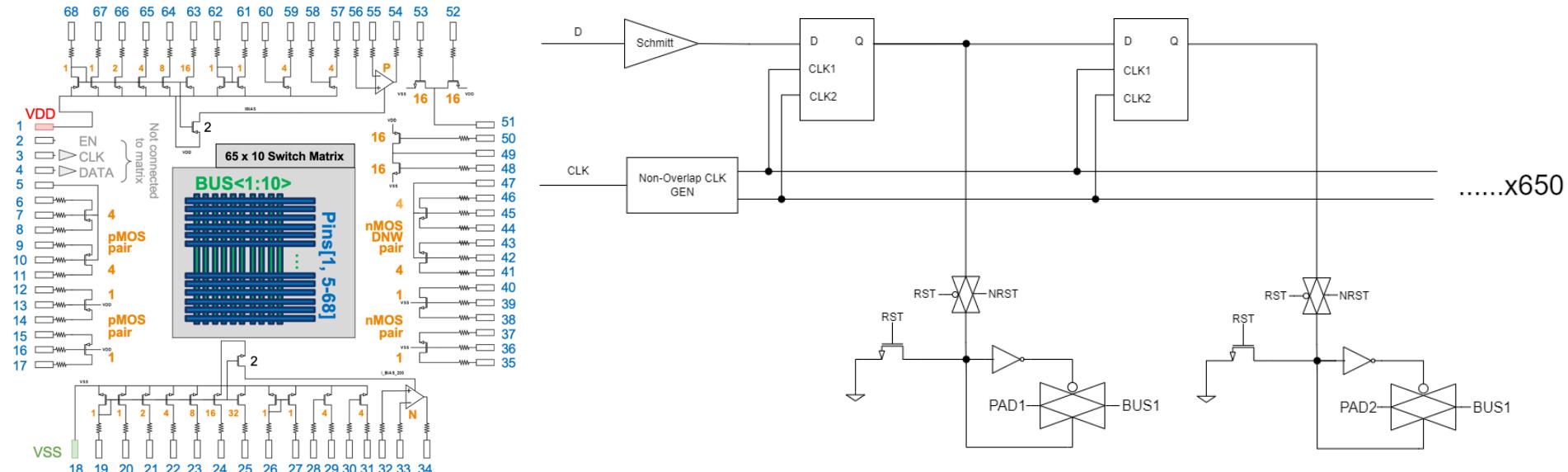


https://github.com/mosbiuschip/chipathon2025/blob/main/gf180mcuD_technology_info/README.md

Switch Matrix Design Considerations

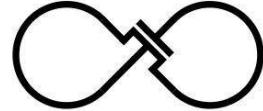


- R_{on} of the Transmission Gate
 - 50-100 Ohm depending on your choice of bias point & transistor sizes
- Control Path
 - Shift Register → careful with clocking (hold time violations ...) → we generate non-overlapping clocks



[Details for current MOSbius](#)

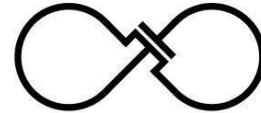
How to architect your MOSbius chip:



- Think about use cases for your chip
 - What experiments can your chip support?
 - How easy will your chip be to use, program, ...
 - How will your chip & experiments draw people into IC design?

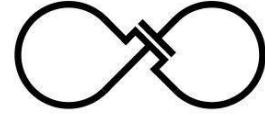
The design goals are not only about the design and tape-out, but also about your **chip's application**, i.e., what **experiments** your chip can support.

MOSbius Chipathon Ideas



- Port current '*analog*' MOSbius (*in part*) to GF180
 - Significant benefits that everything will be in open-source, in particular, transistor models and layouts → better simulations, 3D animations, ...
- Develop '*digital-transistor-level*' MOSbius
 - DFFs, logic gates, ... at circuit level
- (very advanced) *RF MOSbius*
 - RF building blocks to configure various RF receiver topologies
- **Your Ideas**

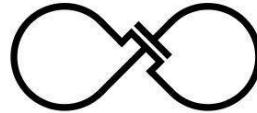
Make a Chip Proposal



- Datasheet
 - Functionality of your chip & target specs
 - Block diagram
 - Functionality of building blocks
 - Schematics, if available, and design complexity of building blocks
 - Pin-out
 - Application diagrams
 - How do you test/demonstrate your chip
- Team members
 - Work distribution across team
- Schedule
 - Week by week
 - Align with Chipathon schedule

Put it in your GitHub project repository & share with mentors
on fossi-chat so we can start reviewing and give feedback

MOSbius Chipathon Documentation



- <https://github.com/mosbiuschip/chipathon2025>
 - main branch → confirmed
 - other branches → WIP
 - linked from SSCS Chipathon 2025 Repo
- Information on Tools
- Information on GF180
- Project Repo Template

README

IEEE SSCS Chipathon2025: MOSbius Track Documentation

In this repository you will find the main documentation associated with the MOSbius track for the [IEEE SSCS Chipathon 2025](#)

Getting Started with Your Project

- [Overview of the MOSbius Track](#)

MOSbius Track Documentation Resources

- [MOSbius Website](#)
- [MOSbius Chipathon 2025 Documentation \(this repo\)](#) has documentation, installation instructions, and technology information.
- [GF180 Analog Design Project Template Repo](#) is a template for creating your project file repository on GitHub (see below and in [CAD_tool_installation](#))

Structure of This Repository

- [CAD_tool_installation](#) has installation instructions for the open-source IC CAD tools.
- [CAD_tool_computing_constellation](#) gives an overview how the tools are being run on your computer.
- [CAD_tool_flow](#) explains the various CAD tools, their input and output files, and how they interact.
- [gf180mcuD_technology_info](#) has information resources about the GF180 technology gf180mcuD and links to design examples.

Creating Your GitHub Repository for Your Design Files

- To create the GitHub repository for your design files so you can collaborate among your team, you can create a new repository from the template in the [GF180 Analog Design Project Template Repo](#).
- The template has a suggested folder structure, as well as an example of a small design of a five-transistor operational transconductance amplifier (5T-OTA) including schematics and layout.
- This template is part of the [installation instructions \(simplest version\)](#).