Design Project – EECE 416, Fall 2019

(*while this is an evolving document with details subject to change, the "gist" of the design project assignment is as described*)

As discussed in lecture, the goal of this project is to design a 8-bit successive approximation analog-to-digital converter (SAR ADC) in the MOSIS AMI 0.6µm CMOS process (where the minimum width and length for transistors is 3µm and 0.6µm, respectively). To accomplish this task, your team will need to design the following blocks:

1. Digital-to-Analog Converter (shared between team members),
2. SAR Logic/Register (to be done by team member A)
3. "Clocked" Comparator + Timing Circuitry (to be done by team member B)

You do not need to design a sample-and-hold (S/H) circuit, and you may use a SPICE macromodel for the S/H in your simulations.

In addition to having a functional chip, the goal of your project is to have made design efforts towards maximizing the "speed" (i.e. conversation rate) of your ADC.

Collaboration vs. Cheating

While it is encouraged to help each other out, there are limits to sharing ideas with other group members/teams. **DO** brainstorm on the "big picture" and general design ideas associated with different topologies. **DO** help each other debug simulation problems. However, **DO NOT** share actual designs **nor** simulation files with other group members/teams.

Project Milestones

September 13	Determined team members and block responsibilities; Begun design of the chip using behavioral models for components (logic gates, flip-flops, switches, comparator, DAC)
October 11	Behavioral system design of ADC complete (LTSPICE verified); Begun transistor-level design of each block
November 15	LTSPICE transistor-level simulation, verification of each block complete; Begun integrating all blocks at transistor-level to form entire chip
November 22	LTSPICE verified operation of entire chip at transistor-level
Post-Thanksgiving	Final Report, Presentation