

**California State University, Chico**  
Department of Electrical and Electronics Engineering



EECE 316 Electronics II

**Design Project**

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Due 5/8/2019

**Objectives for the Design Project:**

The Design Project is separated into two phases and both collaborators were involved in the project as a whole. The goals for the first stage is to design, simulate, build and test a fixed 8 V output linear voltage regulator.

The specifications for the regulator:

1. Input voltage: 0 V - 12 V
2. Output load current (realized by load box): 0 mA - 100 mA
3. Max values for electrolytic, ceramic caps CE and CC are 100  $\mu$ F and 100 nF
4. Define the dropout voltage VDO as the minimum input voltage that yields an output voltage  $8 \text{ V} \pm 2\%$  (i.e. for  $\text{VDO} \leq \text{input voltage} \leq 12 \text{ V}$ , output voltage of your regulator is  $8 \text{ V} \pm 2\%$  )
5. Define the circuit current ICIRCUIT as the current consumed (dissipated) by your regulator circuitry for an input voltage 12 V
6. Define the transient settling time tSETTLE as the worst-case time necessary for your regulator's output voltage to settle to  $8 \text{ V} \pm 2\%$  upon switching 0 mA - 100 mA . It is assumed that the input voltage is constant at 12 V
7. Figure of Merit (FOM)= $\text{VDO} (@ \text{worst-case load condition}) \times \text{ICIRCUIT} (@ \text{worst-case load condition})$

The specifications for the Differential Amplifier:

1. Differential-mode gain  $\geq 1000$
2. Common-mode rejection ratio: Maximize

#### Application:

The voltage regulator that is being designed for this project could be used for many applications. Almost all of circuitry today requires a stable power supply to be able to function properly so this is of importance to be familiar with and obtain this practice. This design project gave us an internal view of a real life application that could be asked of us to design in our near future as electrical engineers. With the ability to maintain a stable voltage, like the 8 volts that is required for the design project, we have endless possibilities for this voltage regulator. Now comes the importance of the load. The requirement for this design project is to be able to have a voltage regulator that has the ability to handle a load of 0-100mA. This load could be a device that pulls that amount of current and it could be anything from a microprocessor, sensor, or even a LED. Therefore, the concept of making a voltage regulator is important in the field of electrical engineering, due to how common it is in everyday circuits and how it affects a large portion of citizens everyday lives. The specifications that were achieved for the design project regulator were:

- To have an Input voltage: 0 V -12 V
- To have an Output load current: 0 mA -100 mA
- Obtain an Output voltage:  $8 \text{ V} \pm 2\%$
- Define the dropout voltage VDO
- Tsettle
- Differential-mode gain  $\geq 1000$

## Circuit Schematic/Description

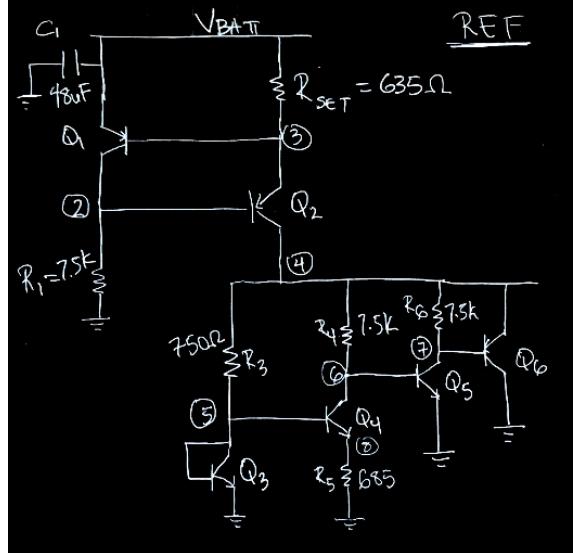
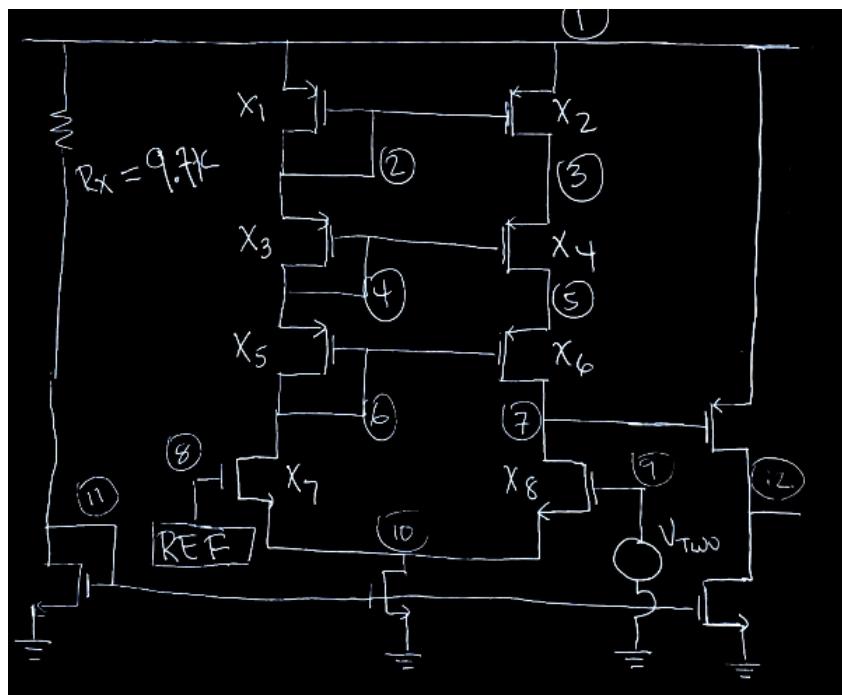


Figure 1. Operational Amplifier

Figure 2. REF Circuit which produce 1.3166V

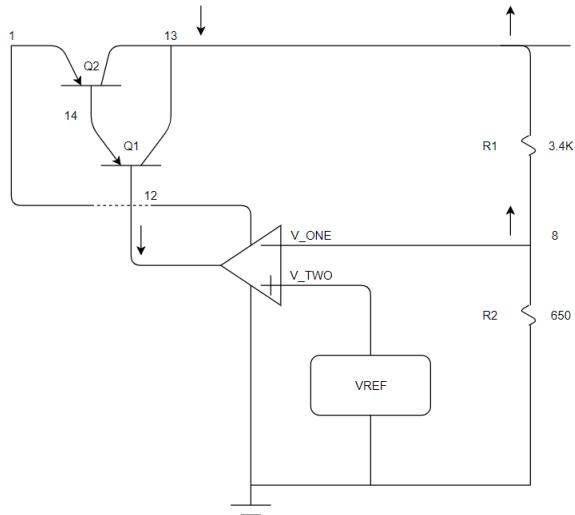


Figure 3. Negative Feedback and complete circuit of part I  
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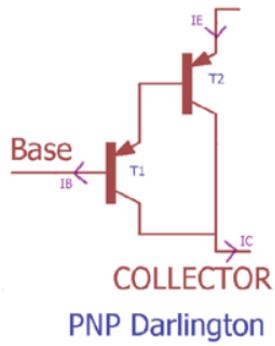


Figure 4: PNP Darlington Pair

### Analysis Calculations

Let's analyze and derive an equation for the Op Amp. To accomplish this we need to state the resistance rules we used.

#### Resistance Rules

Open Amp

Resistor Rules

$$R_{eq} = \frac{1}{g_m}$$
  

$$R_{eq} = \frac{r_o + R_y}{1 + (g_m)(r_o)} \approx \frac{R_y}{(g_m)(r_o)} \approx \frac{1}{g_m}$$

$$g_m = 2\sqrt{k I_D}$$

↑  
↳ Same k value for two or more NPN  
↳ same is true for PNP

Figure 3. Equation I, and Equation II

Using the Gain Rules shown above which was learned in EECE 315 and Review in EECE 316.

$$\frac{V_o}{V_{in}} = \frac{-g_m R_y}{1 + g_m R_x}$$

Figure 4. Equation III

To find the small signal gain of our Op Amp:

- We can replace the current source which is produced by the circuit shown below with an ideal current source

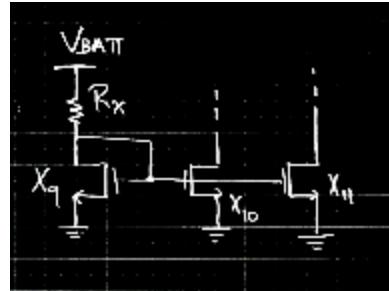


Figure 5

We will investigate the current source in figure 5 later.

To simplify our computation, we will remove the piece at node 7 shown below

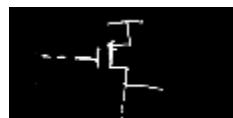
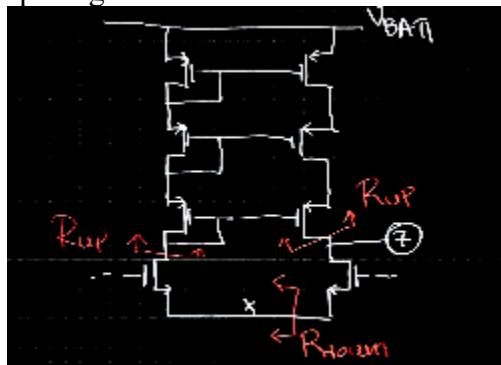


Figure 6

We will add the piece in figure 6 once our equation is derive for node 7.

We can open  $I_{SOURCE}$  to find the gain at Node 7 &

→ Redrawing the Op Amp we get:



Using Equation I, we can solve for  $R_{up}$ ,  $R_{down}$ , and  $R_{up}$  which give us:

Equation IV:

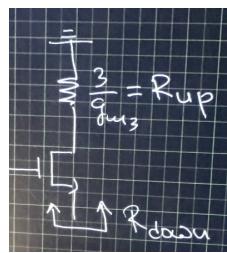
$$R_{up} = 1/g_{m1} + 1/g_{m3} + 1/g_{m5}$$

Using figure 3 Equation I, and Equation II we found that:  $g_{m1} = g_{m2} = g_{m3}$

Equation IV can be rewritten as:

$$\therefore R_{up} = 3/g_{m1}$$

We can redraw the left side of the Op Amp:



We can solve for  $R_{down}$  by applying Equation II. we obtain Equation V:

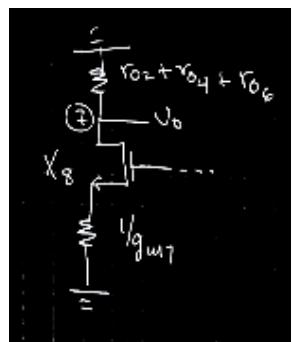
$$R_{down} = (r_{o7} + 3/g_{m3})/(I + g_{m7}(r_{o7})) \approx I/g_{m7}$$

We solve for  $R_{up}$  on the right hand side which gives

Equation VI

$$R_{eq} = r_{o2} + r_{o4} + r_{o6}$$

We can redraw the right side of the Opamp:



Using the gain equation 4

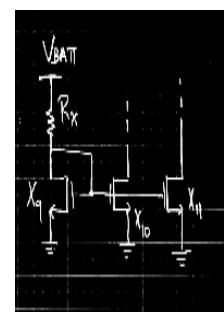
Equation VI

- $\frac{V_o}{V_{in}} = \frac{-g_{m8}(r_{02}+r_{04}+r_{06})}{1+g_{m8}(\frac{I}{g_{m7}})}$
- Using figure 3, it can be observed that X7 and X8 have the same  $g_m$  value
- Now equation VI can be simplified to  $\frac{V_o}{V_{in}} = \frac{-g_{m8}(r_{02}+r_{04}+r_{06})}{2}$

Equation VI

$$I_{C10} = I_{C11} = I_{C9} = \frac{VBATH - V_{G9}}{RX}$$

We can redraw the right side of the Opamp:



Lets analyze the current source in figure 5

- The drain current of X9 can be determined by  $I_c = \frac{VBATH - V_{G9}}{RX}$
- For NMOS, it is known that  $I_D$  (Drain Current) flows from drain to Source of X9
- Since  $V_{GS9}=V_{G9}-0$ , this holds true for X10 and X11, respectively
- Therefore,  $I_D$  of X9 is mirrored across the drain of source of X10 and X11

### Gain Equation

$$\frac{V_0}{V_{in}} = \frac{(-g_{m12})(r_{011})(-g_{m8})(r_{02}+r_{04}+r_{06})}{2}$$

Redrawing the Op Amp and using the gain equation we get:

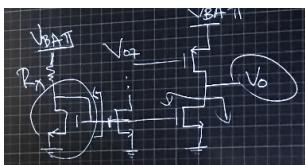


Figure 6B

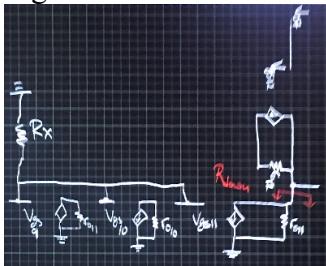


Figure 6C

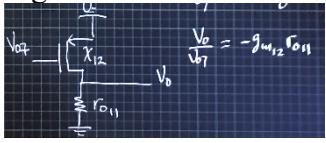


Figure 6D

Now we add figure 6 to the Op Amp. This will give us the complete Op Amp shown in figure 1.

- $V_{07} = \frac{(-g_{m12})(r_{02}+r_{04}+r_{06})}{2} * V_{in}$

We can finally add figure 6 to get figure 1 (see figure 6B).

We draw the small signal for figure 6B as shown in Figure 6C.

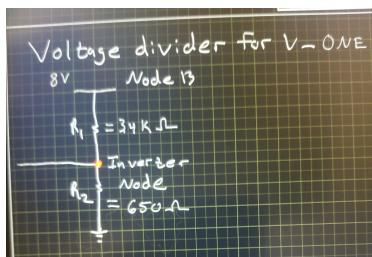
Using figure 6C, we found  $R_{down} = r_{011}$ . Therefore, we can redraw figure 6B and find the gain of our opm amp.

- $\frac{V_0}{V_{in}} = (-g_{m12})(r_{011})$

- $V_0 = \frac{(-g_{m12})(r_{011})(-g_{m8})(r_{02}+r_{04}+r_{06})}{2} * V_{in}$

- $\frac{V_0}{V_{in}} = \frac{(-g_{m12})(r_{011})(-g_{m8})(r_{02}+r_{04}+r_{06})}{2}$

### Voltage Divider for V\_ONE

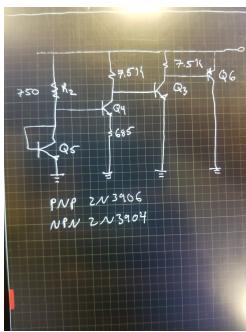


Calculating the appropriate voltage for V\_One is as follows:

- $V_- = V_{out} * \left( \frac{R2}{R1+R2} \right)$
- For optimal gain, a voltage of 1.31664 V is required.
  - Therefore 1 unknown is left in the Voltage Divider equation.
  - $V_- = 1.31664$ ,  $V_{out} = 8V$ , An arbitrary resistor in the 315 parts kit is chosen and  $R1 = 3.3k\Omega$ .
- $1.31664V = 8V * \left( \frac{R2}{3.3k + R2} \right)$
- $\frac{1.31664V}{8V} = \left( \frac{R2}{3.3k + R2} \right)$
- $\left( \frac{3.3k + R2}{R2} \right) = \frac{8V}{1.31664V}$
- After algebraic massaging,  $R2 = 650\Omega$ .

## Ref Block

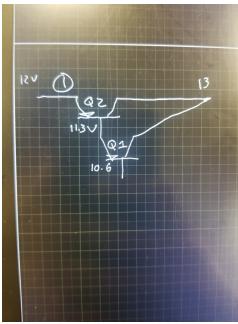
## Negative Feedback current source



- RSet allows us to set the desired current value for the source into the Bandgap.
  - $I_{Load} = \frac{VBATH - 0.7}{R_{SET}}$
  - $R_{SET} = \frac{VBATH - 0.7}{I_{LOAD}}$ , This  $I_{LOAD}$  is the one that we want
  - The current across R1 role is to provide a path for the necessary collector and base current of Q1 and Q2 respectfully
    - $I_1 = \frac{0.7 - 0}{R_x} = \frac{0.7 - 0}{7500}$

## BandGap Temperature Equation

- The Bandgap circuit offset voltage  $\Delta V_{BE}$  can be any of the following equations:
    - $\Delta V_{BE} = V_{BE1} - V_{BE2}$
    - $\Delta V_{BE} = \frac{KT}{g} \ln \frac{I_{c1}}{I_{c2}}$ 
      - Where:  $\frac{KT}{g} = V_T$  = Thermal Voltage = 25.7 mV
      - $I_c$  = Collector Current
      - $K$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  J/K
      - $g$  = Charge of the electron =  $1.6 \times 10^{-19}$  C
      - $\Delta V_{BE} = \frac{KT}{g} \ln \frac{R1}{R2}$ 
        - Where R3 or R4 or R6 = Resistor value
          - (Using in a ratio of 8:1, 10:1, etc)
    - The circuit's temperature coefficient ( $TC$ ) can be determined by the following :
      - $TC(\text{in } \mu\text{V}/\text{C}^\circ) = \frac{\Delta V_{BE}}{\Delta V_{TEMP}} - \frac{K}{g} \ln \left( \frac{I_{c1}}{I_{c2}} \right)$ 
        - Where:
          - $\frac{K}{g} = 86.25 \text{ } \mu\text{V}/\text{C}^\circ$



### Calculating the Current gain( $\beta$ ) for the VCCS Darlington Pair (2N3904)

- For best and worst case scenario for 0-100mA, and all of this information came from the 2N3906 Data Sheet
  - $I_c=0.1\text{mA}$ ,  $\beta = 60$
  - $I_c=100\text{mA}$ ,  $\beta = 30$
- $\beta_{TOT} = \beta_{Q1} * \beta_{Q2} + \beta_{Q1} + \beta_{Q2}$
- This is for the worst case scenario
  - $\beta_{TOT} = 30^2 + 60$
  - $\beta_{TOT} = 960$

$\beta$  is the ratio of the collector current to the base current

The way that the Darlington Pair is able to achieve such a large current gain can be symbolically explained as follows:

1. The circuit layout is that the collectors of Q1 and Q2 are connected and the emitter of Q1 is able to drive Q2 base. This is key to why  $\beta$  is able to practically become squared.
2.  $I_c = I_{c1} + I_{c2}$ 
  - a. Equation 1:  $I_c = \beta_1 * I_B + \beta_2 * I_{B2}$
  - b. Since the emitter of Q1 " $I_{E1}$ " is connected to Q2  $I_{B2}$   
Equation 2:  $I_{B2} = I_{E1} = I_{C1} + I_B = \beta_1 * I_B + I_B = (\beta_1 + 1) * I_B$
  - c. By combining Equation 1 and Equation 2, the value of  $\beta$  can be solved as:  

$$I_c = \beta_1 * I_B + \beta_2 (\beta_1 + 1) * I_B$$

$$I_c = \beta_1 * I_B + \beta_2 \beta_1 I_B + \beta_2 I_B$$

$$I_c = (\beta_1 + \beta_2 \beta_1 + \beta_2) I_B$$

PBJT formula:  $P_{BJT} = I_c(V_{CE}) + I_B(V_{BE})$

c(Q2) :	-0.100968	device_current
b(Q2) :	-0.00101191	device_current
e(Q2) :	0.10198	device_current
c(Q1) :	-0.00100693	device_current
b(Q1) :	-4.98445e-006	device_current
e(Q1) :	0.00101191	device_current

To solve the PBJT formula:

- For each Q1 value and Q2 value, we had to substitute the appropriate Collector and Base current.
- After, we add both equations to have the total PBJT formula and use that to find the  $\Delta T_{XTOR} = (P_{XTOR})(\theta)$ 
  - $= 2.8 * 10^{-4} (200)$
  - $= .056$
  - $T_{XTOR} = (25^\circ C)(\Delta T_{XTOR})$
  - $= 25.056^\circ C$

## Simulations



Figure 7. Change in Bandgap temperature.

The figure above is the LTSpice simulation for the change in temperature to the BandGap reference. The step size for this module is 1 degree celsius and it starts at room temperature of  $23^{\circ}\text{C}$  (*approximately*  $73^{\circ}\text{F}$ ) to  $30^{\circ}\text{C}$  (*approximately*  $86^{\circ}\text{F}$ ). The change from  $23^{\circ}\text{C}$  to  $30^{\circ}\text{C}$  only produces a 24mV difference. Also, at optimal temperatures the Bandgap reference produces the desired voltage.

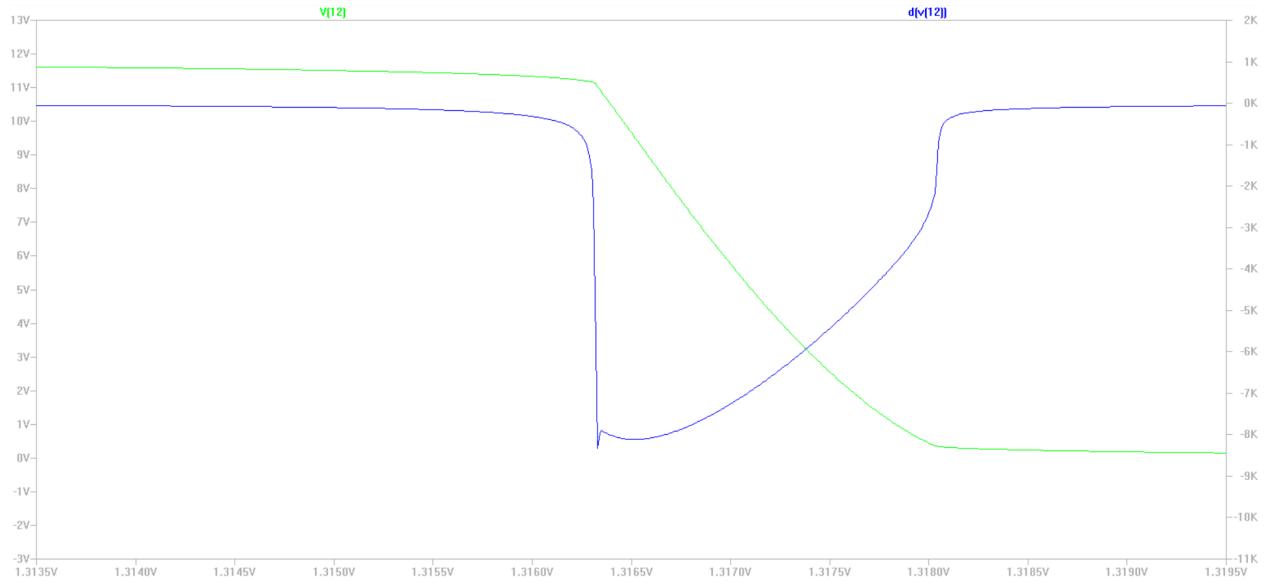


Figure 8. Green shown the Gain and the Blue line show the derivative on the gain.

The figure above is the image obtained from LTSpice and due to these results, we came to the conclusion that the theoretical results were satisfactory enough to proceed and physically build the Operational Amplifier.



Figure 9. The green plot show the Op Amp in figure 3 at node 13 without a current load. The remaining plots show node 13 with  $I_{load}$  ranging from 0-100mA and at increments of 20mA.  
8.712 -8.888

## Experiments

In the beginning of the design project, the first task became to build an Operational Amplifier with a minimum gain greater than 1000. Once we came to the conclusion that a Differential Op Amp with an Active load would be our design, building the circuit seemed straightforward. Our main focus became to construct the first stage of the Op Amp. The first gain stage of the circuit can be seen in figure 1 but excluding the current source. The PMOS transistor X1, X3, and X5 is the region in the circuit that is the Active Load and cascode three times. It can be distinguished that this is a active load by observing that this topography is a transistor current source that is essentially replacing the drain resistors. This is done by having the terminals of the transistors in figure 1(X1, X3, and X5) “sharing” their Gate and Drain node, hence producing a current mirror. The building of the Differential Op Amp which seemed straightforward presented the most challenge. The first construction of the Op Amp failed, which left us second guessing everything. It turned out that there were wiring issues with the first gain stage of the OP Amp and this issue resolved itself by becoming more organized and eliminating unnecessary long wires that cluttered the circuit board. With the addition of the current source, the design that we used allowed there to be a second gain stage and increased the gain of the Differential pair immensely. Also the value for RX would determine the amount of current that would flow through the current source and therefore influence the slope of whether the voltage regulator output would be almost an ideal 8V or  $\pm$  a degree of voltage, see figure 9. After the stepback with wiring, we looked at lab 2B for guidance to make sure that we had the appropriate gain that we theoretically obtained from LTSpice. Exactly like in lab 2B, we Configured the function generator to produce a “slow” triangular wave that sweeps the input voltage from 0V to 12V. This is just like performing a DC sweep and we then used the X-Y plot setting of the oscilloscope to plot the output voltage versus input voltage, gain of the Op Amp, and identify the approximate range for when the gain is  $\approx -7000$ . The last setback that we had for the Op Amp was that we flipped the polarity for the entire circuit and fried all of the PMOS and NMOS array chips. This happened due to the sensitivity of the transistor arrays and essentially doing the complete opposite of making Pin number 4 (for each chip) be tied to the most negative voltage in the circuit and also Pin number 11 (for each chip) be tied to the most positive voltage in the circuit. Irreversible damage was caused to the chips and the solution became to buy a new set of PMOS and NMOS array chips. After this predicament, the Op Amp became a fully operational module.

The building of the voltage reference (REF) in figure 2 was straight forward. We connected the circuit as shown in figure 2 directly onto a breadboard. Due to not having the exact resistors values in the supply kits. We first used the lab potentiometer as  $R_{SET}$  and changed it's value to get the right voltage for our bandgap circuit. The building of the bandgap presented a major challenge. The output voltage produced by figure 2 did not match LTSpice model of 1.3V. To solve this problem, we change the value of  $R_5$  for reasons which are stated in the discussion section on this report. Reducing  $R_5$  to  $10\Omega$  and changing  $R_{SET}$  to  $677\Omega$ , gave us a voltage of 1.3V.

With the reference voltage (REF) working and connected to the Op Amp, the next step was to connect VCCS to the Op Amp and use a voltage divider to achieve the desired voltage at Node 8, see figure 3 and Voltage Divider for V\_ONE equation. The voltage divider equation was performed by hand calculation with the assumption that the output voltage at Node 13 was 8V. This assumption was base on the lab description and our LTSpice model (netlist) with a current load of 100mA. Base on the theoretical calculation and computer simulation,  $R_1$  and  $R_2$  was set to  $3.3\text{k}\Omega$  and  $650\Omega$ , respectively. The actual breadboard circuit didn't produce 1.29V to 1.316V range. To solve this, we change  $R_1$  to 3.4K and used a Resistor Box to adjust the value of  $R_2$ . Increasing the value of  $R_2$ , decreases the value at Node 8, and decreasing the value of  $R_2$ , decreases the values of Node 8. At  $R_2 = 581$  we obtained our desired voltage at Node 8 of 1.29V.

## Discussion

The big picture of figure 1 is to be able to produce an Operational Amplifier that has a large enough gain that it could utilize negative feedback to oppose noise, distortion, and sensitivity to external changes. This is a pivotal feature for this project to be successful and that is why the minimum gain has to be a value of Differential-mode gain  $\geq 1000$ . The Operational Amplifier topology that we chose for the design project is the differential pair with an active load that is cascaded three times and has two gain stages. The active load can be seen as the PMOS transistors X1–X6 and transistors X1, X3, and X5 are current mirrors due to the Gate and Drain of the transistors being connected to each other. See figure 5 and Equation VI and Equation IV for further elaboration.

The Voltage Reference (REF) which is shown in figure 2, ideally produces a fixed/constant voltage irrespective to a load on the device, power supply variation, and temperature change. The goal was to create a reference voltage that is not sensitive to change in  $V_{BATT}$  and/or change in temperature. This was accomplished by creating a negative feedback current source which produce a constant current regardless of change in  $V_{BATT}$ . And attaching that current source to a bandgap topology. Together both structure produced a reference voltage that's not sensitive to change in  $V_{BATT}$  and/or temperature. Let's break apart the structure in figure 2, and focus on the working of the negative feedback circuit.

The top half of figure 2, which runs from  $V_{BATT}$  to Node 4 served as the current source. This circuit depicts a current source that includes a negative feedback loop. Negative feedback is an effective technique for providing enhanced output impedance. The role of  $R_1$  is to provide a path for the necessary collector and base current of transistor Q1 and Q2, respectively.  $R_{SET}$  allow the designer to set the desired value of the current of the source. In other words, since current flows from emitter to collector in a PNP transistor. The current flowing through the emitter and

collector of Q2 is produced by the base current of  $Q_1$  plus the current through  $R_{SET}$ . Therefore, increasing the value of  $R_{SET}$ , increases the source current, and decreasing the value of Rset decreases the value of the source current which is being applied to the bandgap voltage Reference.

The second half of figure 2 depicts a bandgap voltage reference circuit, which is a temperature independent voltage reference circuit. It product a fixed voltage regardless of power supply variation, temperature change, and load added to the device. It commonly has an output voltage around the theoretical 1.22 eV bandgap of silicon at 0 °C. The operation of our bandgap circuit is as such, three identical NPN transistors and one PNP transistor, with three of the NPN typically operating at either an 8:1 or 10:1 current density ratio. If  $Q_3$ 's collector current is make to be 10 times that of transistor  $Q_2$ , then the  $V_{BE}$  difference will appear across  $R_5$ . This may be achieved using either 10 times the emitter area or 10 times the current level. At room temperature, and with this 10:1 current density ratio, the change in  $V_{BE}$  will be 59mV, and with a negative tempco of approximately -0.2mV/C (Please refer to data sheet). This is because two identical junctions with different currents flowing through will produce different voltage drops. The ratio of the two collector currents determines the value of this offset voltage ( $\Delta V_{BE}$ ), as will be shown in equation 2 of the analysis calculations on this report. In other word, Transistor  $Q_4$  and  $Q_5$  realize the change voltage  $V_{BE}$  generated for the bandgap circuit. Transistor  $Q_3$  realizes the  $V_{BE}$  voltage from the bandgap circuit, with transistor  $Q_6$  and resistor  $R_6$  used to fix the current of  $Q_3$ .

The big picture, without going above the level on this class and undergraduate level. Is that as long as the current ratio, which is produced by resistance  $R_3$ ,  $R_4$ ,  $R_5$ , and  $R_6$ , is maintained at a constant level then change  $\Delta V_{BE}$  will be linear with absolute temperature, over most of the temperature range. It's worth noting that  $\Delta V_{BE}$  of  $Q_3$  is summed with the voltage across  $R_4$ .

Therefore,  $\Delta V_{BE}$  is just equal to node 6. The current through the collector and emitter of  $Q_5$ , also known as the collector current of  $Q_5$ , can be found by using equation learned in EECE 315 which depend on knowing the value of  $\Delta V_{BE}$ . And since  $\Delta V_{BE}$  of Q6 is summed the the voltage of node 7, this creates a constant output voltage at node 4.

The big picture here is that the above topology shown in figure 2 (The negative feedback current source and The Bandgap Voltage Reference Circuit) give us a REF block that is responsible for producing a precise/temperature independent reference voltage.

Figure 3: Voltage Controlled Current Source

For the voltage controlled current source, the main topology that was focused on to produce the desired results was the Darlington transistor circuit (Darlington Pair). The purpose of a VCCS is to have a desired controlled voltage and to use this factor to dictate the behavior of the current device. Now let us focus on the why a PNP BJT (**2N3906**) was chosen for the the Darlington pair. First off, if noise were to be injected into **Node 13**, above R1, this would reciprocate that node 8 would also go up as well. Since V\_ONE is the inverter input that is tied to the voltage divider, this important note leads to the original injected noise to be flipped due to it being the inverter terminal. Now the output of the Operational Amplifier will feed to the VCCS and to choose the appropriate BJT, the correct polarities will have to be looked into.

Polarities of BJT rules:

- Base to Collector: Negative
- Base to Emitter: Positive
- Emitter to Collector: Positive

The Base to Collector of Q1 will complete the loop for Negative feedback and the diagram below proves that this design follows the rules for negative feedback.

Why was a PNP chosen over a NPN BJT in the first place? PNP and NPN BJTs are almost identical in every way other than how the junctions are biased. The differences in polarities of the voltages, which leads to opposite flow of current, have a major impact on the design for the VCCS. For PNP  $V_{BE}$ , the base junction is guaranteed to be biased negative with respect to the emitter and a given rule is that the emitter supply voltage is positive to  $V_{CE}$ . What this translates to is that a PNP BJT needs to have a higher voltage at the emitter to conduct, with respect to both Base and Collector. The PNP approach is perfect for the the VCCS and this proves that NPN wouldn't work as well or as efficiently for the VCCS.

Originally, the idea of using QTIP32 PNP model seemed like an attractive thought at first but there were many complications that came with it. The QTIP32 is a great PNP BJT and this is due to the packaging of it. The reasoning to why the packaging is such an important issue to the VCCS is due to how the "Thermal Resistance"(Junction-to- ambient) would affect the temperature of the chip and losing power in the form of heat. This would make our design not as efficient as it could be.

- QTIP32 TO-220 package  $\theta_{j-a}=50-60 \text{ } ^\circ\text{C/W}$
- 2N3906 TO-92 package  $\theta_{j-a}=190-200 \text{ } ^\circ\text{C/W}$

The QTIP32 PNP model has the desired "Thermal Resistance"(Junction-to- ambient) but the complications to this model is that it doesn't allow sufficient current to flow through either Q1 or Q2. On LTSpice, there was no issue using the QTIP32 and it allowed the voltage regulator to perform its duties but building the physical circuit on the breadboard showed that Q1 remained in saturation with  $aV_{BE}=.584\text{V}$ . This means that Q1 emitter couldn't drive the base of Q2 so it couldn't perform the desired task. With the replacement of QTIP32 with a 2N3906, there was proper flow of current and both BJT's were able to stay in forward active regions. Also, having a Darlington pair greatly reduces the heat that would be a byproduct of the NPN BJT. This is due to reducing the current that goes into a BJT and splitting the current associated to each PNP. See PBjt formula for explanation.

## Part II The Voltage Regulator or Booster Converter.

The objective of this section was to designed a boost converter to boost a 5V input and produce an 8V output when a load of 100mA is applied.

### Circuit Schematic/Description:

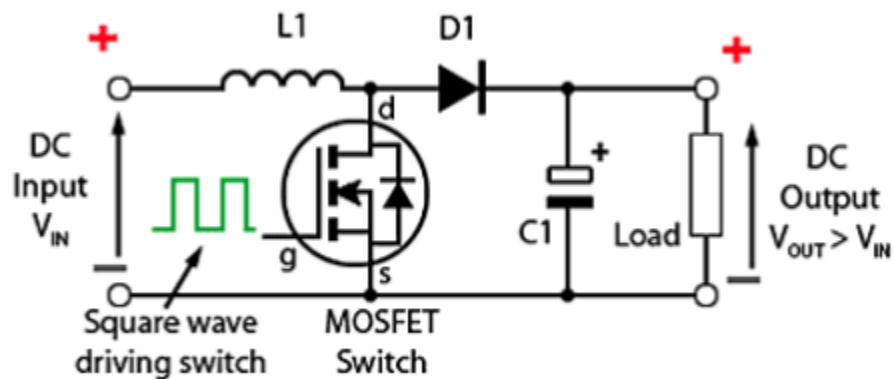


Figure 1. The basic boost converter circuit

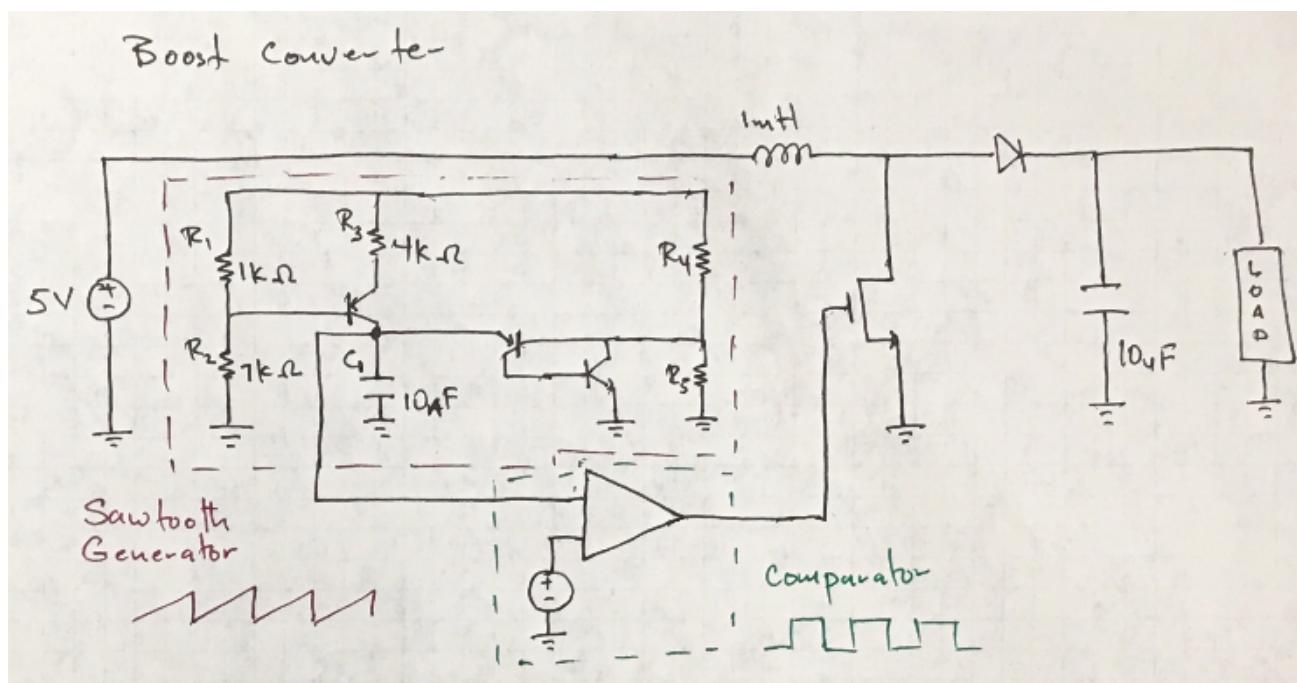


Figure 2. Full design of Booster Circuit with Sawtooth and comparator

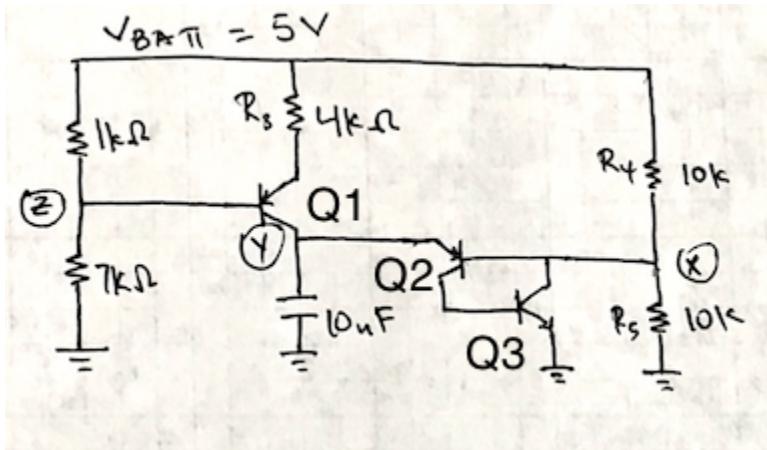


Figure 3. Sawtooth Generator

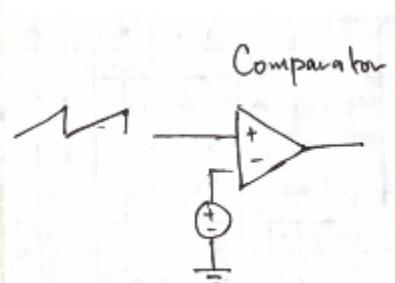


Figure 4. Comparator

### Analysis Calculations:

Calculation for the Sawtooth Generator shown in figure 3.

The value of  $R_1$  and  $R_2$  was determined by using a voltage divider. The goal of these two resistors is to turn ON  $Q_1$ . For the transistor  $Q_1$  to be ON the Base to Emitter voltage must be 0.7V or greater. So solving for  $R_1$  and  $R_2$  is just a simple voltage divider at the base of  $Q_1$ .

$$\text{Equation I: } 0.7V = [R_2/(R_1 + R_2)](5V)$$

Using Equation I, we can easily find the values for  $R_1$  and  $R_2$ , respectively. But since we only need to keep  $Q_1$  ON, we can approximate the range of value for  $R_1$  and  $R_2$  that will produce a voltage at  $V_Z$  that is greater than or equal to 0.7V

Now that transistor  $Q_1$  is turn ON, We needed to store electrical charge in the capacitor. To accomplish this we need to drive a current across the emitter to collect of  $Q_1$ . By adding a resistor  $R_3$  to the emitter of  $Q_1$ , we can control the amount of current in the capacitor.

The current through the capacitor is determine by the equation:

$$\text{Equation II: } i = Cdv/dt$$

Depending on how fast we want the capacitor to charge, we must account for the size on the capacitor. In other words, for bigger size capacitor, we need to a small value for  $R_3$ , and for smaller capacitor, the resistor value need to large. This is due to ohm's law which states

$$\text{Ohm's Law: } V = IR$$

Applying ohm's law to find the current through  $R_3$ , obtained

$$\text{Equation III: } I = (V_{BATT} - V_E)/R_3$$

Equation III shows that smaller values of  $R_3$ , produce a larger current. And larger values on  $R_3$  result in smaller current.

Using these factors and equation II, which states that the current through a capacitor is equal to the capacitance times the change in voltage over time. And we know that the capacitance is determined by the size of the capacitor. This property is shown in the equation IV below

$$C = \frac{\epsilon A}{d}$$

Where,

**C = Capacitance in Farads**

**$\epsilon$  = Permittivity of dielectric (absolute, not relative)**

**A = Area of plate overlap in square meters**

**d = Distance between plates in meters**

We decided to use a large resistance  $R_3 = 4k$  for a capacitor value of  $C_1 = 10nF$ . Our decisions were based on equation II -- IV.

The value on  $R_4$  and  $R_5$  was also determined using a voltage divider. We needed the voltage at node X to be 0.7V or greater. This was accomplished by using equation I, and substituting  $R_5$  for  $R_2$ , and  $R_4$  for  $R_1$ .

### The Frequency of the Sawtooth

$$V_{breakdown} = 8.7V \rightarrow 3\% \quad (8.7 \text{ -- } 8.65)$$

Using the equation derived in during lecture:

$$\text{Energy in a capacitor : } C_{CAP} = 1/2 * CV^2$$

$$E_{INITIAL} = (1/2)(10u)(8.7)^2 = 378.45uJ$$

$$E_{FINAL} = (1/2)(10u)(8.65)^2 = 374.1uJ$$

$$\Delta E = 4.35uJ$$

Using the energy of capacitor to find  $T_{on/off}$  from the inductor energy:

$$E_{inductor} = (1/2)Lt^2 \quad \rightarrow \quad i^2 = \Delta t^2 = (V_{BATT}/L * \Delta t)^2$$

$$16.2u = (1/2)(Im)(V_{BATT}/L * \Delta t)^2$$

$$16.2u = (1/2)(Im)(5/1m * \Delta t)^2$$

Solve for  $\Delta t = 36usec = T_{on}$

To find time off:  $V_{breakdown} = V_{BATH}(1 + T_{on}/Toff)$

$$8.7V = 5V(1 + 36u/Toff)$$

Solve for  $Toff = 48.648usec$

$$T_{total} = T_{on} + T_{off} = 84.648usec$$

$$f = 1/T_{total} = 11.8kHz$$

To find the percentage in which we need to divide the  $V_{breakdown}$  by for the negative terminator voltage of the comparator. We used the equation shown below

$$T_{on}/T_{total} = 74\%$$

### Simulations:

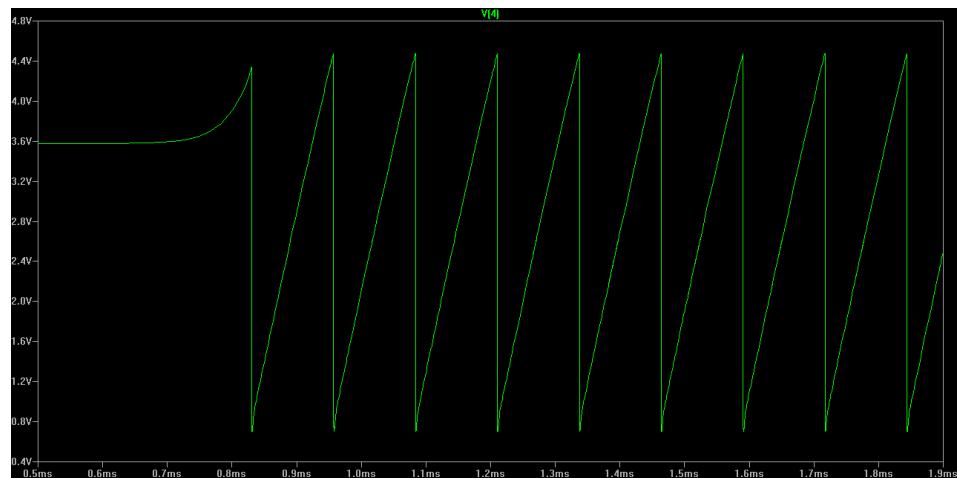


Figure 5. The Sawtooth Generator output

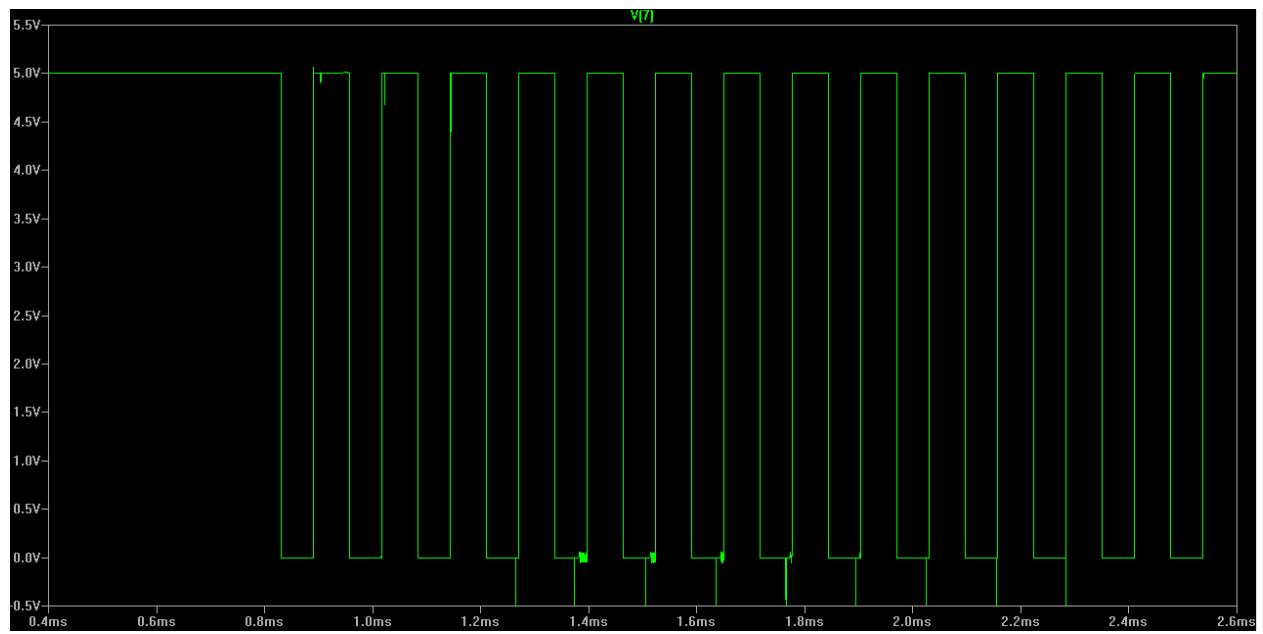


Figure 6. The Comparator Output

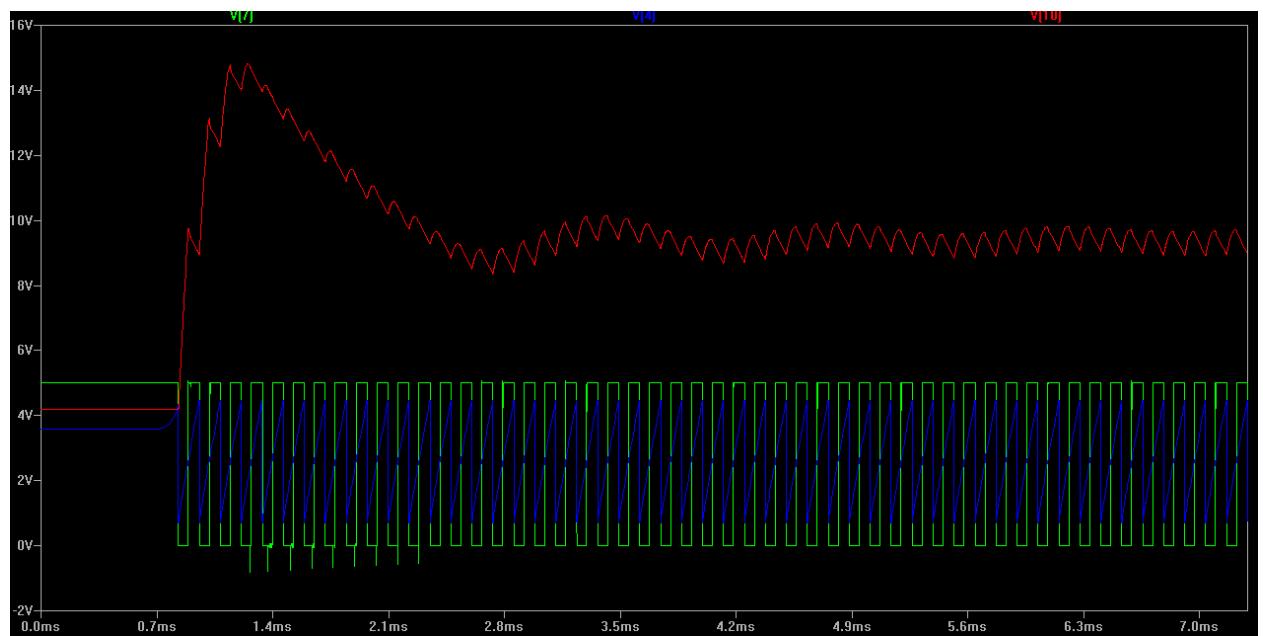


Figure 7. The red plot shows the boost converter output voltage. The blue is the same as fig.5 and the green is the same as fig. 6

## Experiments:

The building of the sawtooth circuit was not as straightforward as the LTSpice simulation. After building the circuit, the sawtooth display on the oscilloscope was completely different than our actual design in terms of frequency. This was due to not having the exact capacitor value and there being a margin of error when it came to the resistor values. Since the capacitor is very small, it's very sensitive to change in current being dump into it, see equation III and IV. Note, since node X, and Z depend on  $V_{BATT}$ , if the voltage drop across its resistor, respectively. This affects the voltage at those node. Therefore, adjusting the value of  $R_3$  is required to configure the value of  $R_1, R_2, R_4$ , and  $R_5$ .

Due to these facts, we reconfigured the resistors and capacitor values in Netlist (LTSpice). Changing  $R_1 = 1k$ ,  $R_2 = 7k$ ,  $R_3 = 5K$ ,  $R_5 = 5.537k$ , and  $C_1 = 200pF$  these values were based on the understanding of Equation III and IV which state that if  $R_3$  increases  $C_1$  must decrease and versa visa. And using Equation I (voltage divider) we could approximate values for  $R_1, R_2, R_4$ , and  $R_5$  that will keep node X and node Z greater than or equal to 0.7V. We adjusted the negative input voltage of the comparator to about 50% of  $V_{BATT}$ . This work both on the simulation and on the breadboard. Figure 5, shows the square generated with the negative terminal of the comparator at 2.5V.

## Discussion:

The goal of boost converter is to boost small input voltage and produce large output voltage. This is accomplish as such, when a High frequency square wave is applied to the NMOS Gate at startup, see figure 1. During this time the NMOS conducts, placing a short circuit which allow current to flow from  $V_{BATT}$  through the inductor  $L_1$  and through the NMOS and to ground. Therefore, there is virtually no current flowing in the remainder of the circuit.

During the Low period of the switching square wave cycle. The NMOS is rapidly turned off and the sudden drop in current across  $L_1$  produces a back emf in the opposite polarity to the voltage across  $L_1$  during the ON period, to keep current flowing. This results in two voltages, the supply voltage  $V_{BATT}$  and the back e.m.f across  $L_1$  in series with each other.

This higher voltage ( $V_{BATT} + V_{L(inductor)}$ ), now that there is no current path through the NMOS, forward biases  $D_1$ . The resulting current through  $D_1$  charges up  $C_1$  to  $V_{BATT} + V_L$  minus the small forward voltage drop across  $D_1$ , and also supplies the load.

The circuit action during NMOS ON (High frequency square wave) periods after the initial start up. Each time the NMOS conducts, the cathode of  $D_1$  is more positive than its anode, due to the charge on  $C_1$ .  $D_1$  is therefore turned off so the output of the circuit is isolated from the input, however the load continues to be supplied with  $V_{BATT} + V_L$  from the charge on  $C_1$ . Although the charge  $C_1$  drains away through the load during this period,  $C_1$  is recharged each time the NMOS switches off, so maintaining an almost steady output voltage across the load.

To produce the square wave which turned the NMOS ON and OFF. We designed a Sawtooth Generator (see figure 5) and passed its output into a comparator to produce a square wave. Figure 3, was used to generate the sawtooth and this is accomplished by using a current source with  $R_1$  and  $R_2$  which set up a bias voltage on the PNP transistor  $Q_1$ . Resistor  $R_3$  is producing a current and that is dumping into the capacitor which produces a linear voltage ramp/slope as the capacitor charge, this is due to Equation II.

Once the capacitor is charged. To discharge the capacitor and start the process over, we added  $Q_2$  and  $Q_3$  structure/connection of which is a positive feedback like circuit. Once it's turned on, its ( $Q_2$  and  $Q_3$  structure) stays on until it gets starved of current or get shut off. When the capacitor gets charged to the point where it turns the base-emitter junction of  $Q_2$  ON. The PNP  $Q_2$  transistor starts conducting. The collector current of  $Q_2$  becomes base current of  $Q_3$  (NPN transistor), turning it ON. Once  $Q_3$  is turned on, the collector current starts pulling current both from the base of  $Q_2$  and Node X.

By pulling current from the base of  $Q_2$ , we are turning  $Q_2$  on harder and that basically just reinforces both  $Q_2$  and  $Q_3$  to stay turn-on. What happens is when  $Q_2$  and  $Q_3$  is turned on both really hard,  $Q_3$ 's collector gets pulled toward ground which saturates  $Q_3$ . Since  $Q_1$  is an emitter follower, it also pulls down Node Y, discharging the capacitor. Once the capacitor is discharged,  $Q_2$  and  $Q_3$  structure/connection shut itself off because there is no current available to keep it conducting. When shutoff, the process repeats itself. The capacitor gets charged again until it hits threshold and starts over.

The working of our complete boost converter with  $I_{load}$  attached is shown in figure 7. The red plot shows the booster circuit producing voltage in the range from 8.3V - 9.5V. This plot showed that our circuit works and the completion of part II of this project.