UNIVERSITATEA TEHNICĂ DIN CLUJ-NAPOCA

Procesorul MIPS Pipeline

MOȘILĂ LUCIANA

30226

ARHITECTURA CALCULATOARELOR

2023

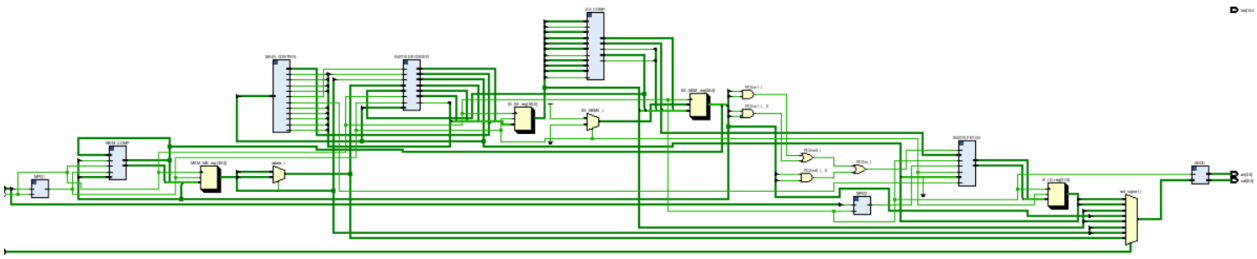
```
B"001_000_001_0000000",
B"001_000_010_0000001",
B"001_000_011_0000101",
B"001_000_100_0000000",
B"000_000_000_000_0_000",
B"100_001_011_0000100",
B"000_000_000_000_0_000",
B"000_100_010_100_0_000",
B"001_010_010_0000010",

B"001_001_001_0000001",
B"111_0000000000100",
B"011_000_100_0010100",
```

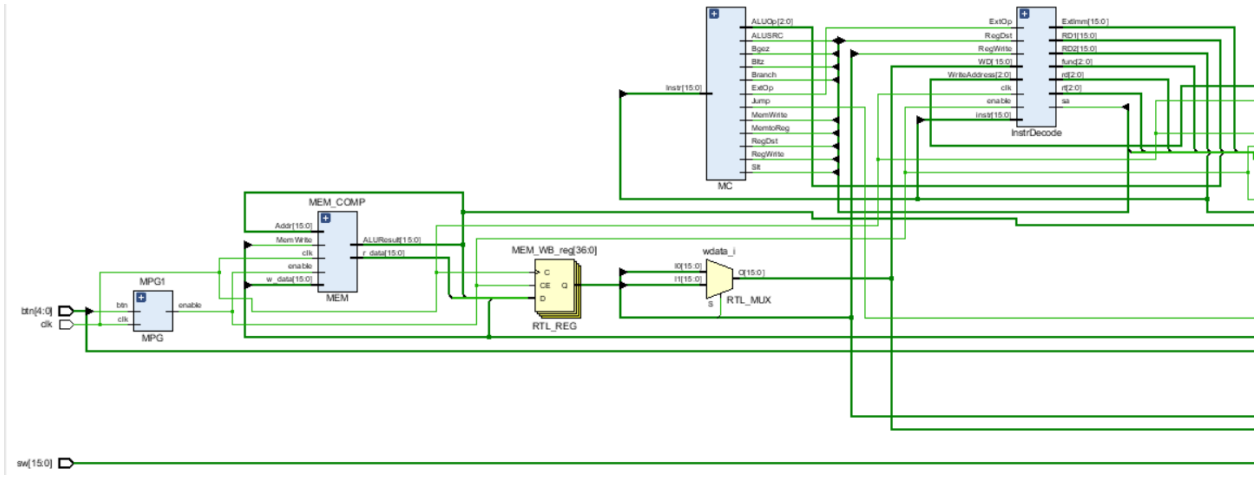
Analizarea hazardurilor

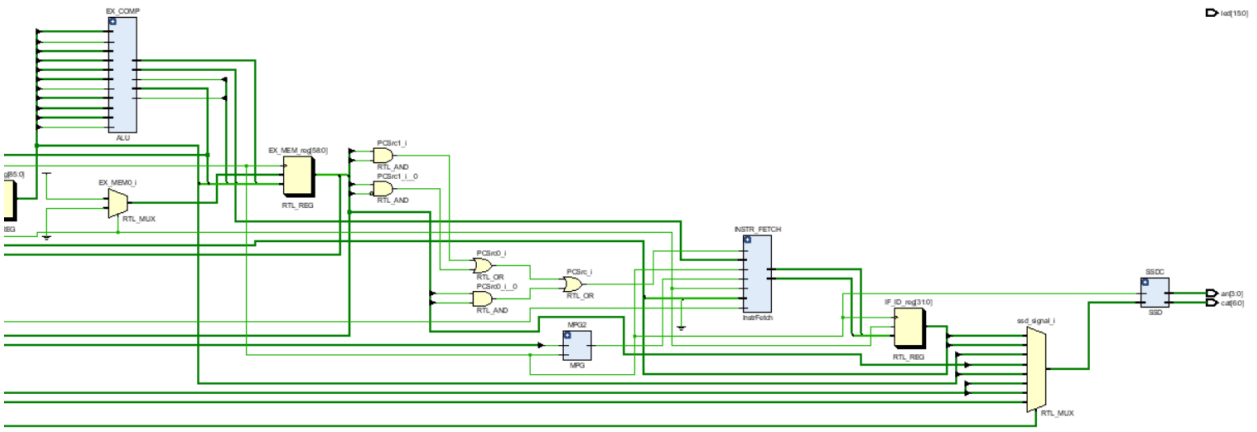
Instr/Clk	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
addi $1, $0, 0	IF	ID	EX	MEM	WB($1)									
addi $2, $0, 1		IF	ID	EX	MEM	WB($2)								
addi $3, $0, 5			IF	ID	EX	MEM	WB($3)							
addi $4, $0, 0				IF	ID	EX	MEM	WB($4)						
beq $1, $3, 4					IF	ID($1,$3)	EX	MEM	WB					
add $4, $2, $4						IF	ID($2,$4)	EX	MEM	WB($4)				
addi $2, $2, 2							IF	ID($2)	EX	MEM	WB($2)			
addi $1, $1, 1								IF	ID($1)	EX	MEM	WB($1)		
j 4									IF	ID	EX	MEM	WB	
sw $4, 20($0)										IF	ID($4)	EX	MEM	WB

Instr. Nr.	Program
0	addi $1, $0, 0
1	addi $2, $0, 1
2	addi $3, $0, 5
3	addi $4, $0, 0
4	beq $1, $3, 4
5	add $4, $2, $4
6	addi $2, $2, 2
7	addi $1, $1, 1
8	j 4
9	sw $4, 20($0)

Programul original







Testarea nu a fost efectuata pe placuta FPGA.

Tabel cu descrierea regiștrilor

REG_IF_ID(31 – 0)	REG_ID_EX(85 – 0)	REG_EX_MEM(58 – 0)	REG_MEM_WB(36 – 0)
Instruction(31 – 16)	RegDst(0)	MemtoReg(0)	MemtoReg(0)
PC + 1(15 – 0)	ALUSrc(1)	RegWrite(1)	RegWrite(1)
	Branch(2)	MemWrite(2)	ReadData(17 – 2)
	Bgez(3)	Branch(3)	ALURes(33 – 18)
	Bltz(4)	Bgez(4)	WriteAddress(36 – 34)
	Slt(5)	Bltz(5)	
	ALUOp(8 – 6)	BranchAddress(21 – 6)	
	MemWrite(9)	Zero(22)	
	MemtoReg(10)	Sign(23)	
	RegWrite(11)	ALURes(39 – 24)	
	sa(12)	RD2(55 – 40)	
	PC + 1(28 – 13)	WriteAddress(58 – 56)	
	RD1(44 – 29)		
	RD2(60 – 45)		
	ExtImm(76 – 61)		
	Func(79 – 77)		
	rt(82 – 80)		
	rd(85 – 83)		