Microcontroller Engineering
TMIK13
Lecture 13

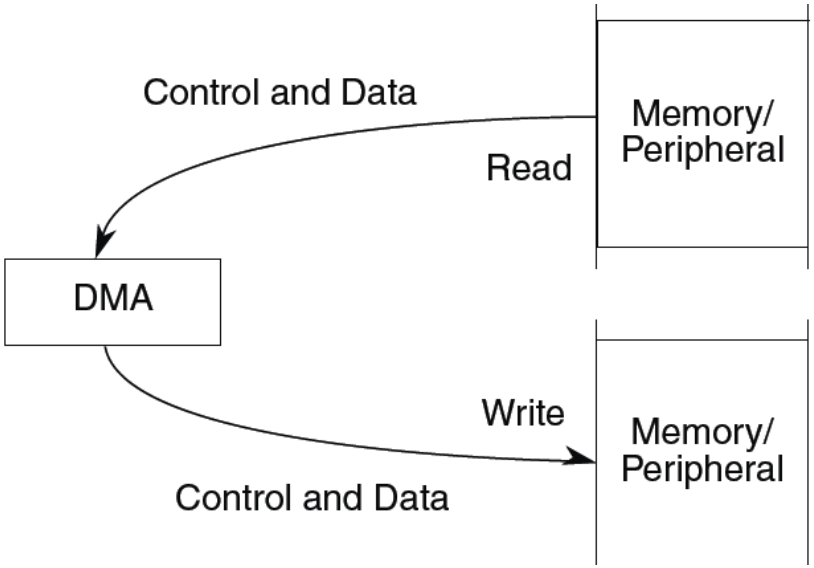
DIRECT MEMORY ACCESS (DMA)

ANDREAS AXELSSON (ANDREAS.AXELSSON@JU.SE)

DMA – Basic Concepts

Hardware which reads data from a source and writes it to a destination

- Can copy data quickly
- Can eliminate ISRs which just copy data (e.g. unload UART receive buffer into queue)

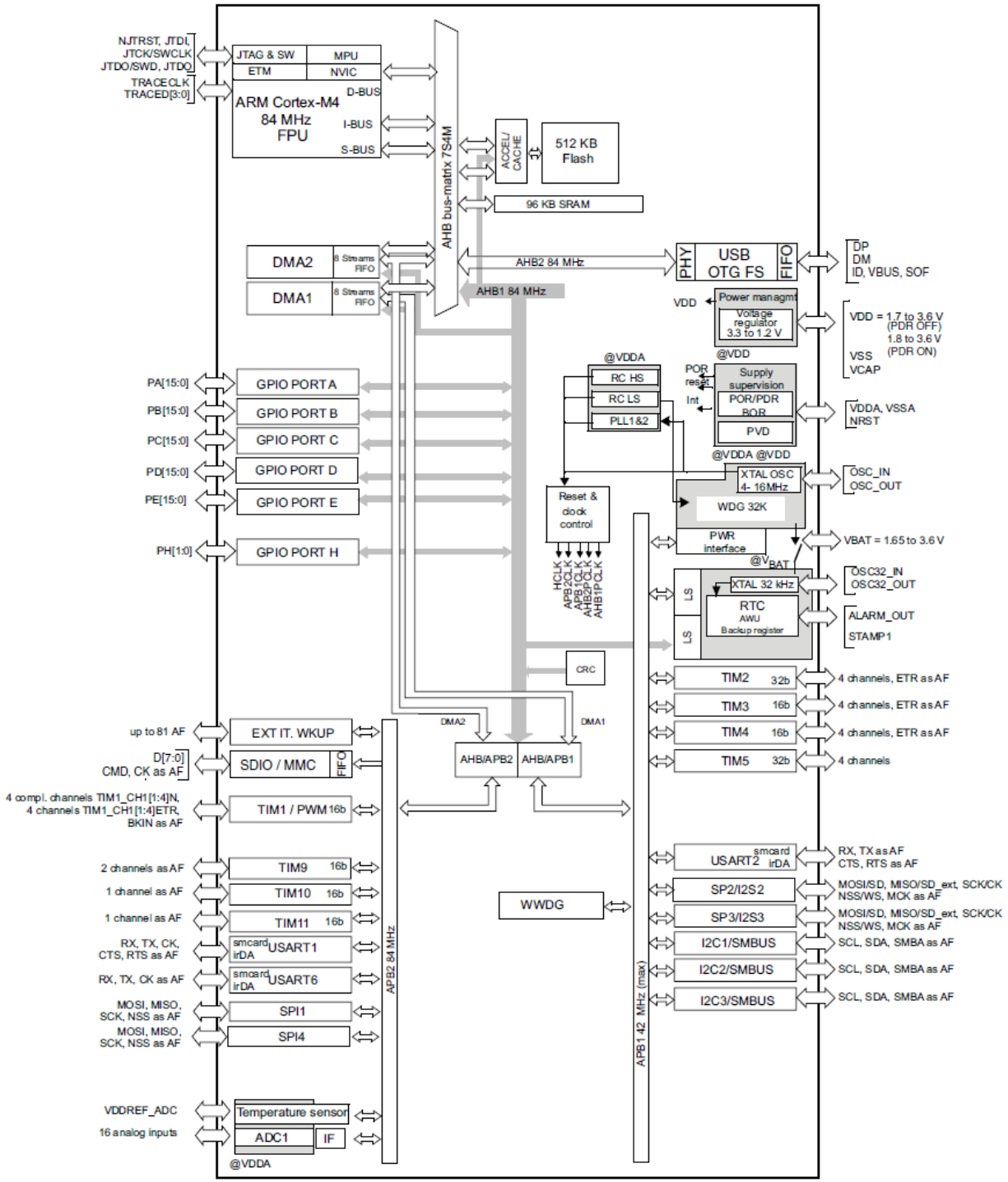


Various configurable options

- Number of data items to copy
- Source and destination addresses can be fixed or change (e.g. increment, decrement)
- Size of data item
- When transfer starts

Operation

- Initialization: Configure controller
- Transfer: Data is copied
- Termination: Channel indicates transfer has completed


NJTRST, JTDI, JTCK/SWCLK JTDO/SWD, JTDO
TRACECLK TRACED[3:0]
JTAG & SW
MPU
ETM
NVIC
ARM Cortex-M4 84 MHz FPU
D-BUS
I-BUS
S-BUS
AHB bus-matrix 7S4M
ACCEL/ CACHE
512 KB Flash
96 KB SRAM
DMA2
DMA1
8 Streams FIFO
AHB2 84 MHz
AHB1 84 MHz
PHY
USB OTG FS
FIFO
DP
DM
ID, VBUS, SOF
VDD
Power managmt
Voltage regulator 3.3 to 1.2 V
@VDD
VDD = 1.7 to 3.6 V (PDR OFF) 1.8 to 3.6 V (PDR ON)
VSS
VCAP
@VDDA
RC HS
RC LS
PLL1&2
POR reset
Int
Supply supervision
POR/PDR BOR
PVD
@VDDA @VDD
VDDA, VSSA
NRST
PA[15:0]
PB[15:0]
PC[15:0]
PD[15:0]
PE[15:0]
PH[1:0]
GPIO PORT A
GPIO PORT B
GPIO PORT C
GPIO PORT D
GPIO PORT E
GPIO PORT H
Reset & clock control
XTAL OSC 4- 16MHz
WDG 32K
PWR interface
@VBAT
VBAT = 1.65 to 3.6 V
OSC_IN
OSC_OUT
HCLK
APB2CLK
APB2PCLK
AHB2PCLK
AHB1PCLK
LS
XTAL 32 kHz
RTC
AWU
Backup register
OSC32_IN
OSC32_OUT
ALARM_OUT
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TIM2 32b
TIM3 16b
TIM4 16b
TIM5 32b
4 channels, ETR as AF
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DMA2
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up to 81 AF
EXT IT. WKUP
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TIM9 16b
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RX, TX, CK, CTS, RTS as AF
smcard irDA USART1
RX, TX, CK as AF
smcard irDA USART6
MOSI, MISO, SCK, NSS as AF
SPI1
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SPI4
APB2 84 MHz
WWDG
USART2 smcard irDA
RX, TX as AF
CTS, RTS as AF
SP2/I2S2
MOSI/SD, MISO/SD_ext, SCK/CK NSS/WS, MCK as AF
SP3/I2S3
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I2C1/SMBUS
SCL, SDA, SMBA as AF
I2C2/SMBUS
SCL, SDA, SMBA as AF
I2C3/SMBUS
SCL, SDA, SMBA as AF
APB1 42 MHz (max)
VDDREF_ADC
16 analog inputs
Temperature sensor
ADC1
IF
@VDDA

Basic Use of DMA

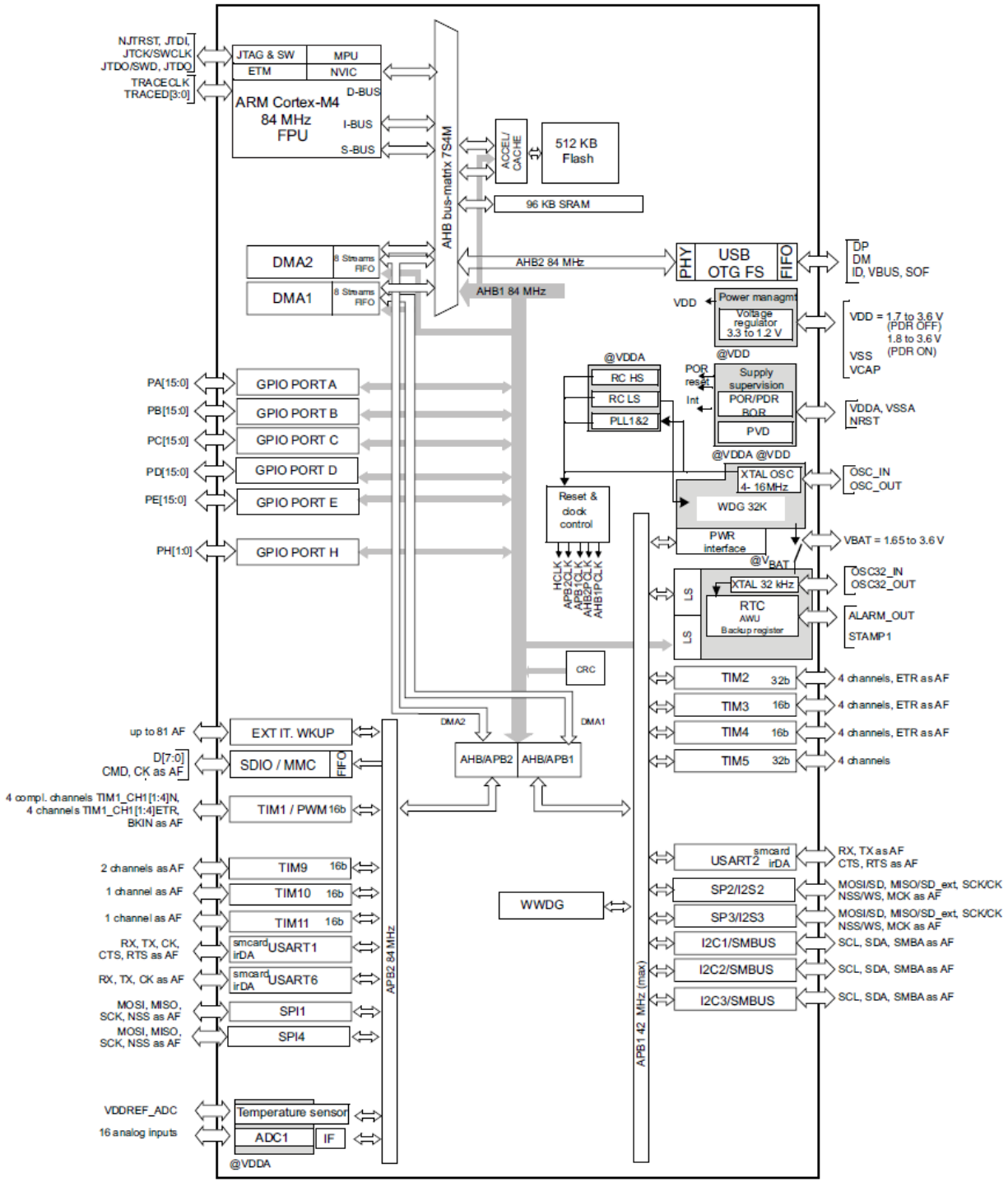
Configuration

- Enable clock to DMA module
- Initialize control registers
- Load SARn with source address
- Load DARn with destination address
- Load BCRn with number of bytes to transfer
- Clear DSRn[DONE]

Start transfer by setting DCRn[START]

Wait for end of transfer

- Interrupt generated if DCRn[EINT] is set (DMAn_IRQHandler)
- Or else poll DSRn[DONE]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USART2 smcard irDA
RX, TX as AF
CTS, RTS as AF
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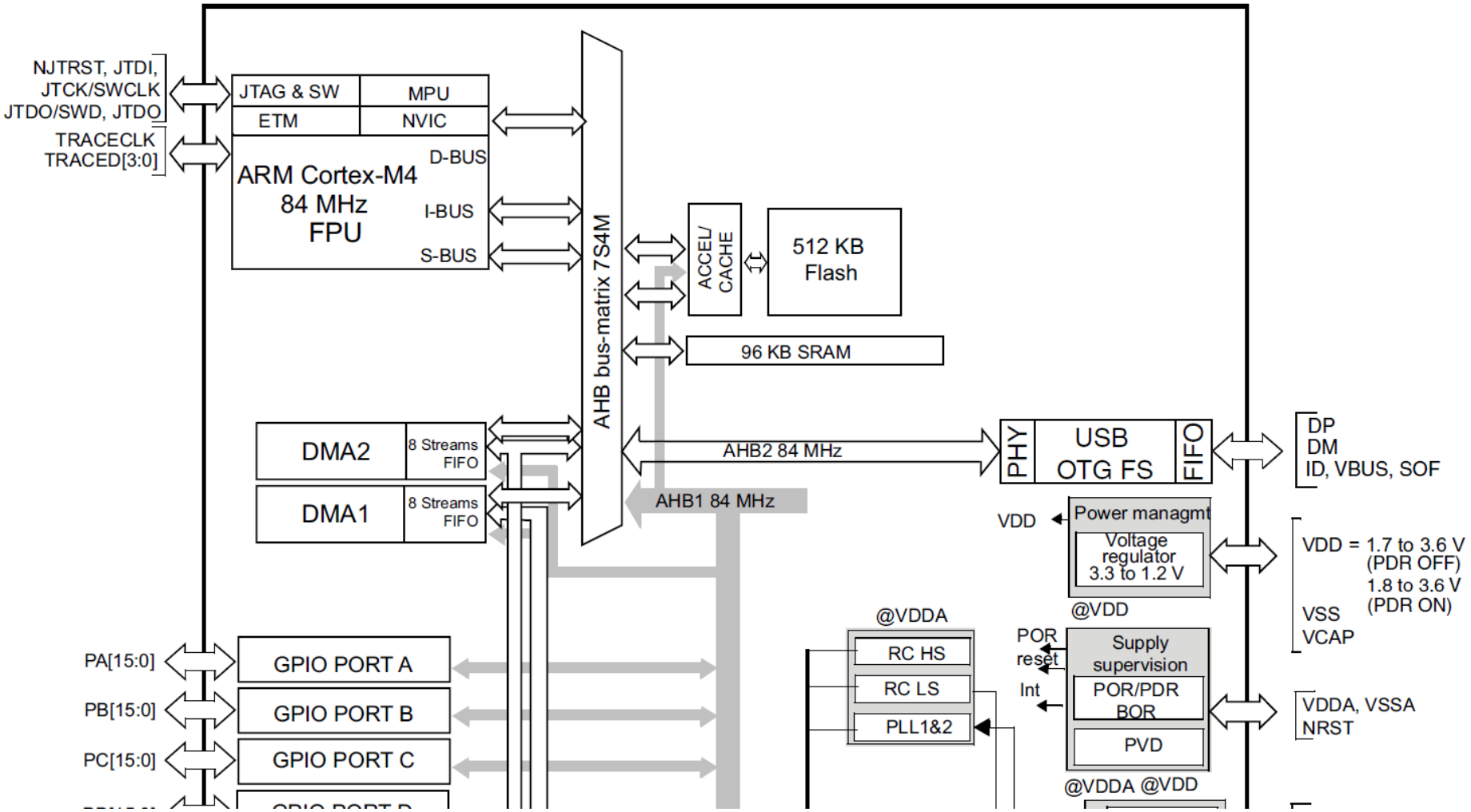
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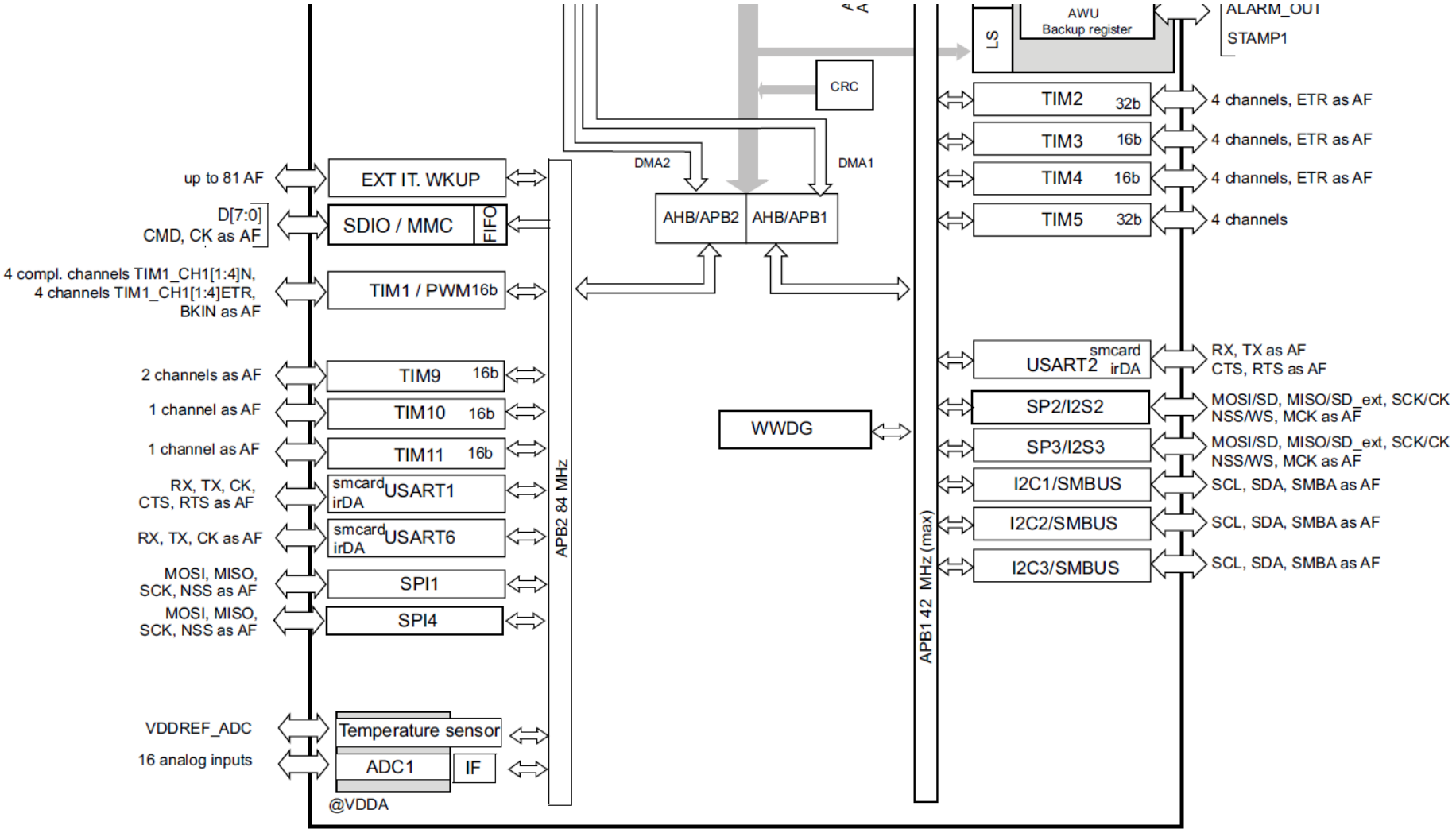
PB[15:0]
GPIO PORT B
PC[15:0]
GPIO PORT C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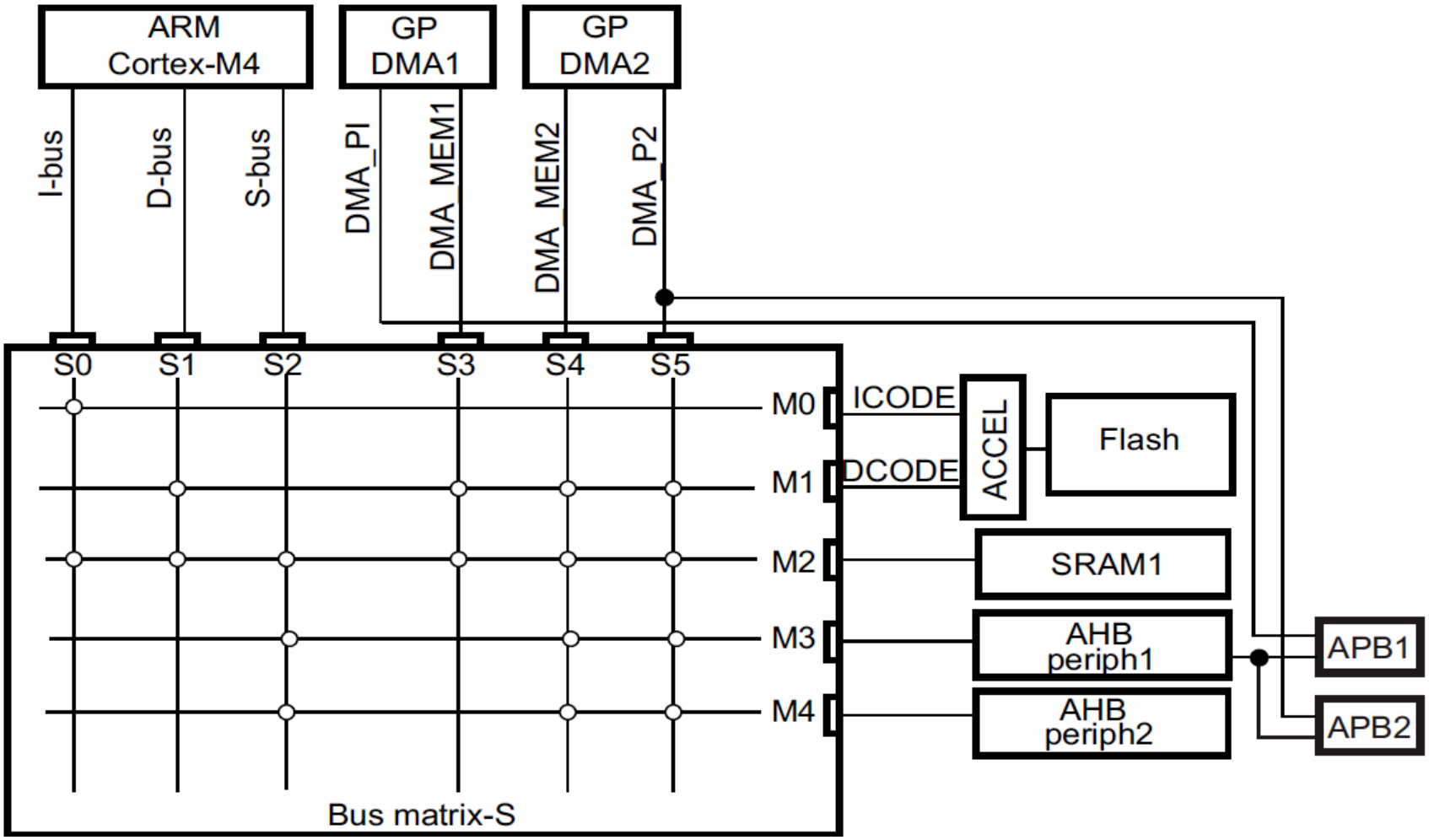
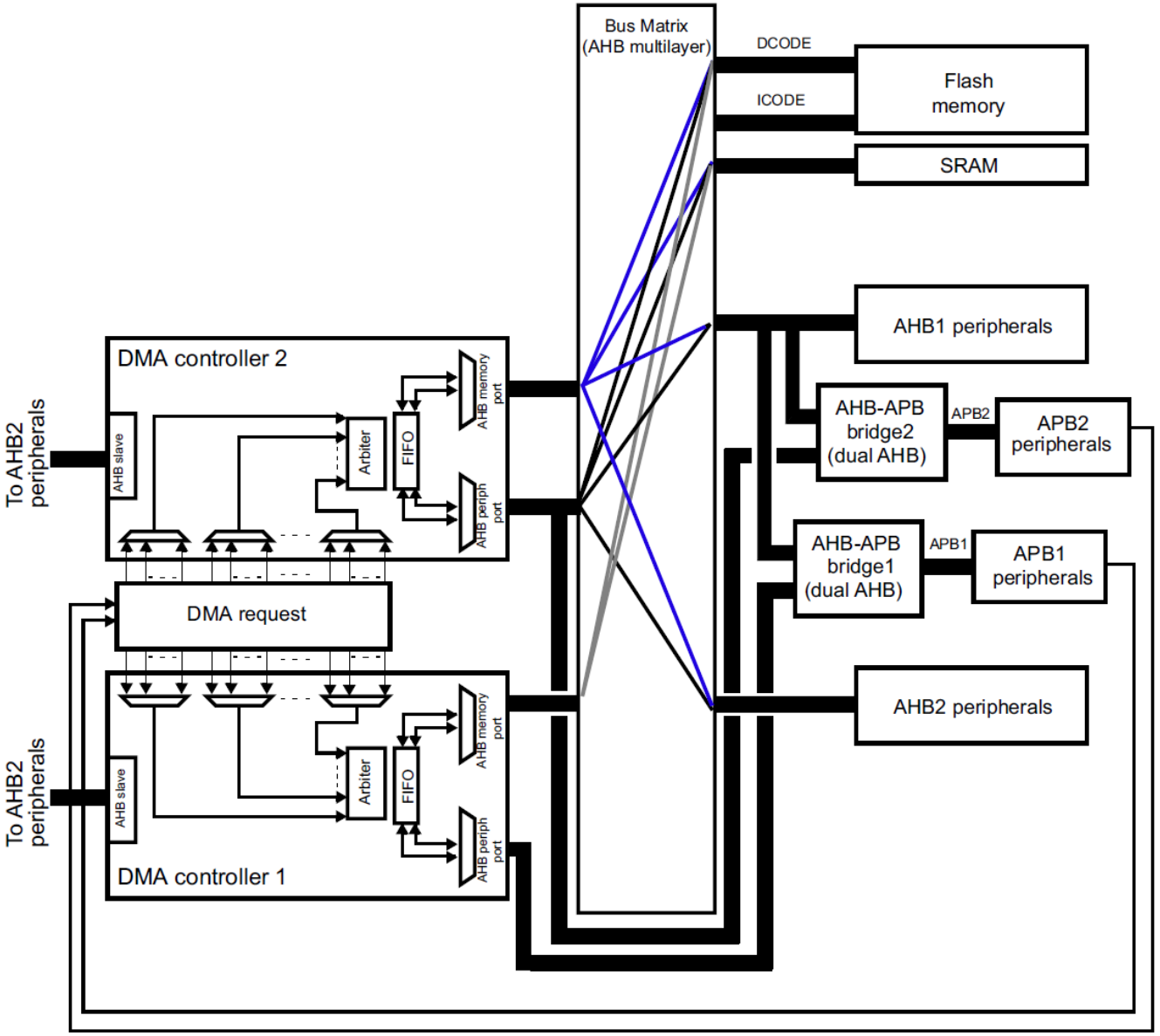
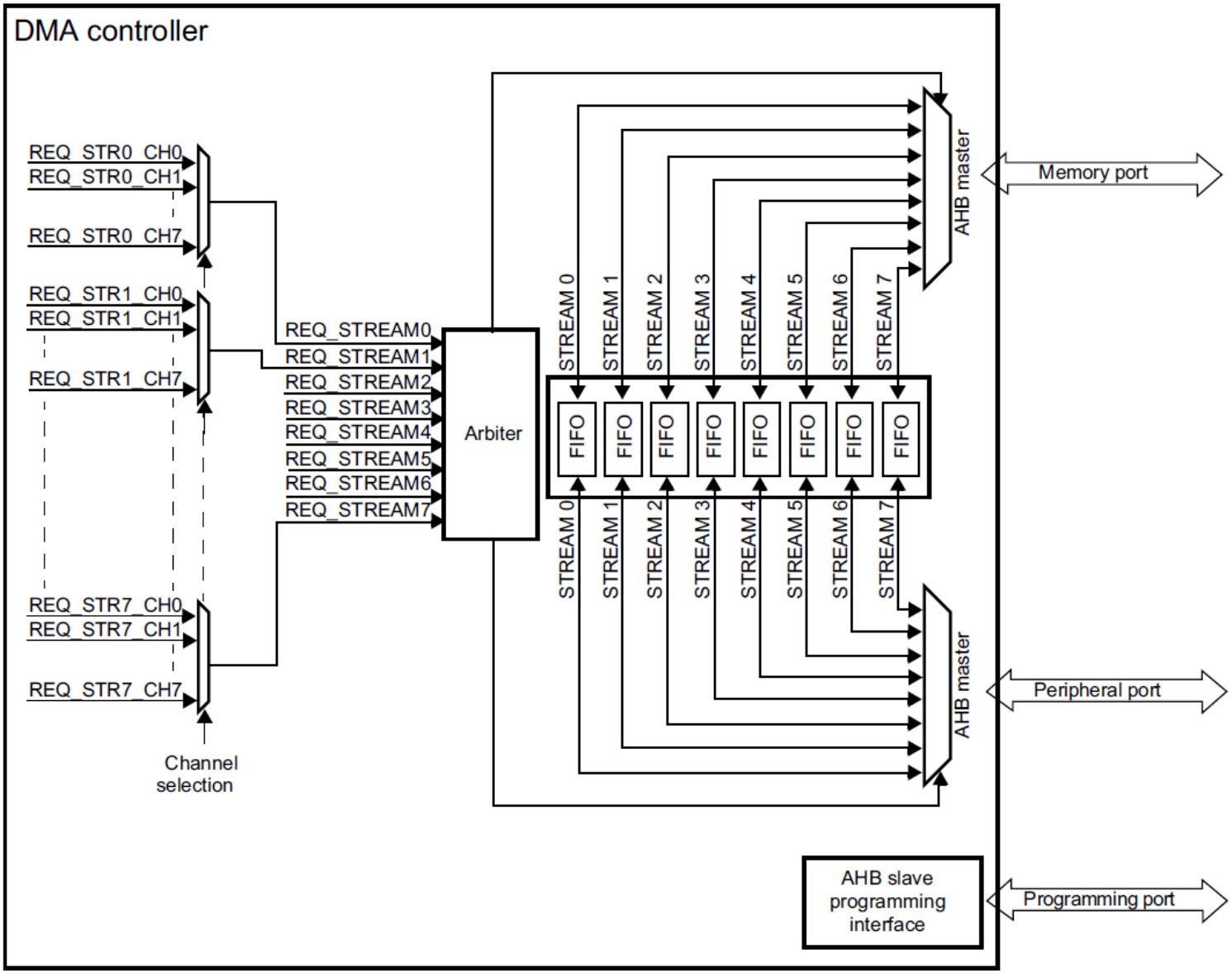
System Bus Architecture



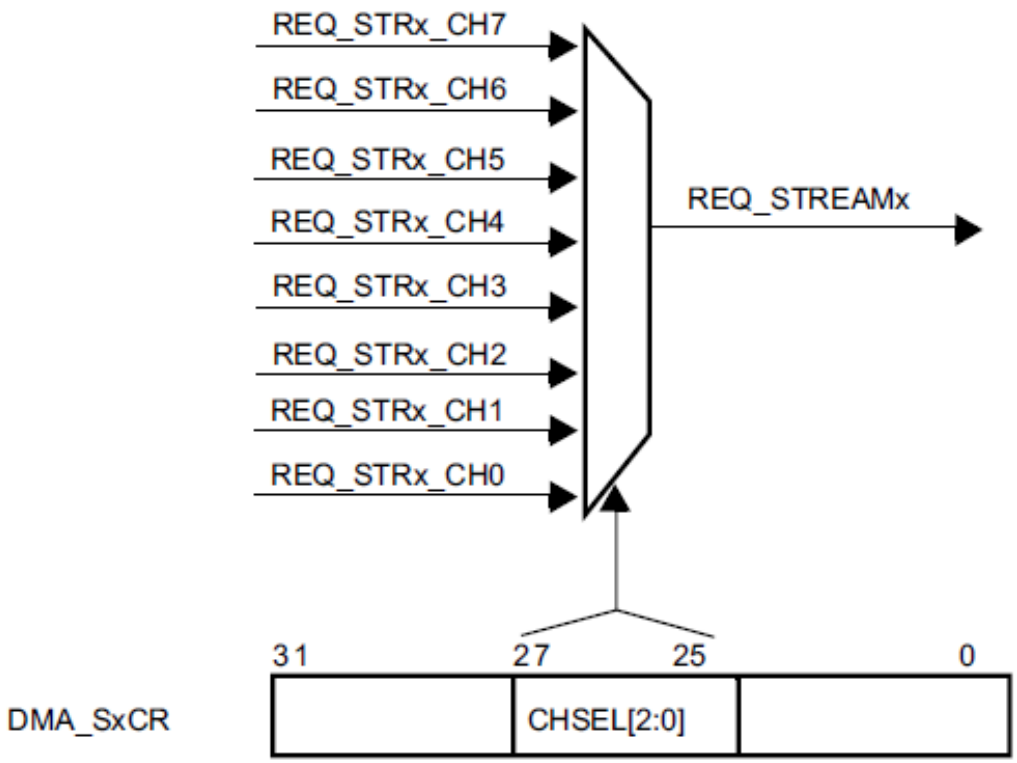
Overview DMA – STM32F401



DMA Controller – STM32F401



Channel Selection



Channel Sources – DMA1

Table 28. DMA1 request mapping (STM32F401xB/C and STM32F401xD/E)

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
Channel 0	SPI3_RX	-	SPI3_RX	SPI2_RX	SPI2_TX	SPI3_TX	-	SPI3_TX
Channel 1	I2C1_RX	I2C3_RX	-	-	-	I2C1_RX	I2C1_TX	I2C1_TX
Channel 2	TIM4_CH1	-	I2S3_EXT_RX	TIM4_CH2	I2S2_EXT_TX	I2S3_EXT_TX	TIM4_UP	TIM4_CH3
Channel 3	I2S3_EXT_RX	TIM2_UP TIM2_CH3	I2C3_RX	I2S2_EXT_RX	I2C3_TX	TIM2_CH1	TIM2_CH2 TIM2_CH4	TIM2_UP TIM2_CH4
Channel 4	-	-	-	-	-	USART2_RX	USART2_TX	-
Channel 5	-	-	TIM3_CH4 TIM3_UP	-	TIM3_CH1 TIM3_TRIG	TIM3_CH2	-	TIM3_CH3
Channel 6	TIM5_CH3 TIM5_UP	TIM5_CH4 TIM5_TRIG	TIM5_CH1	TIM5_CH4 TIM5_TRIG	TIM5_CH2	I2C3_TX	TIM5_UP	-
Channel 7	-	-	I2C2_RX	I2C2_RX	-	-	-	I2C2_TX

Channel Sources – DMA2

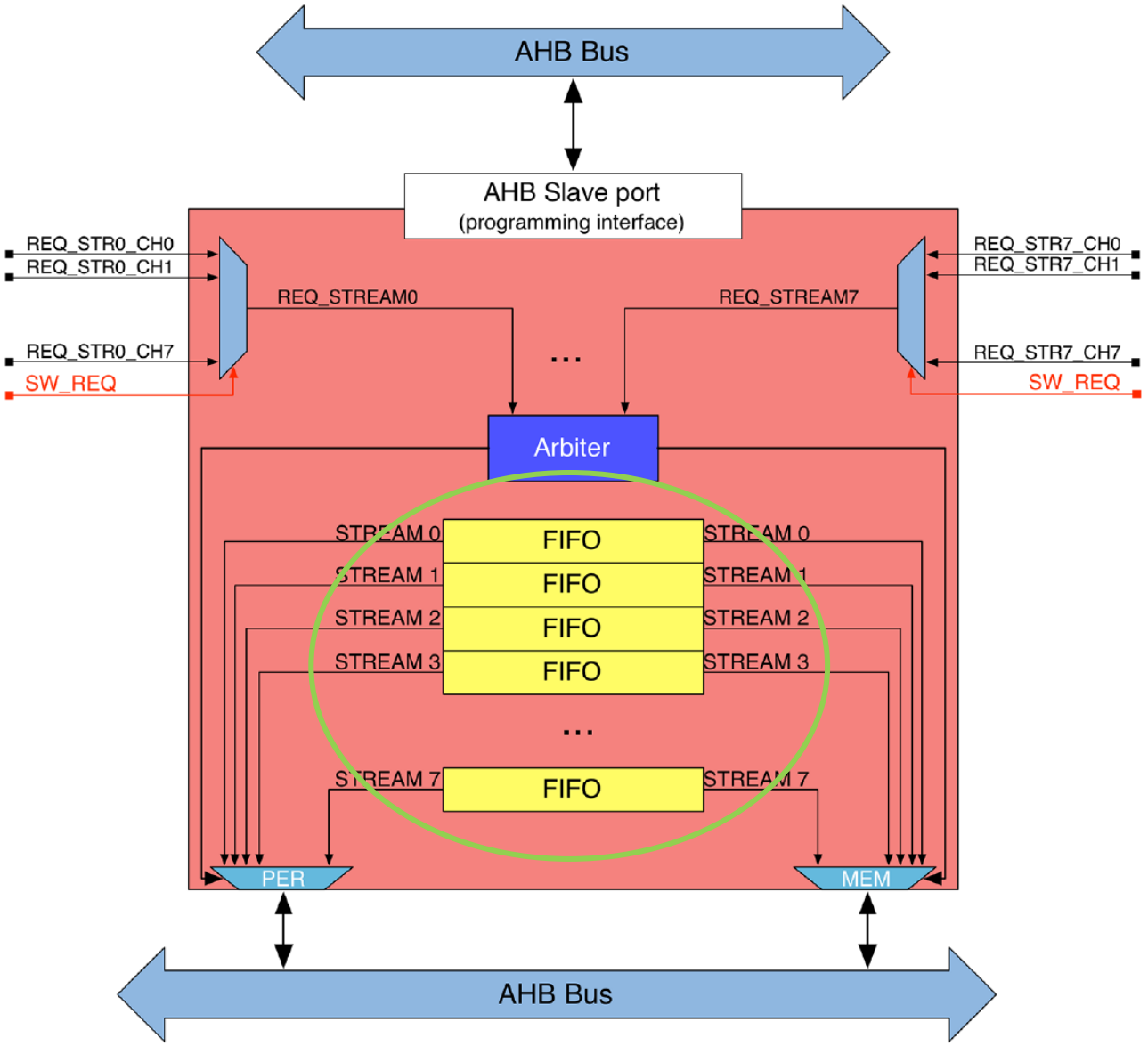
Table 29. DMA2 request mapping (STM32F401xB/C and STM32F401xD/E)

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
Channel 0	ADC1	-	-	-	ADC1	-	TIM1_CH1 TIM1_CH2 TIM1_CH3	-
Channel 1	-	-	-	-	-	-	-	-
Channel 2	-	-	-	-	-	-	-	-
Channel 3	SPI1_RX	-	SPI1_RX	SPI1_TX	-	SPI1_TX	-	-
Channel 4	SPI4_RX	SPI4_TX	USART1_RX	SDIO	-	USART1_RX	SDIO	USART1_TX
Channel 5	-	USART6_RX	USART6_RX	SPI4_RX	SPI4_TX	-	USART6_TX	USART6_TX
Channel 6	TIM1_TRIG	TIM1_CH1	TIM1_CH2	TIM1_CH1	TIM1_CH4 TIM1_TRIG TIM1_COM	TIM1_UP	TIM1_CH3	-
Channel 7	-	-	-	-	-	-	-	-

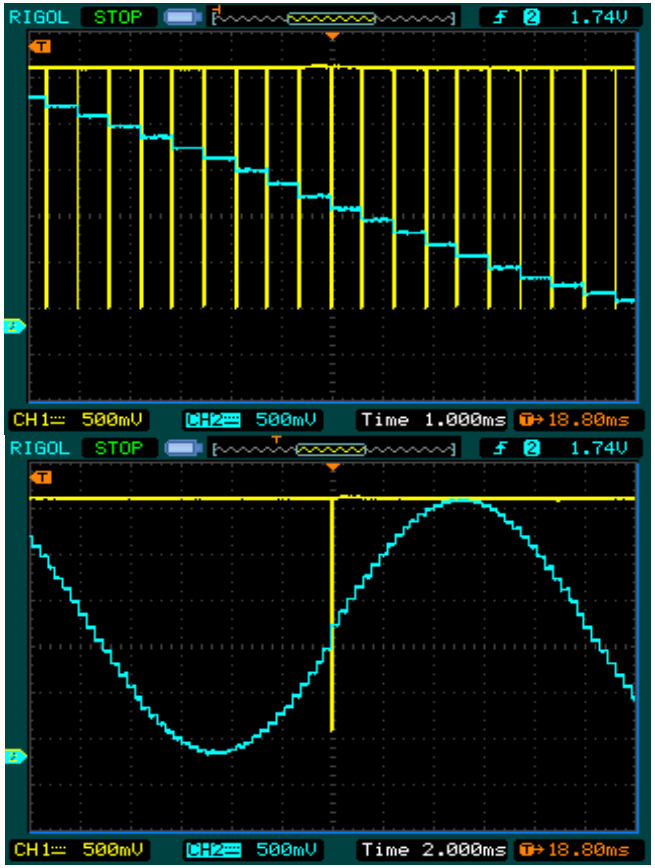
Stream Control Registers

0x0010	**DMA_S0CR**	Reserved			CHSEL[2:0]			MBURST[1:0]		PBURST[1:0]		Reserved	CT	DBM	PL[1:0]		PINCOS	MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR[1:0]		PFCTRL	TCIE	HTIE	TEIE	DMEIE	EN
	Reset value				0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0014	**DMA_S0NDTR**	Reserved															NDT[15:.]															
	Reset value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0018	**DMA_S0PAR**	PA[31:0]																														
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x001C	**DMA_S0M0AR**	M0A[31:0]																														
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0020	**DMA_S0M1AR**	M1A[31:0]																														
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0024	**DMA_S0FCR**	Reserved																										FEIE	Reserved	FS[2:0]			DMDIS	FTH [1:0]	
	Reset value																											0		1	0	0	0	0	1

DMA – Direct and FIFO Mode



Performance Comparison



Traces

- Yellow: ISR is executing when trace is low
- Blue: DAC output (PTE30, pin 11 of J10)

Without DMA: Interrupt per sample

- 4.7 microseconds per 620 microseconds
- 0.758% of processor's time

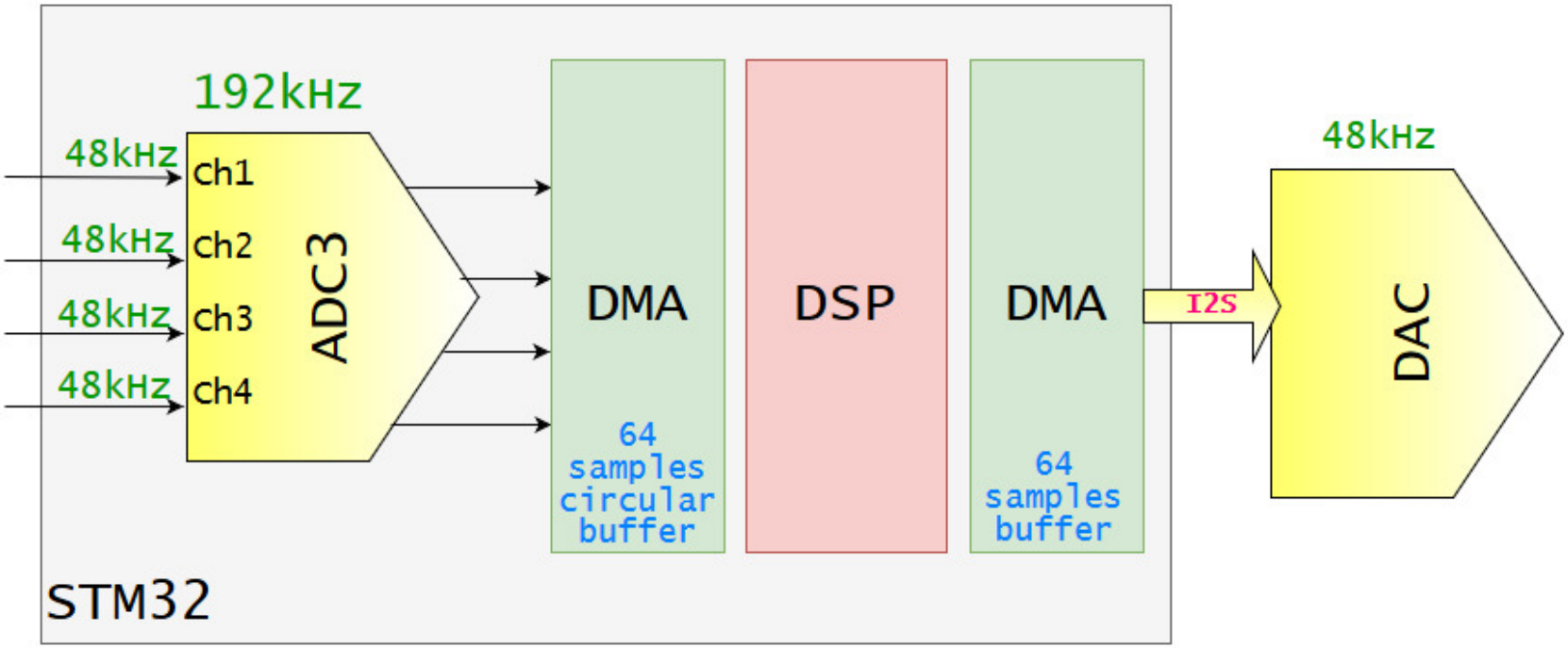
With DMA: Interrupt per cycle

- 5.0 microseconds per 20 milliseconds
- 0.025% of processor's time

How is this useful?

- Saves CPU time
- Reduces timing vulnerability to interrupts being disabled
- Enables CPU to sleep longer, wake up less often
  (20 milliseconds vs. 620 microseconds)

Application – Sound Processing



WS2812B

Intelligent control LED integrated light source

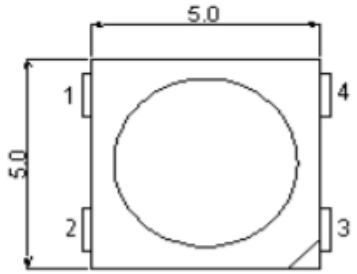
Features and Benefits

- Intelligent reverse connect protection, the power supply reverse connection does not damage the IC.
- The control circuit and the LED share the only power source.
- Control circuit and RGB chip are integrated in a package of 5050 components, form a complete control of pixel point.
- Built-in signal reshaping circuit, after wave reshaping to the next driver, ensure wave-form distortion not accumulate.
- Built-in electric reset circuit and power lost reset circuit.
- Each pixel of the three primary color can achieve 256 brightness display, completed 16777216 color full color display, and scan frequency not less than 400Hz/s.
- Cascading port transmission signal by single line.
- Any two point the distance more than 5m transmission signal without any increase circuit.
- When the refresh rate is 30fps, cascade number are not less than1024 points.
- Send data at speeds of 800Kbps.
- The color of the light were highly consistent, cost-effective..

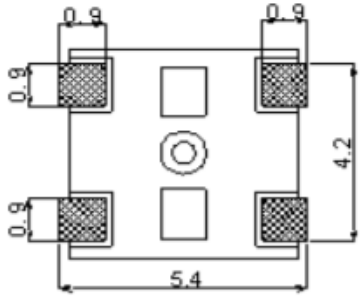
Applications

- Full-color module, Full color soft lights a lamp strip.
- LED decorative lighting, Indoor/outdoor LED video irregular screen.

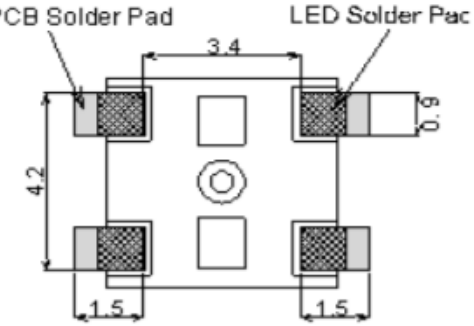
Mechanical Dimensions



Top View

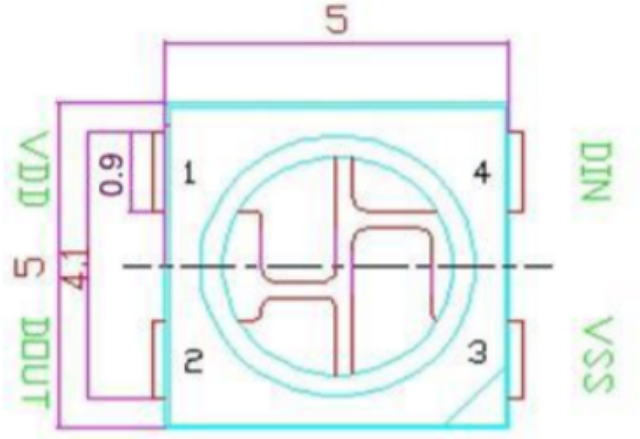


Back View



Solder Pad

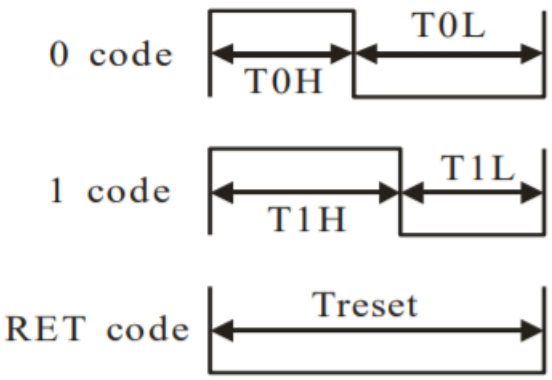
PIN configuration

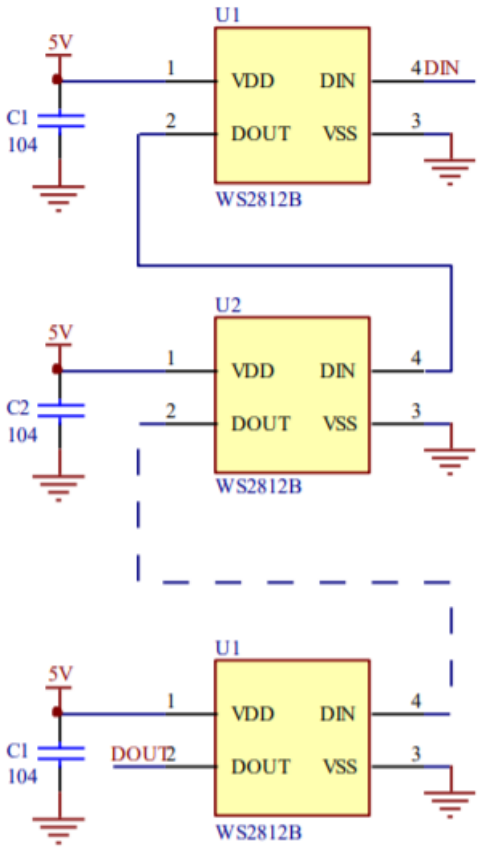


PIN function

NO.	Symbol	Function description
1	VDD	Power supply LED
2	DOUT	Control data signal output
3	VSS	Ground
4	DIN	Control data signal input

WS2812B Protocol





T0H	0 code ,high voltage time	0.4us	±150ns
T1H	1 code ,high voltage time	0.8us	±150ns
T0L	0 code , low voltage time	0.85us	±150ns
T1L	1 code ,low voltage time	0.45us	±150ns
RES	low voltage time	Above 50μs	

Composition of 24bit data:

G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	B7	B6	B5	B4	B3	B2	B1	B0

Note: Follow the order of GRB to sent data and the high bit sent at first.

STM32CubeIDE Demo

Lets go!!!

Microcontroller Engineering

Questions?

Contact information

Andreas Axelsson

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Mobile: 0709-467760