Microcontroller Engineering
TMIK13
Lecture 11

MEMORIES

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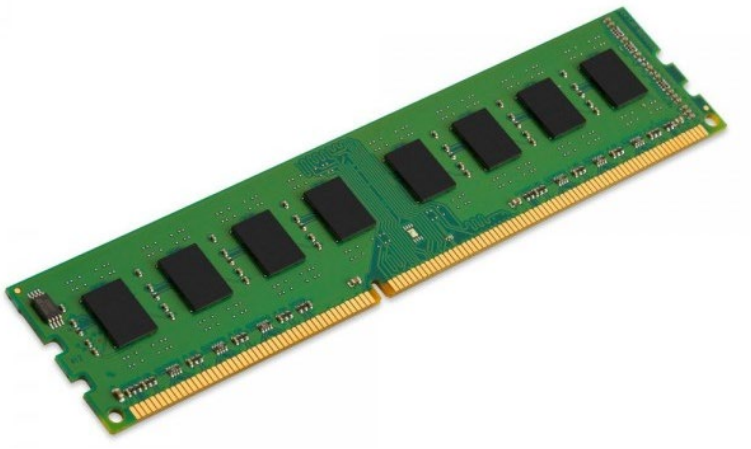
Digital Memories

Volatile

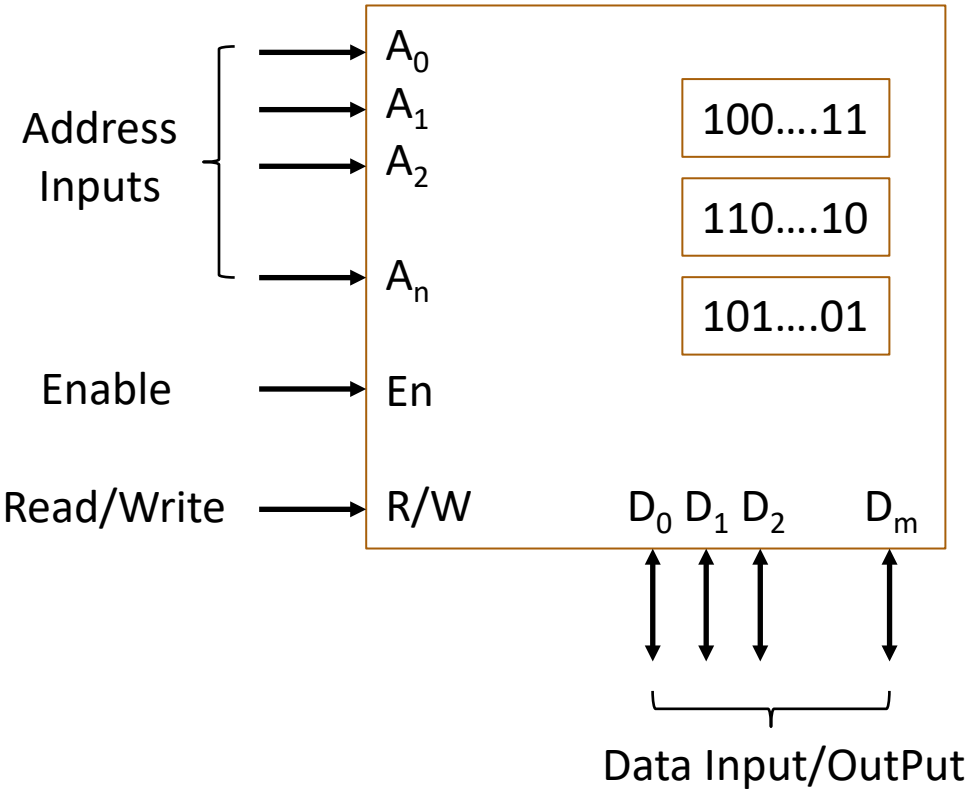
- RAM
  - Static
  - Dynamic



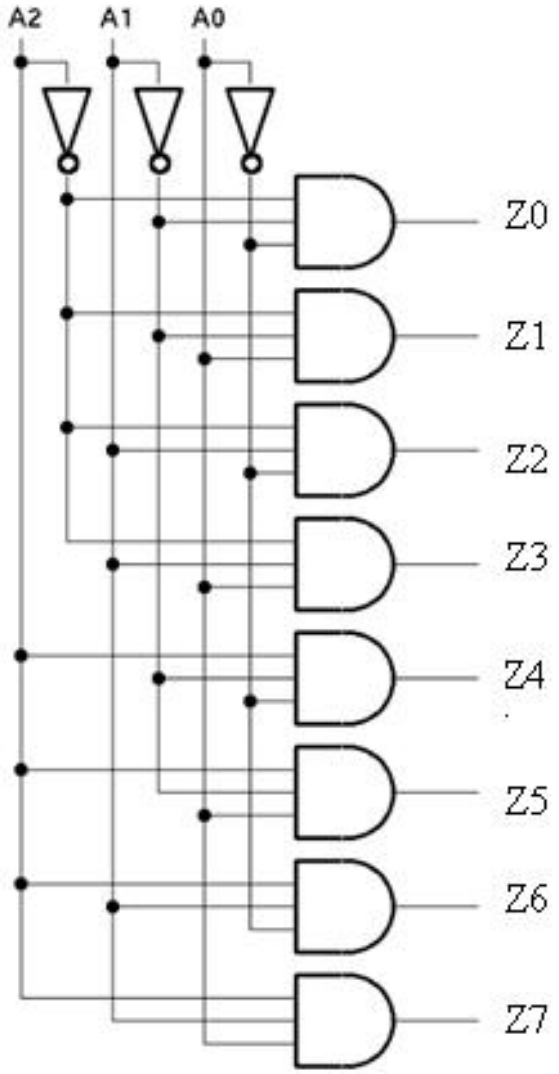
Non-volatile

- ROM / PROM
- EEPROM / FLASH
- FRAM

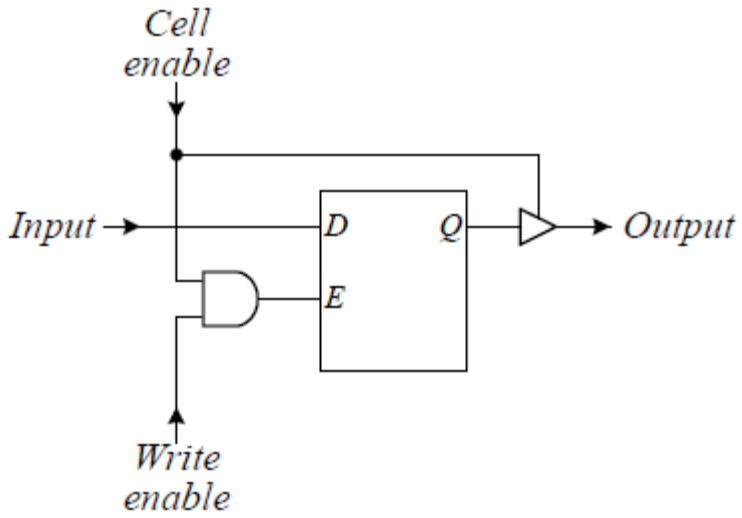
Memory – Block Diagram

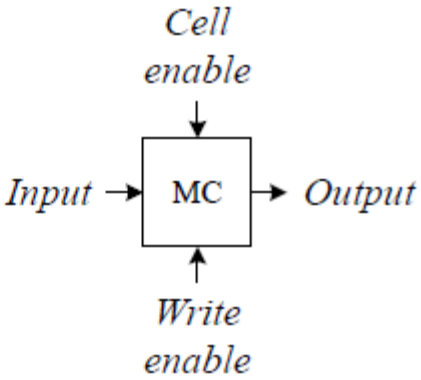


Address Decoder



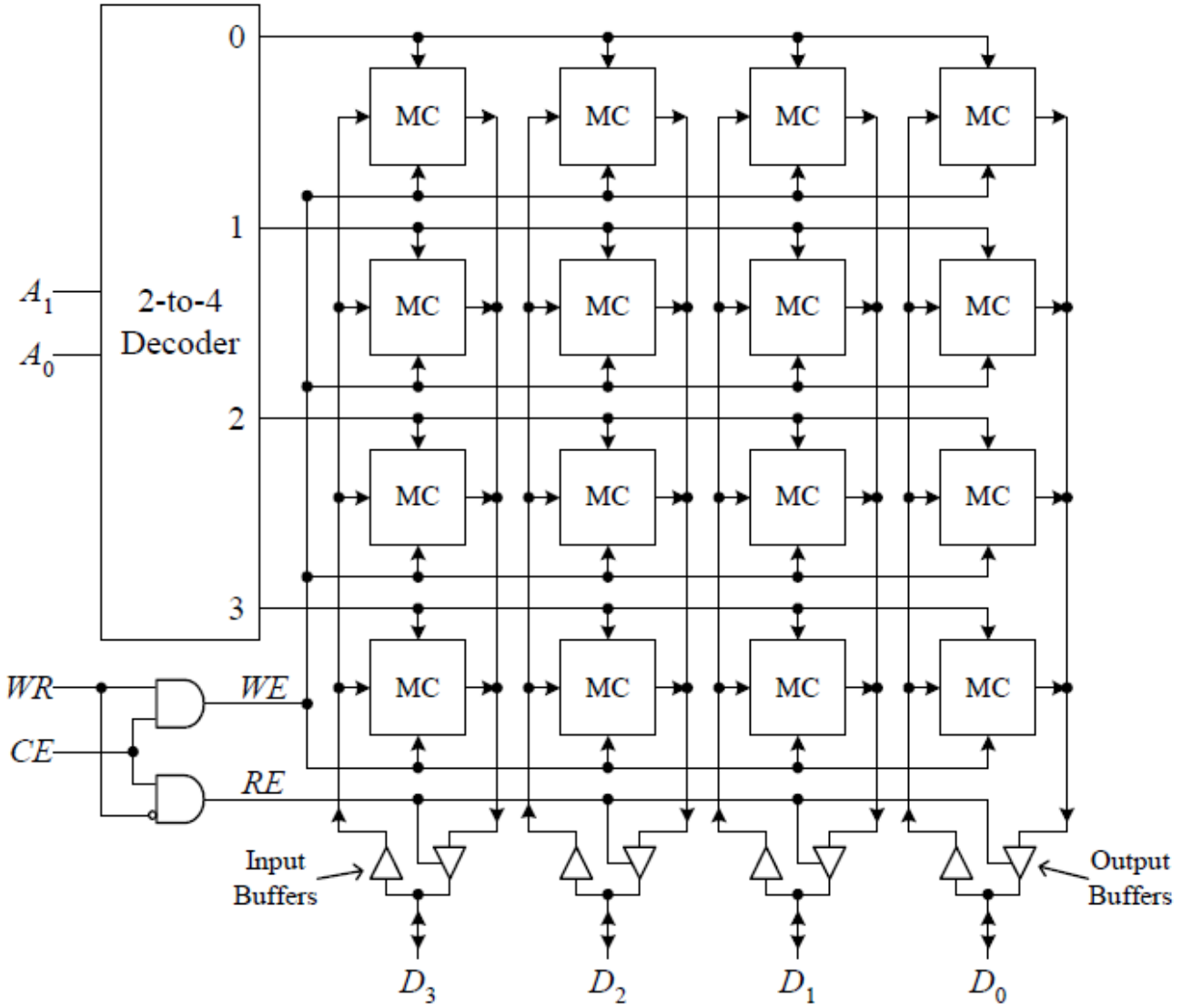
Static RAM – Flip Flop based





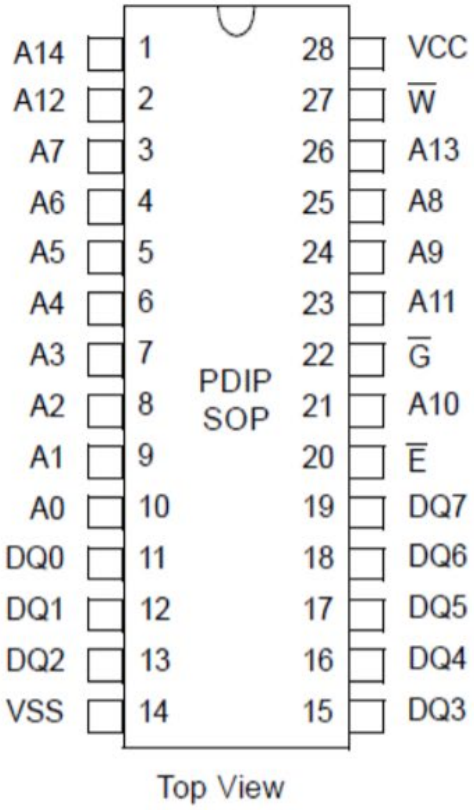
http://quitoart.blogspot.com/2017/10/fpga-vhdl-4-x-4-ram-memory-behavioural.html

Random Access Memory – RAM



Static RAM – Memory IC

PIN CONFIGURATION

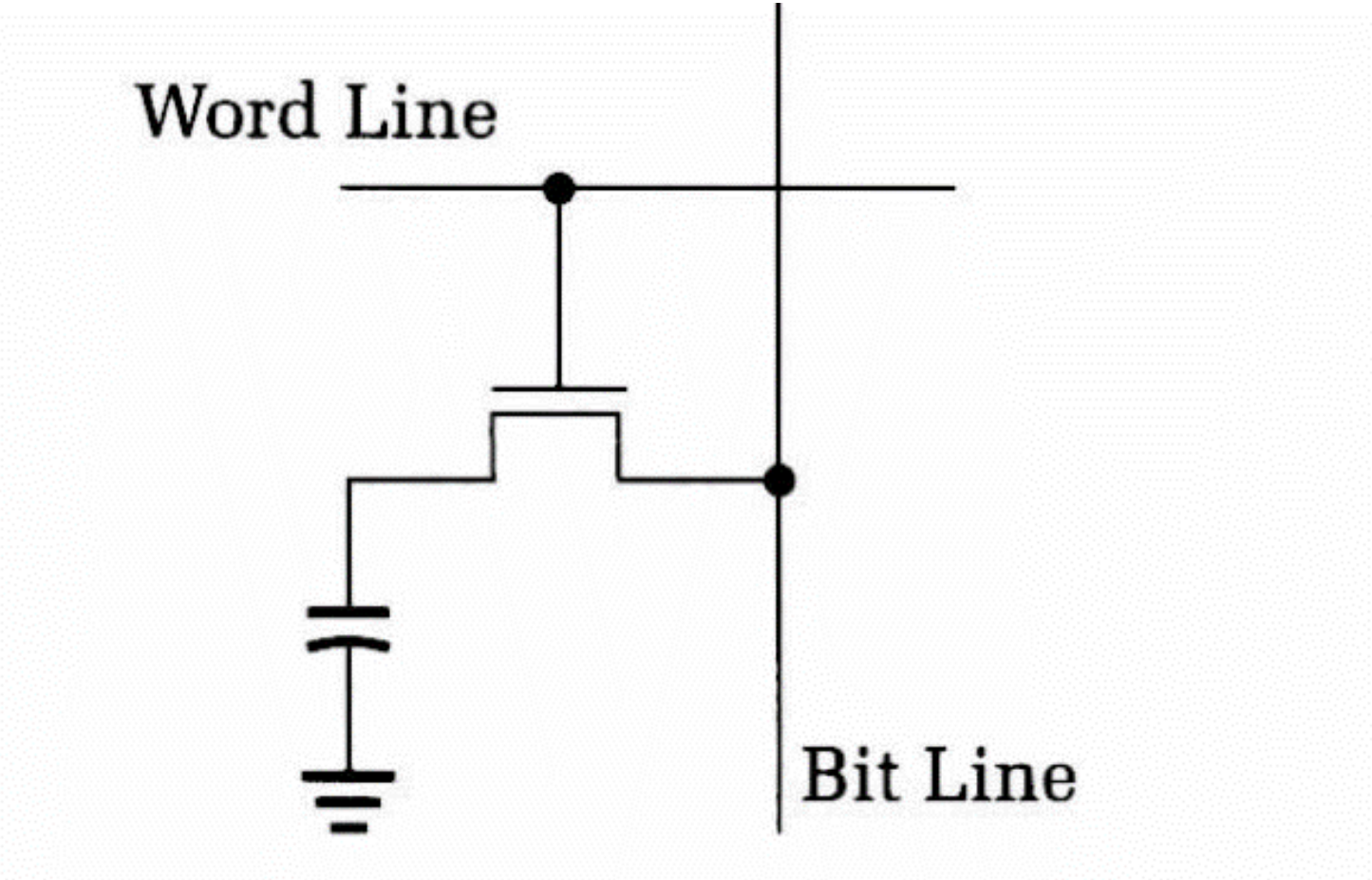


Top View

PIN DESCRIPTION

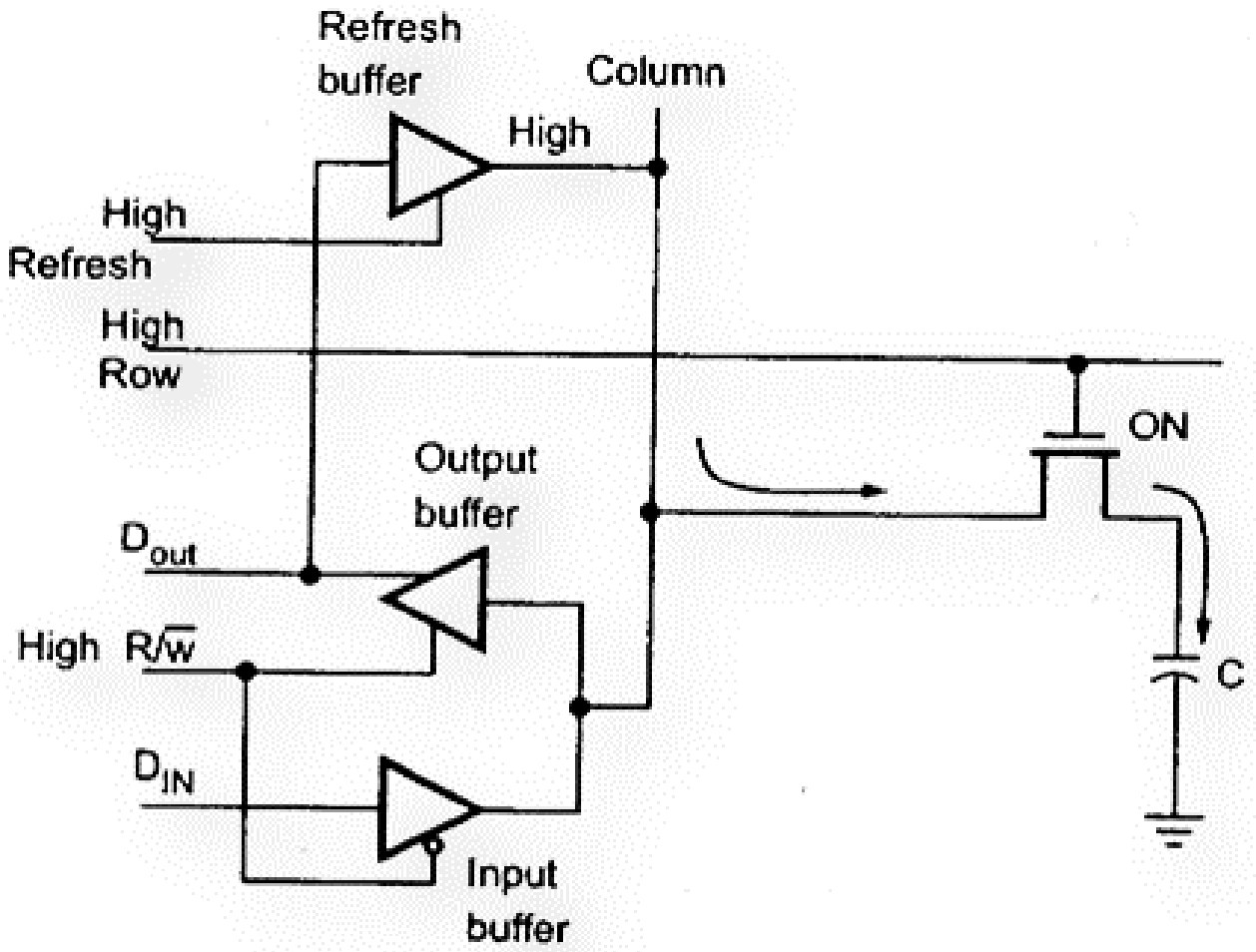
Signal Name	Signal Description
A0 - A14	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground

Dynamic RAM – Capacitor based



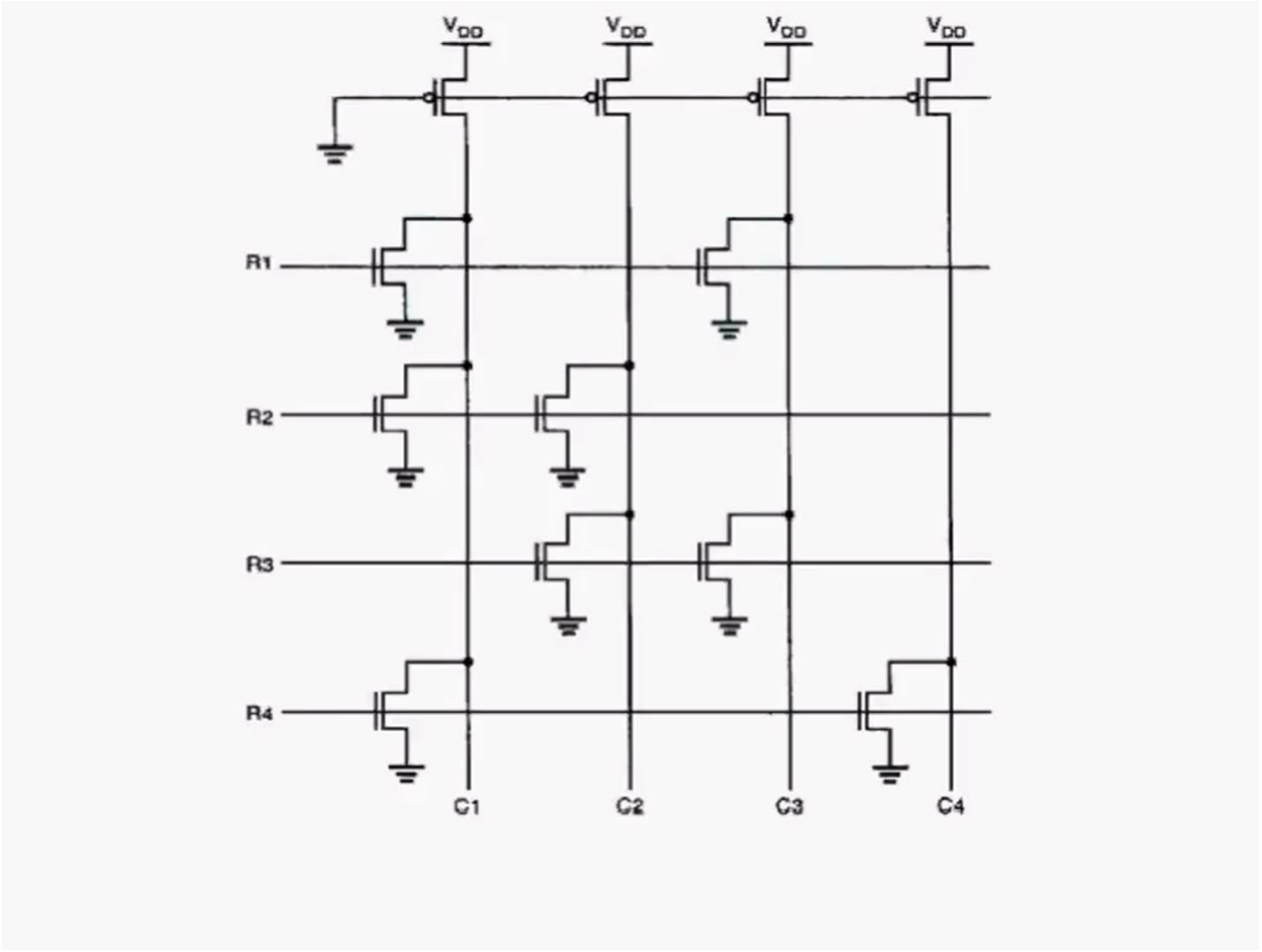
https://www.ee.nthu.edu.tw/jcliao/Logic98/chap07/showch07.html

Dynamic RAM – Capacitor based



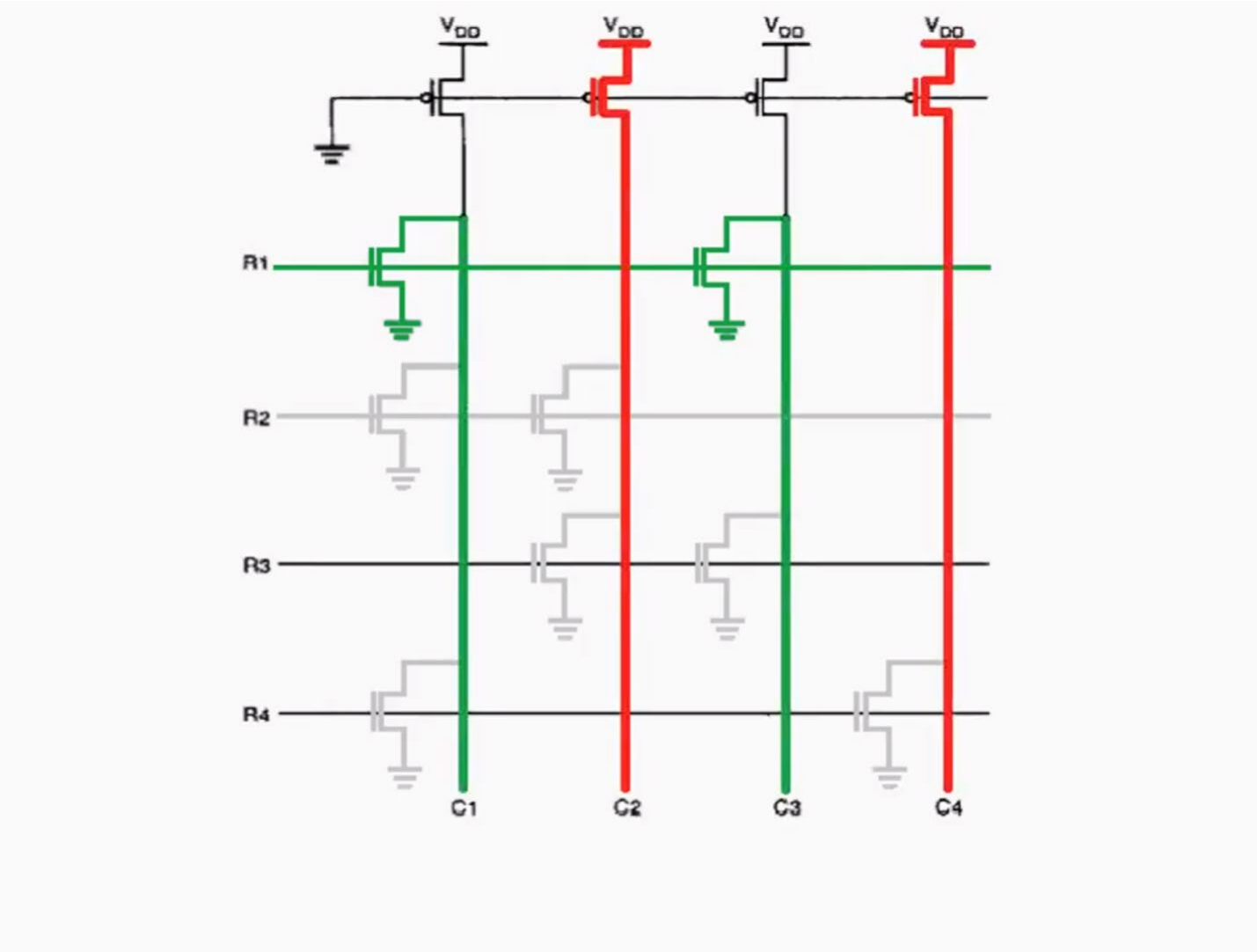
https://passionofphysics.blogspot.com/2019/03/mos-dynamic-ram-cell-refreshing-circuits.html

Read Only Memory - NOR



https://www.youtube.com/watch?v=f0sWw9CwhQY

Read Only Memory - NOR



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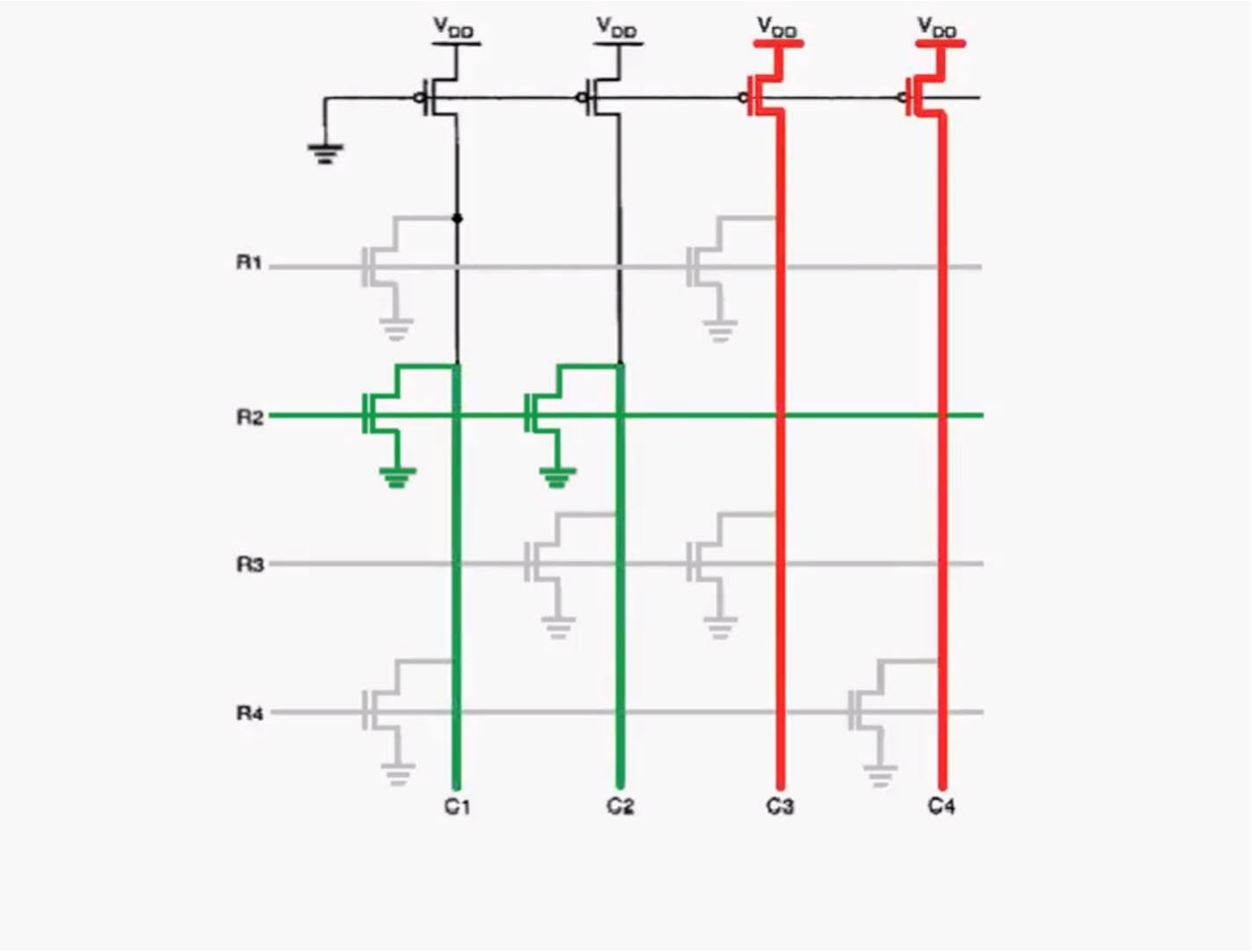
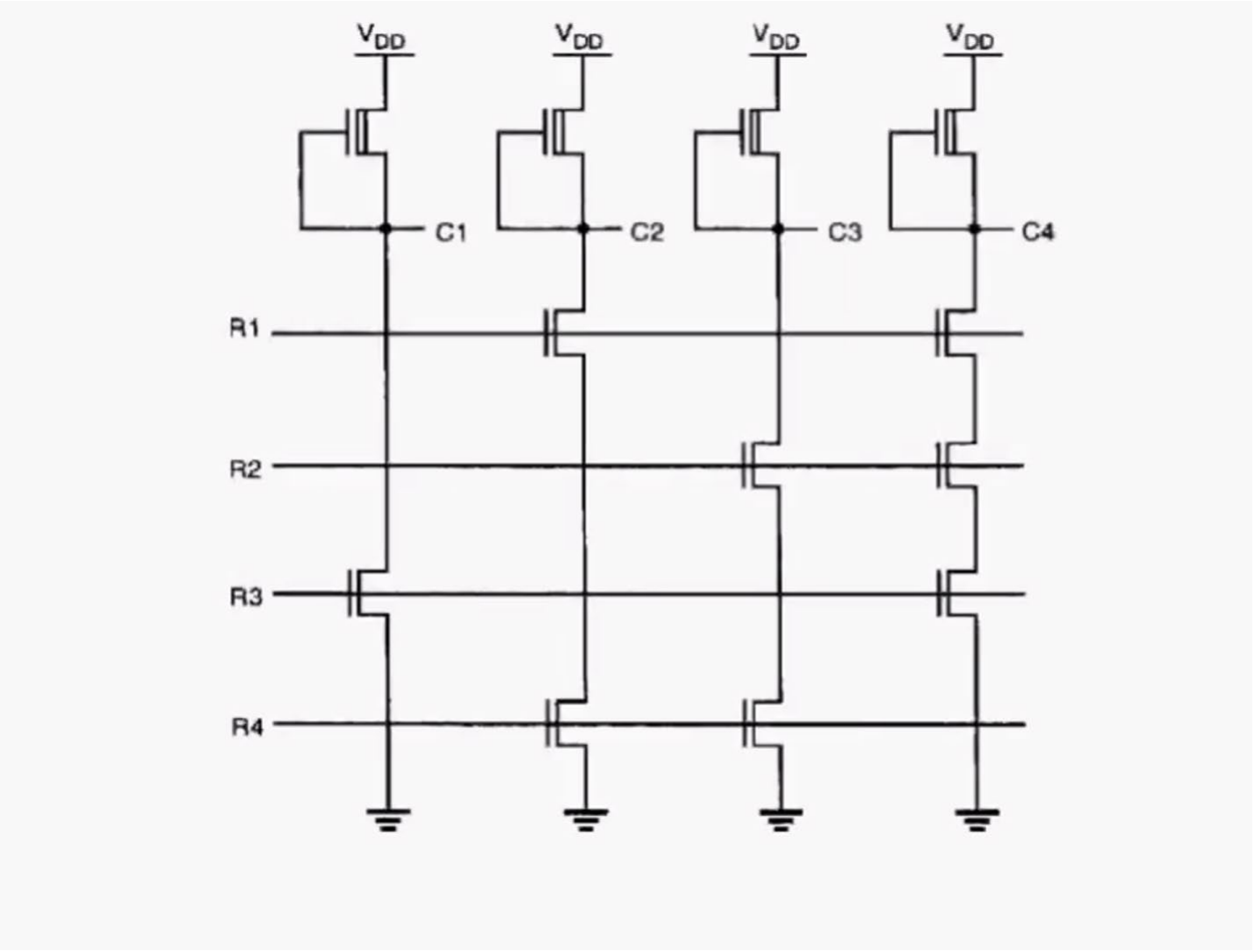
Read Only Memory - NOR



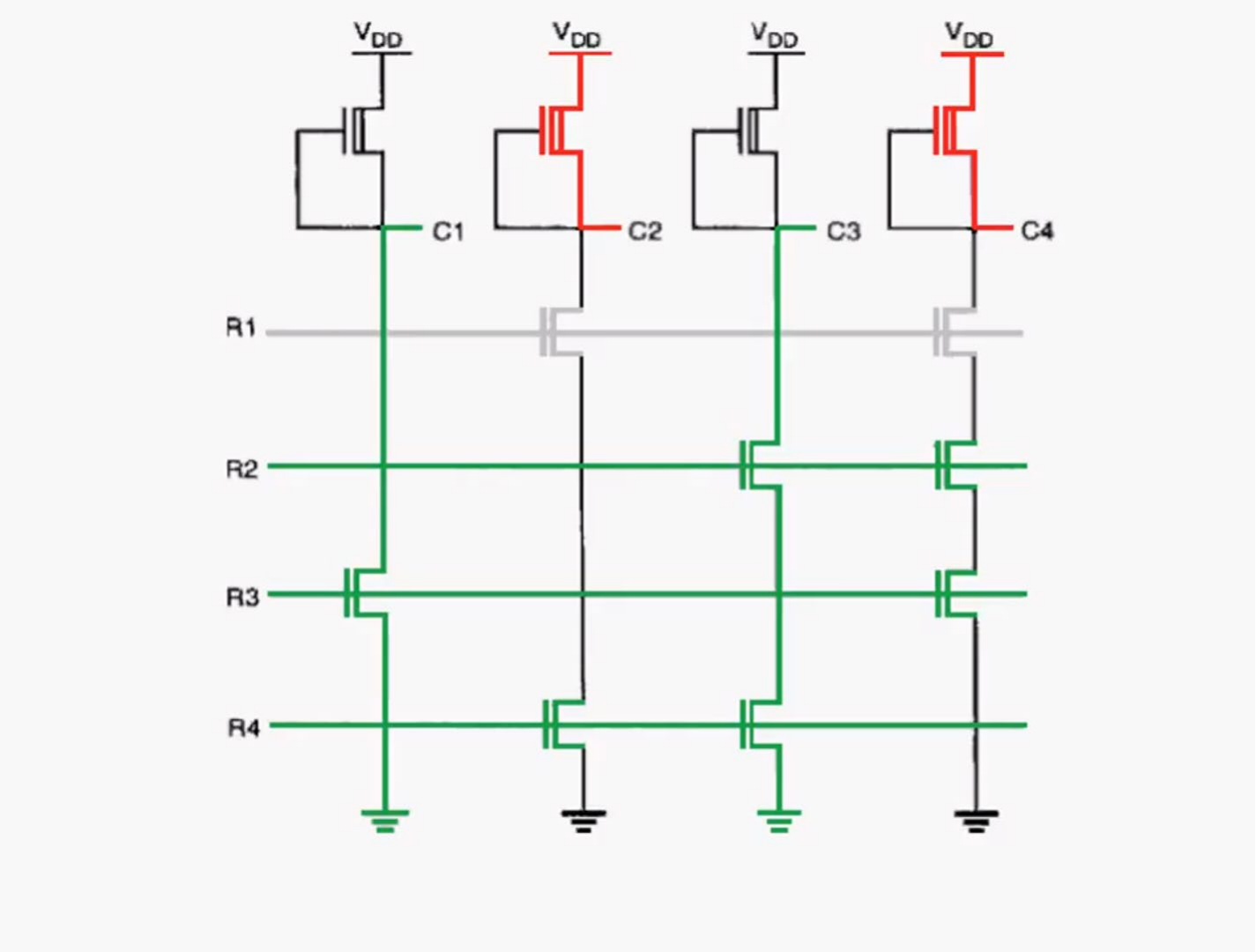
https://www.youtube.com/watch?v=f0sWw9CwhQY

Read Only Memory - NAND



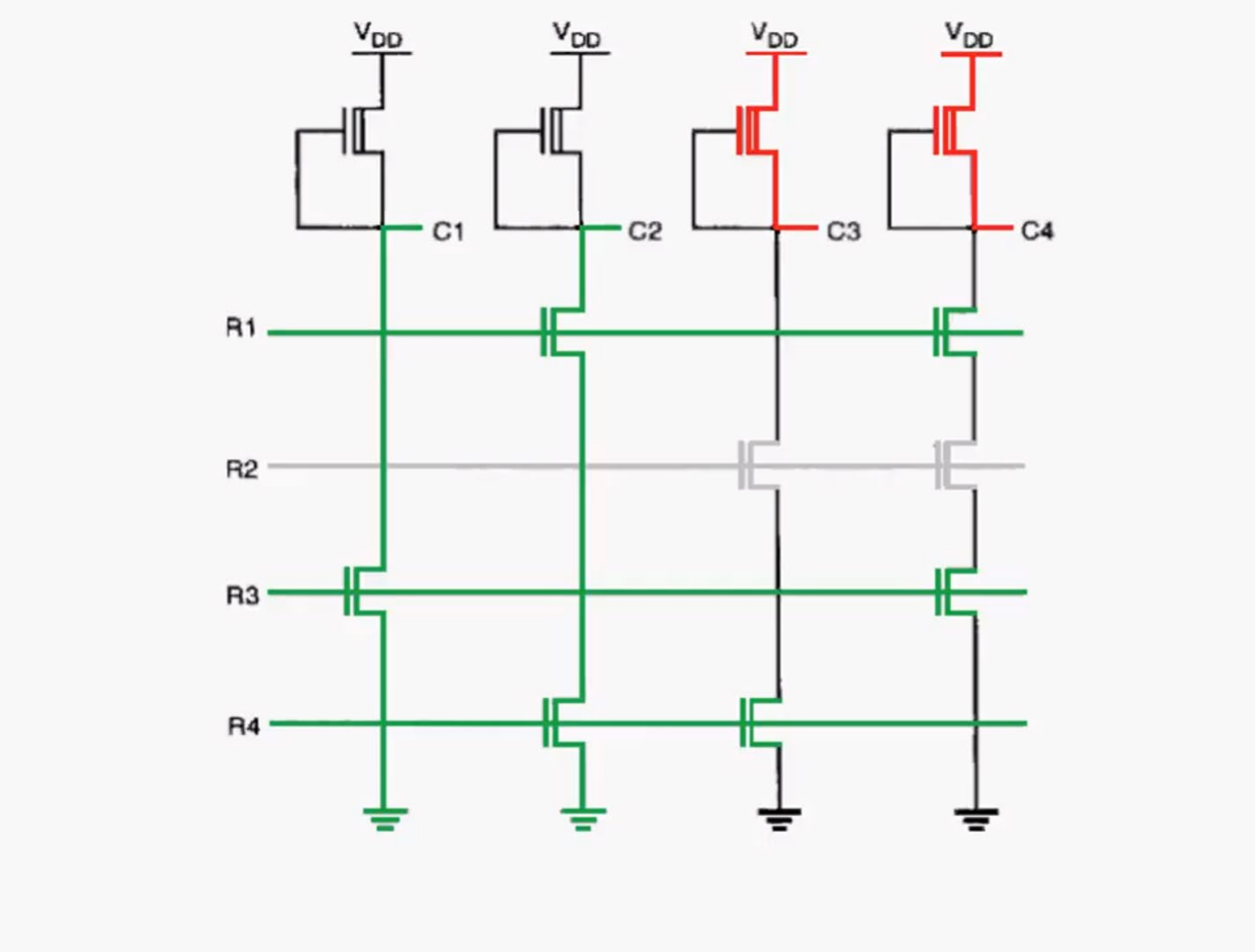
https://www.youtube.com/watch?v=92YIdjzrFuM

Read Only Memory - NAND



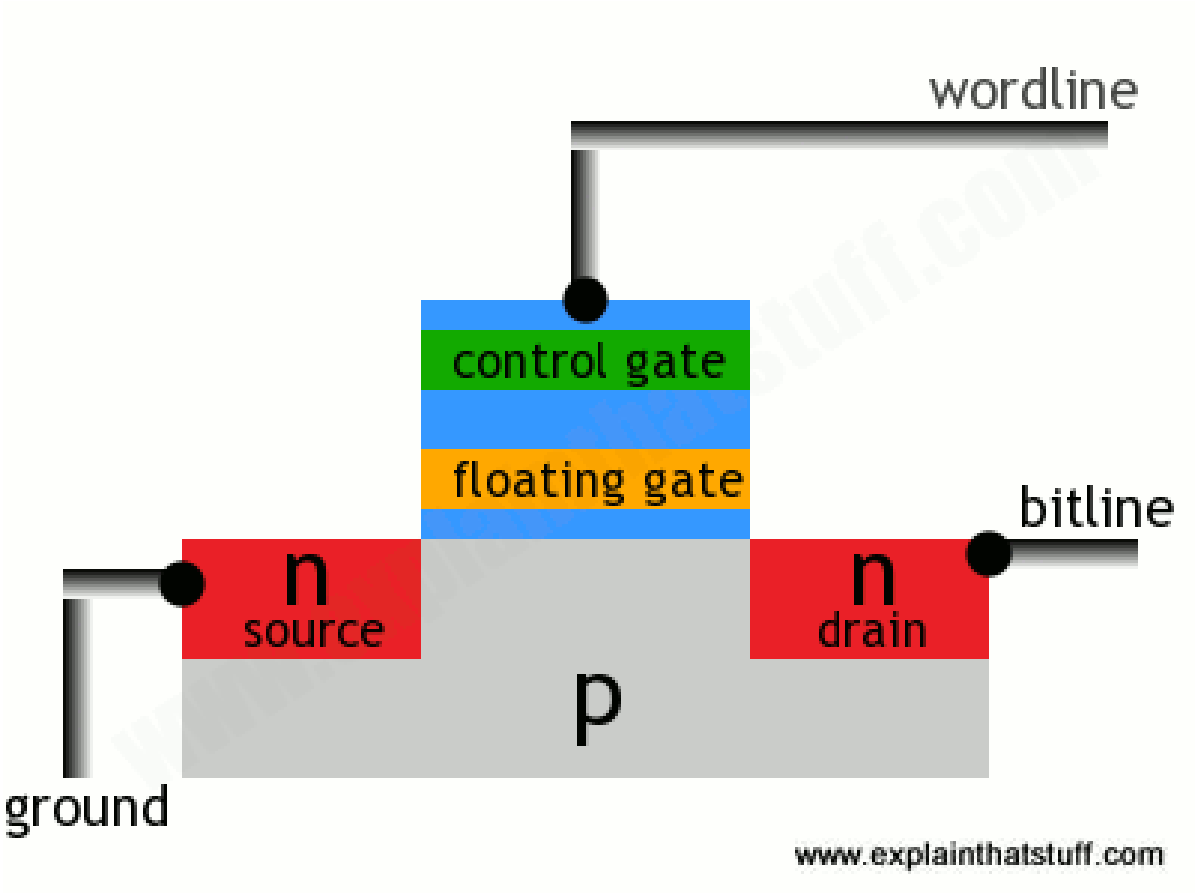
https://www.youtube.com/watch?v=92YIdjzrFuM

Read Only Memory - NAND



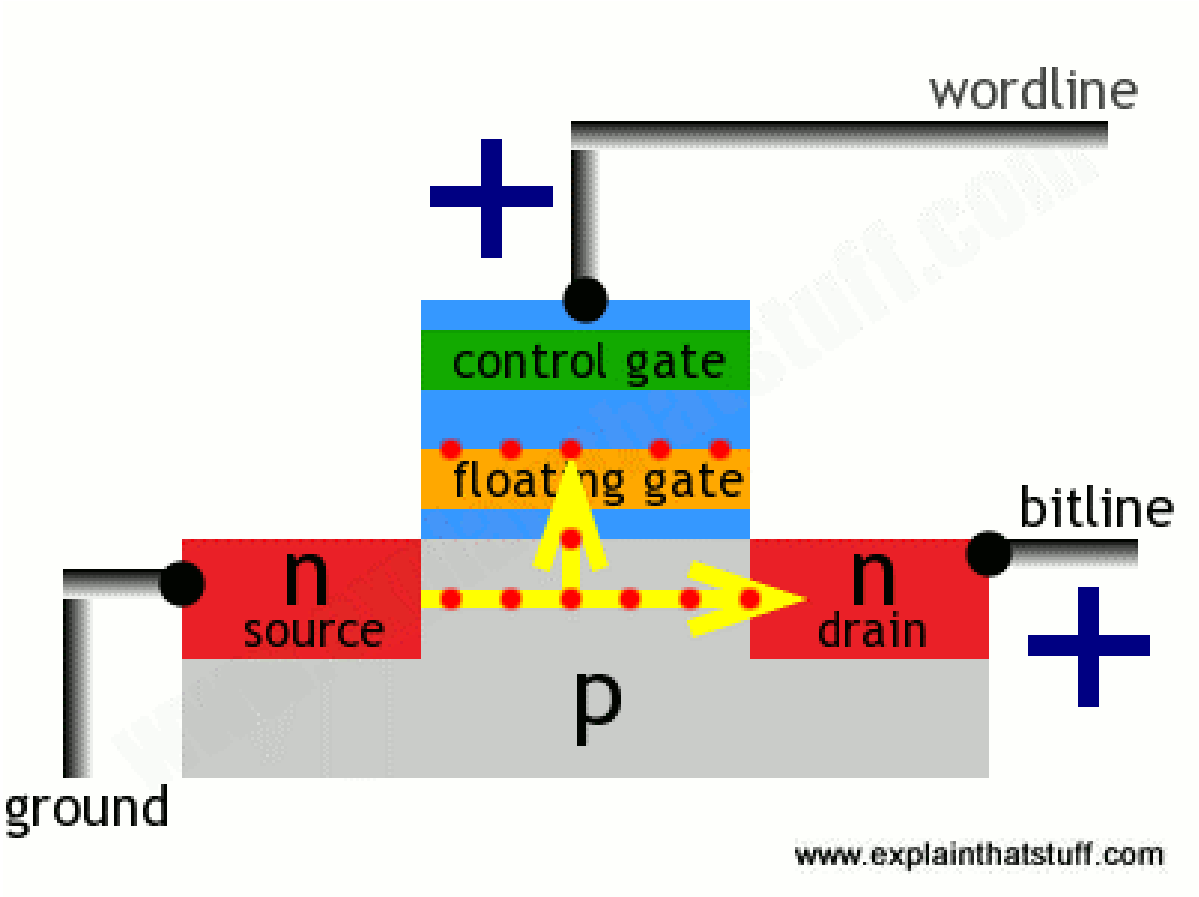
https://www.youtube.com/watch?v=92YIdjzrFuM

Flash memory



https://www.explainthatstuff.com/flashmemory.html

Flash memory

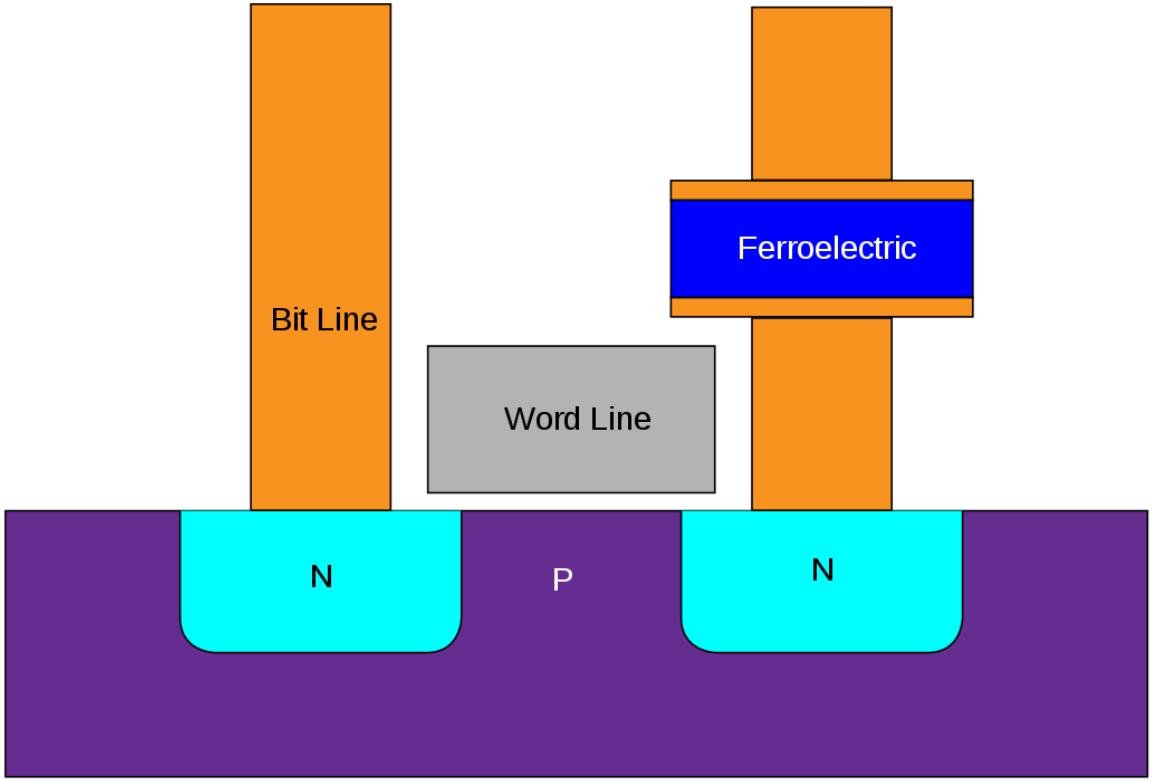


https://www.explainthatstuff.com/flashmemory.html

EPROM – UV erasable

Ferroelectric RAM – FRAM

Similar to DRAM but uses a ferroelectric crystal to store bit information
Keeps its memory after power-off
and has much faster write time compared to Flash and no wear



RAM – Serial Interface

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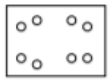
M24M02-DR
M24M02-R

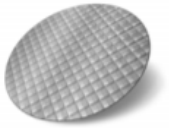
2-Mbit serial I²C bus EEPROM

Datasheet - production data

SO8 (MN)
150 mil width



WLCSP



Unsawn wafer

Features

- Compatible with all I^2C bus modes:
  - 1 MHz
  - 400 kHz
  - 100 kHz
- Memory array:
  - 2 Mbit (256 Kbyte) of EEPROM
  - Page size: 256 byte
  - Additional Write lockable page (M24M02-DR order codes)
- Single supply voltage:
  - 1.8 V to 5.5 V over –40 °C / +85 °C
- Write:
  - Byte Write within 10 ms
  - Page Write within 10 ms
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 4 million Write cycles
- More than 200-years data retention

Packages

- SO8 ECOPACK2®
- WLCSP ECOPACK2®
- Unsawn wafer (each die is tested)
- RoHS compliant and halogen-free (ECOPACK2®)

signetics FULLY ENCODED, 9046 X N, RANDOM ACCESS WRITE-ONLY-MEMORY

25120

FINAL SPECIFICATION[10]

DESCRIPTION

The Signetics 25000 Series 9C46XN Random Access Write-Only-Memory employs both enhancement and depletion mode P-Channel, N-Channel and Neu[1] channel MOS devices. Although a static device, a single TTL level clock phase is required to drive the on-board multi-port clock generator. Data refresh is accomplished during CB and LH periods [11]. Quadri-state outputs (when applicable) allow expansion in many directions, depending on organization.

The static memory cells are operated dynamically to yield extremely low power dissipation. All inputs and outputs are directly TL compatible when proper interfacing circuitry is employed.

Device construction is more or less S.O.S.[2]

FEATURES

- **FULLY ENCODED MULTI-PORT ADDRESSING**
- **WRITE CYCLE TIME 80nS (MAX. TYPICAL)**
- **WRITE ACCESS TIME[3]**
- **POWER DISSIPATION 10µW/BIT TYPICAL**
- **CELL REFRESH TIME 1mS (MIN. TYPICAL)**
- **TTL/DTL COMPATIBLE INPUTS[4]**
- **AVAILABLE OUTPUTS "n"**
- **CLOCK LINE CAPACITANCE 2pF MAX.[5]**
- **V^{CC} = +10V**
- **V^{DD} = 0V ±2%**
- **V^{FF} = 6.3V[ac][6]**

APPLICATIONS

DON'T CARE BUFFER STORES
LEAST SIGNIFICANT CONTROL MEMORIES
POST MORTEM MEMORIES (WEAPON SYSTEMS)
ARTIFICIAL MEMORY SYSTEMS
NON-INTELLIGENT MICRO CONTROLLERS
FIRST-IN NEVER-OUT (FINO) ASYNCHRONOUS BUFFERS.
OVERFLOW REGISTER (BIT BUCKET)

PROCESS TECHNOLOGY

The use of Signetics unique SEX[7] process yields Vth (var.) and allows the design[8] and production[9] of higher performance MOS circuits than can be obtained by competitor's techniques.

BIPOLAR COMPATIBILITY

All data are clock input pins applicable output will interface directly or nearly directly with bipolar circuits of suitable characteristics in any event use 1 amp fuses in all power supply and data lines.

INPUT PROTECTION

All terminals are provided with slip-on latex protectors for the prevention of Voltage Destruction. (PILL packaged devices do not require protection.)

SILICON PACKAGING

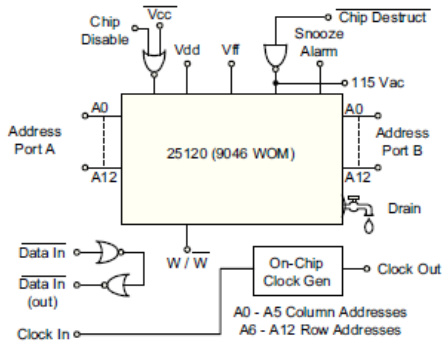
Low cost silicon DIP packaging is implemented and reliability is assured by the use of a non-hermetic sealing technique which prevents the entrapment of harmful ions,, but which allows the free exchange of friendly ions.

SPECIAL FEATURES

Because of the employment of the Signetics' proprietary Sanderson-Rabbet Channel the 25120 will provide 50% higher speed than you will obtain.

COOLING

The 25120 is easily cooled by the employment of a six foot fan ½" from the package. If the device fails you have exceeded the ragings. In such cases, more air is recommended.



PART IDENTIFICATION

TYPE	"n"	TEMP. RANGE	PACKAGE
25120	0	0 to –70°C	Whatever's Right

1. "Neu" channel 16V CMOS enhances or depletes regardless of gate polarity, either simultaneously or randomly. Sometimes not at all.
2. "S.O.S" copyrighted U.S. Army Commissary, 1940.
3. Not applicable.
4. You can somehow drive these inputs from TTL, the method is obvious.
5. Measure at 1MHz, 25mvac, 1.8pf in series.
6. For filaments, what else!
7. You have a dirty mind. S.E.X. is a Signetics Extra Secret process. "One Shovel Full to One Shovel Full", patented by Yagura, Kashkooli, Converse and AL, Circa 1921.
8. J. Kana calls it design (we humor him).
9. See "Modem Production Techniques" by T. Arrieta (not yet written).
10. Final until we got a look at some actual parts.
11. Coffee breaks and lunch hours.
12. Due credit to EIMAC for inspiration.

STM32F411RE

- Memories
  - Up to 512 Kbytes of Flash memory
  - 128 Kbytes of SRAM

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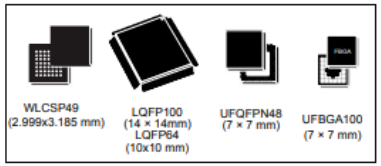
STM32F411xC STM32F411xE

Arm® Cortex®-M4 32b MCU+FPU, 125 DMIPS, 512KB Flash, 128KB RAM, USB OTG FS, 11 TIMs, 1 ADC, 13 comm. interfaces

Datasheet - production data

Features

- Dynamic Efficiency Line with BAM (Batch Acquisition Mode)
  - 1.7 V to 3.6 V power supply
  - - 40°C to 85/105/125 °C temperature range
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 100 MHz, memory protection unit, 125 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 512 Kbytes of Flash memory
  - 128 Kbytes of SRAM
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Power consumption
  - Run: 100 µA/MHz (peripheral off)
  - Stop (Flash in Stop mode, fast wakeup time): 42 µA Typ @ 25C; 65 µA max @25 °C
  - Stop (Flash in Deep power down mode, slow wakeup time): down to 9 µA @ 25 °C; 28 µA max @25 °C
  - Standby: 1.8 µA @25 °C / 1.7 V without RTC; 11 µA @85 °C @1.7 V
  - V_{BAT} supply for RTC: 1 µA @25 °C
- 1×12-bit, 2.4 MSPS A/D converter: up to 16 channels
- General-purpose DMA: 16-stream DMA controllers with FIFOs and burst support
- Up to 11 timers: up to six 16-bit, two 32-bit timers up to 100 MHz, each with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input, two watchdog timers (independent and window) and a SysTick timer



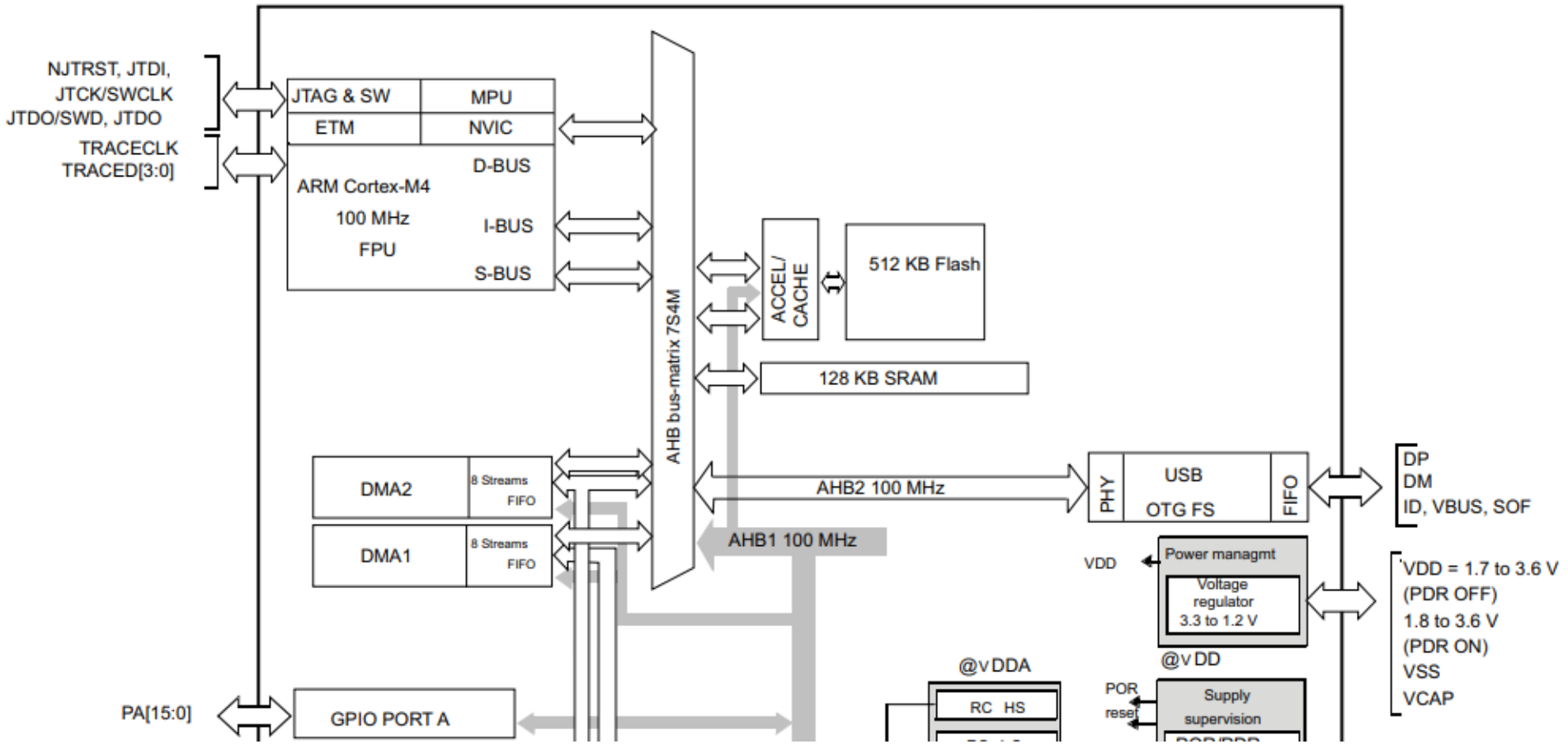
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex®-M4 Embedded Trace Macrocell™
- Up to 81 I/O ports with interrupt capability
  - Up to 78 fast I/Os up to 100 MHz
  - Up to 77 5 V-tolerant I/Os
- Up to 13 communication interfaces
  - Up to 3 x I^2C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (2 x 12.5 Mbit/s, 1 x 6.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 5 SPI/I2Ss (up to 50 Mbit/s, SPI or I2S audio protocol), SPI2 and SPI3 with muxed full-duplex I^2S to achieve audio class accuracy via internal audio PLL or external clock
  - SDIO interface (SD/MMC/eMMC)
  - Advanced connectivity: USB 2.0 full-speed device/host/OTG controller with on-chip PHY
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- All packages (WLCSP49, LQFP64/100, UFQFPN48, UFBGA100) are ECOPACK®2

Table 1. Device summary

Reference	Part number
STM32F411xC	STM32F411CC, STM32F411RC, STM32F411VC
STM32F411xE	STM32F411CE, STM32F411RE, STM32F411VE

This is information on a product in full production. www.st.com

STM32F411RE



STM32F411RE

Table 3. Memory mapping vs. Boot mode/physical remap in STM32F411xC/E

Addresses	Boot/Remap in main Flash memory	Boot/Remap in embedded SRAM	Boot/Remap in System memory
0x2000 0000 - 0x2002 0000	SRAM1 (128 KB)	SRAM1 (128KB)	SRAM1 (128KB)
0x1FFF 0000 - 0x1FFF 77FF	System memory	System memory	System memory
0x0804 0000 - 0x1FFE FFFF	Reserved	Reserved	Reserved
0x0800 0000 - 0x0807 FFFF	Flash memory	Flash memory	Flash memory
0x0400 000 - 0x07FF FFFF	Reserved	Reserved	Reserved
0x0000 0000 - 0x0007 FFFF(1)	Flash (512 KB) Aliased	SRAM1 (128 KB) Aliased	System memory (30 KB) Aliased

1. Even when aliased in the boot memory space, the related memory is still accessible at its original memory space.

Table 2. Boot modes

Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as the boot space
0	1	System memory	System memory is selected as the boot space
1	1	Embedded SRAM	Embedded SRAM is selected as the boot space

STM32F411RE

Table 5. Number of wait states according to CPU clock (HCLK) frequency

Wait states (WS) (LATENCY)	HCLK (MHz)			
	Voltage range 2.7 V - 3.6 V	Voltage range 2.4 V - 2.7 V	Voltage range 2.1 V - 2.4 V	Voltage range 1.71 V - 2.1 V
0 WS (1 CPU cycle)	0 < HCLK≤ 30	0 < HCLK ≤24	0 < HCLK ≤ 18	0 < HCLK ≤ 16
1 WS (2 CPU cycles)	30 < HCLK ≤64	24 < HCLK ≤48	18 < HCLK ≤36	16 <HCLK ≤32
2 WS (3 CPU cycles)	64 < HCLK ≤90	48 < HCLK ≤72	36 < HCLK ≤54	32 < HCLK ≤48
3 WS (4 CPU cycles)	90 < HCLK ≤ 100	72 < HCLK ≤96	54 < HCLK ≤72	48 < HCLK ≤64
4 WS (5 CPU cycles)	-	96 < HCLK ≤ 100	72 < HCLK ≤90	64 < HCLK ≤80
5 WS (6 CPU cycles)	-	-	90 < HCLK ≤ 100	80 < HCLK ≤96
6 WS (7 CPU cycles)	-	-	-	96 < HCLK ≤ 100

Uses ACCEL (cache and prefetch) to hide wait-states

https://www.st.com/resource/en/reference_manual/rm0383-stm32f411xce-advanced-armbased-32bit-mcus-stmicroelectronics.pdf

Microcontroller Engineering

Questions?

Contact information

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