Cse 231 (Digital Logic Design)

Group Project: EID – 2021

Group Number : 04

Group members :

1. Mosroor Mofiz Arman (1921079642) – [SOP]
2. Md Ariful Hasan Suvo (1913087626) - [NAND]
3. Raiyan Rafsan (1921244042) - [NOR]
4. Latifa Hamid Munni (1921099042) - [POS]

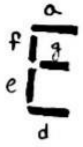
Submitted to:

Dr Mohammad Monirujjaman Khan (KMM)

Date: 27.04.2021

Using (POS) by Latifa :

Project : EId - 2021

E → 

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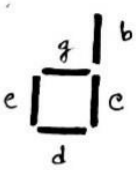
d → 

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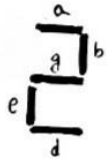
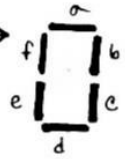
2 → 

0 → 

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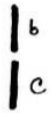
1 → 

Truth Table :

Words and Decimal numbers	Inputs			outputs						
	A	B	C	a	b	c	d	e	f	g
E	0	0	0	1	0	0	1	1	1	1
I	0	0	1	0	1	1	0	0	0	0
d	0	1	0	0	1	1	1	1	0	1
—	0	1	1	0	0	0	0	0	0	1
2	1	0	0	1	1	0	1	1	0	1
0	1	0	1	1	1	1	1	1	1	0
2	1	1	0	1	1	0	1	1	0	1
1	1	1	1	0	1	1	0	0	0	0

The POS Equations :

a : $(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+\bar{C})$

b : $(A+B+C)(A+\bar{B}+\bar{C})$

c : $(A+B+C)(A+\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+\bar{B}+C)$

d : $(A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+\bar{C})$

e : $(A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+\bar{C})$

f : $(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+\bar{B}+C)(\bar{A}+\bar{B}+\bar{C})$

g : $(A+B+\bar{C})(\bar{A}+B+\bar{C})(\bar{A}+\bar{B}+\bar{C})$

For Segment a:

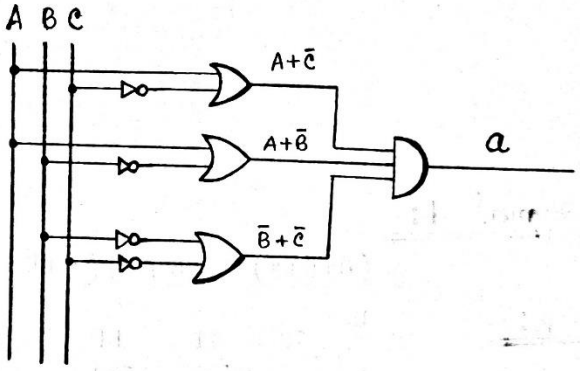
$(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+\bar{C})$

K-map:

A \ BC	00	01	11	10
0	1	0	0	0
1	1	1	0	1

$\therefore a = (A+\bar{C})(A+\bar{B})(\bar{B}+\bar{C})$

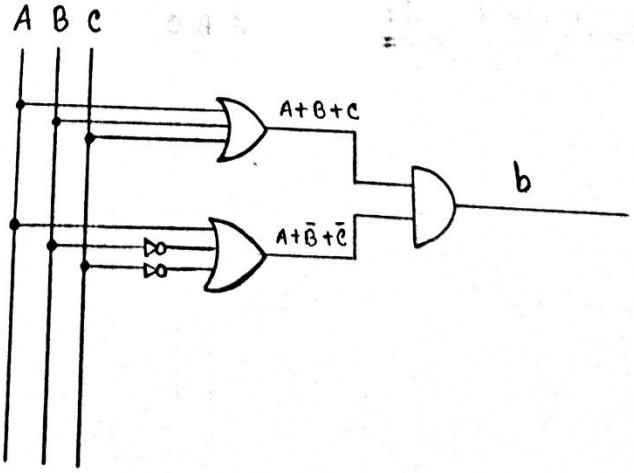
Logic circuit for a:



For Segment b:

$(A+B+C)(A+\bar{B}+\bar{C})$

Logic circuit for b:



for segment c :

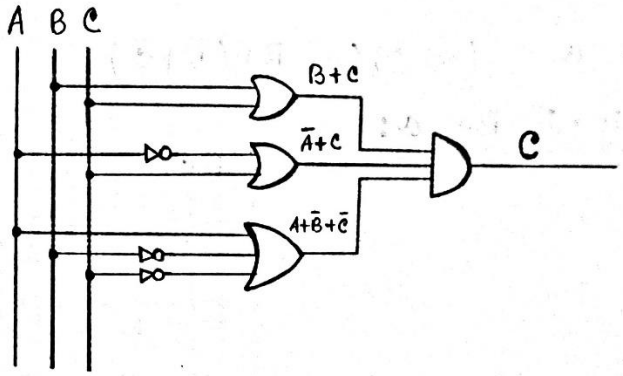
$$(A+B+C)(A+\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+\bar{B}+C)$$

K-map :

A \ BC	00	01	11	10
0	0	1	0	1
1	0	1	1	0

$$\therefore \quad C = (B+C)(\bar{A}+C)(A+\bar{B}+\bar{C})$$

Logic circuit for c :



for segment d :

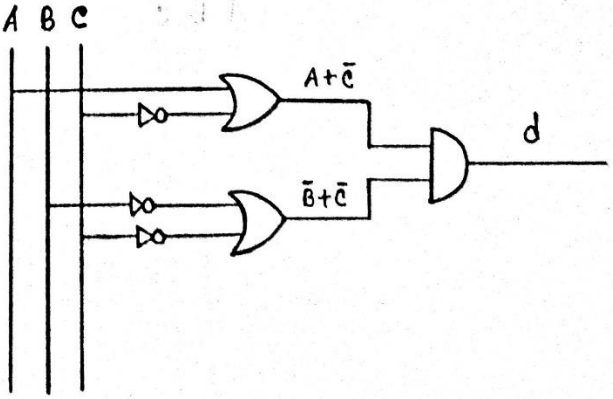
$$(A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+\bar{C})$$

K-map :

A \ BC	00	01	11	10
0	1	0	0	1
1	1	1	0	1

$$\therefore \quad d = (A+\bar{C})(\bar{B}+\bar{C})$$

Logic circuit for d :



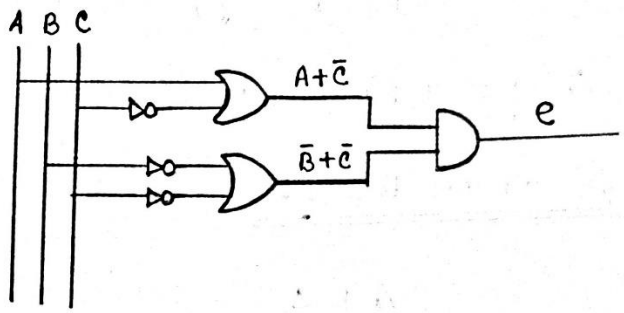
for segment e : $(A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+\bar{C})$

K-map :

A \ BC	00	01	11	10
0	1	0	0	1
1	1	1	0	1

$\therefore e = (A+\bar{C})(\bar{B}+\bar{C})$

Logic circuit for e :



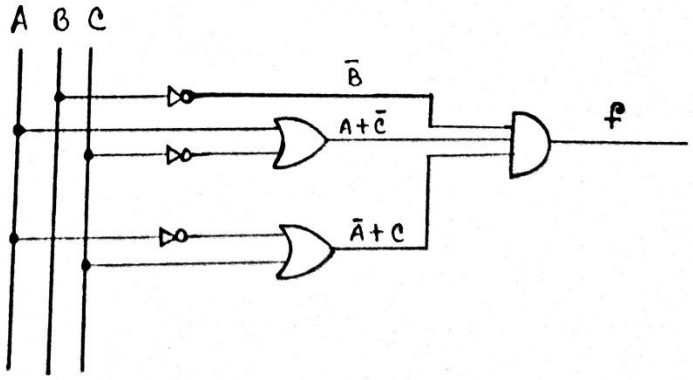
for segment f :

$(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+\bar{B}+C)(\bar{A}+\bar{B}+\bar{C})$

A \ BC	00	01	11	10
0	1	0	0	0
1	0	1	0	0

$\therefore f = \bar{B} \cdot (A+\bar{C}) \cdot (\bar{A}+C)$

Logic circuit for f :



for segment g:

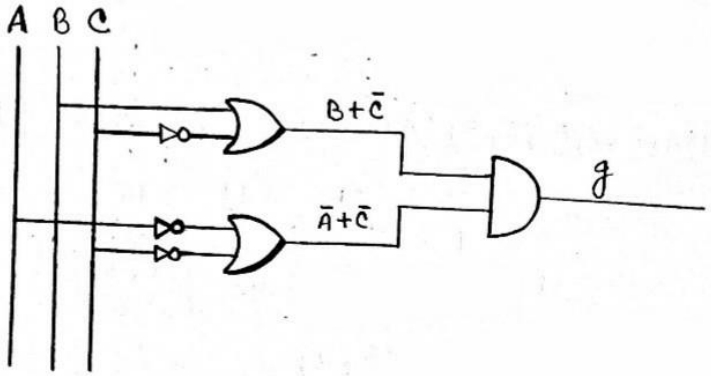
$$(A+B+\bar{C})(\bar{A}+B+\bar{C})(\bar{A}+\bar{B}+\bar{C})$$

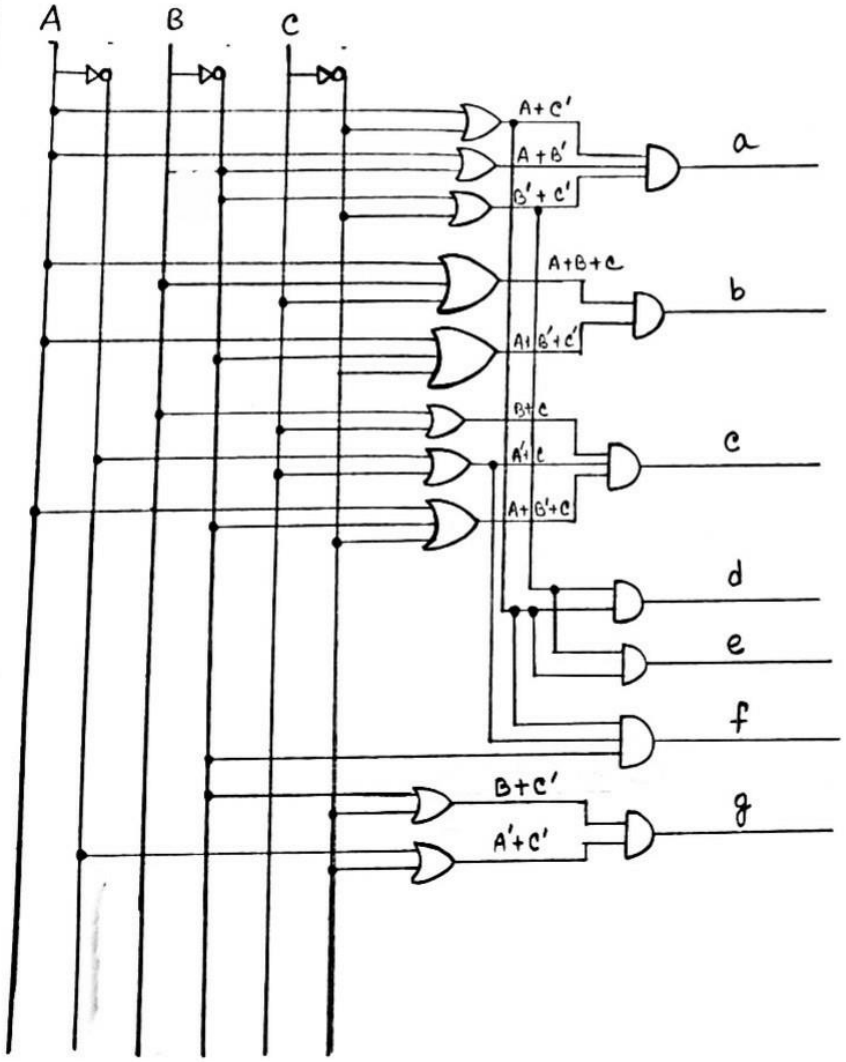
K-map:

A \ BC	00	01	11	10
0	1	0	1	1
1	1	0	0	1

$$\therefore g = (B+\bar{C})(\bar{A}+\bar{C})$$

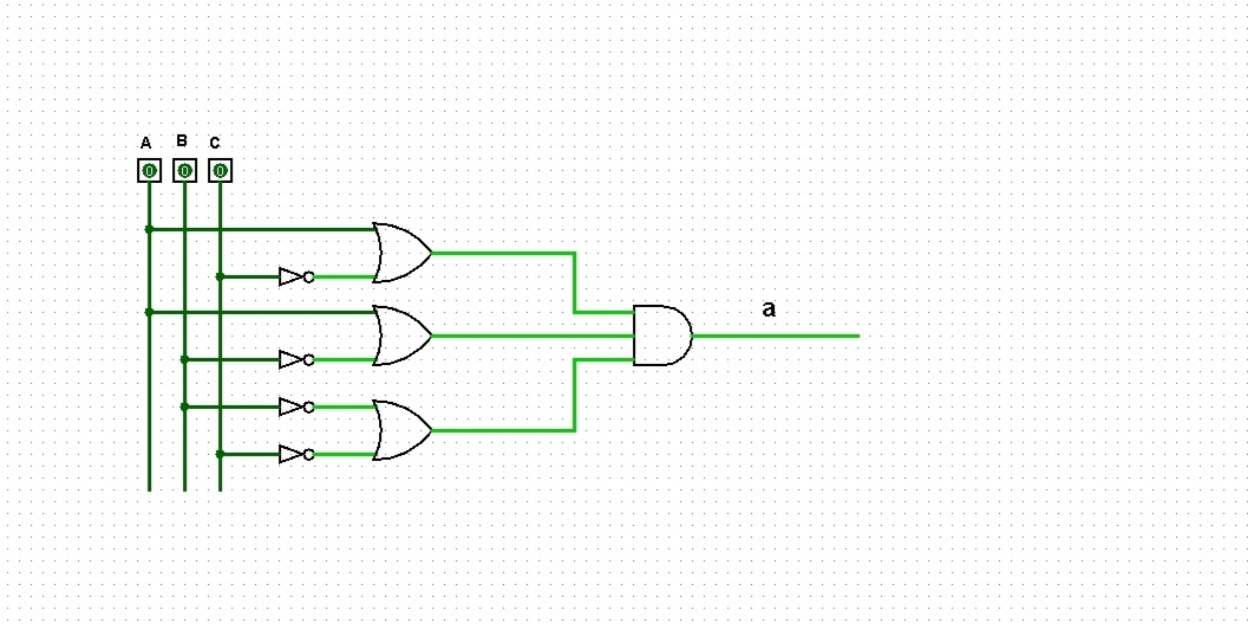
Logic circuit for g:

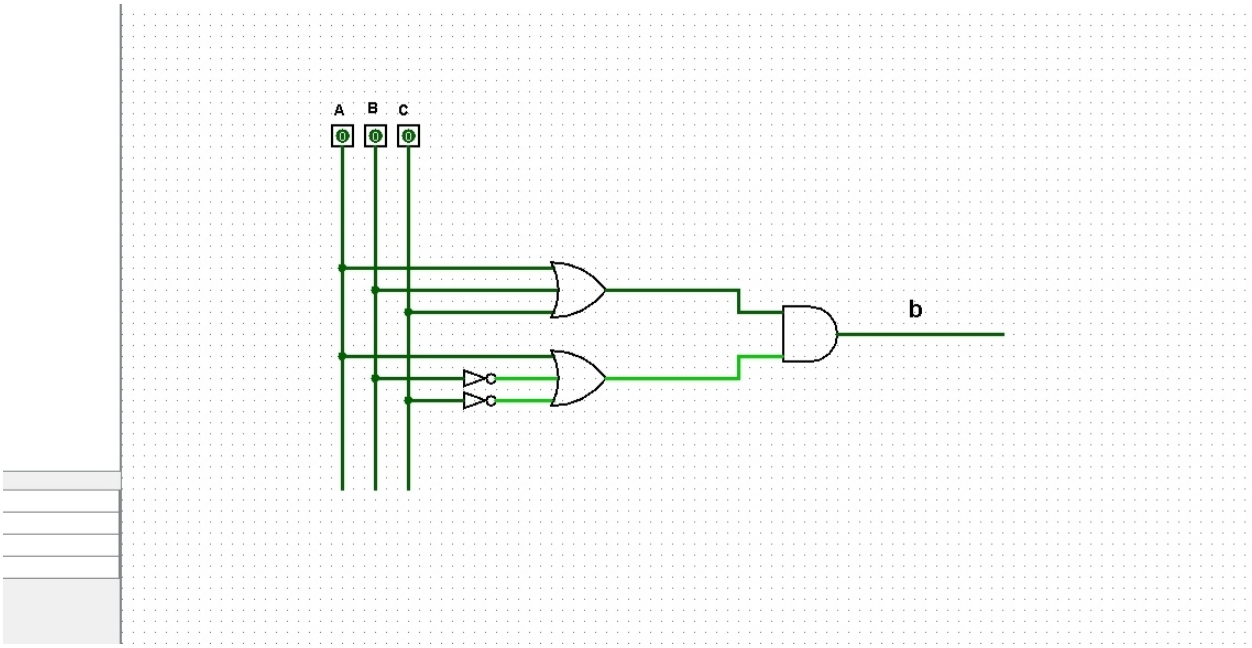


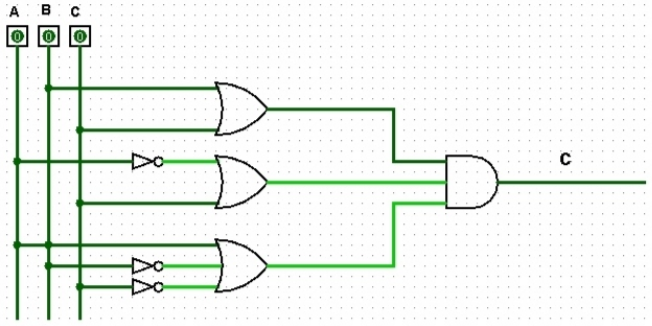


Project figure : The seven segment Decoder circuit for Eid - 2021

Logism Diagram:



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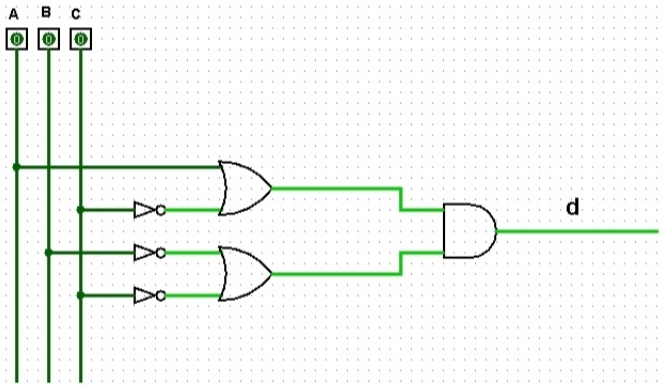
0
c


A
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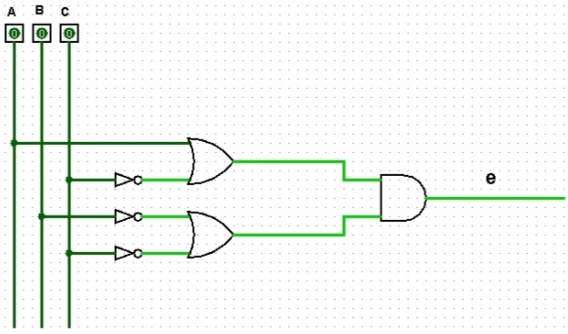
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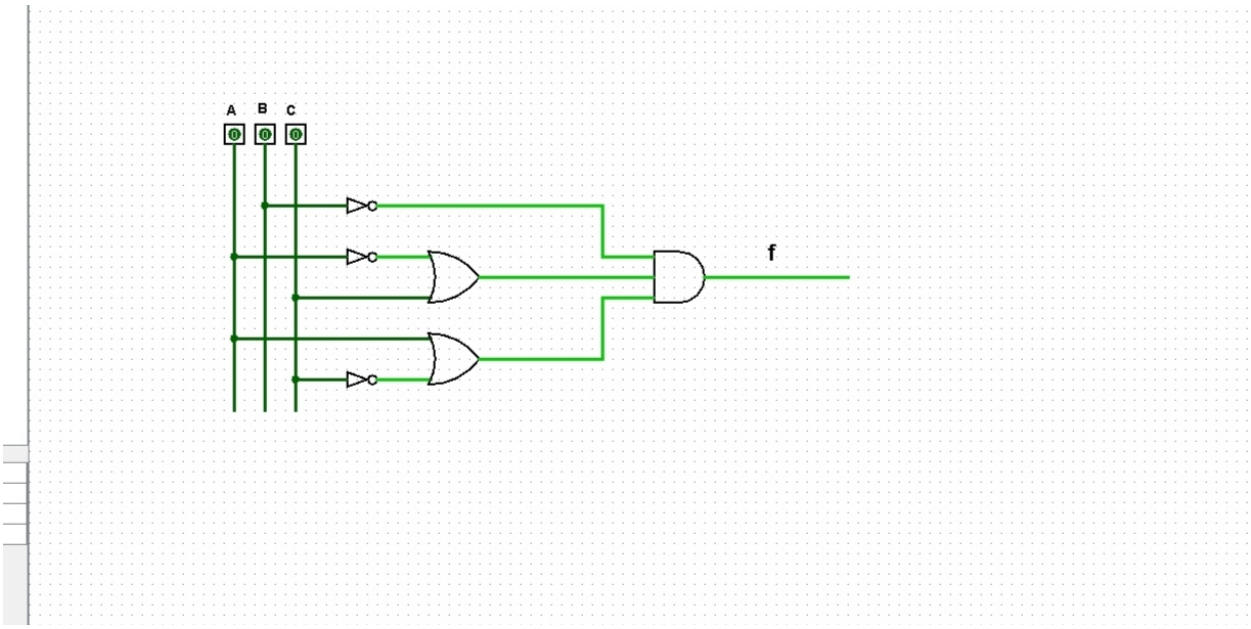
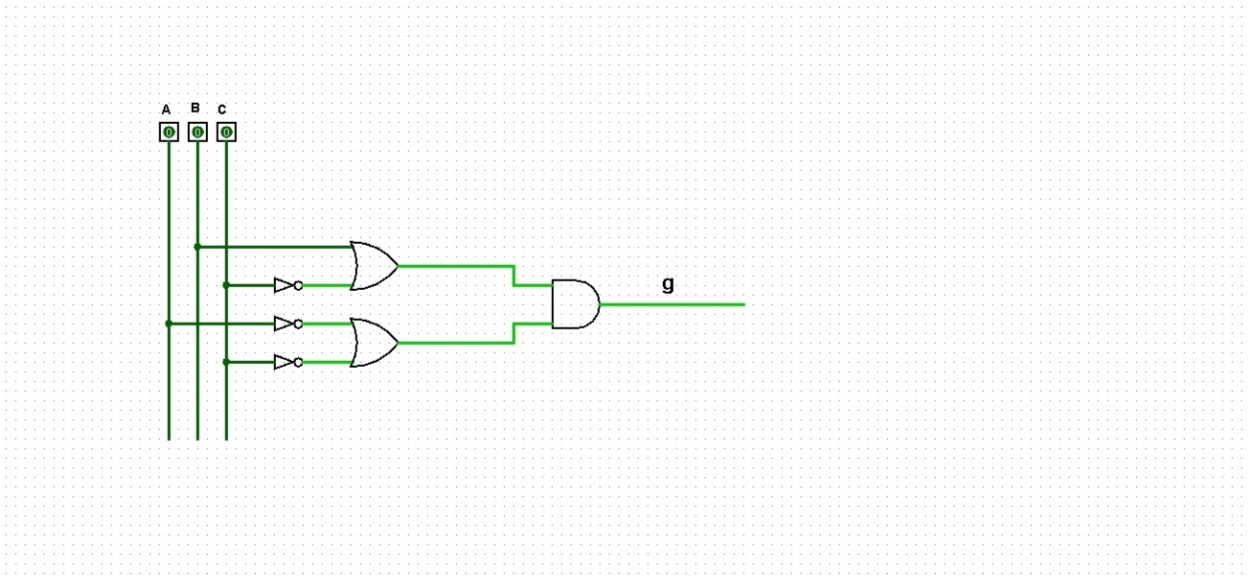

A
B
C
f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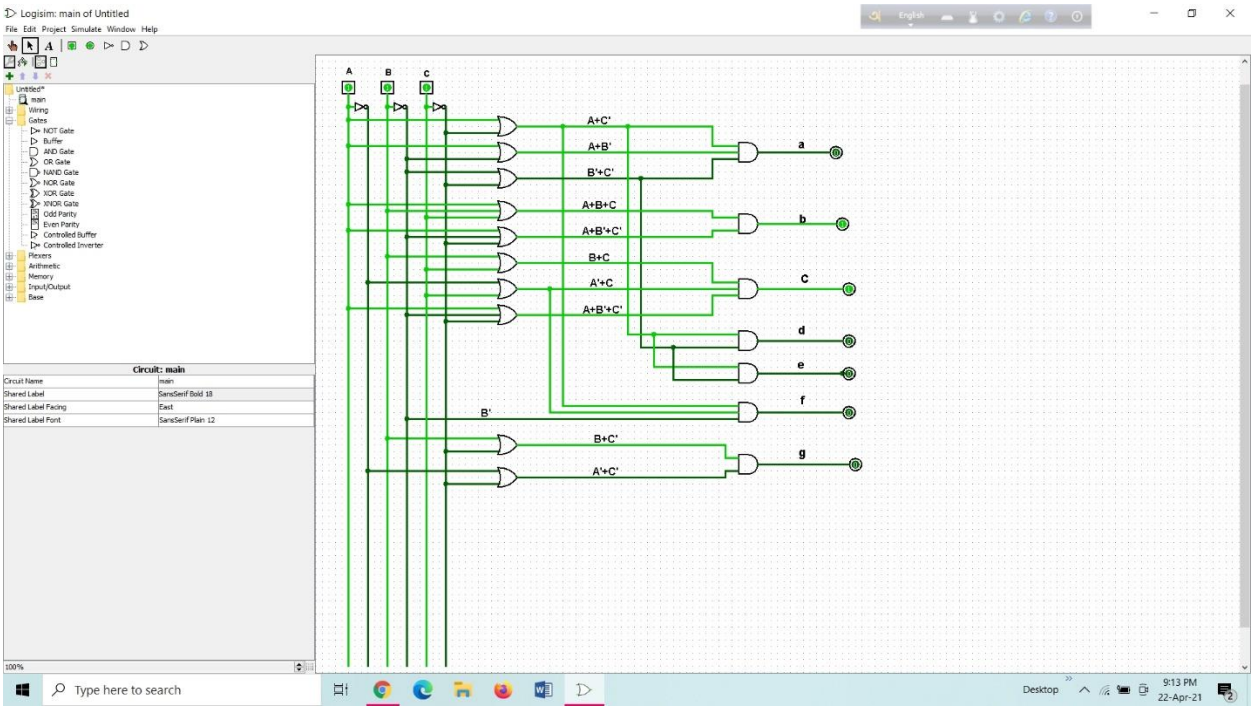
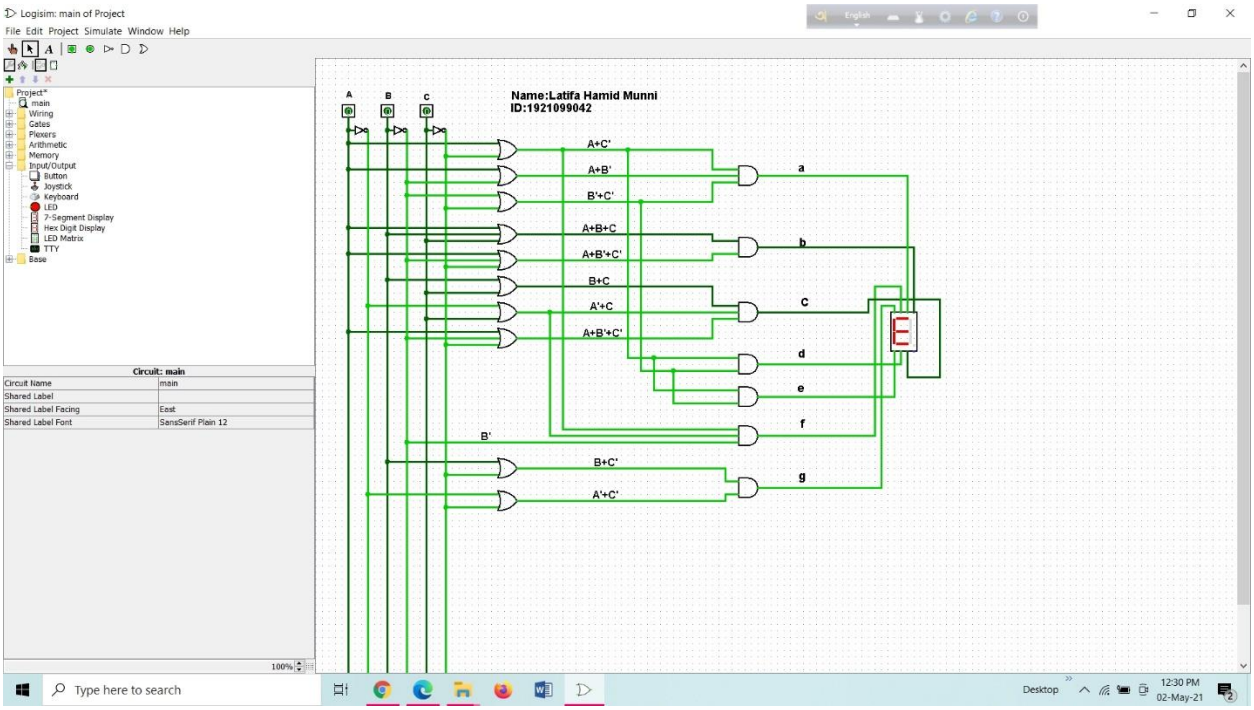
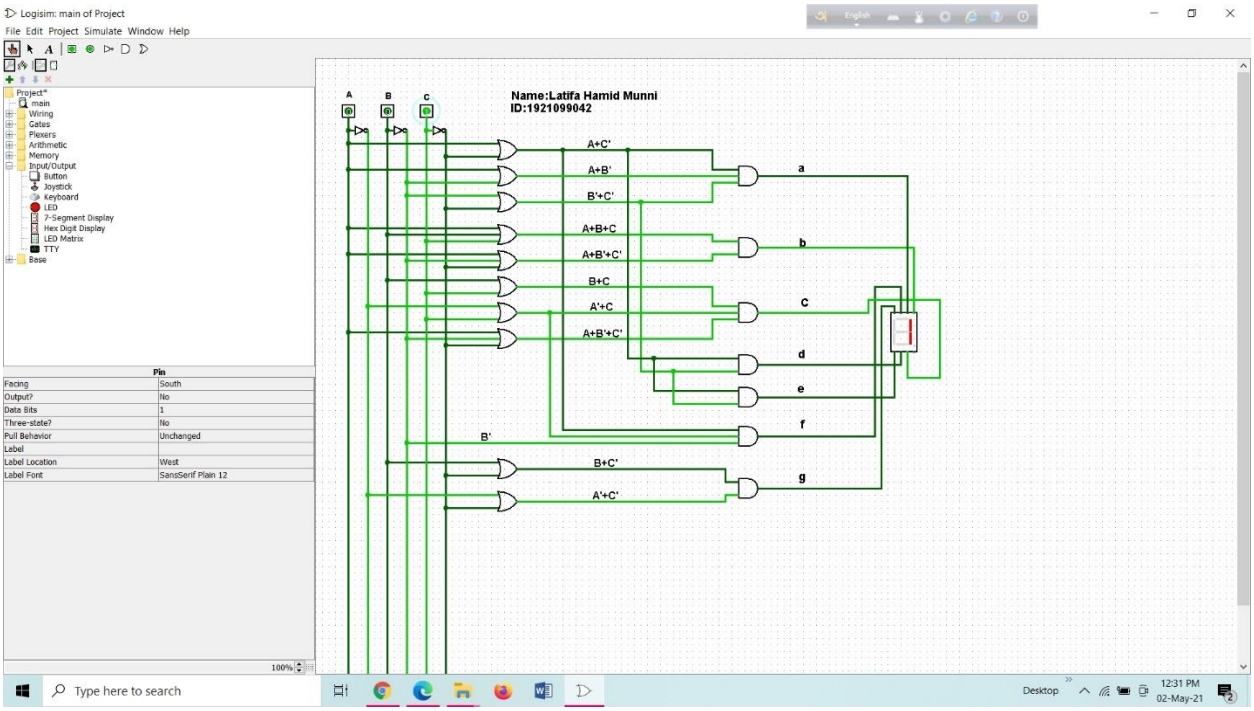


Seven Segment Display Of : Eid – 2021 (POS) by Latifa

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ID:1921099042
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Pin
Facing South
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
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Label Location West
Label Font SansSerif Plain 12
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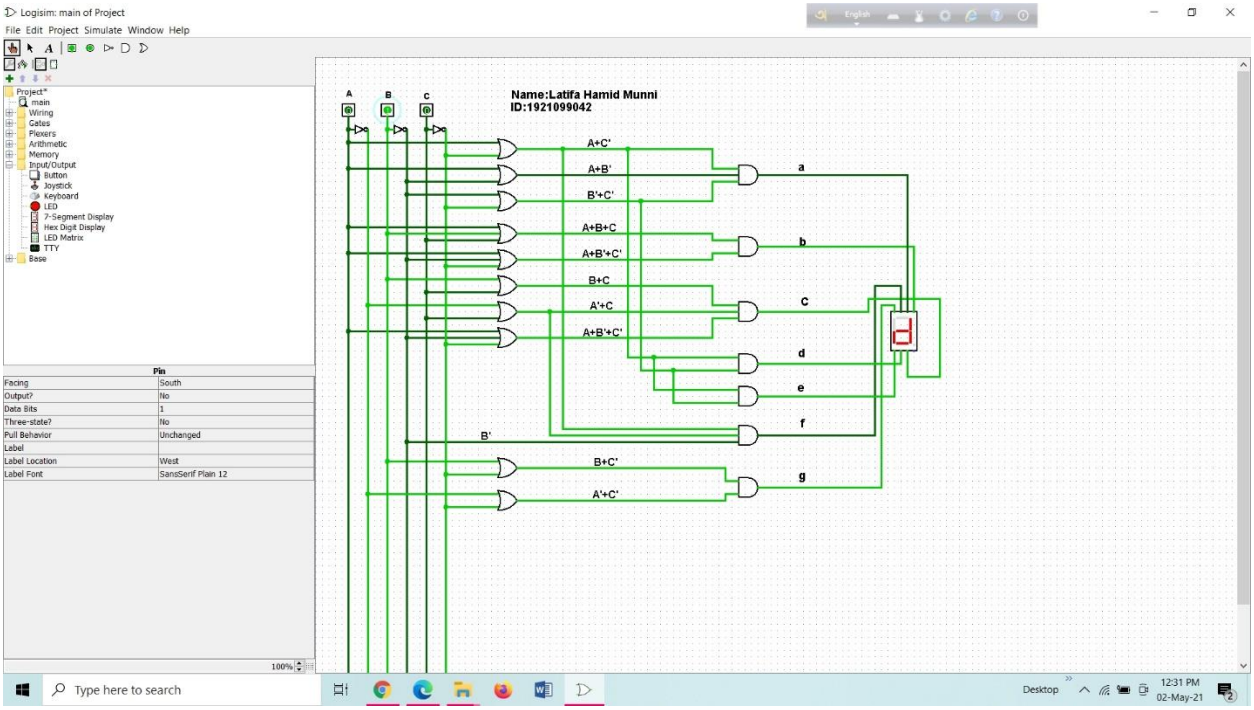
02-May-21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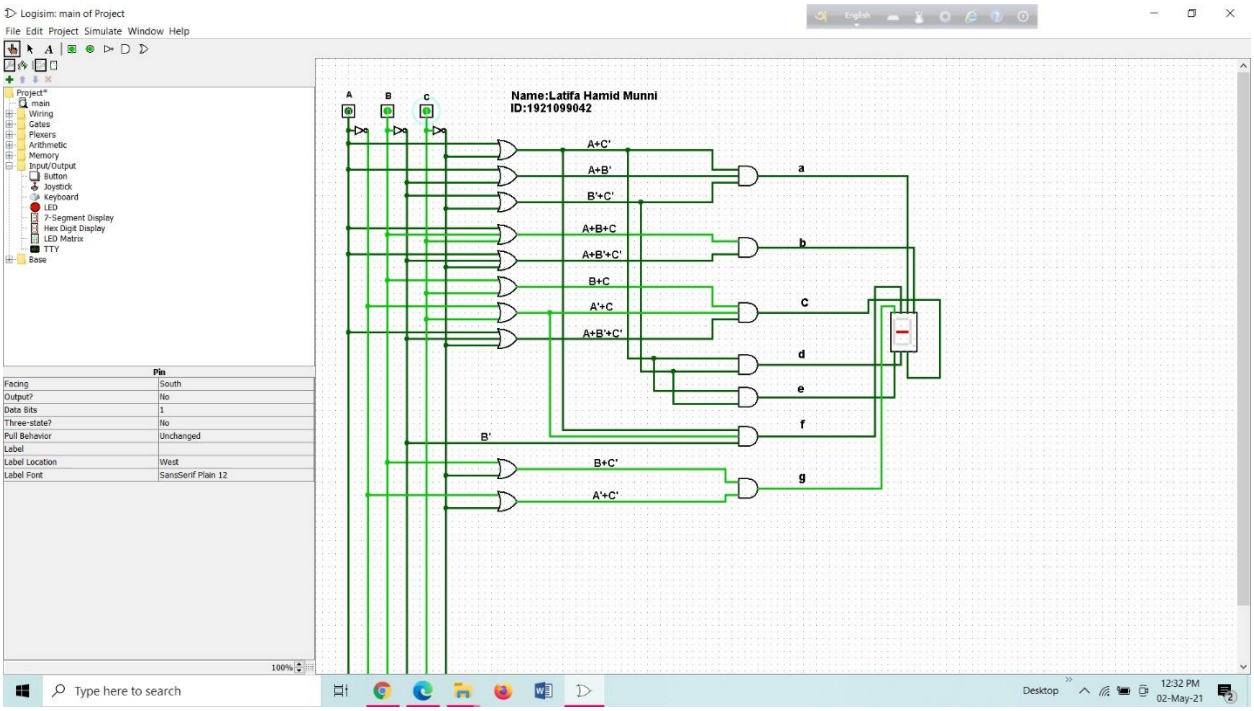
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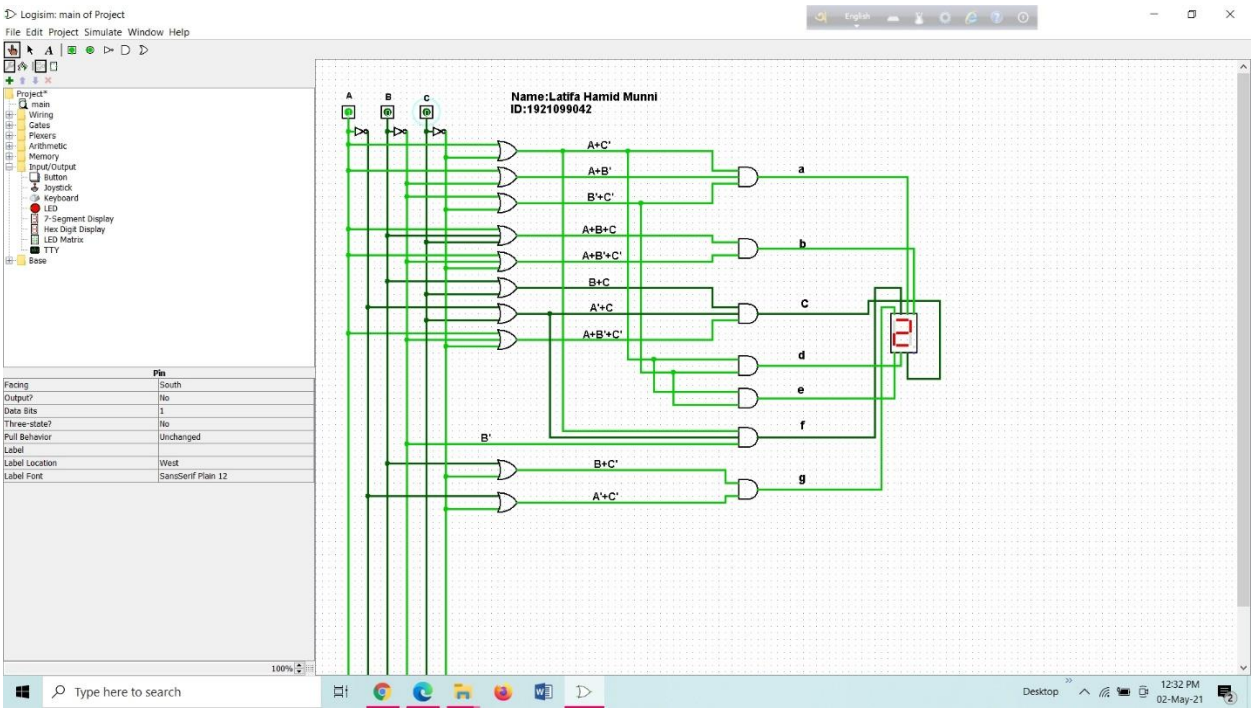
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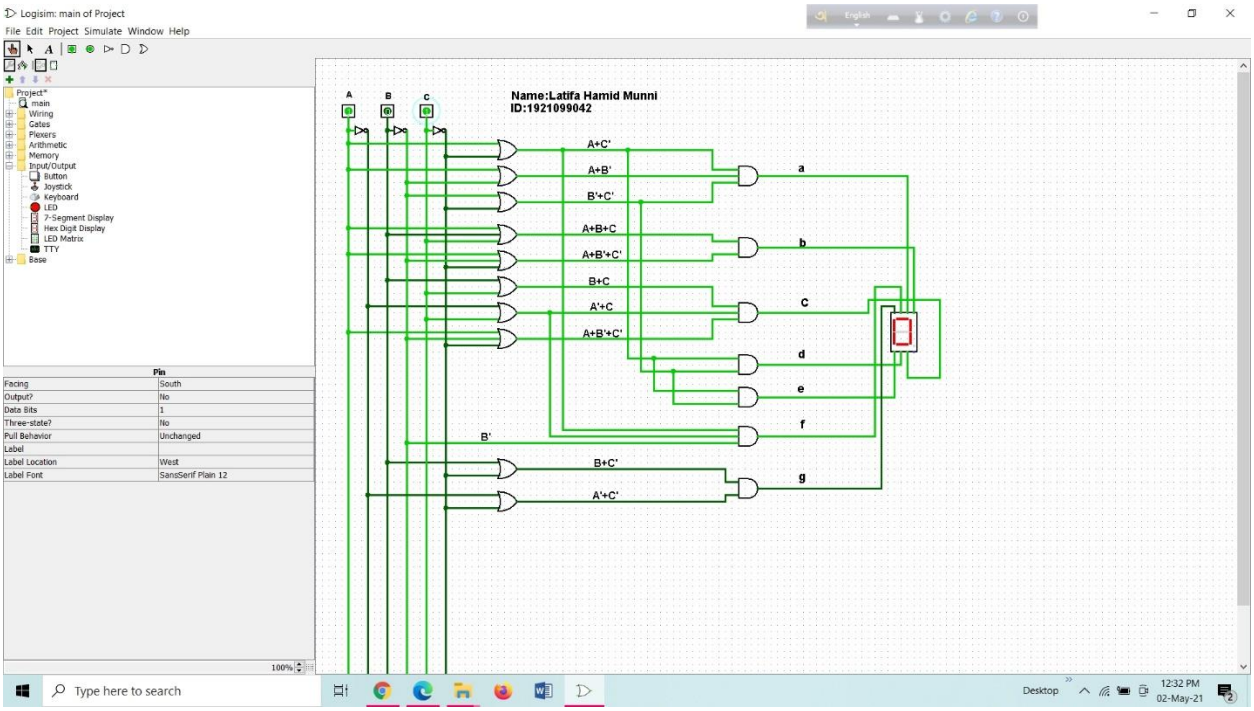
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Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label
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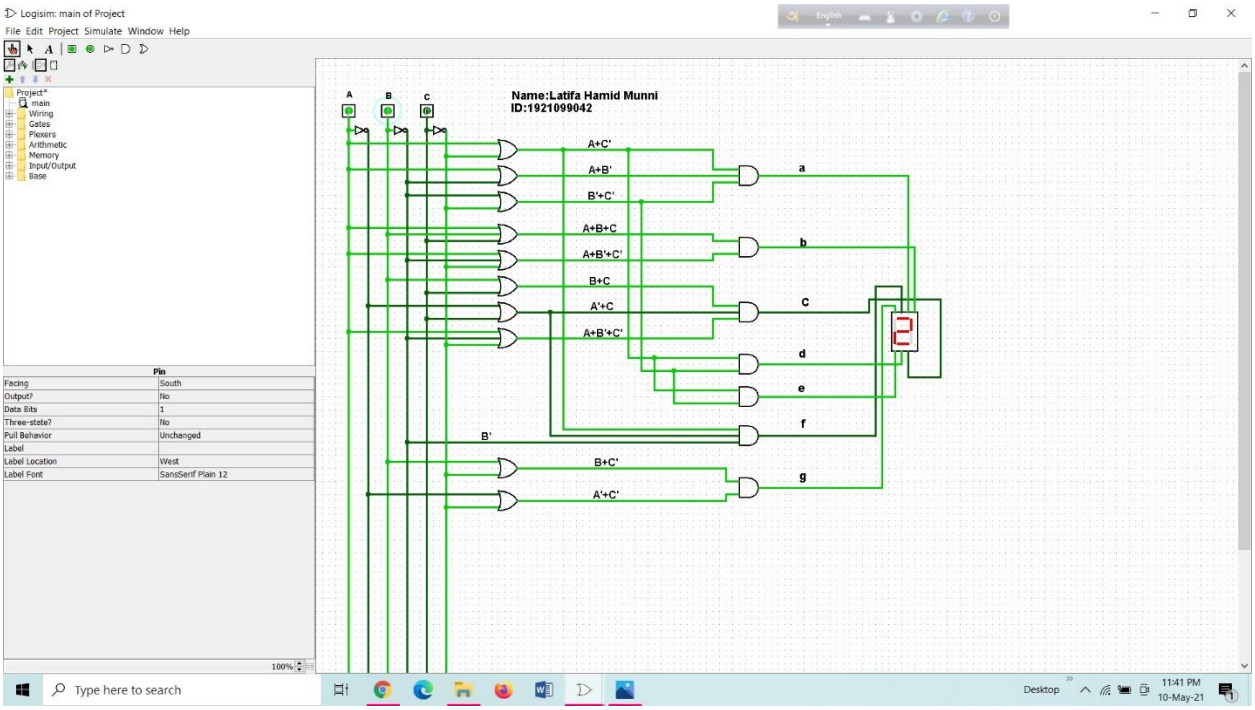
02-May-21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g
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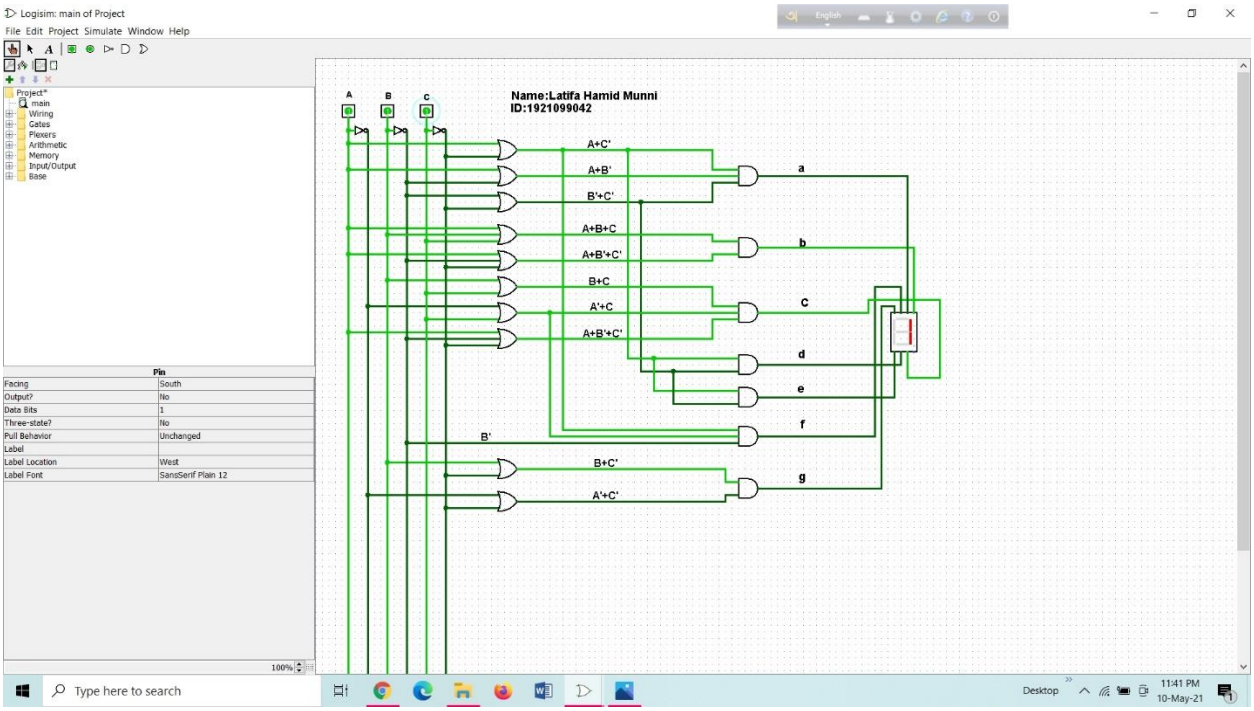
10-May-21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Project*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing South
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label
Label Location West
Label Font SansSerif Plain 12
100%
A
B
C
Name:Latifa Hamid Munni
ID:1921099042
A+C'
A+B'
B'+C'
A+B+C
A+B'+C'
B+C
A'+C
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10-May-21

About 555 timer :

The 555 timer is a single chip version of a commonly used circuit called a multivibrator which is useful in a wide variety of electronic circuits. The 555 timer chips probably the most popular integrated circuit ever made

The 555 timer is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the timer is precisely controlled by one external resistor and capacitor

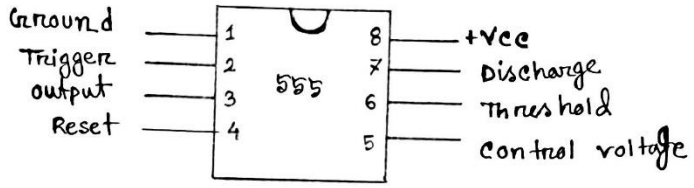


Figure : A 555 - timer chip

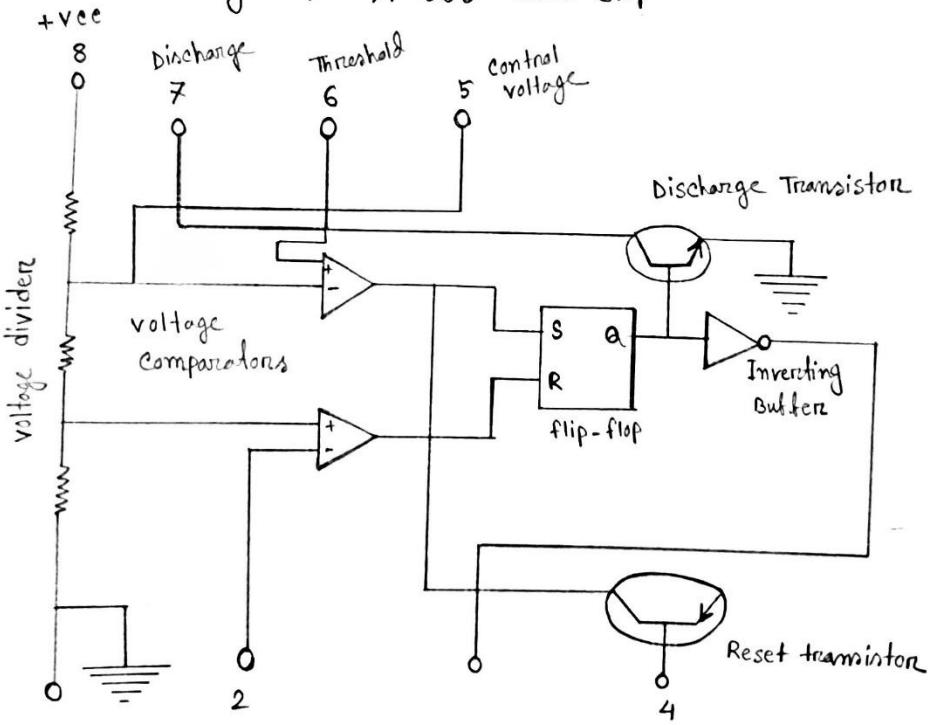
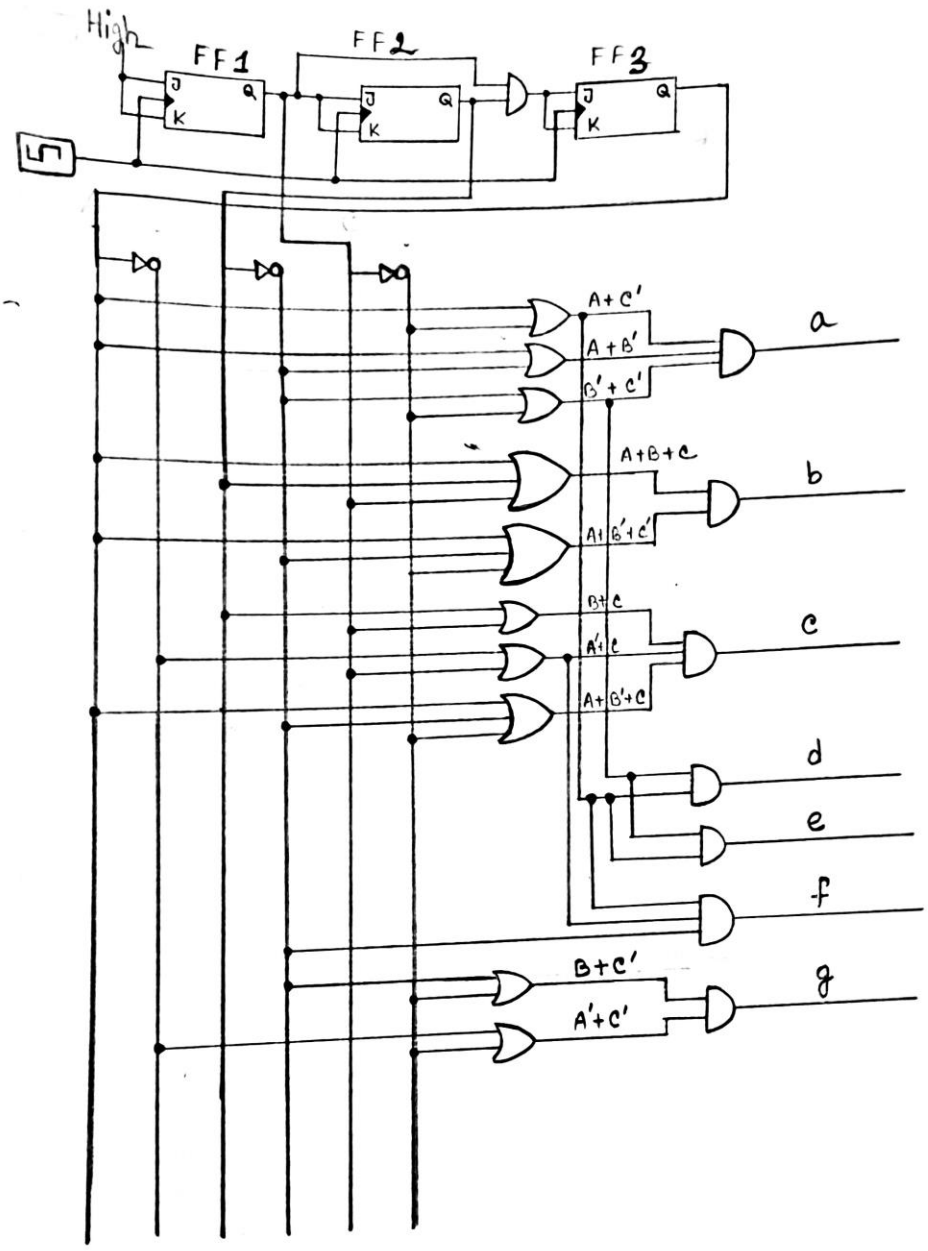
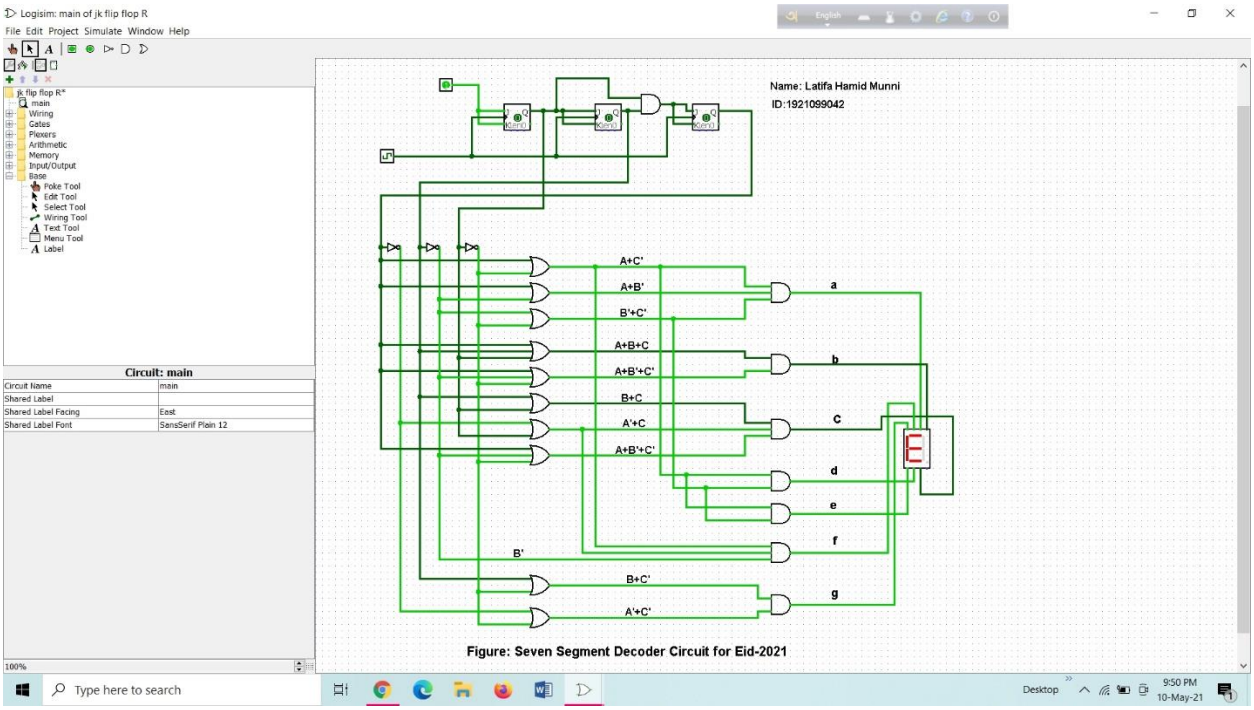


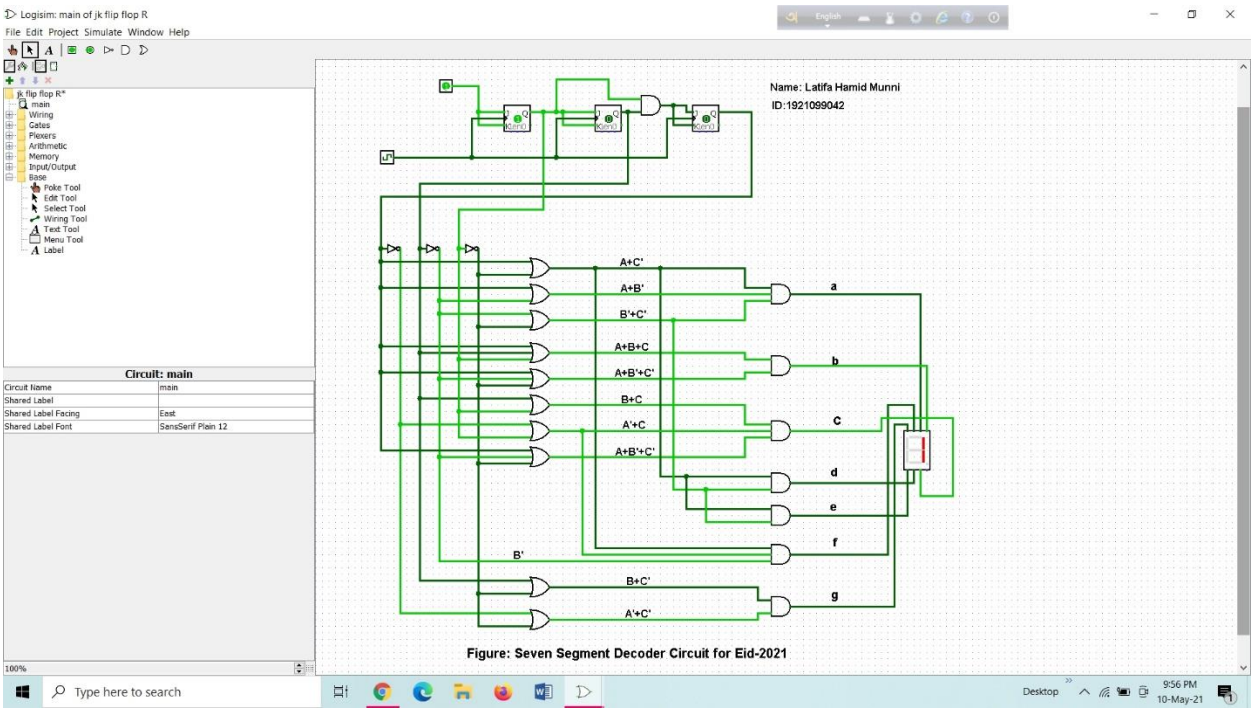
Figure : Internal construction of 555 timer

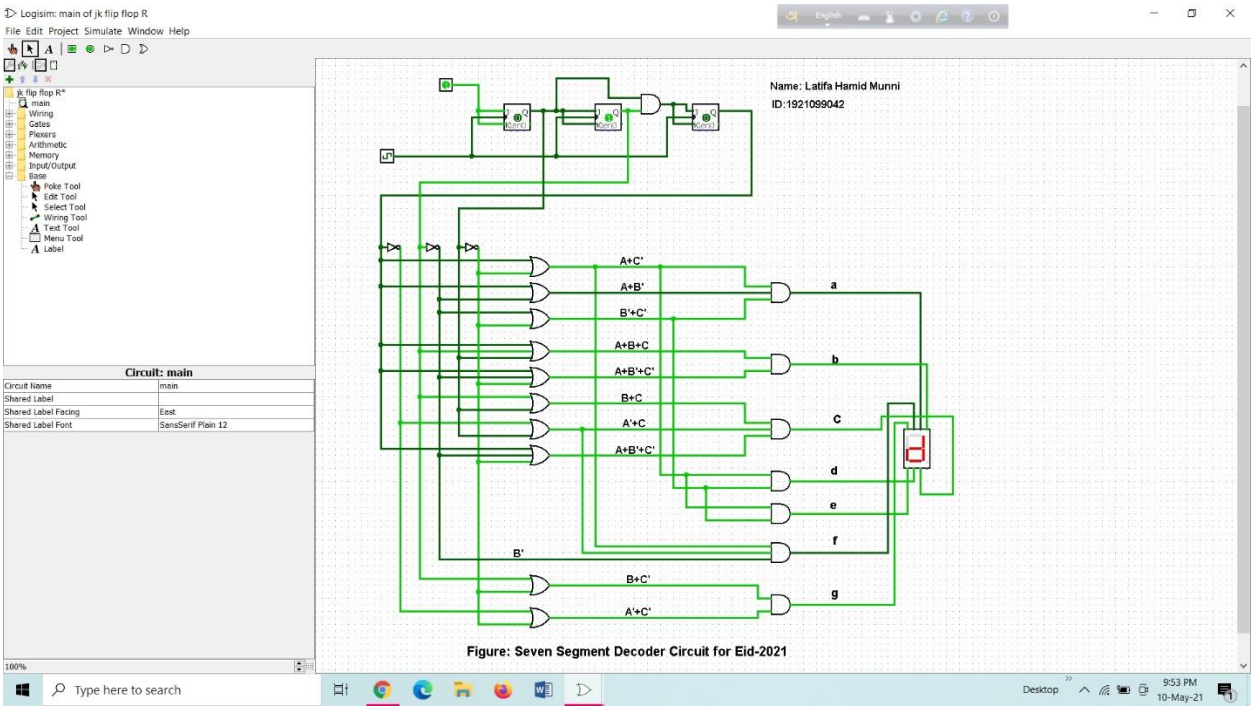


Project figure: The seven segment Decoder circuit for Eid-2021 with 3 bit synchronous counter

3 bit Synchronous counter with j k flip flop by Latifa:






Logisim: main of jk flip flop R
File Edit Project Simulate Window Help
jk flip flop R*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Poke Tool
Edit Tool
Select Tool
Wiring Tool
Text Tool
Menu Tool
Label
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Name: Latifa Hamid Munni
ID:1921099042
A+C'
A+B'
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B+C
A'+C
A+B'+C'
B'
B+C'
A'+C'
a
b
c
d
e
f
g
Figure: Seven Segment Decoder Circuit for Eid-2021
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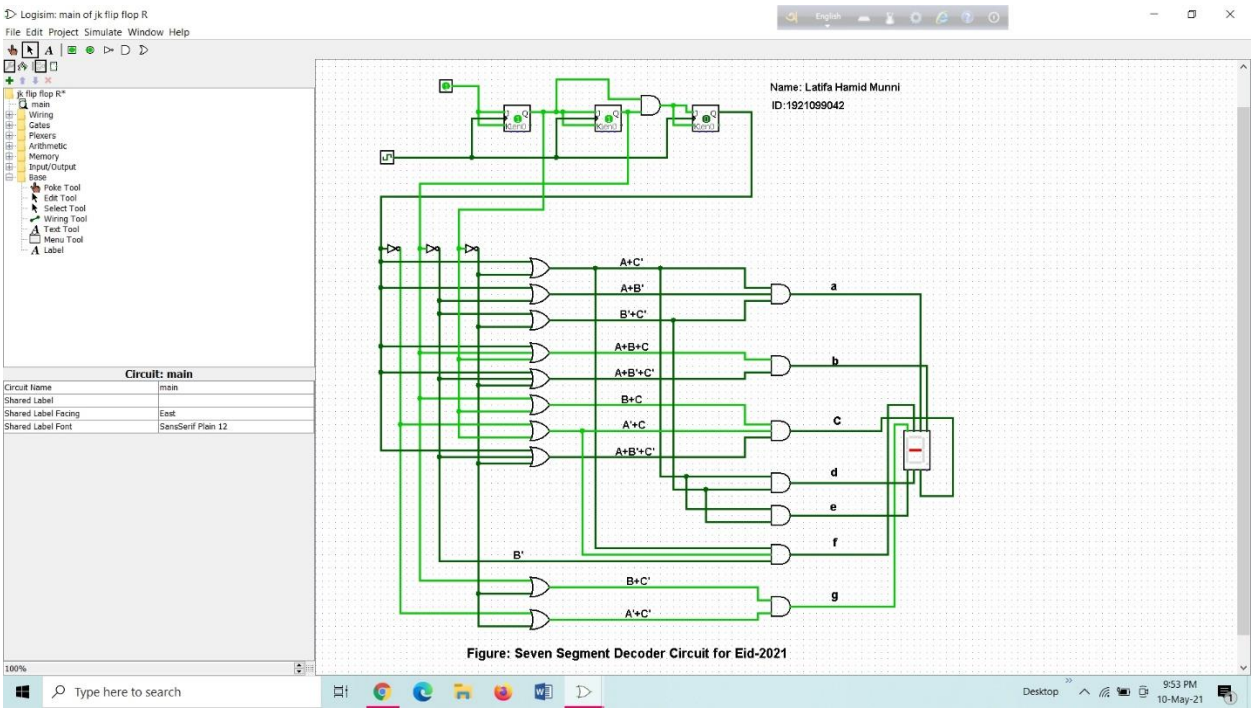
10-May-21


Logisim: main of jk flip flop R
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jk flip flop R*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Poke Tool
Edit Tool
Select Tool
Wiring Tool
Text Tool
Menu Tool
Label
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Name: Latifa Hamid Munni
ID:1921099042
A+C'
A+B'
B'+C'
A+B+C
A+B'+C'
B+C
A'+C
A+B'+C'
B'
B+C'
A'+C'
a
b
c
d
e
f
g
Figure: Seven Segment Decoder Circuit for Eid-2021
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10-May-21

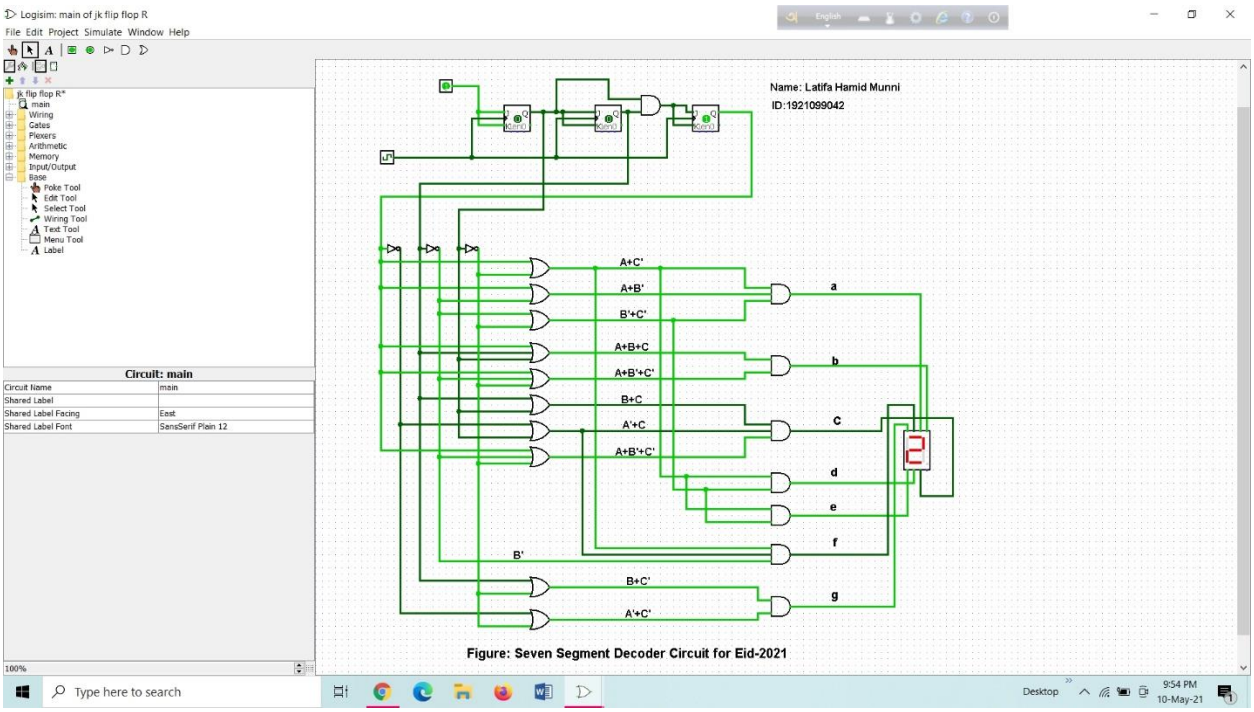


Figure: Seven Segment Decoder Circuit for Eid-2021

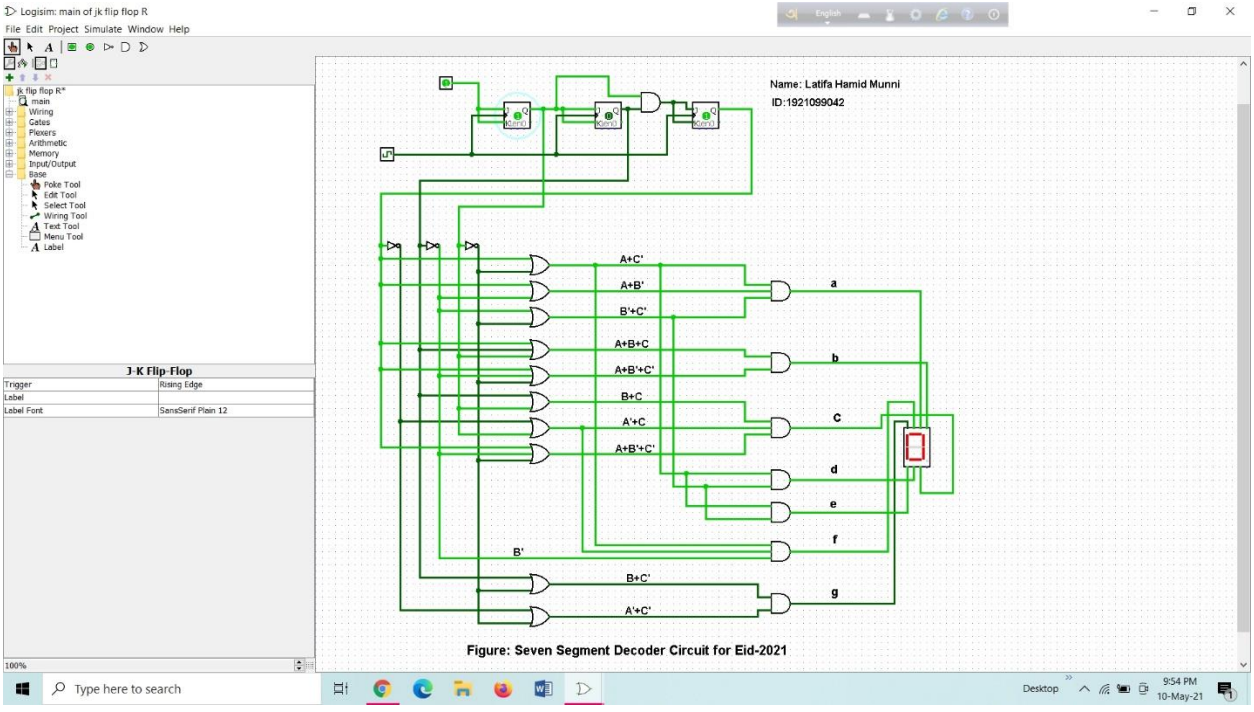


Figure: Seven Segment Decoder Circuit for Eid-2021

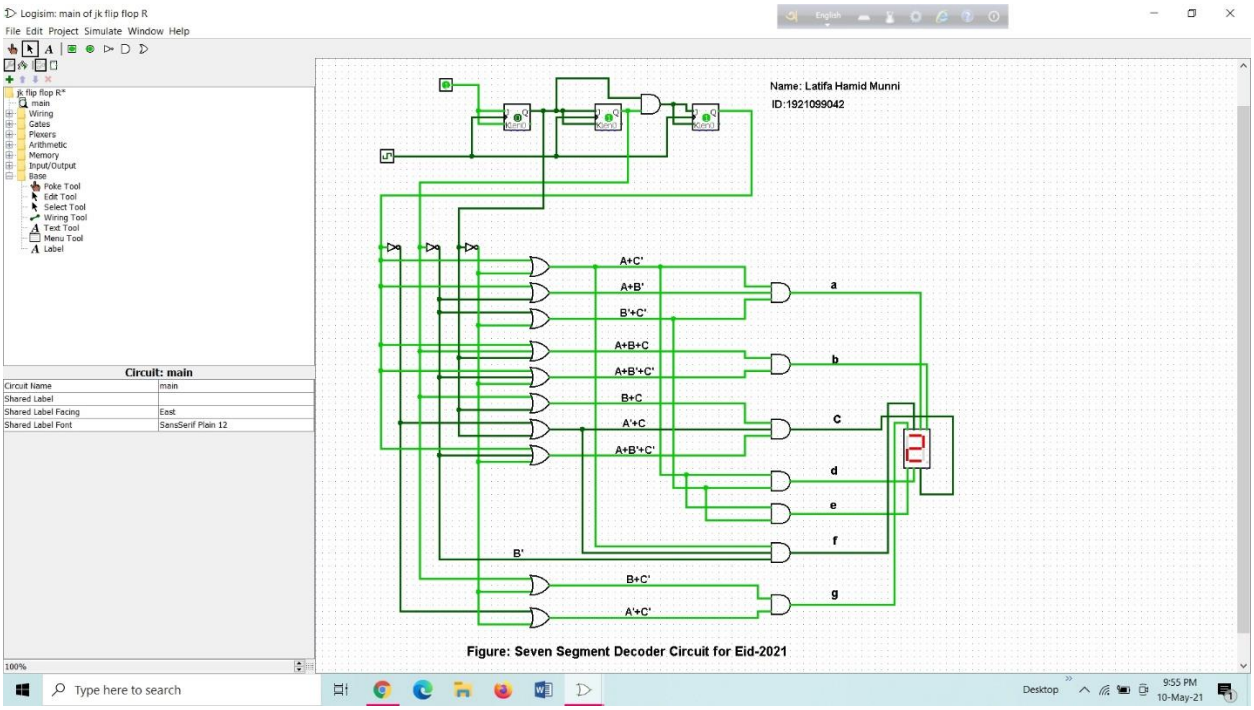


Figure: Seven Segment Decoder Circuit for Eid-2021

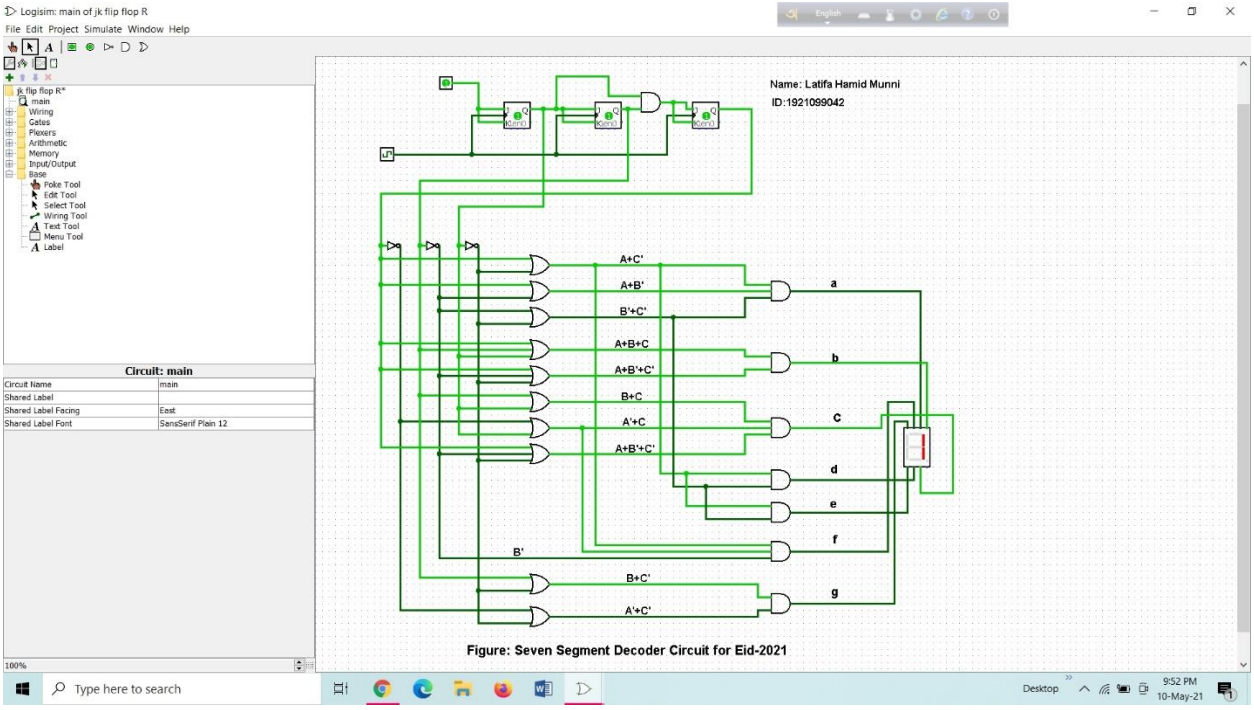


Figure: Seven Segment Decoder Circuit for Eid-2021

Using (SOP) by Arman:

Project Name : EID-2021 (Display by seven segment decoder).

Decimal	BCD inputs			Outputs						
Numbers	A	B	C	a	b	c	d	e	f	g
0	0	0	0	1	0	0	1	1	1	1
1	0	0	1	0	0	0	0	1	1	0
2	0	1	0	0	1	1	1	1	0	1
3	0	1	1	0	0	0	0	0	0	1
4	1	0	0	1	1	0	1	1	0	1
5	1	0	1	1	1	1	1	1	1	0
6	1	1	0	1	1	0	1	1	0	1
7	1	1	1	0	1	1	0	0	0	0

Equations :

$a = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$

$b = \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC.$

$c = \bar{A}B\bar{C} + A\bar{B}C + ABC.$

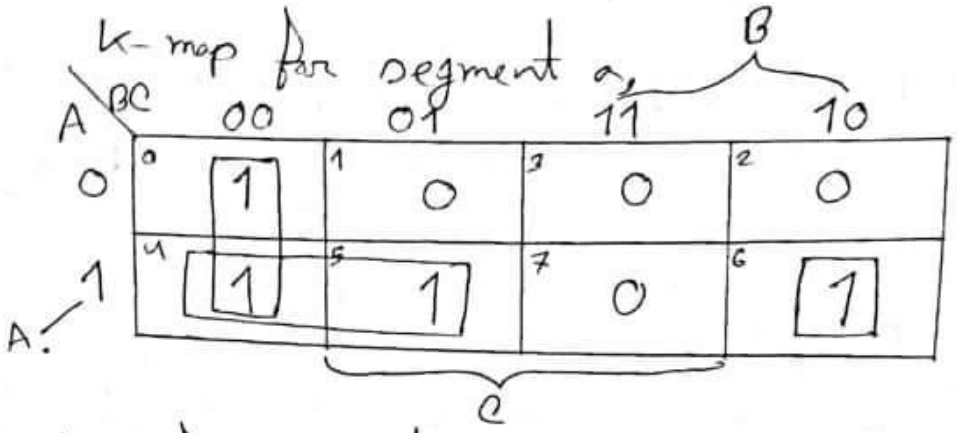
$d = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$

$e = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$

$f = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}C.$

$g = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$

K-map for segment a,



∴ Logic for segment a = $\bar{B}\bar{C} + A\bar{B} + A\bar{C}$

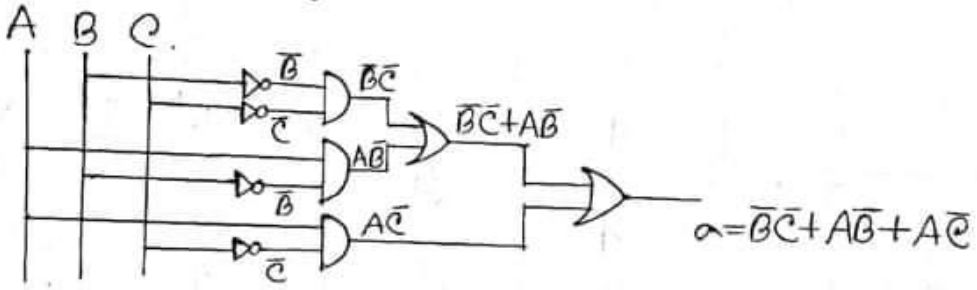
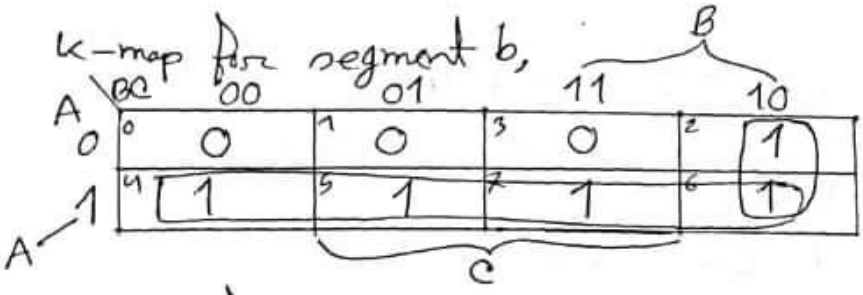


Figure: Logic circuit for segment a.

K-map for segment b,



∴ Logic for segment b = $B\bar{C} + A$

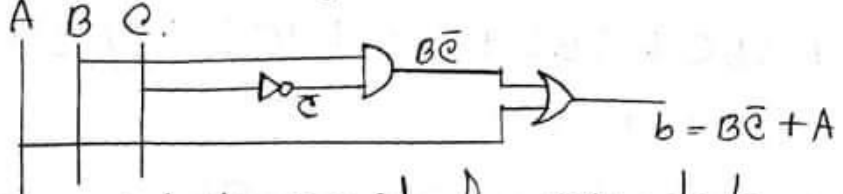
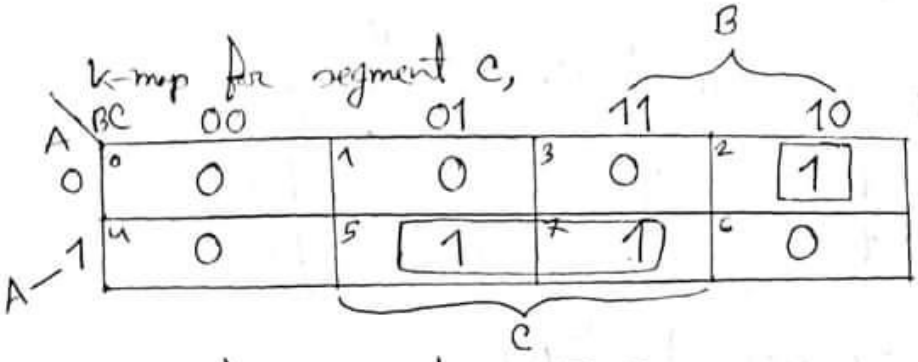


Figure: Logic circuit for segment b.



∴ Logic for segment c = $\bar{A}B\bar{C} + AC$.

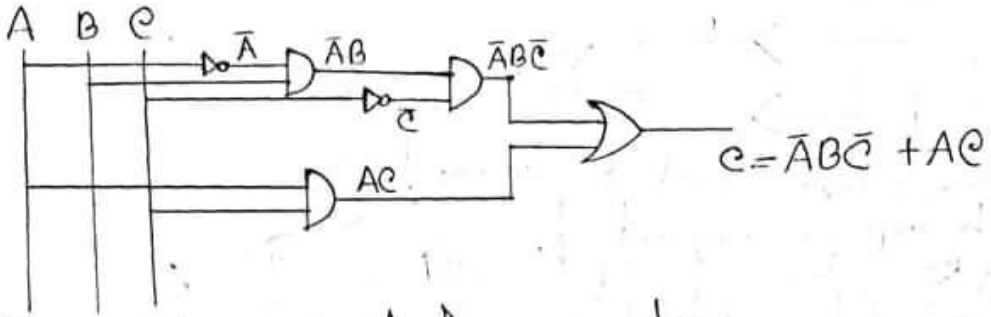
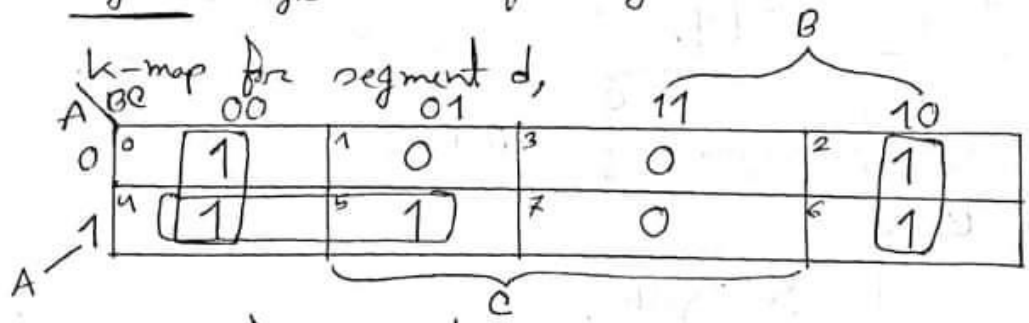


Figure : Logic circuit for segment c.



∴ Logic for segment d = $\bar{C} + A\bar{B}$

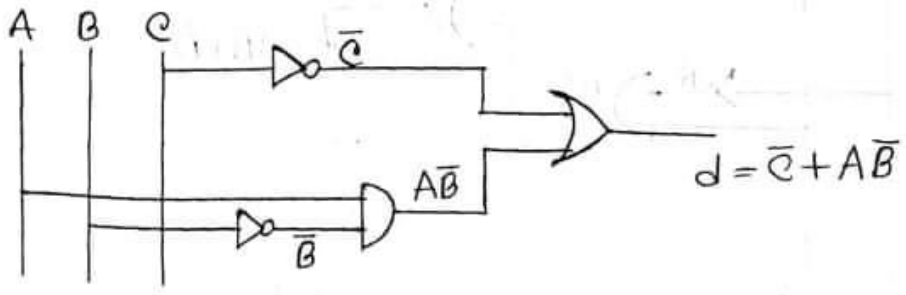
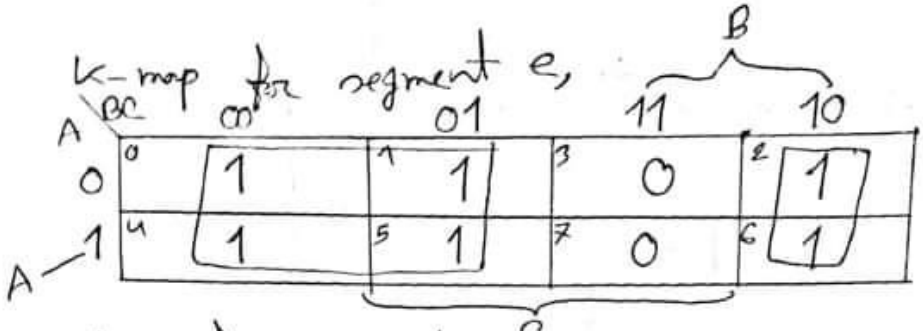


Figure : Logic circuit for segment d.

K-map for segment e,



∴ Logic for segment $e = \bar{B} + \bar{C}$

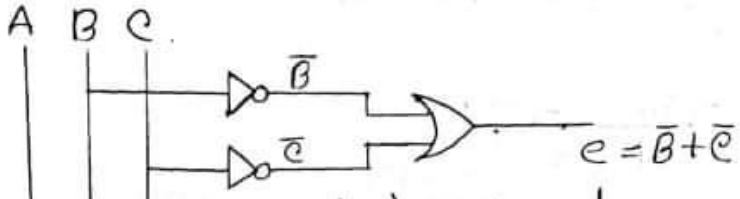
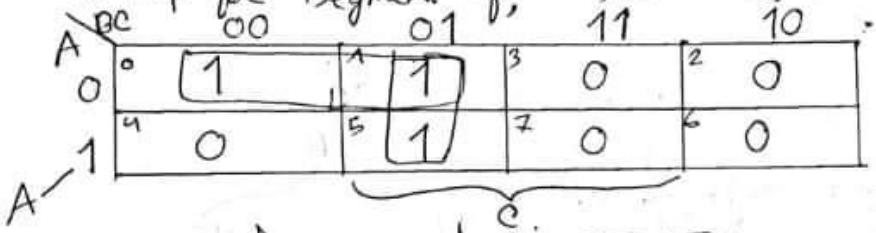


Figure : Logic circuit for segement e.

K-map for segment f,



∴ Logic for segment $f = \bar{A}\bar{B} + \bar{B}C$

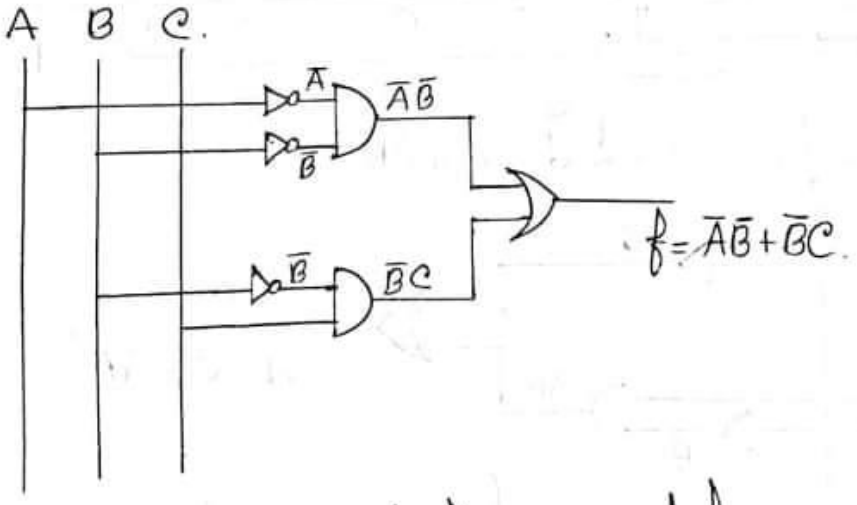
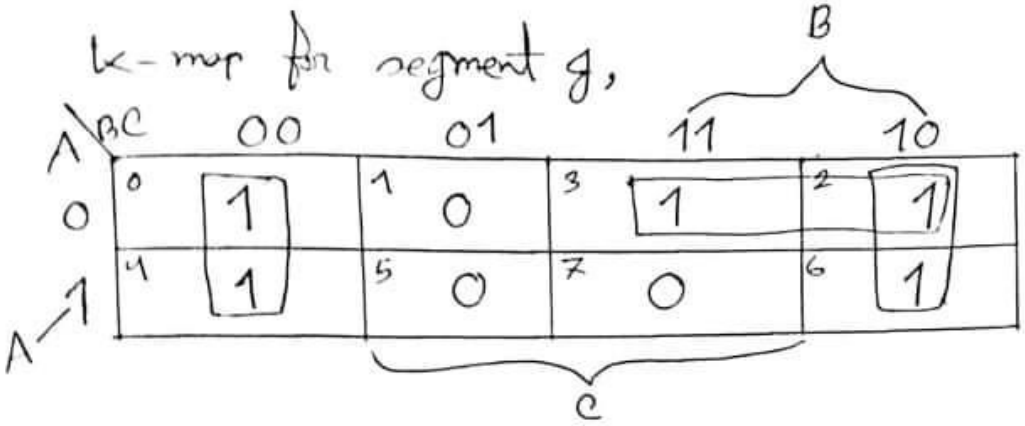


Figure : Logic circuit for segment f.

K-map for segment g,



∴ Logic for segment $g = \bar{C} + \bar{A}B$.

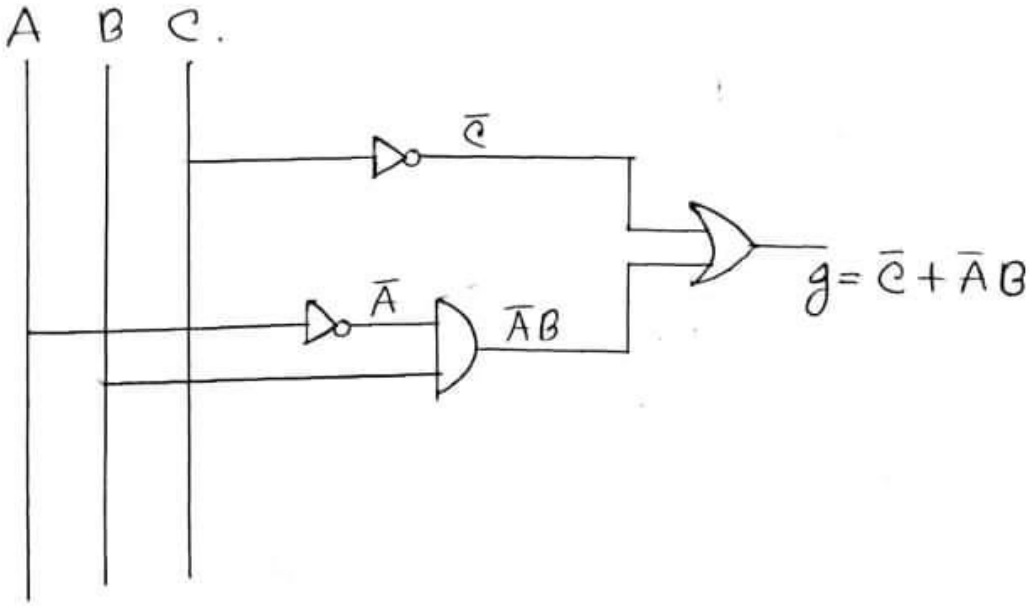


Figure : Logic circuit for segment g.

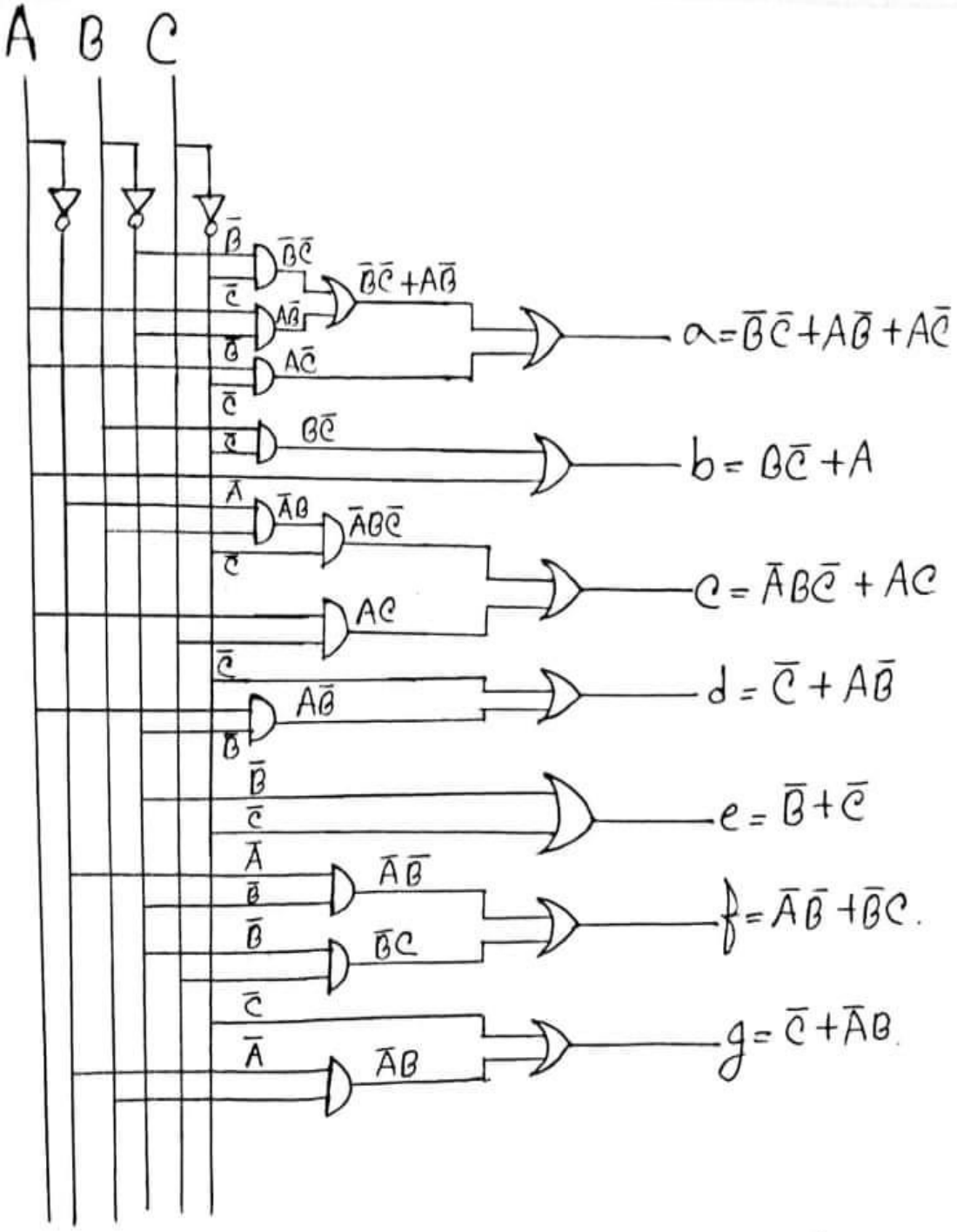


Figure: The Seven Segment Decoder circuit for EID-2021.

Name: Mosroor Mofiz Arman Course: CSE231
ID: 1921079642 Section: 10
Date: 02-05-2021

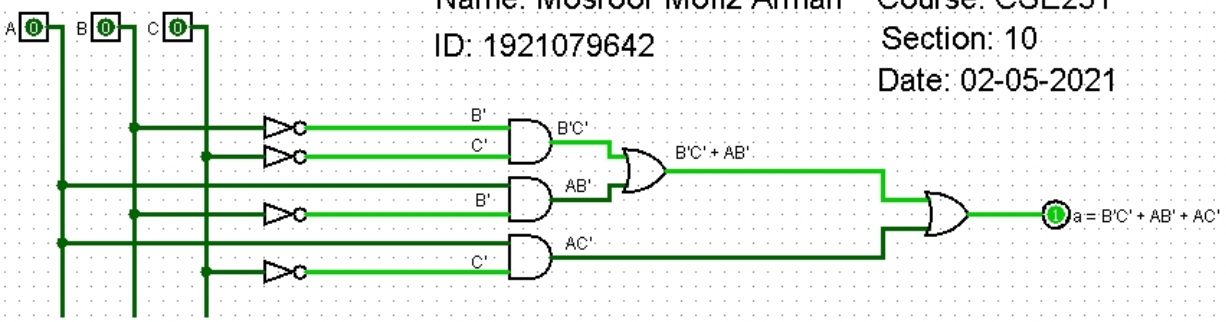


Figure: Logic circuit for segment a

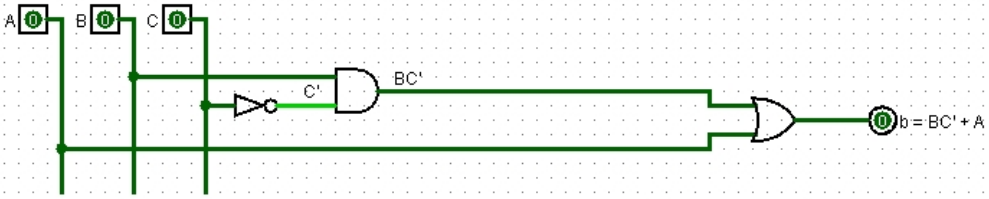


Figure: Logic circuit for segment b

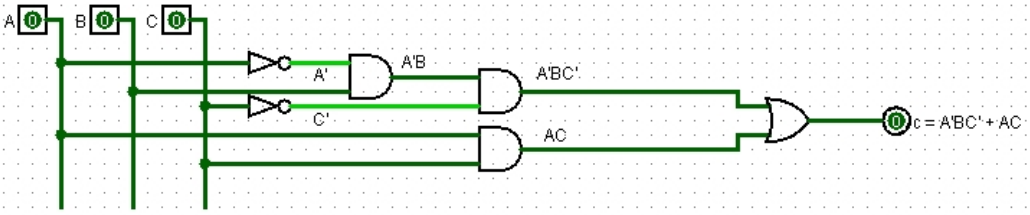


Figure: Logic circuit for segment c

Name: Mosroor Mofiz Arman Course: CSE231
ID: 1921079642 Section: 10
Date: 02-05-2021

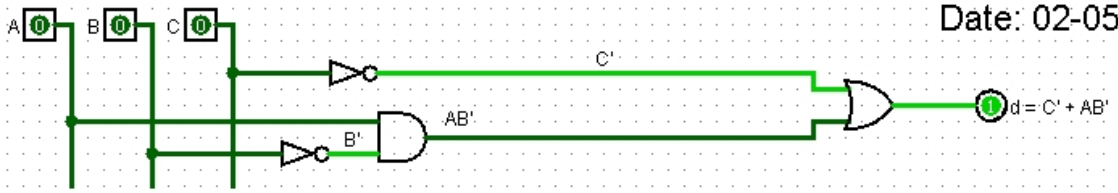


Figure: Logic circuit for segment d

Figure: Logic circuit for segment e

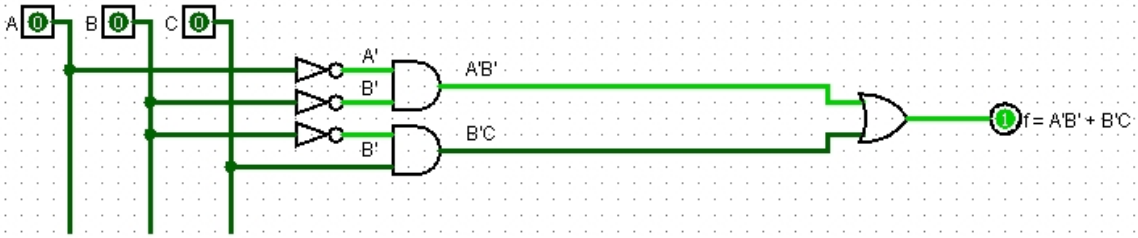


Figure: Logic circuit for segment f

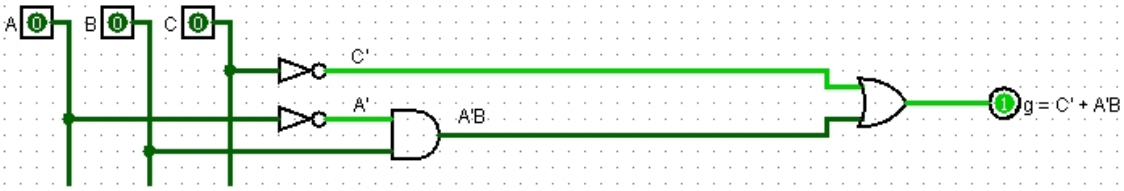


Figure: Logic circuit for segment g

Seven Segment Display (SOP) by Arman:

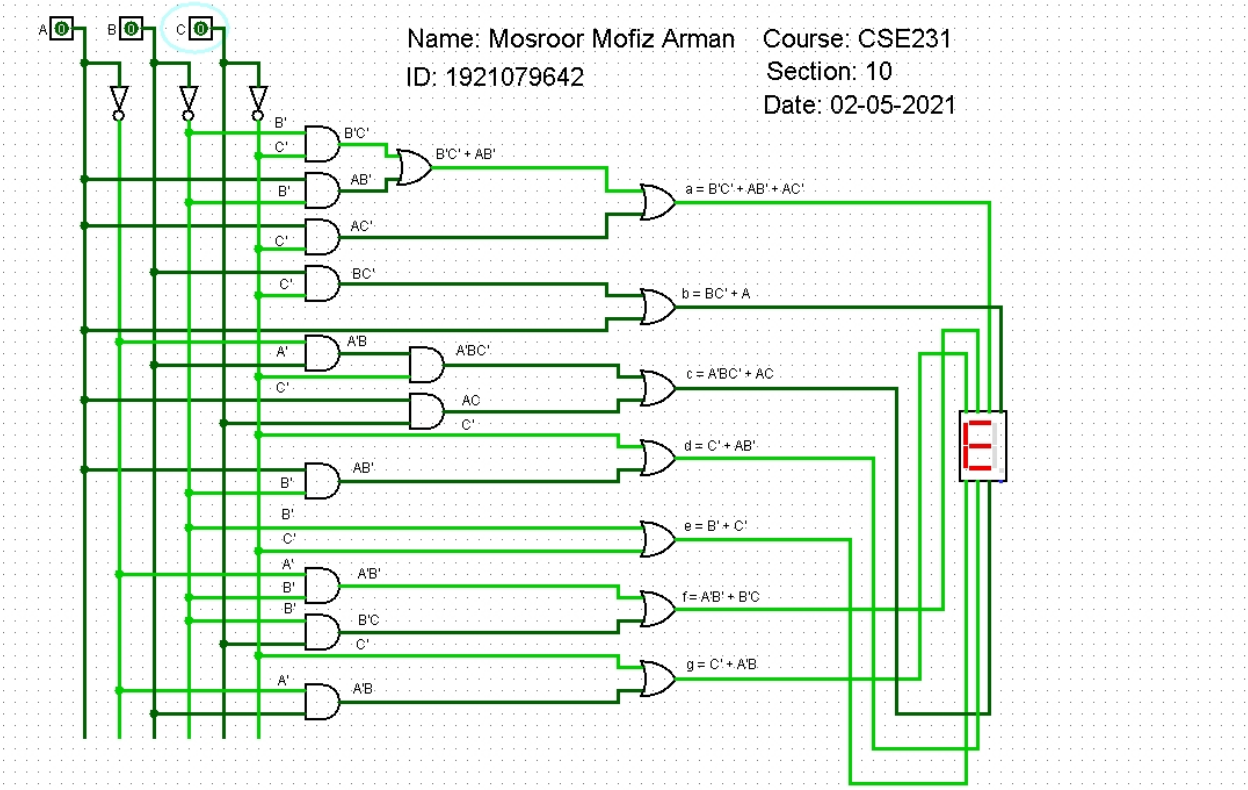


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display by Sum of Product

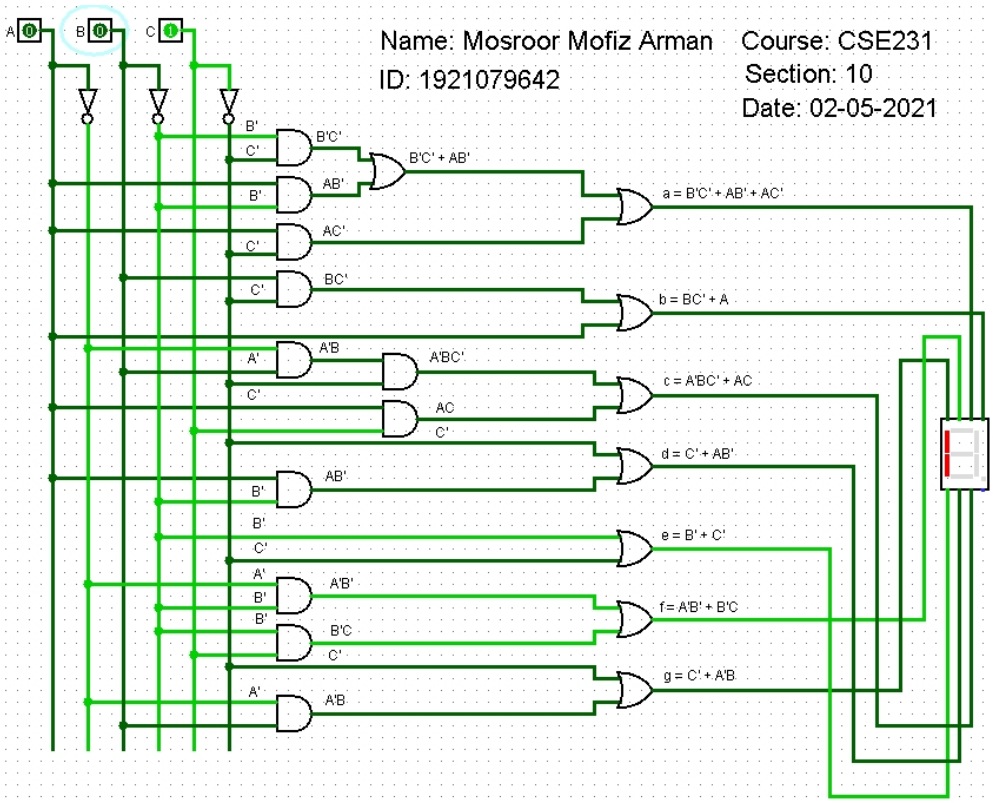


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display by Sum of Product

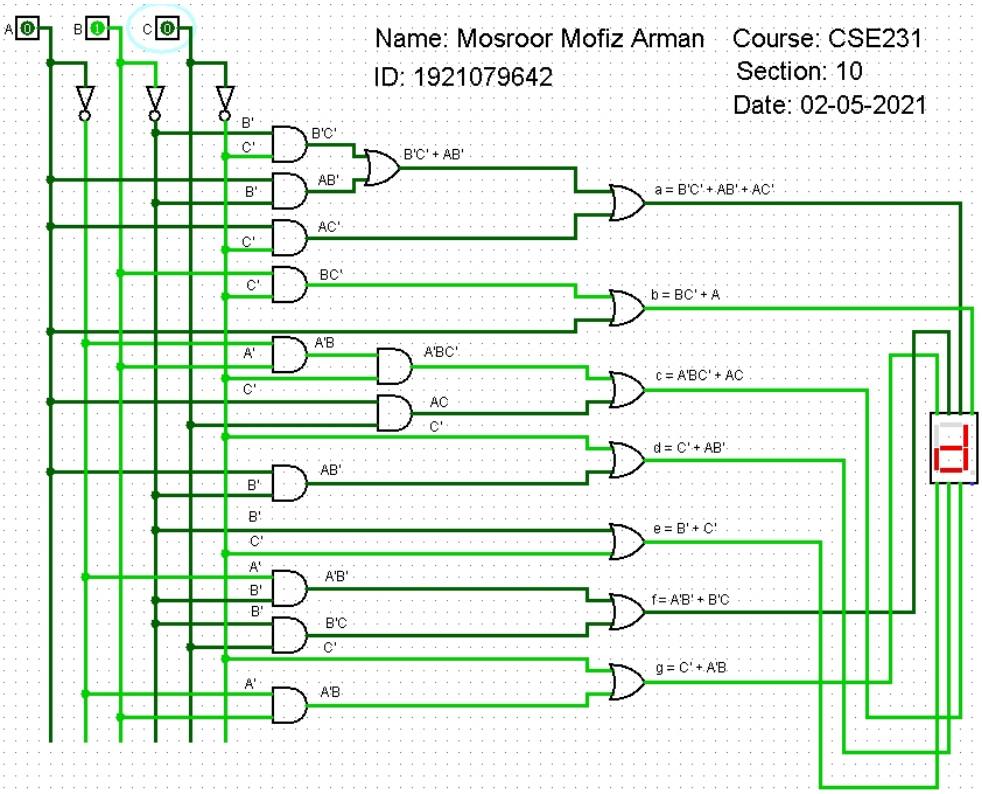


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display by Sum of Product

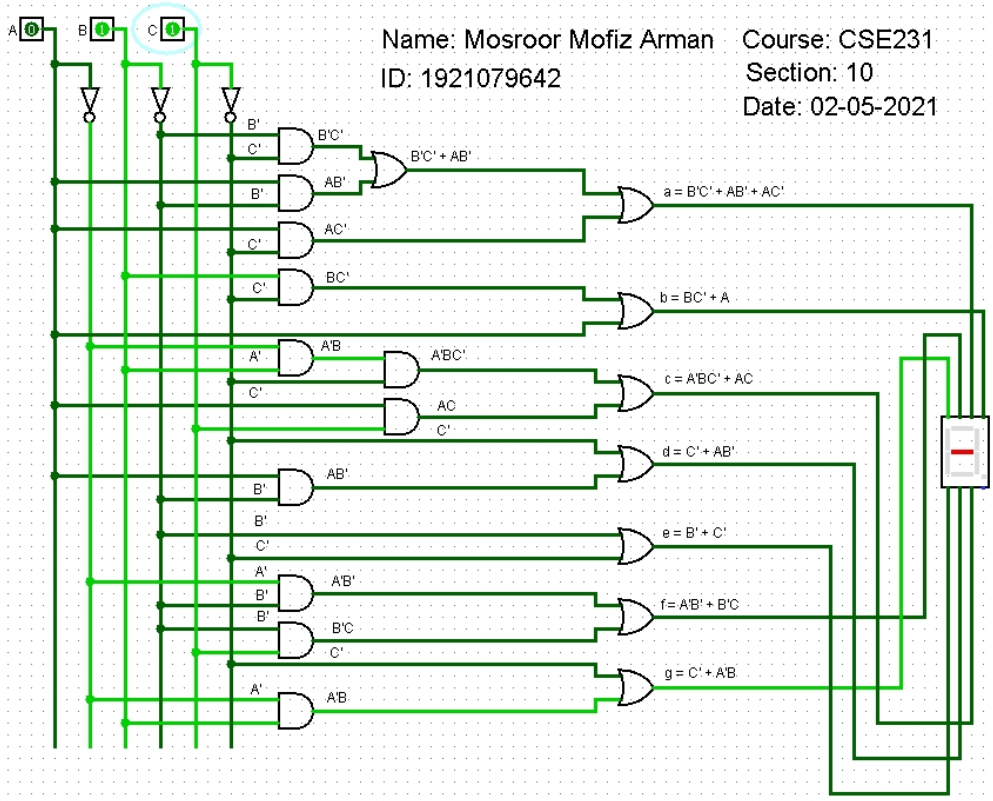


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display by Sum of Product

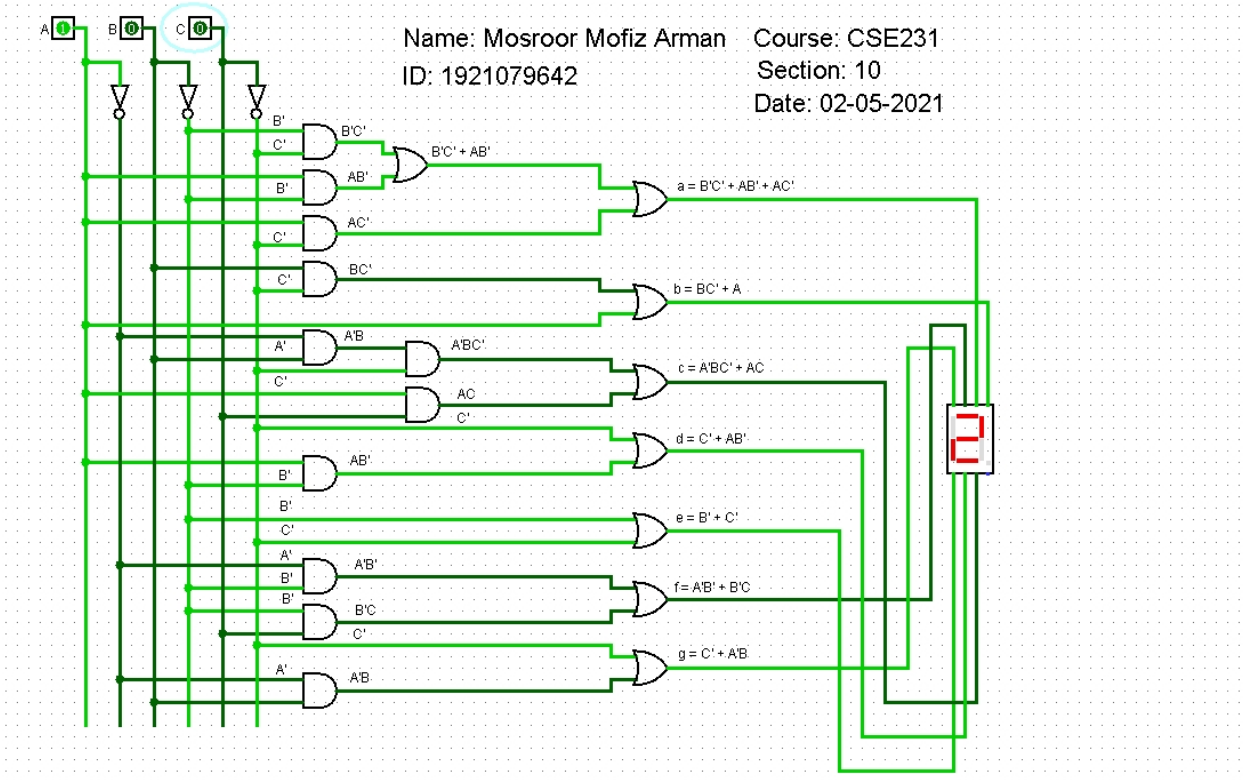


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display by Sum of Product

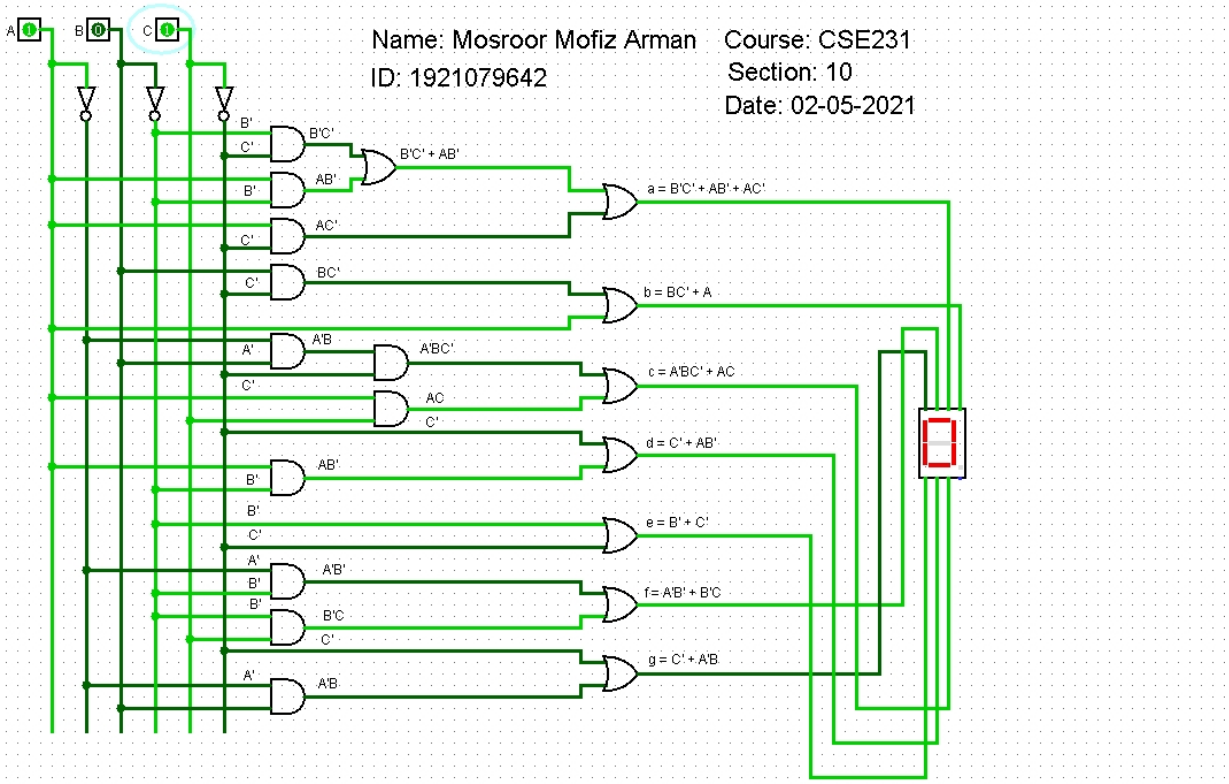


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display by Sum of Product

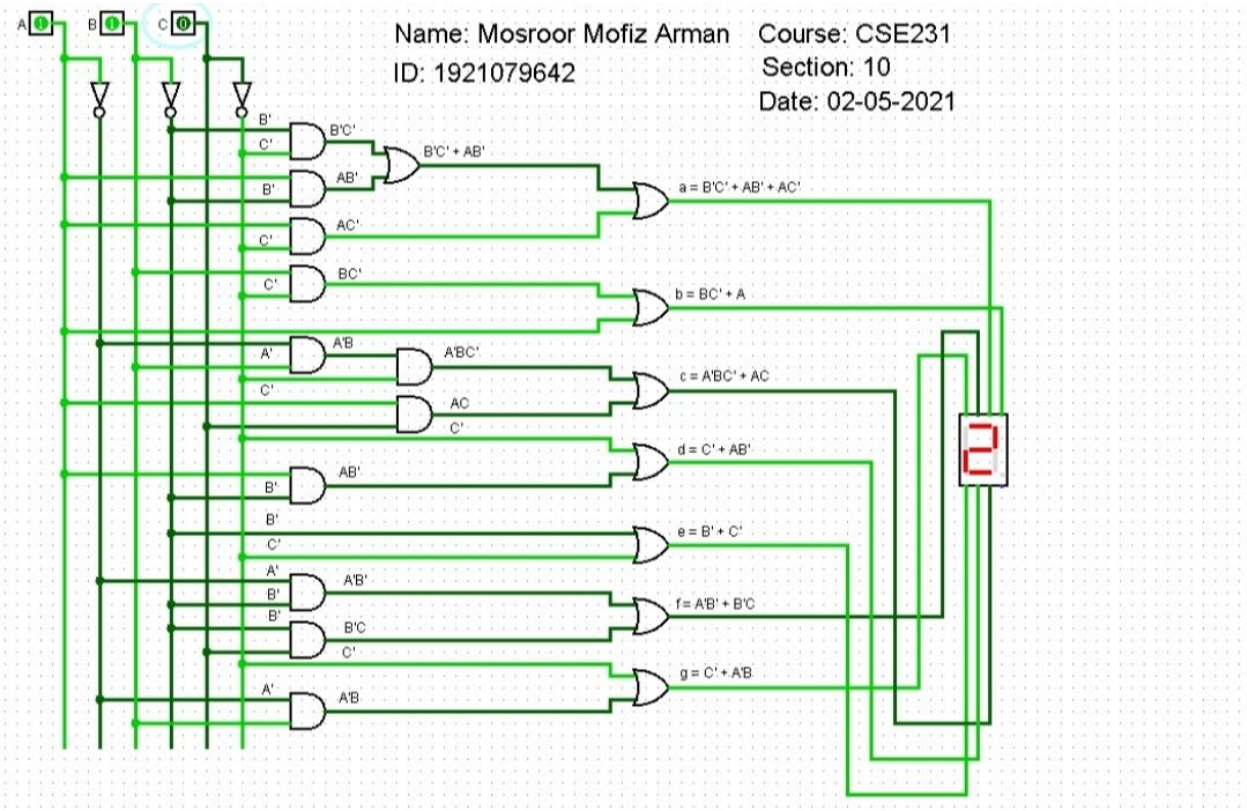


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display by Sum of Product

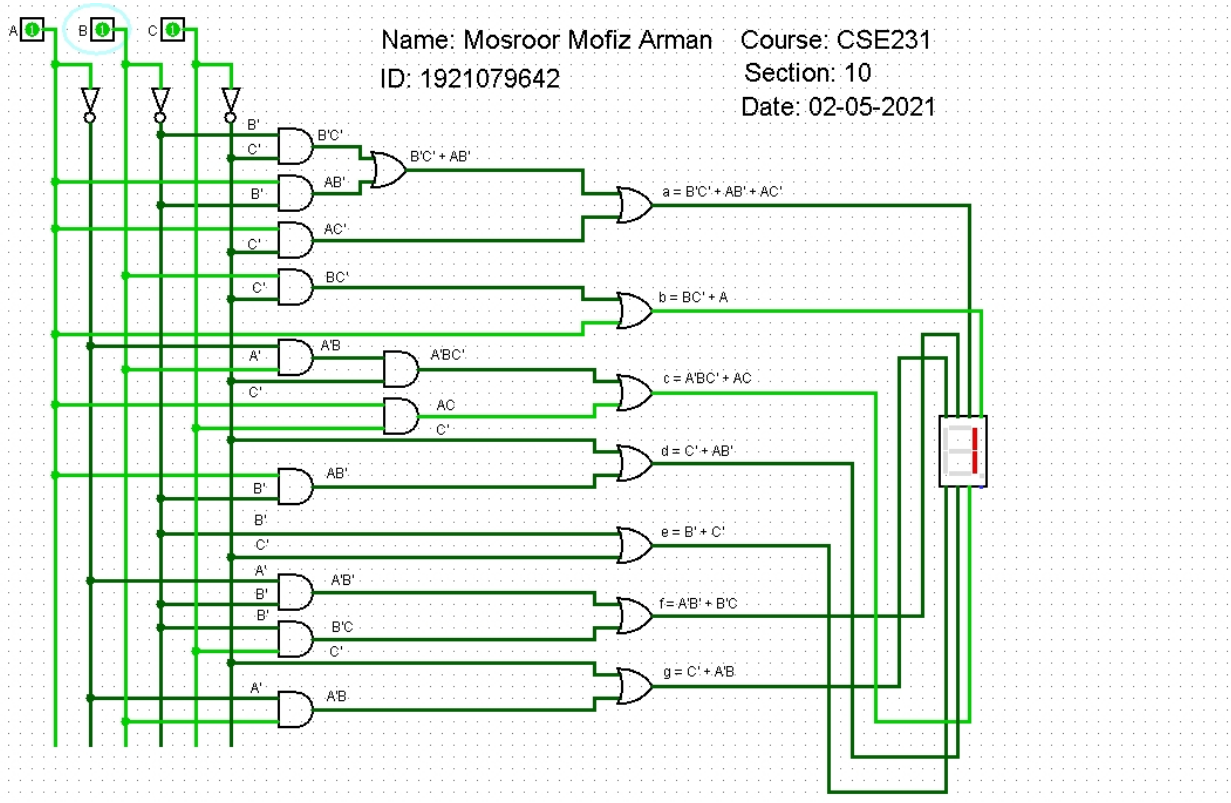


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display by Sum of Product

3 bit counter by Arman:

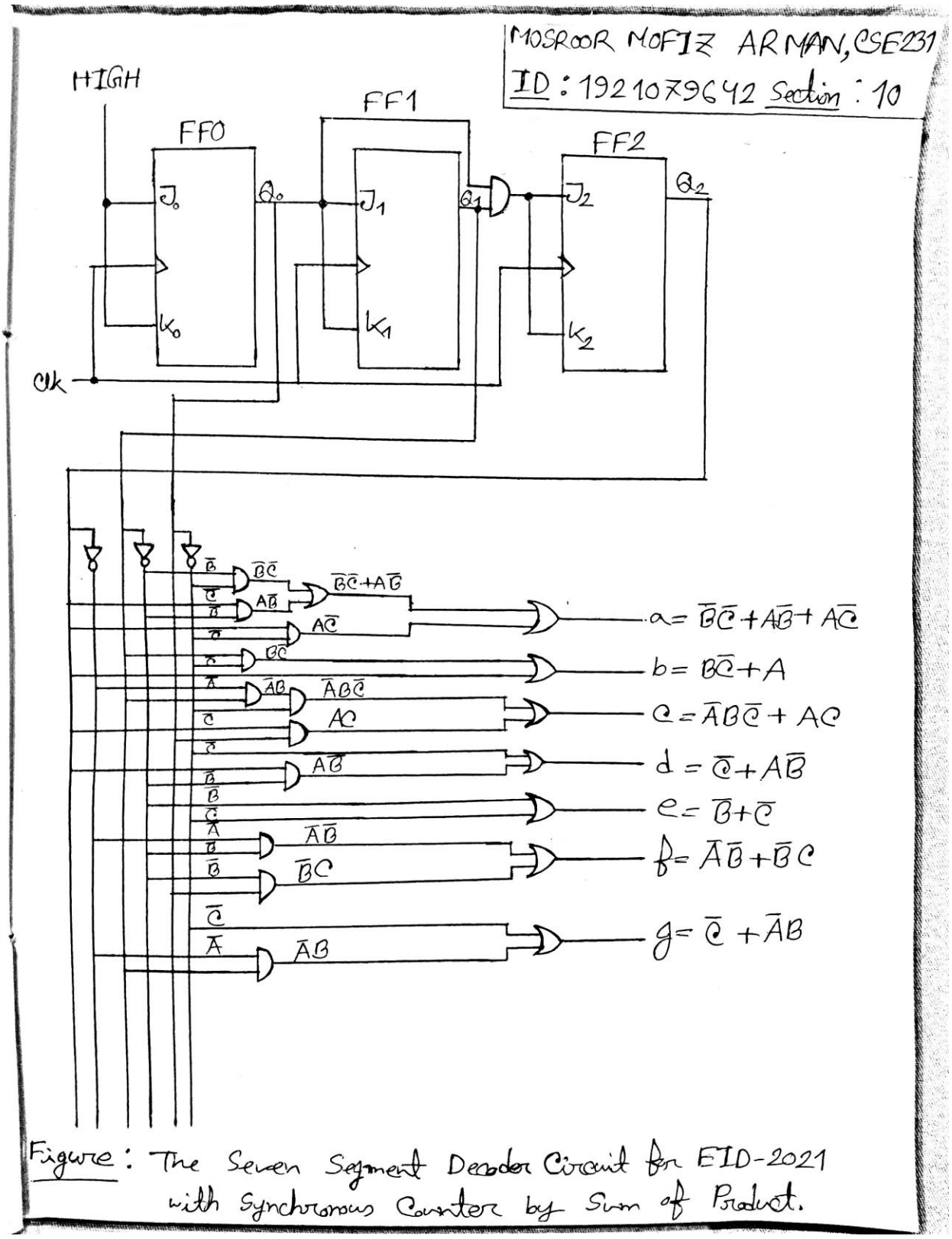


Figure: The Seven Segment Decoder Circuit for EID-2021 with Synchronous Counter by Sum of Product.

3 bit Synchronous Counter by Arman:

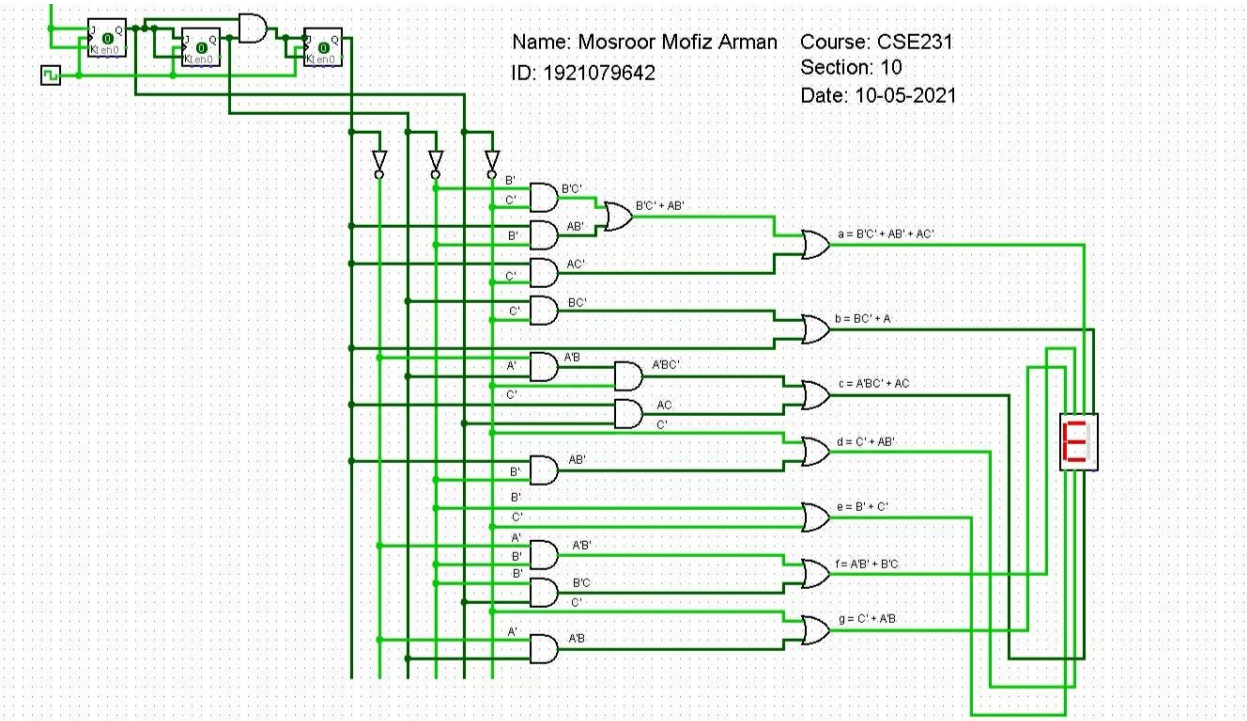


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display and Synchronous Counter by Sum of Product

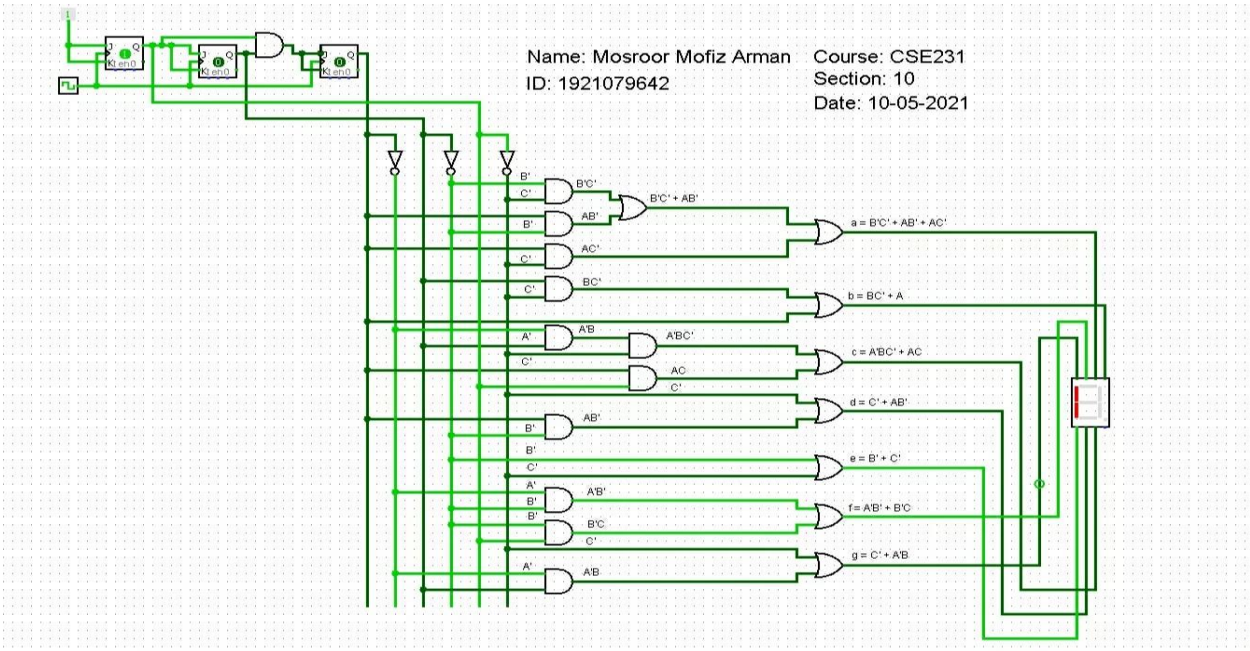


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display and Synchronous Counter by Sum of Product

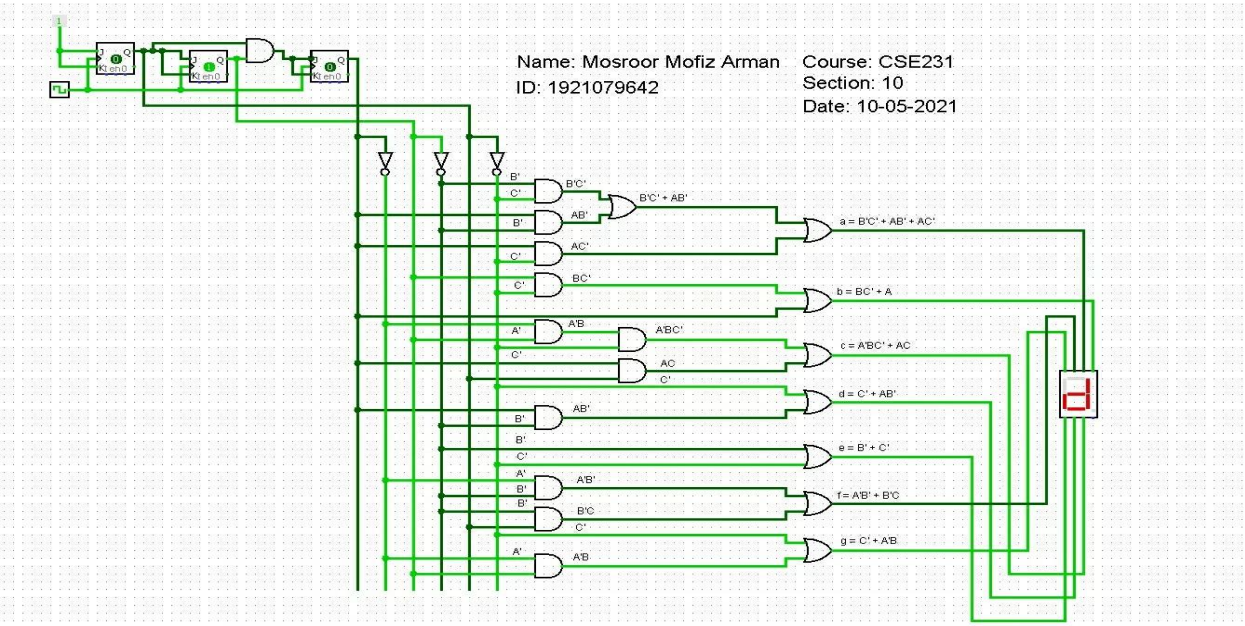


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display and Synchronous Counter by Sum of Product

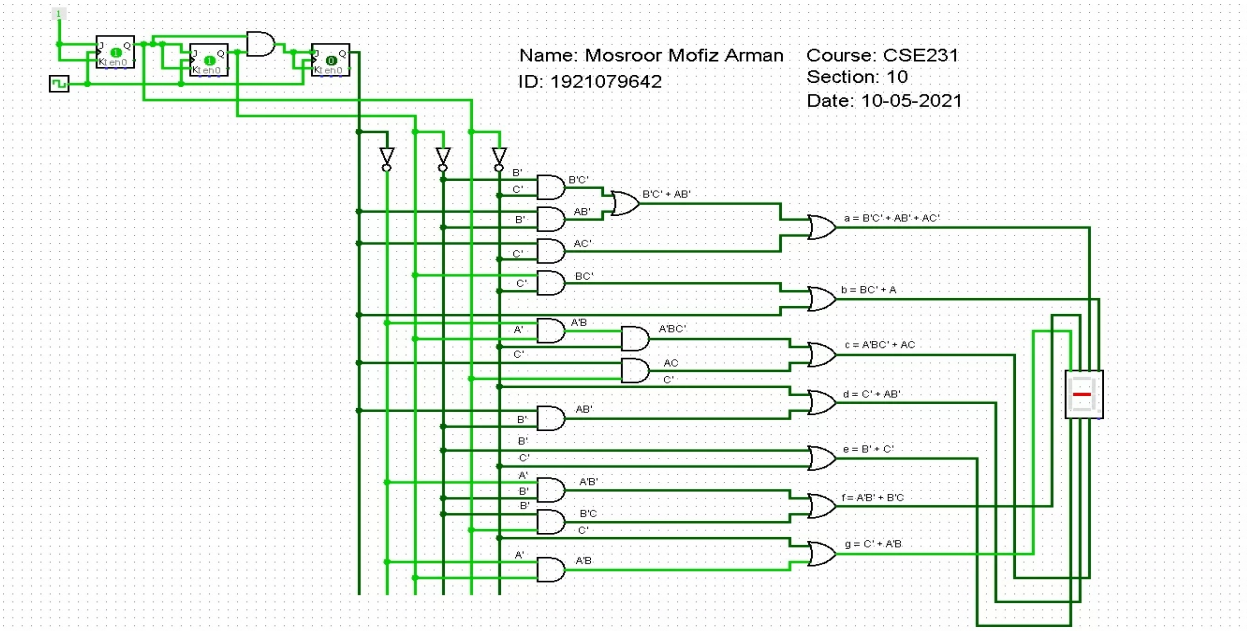


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display and Synchronous Counter by Sum of Product

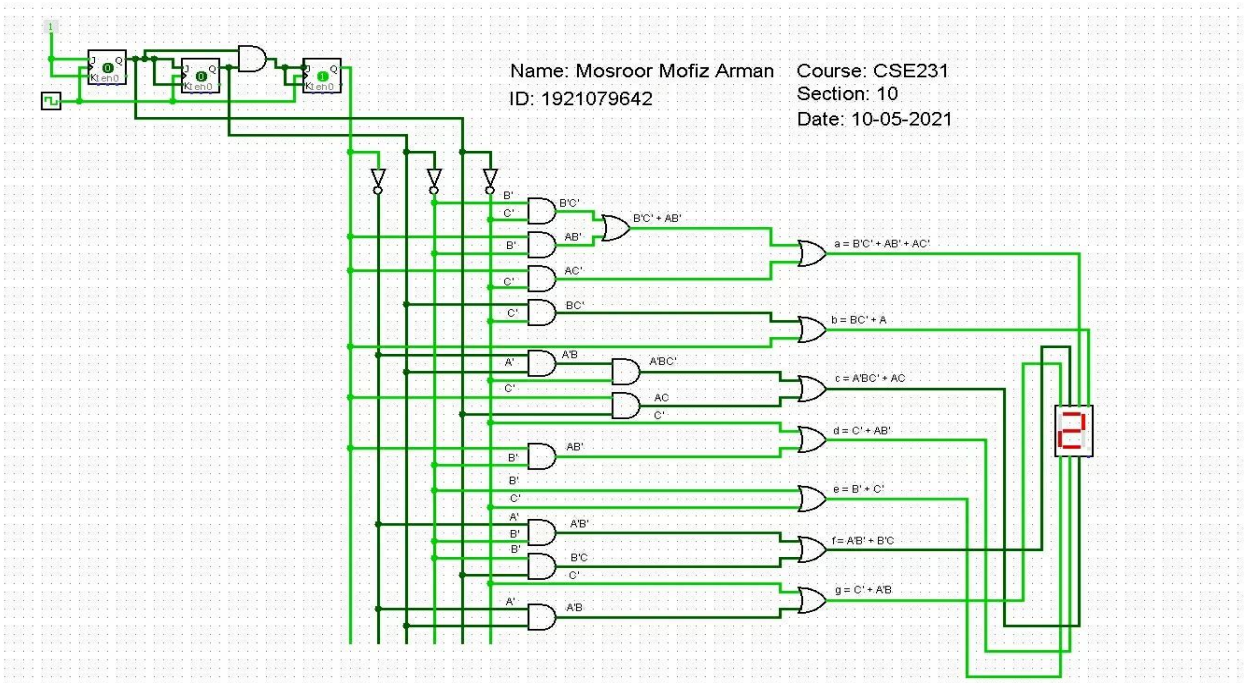


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display and Synchronous Counter by Sum of Product

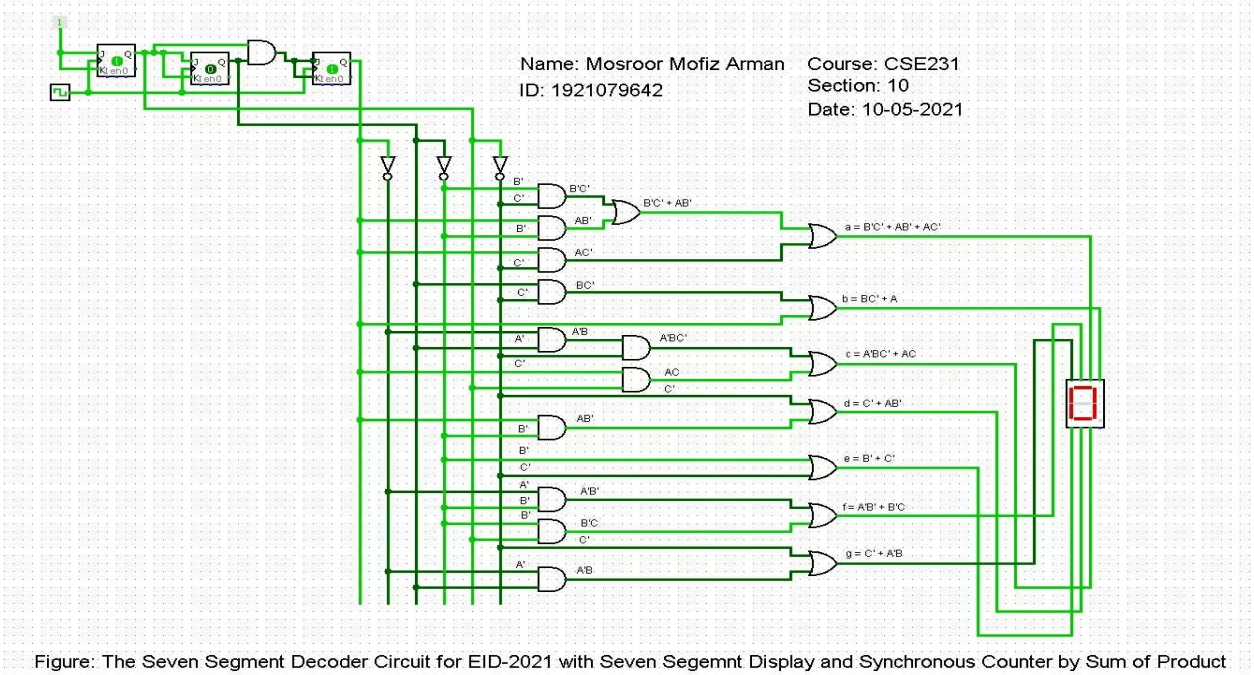


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display and Synchronous Counter by Sum of Product

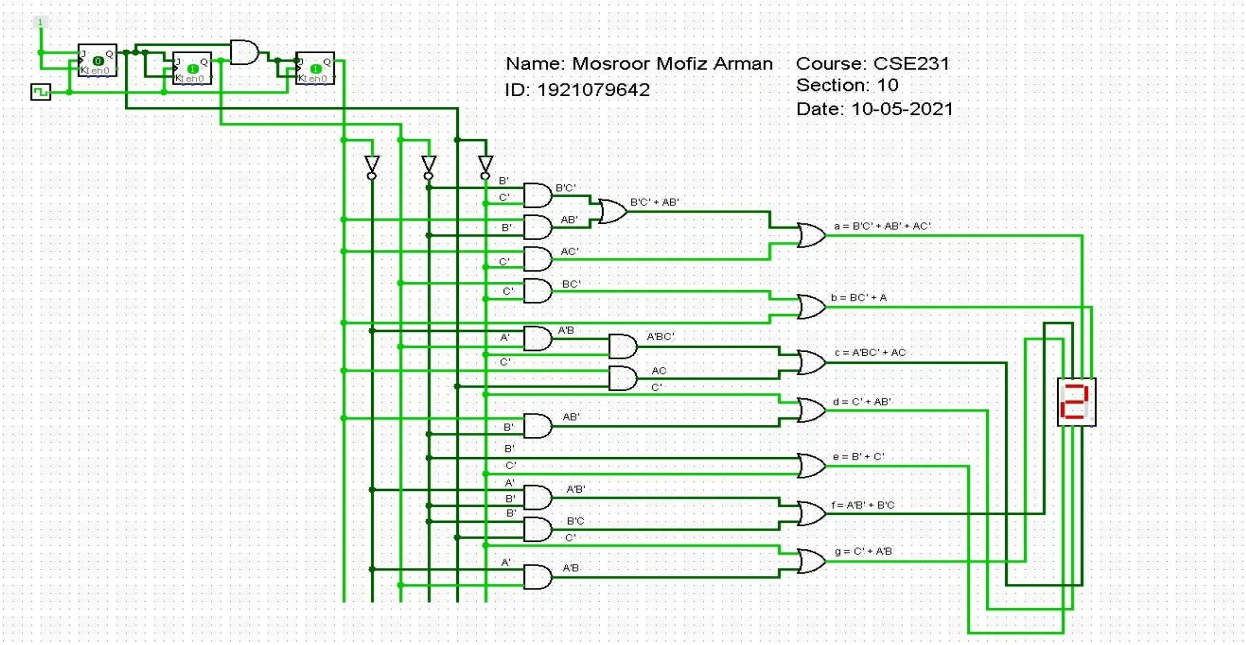


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display and Synchronous Counter by Sum of Product

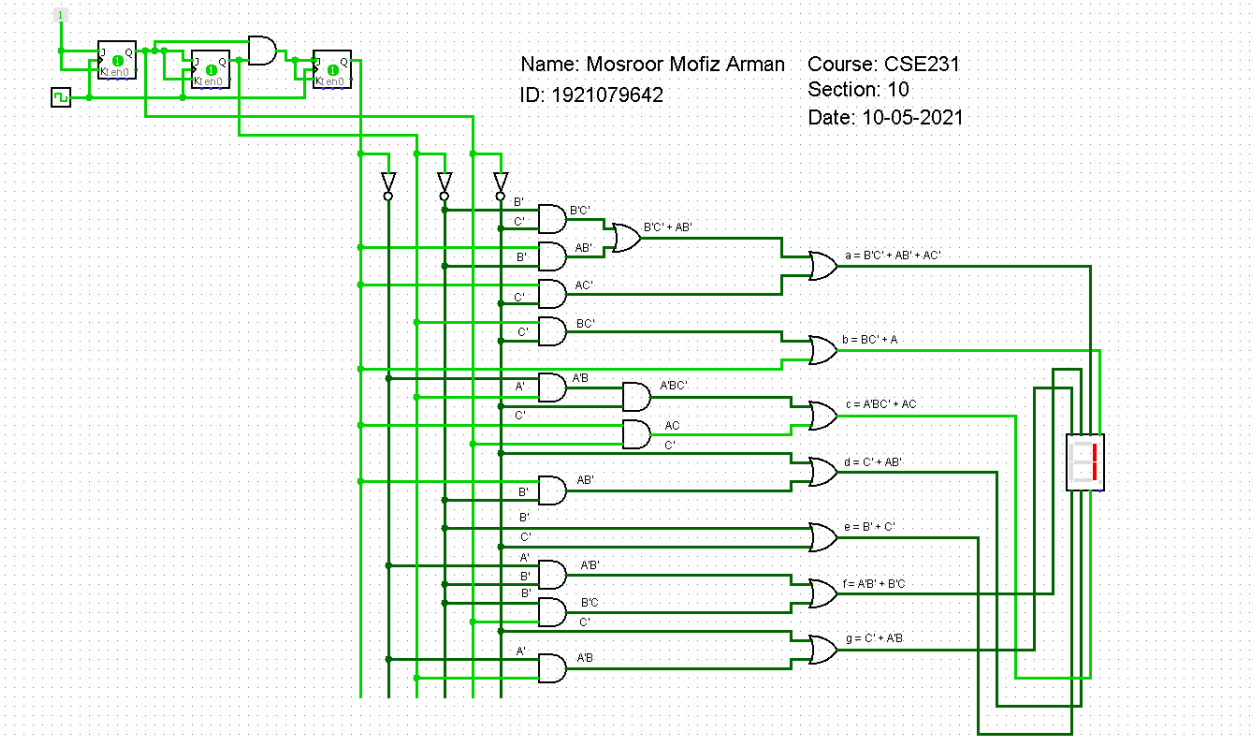
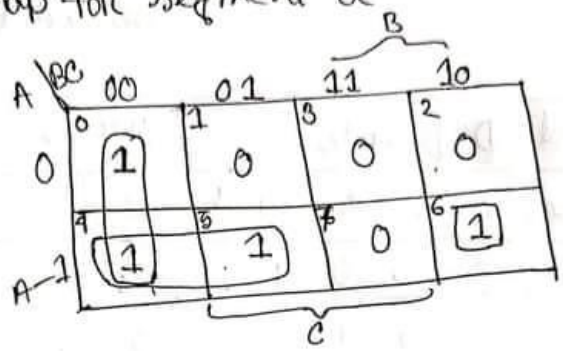


Figure: The Seven Segment Decoder Circuit for EID-2021 with Seven Segemnt Display and Synchronous Counter by Sum of Product

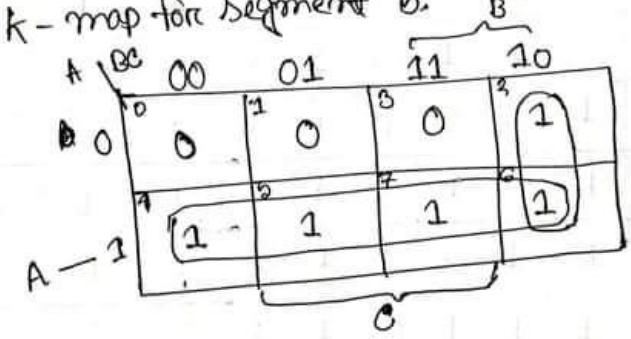
Using (SOP -NAND) by Ariful:

K-map

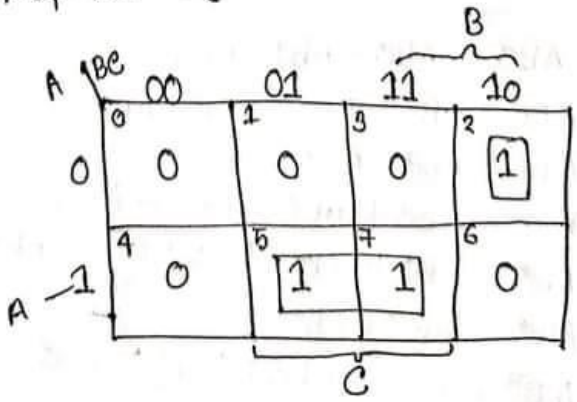
K map for segment a



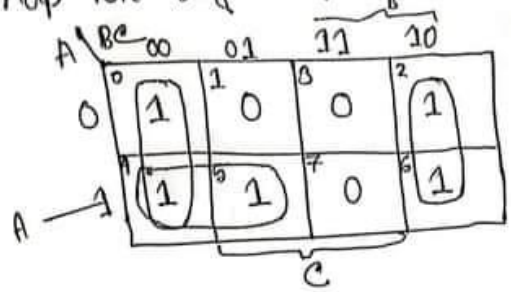
K-map for segment b.



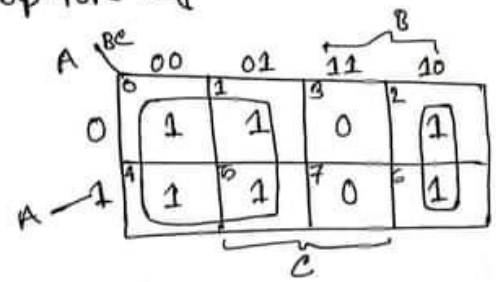
K-map for segment C



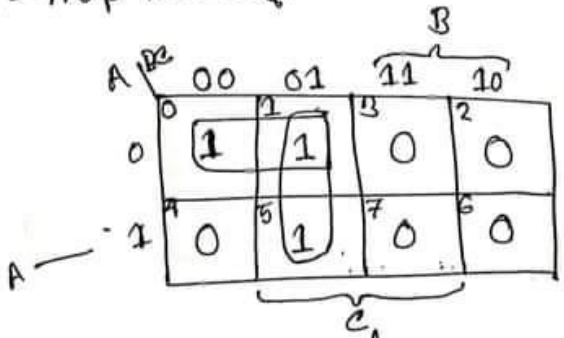
K-map for segment - d



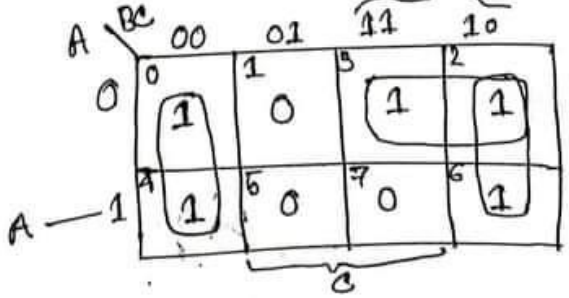
K-map for segment e



K-map for segment f



K-map for segment g



∴ Logic for segment $a = B\bar{C} + A\bar{B} + A\bar{C}$

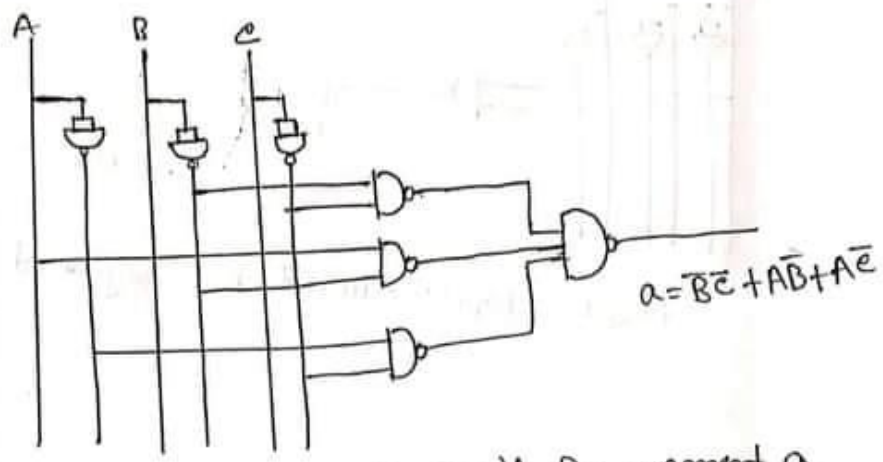


Figure: Logic circuit for segment a

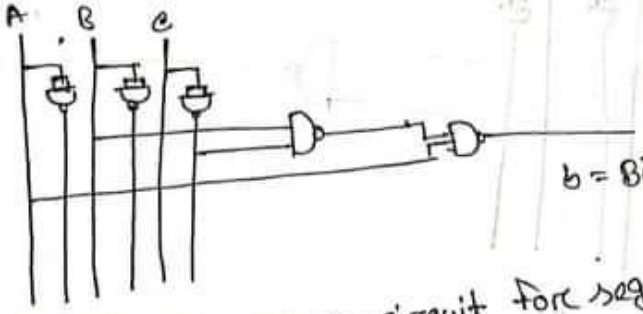


Figure: Logic circuit for segment b

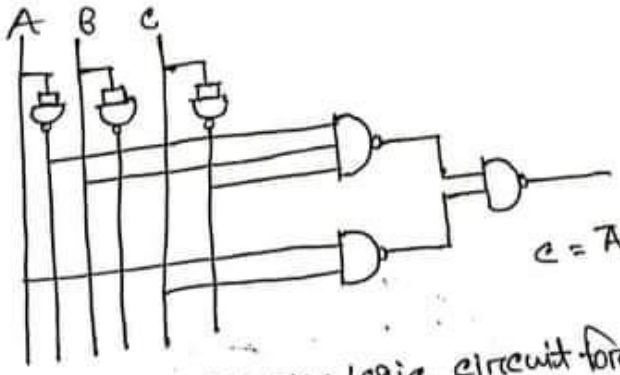


Figure: Logic circuit for segment c

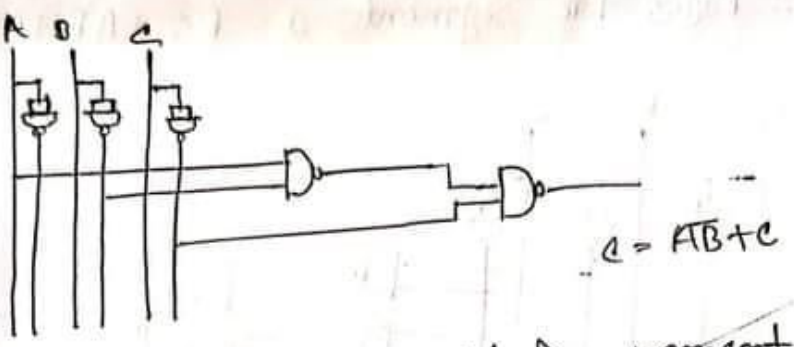


Figure: Logic circuit for segment d

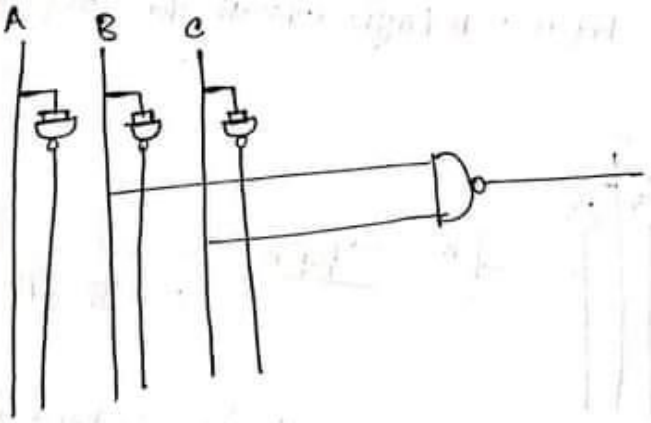


Figure : Logic circuit for segment e

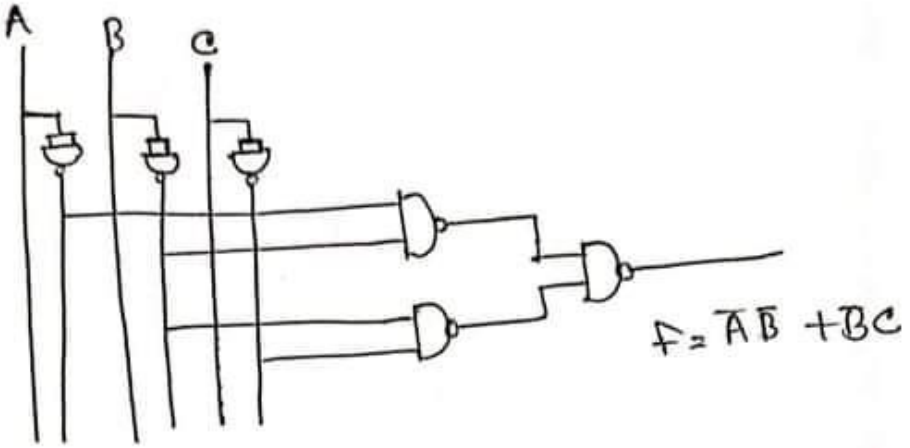


Figure: Logic circuit for segment f

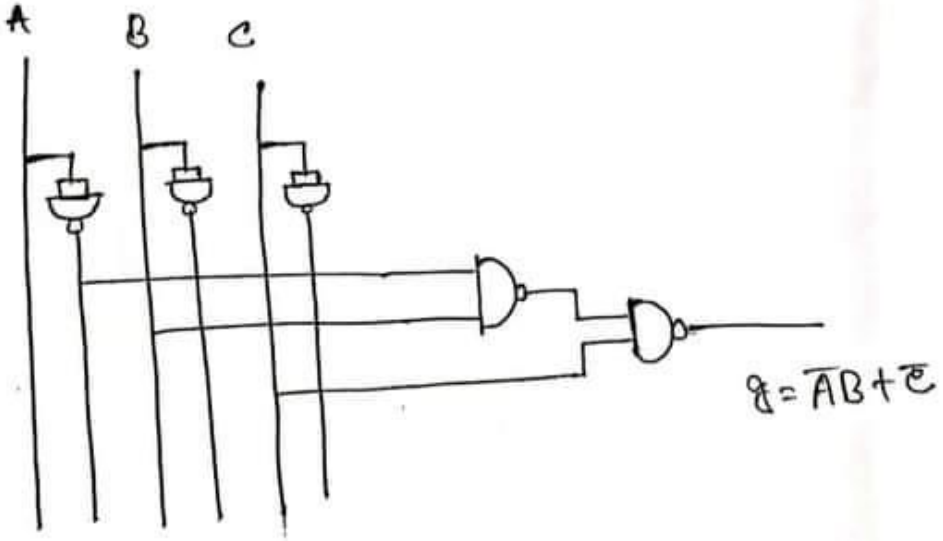


Figure: Logic circuit for segment g.

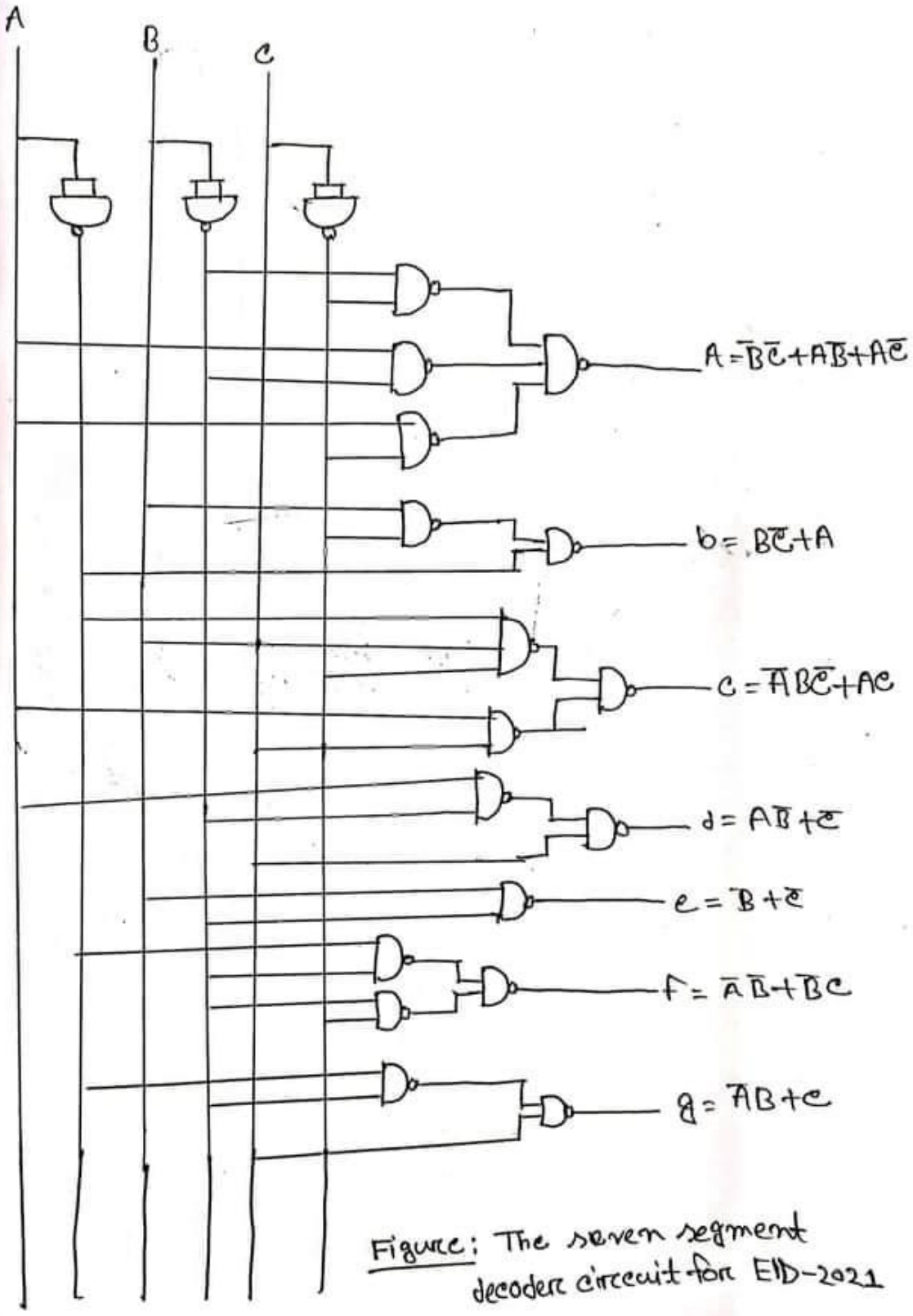
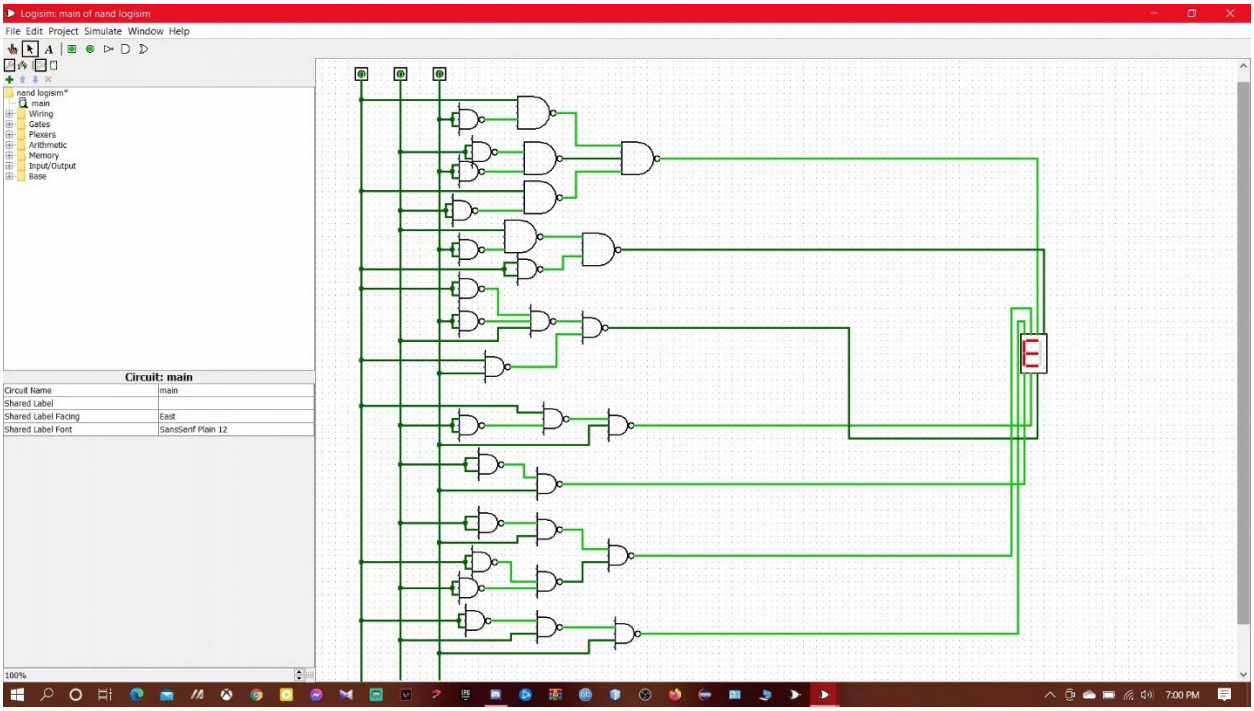
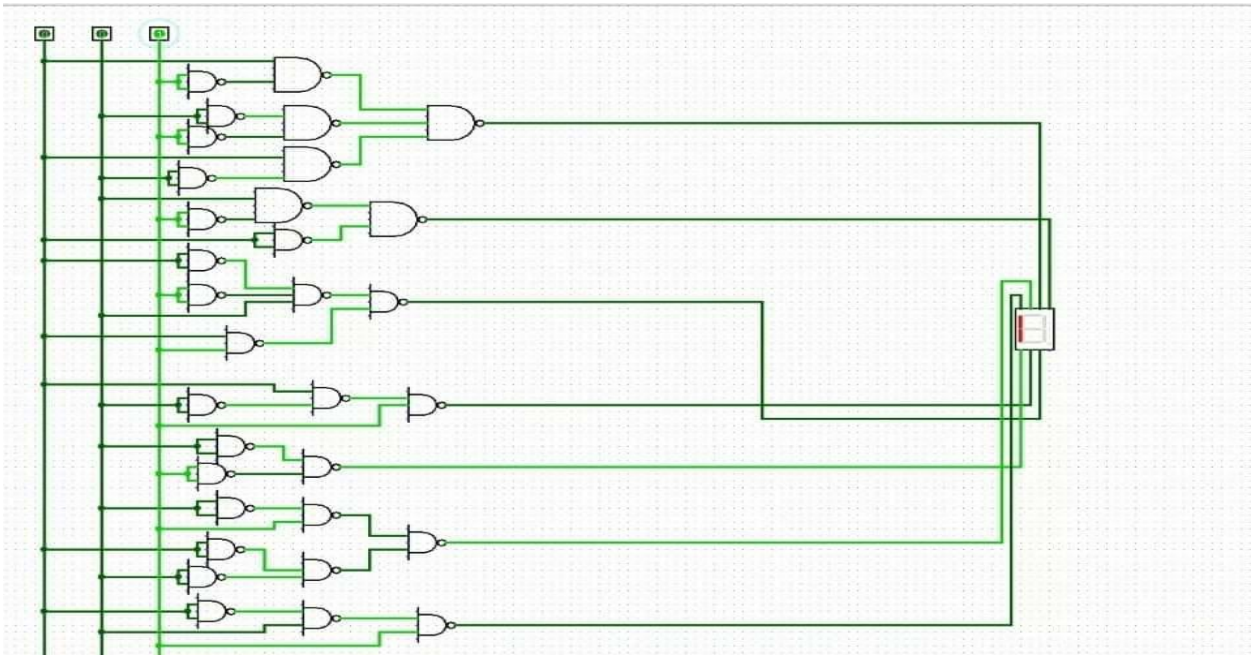
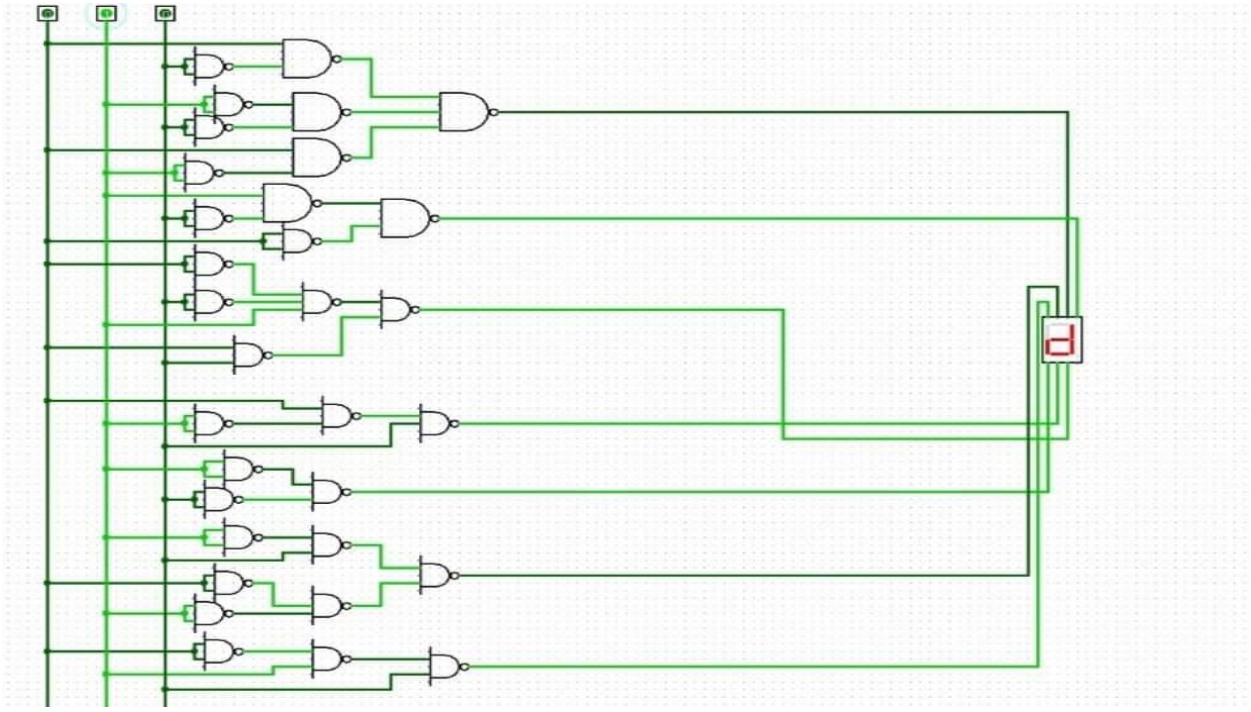


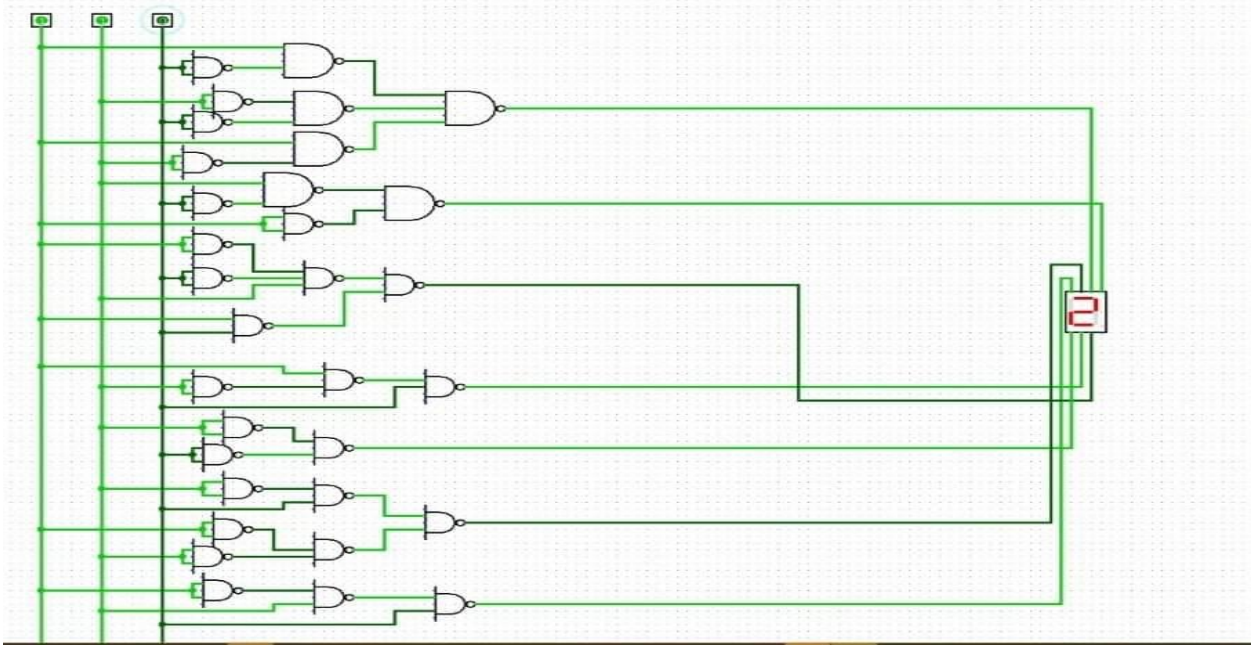
Figure: The seven segment decoder circuit for EID-2021

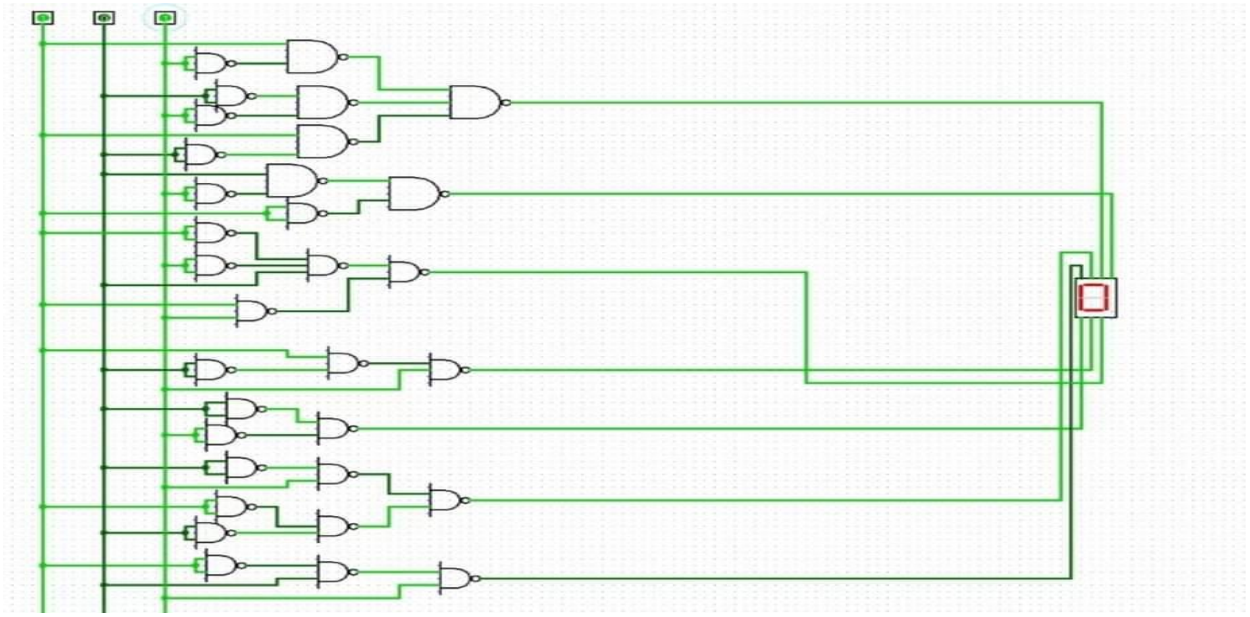
Seven segment display by Suvo (NAND):







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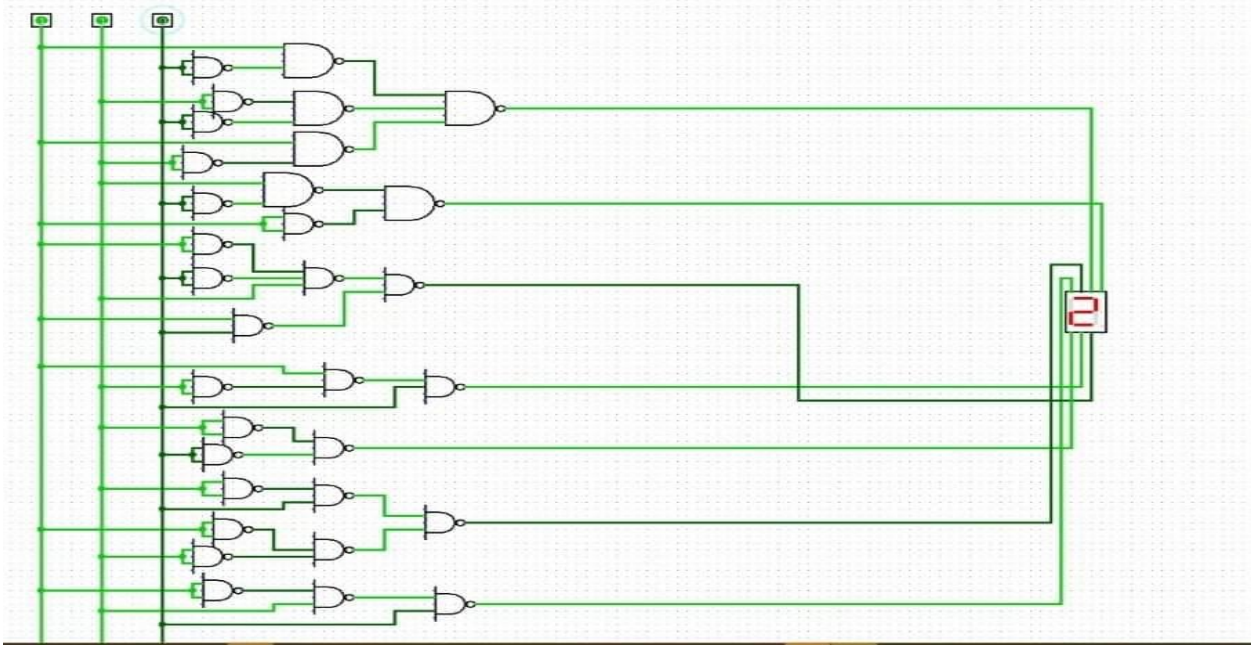
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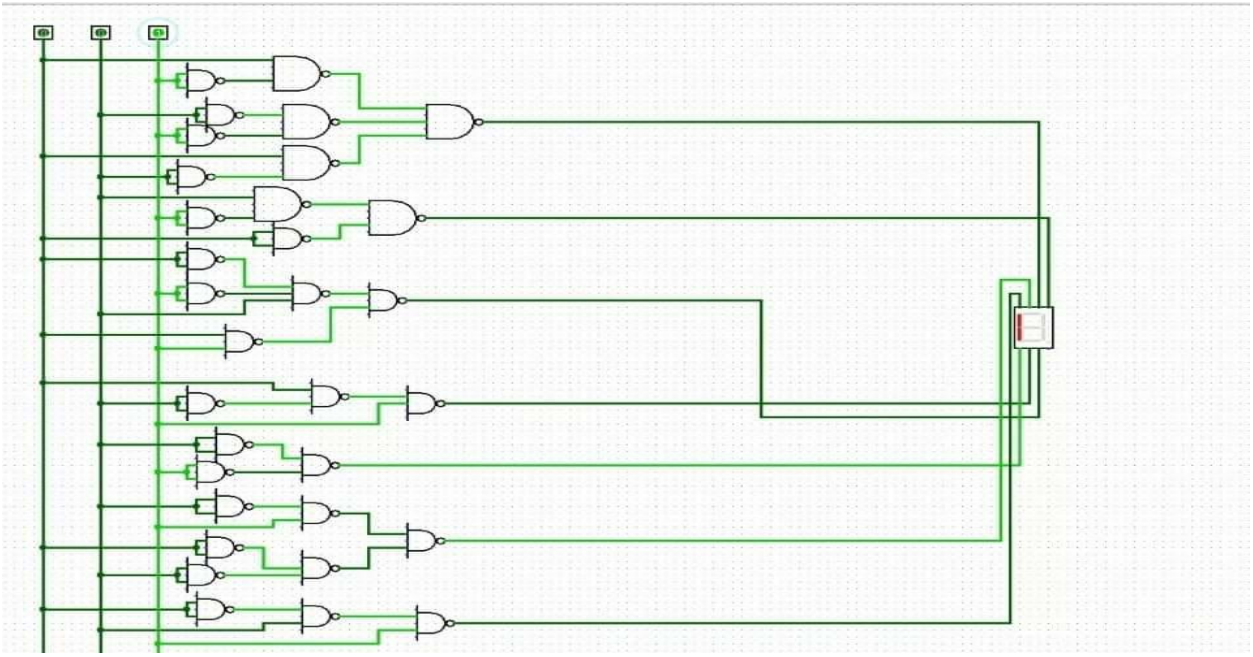
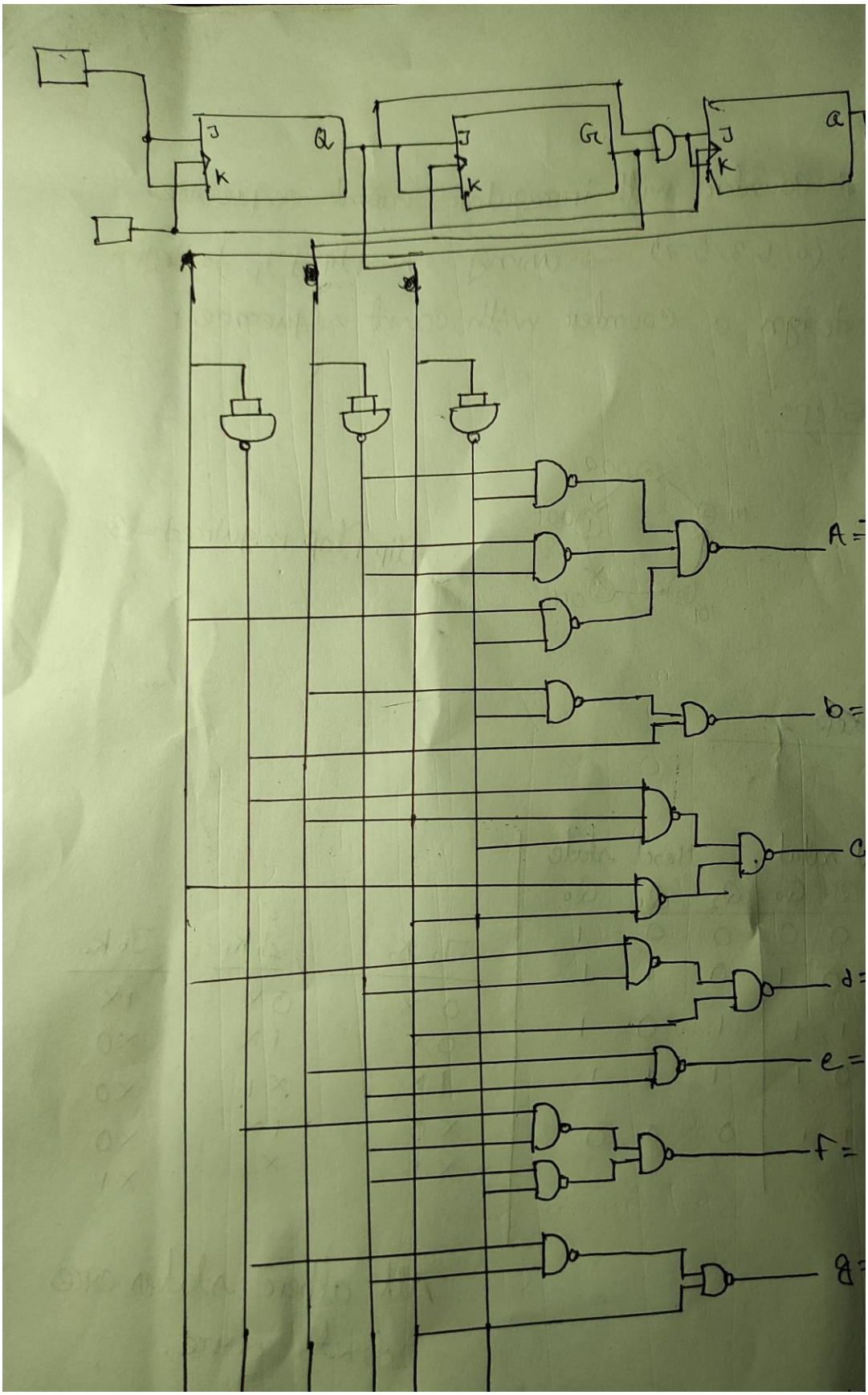
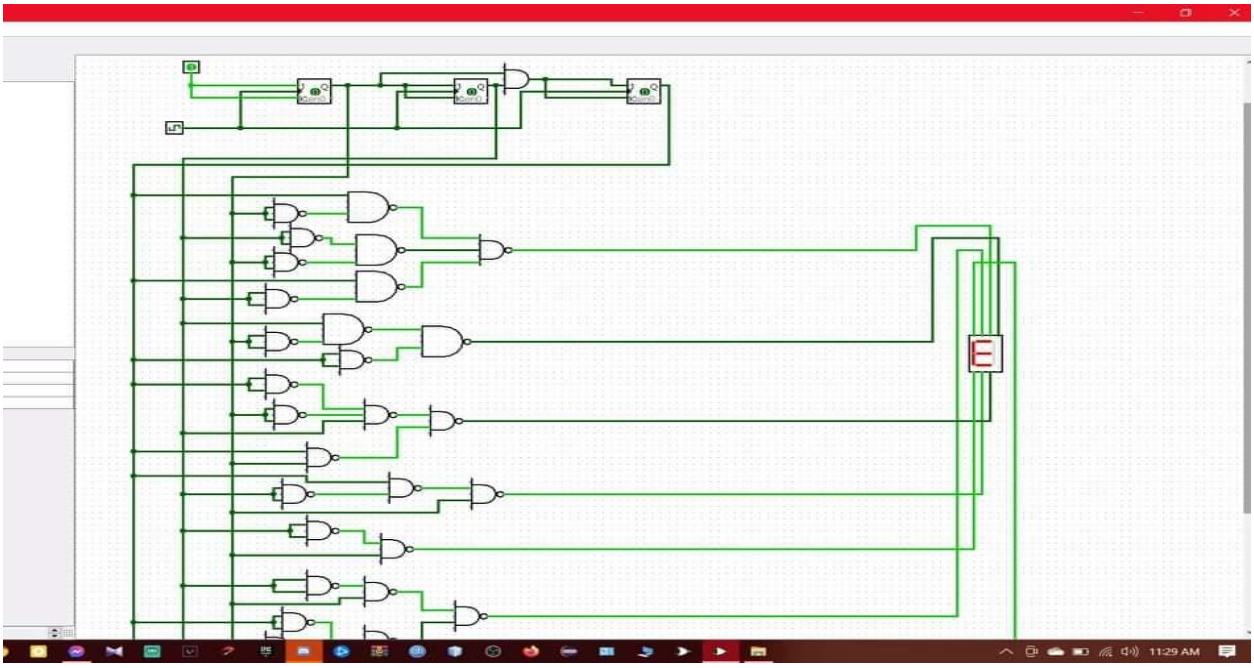
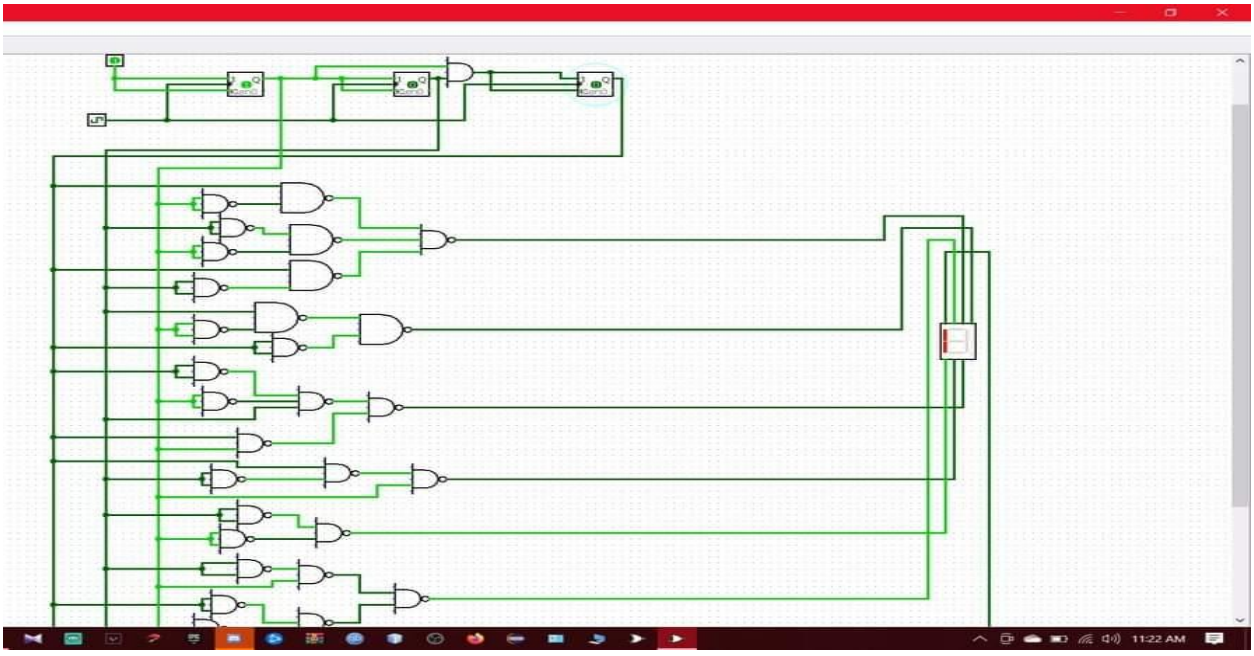
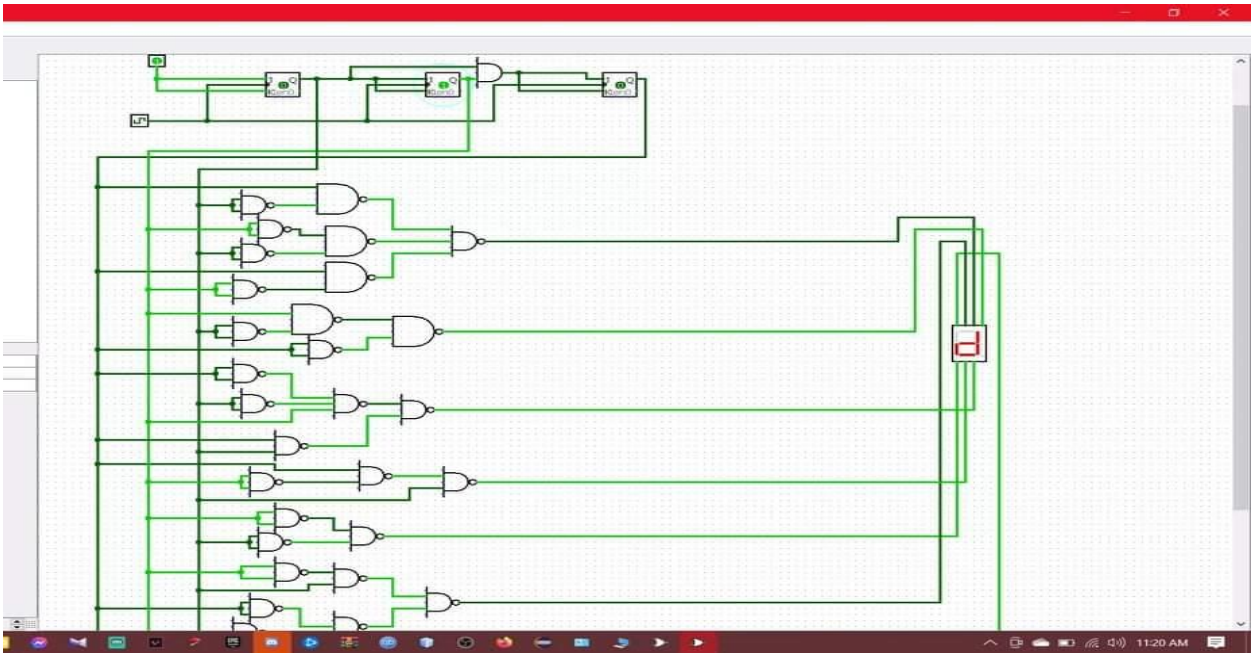



J
Q
K
J
Q
K
J
Q
K
A=
b=
c
d=
e=
f=
g=

3 bit counter by suvo:







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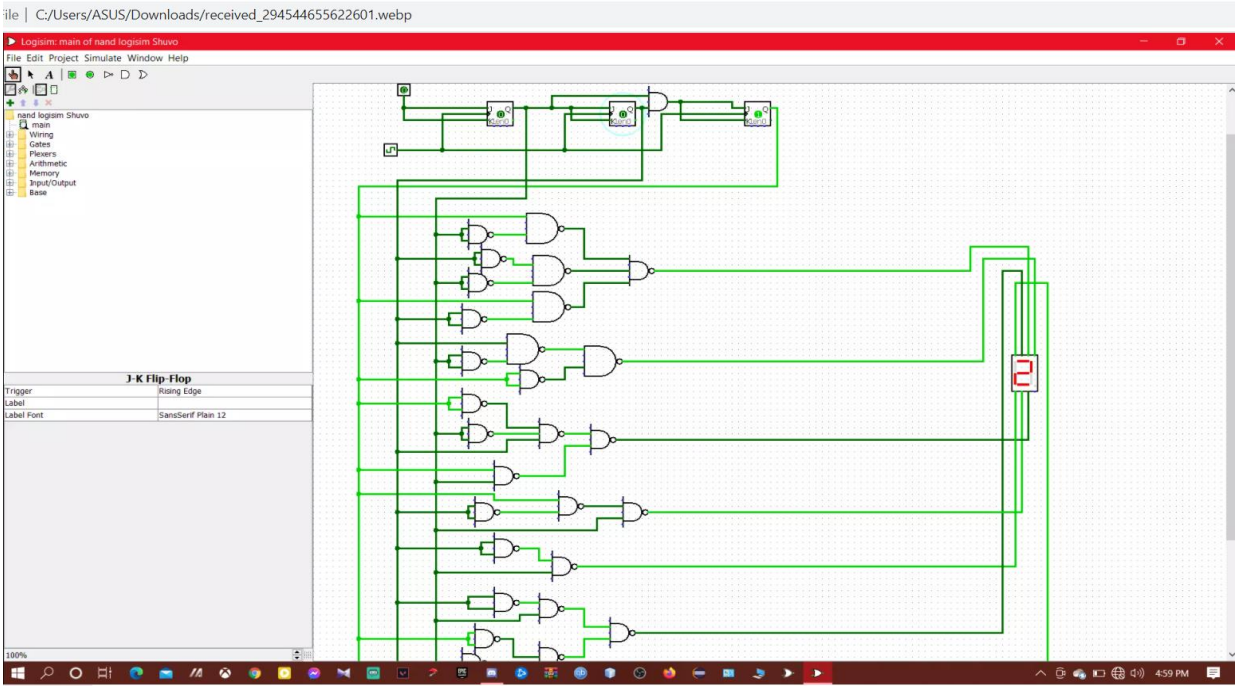

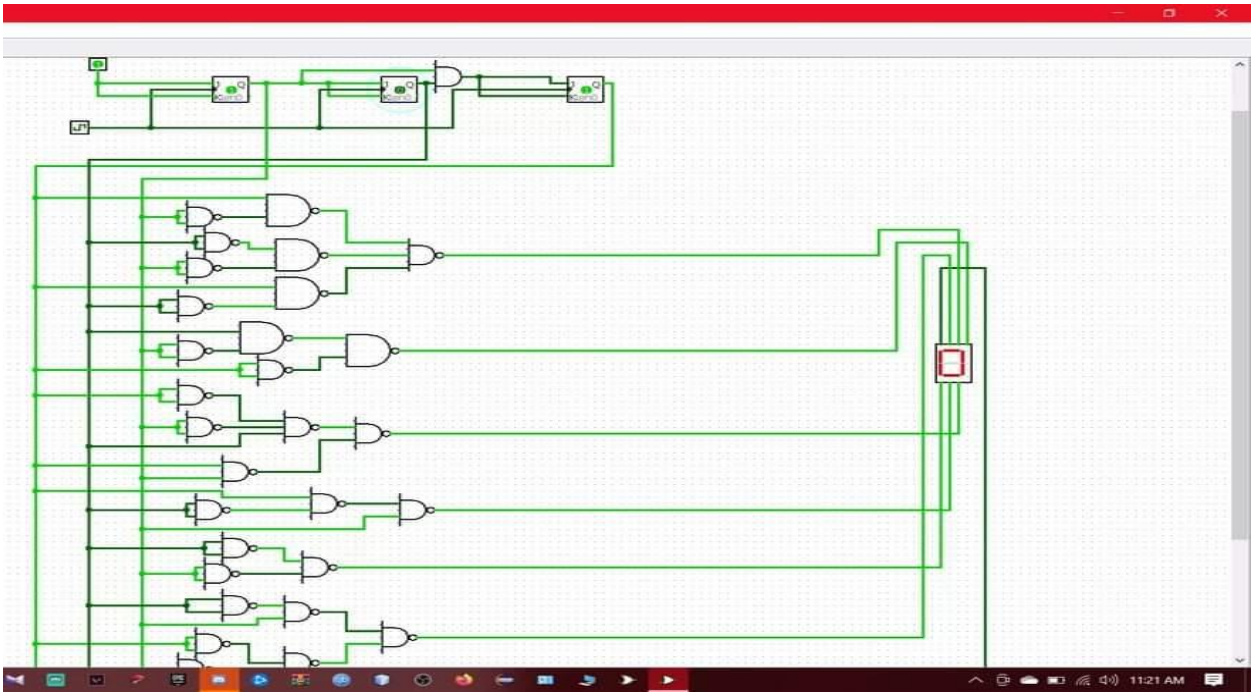
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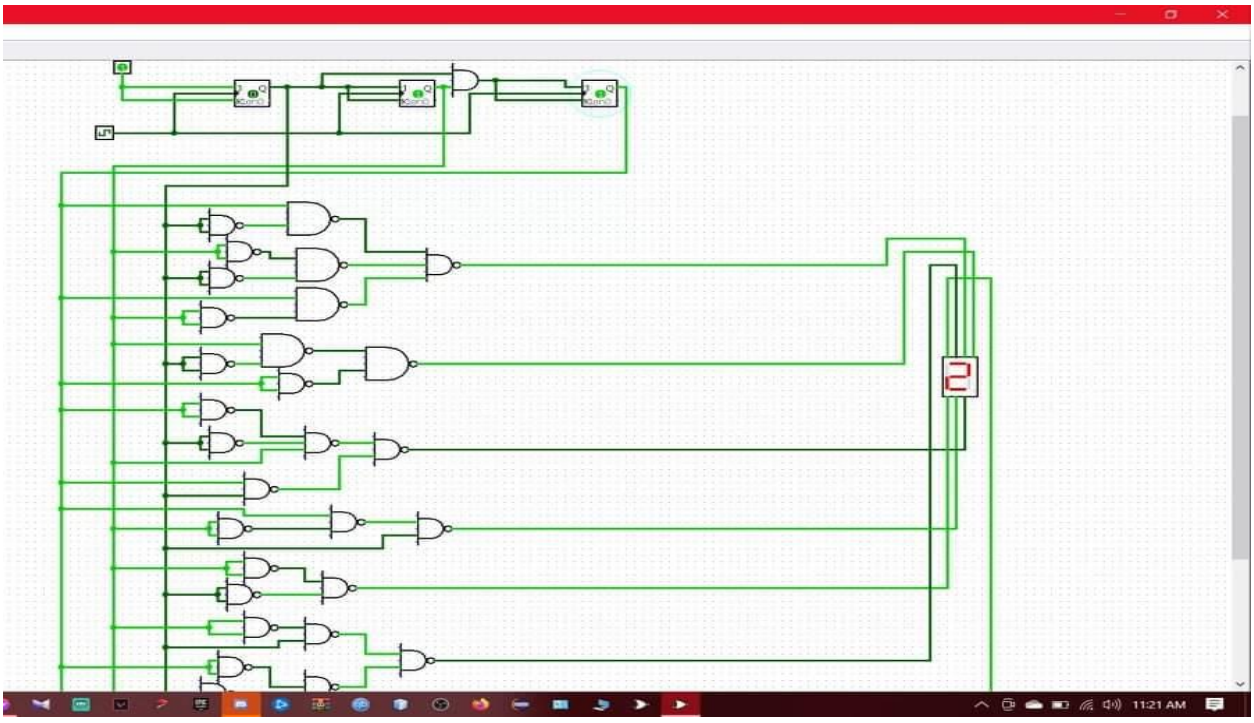
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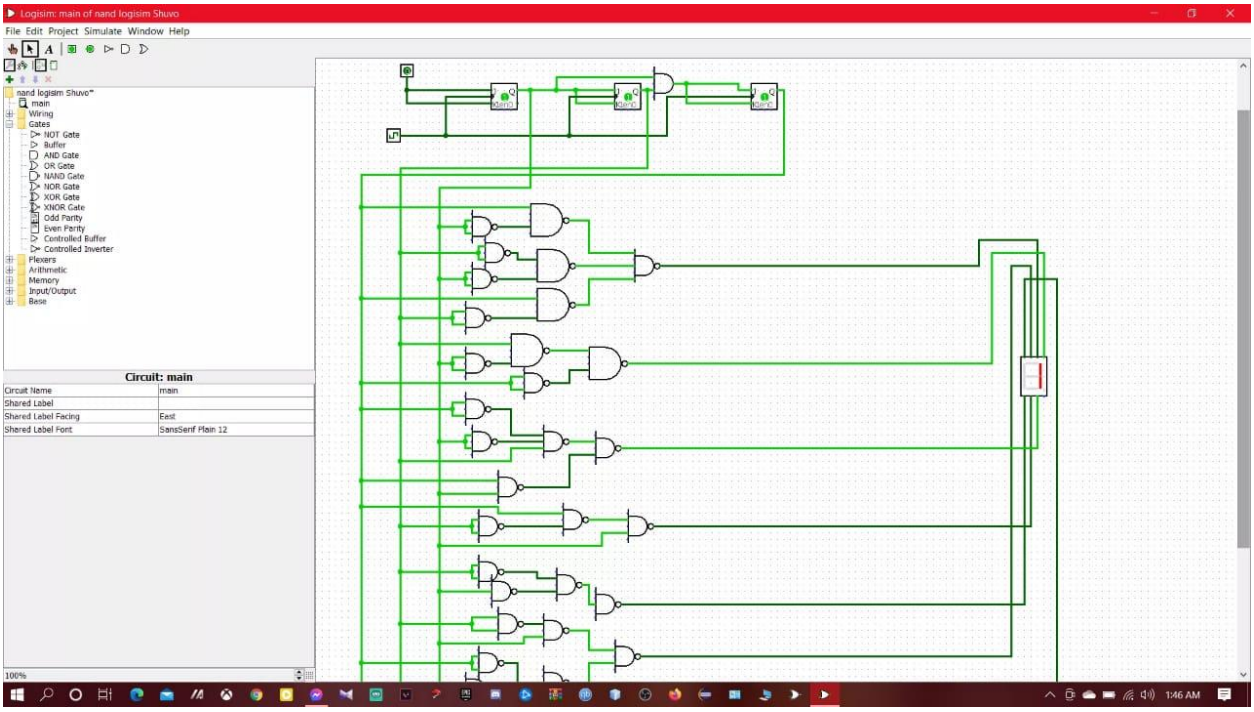

Logisim: main of nand logisim Shuvo
File Edit Project Simulate Window Help
nand logisim Shuvo*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: main
Circuit Name
main
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12
100%
1:46 AM

Using (SOP – NOR) by Raiyan:

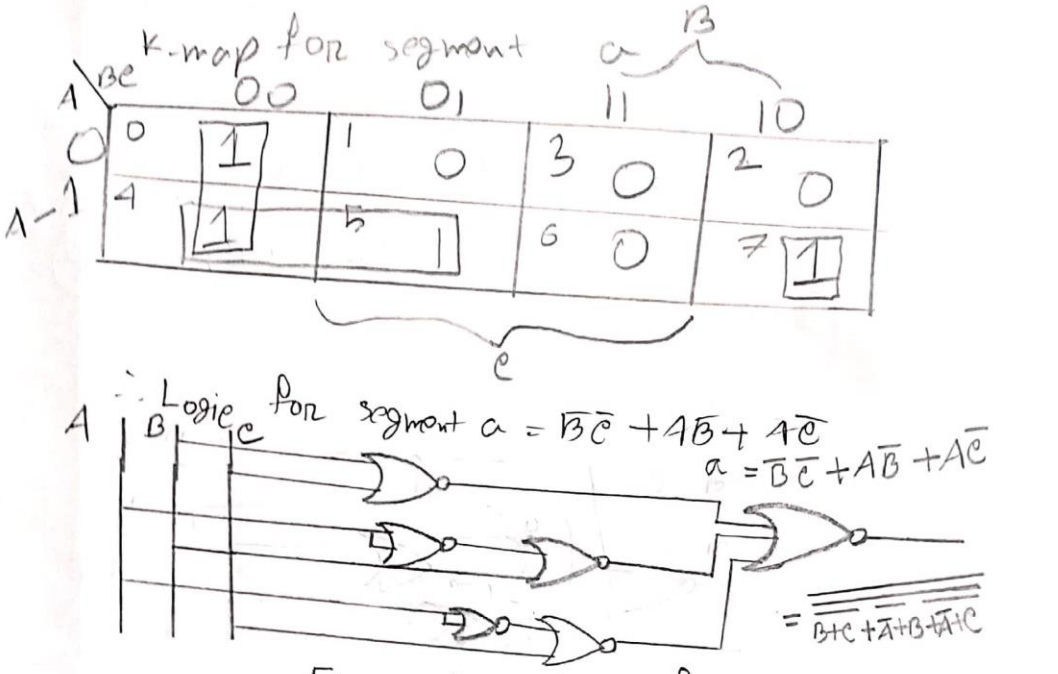


Figure: Logic circuit for segment a

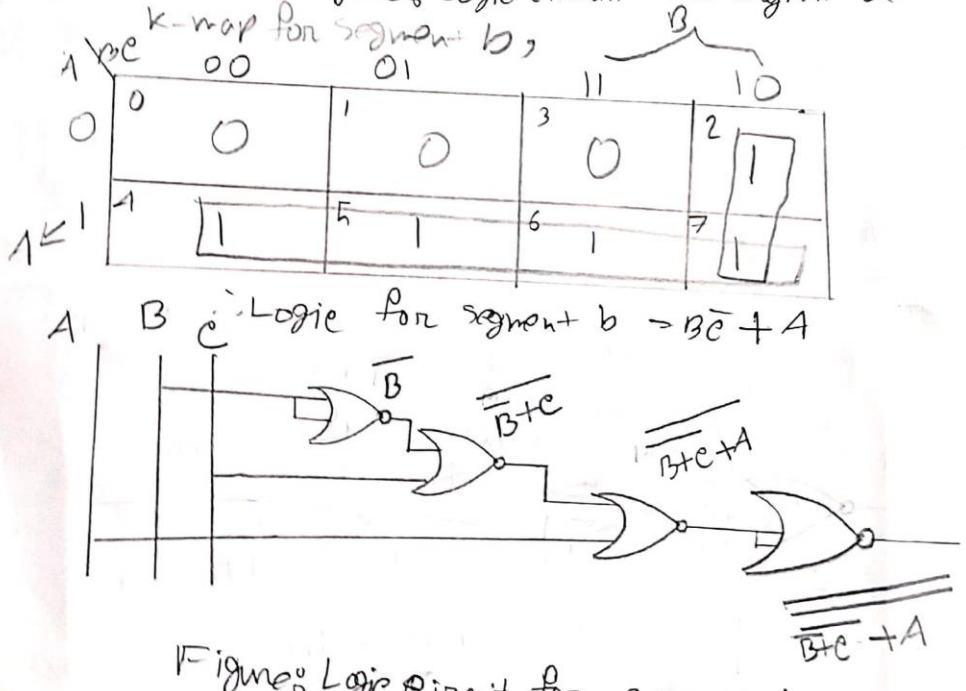
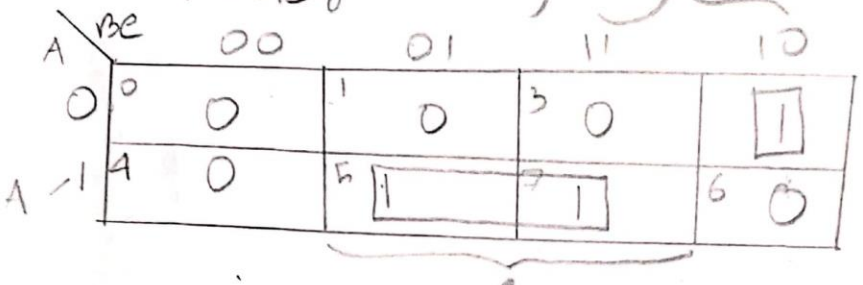


Figure: Logic circuit for segment b

K-map segment for c,



∴ Logic for segment $c = \bar{A}B\bar{C} + AC$

$c = \overline{\bar{A}B\bar{C} + AC}$

$= \overline{\bar{A}B\bar{C}} \cdot \overline{AC}$

$= A + \bar{B} + C + \bar{A} + \bar{C}$

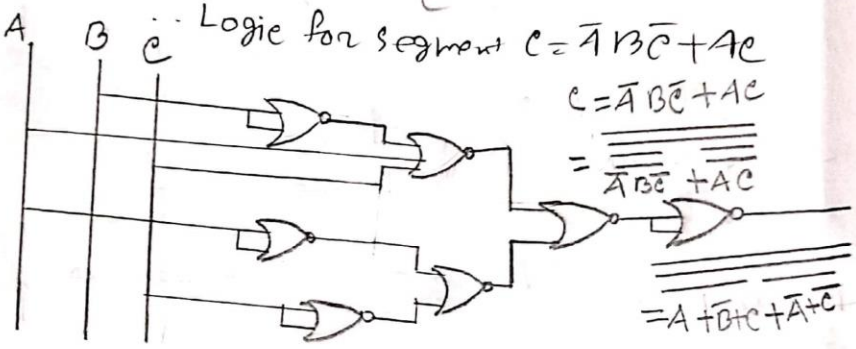
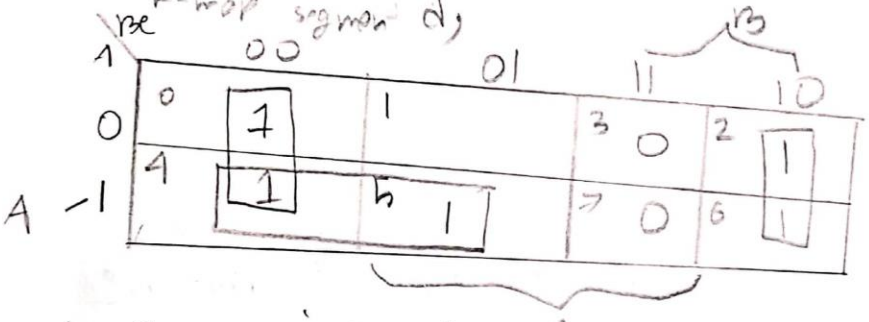


Figure: Logic circuit for segment c

K-map segment d;



∴ Logic for segment $d = \bar{C} + AB$

$d = \overline{\bar{C} + A\bar{B}}$

$= \bar{C} \cdot \overline{A + B}$

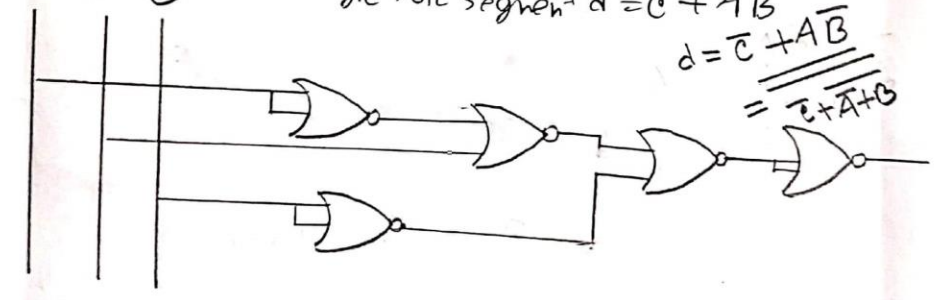
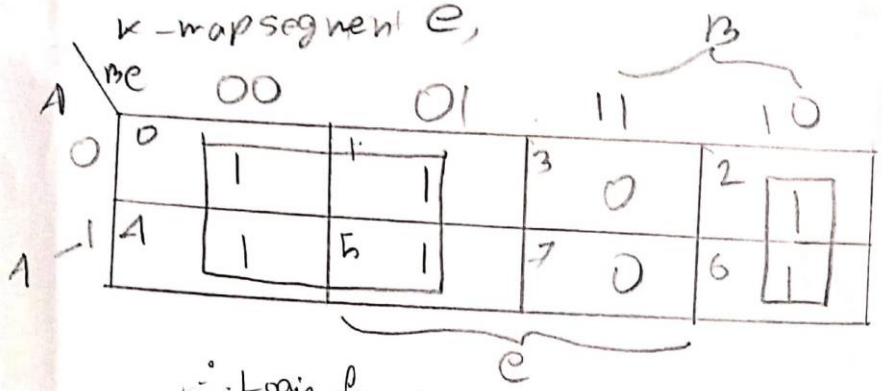


Figure: Logic circuit for segment d

K-map segment e,



∴ Logic for segment $e = \bar{B} + \bar{C}$

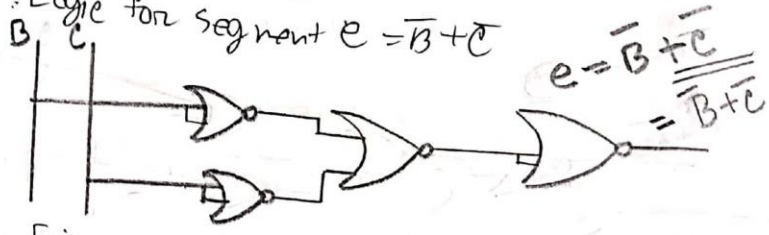
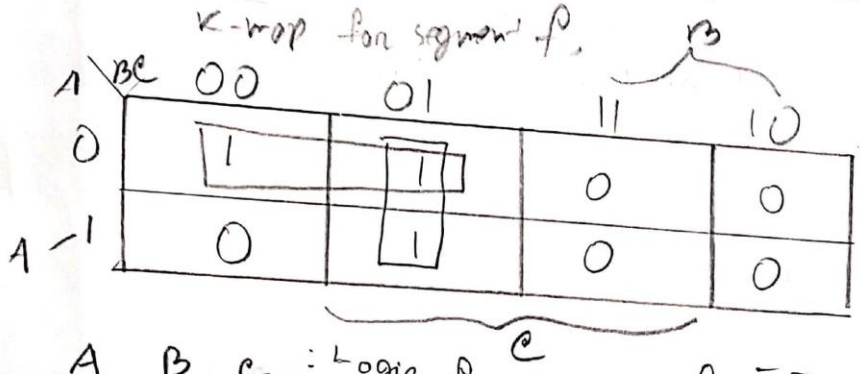


Figure: Logic circuit for segment $e = \bar{B} + \bar{C}$

K-map for segment f,



A B C : Logic for segment $f = \bar{A}\bar{B} + \bar{B}C$

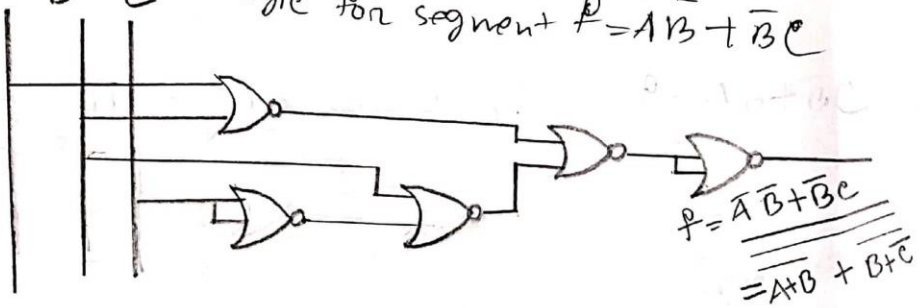


Figure: Logic circuit for segment f

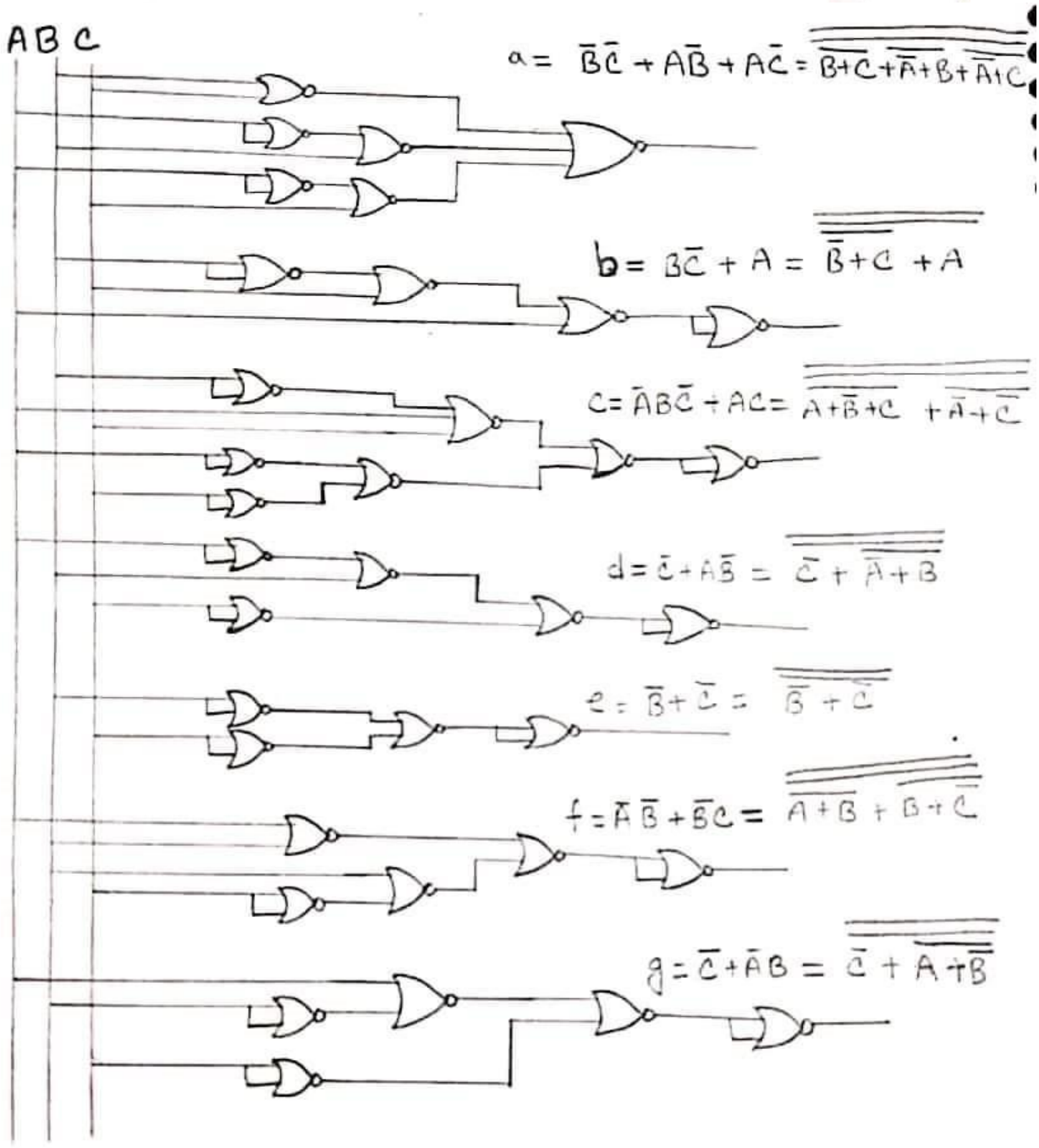
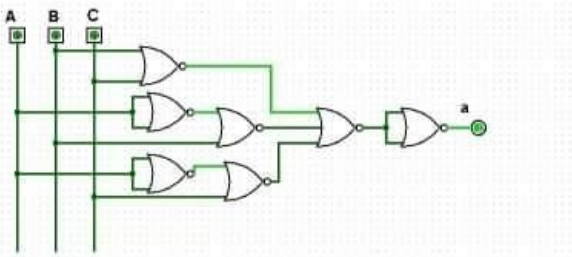
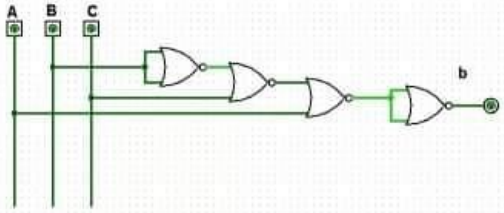
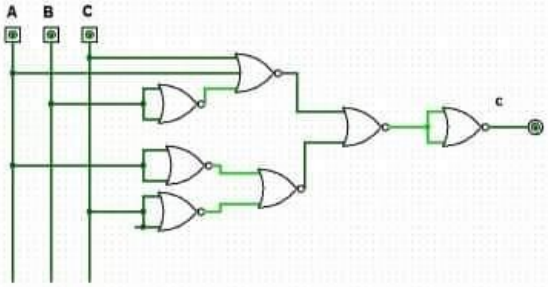
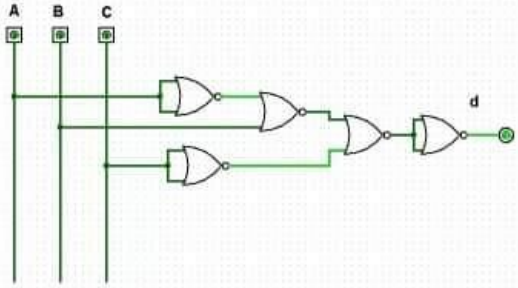


Figure : The seven segment decoder circuit for EID-2021

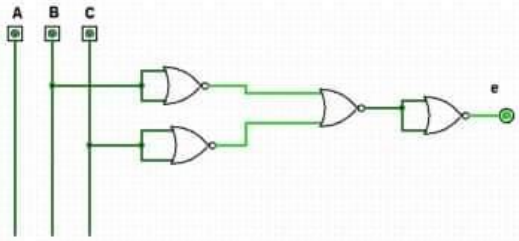


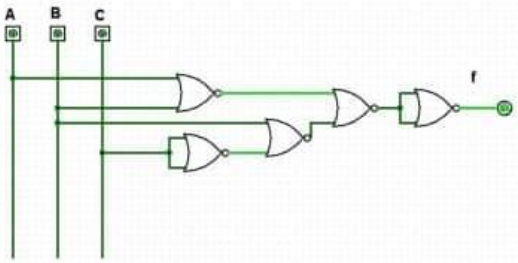


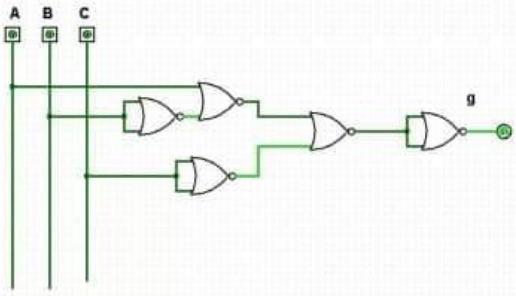




Name:Raiyan rafsan
ID:1921244042

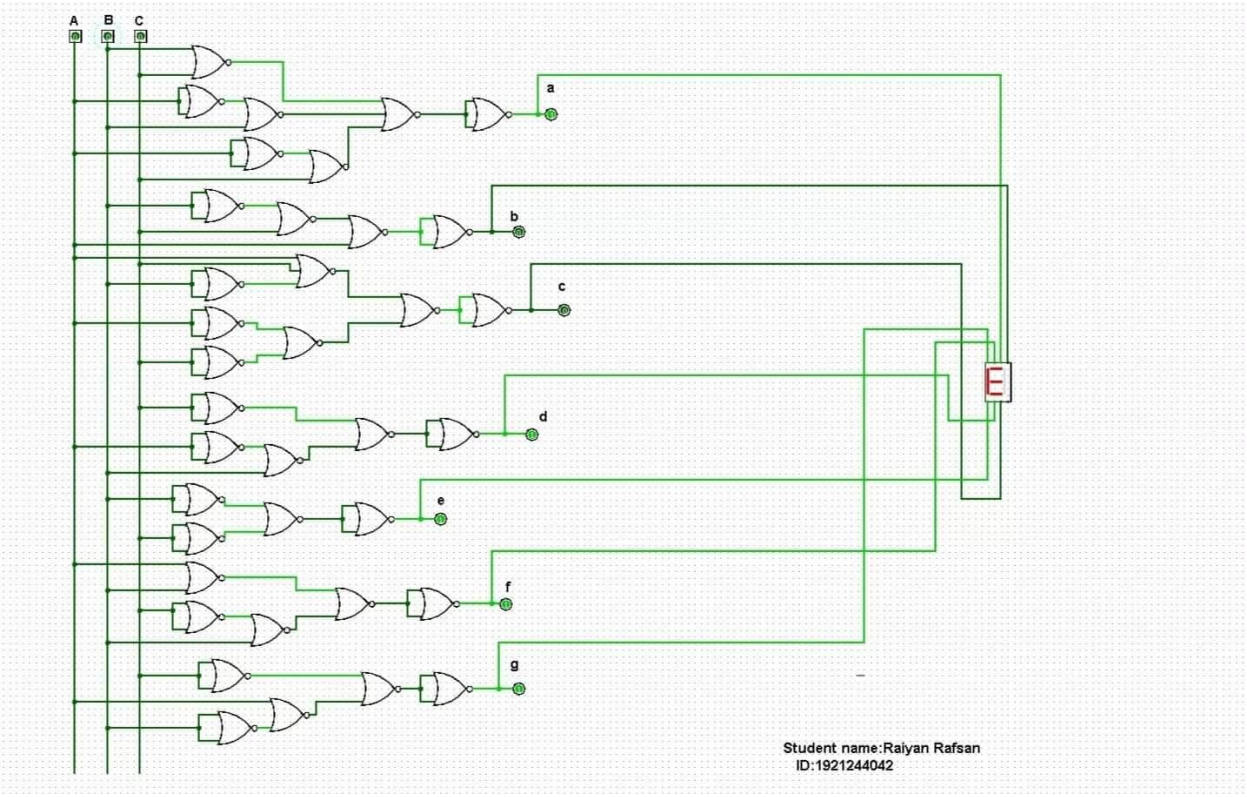


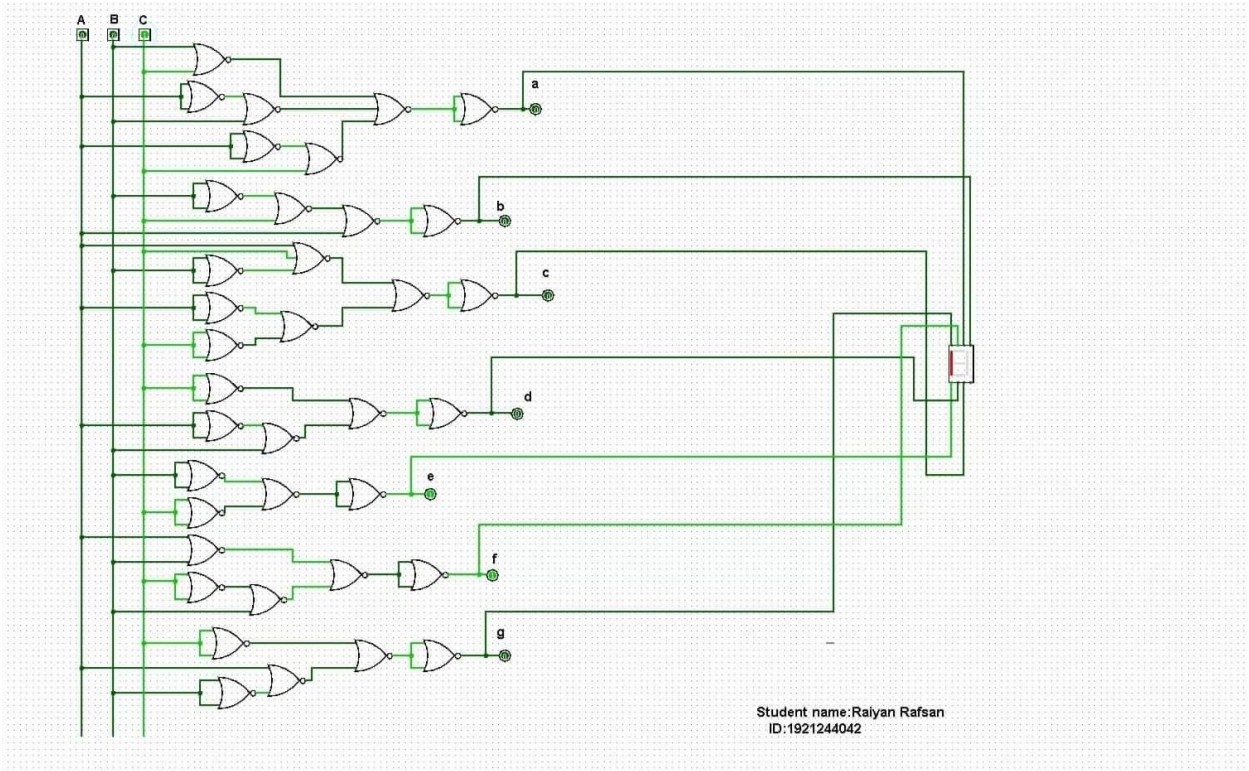


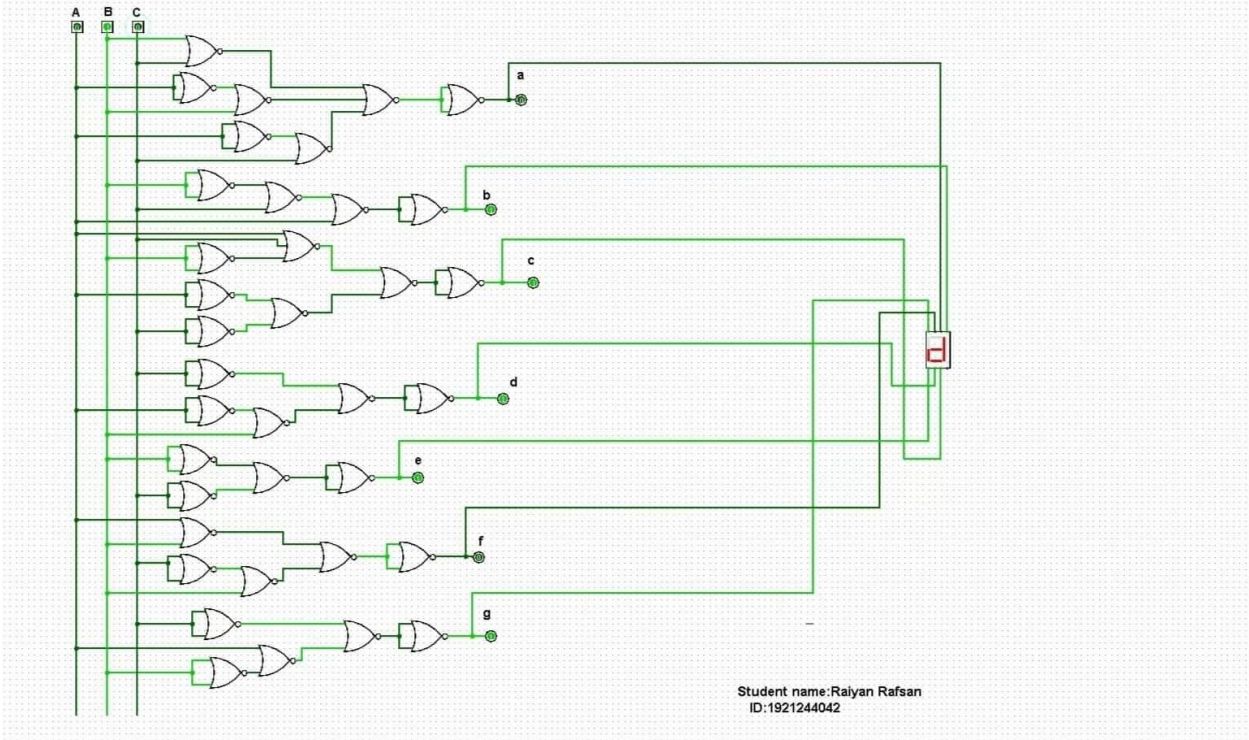


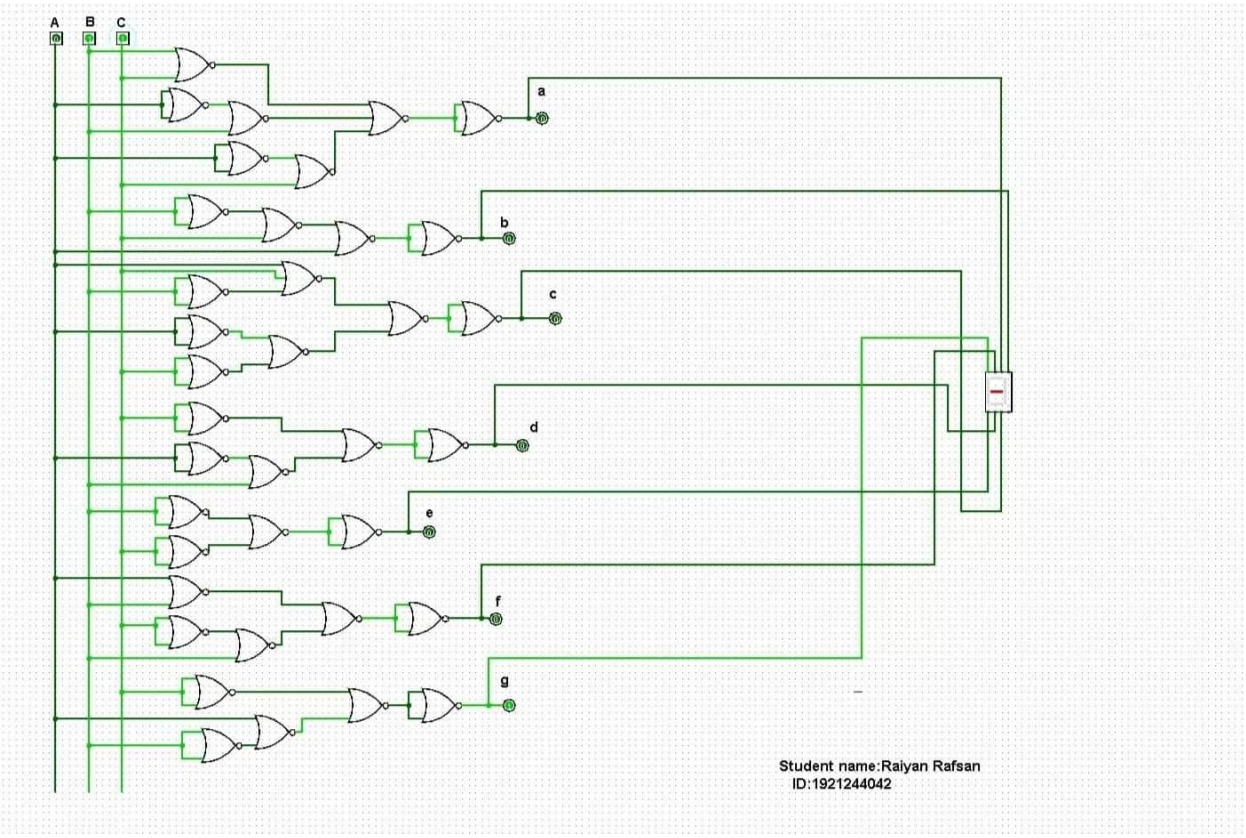
Name:Raiyan Rafsan
ID:1921244042

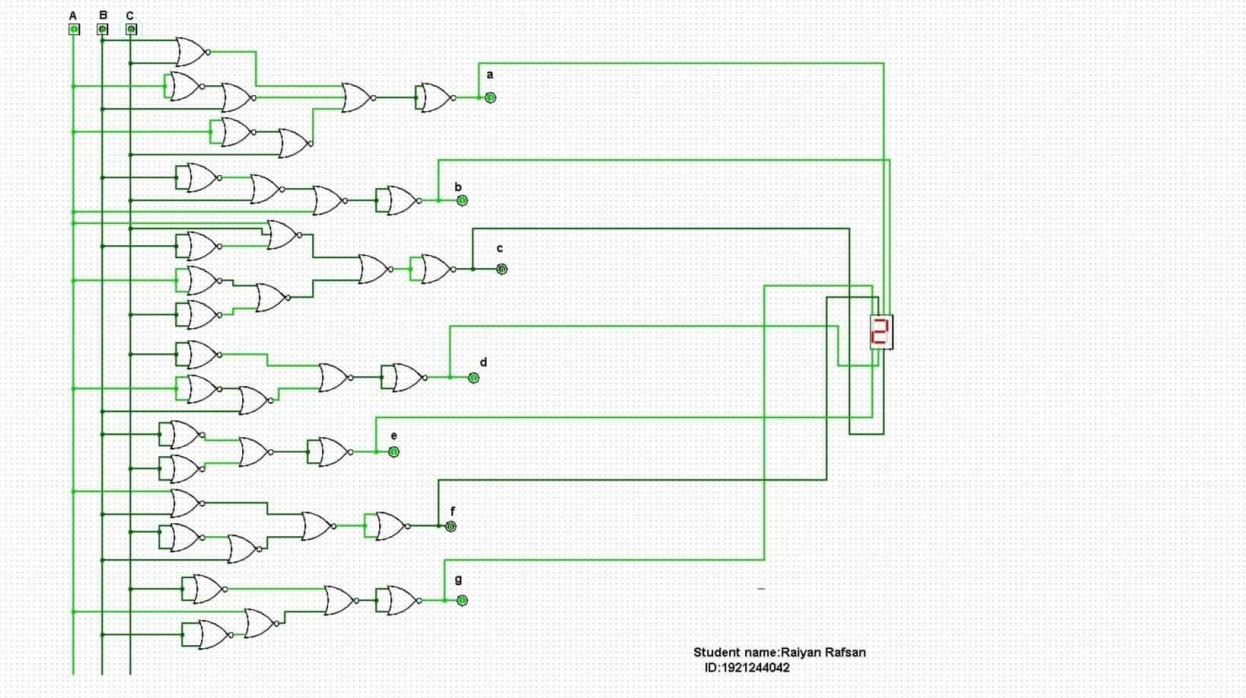
Seven segment display by Raiyan (NOR):

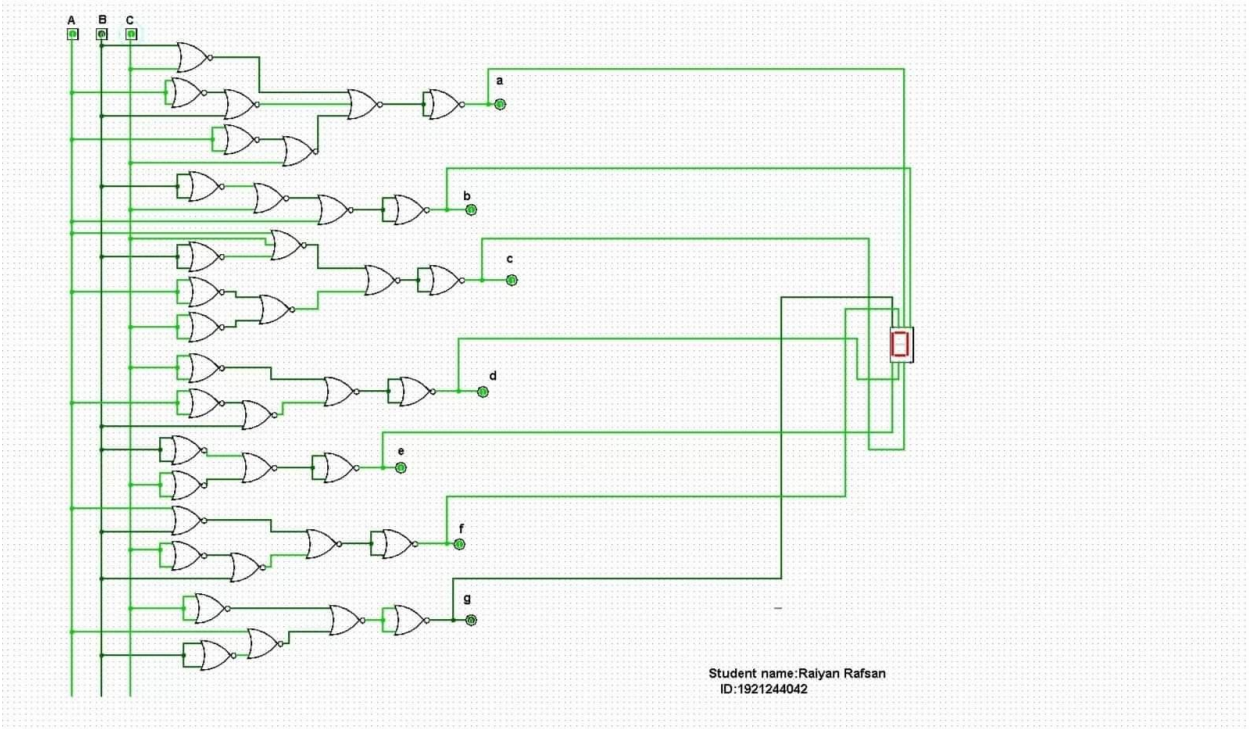



A
B
C
a
b
c
d
e
f
g
Student name:Raiyan Rafsan
ID:1921244042


A
B
C
a
b
c
d
e
f
g
Student name:Raiyan Rafsan
ID:1921244042


A
B
C
a
b
c
d
e
f
g
1
Student name:Raiyan Rafsan
ID:1921244042


A
B
C
a
b
c
d
e
f
g
2
Student name:Raiyan Rafsan
ID:1921244042


A
B
C
a
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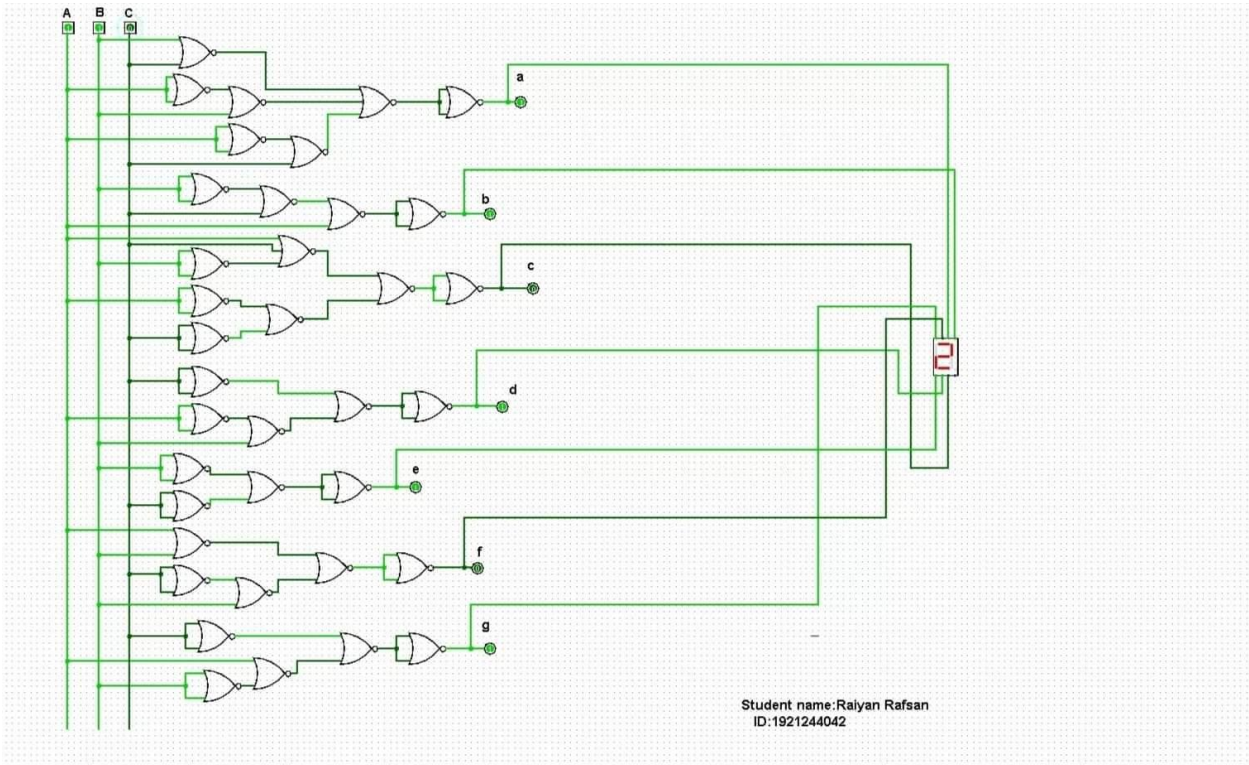
0
Student name:Raiyan Rafsan
ID:1921244042


A
B
C
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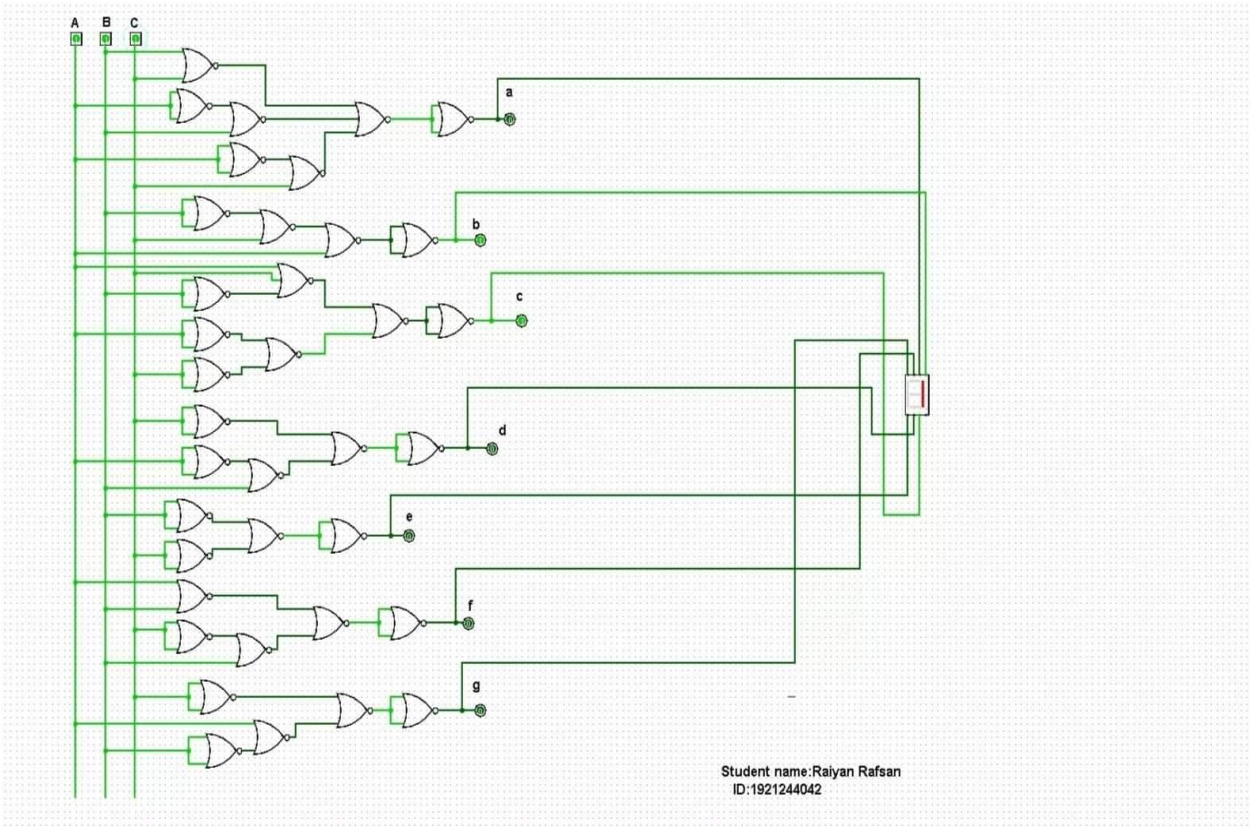
2
Student name:Raiyan Rafsan
ID:1921244042


A
B
C
a
b
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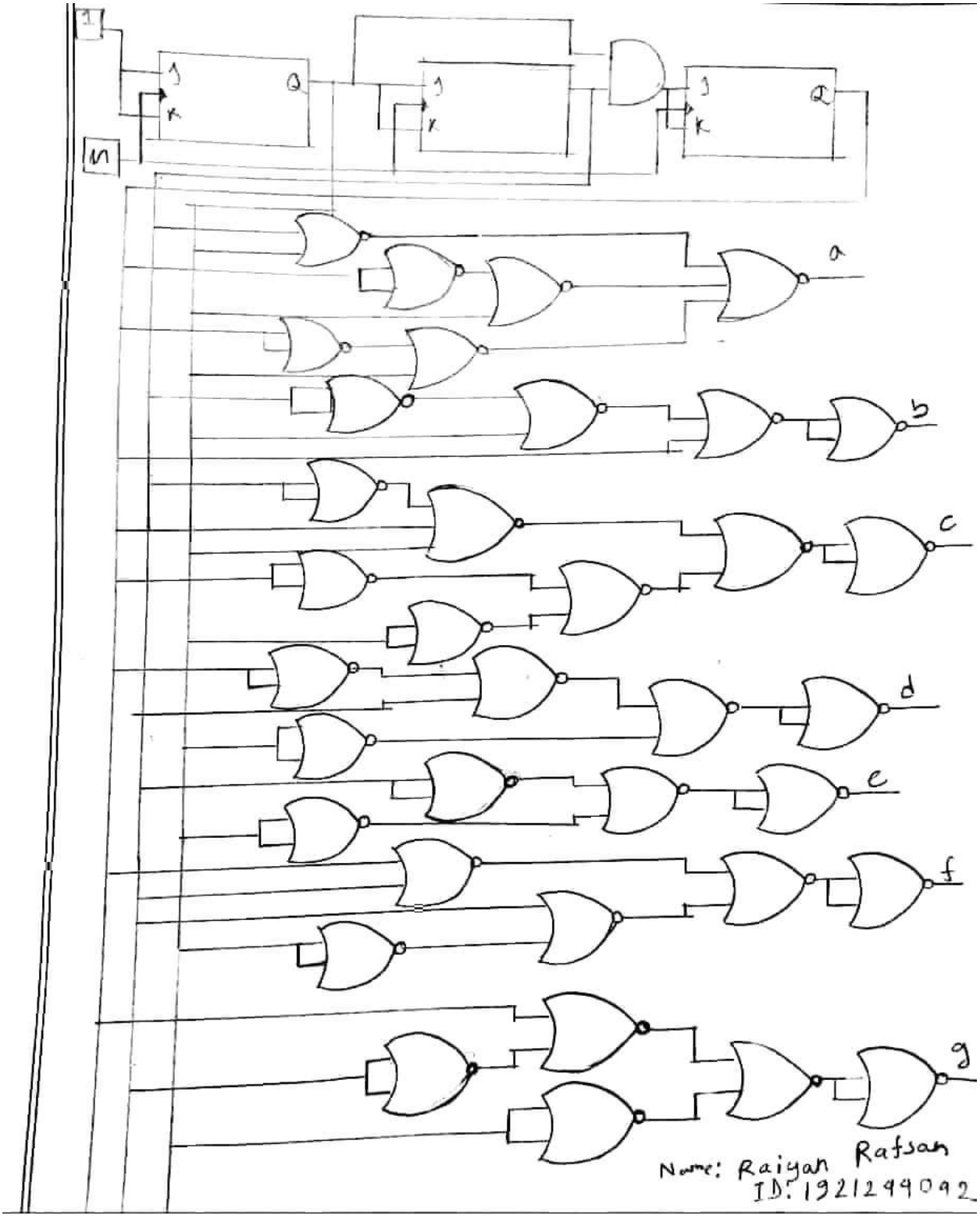
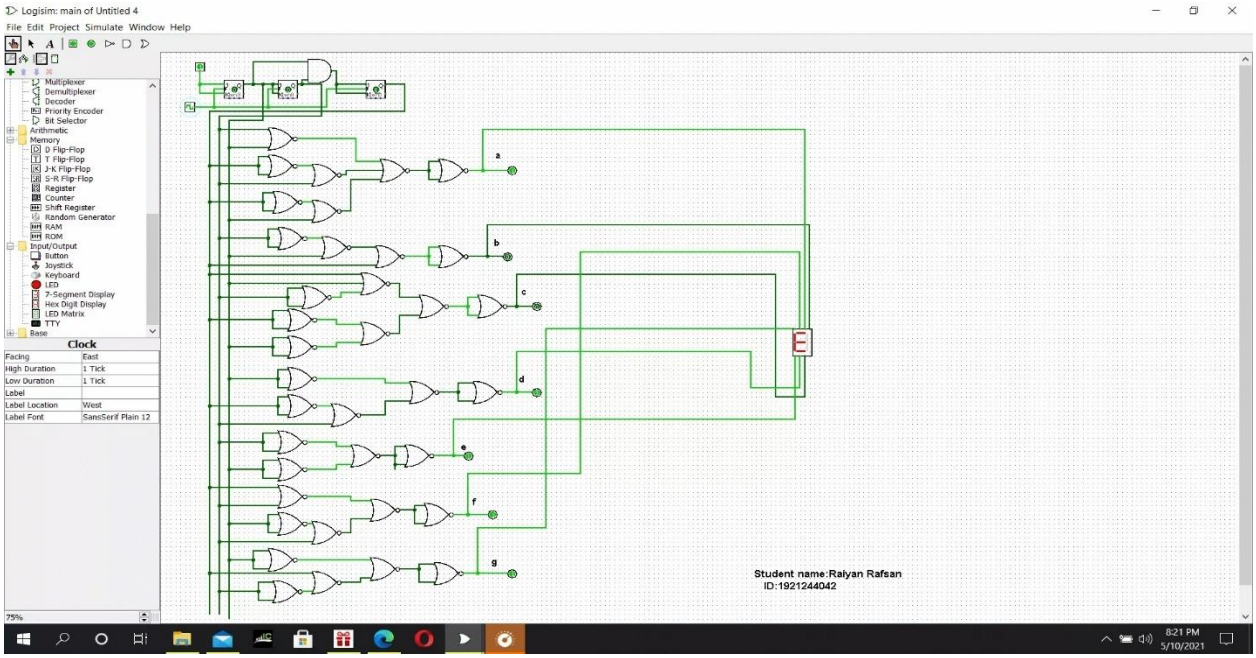
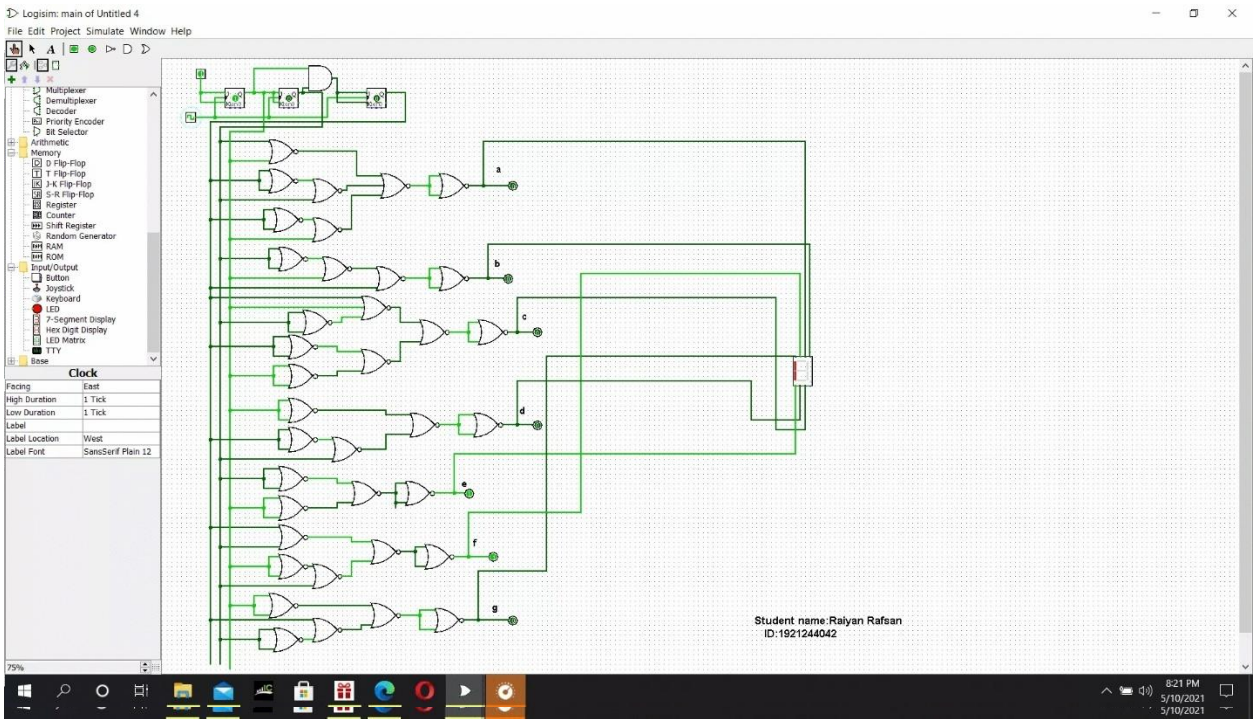
d
e
f
g
Student name:Raiyan Rafsan
ID:1921244042

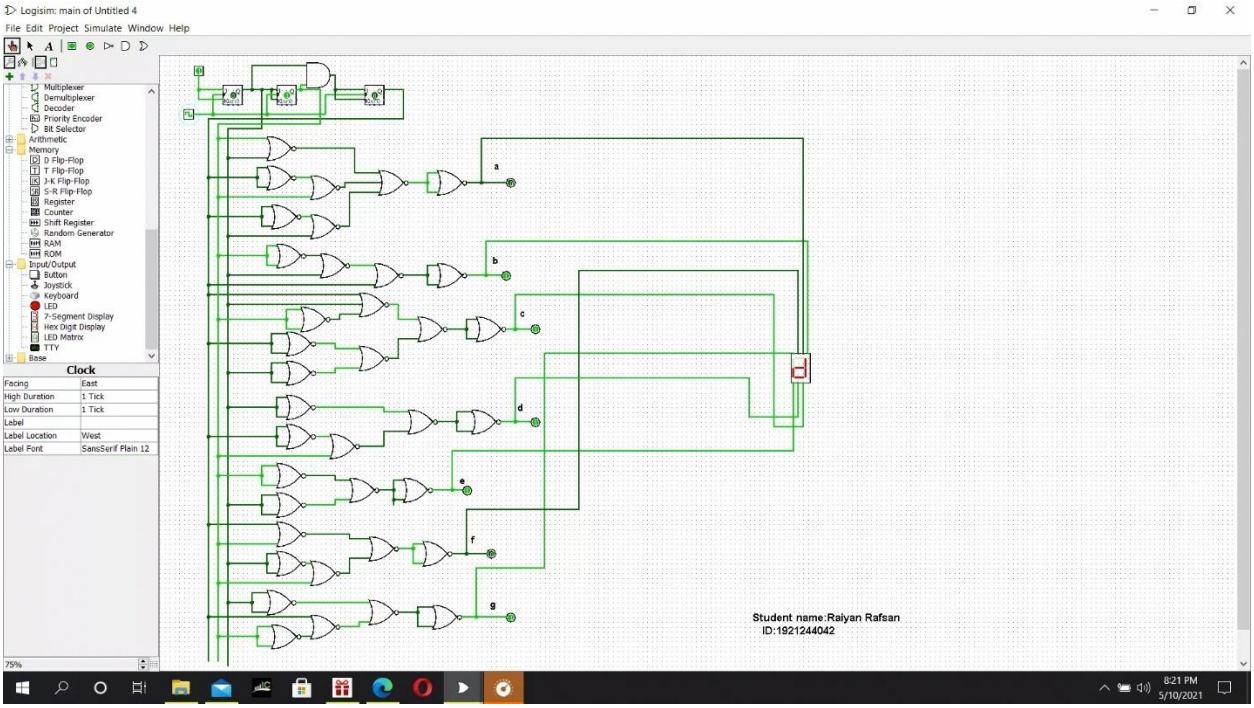
3 bit counter by Raiyan:

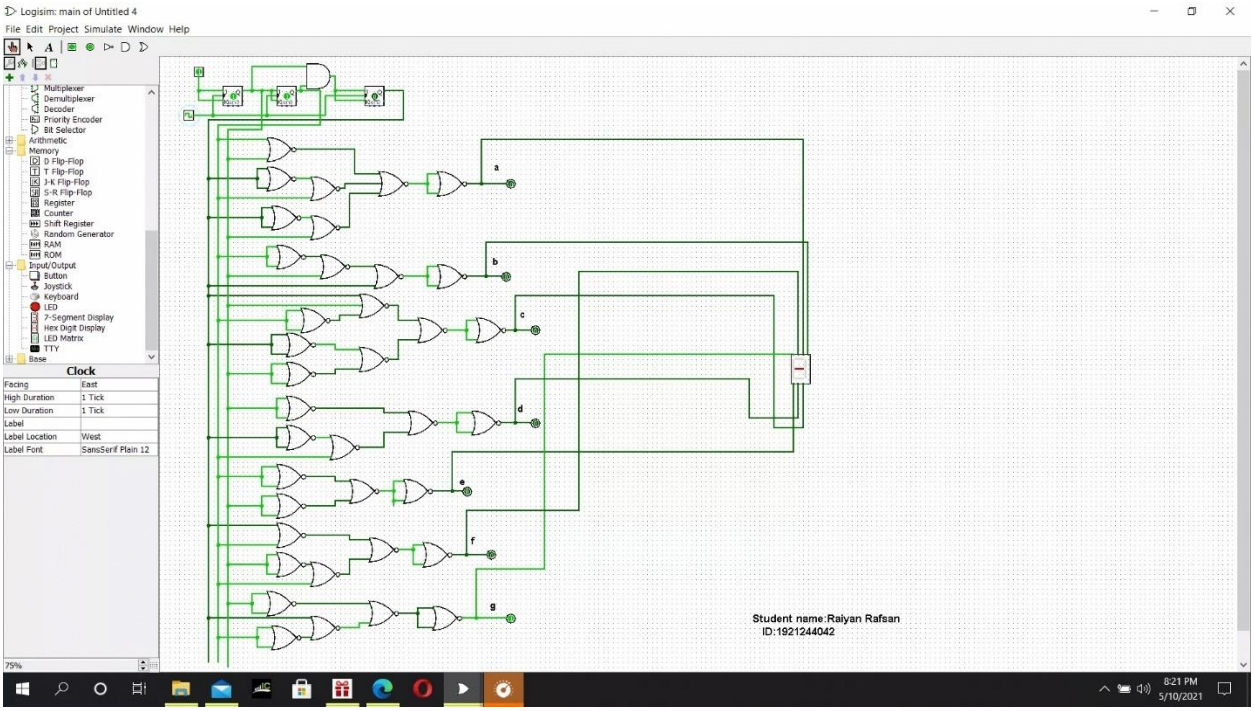


3 bit synchronous counter by Raiyan:






Logisim: main of Untitled 4
File Edit Project Simulate Window Help
Multiplexer
Demultiplexer
Decoder
Priority Encoder
Bit Selector
Arithmetic
Memory
D Flip-Flop
T Flip-Flop
J-K Flip-Flop
S-R Flip-Flop
Register
Counter
Shift Register
Random Generator
RAM
ROM
Input/Output
Button
Joystick
Keyboard
LED
7-Segment Display
Hex Digit Display
LED Matrix
TTY
Base
Clock
Facing East
High Duration 1 Tick
Low Duration 1 Tick
Label
Label Location West
Label Font SansSerif Plain 12
75%
a
b
c
d
e
f
g
Student name:Raiyan Rafsan
ID:1921244042
8:21 PM
5/10/2021


Logisim: main of Untitled 4
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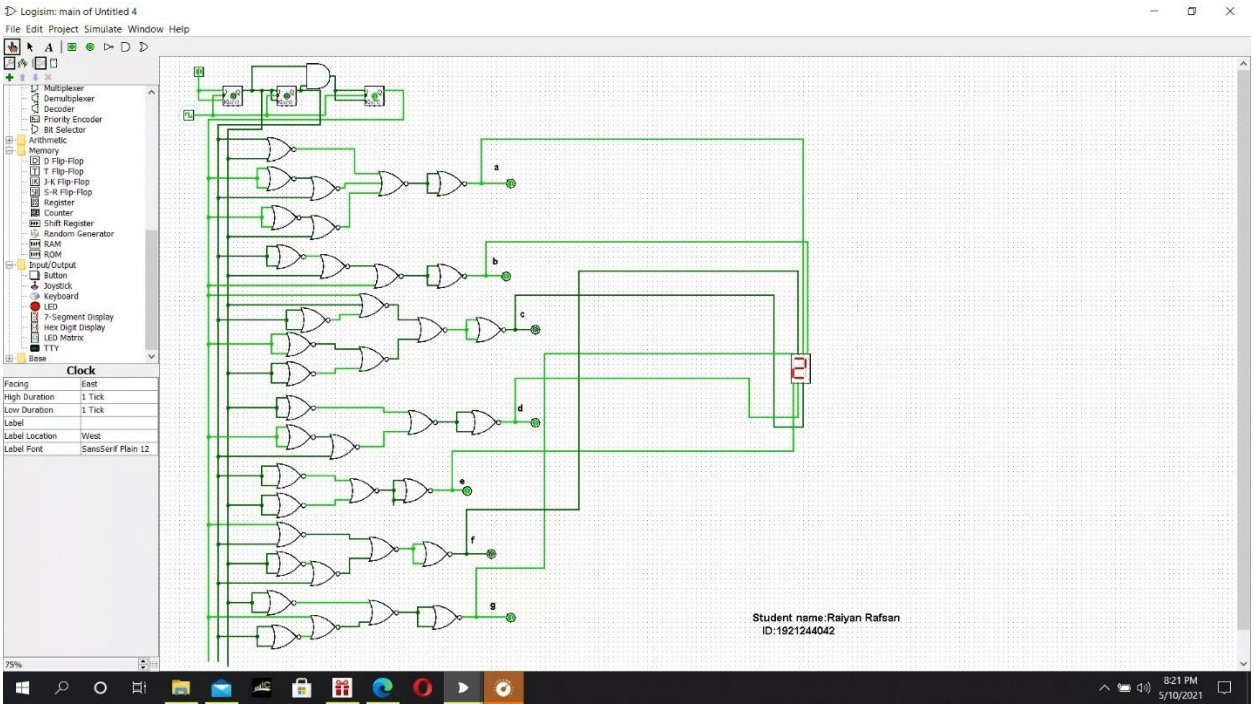
Student name:Raiyan Rafsan
ID:1921244042
8:21 PM
5/10/2021


Logisim: main of Untitled 4
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Clock
Facing East
High Duration 1 Tick
Low Duration 1 Tick
Label
Label Location West
Label Font SansSerif Plain 12
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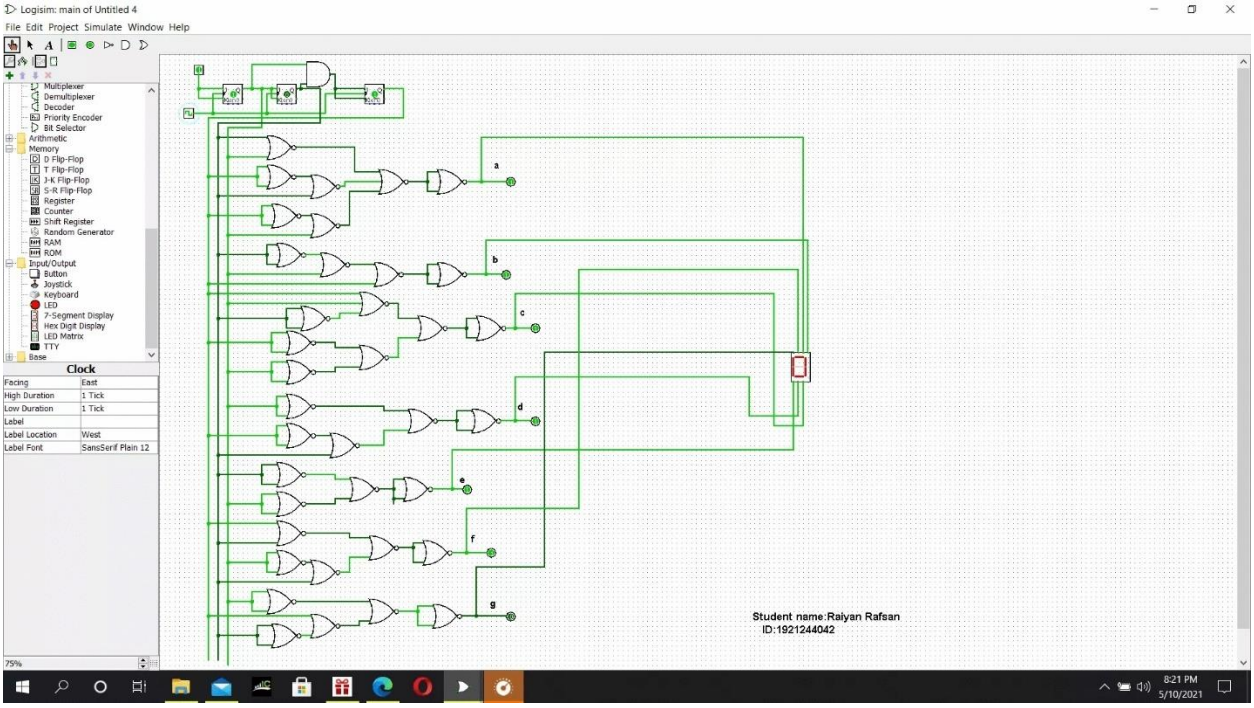
f
g
Student name:Raiyan Rafsan
ID:1921244042
75%
8:21 PM
5/10/2021


Logisim: main of Untitled 4
File Edit Project Simulate Window Help
Multiplexer
Demultiplexer
Decoder
Priority Encoder
Bit Selector
Arithmetic
Memory
D Flip-Flop
T Flip-Flop
J-K Flip-Flop
S-R Flip-Flop
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LED Matrix
TTY
Base
Clock
Facing East
High Duration 1 Tick
Low Duration 1 Tick
Label
Label Location West
Label Font SansSerif Plain 12
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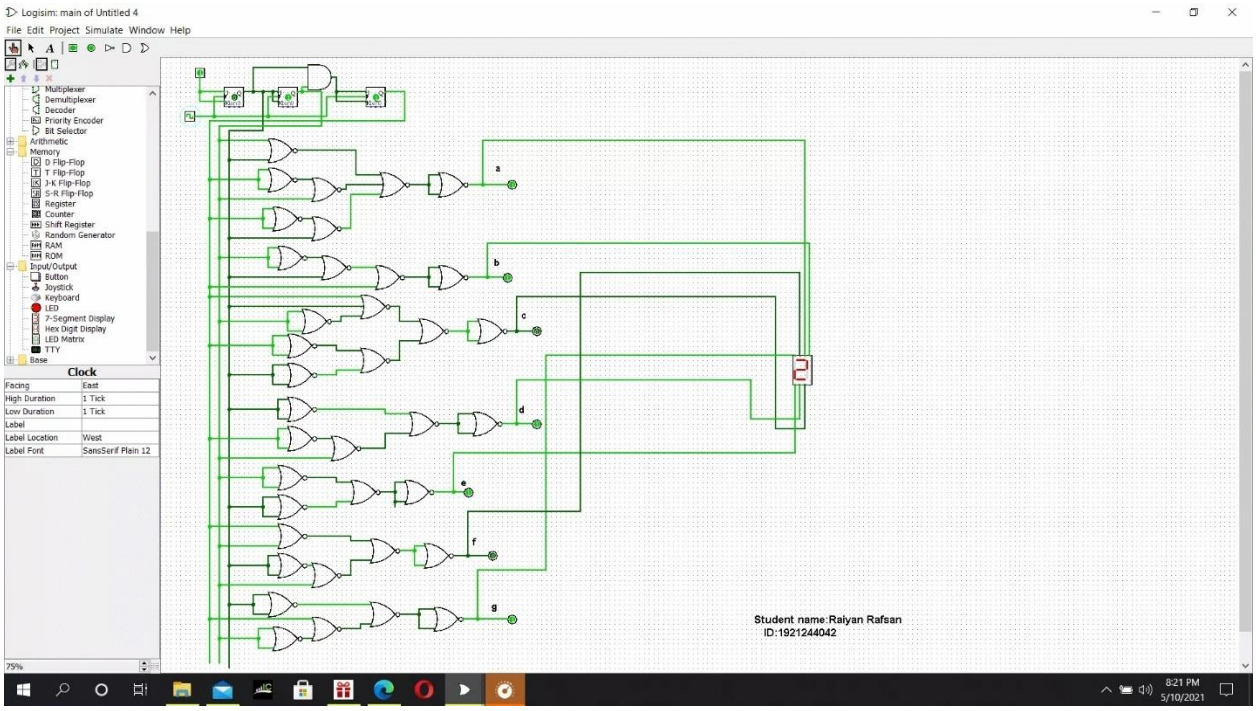
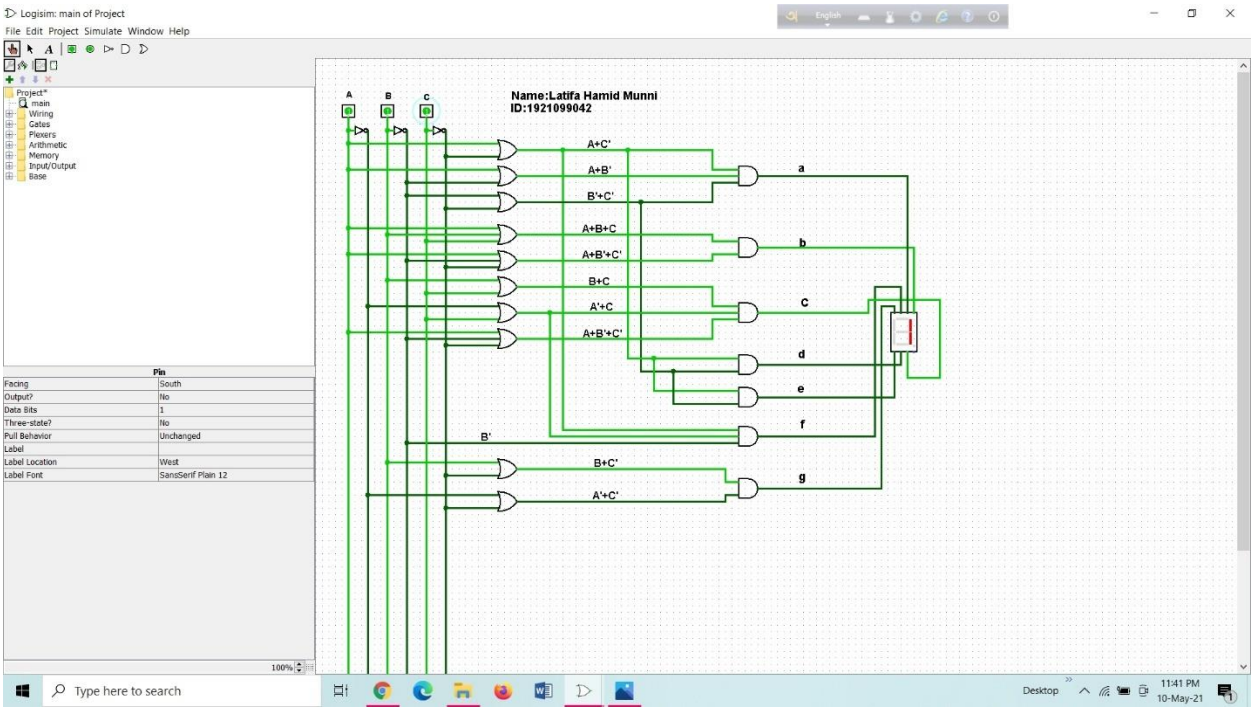
g
Student name:Raiyan Rafsan
ID:1921244042
75%
8:21 PM
5/10/2021


Logisim: main of Untitled 4
File Edit Project Simulate Window Help
Clock
Facing East
High Duration 1 Tick
Low Duration 1 Tick
Label
Label Location West
Label Font SansSerif Plain 12
a
b
c
d
e
f
g
Student name:Raiyan Rafsan
ID:1921244042
8:21 PM
5/10/2021


Logisim: main of Project
File Edit Project Simulate Window Help
Pin
Facing South
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label
Label Location West
Label Font SansSerif Plain 12
A
B
C
Name:Latifa Hamid Munni
ID:1921099042
A+C'
A+B'
B'+C'
A+B+C
A+B'+C'
B+C
A'+C
A+B'+C'
B'
B+C'
A'+C'
a
b
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d
e
f
g
Type here to search
Desktop
11:41 PM
10-May-21