



North South University
Department of Electrical & Computer Engineering

LAB REPORT

Course Name: CSE231L

Section: 10

Experiment Number: **08**

Experiment Name: **Introduction to Flip-Flop and Register circuit.**

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Group Number: N/A

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Remarks:	

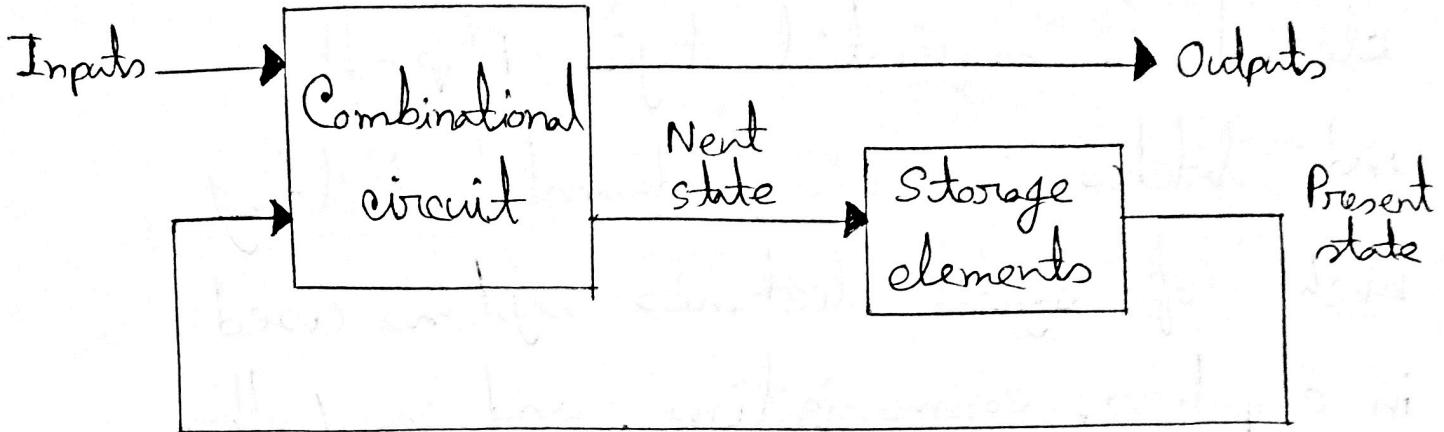
Name : Introduction to Flip-Flop and Register circuit.

Objectives :

- * Familiarize with the analysis of Flip-Flop & Register circuits.
- * Learn the implementation of Flip-Flop & Register circuits.
- * Verify the Flip-Flop & Register circuit with the Truth table.

Theory :

Digital electronic circuit is classified into combinational logic and sequential logic. Combinational logic output depends on the inputs levels, whereas sequential logic output depends on stored levels and also the input levels.



The storage elements (Flip-flops) are devices capable of storing 1-bit binary info. The binary info stored in the memory element determine the output. Storage elements next state is also a function of external inputs and present state.

Flip-Flop

A flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one

or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

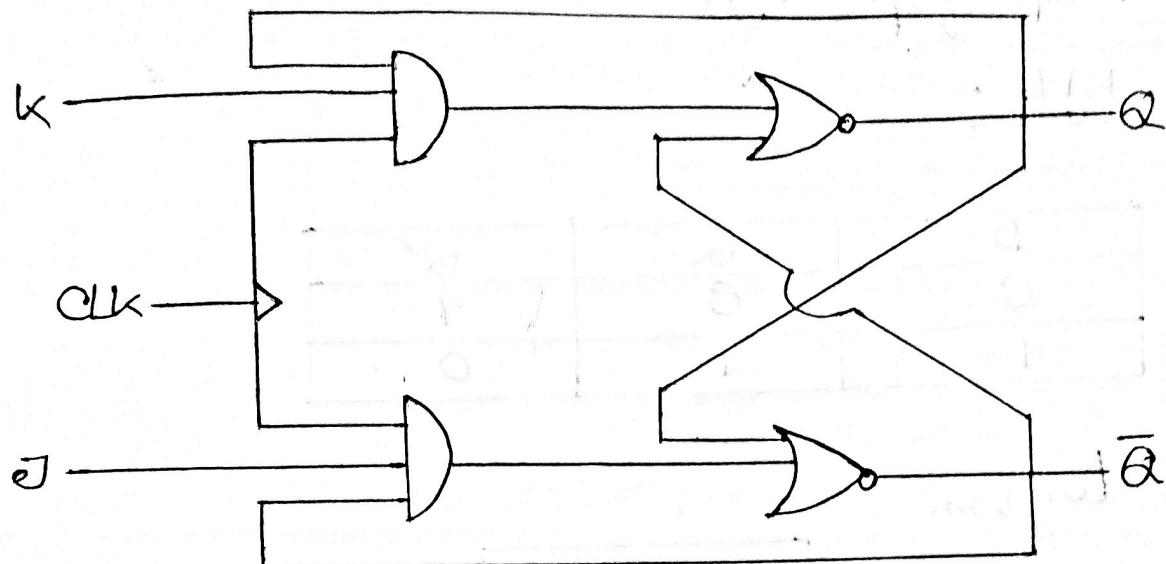
We'll design JK flip-flop, T flip-flop and D flip-flop in this experiment.

JOB - 1 : Design of a JK Flip-flop using AND & NOR gates only.

Truth table:

J	K	Q	\bar{Q}
1	0	1	0
0	0	$Q = 1$	$\bar{Q} = 0$
0	1	0	1
0	0	$Q = 0$	$\bar{Q} = 1$
1	1	$\bar{Q} = 1$	$Q = 0$
1	0	1	0
1	1	$\bar{Q} = 0$	$Q = 1$

Circuit diagram:

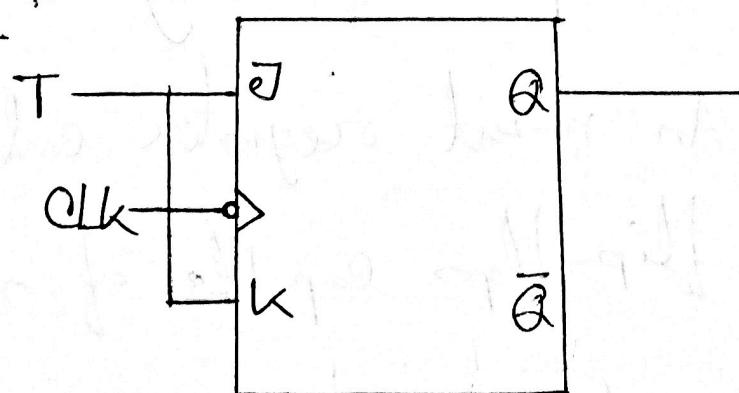


JOB-2: Design of a T Flip-flop using J-K Flip-flop only.

Truth table:

T	Q	Q'
0	Q	\bar{Q}
1	\bar{Q}	Q.

Circuit diagram:



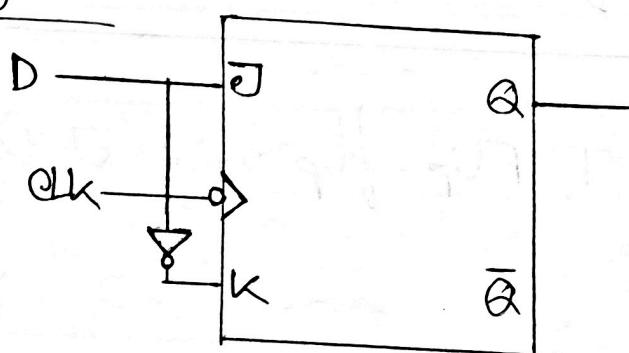
JOB-3: Design of a D flip-flop using

J-K Flip-flop only.

Truth table:

D	Q	Q'
0	0	1
1	1	0

Circuit diagram:



Register:

A register is a group of flip-flops.

Each flip-flop is capable of storing one bit of information. An n-bit register contains a group of n flip-flops capable of storing n bits of binary information. In addition

to flip-flops, a register may have combinational gates that perform certain data processing tasks. In broadest definition, a register consists of a group of flip-flops and gates that effect their transition. The flip-flop holds binary information and the gates determine how the information is transferred into the registers.

A register is capable of shifting its binary information either to its right or its left is called a shift register. The logical configuration of a shift register consists of a chain of flip-flops

connected in cascade, with the output of one flip-flop connected to the input of the next flip-flop.

All flip-flops receive a common pulse which causes the shift from one stage to the next.

In this experiment, you will use D flip-flop to

construct a 4 bit right shift register.

JOB-4: Design of a 4bit Right Shift

Register circuit using D Flip-flop.

IC 7474 :

PINS	DESCRIPTION
D0, D1	Data inputs
CP0, CP1	Clock inputs (active rising edge)
SD0, SD1	Set inputs (active low)
RD0, RD1	Reset inputs (active low)
Q0, Q1, Q0, Q1	Data outputs

Circuit diagram :

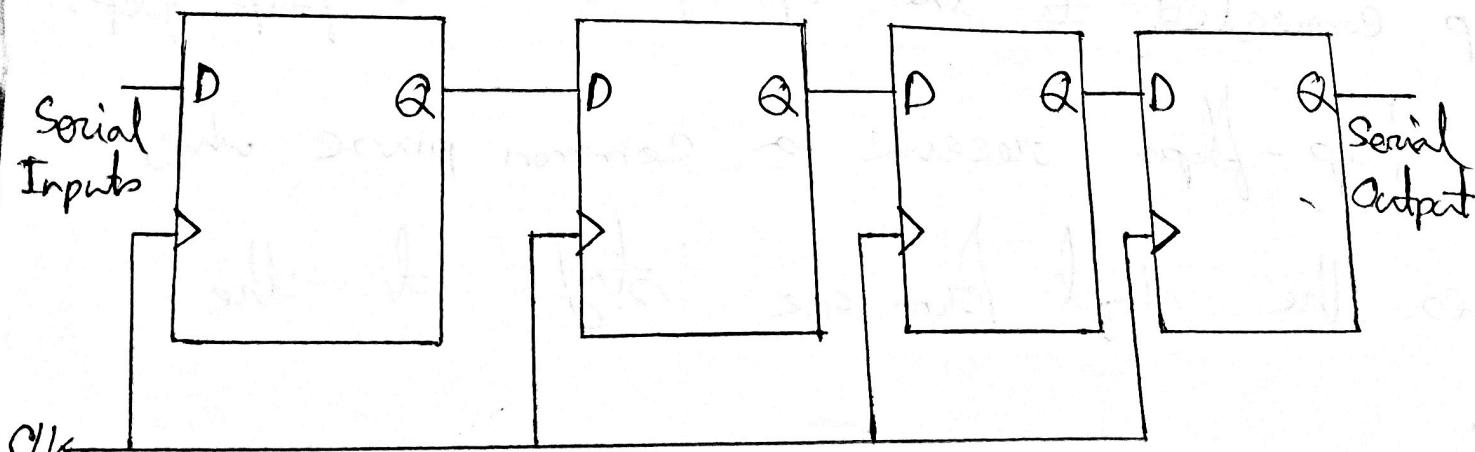


Figure : Shift Register

State Table

States	Input	Output
Initial State	X	xxxx
T1	1	1xxx
T2	0	01xx
T3	1	101x
T4	0	0101

Assignment :

SR flip-flop :

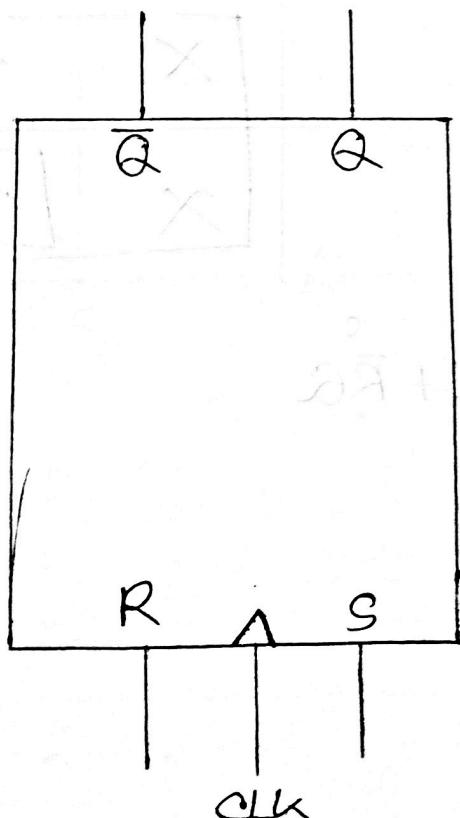


Figure : Logic Diagram for SR flip flop.

Q	S	R	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	in determinate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	in determinate.

Truth table : S-R Flip Flop.

SR	00	01	11	10
Q			X	1
Q	1	1	X	1

$$Q(t+1) = S + \bar{R}Q$$

$$SR = 0.$$

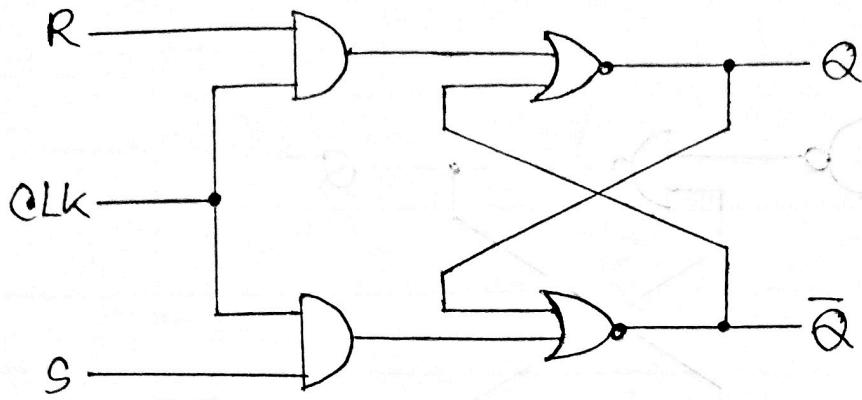


Figure : S-R Flip Flop Circuit.

D Flip Flop :

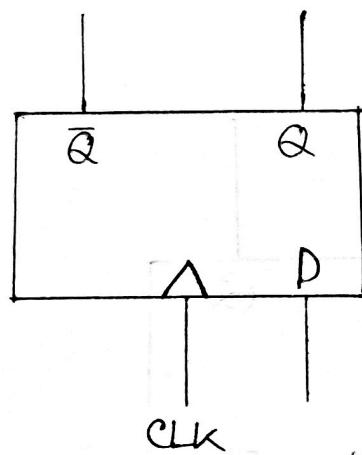
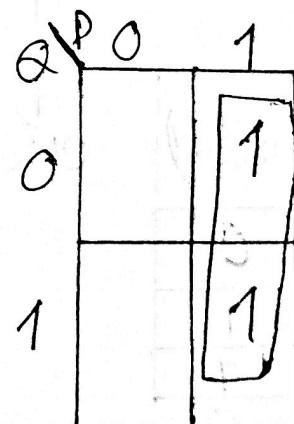


Figure : Logic diagram for D flip flop.

Q	D	$Q(t+1)$
0	0	0
0	1	1
1	0	0
1	1	1



Truth table : D Flip Flop.

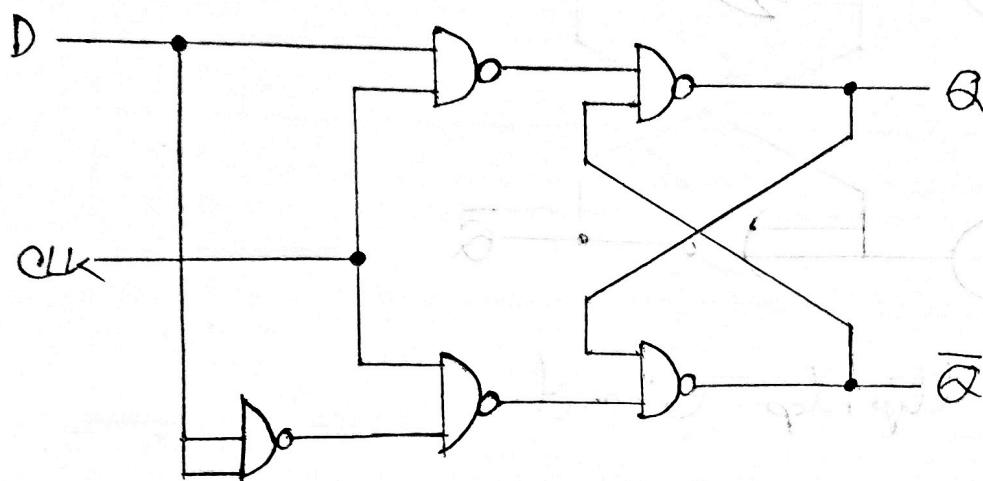
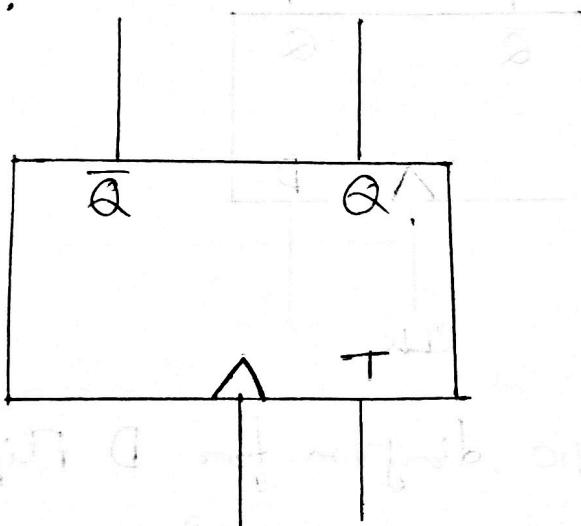


Figure : D Flip-Flop circuit.

T Flip-Flop :



Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Q	0	1
0	0	1
1	1	0

$$Q(t+1) = T\bar{Q} + \bar{T}Q$$

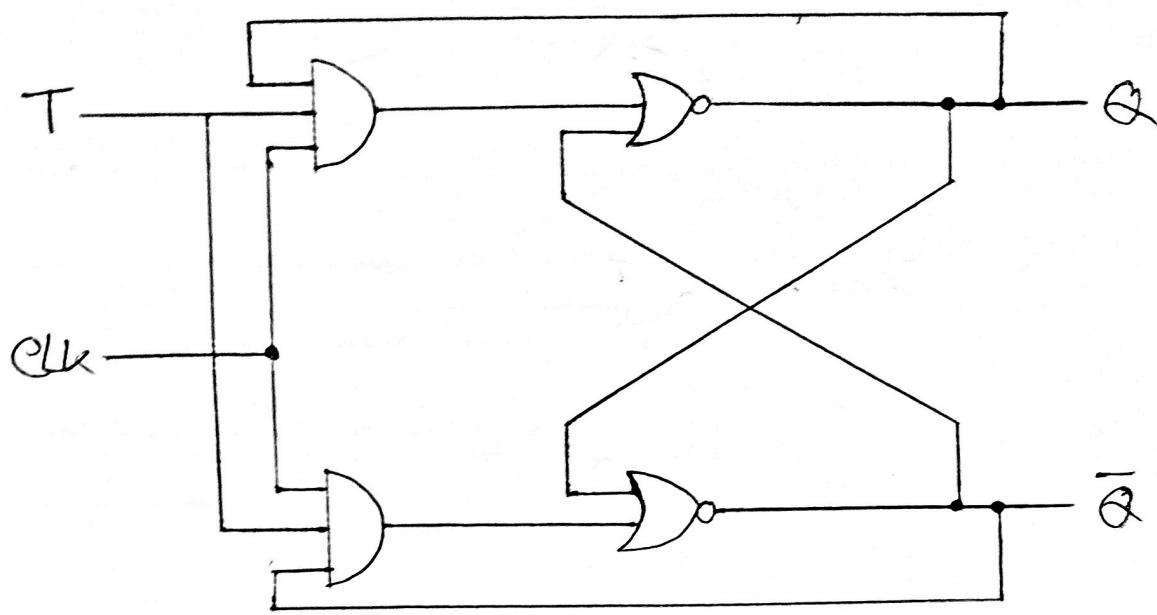


Figure : T Flip Flop Circuit.