



**North South University**  
Department of Electrical & Computer Engineering

**LAB REPORT**

Course Name: CSE231L

Section: 10

Experiment Number: **06**

Experiment Name: : **BCD to seven segment decoder**

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Group Number: N/A

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Remarks:	

Name : BCD to seven segment decoder.

Objectives :

- Familiarize with the analysis of Seven Segment Decoder circuits.
- Learn the implementation of Seven Segment Decoder using Display.
- Verify the Seven Segment Decoder with the logic.

Apparatus :

- Trainer Board
- 1 × IC 7447 Decoder.
- 1 × Seven segment Display
- 7 × Resistors.

### Theory :

An ABCD to seven segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display decimal digit in a familiar form. The seven outputs of the decoder ( $a, b, c, d, e, f, g$ ) select the corresponding segments in the display, as shown in figure (a). The numeric display chosen to represent the decimal digit is shown in figure (b).

Each element ( $a, b, c, d, e, f, g$ ) of the seven segment display is turned on when a logic low is applied to its

corresponding input pin.

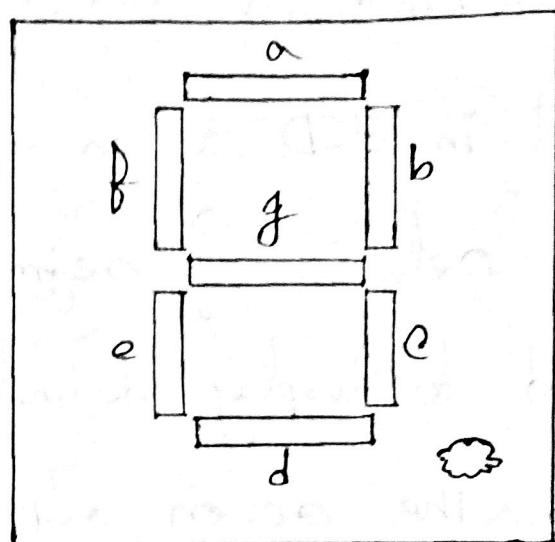
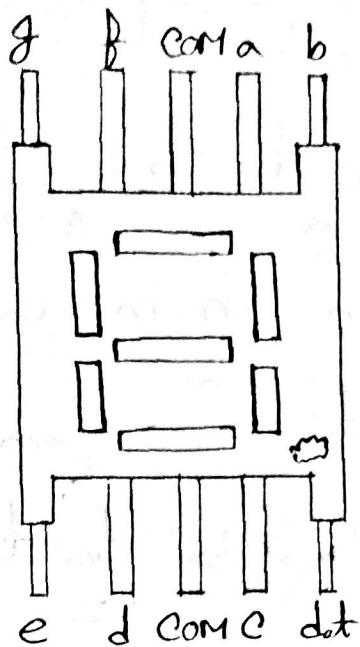
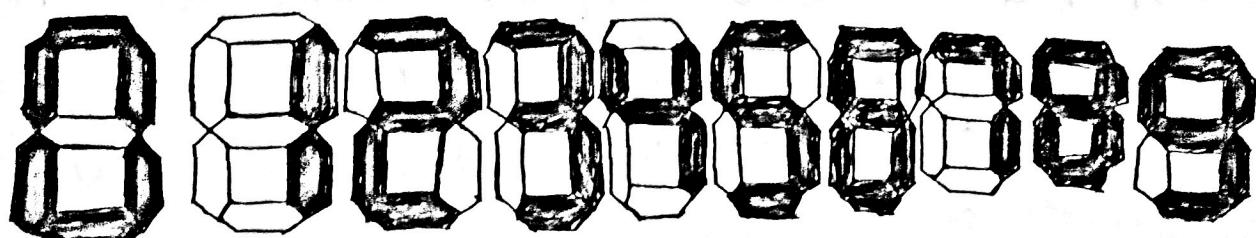
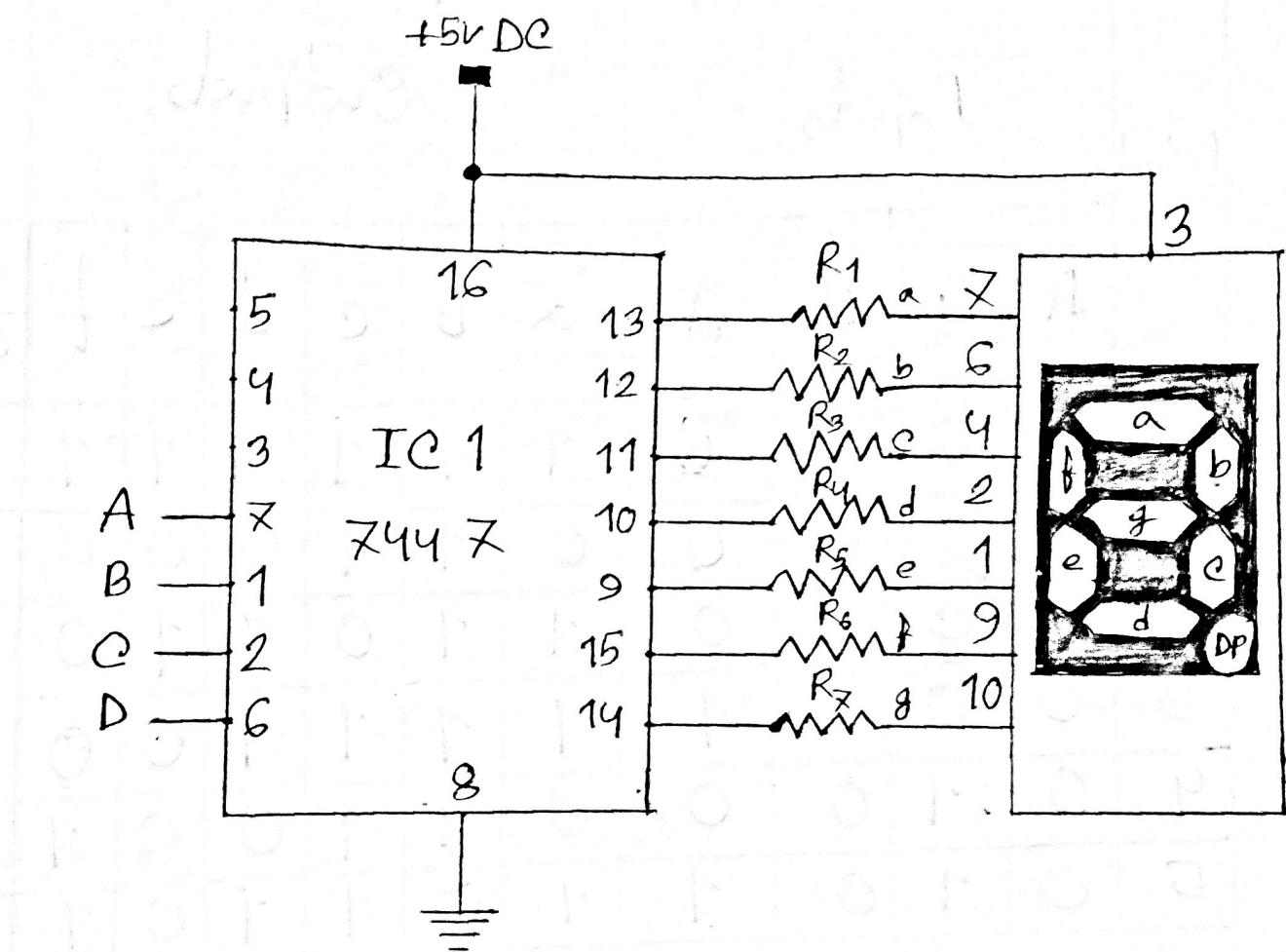


Figure (a) : Seven-Segment Display



Figure(b) : Display of decimal digits with  
a 7-segment device.

## Circuit Diagram :



$$R_1 \text{ to } R_7 = 220 \text{ ohm.}$$

Truth Table:

Decimal	Inputs.				Outputs.						
	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	1	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Assignment :

(a)

AB		CD		C		D	
00	01	00	01	11	10	00	01
1	1	0	1	1	1	1	1
0	1	1	1	1	1	1	1
X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X

$$\therefore F_1(A, B, C, D) = A + C + BD + \bar{B}\bar{D}$$

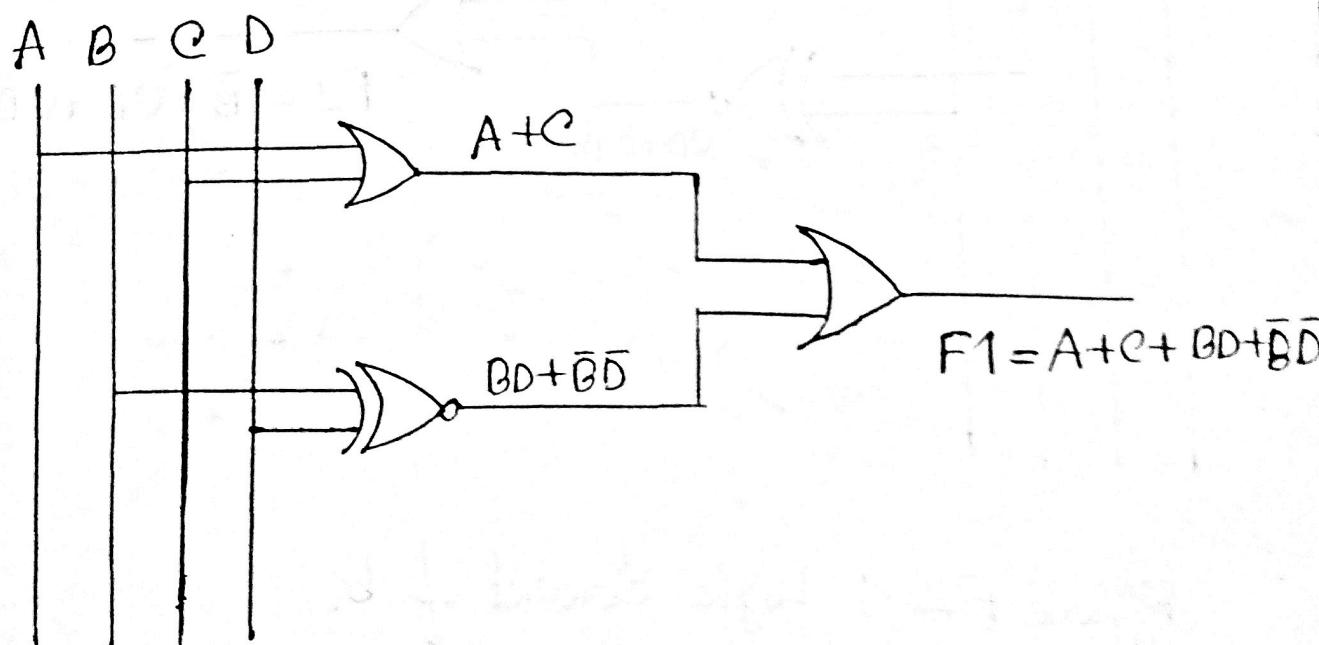


Figure F1 : Logic circuit of a.

(b)

AB		CD	00	01	11	10
			0	1	1	1
			00	01	11	10
A	00	1	1	1	1	1
	01	1	0	X	1	0
	11	X	X	X	X	X
	10	1	1	X	X	X

$$\therefore F_2(A, B, C, D) = \bar{B} + CD + \bar{C}\bar{D}$$

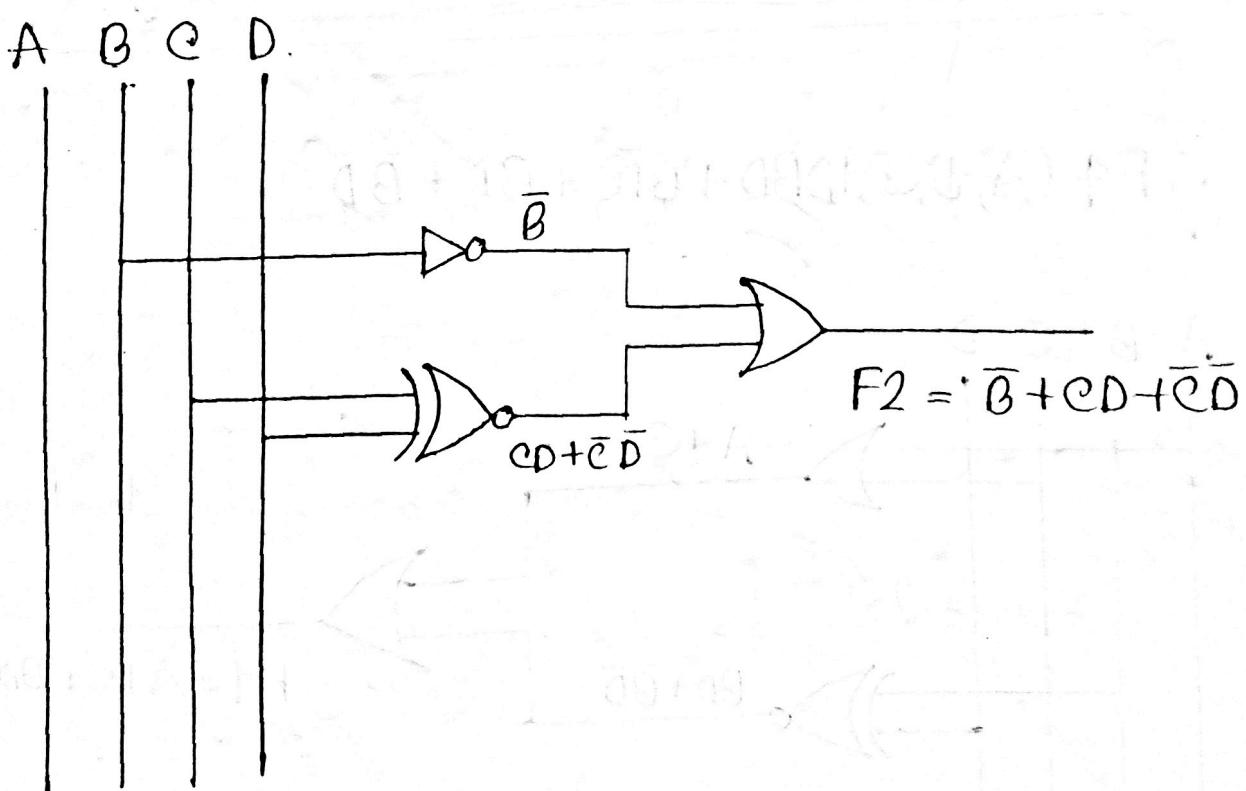


Figure F2 : Logic circuit of b.

		(C)		D.	
AB		00	01	11	10
CD		00	1	1	1
00	00	1	1	1	0
01	01	1	1	1	1
11	11	X	X	X	X
10	10	1	1	X	X

$$\therefore F_3(A, B, C, D) = B + \bar{C} + D.$$

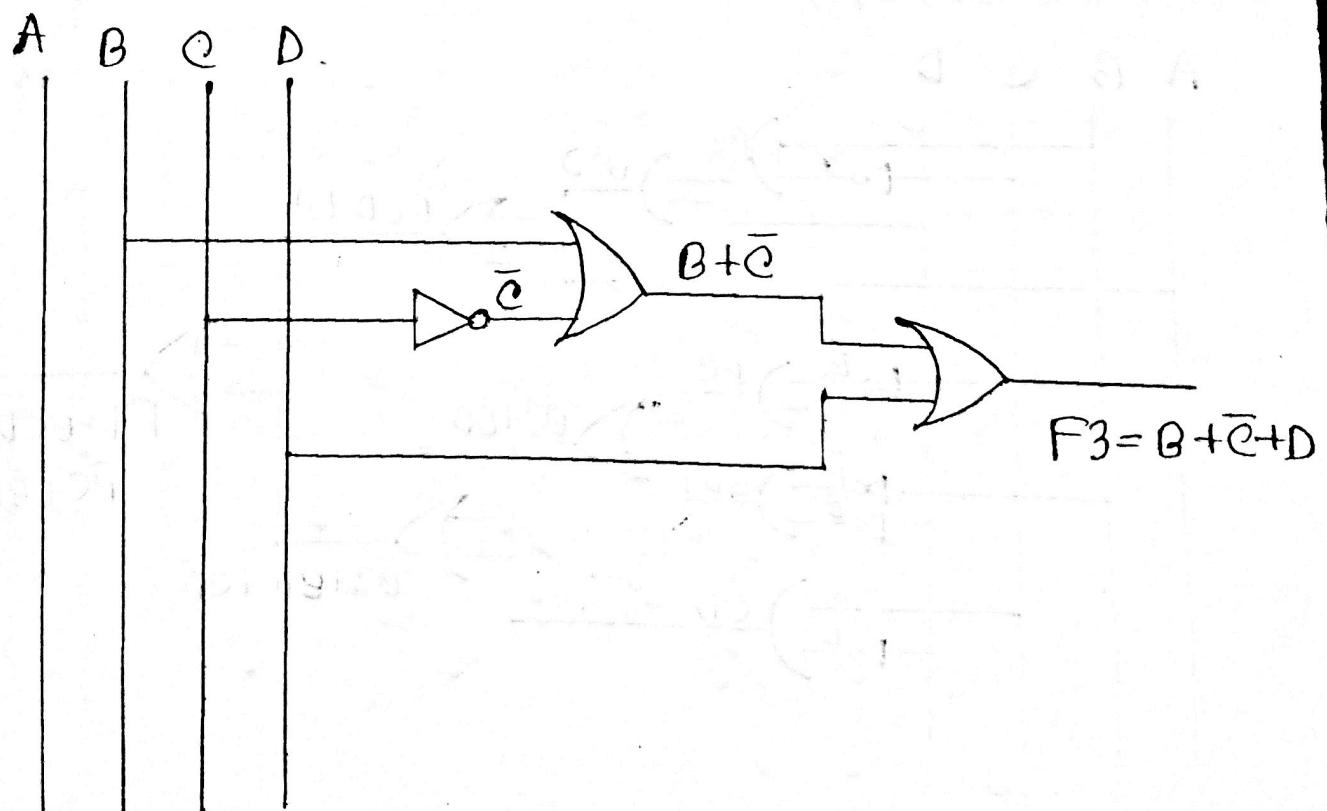


Figure F3 : Logic circuit of c.

(d)

		00		01		11		10	
		00	1	0	1	1	1	1	
		01	0	1	0	0	1	1	
		11	X	X	1	X	X	X	
		10	1	1	1	X	X	X	

A      D      B

$$\therefore F_4(A, B, C, D) = B\bar{C}D + A + \bar{B}C + \bar{B}\bar{D} + C\bar{D}$$

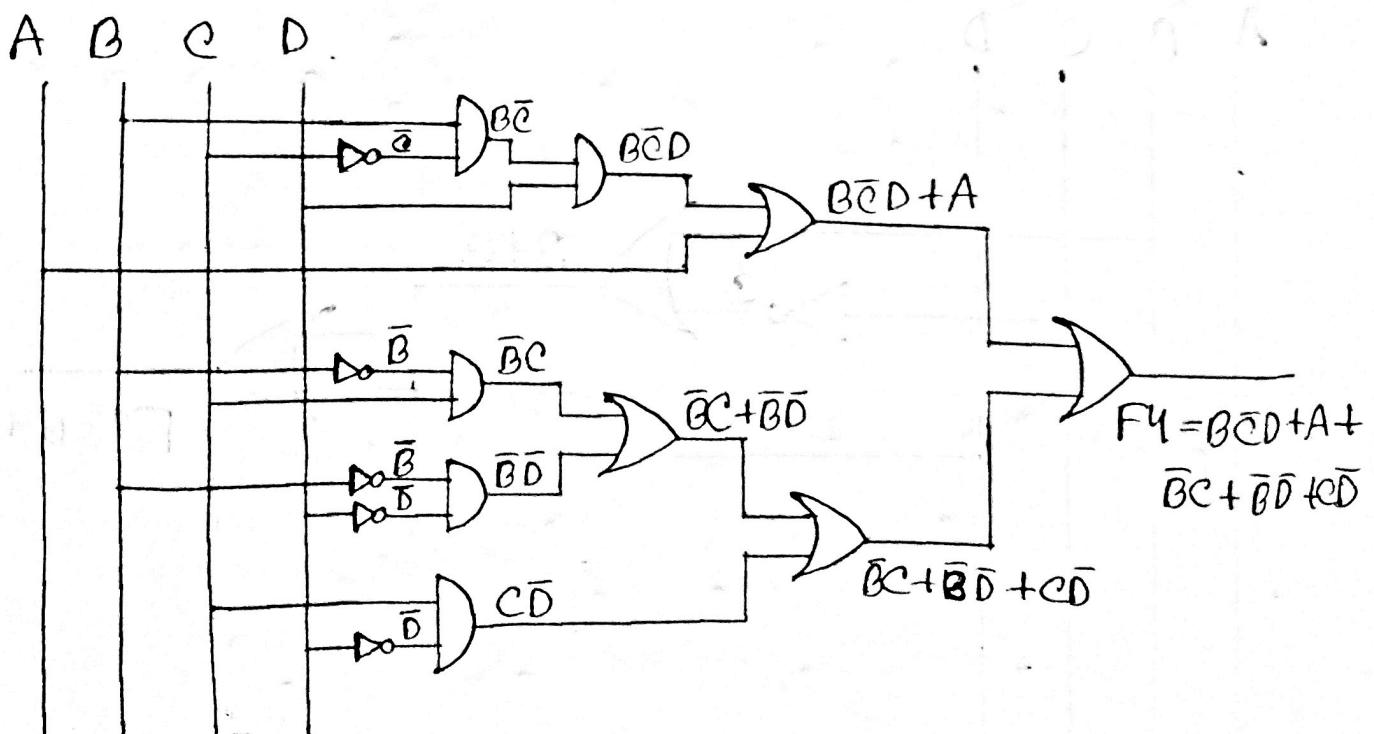


Figure F4 : Logic circuit of d.

(e)

$A\backslash B$	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	X	X	X	X
10	1	0	X	X

$D$

$$\therefore F_5(A, B, C, D) = \overline{BD} + \overline{CD}$$

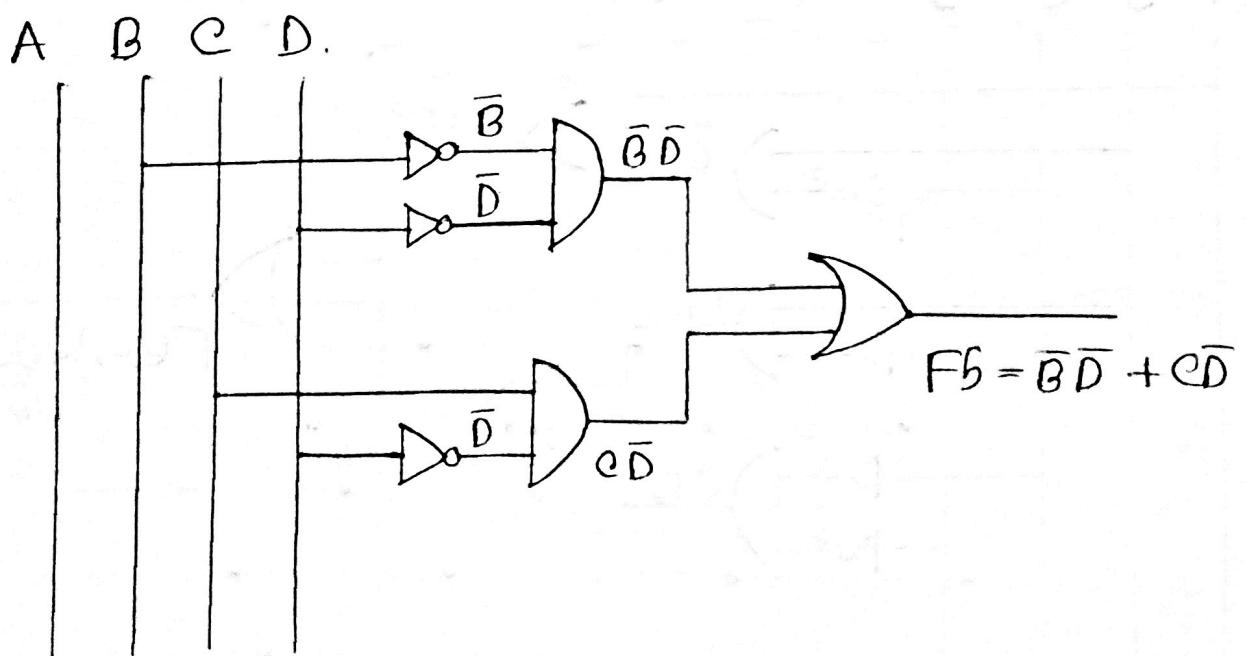


Figure F5 : Logic circuit of e.

(F)

$A \oplus D$	00	01	11	10
	0	1	3	2
	4	5	7	6
A	1	1	0	0
	X	X	X	X
B	1	1	0	1
	X	X	X	X
D	1	1	1	1

$$F_6(A, B, C, D) = A + B\bar{C} + B\bar{D} + \bar{C}\bar{D}$$

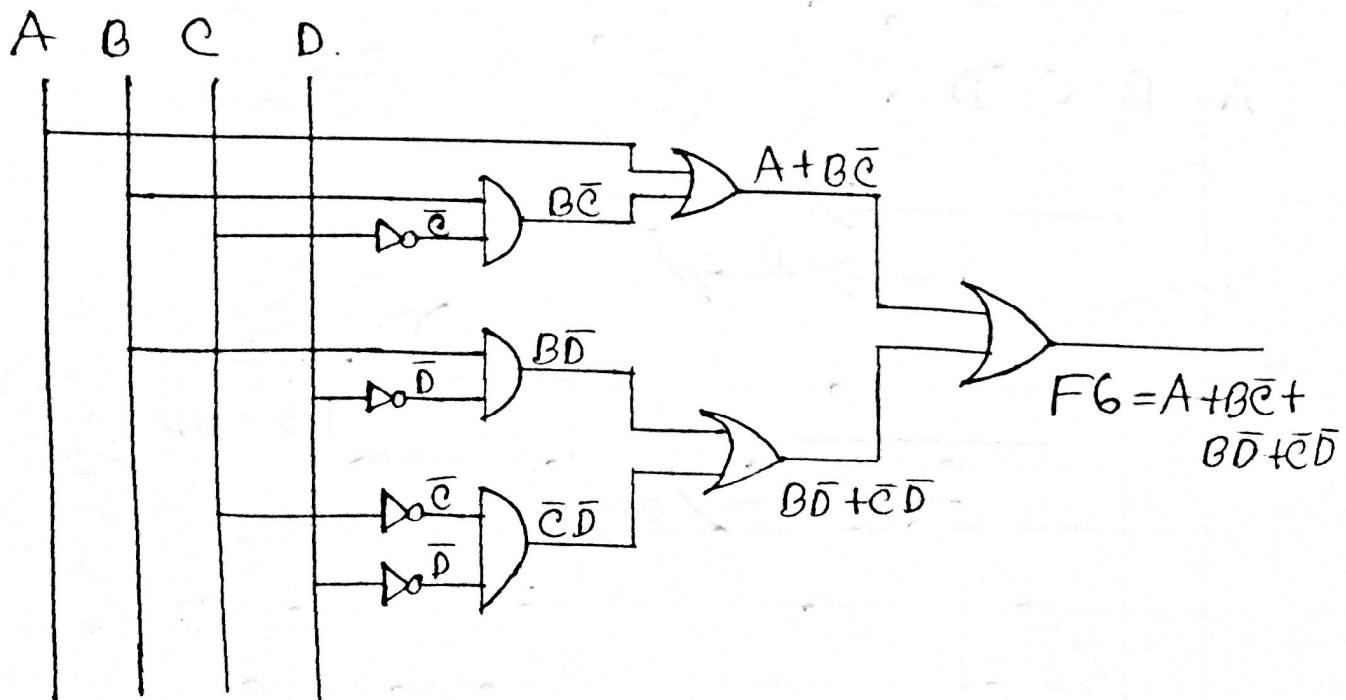


Figure F6 : Logic circuit of f.

(g)

AB		CD		00		01		11		10	
A	B	C	D	00	01	10	11	11	10	10	11
0	0	0	0	0	0	1	0	1	1	1	1
0	1	0	0	1	1	1	X	0	1	1	1
1	1	X	X	X	X	X	X	X	X	X	X
1	0	1	1	1	1	1	X	X	X	X	X

$$F_7(A, B, C, D) = A + B\bar{C} + \bar{B}\bar{C} + C\bar{D}$$

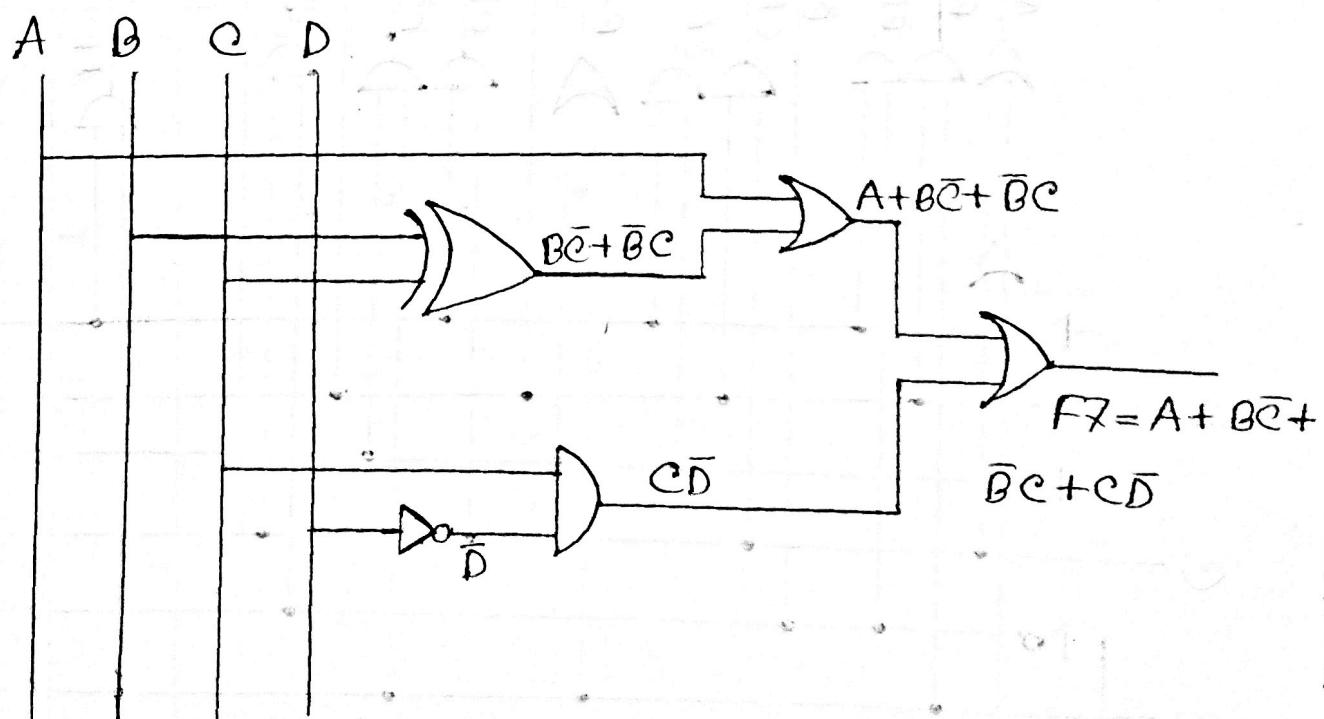


Figure F7 : Logic circuit of g.

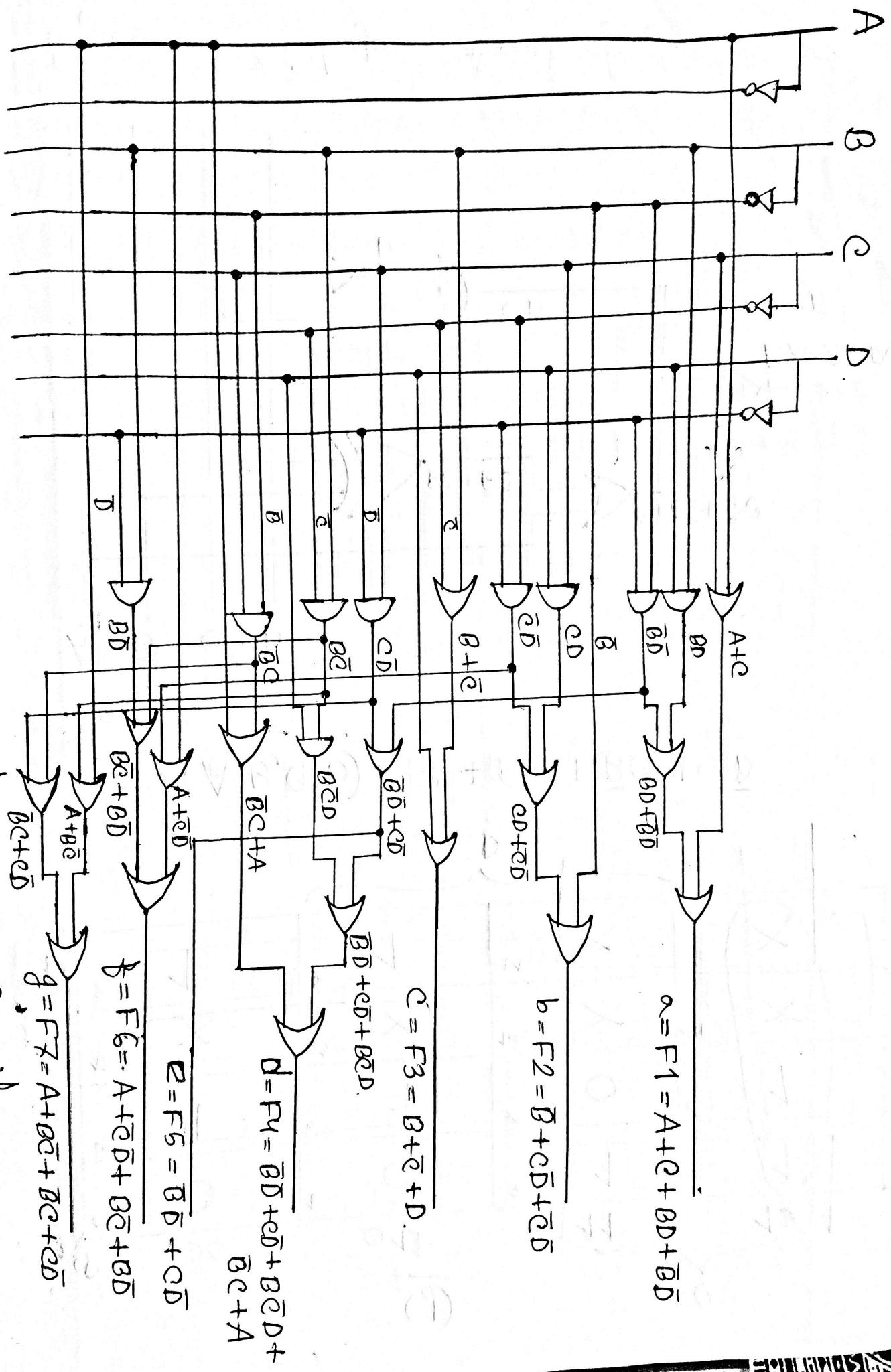


Figure : The Seven Segment Decoder Circuit.