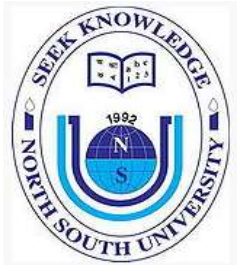


North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	02
Experiment Title:	Design a 4-bit by 4-bit Binary Multiplication Unit.
Course Code:	**CSE332L**
Course Name:	**Computer Organization & Architecture Lab**
Name & ID:	Mosroor Mofiz Arman, 1921079642
Date of Experiment:	10.11.2021
Date of Submission:	10.11.2021

Objectives:

(i) We have to understand behavior of combinational multiplier from module.

(ii) We have to understand the theory and implement the multiplication unit.

(iii) We have to check Multiplying bits and show the sum output.

Equipment list:

(i) 4 x 7408 AND IC

(ii) 3 x 7483 or 74283 4bit Adder IC.

(iii) Trainer Board

(iv) Wires.

Block Diagram:

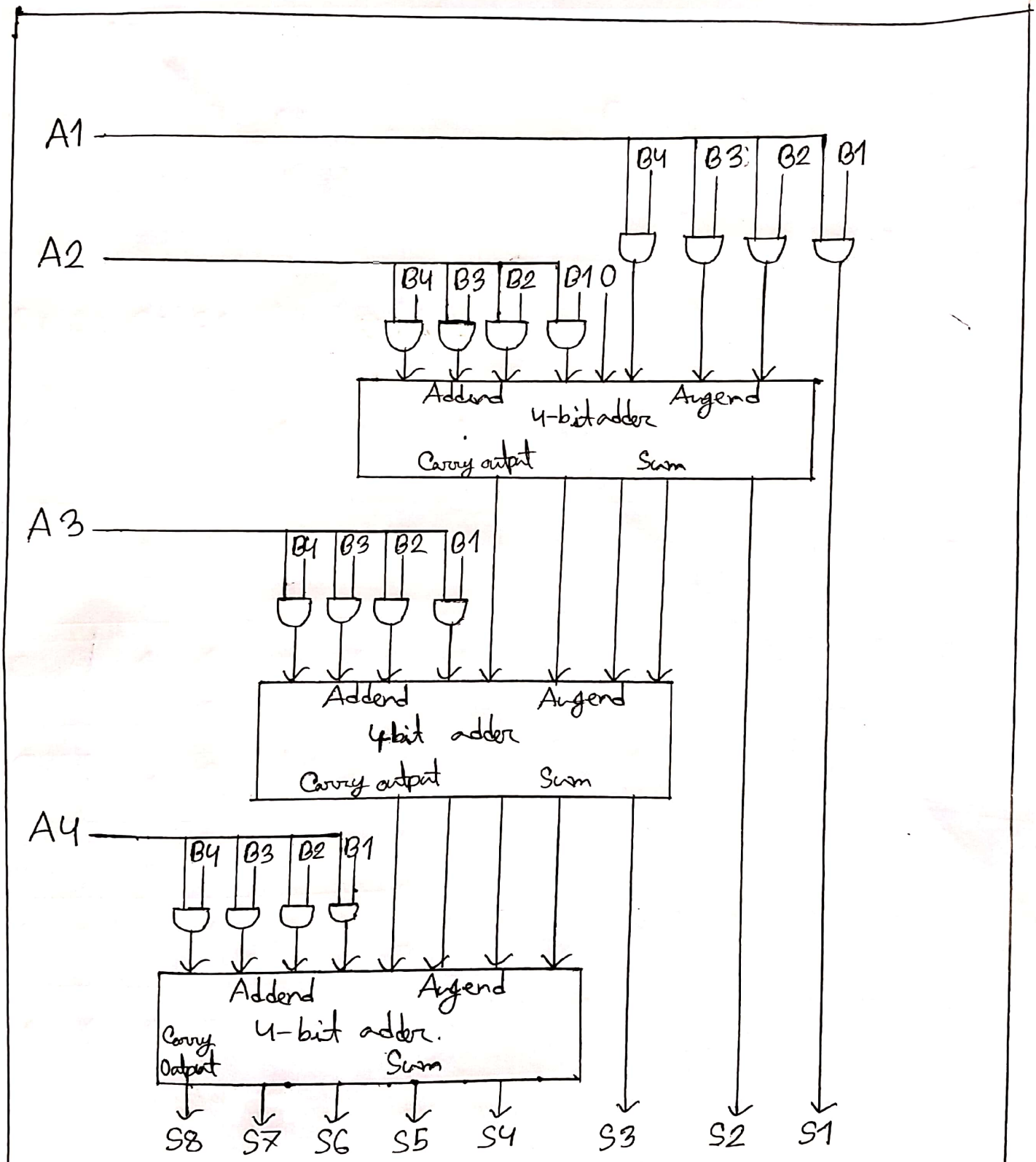
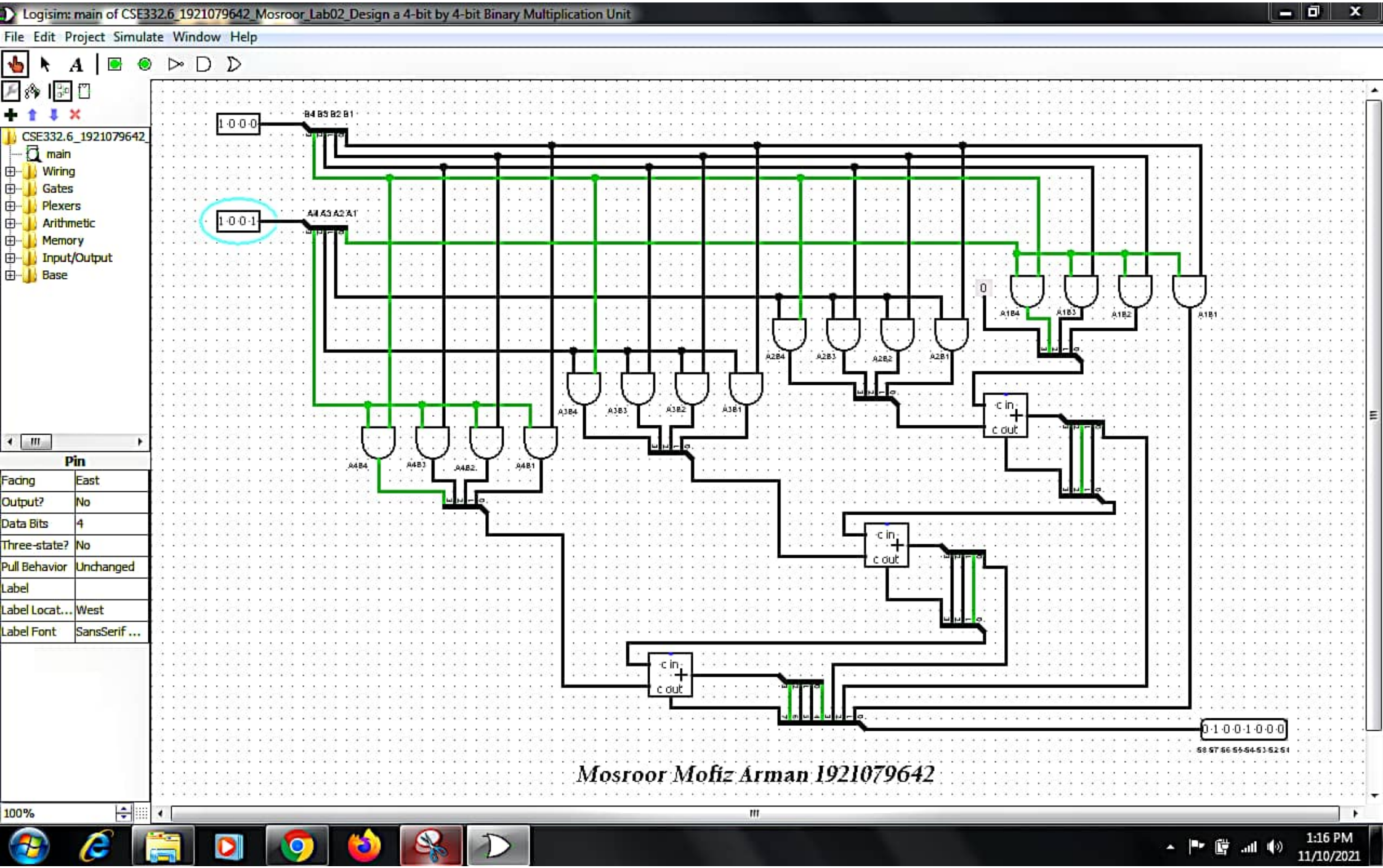


Figure: Block diagram of a 4-bit by 4-bit Binary Multiplier

Table : 2 : Experimental

Multiplicand				Multiplier				Product								Result in Decimal
B4	B3	B2	B1	A4	A3	A2	A1	S8	S7	S6	S5	S4	S3	S2	S0	
1	0	0	0	1	0	0	1	0	1	0	0	1	0	0	0	8×9 = 72
0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	1×2 = 2
0	0	1	1	0	1	1	1	0	0	0	1	0	1	0	1	3×7 = 21
0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	4×8 = 32
0	1	0	1	0	1	1	0	0	0	0	1	1	1	1	0	5×6 = 30
1	0	0	1	0	1	0	0	0	0	1	0	0	1	0	0	9×4 = 36
1	1	1	1	1	0	1	1	1	0	1	0	0	1	0	1	15×11 = 165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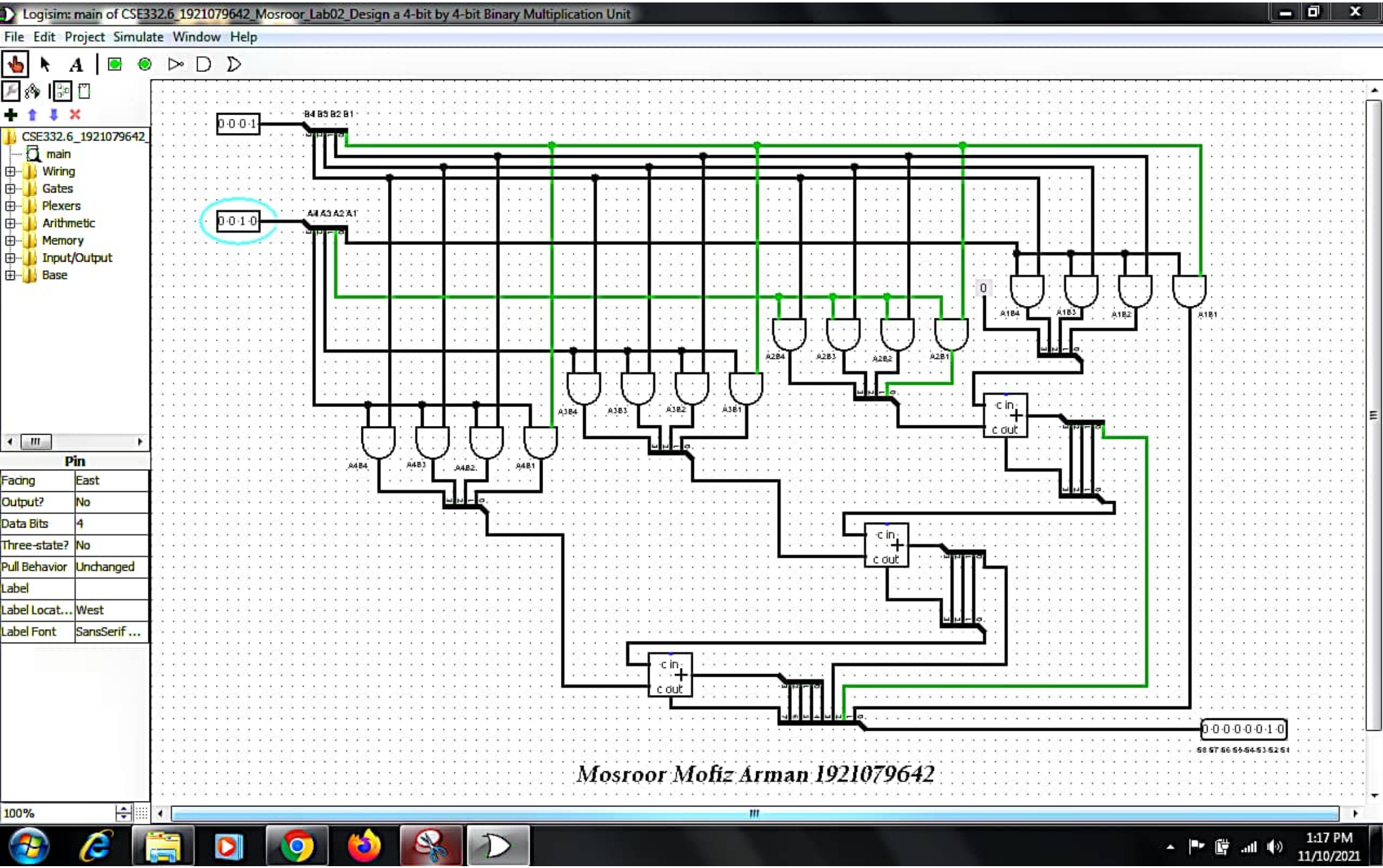
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 4
Three-state? No
Pull Behavior Unchanged
Label
Label Locat... West
Label Font SansSerif ...
100%
1·0·0·0
B4 B3 B2 B1
1·0·0·1
A4 A3 A2 A1
0
c in
c out
0·1·0·0·1·0·0·0
Mosroor Mofiz Arman 1921079642
1:16 PM
11/10/2021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100%
0·0·0·1
B4 B3 B2 B1
0·0·1·0
A4 A3 A2 A1
0
A1B4
A1B3
A1B2
A1B1
A2B4
A2B3
A2B2
A2B1
A3B4
A3B3
A3B2
A3B1
A4B4
A4B3
A4B2
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c in
c out
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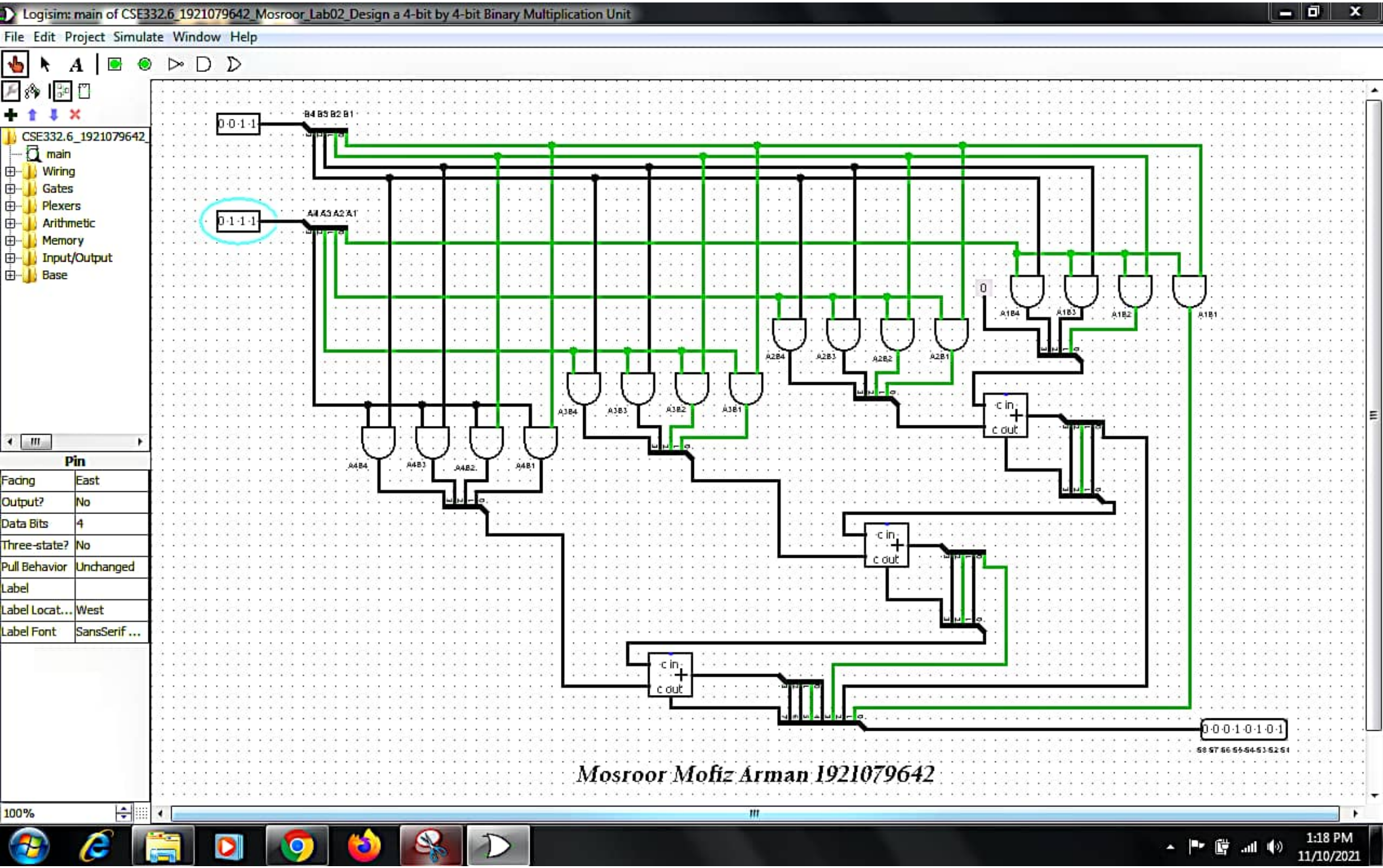
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100%
B4 B3 B2 B1
A4 A3 A2 A1
0·0·1·1
0·1·1·1
c in
c out
0·0·0·1·0·1·0·1
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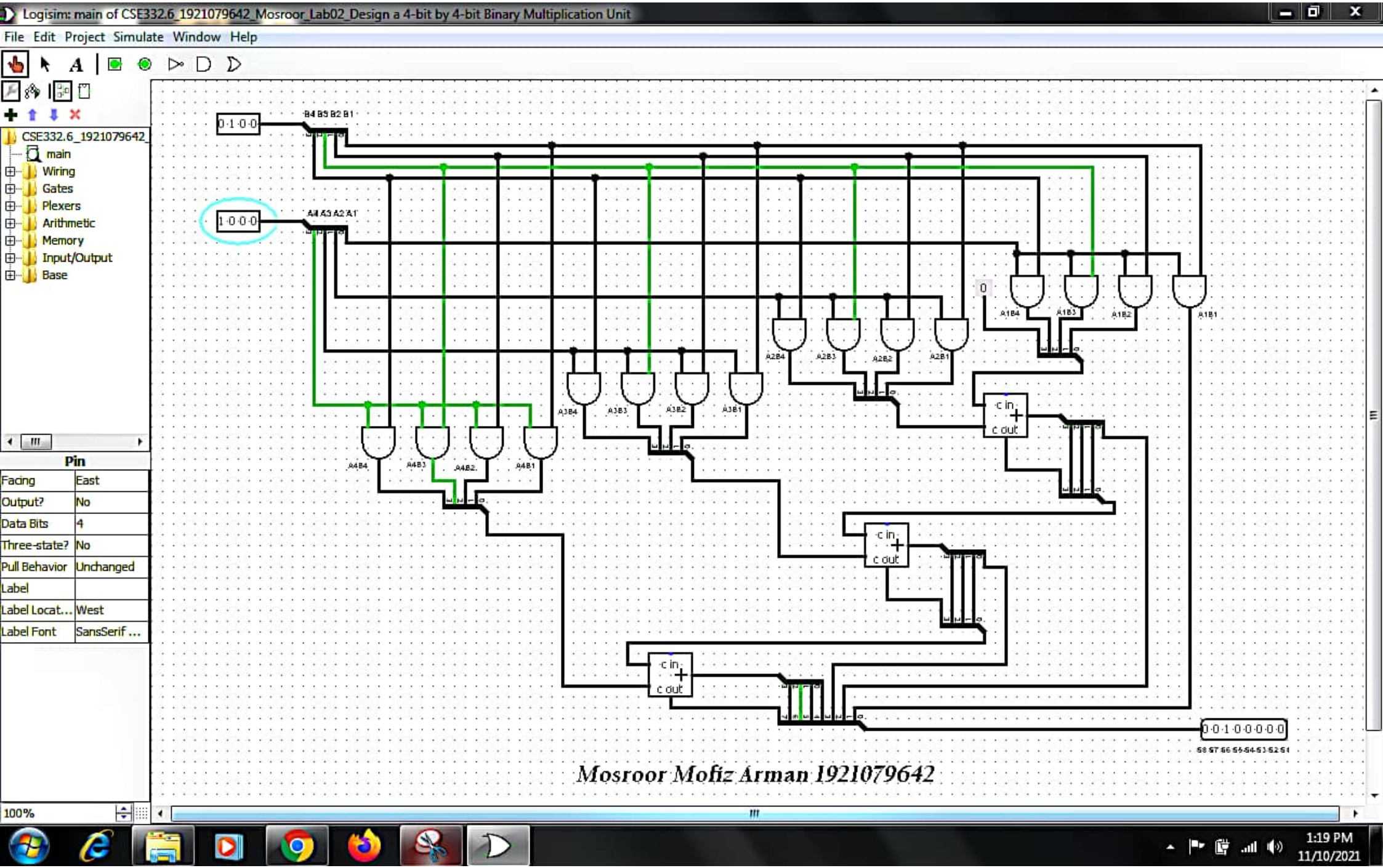
11/10/2021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B4 B3 B2 B1
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A4 A3 A2 A1
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c in
c out
0·0·1·0·0·0·0·0
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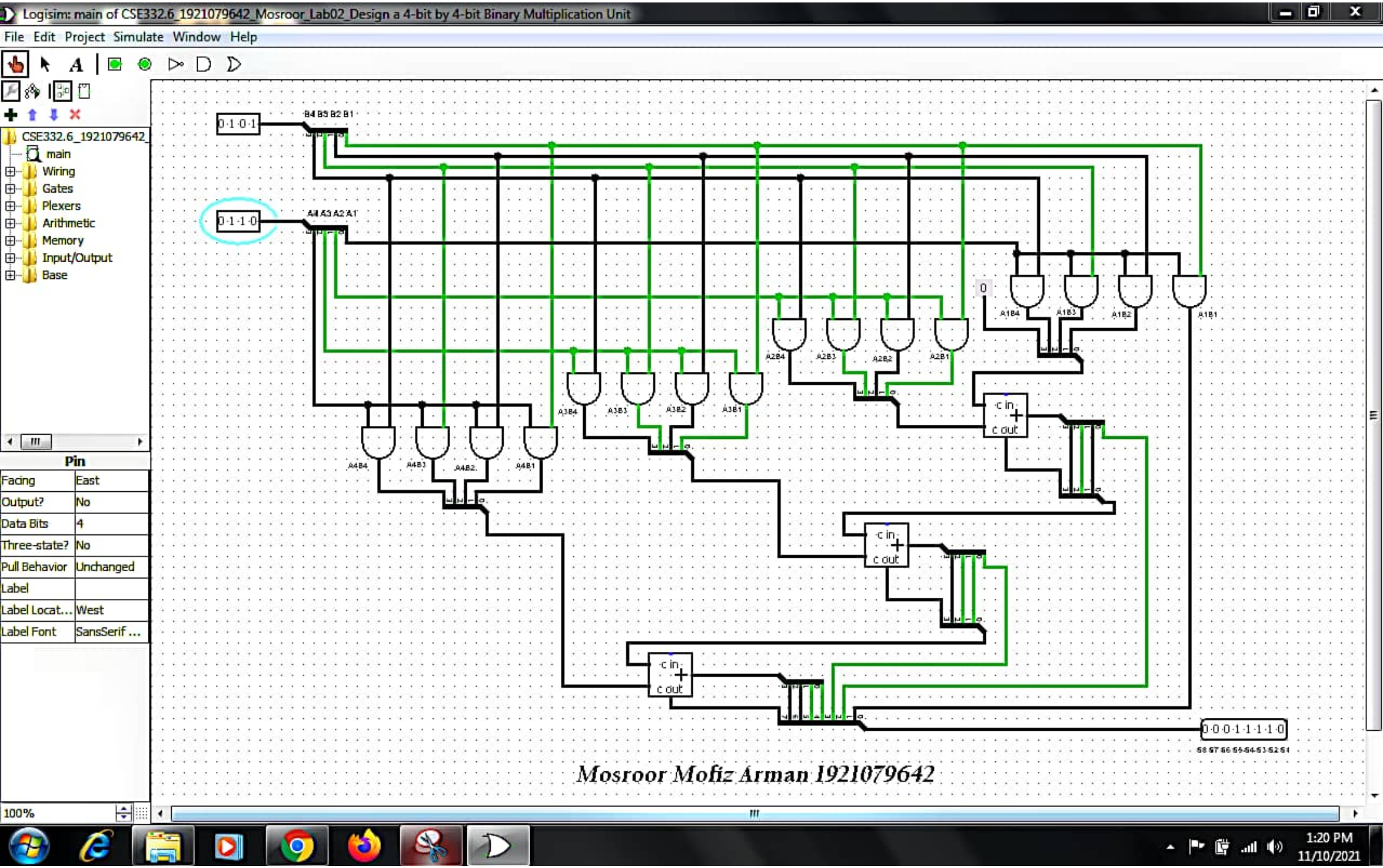
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c out
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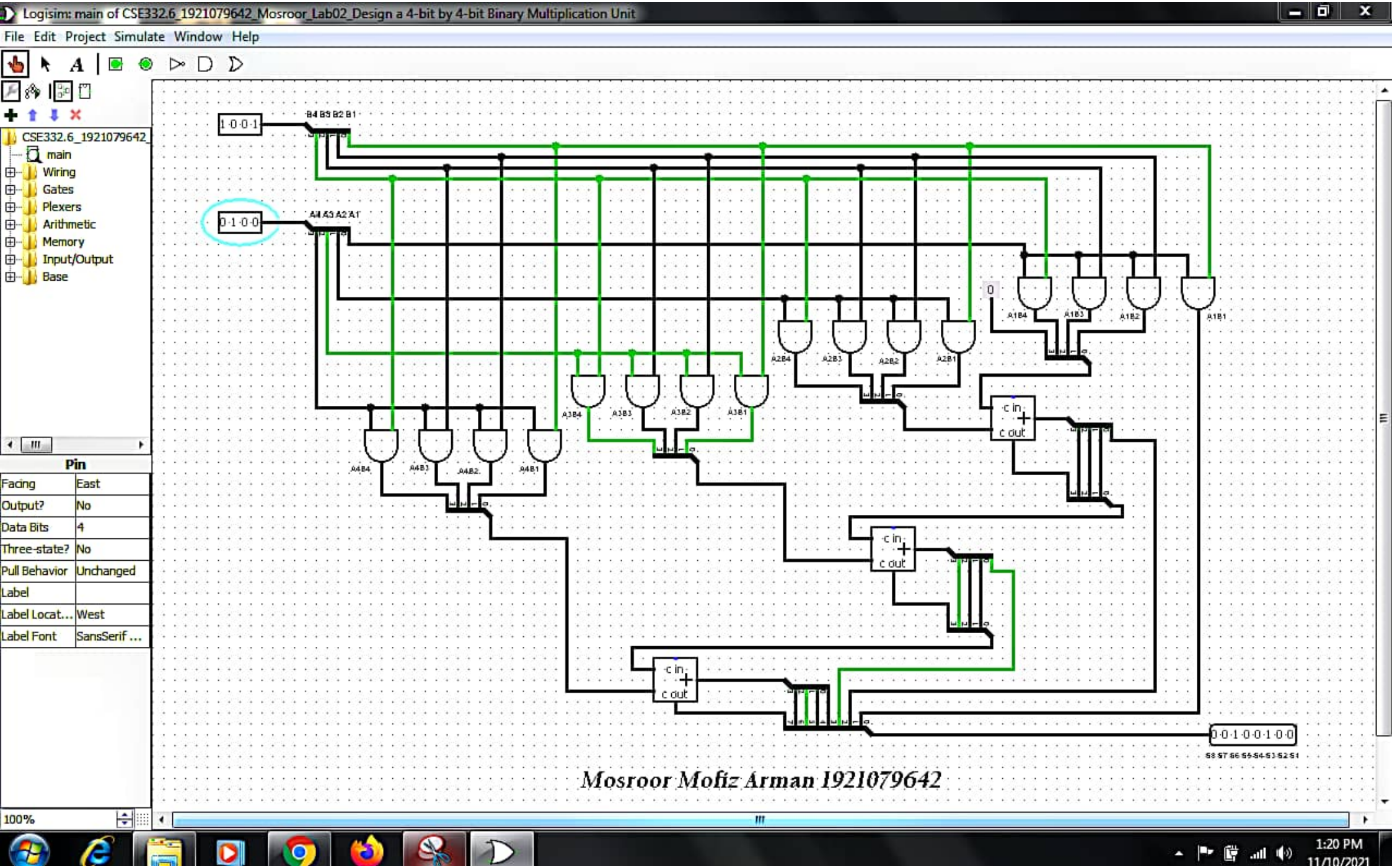
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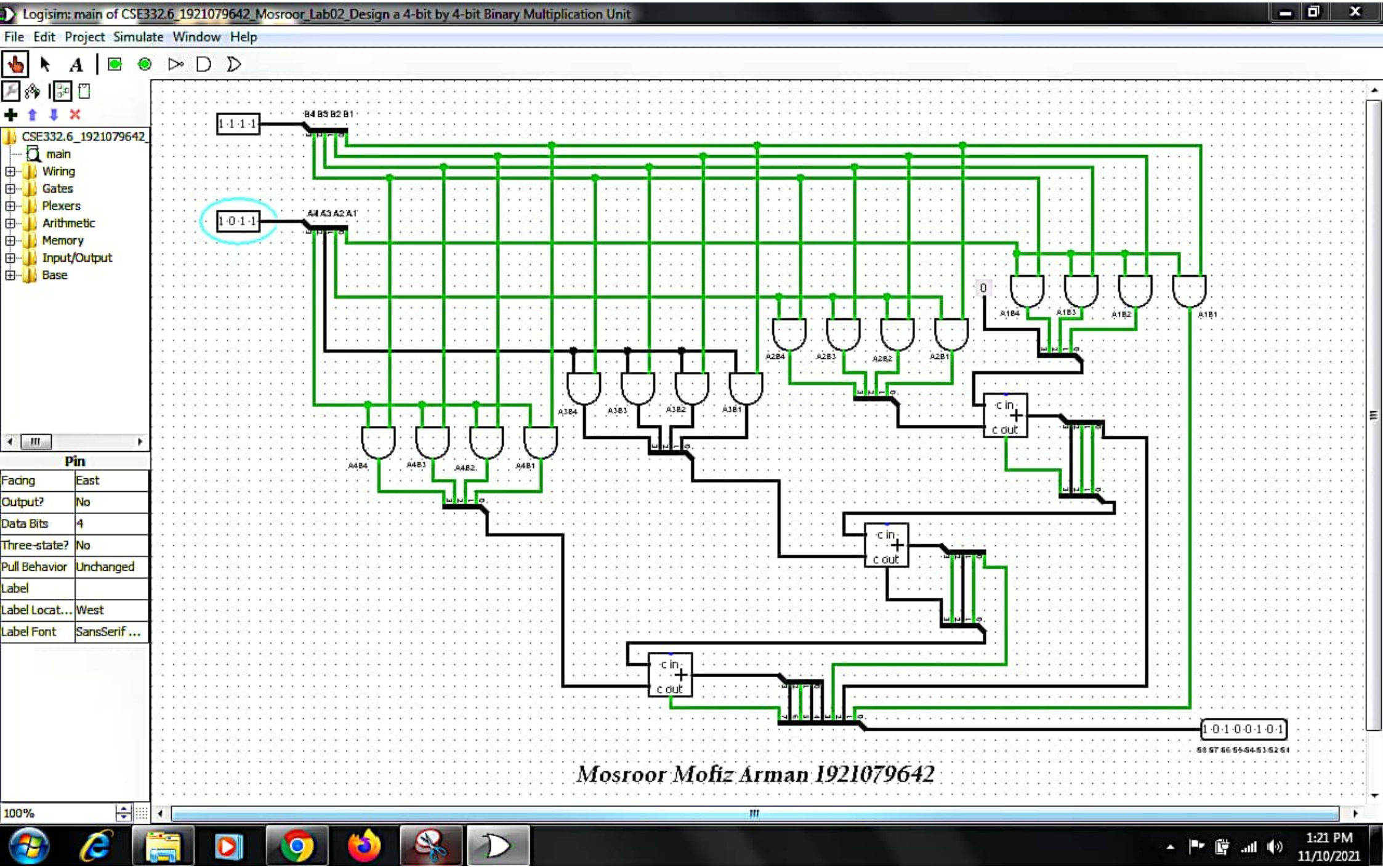
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0
c in
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1·0·1·0·0·1·0·1
Mosroor Mofiz Arman 1921079642
1:21 PM
11/10/2021

Discussion:

In this experiment, we had to design a 4-bit by 4bit Binary Multiplication Unit with combinational multipliers which do multiplication of two unsigned binary numbers. Each bit of the multiplier is multiplied against the multiplicand, the product is aligned according to the position of the bit with in the multiplier and the resulting products are then summed to form the final result. If the multiplier bit is 1, the product is an appropriately shifted copy of the multiplicand, if the multiplier bit is a 0, the product is simply 0. We had used Logisim software and designed the logic part using Logisim software. That's why we didn't have to deal with any hardware instructions. After designing the logic part, we had to check the multiplying bits and the sum outputs from the Logisim software and submit the (.circ) file to our lab instructor on the canvas platform.