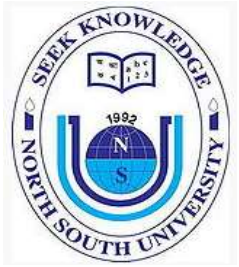


North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	01
Experiment Title:	Design of a 2-bit Logic unit.
Course Code:	**CSE332L**
Course Name:	**Computer Organization & Architecture Lab**
Name & ID:	Mosroor Mofiz Arman, 1921079642
Date of Experiment:	03.11.2021
Date of Submission:	06.11.2021

Objectives:

(i) We have to construct a 2-bit logic unit that is a part of an ALU and this logic unit will have four micro-operations: AND, OR, XOR and NOT operations.

(ii) Logic micro-operations are very useful for manipulating individual bits or portions of a word stored in a register.

(iii) We can change bit values by this operation, delete a group of bits, or insert a new set of bits in a register.

(iv) We have to design a 2-bit logic unit that will give two outputs:

one output for each of the 2 bits.

Equipment list:

(i) Trainer board.

(ii) IC 7404, 7408, 7432, 7486, 74F153.

(iii) Wires for connection.

Block Diagram:

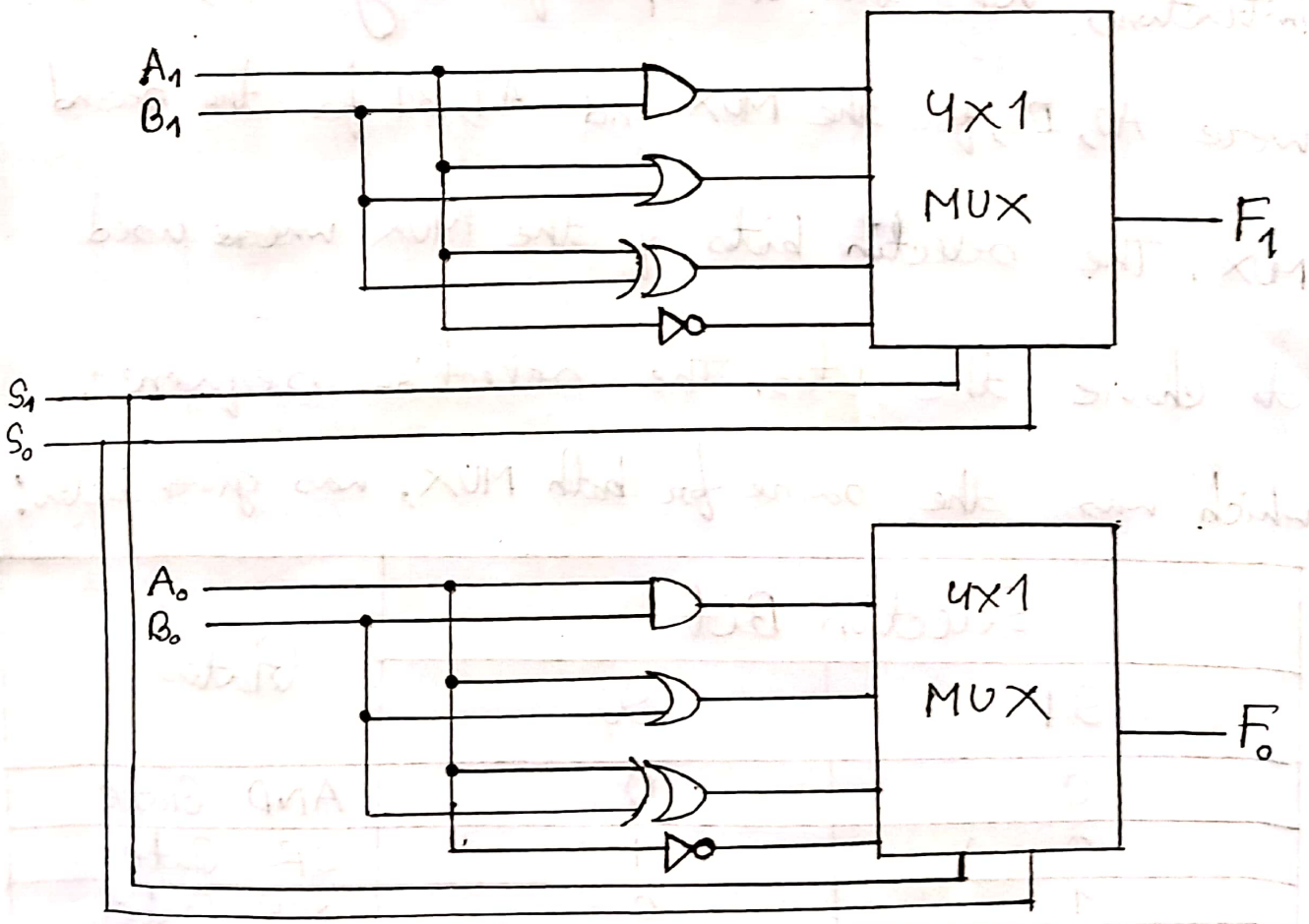


Figure: Block diagram of a 2bit logic unit.

Truth Table :

A1	A0	B1	B0	AND1	AND0	OR1	OR0	XOR1	XOR0	NOT A1	NOT A0
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	1	1	1
0	0	1	0	0	0	1	0	1	0	1	1
0	0	1	1	0	0	1	1	1	1	1	1
0	1	0	0	0	0	0	1	0	1	1	0
0	1	0	1	0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1	1	1	1	0
0	1	1	1	0	1	1	1	1	0	1	0
1	0	0	0	0	0	1	0	1	0	0	1
1	0	0	1	0	0	1	1	1	1	0	1
1	0	1	0	1	0	1	0	0	0	0	1
1	0	1	1	1	0	1	1	0	1	0	1
1	1	0	0	0	0	1	1	1	1	0	0
1	1	0	1	0	1	1	1	1	0	0	0
1	1	1	0	1	0	1	1	0	1	0	0
1	1	1	1	1	1	1	1	0	0	0	0

Table : 2-bit logic unit.

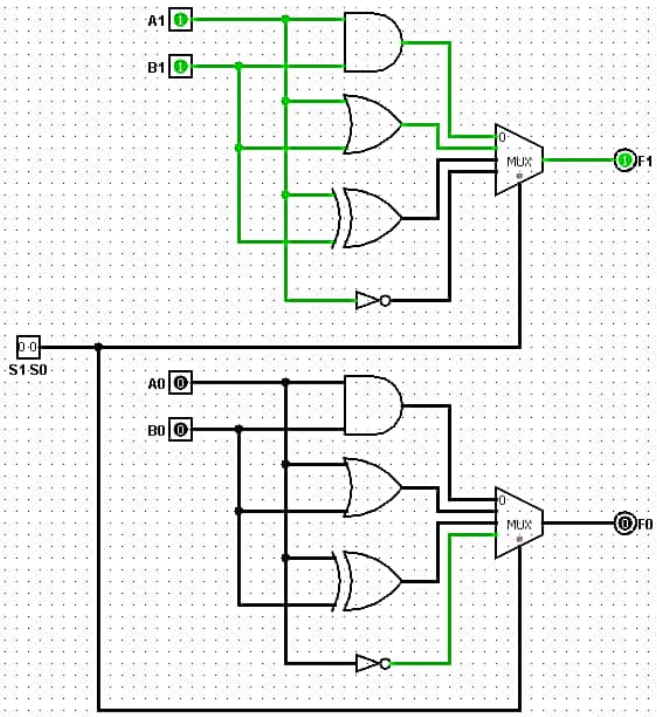
Logisim: main of CSE332.6_1921079642_Mosroor_Lab01_Design of a 2-bit Logic unit

File Edit Project Simulate Window Help

CSE332.6_1921079642_Mosroor_Lab01_Design of a 2-bit Logic unit*
- main
- Wiring
- Gates
- Plexers
- Arithmetic
- Memory
- Input/Output
- Base

Circuit: main

Circuit Name	main
Shared Label	
Shared Label Facing	East
Shared Label Font	SansSerif Plain 12



Mosroor Mofiz Arman
1921079642

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CSE332.6_1921079642_Mosroor_Lab01_Design of a 2-bit Logic unit*
- main
- Wiring
- Gates
- Plexers
- Arithmetic
- Memory
- Input/Output
- Base

Pin	
Facing	East
Output?	No
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	B0
Label Location	West
Label Font	SansSerif Bold 12

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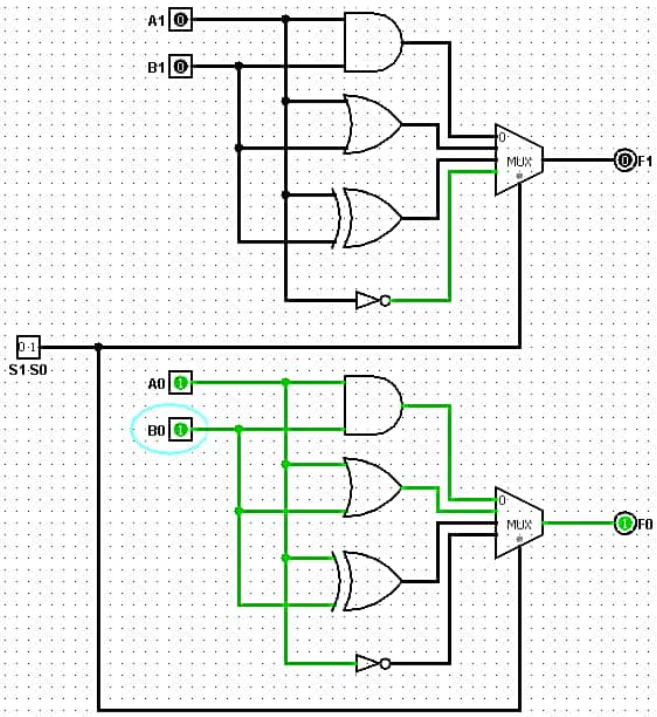

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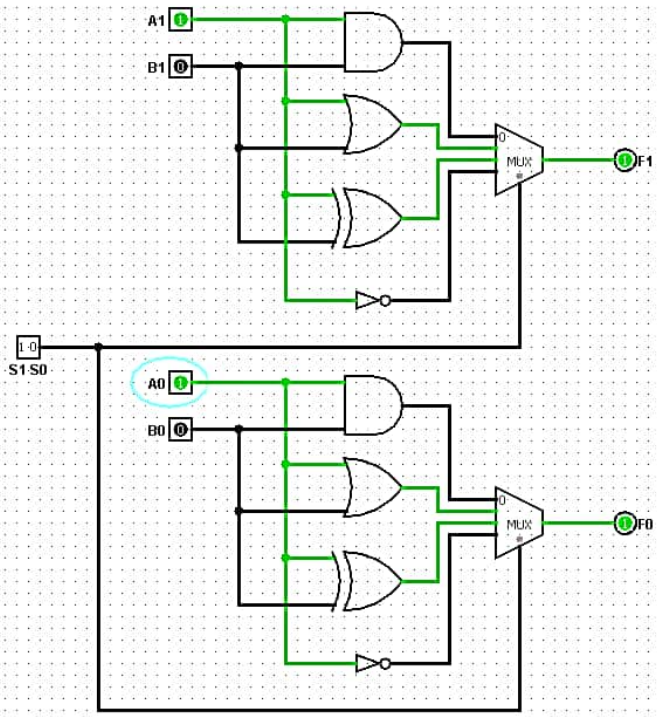
CSE332.6_1921079642_Mosroor_Lab01_Design of a 2-bit Logic unit*
- main
- Wiring
- Gates
- Plexers
- Arithmetic
- Memory
- Input/Output
- Base

Pin	
Facing	East
Output?	No
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	A0
Label Location	West
Label Font	SansSerif Bold 12



Mosroor Mofiz Arman
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Logisim: main of CSE332.6_1921079642_Mosroor_Lab01_Design of a 2-bit Logic unit

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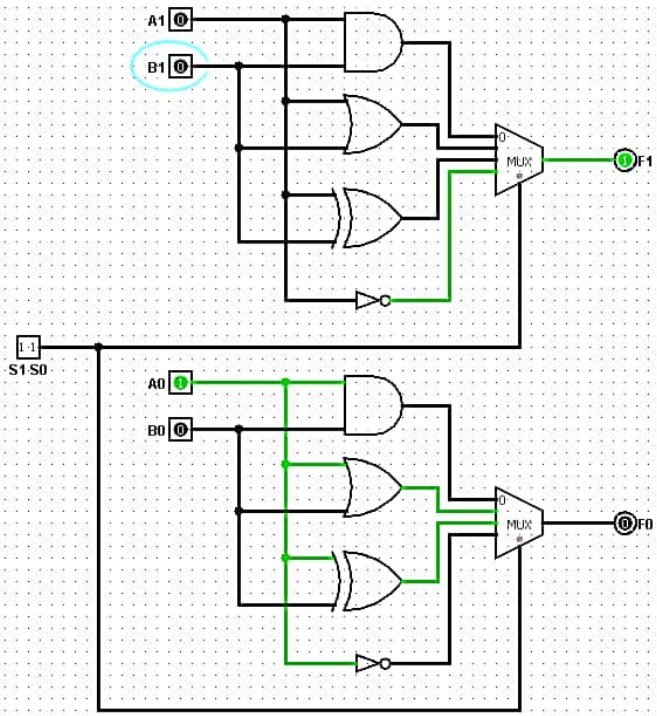
CSE332.6_1921079642_Mosroor_Lab01_Design of a 2-bit Logic unit*
- main
- Wiring
- Gates
- Plexers
- Arithmetic
- Memory
- Input/Output
- Base

Pin	
Facing	East
Output?	No
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	B1
Label Location	West
Label Font	SansSerif Bold 12



Mosroor Mofiz Arman
1921079642

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Discussion:

In this experiment, we had to design a 2bit logic unit with AND, OR, XOR and NOT gate with two different 4x1 MUX. We have used Logisim software and designed the logic part using Logisim software; that's why we didn't have to deal with any hardware instructions. We took two inputs for every MUX, which were A0, B0 for the MUX and A1, B1 for the second MUX. The selection bits of the MUX were used to choose the gates. The selection sequence, which was the same for both MUX, was given below:

Selection Bit		Gates
S1	S0	
0	0	AND Gate
0	1	OR Gate
1	0	XOR Gate
1	1	NOT Gate