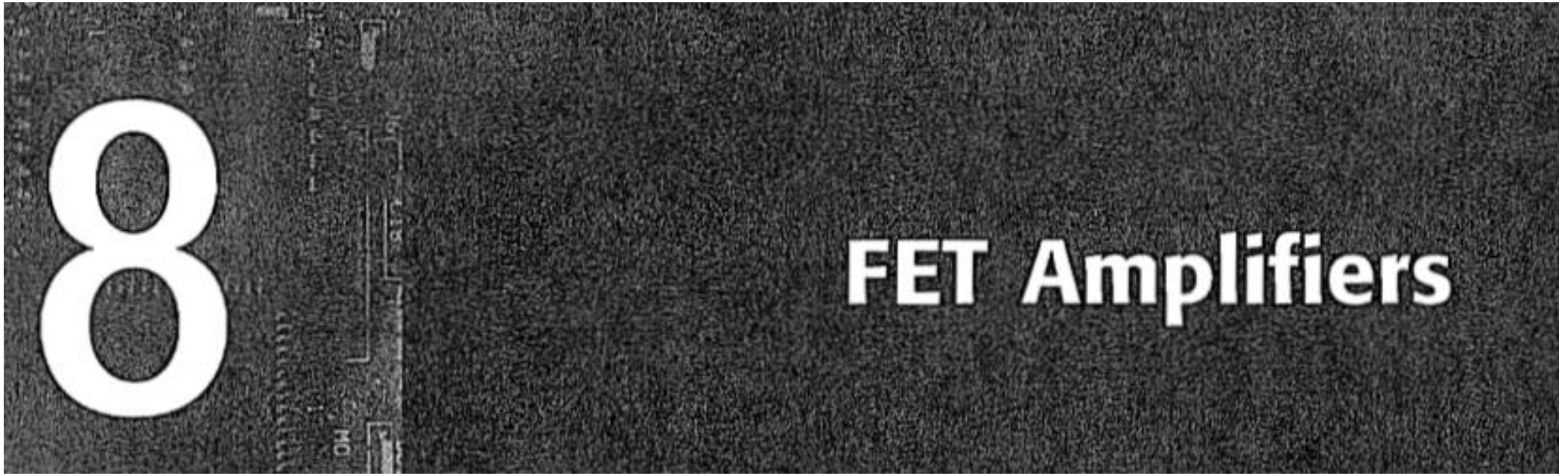


8 FET Amplifiers

CHAPTER OUTLINE

8.1 INTRODUCTION

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight. JFETs, depletion MOSFETs, and MESFETs can be used to design amplifiers having similar voltage gains. The depletion MOSFET (MESFET) circuit, however, has a much higher input impedance than a similar JFET configuration.

Whereas a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. Whereas the BJT has an amplification factor, β (beta), the FET has a transconductance factor, g_m.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications. Table 8.1 in Section 8.13

Although the common-source configuration is the most popular one, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity. Whereas the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

8.2 FET SMALL-SIGNAL MODEL

The ac analysis of an FET configuration requires that a small-signal ac model for the FET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of an FET.

Recall from Chapter 7 that a dc gate-to-source voltage controls the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$. The *change* in collector current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\boxed{\Delta I_D = g_m \Delta V_{GS}} \tag{8.1}$$

The prefix *trans-* in the terminology applied to g_m reveals that it establishes a relationship between an output and an input quantity. The root word *conductance* was chosen because g_m is determined by a voltage-to-current ratio similar to the ratio that defines the conductance of a resistor, $G = 1/R = I/V$.

Solving for g_m in Eq. (8.1), we have

$$\boxed{g_m = \frac{\Delta I_D}{\Delta V_{GS}}} \tag{8.2}$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

and

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}} \tag{8.5}$$

where the added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$ V. Equation (8.4) then becomes

$$\boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{8.6}$$

FET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the FET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 8.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

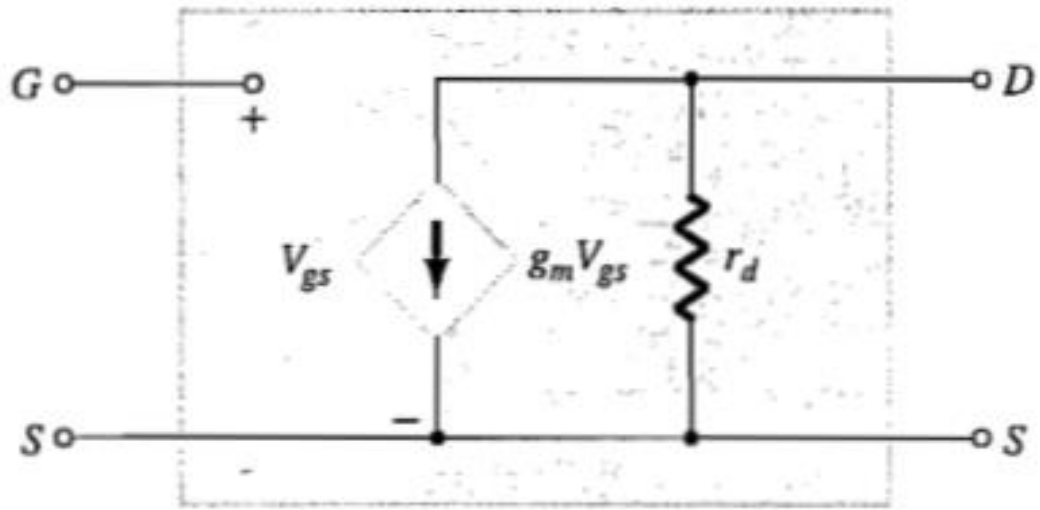


FIG. 8.8
FET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate-to-source voltage is now represented by V_{gs} (lower-case subscripts) to distinguish it from dc levels. In addition, note that the source is common to both input and output circuits, whereas the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.

In situations where r_d is ignored (assumed sufficiently large in relation to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m—clearly a voltage-controlled device.

8.3 JFET FIXED-BIAS CONFIGURATION

Now that the FET equivalent circuit has been defined, a number of fundamental FET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i, Z_o, and A_v for each configuration.

The *fixed-bias* configuration of Fig. 8.10 includes the coupling capacitors C_1 and C_2, which isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

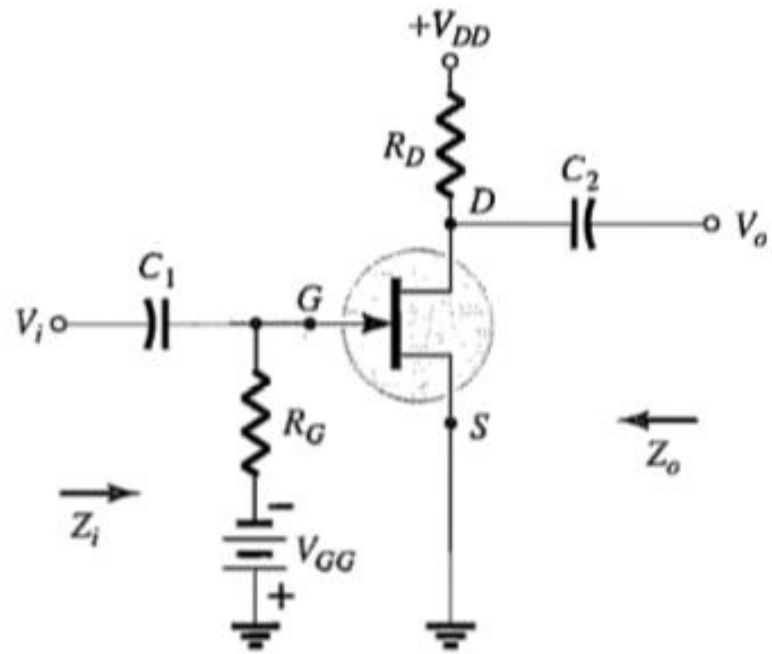
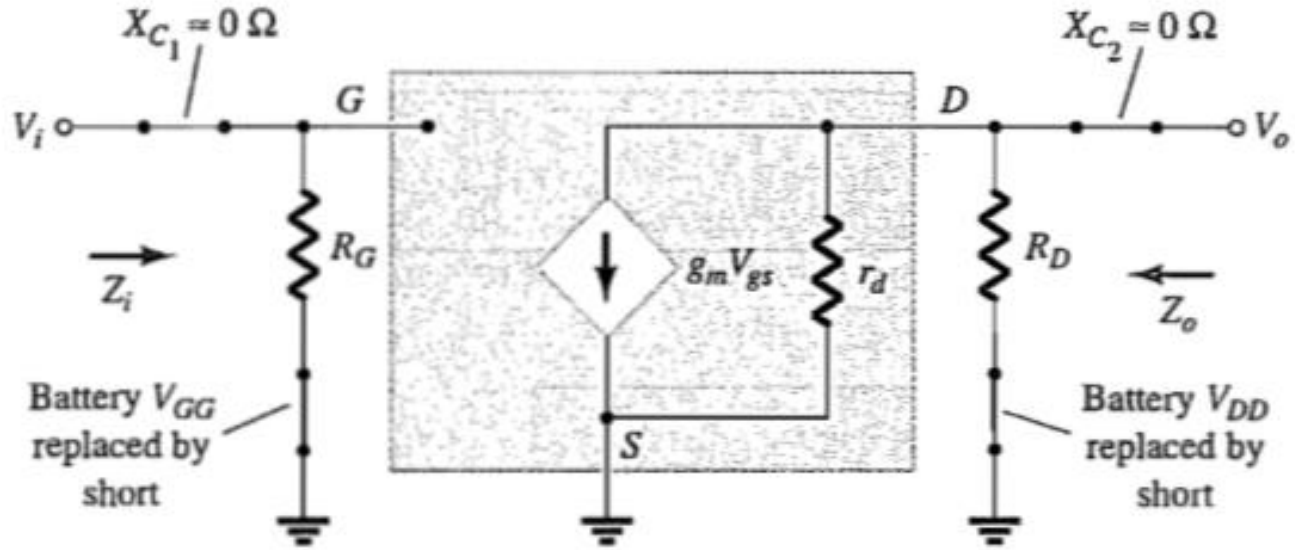
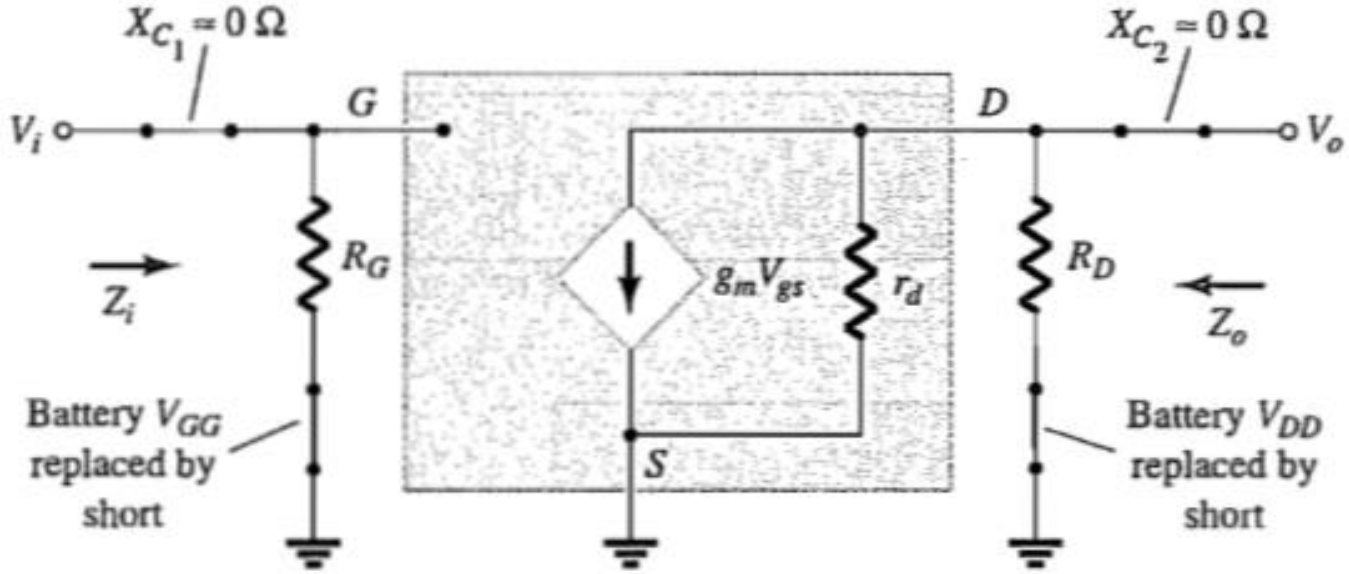


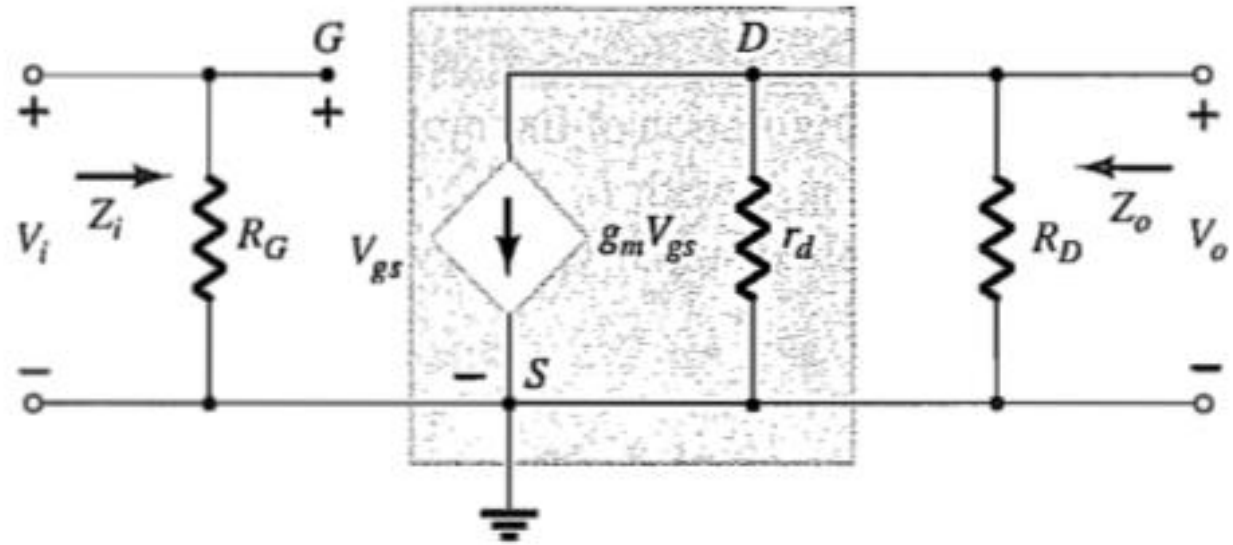
FIG. 8.10
JFET fixed-bias configuration.

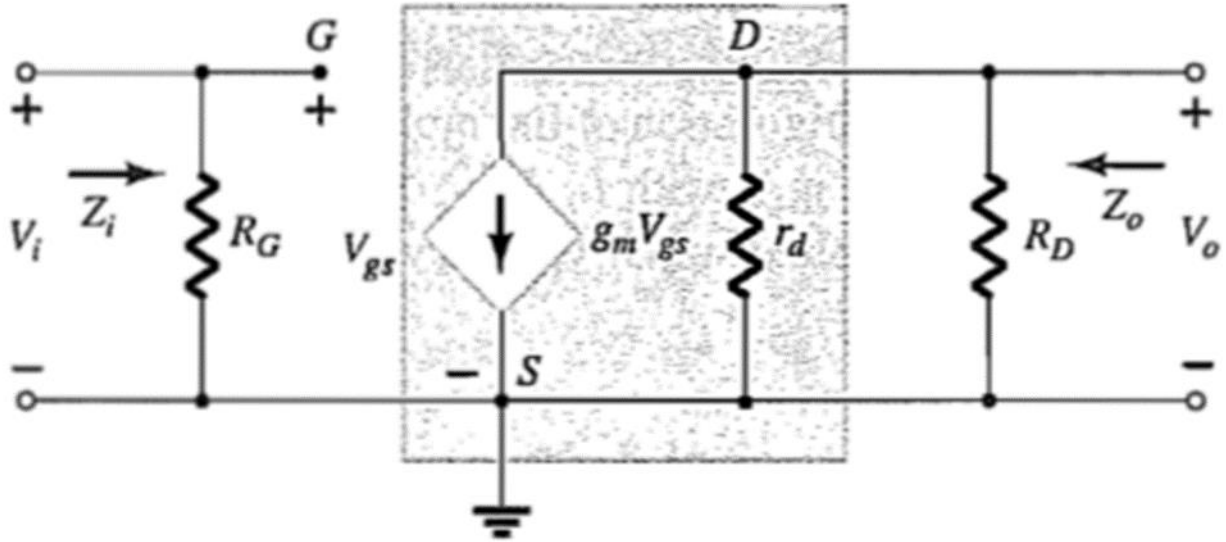
Once the levels of g_m and r_d are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 8.11. Note that both capacitors have the short-circuit equivalent because the reactance $X_C = 1/(2\pi fC)$ is sufficiently small compared to other impedance levels of the network, and the dc batteries V_{GG} and V_{DD} are set to 0 V by a short-circuit equivalent.

The network of Fig. 8.11 is then carefully redrawn as shown in Fig. 8.12. Note the defined polarity of V_{gs}, which defines the direction of $g_m V_{gs}$. If V_{gs} is negative, the direction of the current source reverses. The applied signal is represented by V_i and the output signal across R_D by V_o.




$X_{C_1} \simeq 0\,\Omega$
$X_{C_2} \simeq 0\,\Omega$
V_i
G
D
V_o
R_G
R_D
Z_i
Z_o
$g_m V_{gs}$
r_d
S
Battery V_{GG} replaced by short
Battery V_{DD} replaced by short


G
D
+
+
+
V_i
Z_i
R_G
V_{gs}
$g_m V_{gs}$
r_d
R_D
Z_o
V_o
−
S
−
−



Z_i Figure 8.12 clearly reveals that

$$\boxed{Z_i = R_G}$$

because of the open-circuit equivalence at the input terminals of the JFET. $\boxed{Z_o = R_D \| r_d}$

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{8.15}$$

A_v Solving for V_o in Fig. 8.12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $$V_{gs} = V_i$$

and $$V_o = -g_m V_i(r_d \| R_D)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{8.16}$$

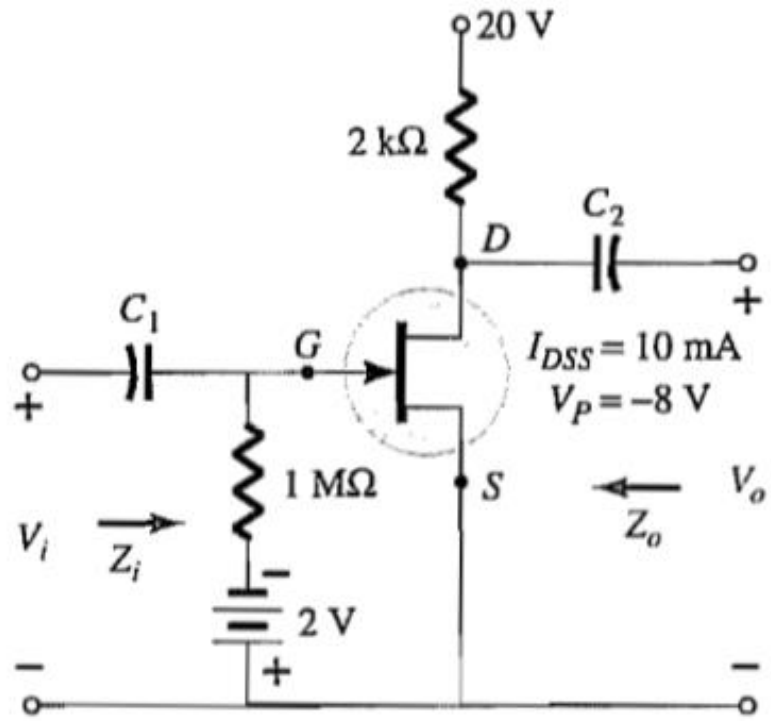
If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m R_D}_{r_d \geq 10R_D} \tag{8.17}$$

Phase Relationship The negative sign in the resulting equation for A_v clearly reveals a phase shift of 180° between input and output voltages.

EXAMPLE 8.7 The fixed-bias configuration of Example 7.1 had an operating point defined by $V_{GS_Q} = -2\,\text{V}$ and $I_{D_Q} = 5.625\,\text{mA}$, with $I_{DSS} = 10\,\text{mA}$ and $V_P = -8\,\text{V}$. The network is redrawn as Fig. 8.14 with an applied signal V_i. The value of y_{os} is provided as $40\,\mu\text{S}$.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o.
e. Determine the voltage gain A_v.
f. Determine A_v ignoring the effects of r_d.



Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\,\text{mA})}{8\,\text{V}} = 2.5\,\text{mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\,\text{mS}\left(1 - \frac{(-2\,\text{V})}{(-8\,\text{V})}\right) = \mathbf{1.88\,mS}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{40\,\mu S} = \mathbf{25\,k\Omega}$$

c. $$Z_i = R_G = \mathbf{1\,M\Omega}$$

d. $$Z_o = R_D \| r_d = 2\,\text{k}\Omega \| 25\,\text{k}\Omega = \mathbf{1.85\,k\Omega}$$

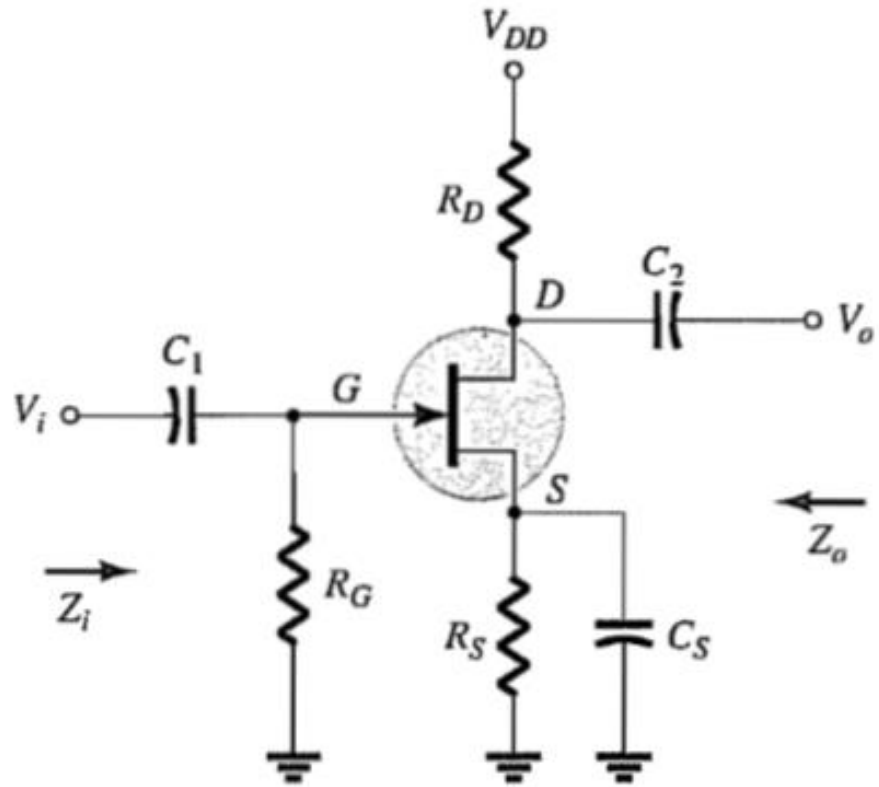
e. $$A_v = -g_m(R_D \| r_d) = -(1.88\,\text{mS})(1.85\,\text{k}\Omega)$$
$$= \mathbf{-3.48}$$

f. $$A_v = -g_m R_D = -(1.88\,\text{mS})(2\,\text{k}\Omega) = \mathbf{-3.76}$$

8.4 JFET SELF-BIAS CONFIGURATION

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 8.15 requires only one dc supply to establish the desired operating point.



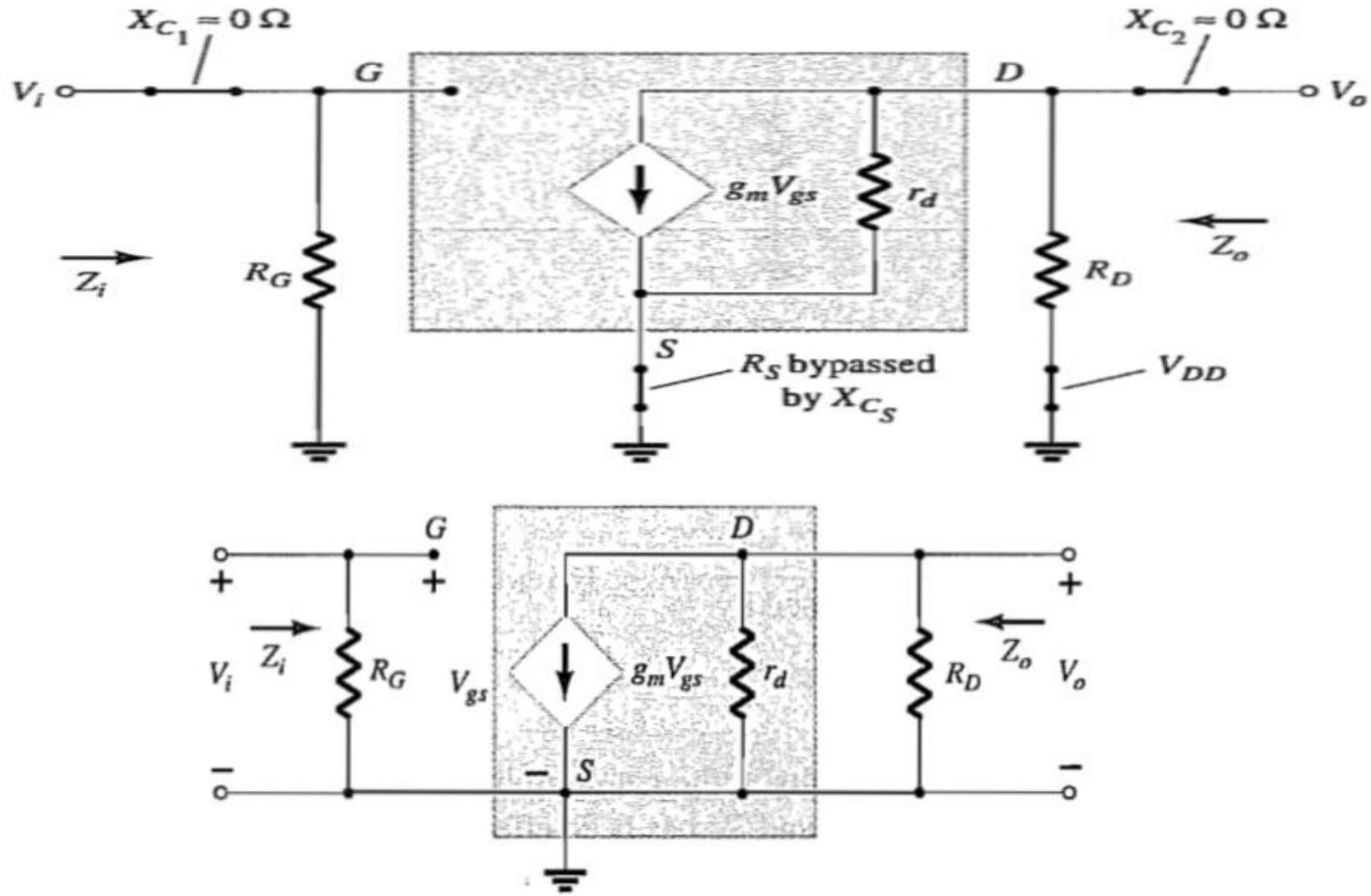


FIG. 8.17

Redrawn network of Fig. 8.16.

Z_i

$$\boxed{Z_i = R_G} \tag{8.18}$$

Z_o

$$\boxed{Z_o = r_d \| R_D} \tag{8.19}$$

If $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{8.20}$$

A_v

$$\boxed{A_v = -g_m(r_d \| R_D)} \tag{8.21}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = -g_m R_D}_{r_d \geq 10R_D} \tag{8.22}$$

Phase Relationship The negative sign in the solutions for A_v again indicates a phase shift of 180° between V_i and V_o.

Unbypassed R_S

If C_S is removed from Fig 8.15, the resistor R_S will be part of the ac equivalent circuit as shown in Fig. 8.18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of Z_i, Z_o, and A_v, one must be very careful with notation and defined polarities and direction. Initially, the resistance r_d will be left out of the analysis to form a basis for comparison.

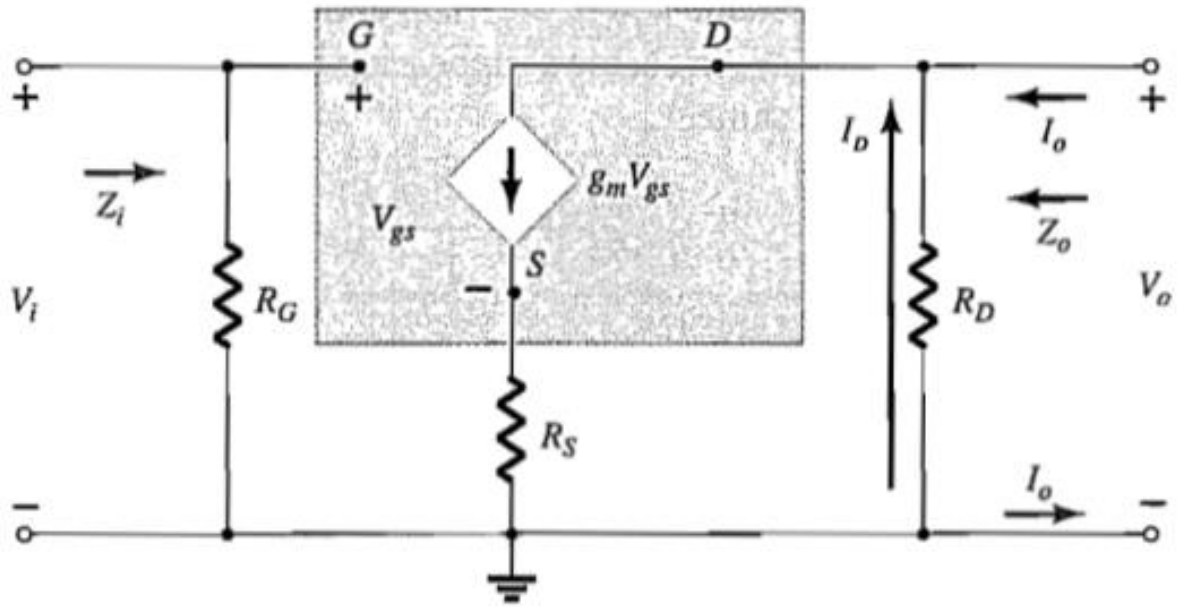


FIG. 8.18

Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

Z_i Due to the open-circuit condition between the gate and the output network, the input remains the following:

$$\boxed{Z_i = R_G} \tag{8.23}$$

Z_o The output impedance is defined by

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0} \qquad \boxed{Z_o = R_D}_{r_d \geq 10R_D}$$

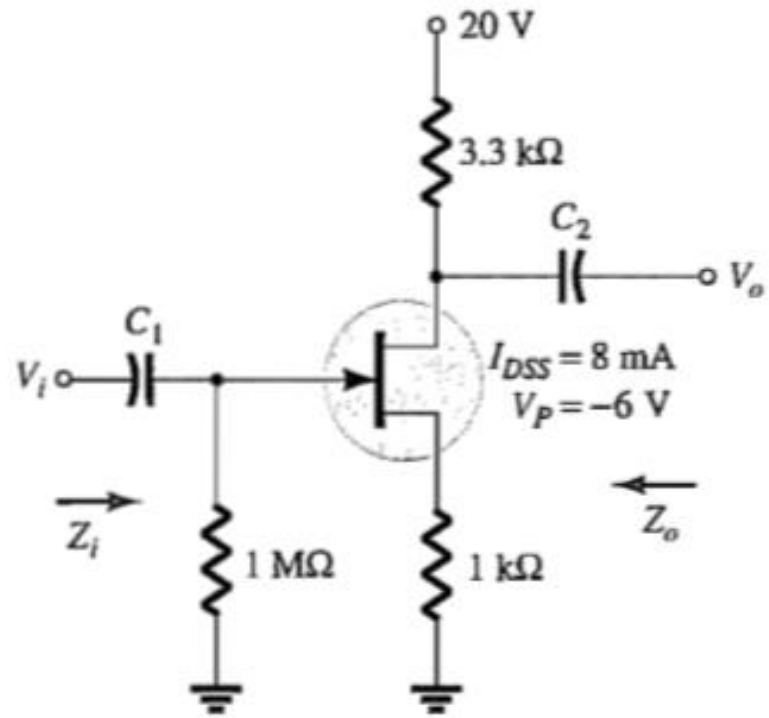
Again, if $r_d \geq 10(R_D + R_S)$,

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S}}_{r_d \geq 10(R_D + R_S)} \tag{8.27}$$

Phase Relationship The negative sign in Eq. (8.26) again reveals that a 180° phase shift will exist between V_i and V_o.

EXAMPLE 8.8 The self-bias configuration of Example 7.2 has an operating point defined by $V_{GS_Q} = -2.6\,\text{V}$ and $I_{D_Q} = 2.6\,\text{mA}$, with $I_{DSS} = 8\,\text{mA}$ and $V_P = -6\,\text{V}$. The network is redrawn as Fig. 8.20 with an applied signal V_i. The value of y_{os} is given as $20\,\mu\text{S}$.

a. Determine g_m.
b. Find r_d.
c. Find Z_i.
d. Calculate Z_o with and without the effects of r_d. Compare the results.
e. Calculate A_v with and without the effects of r_d. Compare the results.



Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\,\text{mA})}{6\,\text{V}} = 2.67\,\text{mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\,\text{mS}\left(1 - \frac{(-2.6\,\text{V})}{(-6\,\text{V})}\right) = \mathbf{1.51\,mS}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{20\,\mu S} = \mathbf{50\,k\Omega}$$

c. $Z_i = R_G = \mathbf{1\,M\Omega}$

d. With r_d,

$$r_d = 50\,\text{k}\Omega > 10R_D = 33\,\text{k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\,k\Omega}$$

If $r_d = \infty\Omega$,

$$Z_o = R_D = \mathbf{3.3\,k\Omega}$$

Without r_d,

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\,\text{mS})(3.3\,\text{k}\Omega)}{1 + (1.51\,\text{mS})(1\,\text{k}\Omega)} = \mathbf{-1.98}$$

8.5 JFET VOLTAGE-DIVIDER CONFIGURATION

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 8.22.

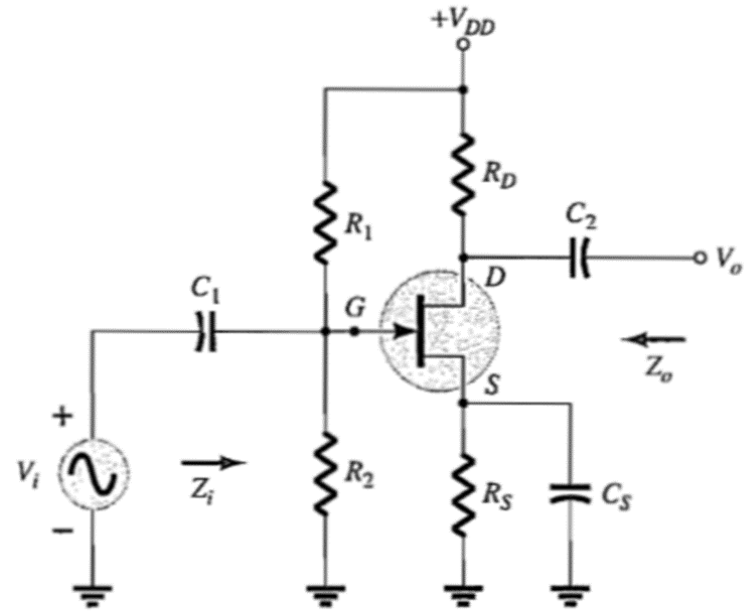


FIG. 8.22
JFET voltage-divider configuration.

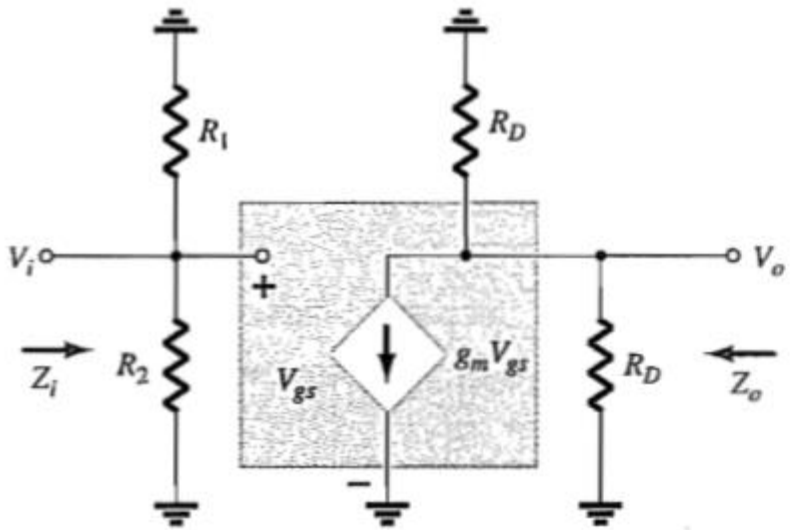


FIG. 8.23
Network of Fig. 8.22 under ac conditions.

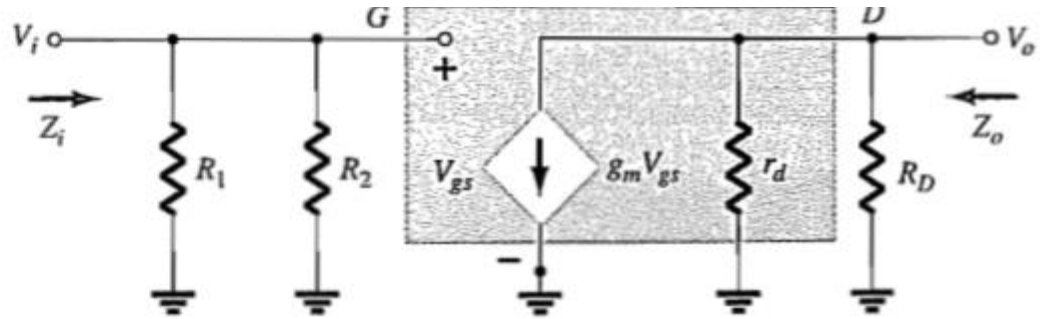


FIG. 8.24
Redrawn network of Fig. 8.23.

Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.23. Replacing the dc supply V_{DD} by a short-circuit equivalent has grounded one end of R_1 and R_D. Since each network has a common ground, R_1 can be brought down in parallel with R_2 as shown in Fig. 8.24. R_D can also be brought down to ground, but in the output circuit across r_d. The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

Z_i R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET, resulting in

$$\boxed{Z_i = R_1 \| R_2} \tag{8.28}$$

Z_o Setting $V_i = 0\,\text{V}$ sets V_{gs} and $g_m V_{gs}$ to zero, and

$$\boxed{Z_o = r_d \| R_D} \tag{8.29}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{8.30}$$

A_v

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{8.31}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}_{r_d \geq 10R_D} \tag{8.32}$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.

8.8 DEPLETION-TYPE MOSFETs

The fact that Shockley's equation is also applicable to depletion-type MOSFETs (D-MOSFETs) results in the same equation for g_m. In fact, the ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs, as shown in Fig. 8.34.

The only difference offered by D-MOSFETs is that V_{GS_Q} can be positive for n-channel devices and negative for p-channel units. The result is that g_m can be greater than g_{m0}, as demonstrated by the example to follow. The range of r_d is very similar to that encountered for JFETs.

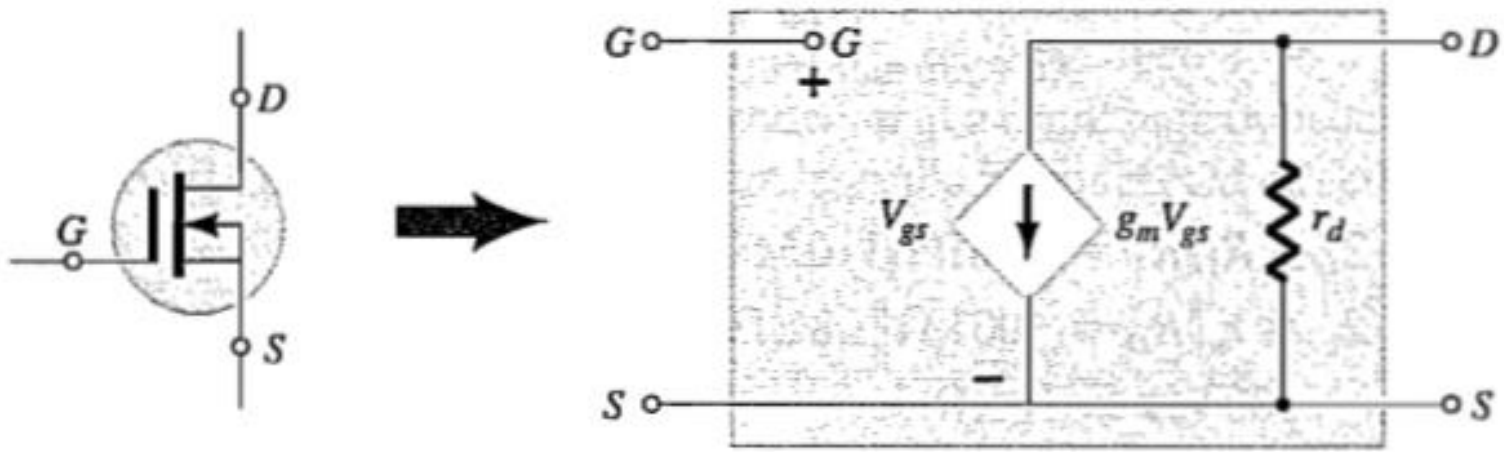
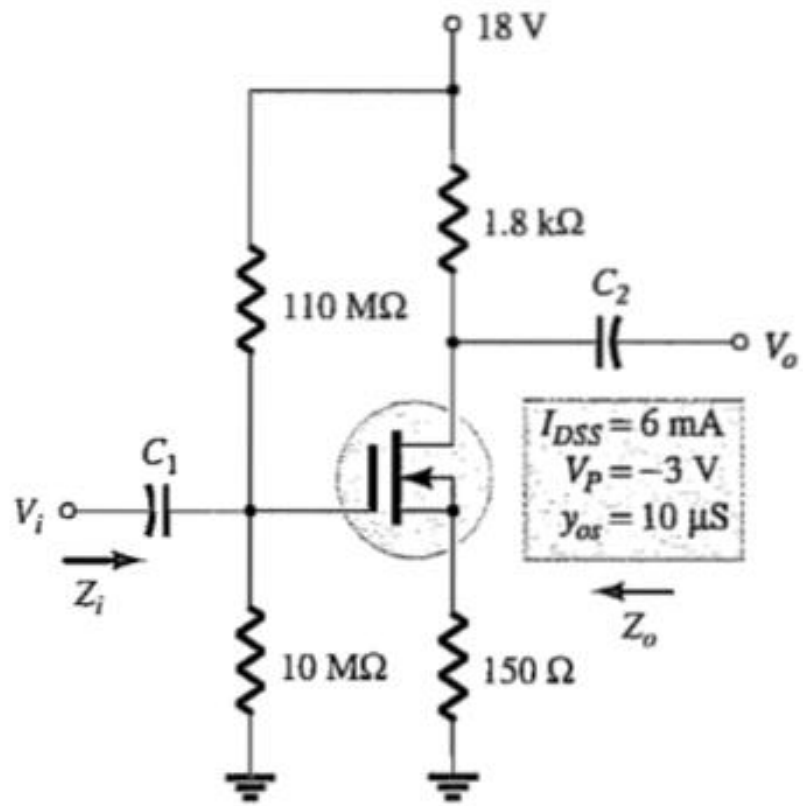


FIG. 8.34
D-MOSFET ac equivalent model.

EXAMPLE 8.11 The network of Fig. 8.35 was analyzed as Example 7.8, resulting in $V_{GS_Q} = 0.35\,\text{V}$ and $I_{D_Q} = 7.6\,\text{mA}$.

a. Determine g_m and compare to g_{m0}.
b. Find r_d.
c. Sketch the ac equivalent network for Fig. 8.35.
d. Find Z_i.
e. Calculate Z_o.
f. Find A_v.



Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(6\text{ mA})}{3\text{ V}} = 4\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{(+0.35\text{ V})}{(-3\text{ V})}\right) = 4\text{ mS}(1 + 0.117) = \mathbf{4.47\text{ mS}}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{10\,\mu\text{S}} = \mathbf{100\text{ k}\Omega}$

c. See Fig. 8.36. Note the similarities with the network of Fig. 8.24. Equations (8.28) through (8.32) are therefore applicable.

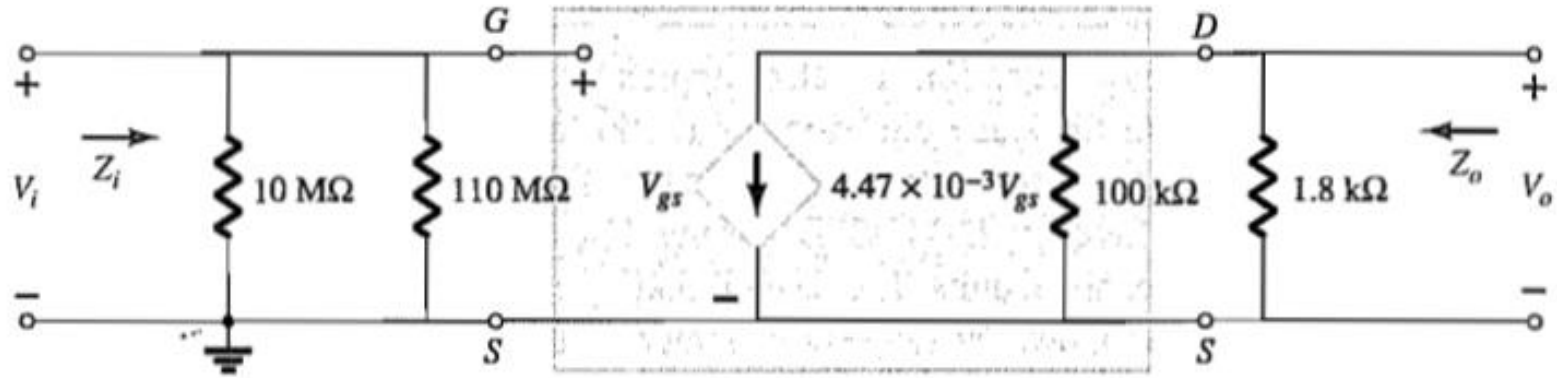


FIG. 8.36
AC equivalent circuit for Fig. 8.35.

d. Eq. (8.28): $Z_i = R_1 \| R_2 = 10\text{ M}\Omega \| 110\text{ M}\Omega = \mathbf{9.17\text{ M}\Omega}$

e. Eq. (8.29): $Z_o = r_d \| R_D = 100\text{ k}\Omega \| 1.8\text{ k}\Omega = \mathbf{1.77\text{ k}\Omega} \cong R_D = \mathbf{1.8\text{ k}\Omega}$

f. $r_d \geq 10R_D \rightarrow 100\text{ k}\Omega \geq 18\text{ k}\Omega$

Eq. (8.32): $A_v = -g_m R_D = -(4.47\text{ mS})(1.8\text{ k}\Omega) = \mathbf{8.05}$

Thank You!