# Field-Effect Transistors

## Topic 6 (Chapter 6)

# Basic Difference Between BJT and FET

- The BJT is a current-controlled device
- The FET is a voltage-controlled device.

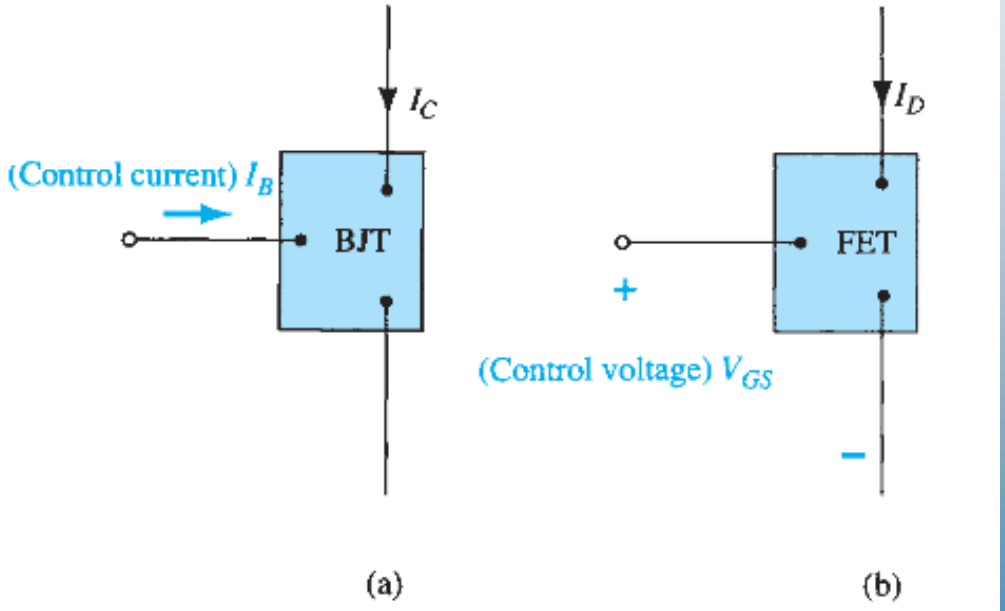



**FIG. 6.1**
*(a) Current-controlled and (b) voltage-controlled amplifiers.*

# FETs vs. BJTs

**Similarities:**

Amplifiers
Switching devices
Impedance matching circuits

**Differences:**

FETs are voltage controlled devices. BJTs are current controlled devices.

FETs have higher input impedance. BJTs have higher gain.

FETs are less sensitive to temperature variations and are better suited for integrated circuits

# FET Types

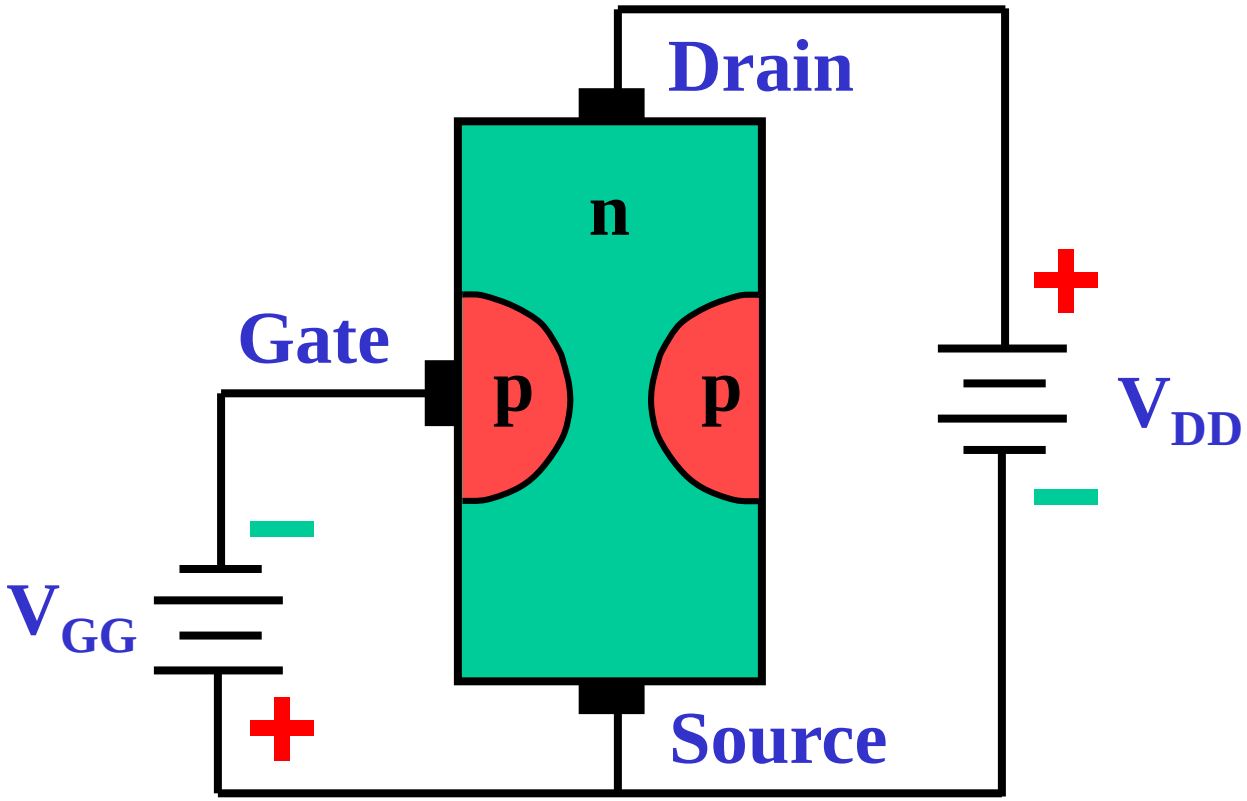
**JFET:** Junction FET

**MOSFET:** Metal–Oxide–Semiconductor FET

**D-MOSFET:** Depletion MOSFET

**E-MOSFET:** Enhancement MOSFET

# Junction field effect transistor (JFET)




**Voltage controlled – the gate voltage controls the drain current**

# JFET Characteristics

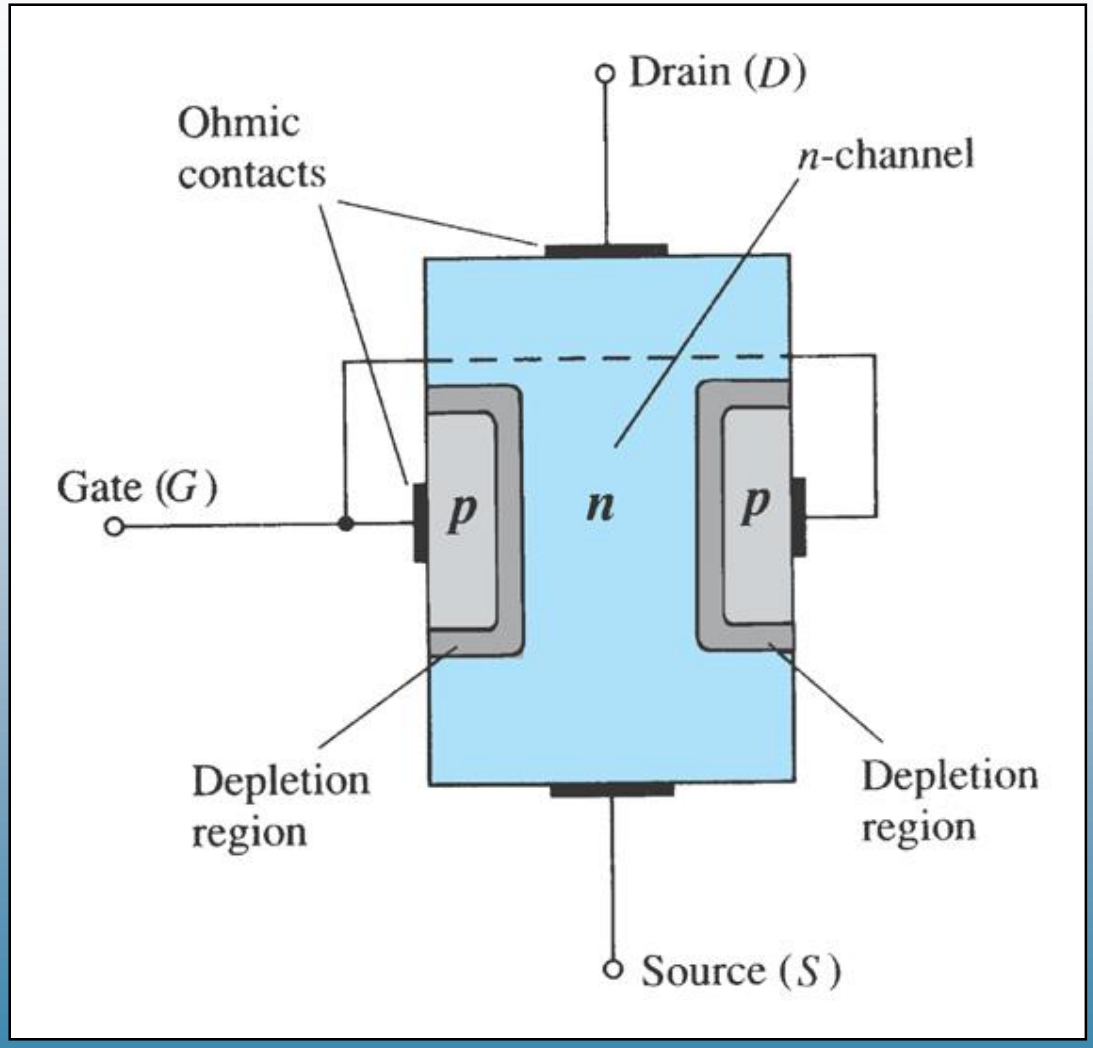
- Unipolar device (one polarity of charge carrier – no minority carriers)
- High input impedance
- Source and drain are interchangeable in most low-frequency applications
- Two diodes: gate-source and gate-drain
- For normal operation the gate-source diode is reverse-biased

# JFET Construction

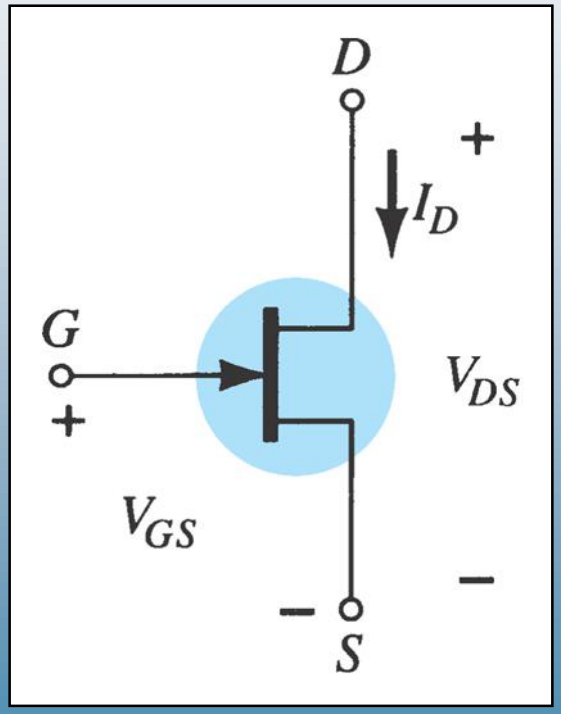
**There are two types of JFETs:**

***n*-channel**
***p*-channel**

*The n-channel is the more widely used of the two.*



# N-Channel JFET Symbol



# JFET Operating Characteristics

***There are three basic operating conditions for a JFET:***

- $V_{GS}$ = 0 V (zero), $V_{DS}$ increasing to some positive value
- $V_{GS}$ < 0 V (negative), $V_{DS}$ at some positive value
- Ohmic region: Voltage-controlled resistor

# JFET Operation: $V_{GS}$=0V

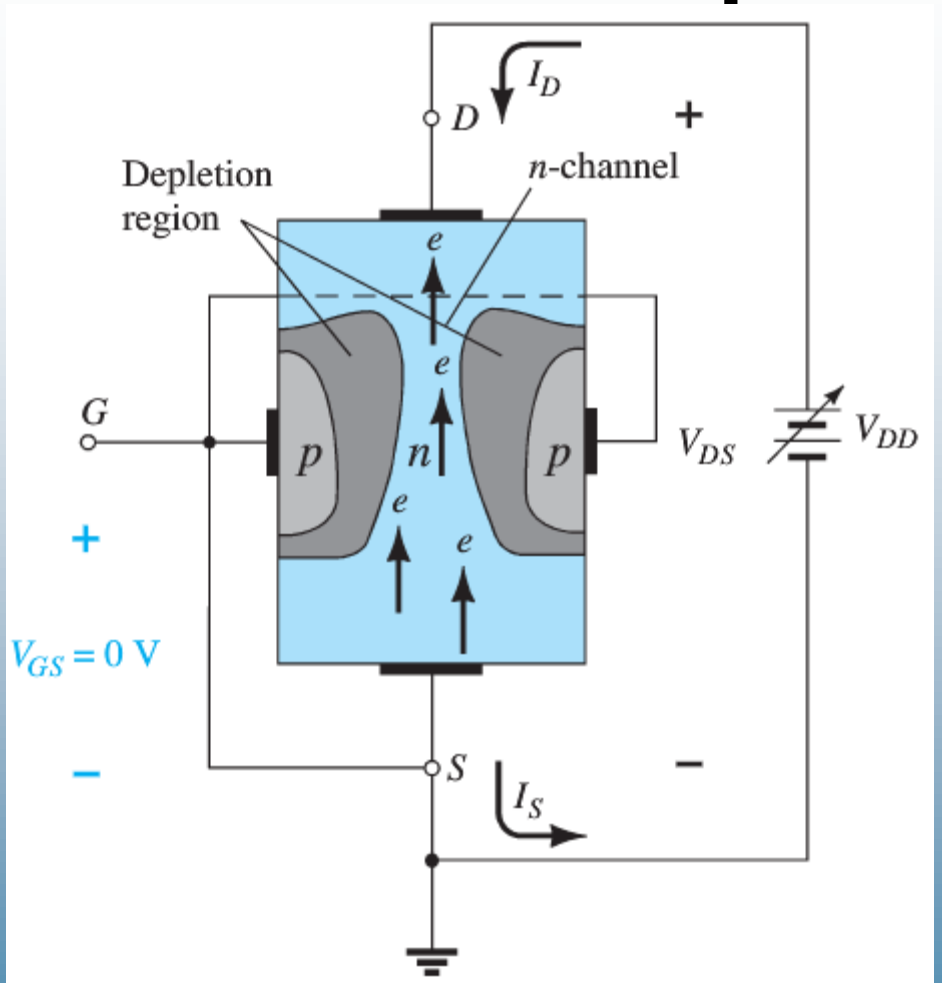



**FIG. 6.5**

*JFET at $V_{GS} = 0$ V and $V_{DS} > 0$ V.*

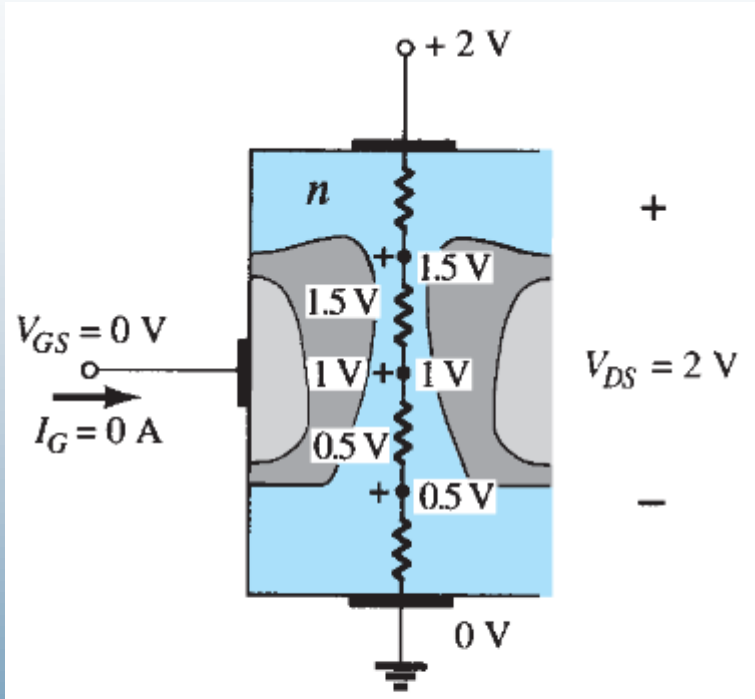


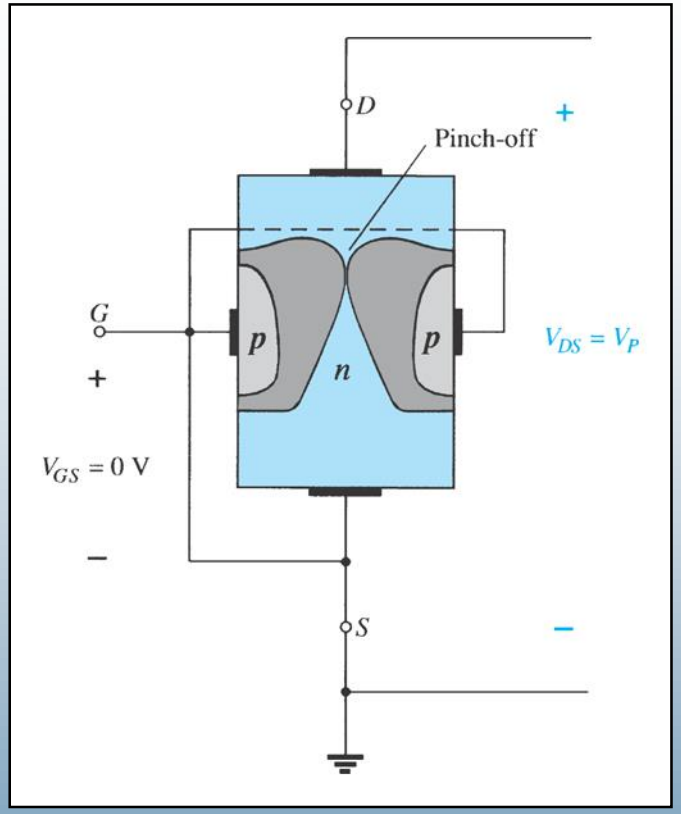

**FIG. 6.6**

*Varying reverse-bias potentials across the p–n junction of an n-channel JFET.*

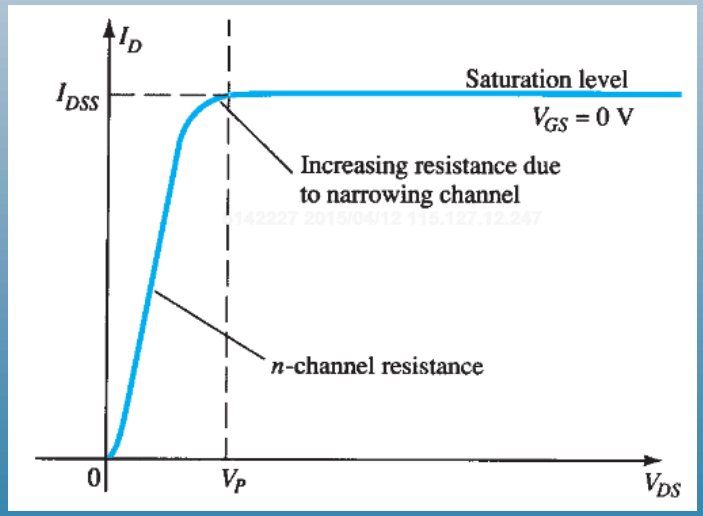
# JFET Characteristics: Pinch Off

• If $V_{GS}$ = 0 V and $V_{DS}$ continually increases, eventually the depletion region gets so large that it pinches off the channel.

**• This suggests that the current in channel ($I_D$) drops to 0 A, but it does not.**
**• Before pinch-off, as $V_{DS}$ increases, so does $I_D$.**
**• Once pinch off occurs, further increases in $V_{DS}$ do not cause $I_D$ to increase.**




*Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).*




*$I_D$ versus $V_{DS}$ for $V_{GS} = 0$ V.*

# At Pinch-Off, The Channel Is Not Really Pinched Off!

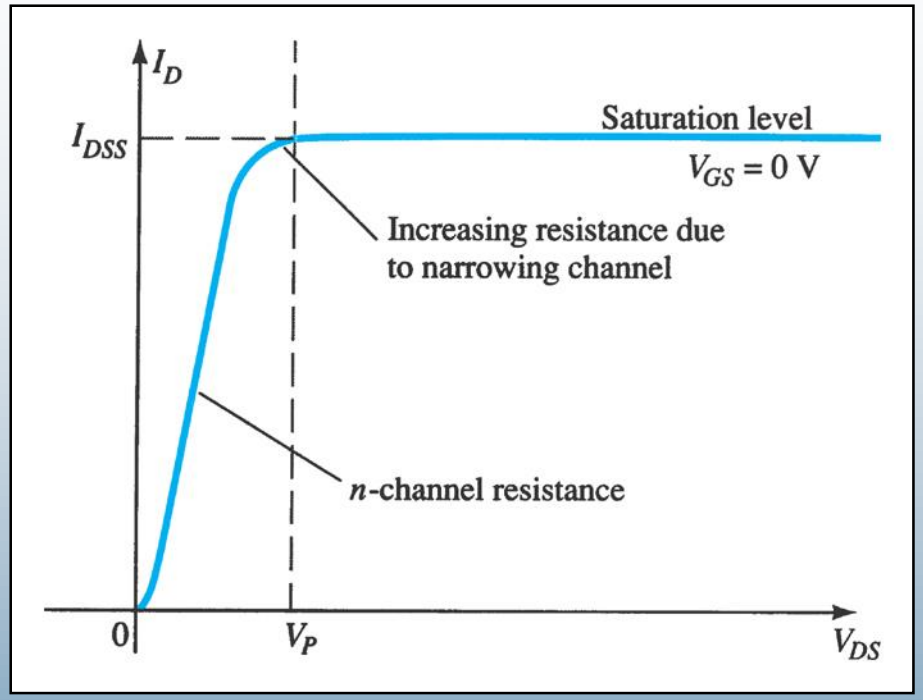
- The term pinch-off is a misnomer in that it suggests the current $I_D$ is pinched off and drops to 0A.
  - However, this is hardly the case — $I_D$ maintains a saturation level defined as $I_{DSS}$
- In reality, a very small channel still exists, with a current of very high density.
- Why zero $I_D$ is not possible at pinch-off? The absence of a drain current would remove the possibility of different potentials along the n-channel to establish the varying levels of reverse bias along the p–n junction.
  - The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

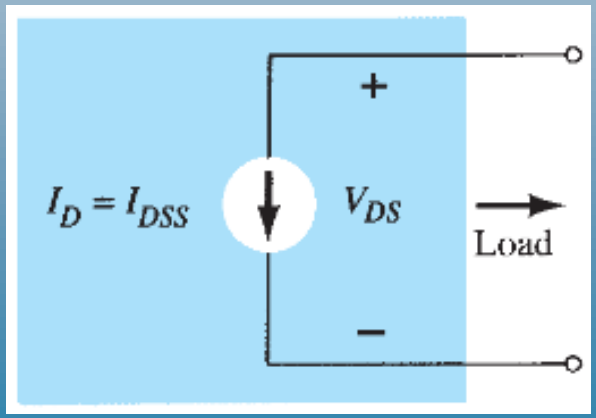
# JFET Characteristics: Saturation

*At the pinch-off point:*

Any further increase in $V_{DS}$ does not produce any increase in $I_D$. $V_{DS}$ at pinch-off is denoted as $V_p$

$I_D$ is at saturation or maximum, and is referred to as $I_{DSS}$.

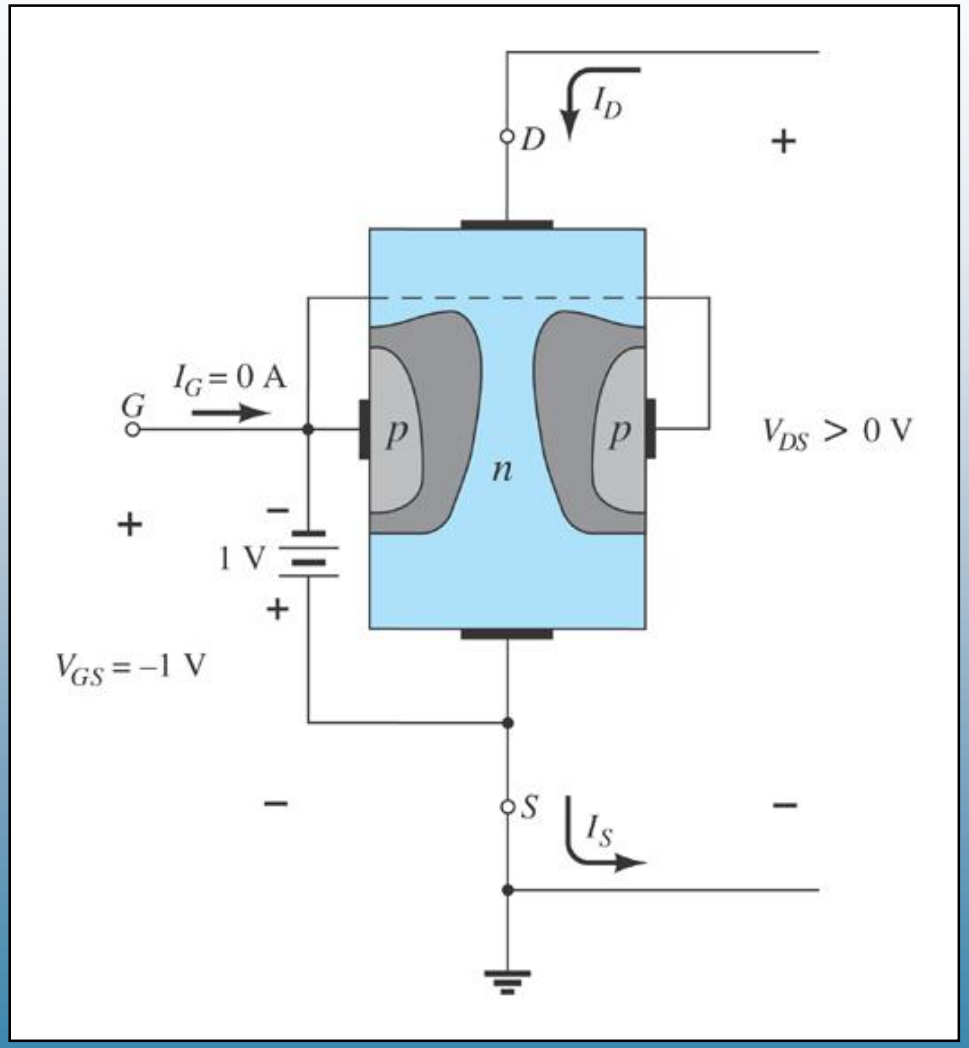



*Current source equivalent for* $V_{GS} = 0$ V, $V_{DS} > V_P$.

# JFET Operating Characteristics, $V_{GS}$<0V

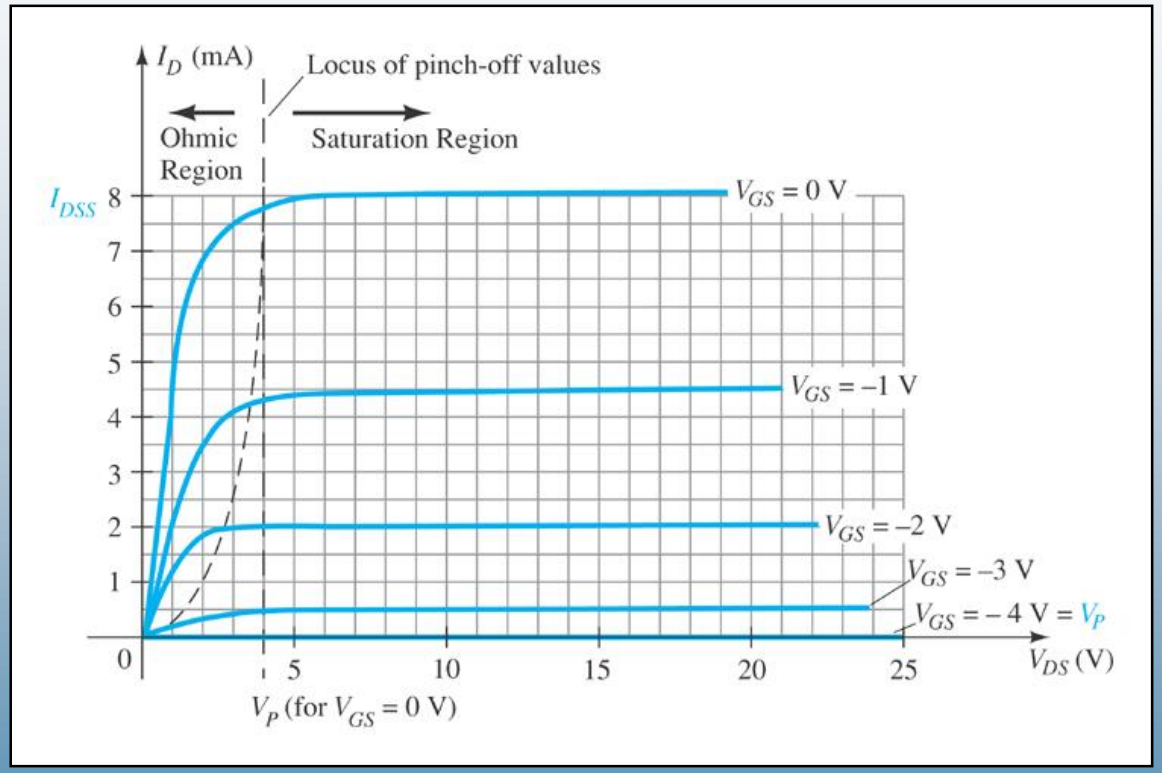
As $V_{GS}$ becomes more negative, the depletion region increases.



# JFET Operating Characteristics

*As $V_{GS}$ becomes more negative:*

- The JFET experiences pinch-off at a lower voltage ($V_P$).
- $I_D$ decreases ($I_D < I_{DSS}$) even when $V_{DS}$ increases
- $I_D$ eventually drops to 0 A. The value of $V_{GS}$ that causes this to occur is designated $V_{GS(off)}$.




At high levels of $V_{DS,}$ the JFET reaches a breakdown situation. $I_D$ increases uncontrollably if $V_{DS} > V_{DSmax}$, and the JFET is likely destroyed.

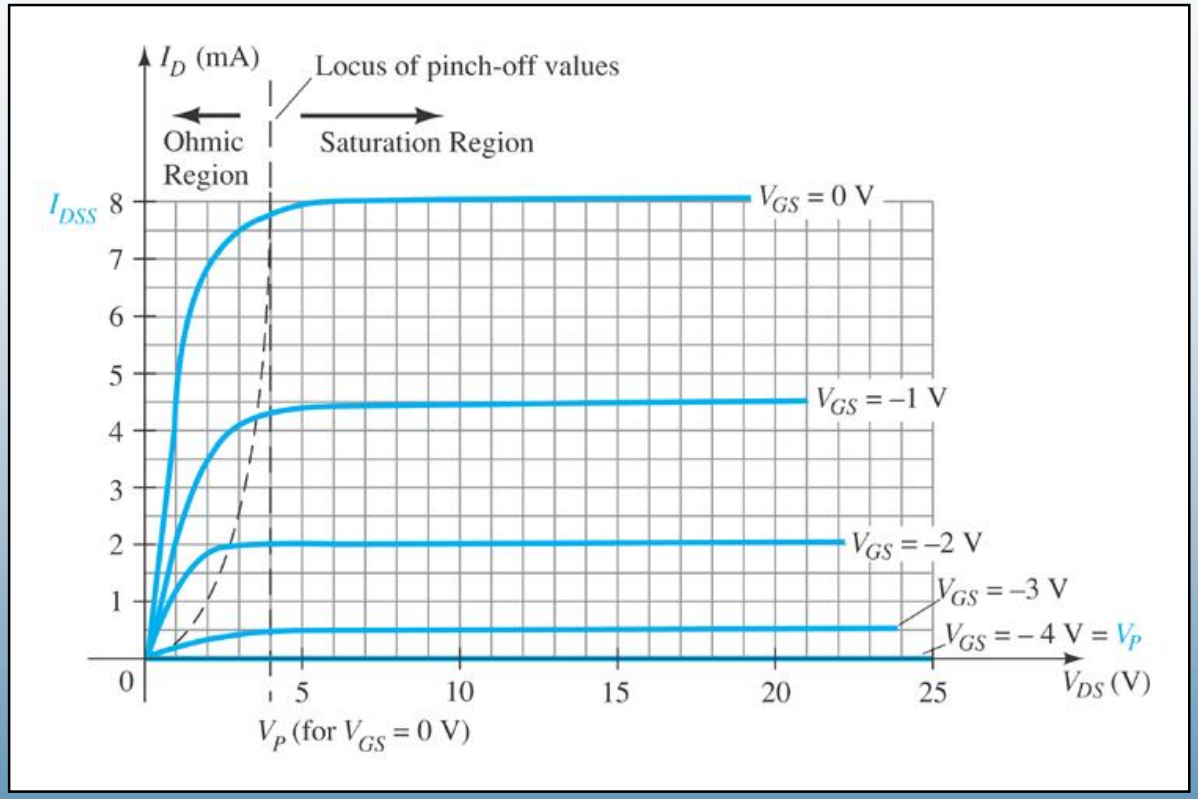
# Voltage-Controlled Resistor

The region to the left of the pinch-off point is called the **ohmic region.**

The JFET can be used as a variable resistor, where $V_{GS}$ controls the drain-source resistance ($r_d$).

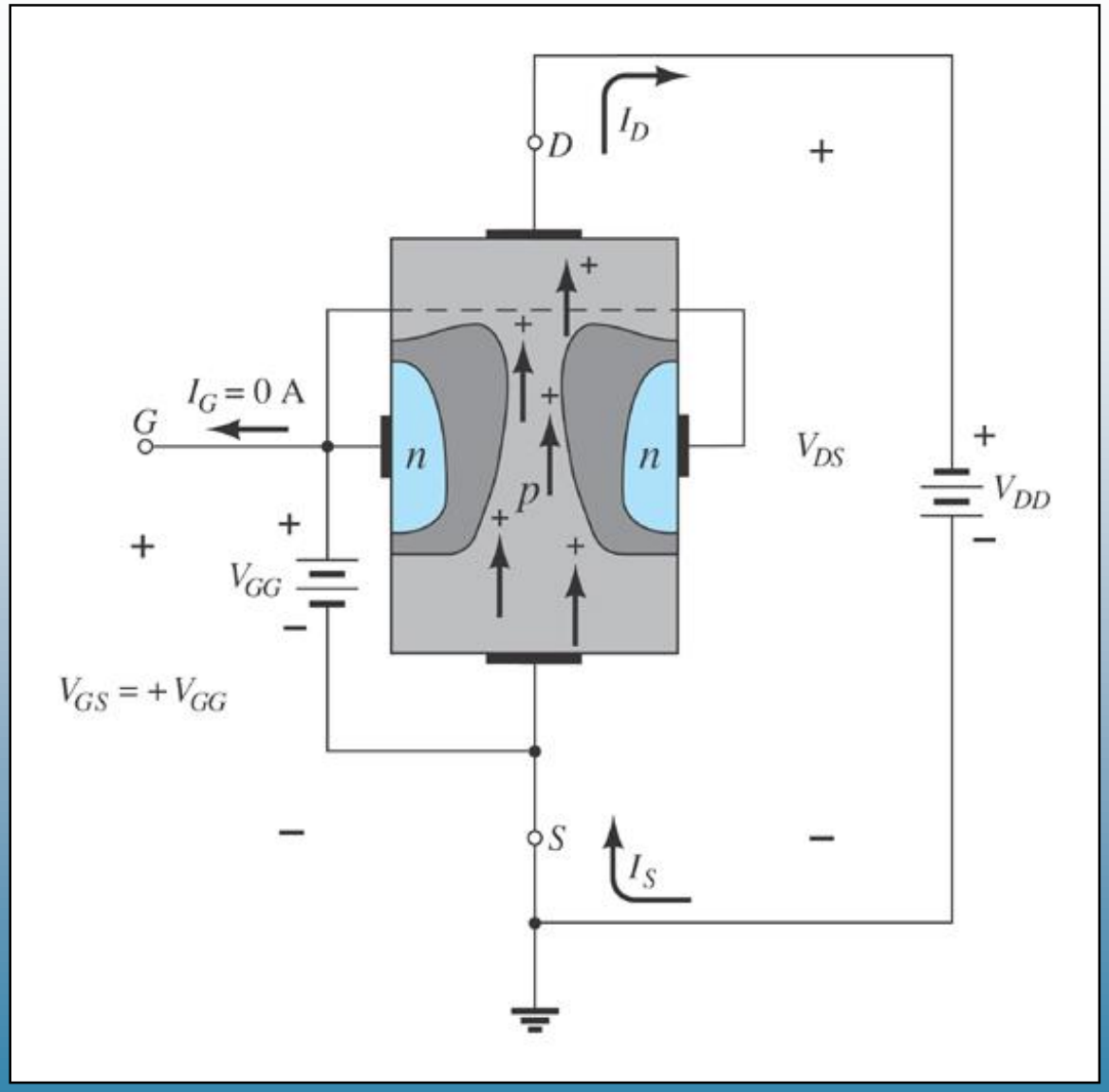
**A good first approximation:**

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$




**As $V_{GS}$ becomes more negative, the resistance ($r_d$) increases.**

# P-Channel JFETs

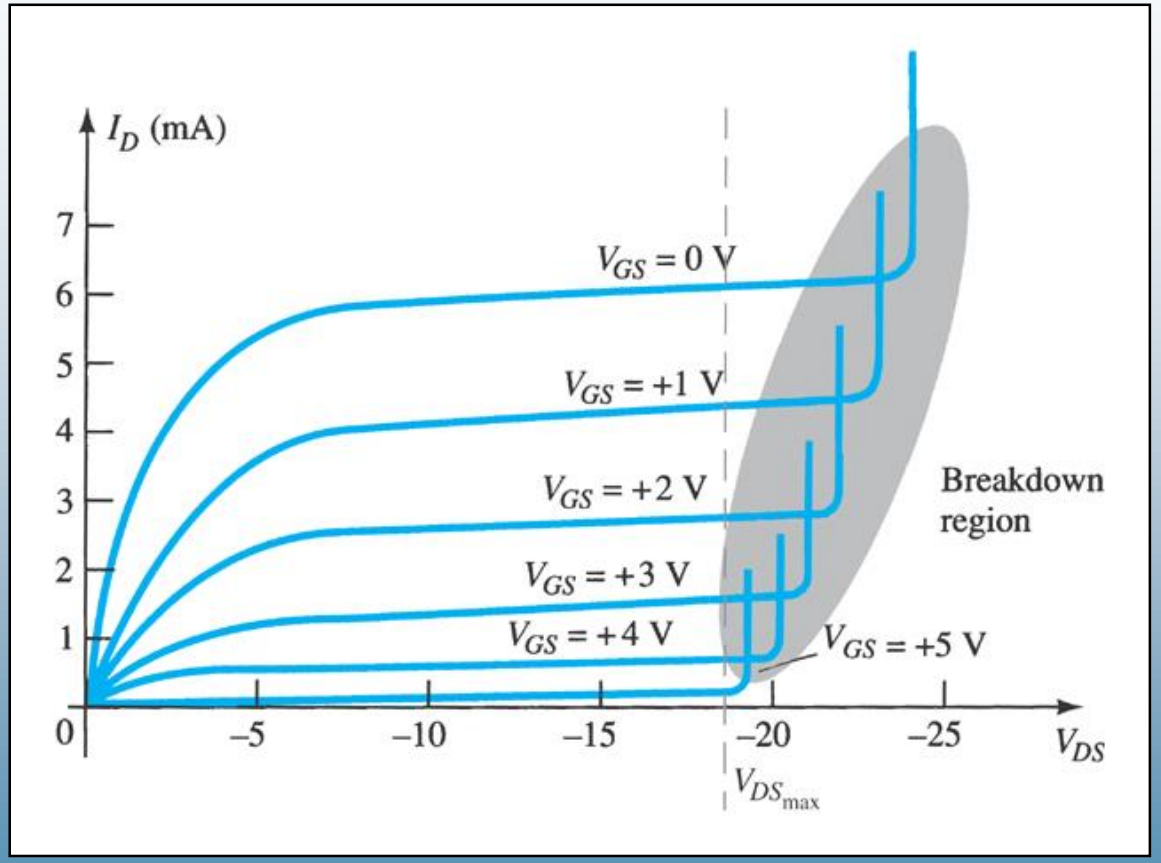



- The *p*-channel JFET behaves the same as the *n*-channel JFET.
- The only differences are that the voltage polarities and current directions are reversed.

# P-Channel JFET Characteristics

*As $V_{GS}$ becomes more positive:*

- The JFET experiences pinch-off at a lower voltage ($V_P$).
- The depletion region increases, and $I_D$ decreases ($I_D < I_{DSS}$)
- $I_D$ eventually drops to 0 A (when $V_{GS} = V_{GSoff}$)




**Also note that at high levels of $V_{DS}$ the JFET reaches a breakdown situation: $I_D$ increases uncontrollably if $V_{DS} > V_{DSmax}$.**

# JFET Symbols

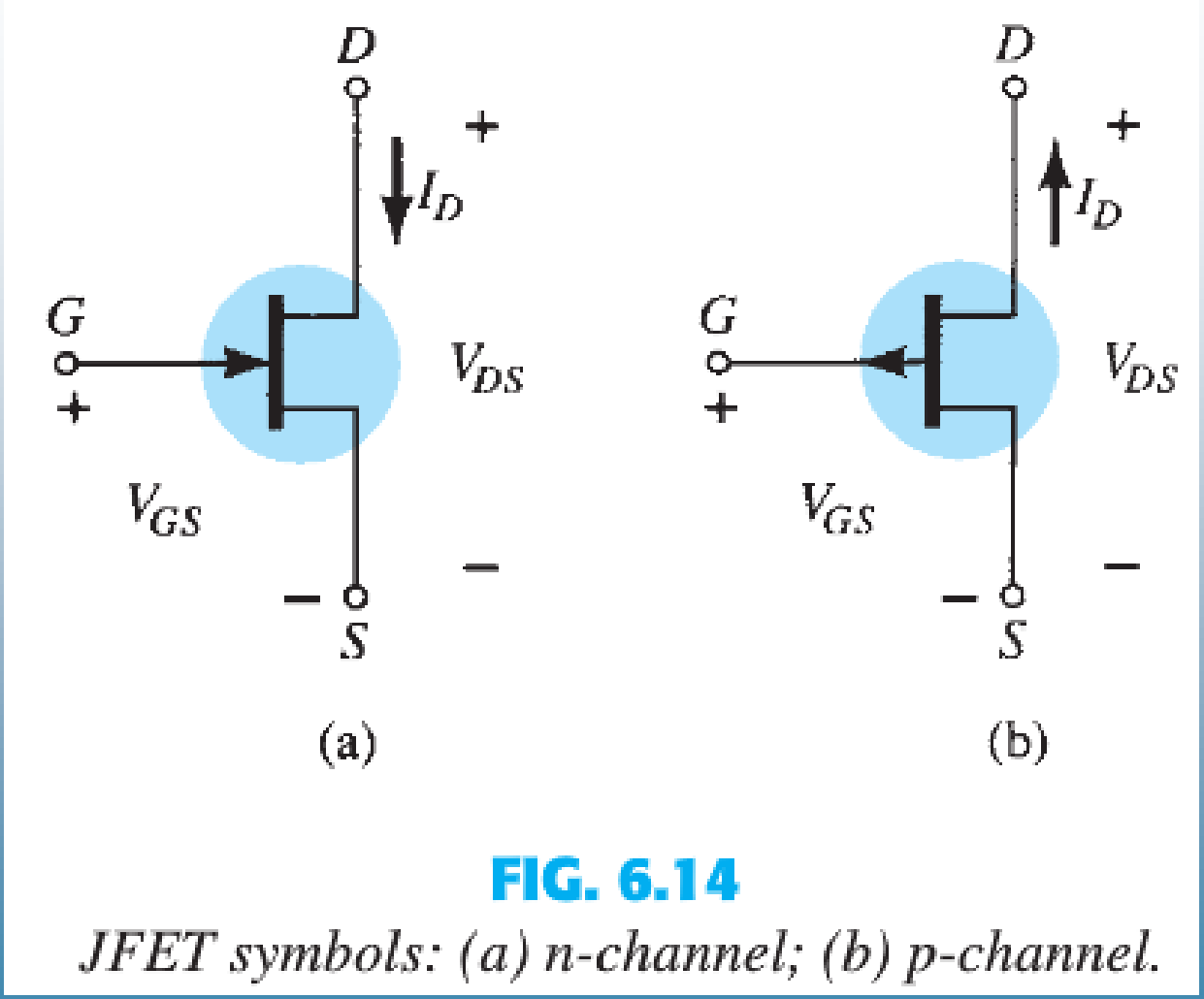


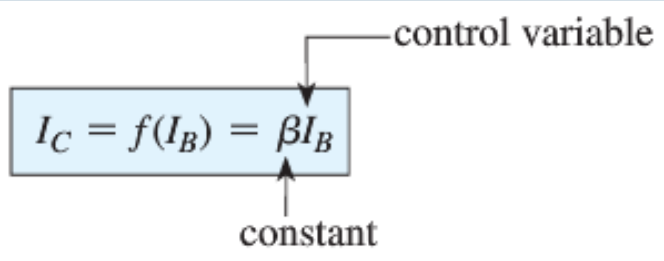

**FIG. 6.14**

*JFET symbols: (a) n-channel; (b) p-channel.*

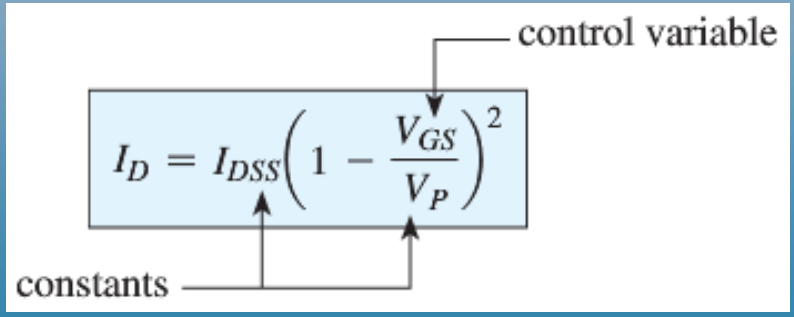
# JFET Transfer Characteristics

*JFET input-to-output transfer characteristics are not as straightforward as they are for a BJT.*

• BJT: $\beta$ indicates the relationship between $I_B$ (input) and $I_C$ (output).




• JFET: The relationship of $V_{GS}$ (input) and $I_D$ (output) is a little more complicated:

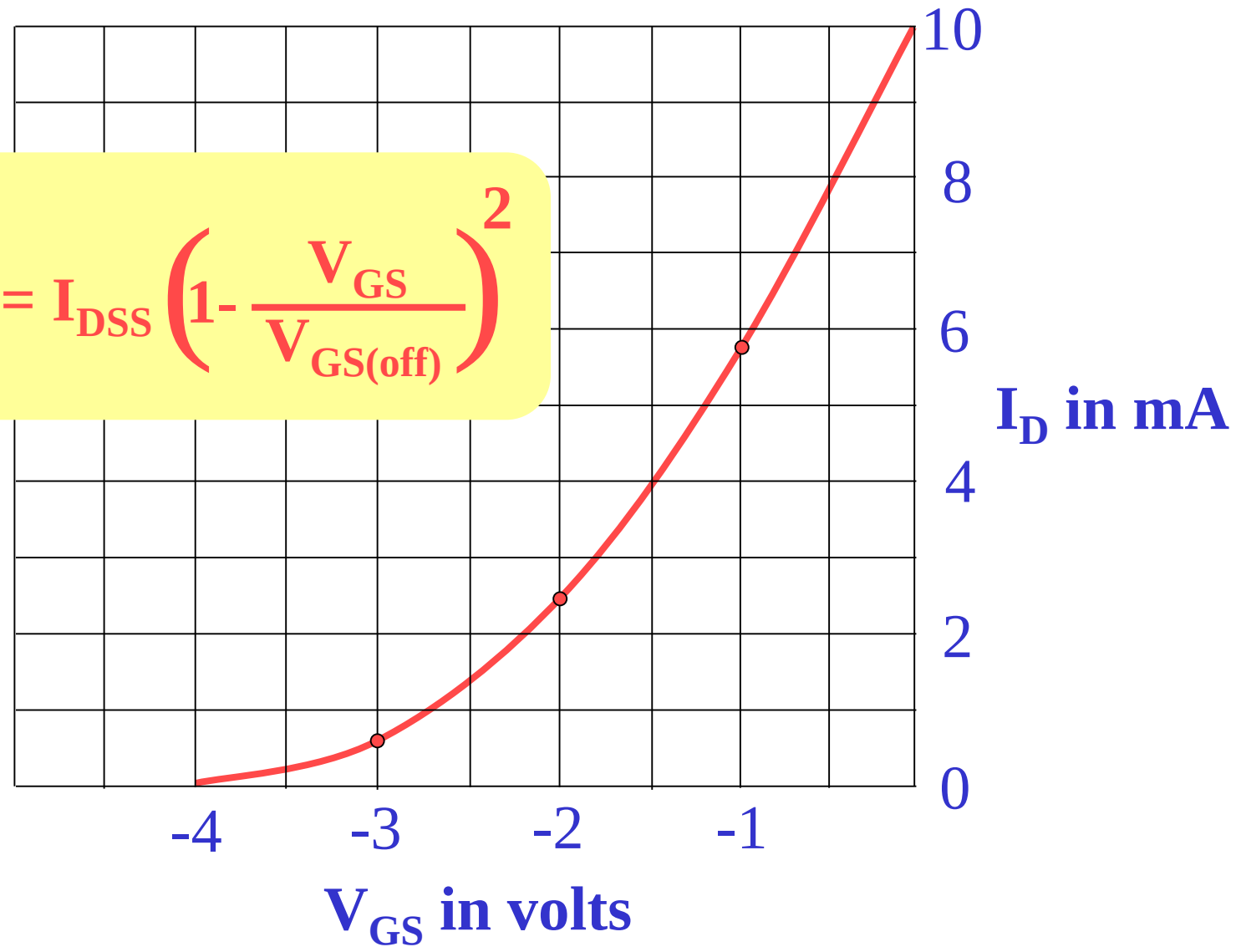



*Shockley's equation*

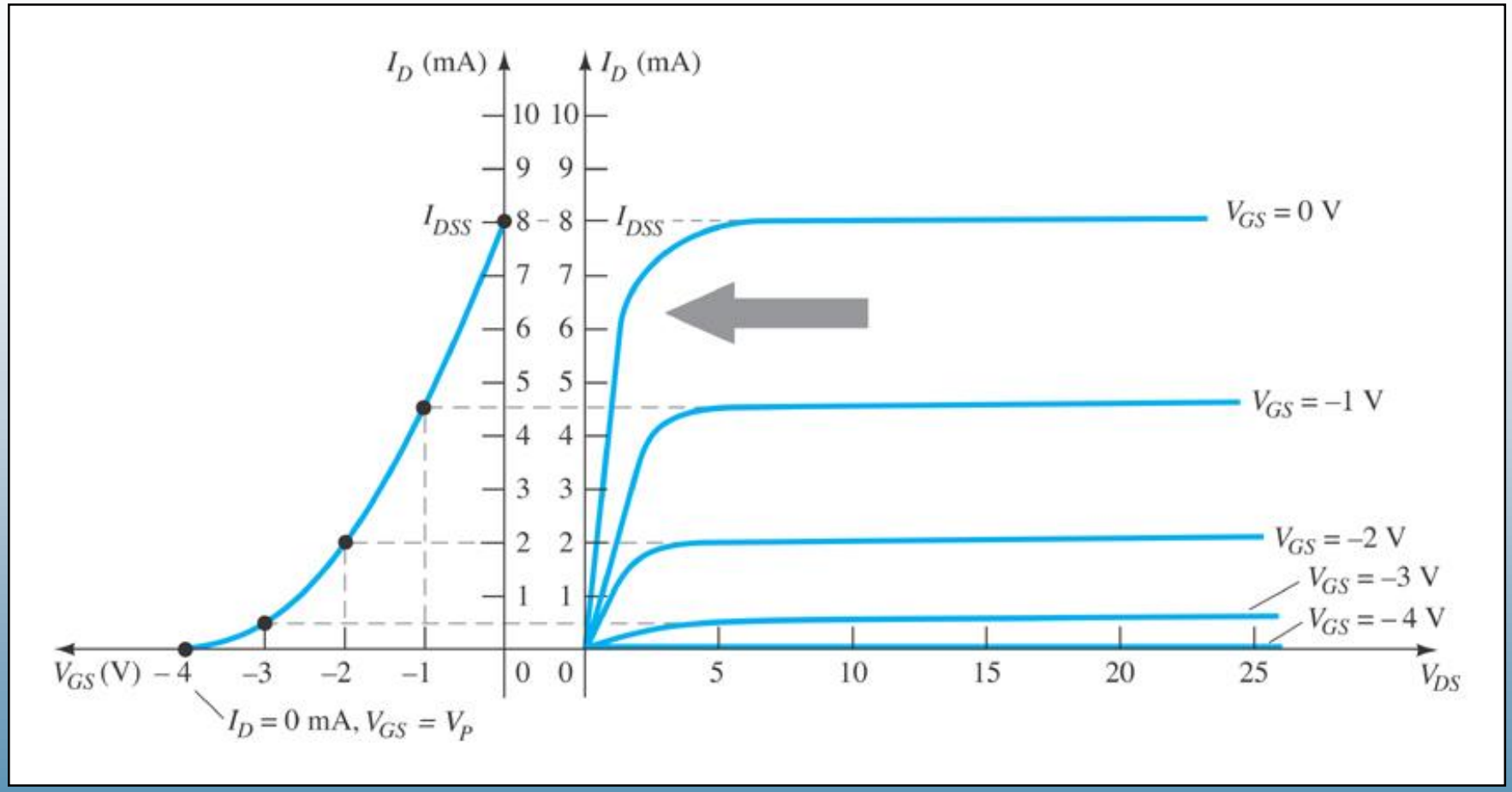
# JFET Transfer Characteristics

## (Transconductance curve)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$



# JFET Transfer Curve




*Obtaining the transfer curve from the drain characteristics.*

**EXAMPLE 6.1** Sketch the transfer curve defined by $I_{DSS} = 12\text{ mA}$ and $V_P = -6\text{ V}$.

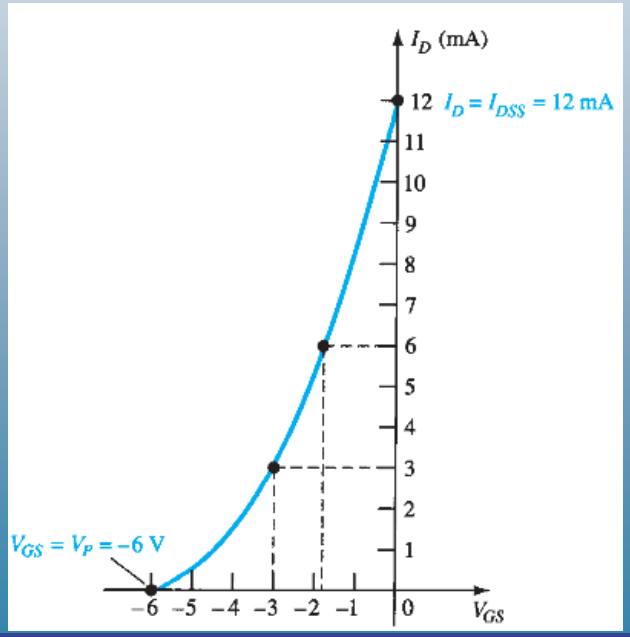
***Solution:*** Two plot points are defined by

$$I_{DSS} = \mathbf{12\text{ mA}} \quad \text{and} \quad V_{GS} = \mathbf{0\text{ V}}$$

and

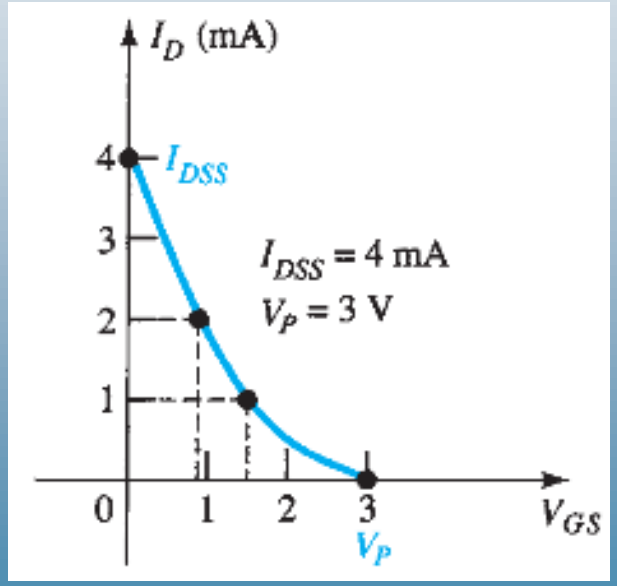
$$I_D = \mathbf{0\text{ mA}} \quad \text{and} \quad V_{GS} = \boldsymbol{V_P}$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = \mathbf{-3\text{ V}}$ the drain current is determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = \mathbf{3\text{ mA}}$. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = \mathbf{6\text{ mA}}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = \mathbf{-1.8\text{ V}}$. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

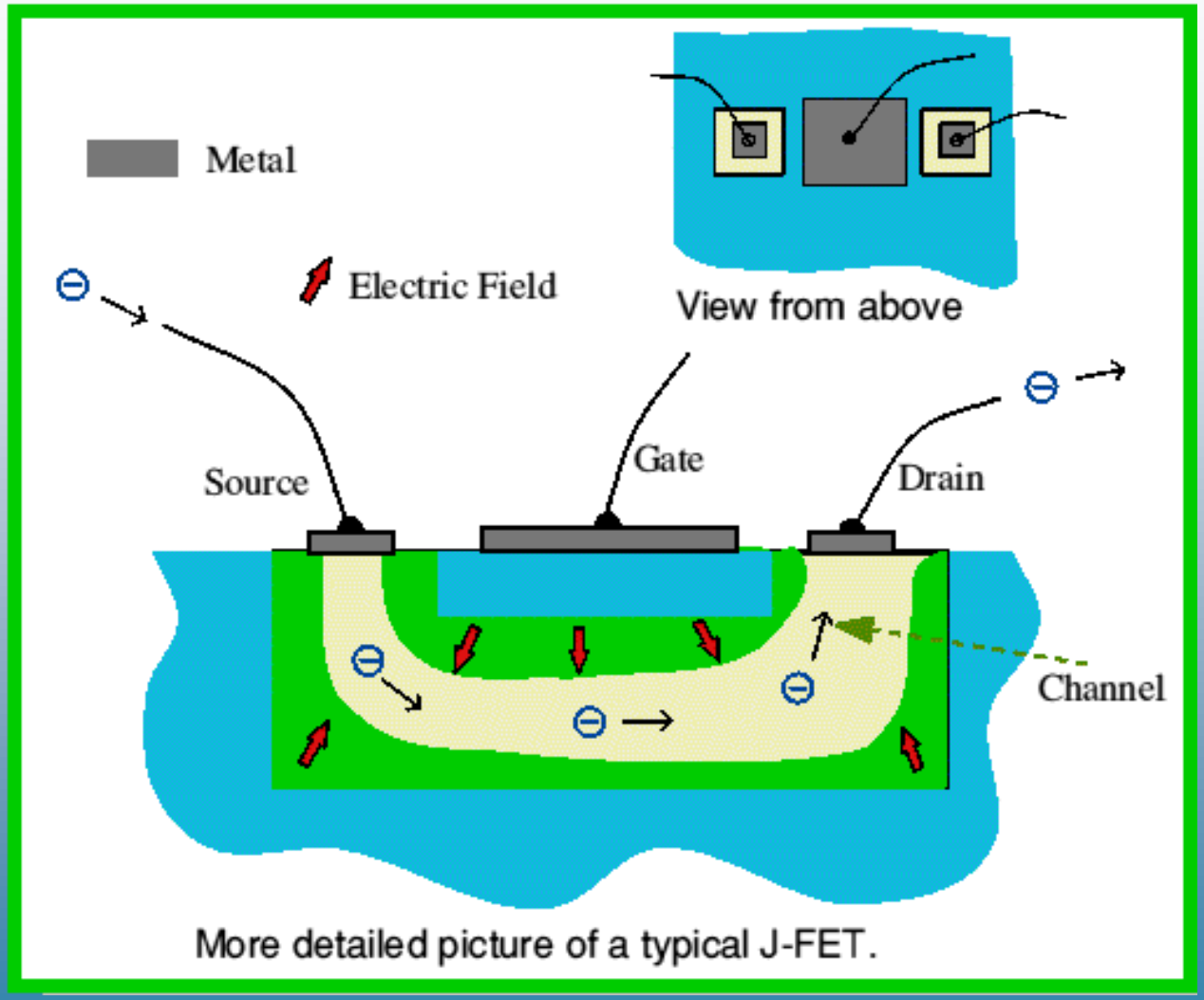


**EXAMPLE 6.2** Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4\,\text{mA}$ and $V_P = 3\,\text{V}$.

***Solution:*** At $V_{GS} = V_P/2 = 3\,\text{V}/2 = \mathbf{1.5\,V}$, $I_D = I_{DSS}/4 = 4\,\text{mA}/4 = \mathbf{1\,mA}$. At $I_D = I_{DSS}/2 = 4\,\text{mA}/2 = \mathbf{2\,mA}$, $V_{GS} = 0.3V_P = 0.3(3\,\text{V}) = \mathbf{0.9\,V}$. Both plot points appear in Fig. 6.19 along with the points defined by $I_{DSS}$ and $V_P$.



# Integrated Circuit Operational View of An N-Channel JFET



# Field-Effect Transistors (MOSFET)

# MOSFETs

**MOSFETs have characteristics similar to those of JFETs and additional characteristics that make then very useful.**

# Introduction

- **Q:** What are two major types of three-terminal semiconductor devices?
  - metal-oxide-semiconductor field-effect transistor (MOSFET)
  - bipolar junction transistor (BJT)
- **Q:** Why are MOSFET's more widely used?
  - size (smaller)
  - ease of manufacture
  - Consumes much less operating power

- MOSFET technology
  - It allows placement of approximately 2 billion transistors on a single IC
    - backbone of very large scale integration (VLSI)
  - It is considered preferable to BJT technology for many applications.

**note:** MOSFET is more widely used in implementation of modern electronic devices

# MOSFET TYPES

- Two types:
  1. Depletion type
  2. Enhancement type

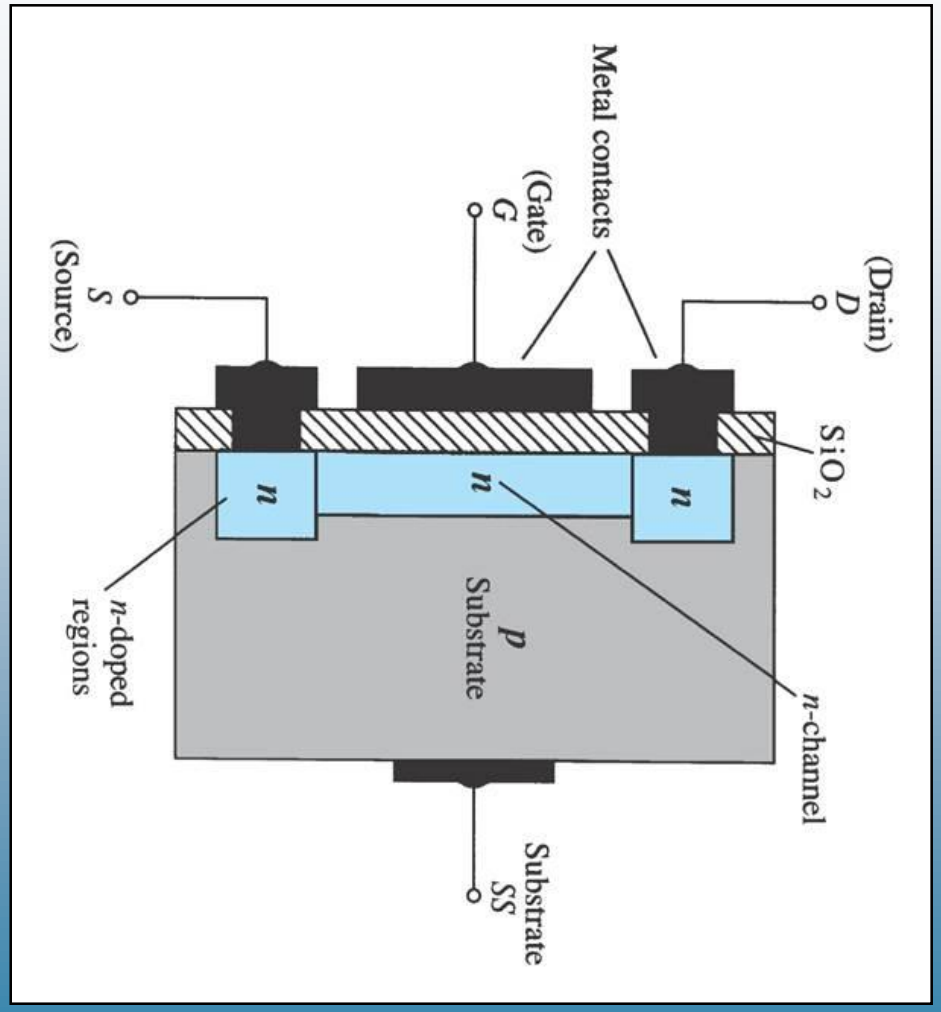
- Both of the above types have two sub-types:
  1. N-channel or simply n-type (also called NMOS in short)
  2. P-channel or simply p-type (also called PMOS in short)

# Some Facts..

- The name MOSFET is derived from its physical structure.
  - Metal Oxide Semiconductor Field Effect Transistor
- However, MOSFET's gates do not actually use any "metal", polysilicon is used instead.
- Another name for MOSFET is insulated gate FET, or IGFET.

# Depletion-Type MOSFET Construction

- The **Drain (D)** and **Source (S)** connect to the to *n*-type regions.
  - The *n*-typed regions are connected via an *n*-channel.
  - The *n*-channel is connected to the **Gate (G)** via a thin insulating layer of silicon dioxide ($SiO_2$).
- The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the **Substrate (SS)**.



# Basic Operation and Characteristics

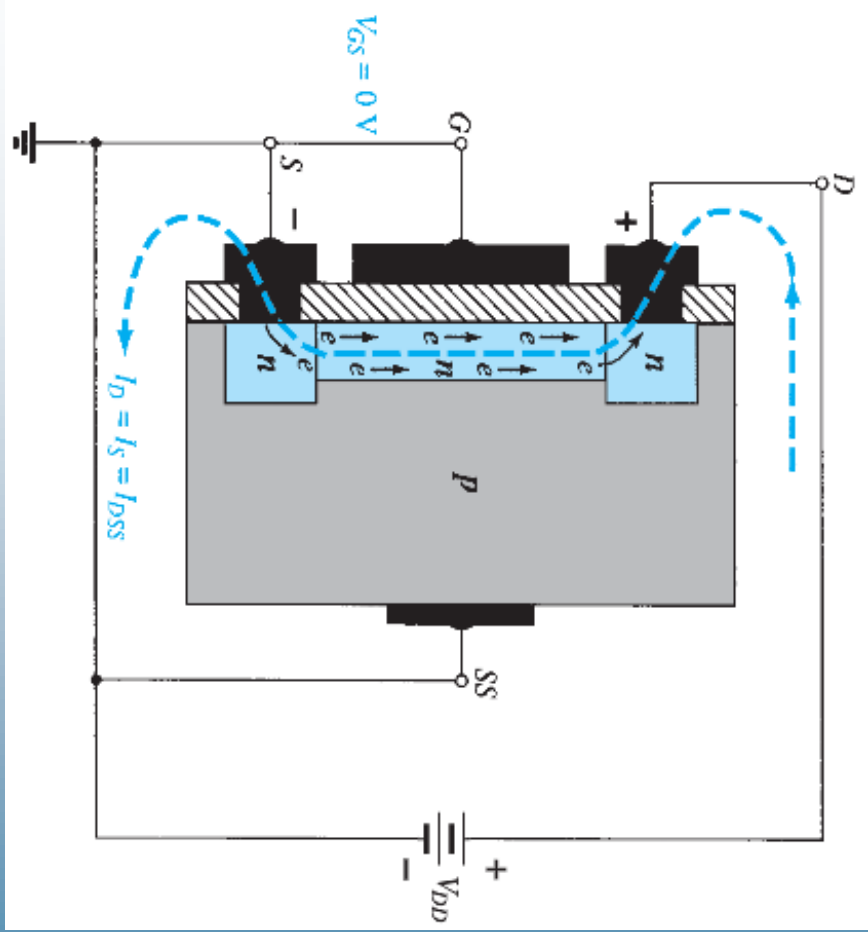



Figure: n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage $V_{DD}$.

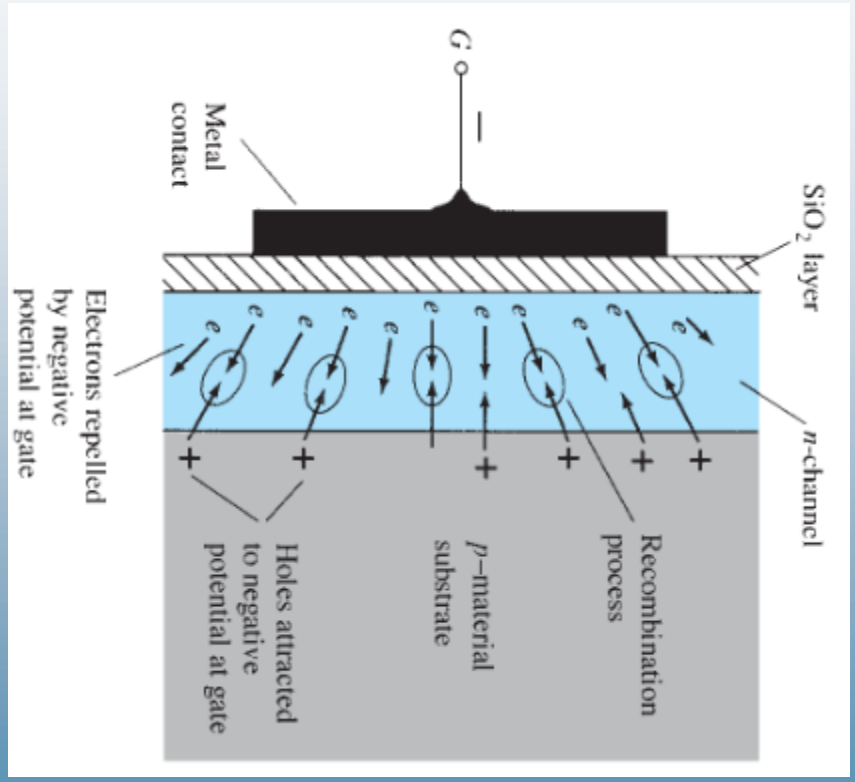
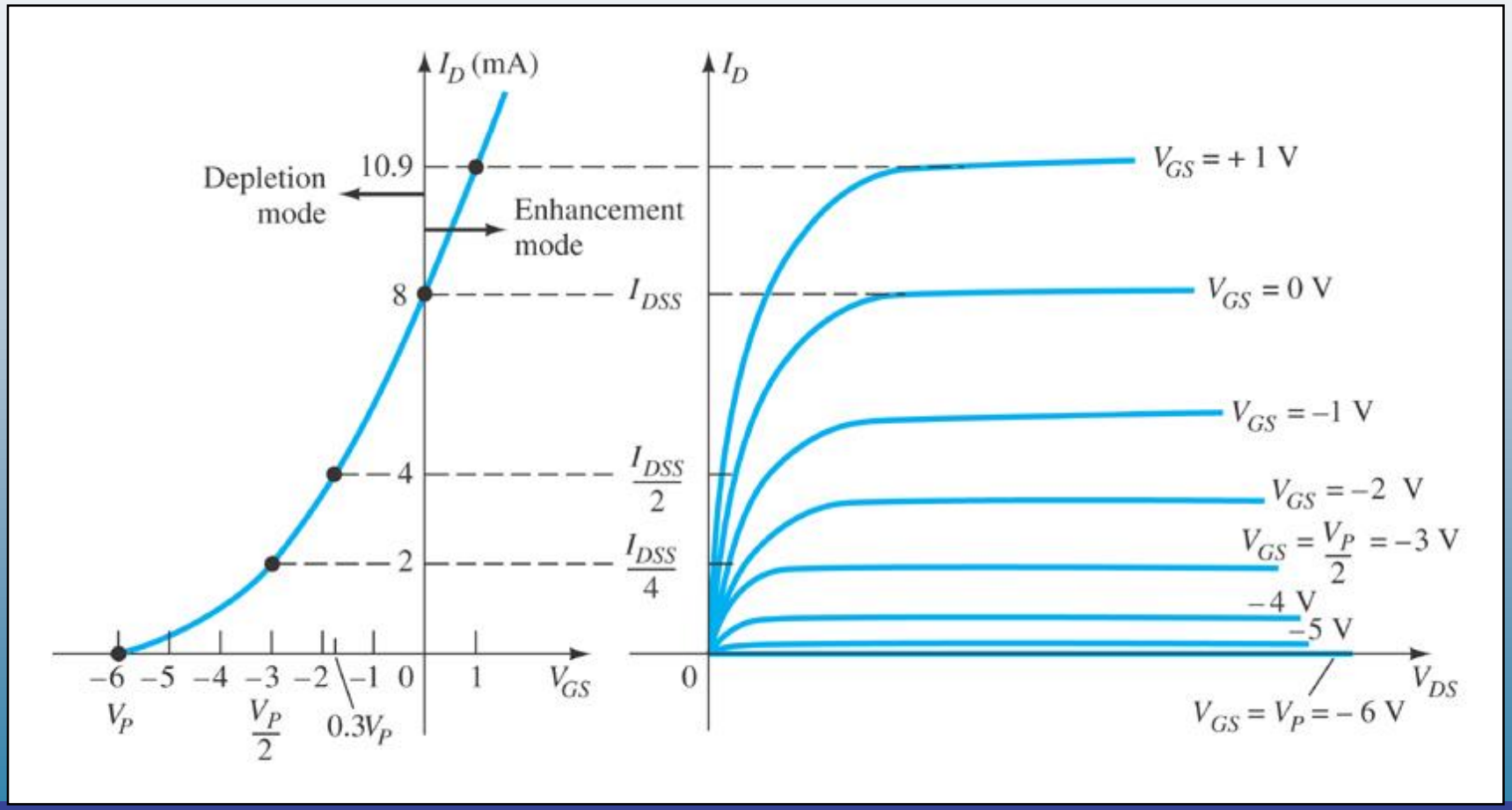



Figure: Reduction in free carriers in a channel due to a negative potential at the gate terminal.

# Basic MOSFET Operation

A depletion-type MOSFET can operate in two modes:

**Depletion and Enhancement modes**

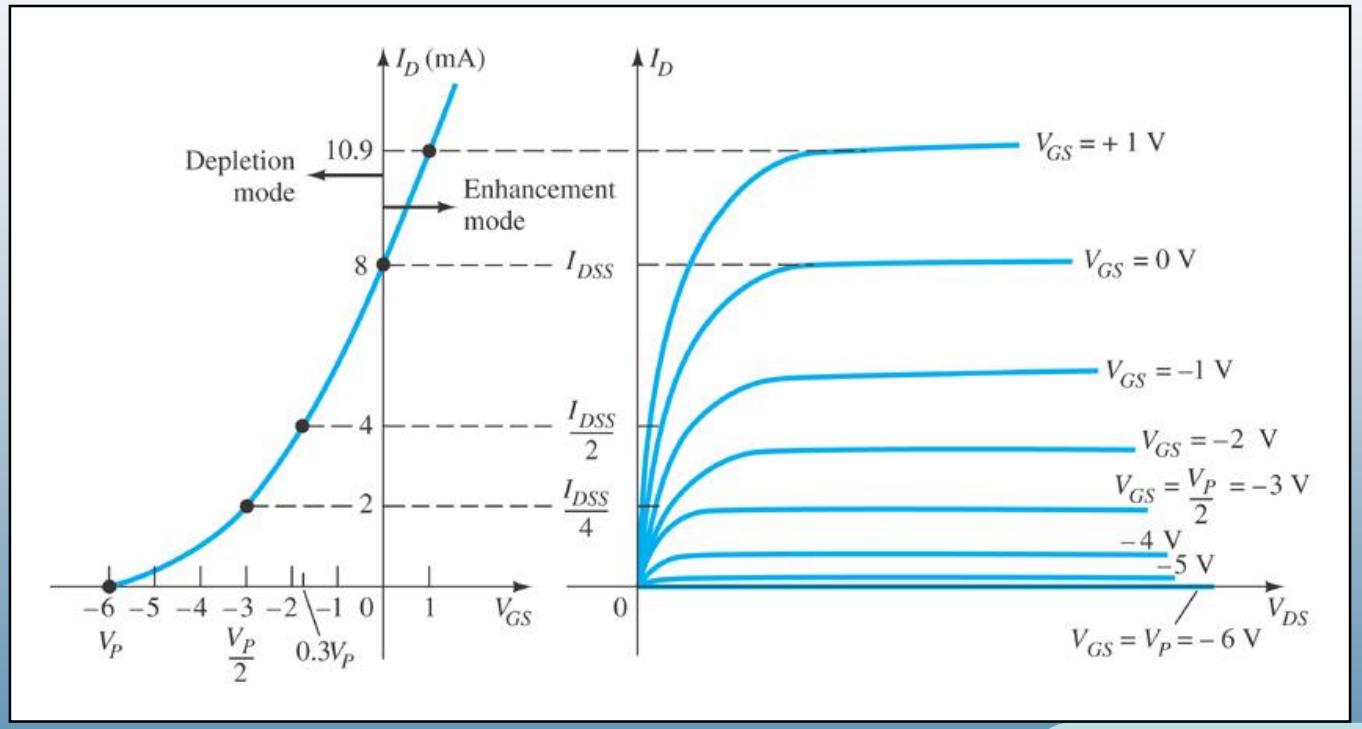


# Depletion Mode Operation (D-MOSFET)

The characteristics are similar to a JFET.

When $V_{GS} = 0$ V, $I_D = I_{DSS}$

When $V_{GS} < 0$ V, $I_D < I_{DSS}$



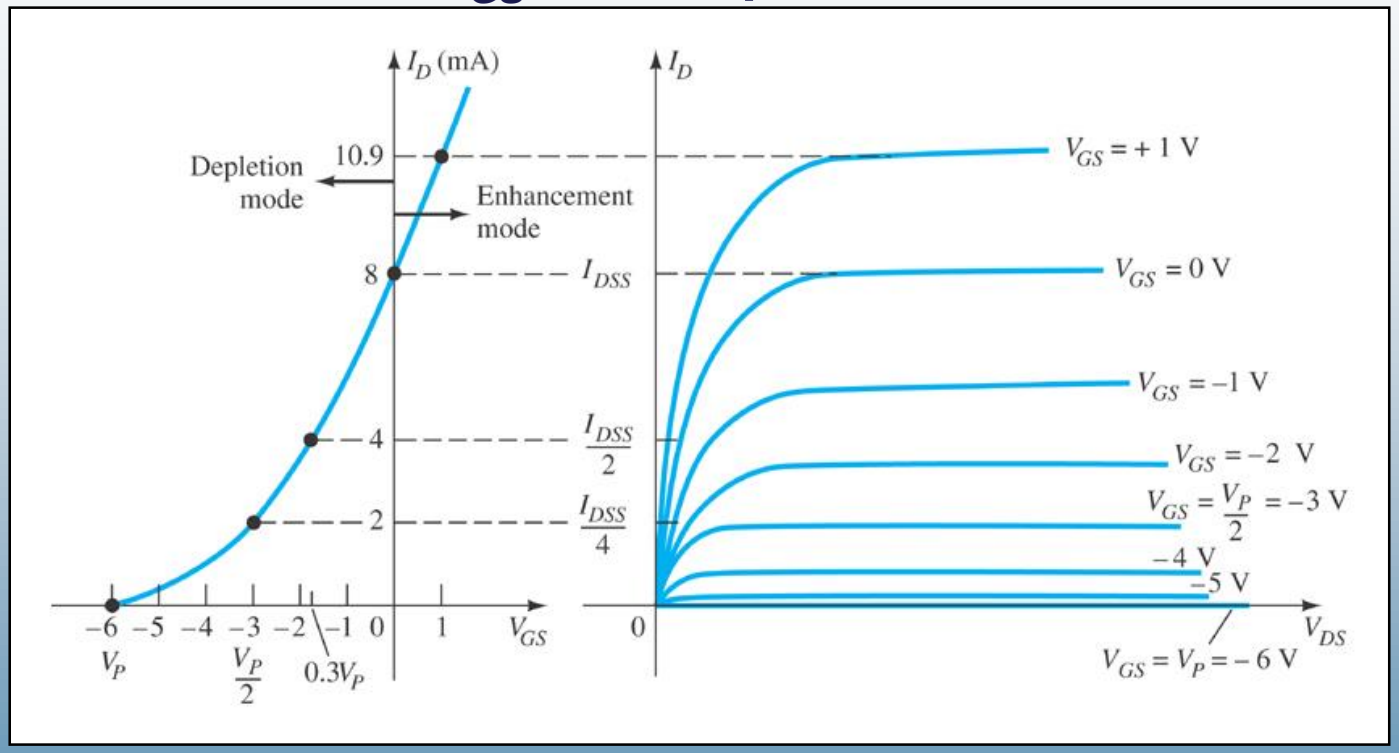

**The formula used to plot the transfer curve for a JFET applies to a D-MOSFET as well:**

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

# Enhancement Mode Operation Of D-MOSFETs

**$V_{GS}$ is now positive**

$V_{GS} > 0$ V, $I_D$ increases above $I_{DSS}$ ($I_D > I_{DSS}$)

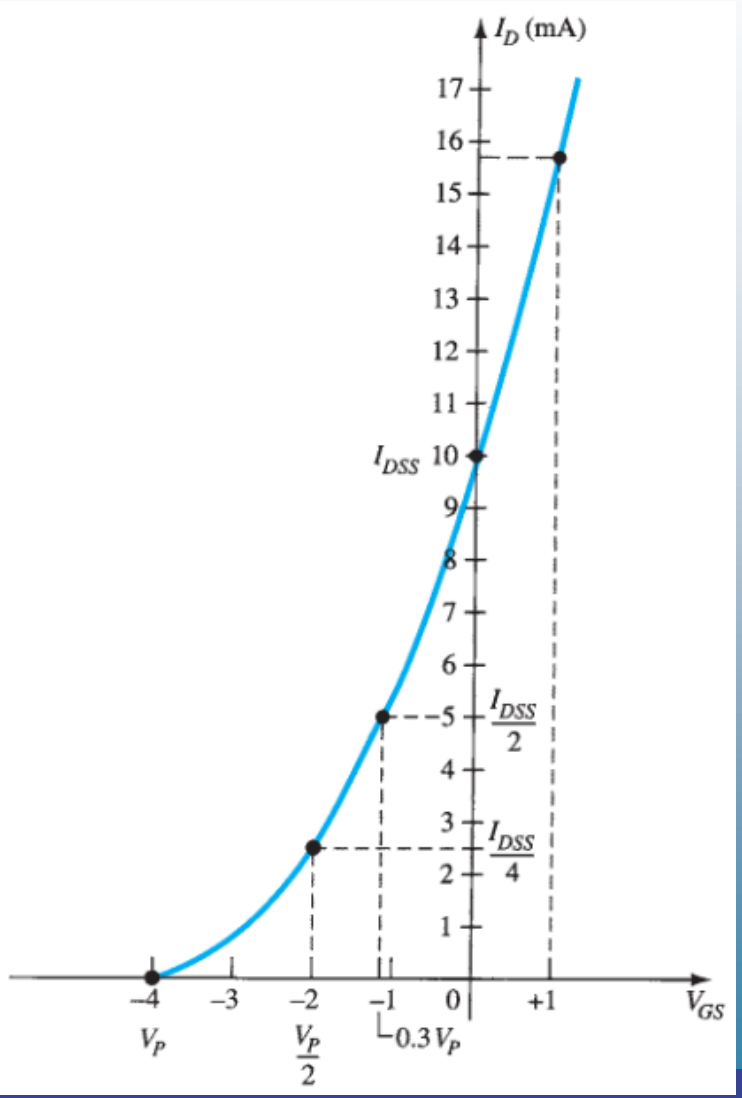



The formula used to plot the transfer curve still applies:

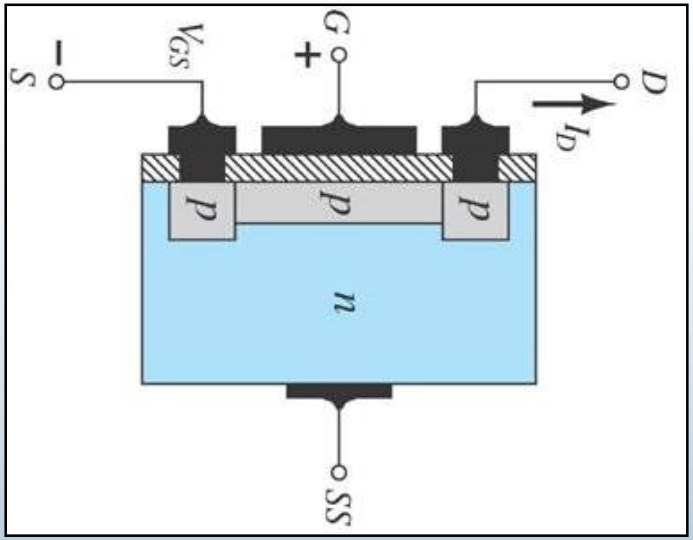
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

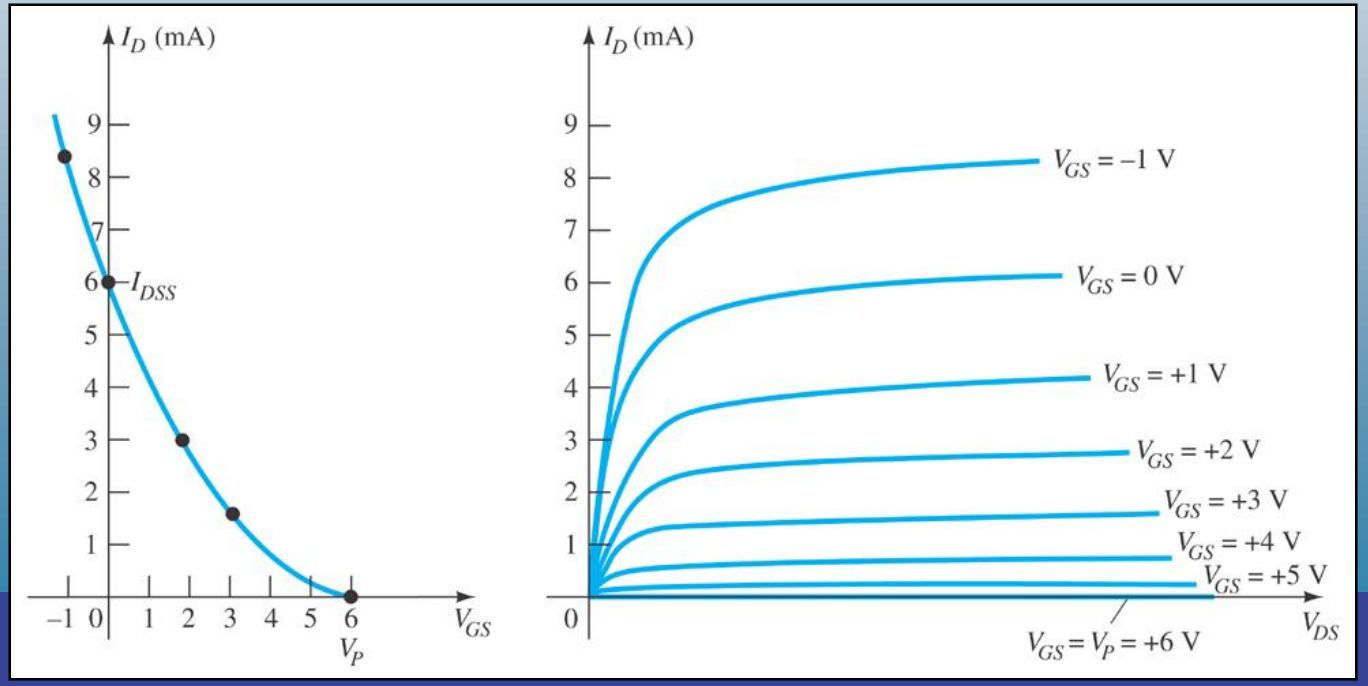
**EXAMPLE 6.3** Sketch the transfer characteristics for an $n$-channel depletion-type MOSFET with $I_{DSS} = 10\,\text{mA}$ and $V_P = -4\,\text{V}$.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

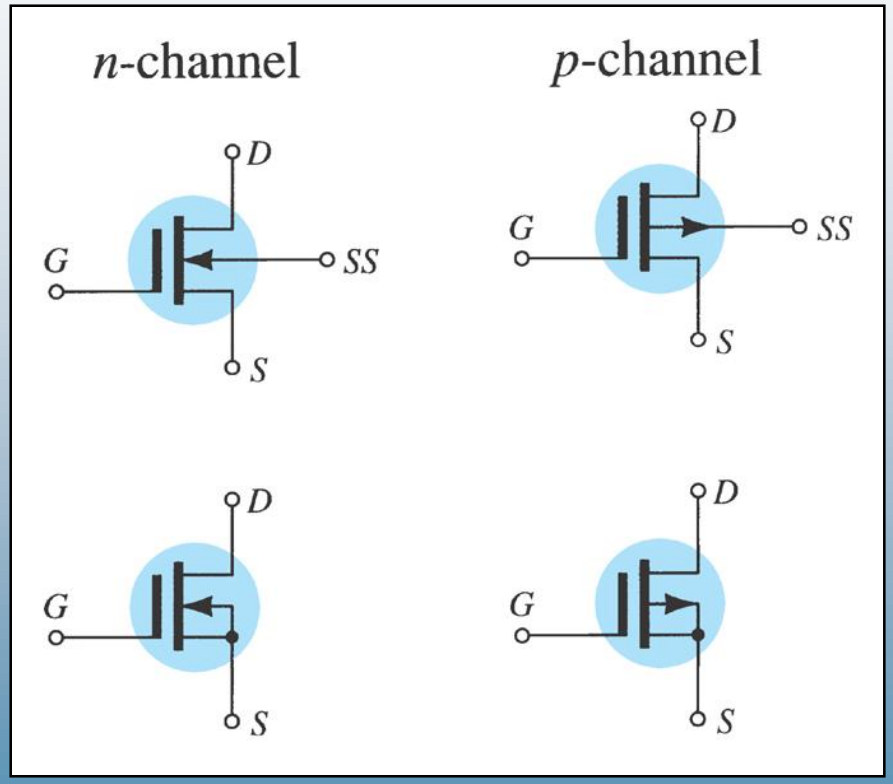


# *p*-Channel D-Type MOSFET



# D-Type MOSFET Symbols




- The symbols try to reflect the actual construction of the device.
- The lack of a direct connection (due to the gate insulation) between the gate and the channel is represented by a space between the gate and the other terminals of the symbol.
- The vertical line representing the channel is connected between the drain and the source and is “supported” by the substrate.
- Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available, whereas in others it is not.
- For most of our analysis, the substrate and the source will be connected and the lower symbols will be employed.

# ENHANCEMENT-TYPE MOSFET

## E-MOSFET

# E-MOSFET CHARACTERISTICS

- Although there are some similarities between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different
- The transfer curve is not defined by Shockley's equation
- The drain current is now cut off until the gate-to-source voltage reaches a specific magnitude (called the threshold voltage)
- Current control in an n-channel device is effected by a positive $V_{GS}$

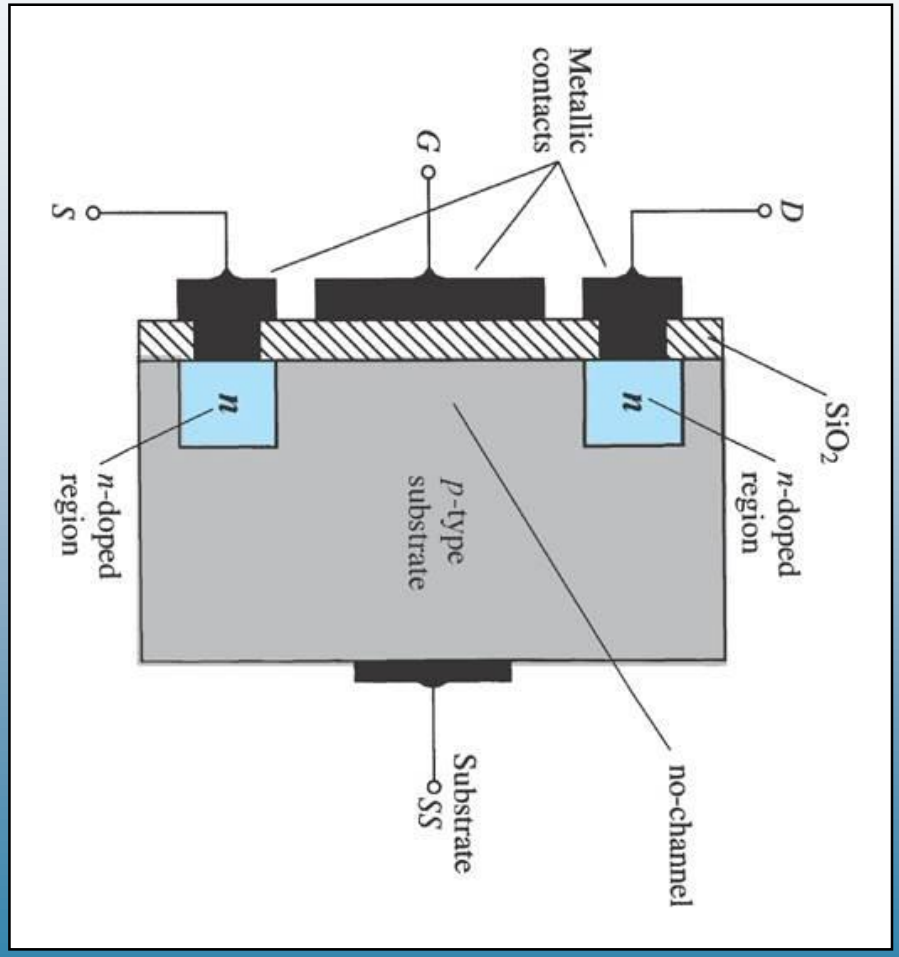
# E-Type MOSFET Construction

The **Drain (D)** and **Source (S)** connect to the to *n*-type regions.

The **Gate (G)** connects to the *p*-type substrate via a thin insulating layer of silicon dioxide ($SiO_2$)

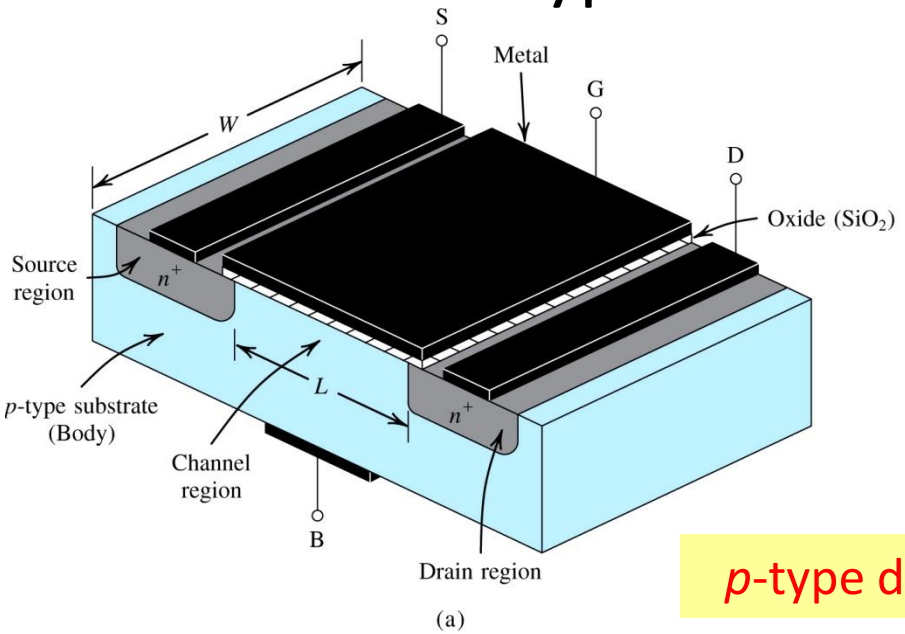
There is no channel!

The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the **Substrate (SS)**



# Device Structure ar

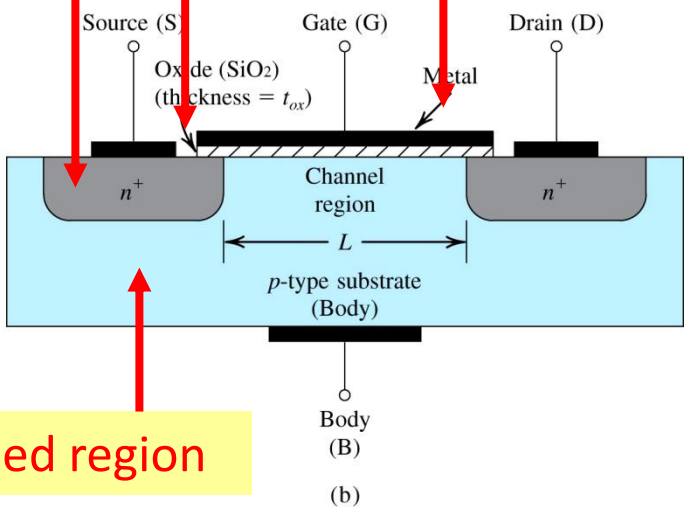
- The figure shows general structure of the *n*-channel enhancement-type MOSFET




two *n*-type doped regions (drain, source)

layer of $SiO_2$ separates source and drain

metal, placed on top of $SiO_2$, forms gate electrode

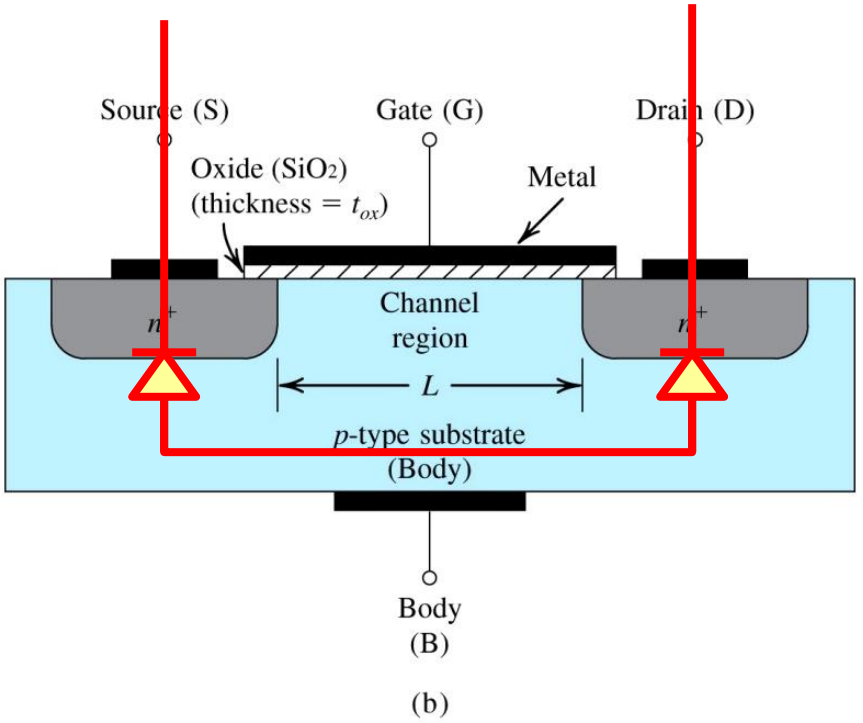



*p*-type doped region

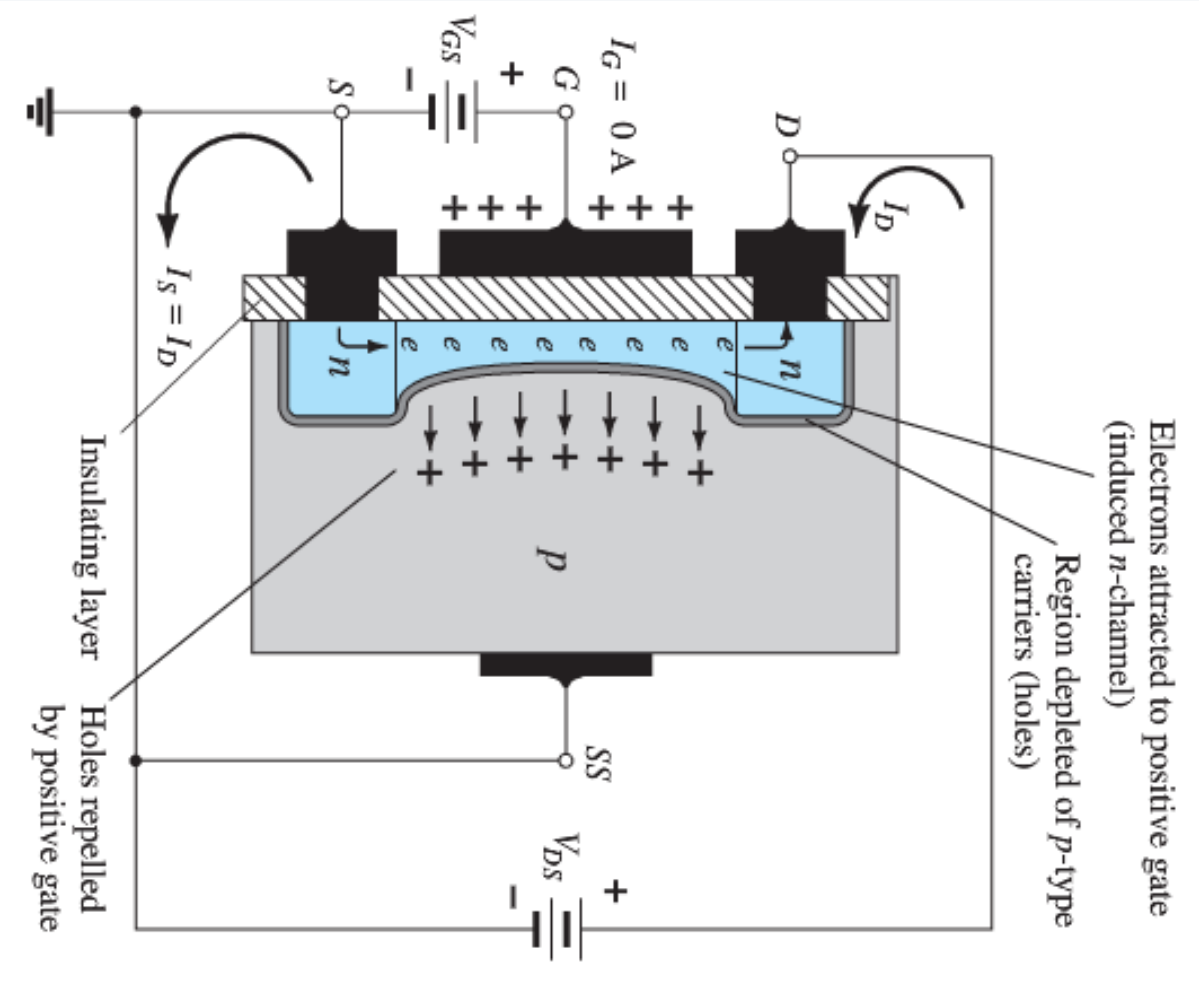
Typically L = 0.03*um* to 1*um*, W = 0.1*um* to 100*um*, and the thickness of the oxide layer ($t_{ox}$) is in the range of 1 to 10*nm*.

# Operation with Zero Gate Voltage

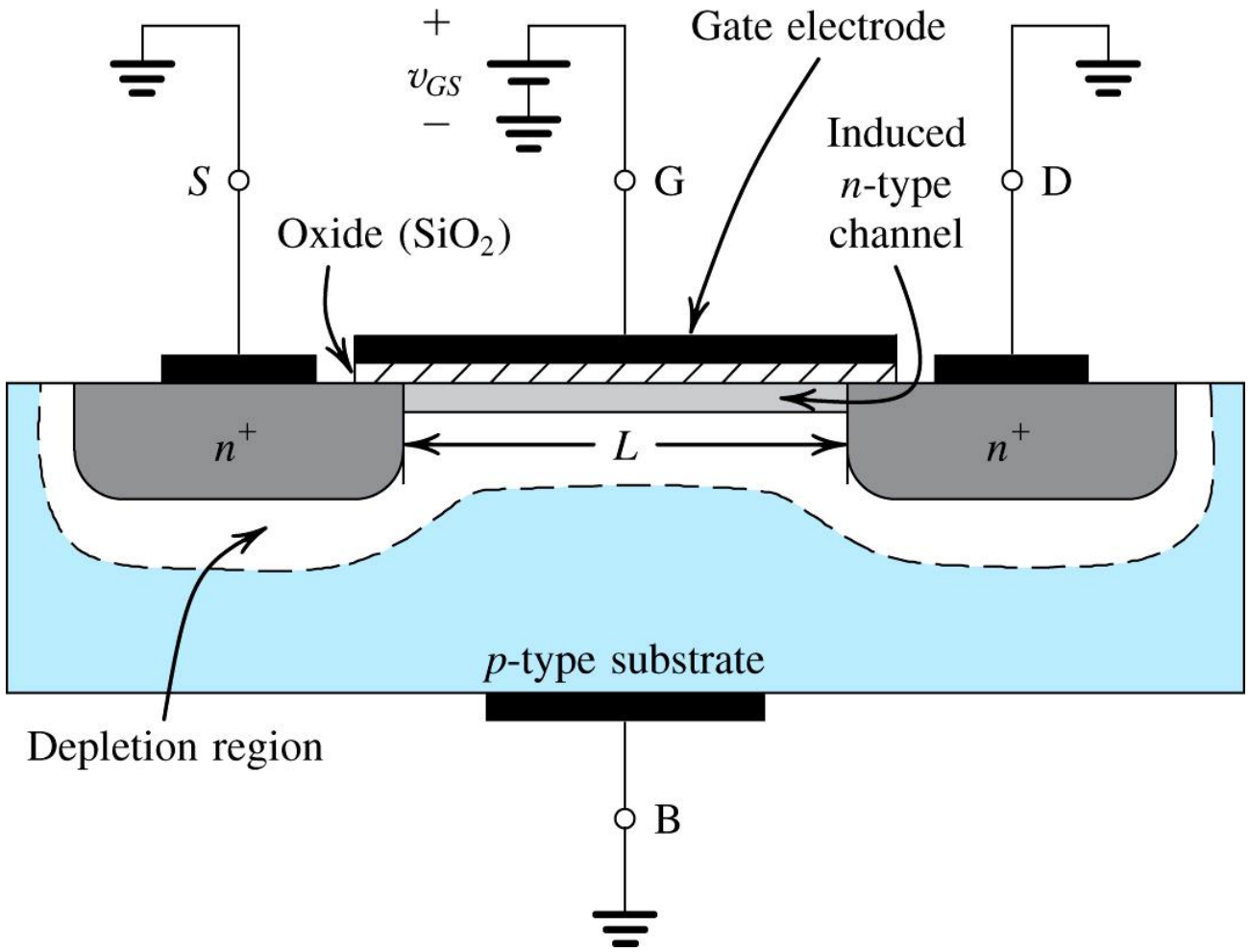
- With zero voltage applied to gate, two back-to-back diodes exist in series between drain and source.
  - Both in reverse-biased condition
- "They" prevent current conduction from drain to source when a voltage $v_{DS}$ is applied.
  - yielding very high resistance ($10^{12}$*ohms*)



# Channel formation in the n-channel enhancement-type MOSFET



# The enhancement-type NMOS transistor with a positive voltage applied to the gate




An *n* channel is induced at the top of the substrate beneath the gate

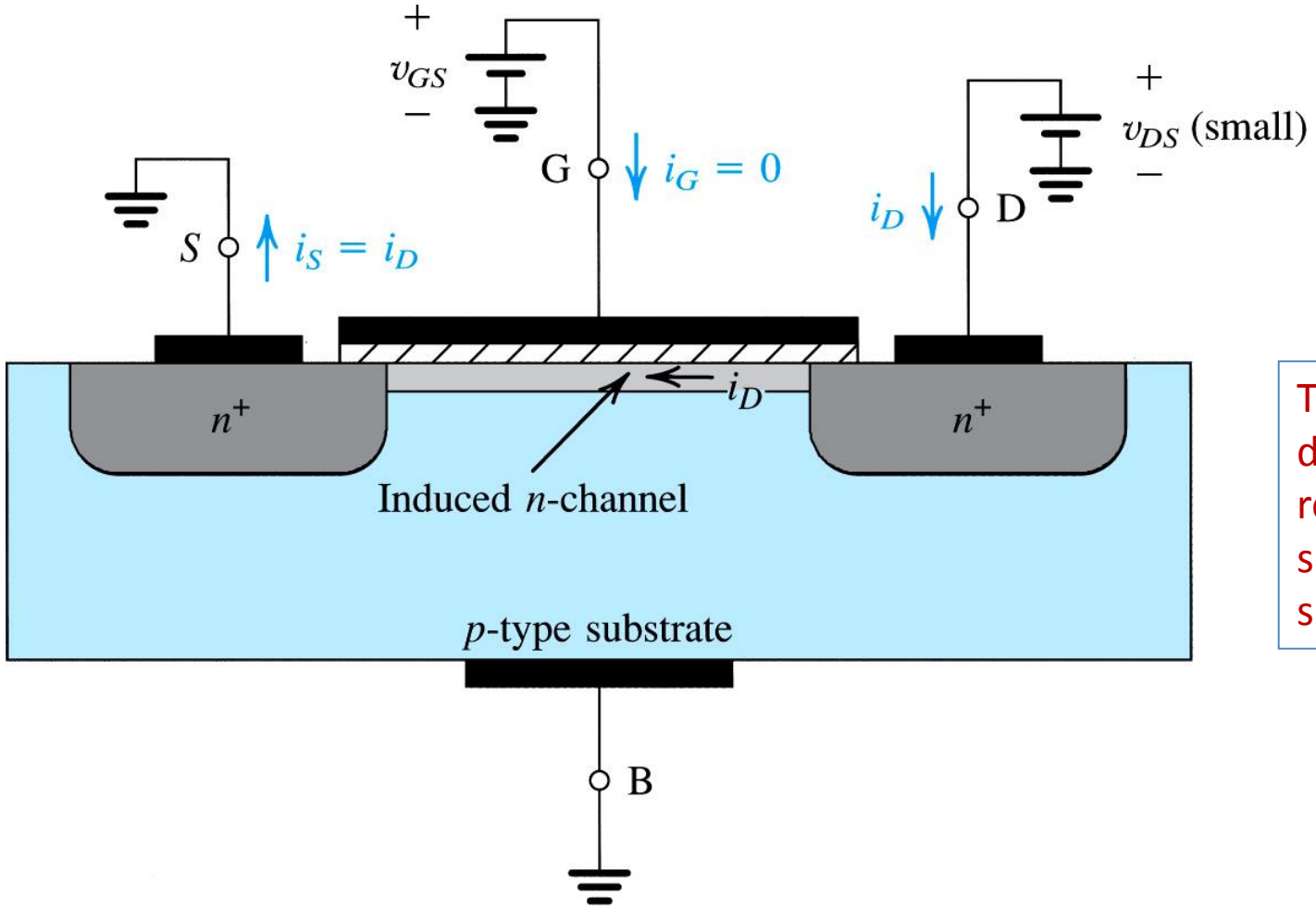
# Threshold Voltage, $V_t$

- The value of  at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage
  - Denoted as $V_t$
  - Positive for an n-channel FET
- The value is controlled during device fabrication
  - Typically $V_t$ lies in the range of 0.3 V to 1.0 V

# Field-Effect

- The gate and the channel region of the MOSFET form a parallel-plate capacitor
  - The oxide layer acts as the capacitor dielectric
- The channel conductivity and the current that flows through the channel is determined by the electric field in the channel
  - Caused by an applied gate voltage
  - This is  the origin of the name “field-effect transistor” (FET)
- A current flows when a voltage $v_{DS}$ is applied

# An NMOS transistor with vGS > Vt and with a small vDS applied




The depletion region is not shown (for simplicity)

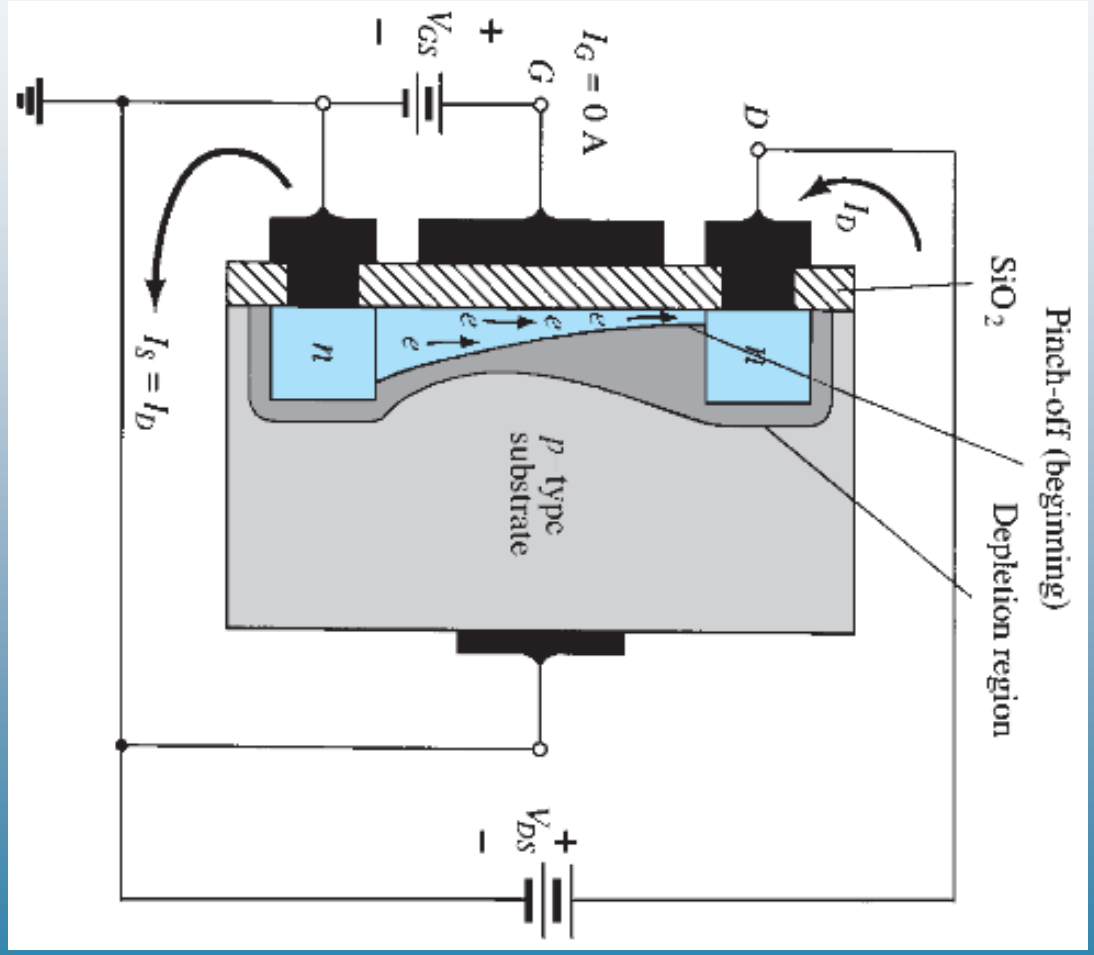
- The device acts as a resistance whose value is determined by $v_{GS}$
- The channel conductance $g_{DS}$ is proportional to $v_{GS} - V_t$

# Summary of MOSFET Behavior (when $v_{DS}$ is kept small)

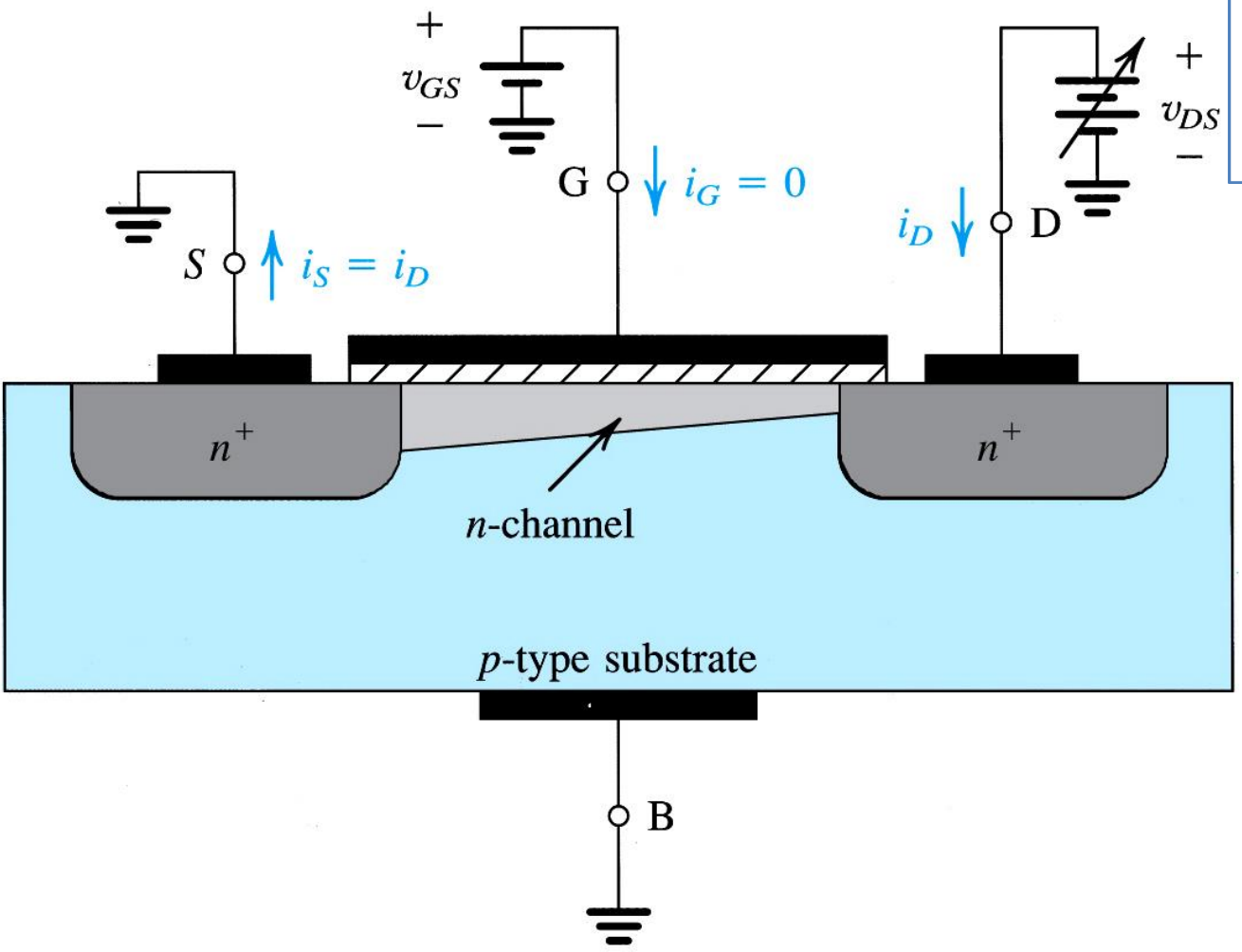
- MOSFET behaves as a linear resistance whose value is controlled by the gate voltage $v_{GS}$
- For MOSFET to conduct, a channel has to be induced.
- Then, increasing above the threshold voltage $V_t$ enhances the channel
  - Hence the names **enhancement-mode operation** and **enhancement-type MOSFET**.
- The current that leaves the source terminal ($i_S$) is equal to the current that enters the drain terminal ($i_D$), and the gate current $i_G = 0$

# Change in channel and depletion region with increasing level of $V_{DS}$ for a fixed value of $V_{GS}$

$$V_{DG} = V_{DS} - V_{GS}$$



# Operation of the enhancement NMOS transistor as $v_{DS}$ is increased

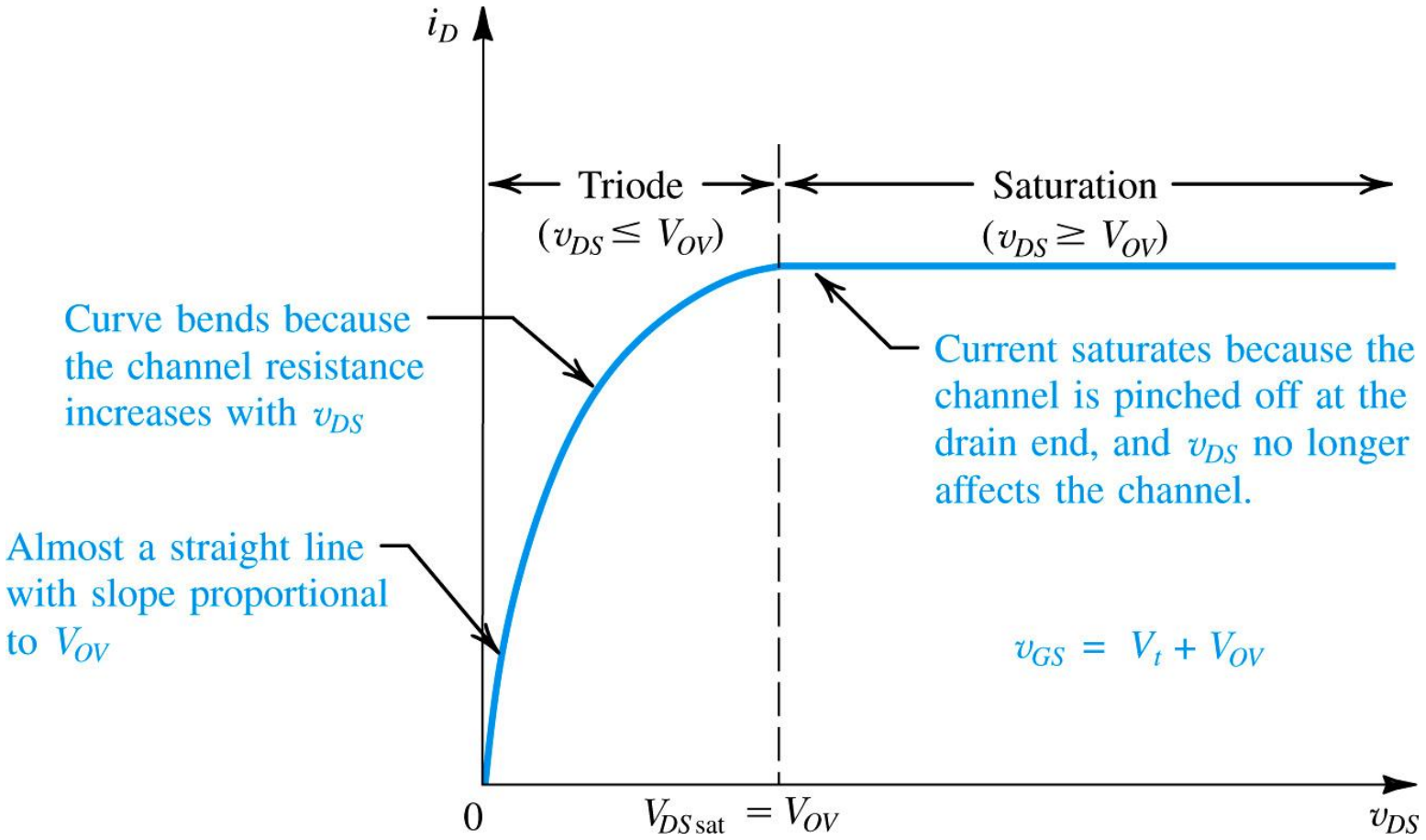



- $v_{GS}$ is kept constant at a value $> V_t$
- $v_{GS} = V_t + V_{OV}$

The induced channel acquires a tapered shape, and its resistance increases as $v_{DS}$ is increased.

# $i_D$ versus $v_{DS}$
# [Enhancement-Type NMOS Transistor]

$$v_{GS} = V_t + V_{OV}$$



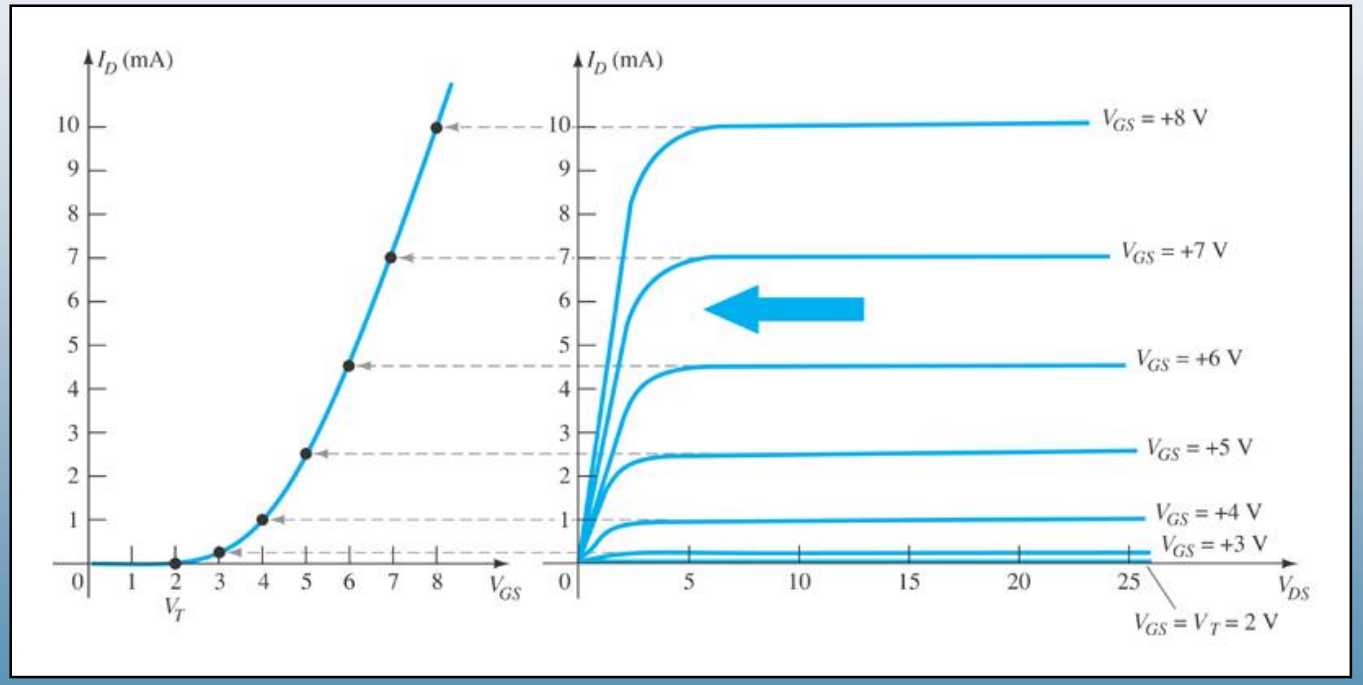
# E-Type MOSFET Operation

*The enhancement-type MOSFET (E-MOSFET) operates only in the enhancement mode.*

$V_{GS}$ is always positive

As $V_{GS}$ increases, $I_D$ increases

As $V_{GS}$ is kept constant and $V_{DS}$ is increased, then $I_D$ saturates ($I_{DSS}$) and the saturation level ($V_{DSsat}$) is reached



# E-Type MOSFET Transfer Curve

To determine $I_D$ given $V_{GS}$:

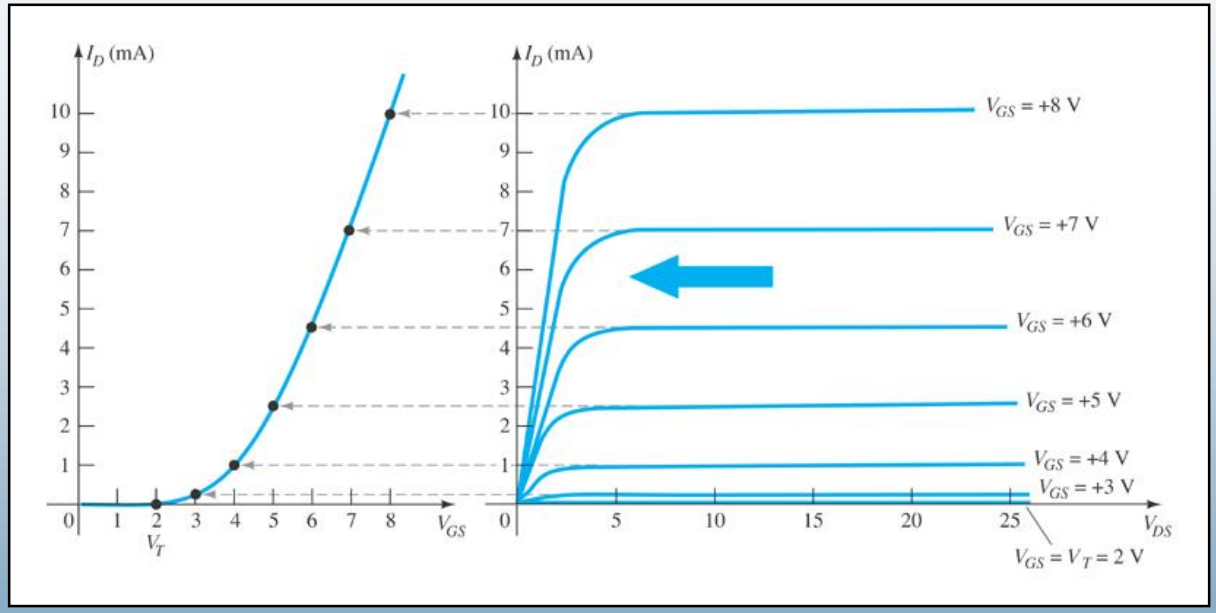
$$I_D = k(V_{GS} - V_T)^2$$

where:

$V_T$ = the E-MOSFET threshold voltage

$k$, a constant, can be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$



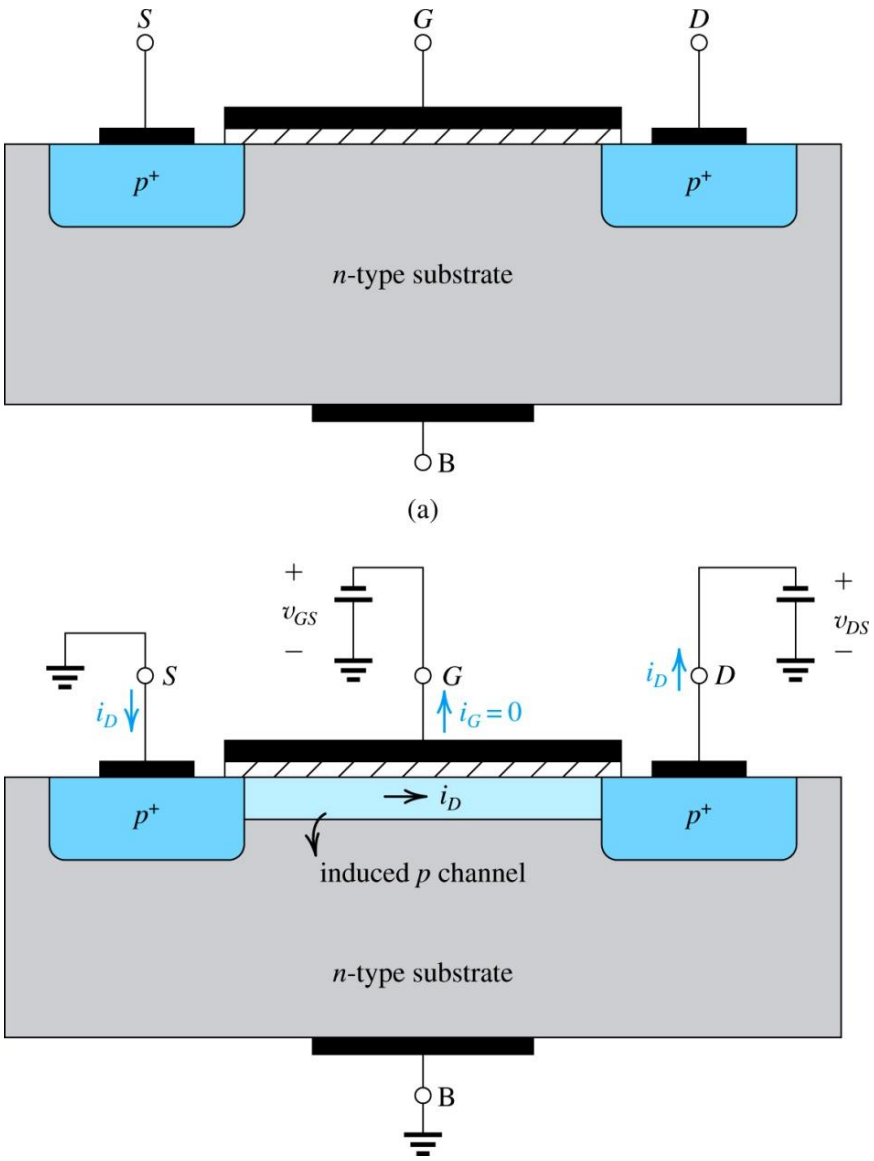

$V_{DSsat}$ can be calculated using:

$$V_{DSsat} = V_{GS} - V_T$$

# Operation of MOSFET at Saturation

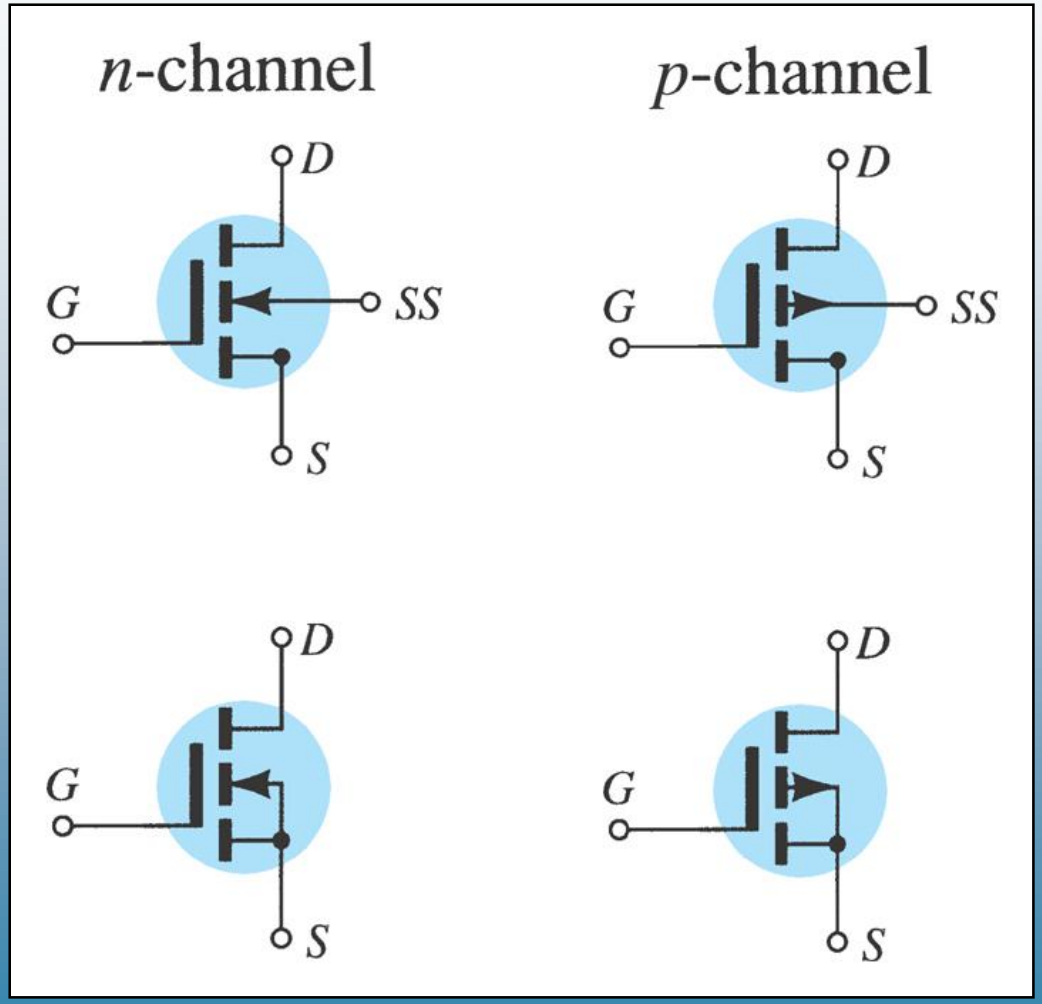
- Channel pinch-off does not mean channel blockage
- Current continues to flow through the pinched-off channel
- Electrons that reach the drain end of the channel are accelerated through the depletion region that exists there and into the drain terminal.

# PMOS transistors




- Similar to the NMOS transistor
  - except that all semiconductor regions are reversed in polarity

# MOSFET Symbols



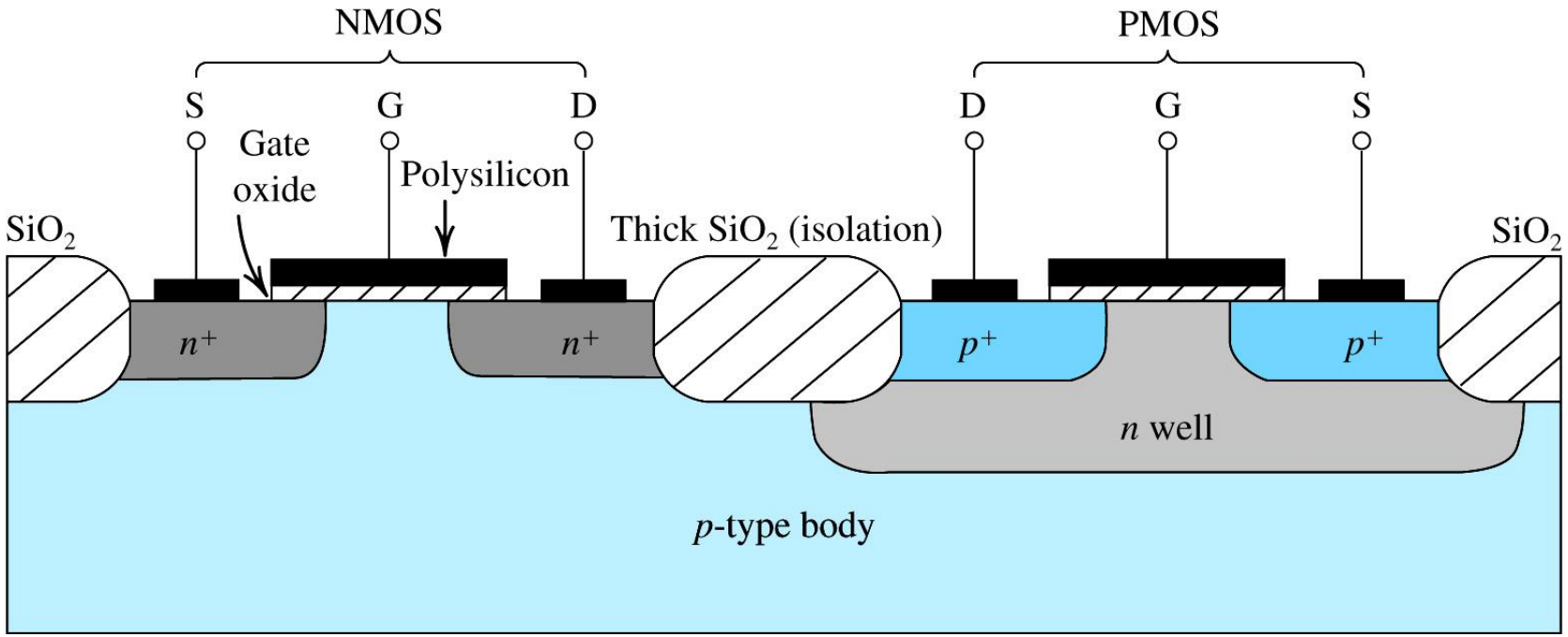

- The symbols try to reflect the actual construction of the device.
- The dashed line between drain and source is chosen to reflect the fact that a channel does not exist between the two under no-bias conditions.
- It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.

# Complementary MOS or CMOS

- CMOS is the most widely used of all the IC technologies
  - Applies to both analog and digital circuits
- Uses both NMOS and PMOS
- Reasons for CMOS displacing bipolar technology in digital applications:
  - CMOS logic circuits dissipate less power.
  - MOS transistors offer higher input impedance.
  - The size of MOS transistors has been reduced drastically in recent past, more so than bipolar technologies.
- Somewhat more difficult to fabricate than NMOS

# CMOS Devices

*CMOS (complementary MOSFET) uses a p-channel and n-channel MOSFET; often on the same substrate.*




- **Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well**

# Digital Logic Inverters

- Most basic element in design of digital circuits.

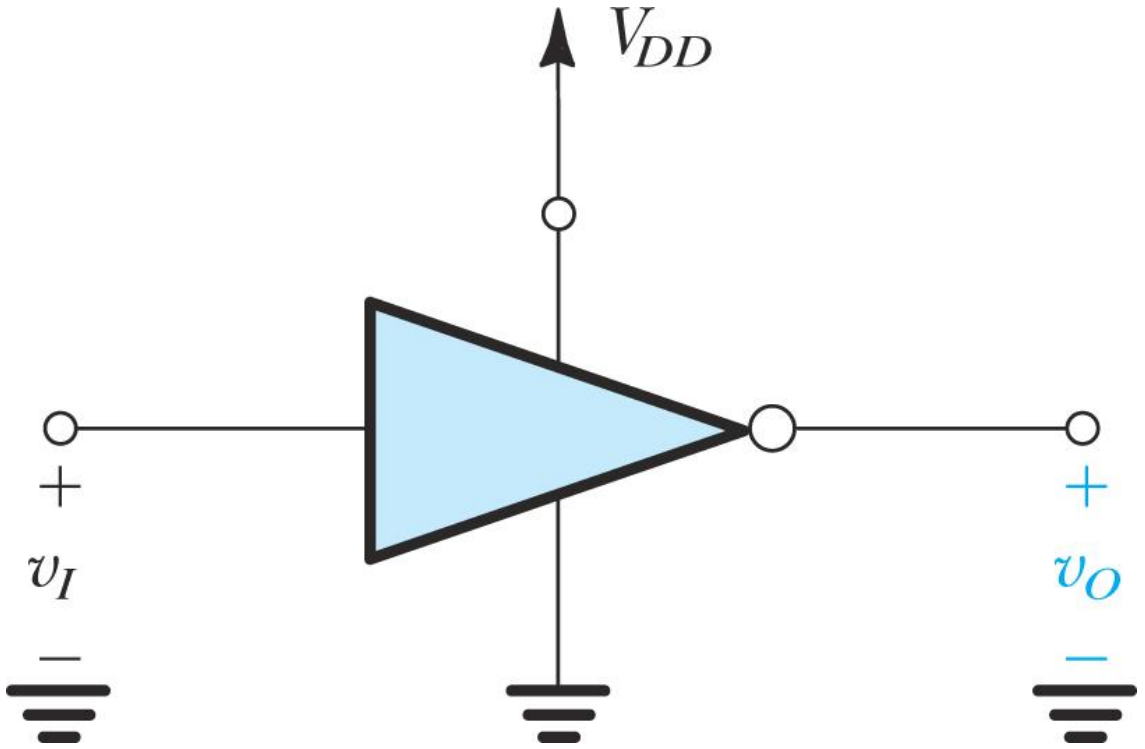
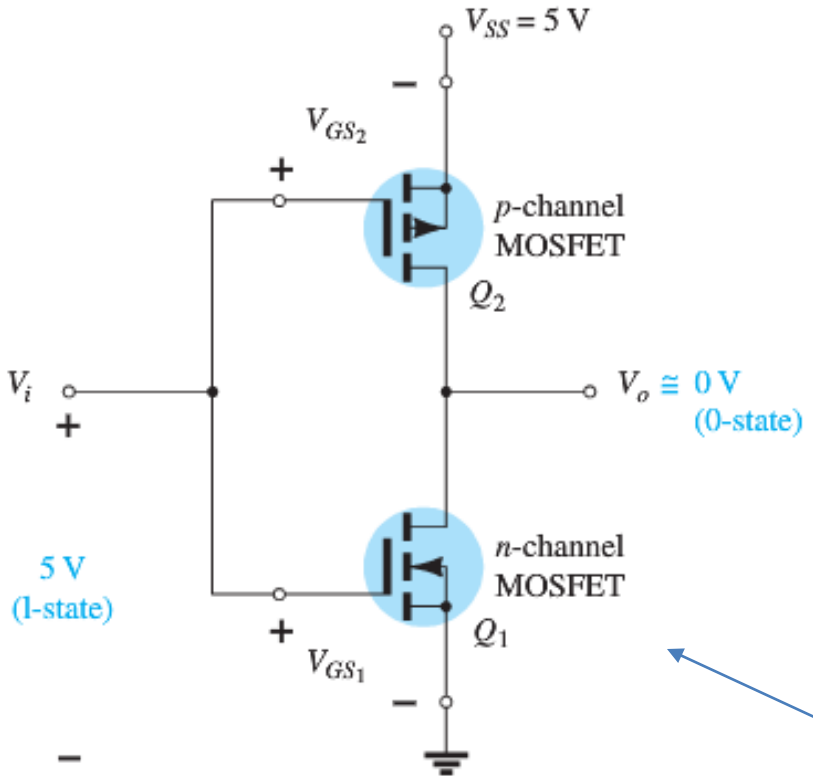
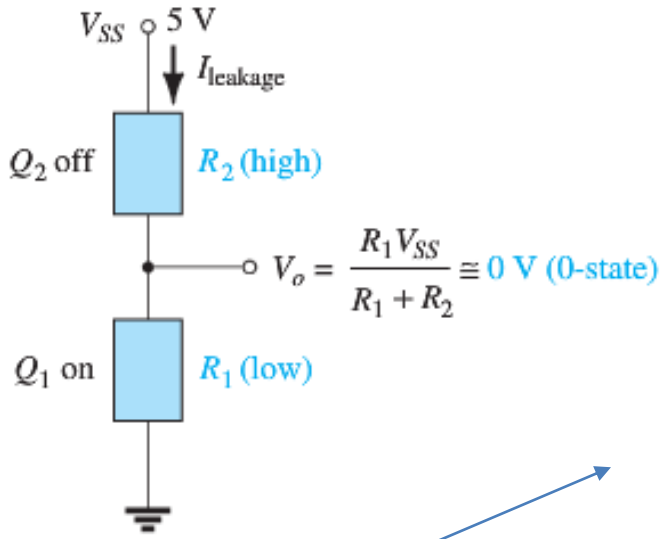
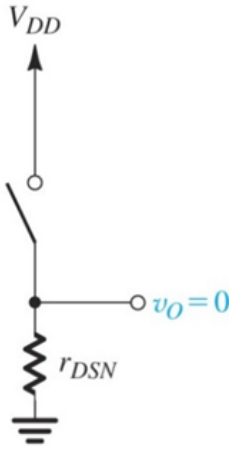


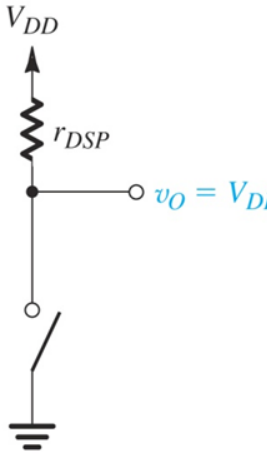

Figure: A logic inverter operating from a dc supply $V_{DD}$.

# CMOS Logic Design: CMOS Inverter



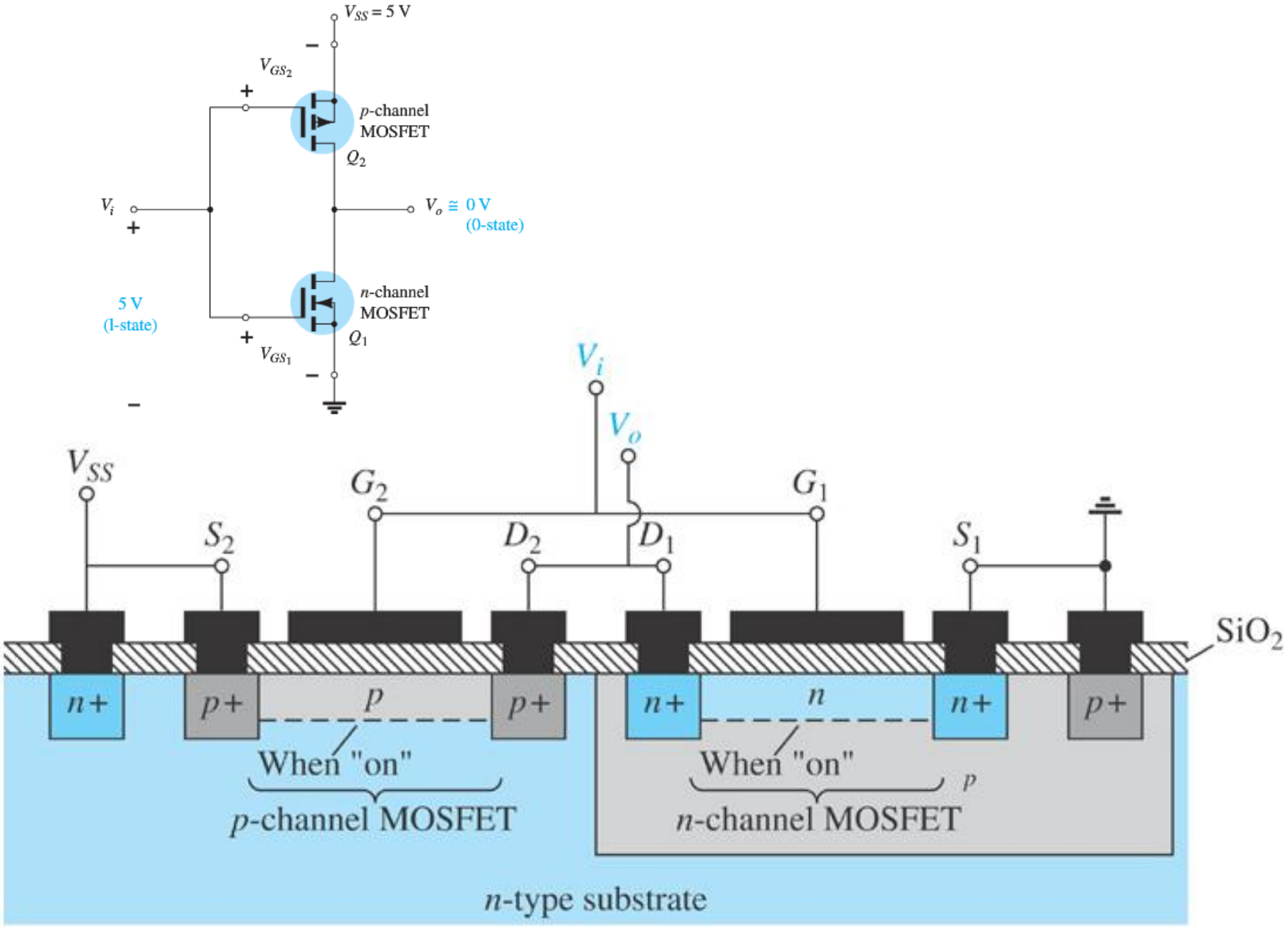



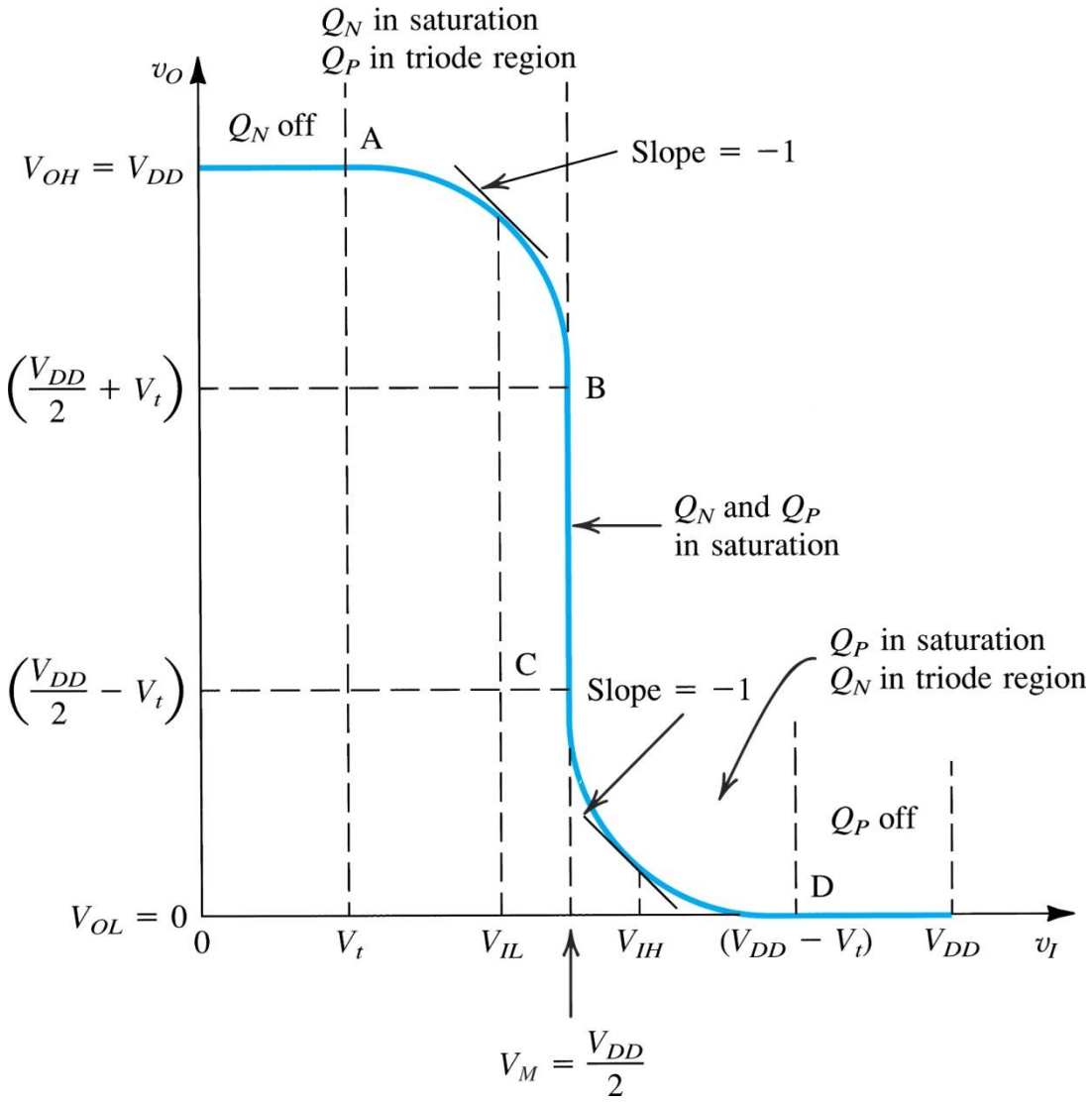

Input 1, Output 0

Input 0, Output 1

# CMOS Logic Design: CMOS Inverter

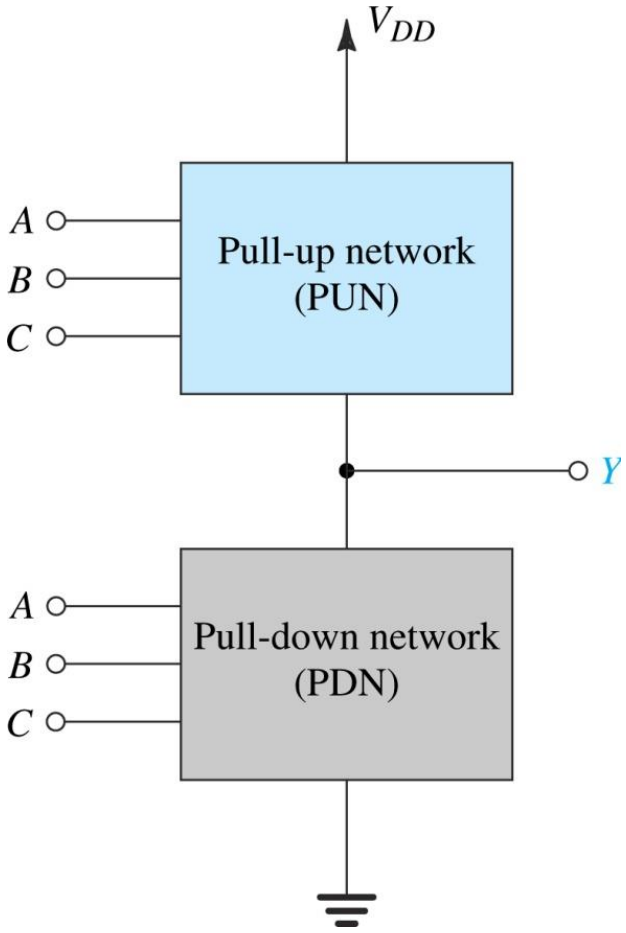


# The voltage-transfer characteristic of the CMOS inverter when $Q_N$ and $Q_P$ are matched.



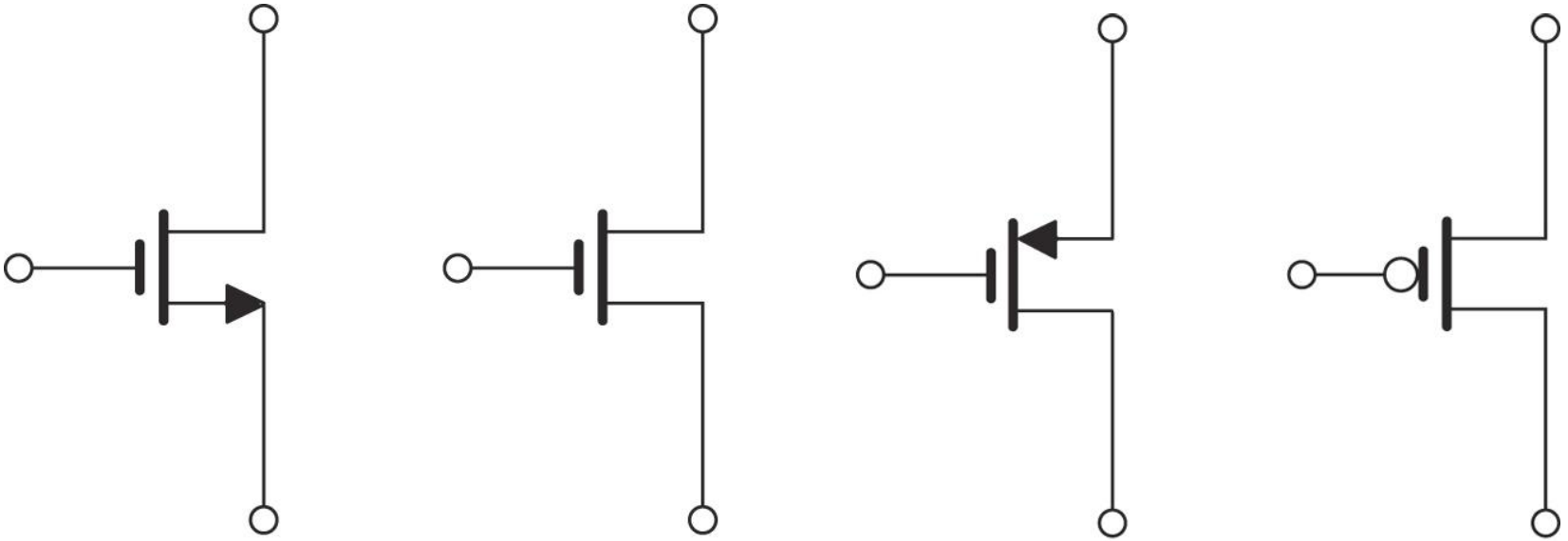
# Basic Architecture of CMOS Logic-Gate Circuits

- The digital logic inverter is the basic building block of digital circuits, just as the amplifier is the basic building block of analog circuits.
- Other CMOS logic gates are extension of the inverter.
  - NMOS pull-down transistor / network
  - PMOS pull-up transistor / network
- These two networks are operated by input variables in an complementary fashion.

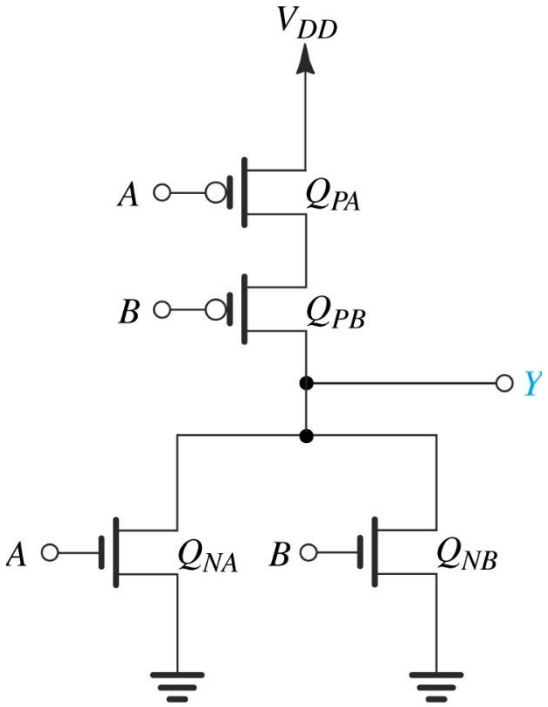



Representation of a three-input CMOS logic gate

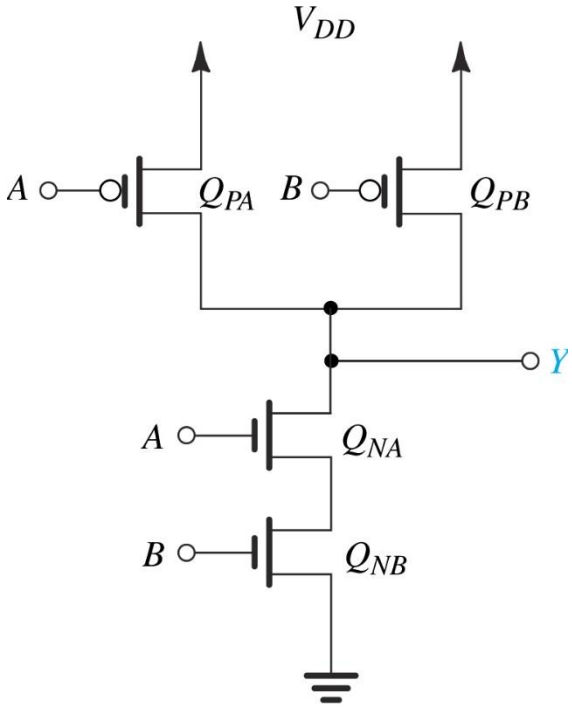
# Alternate symbols for MOSFETs. (Used mostly for digital circuits)



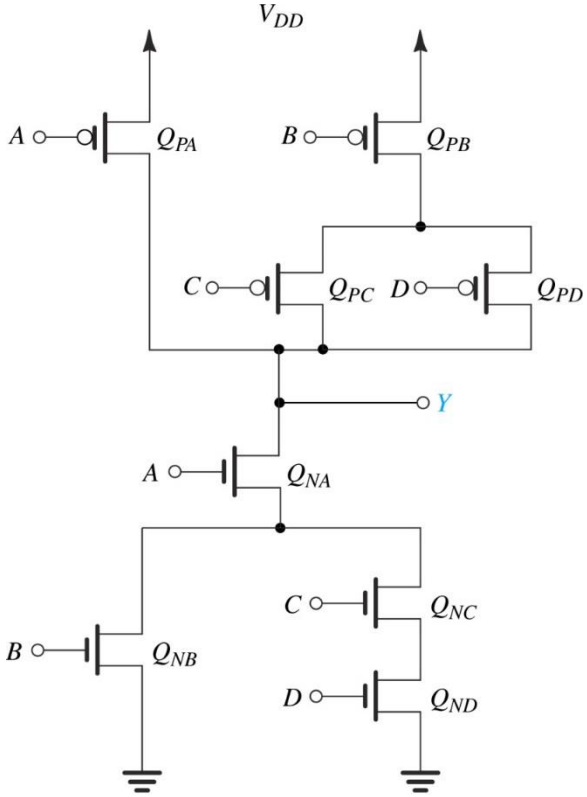
NMOS PMOS




$Y = \overline{A + B}$




$Y = \overline{AB}$




$Y = \overline{A(B + CD)}$

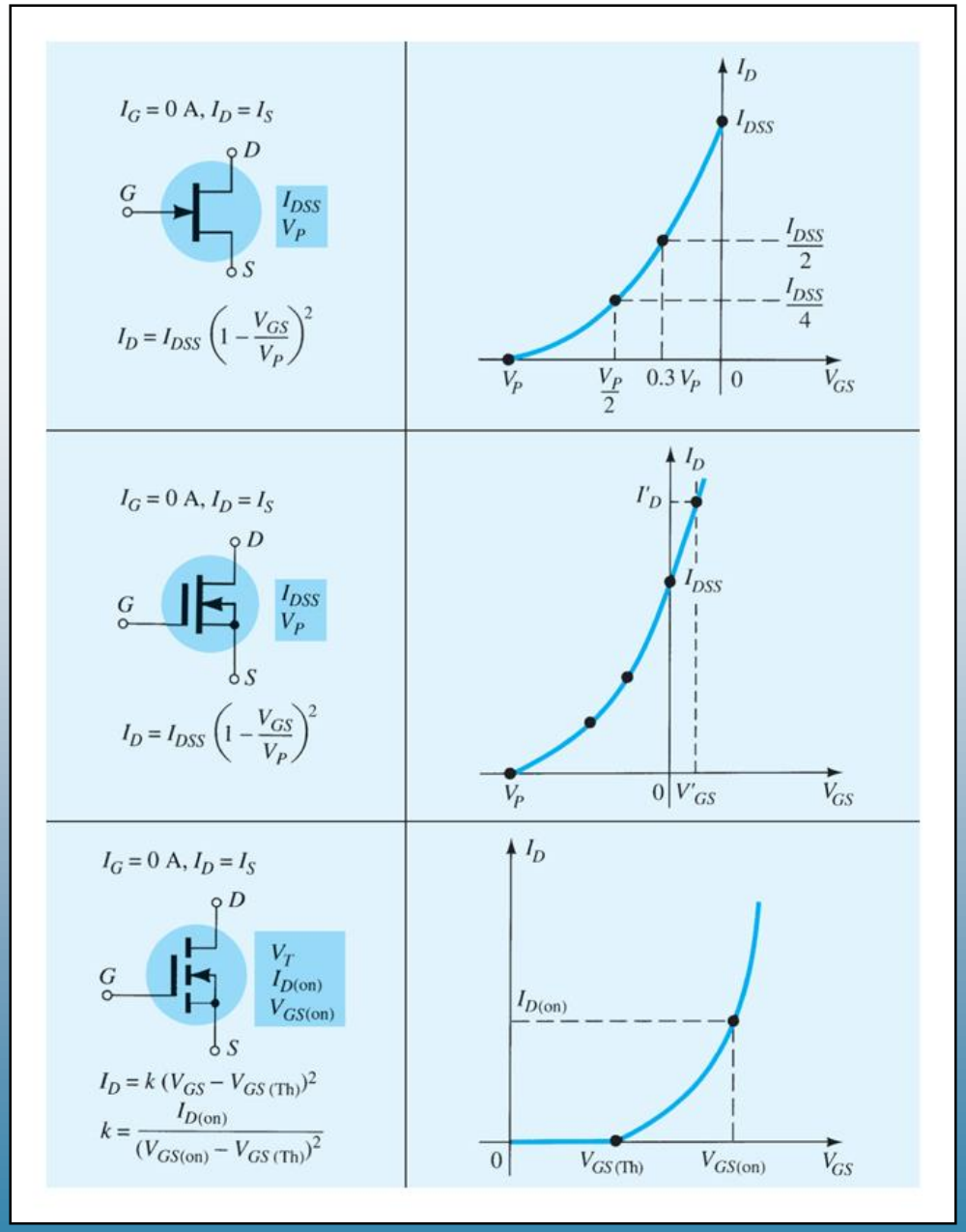
# Power and Speed

- An important performance parameter of the inverter is the amount of power it dissipates
- There are two components of power dissipation: static and dynamic.
  - The first is the result of current flow in either the 0 or 1 state (or both).
  - The second occurs when the inverter is switched and has a capacitor load *C*.
    - Dynamic power dissipation $P_{dyn} = fCV_{DD}^2$.
- The speed of operation of the inverter is characterized by its propagation delay ($t_P$).

# CMOS Summary

- Predominantly because of its lower power dissipation and good scalability, CMOS is by far the more dominant transistor technology for utilization in logic gate design.
- Digital IC's usually utilize the minimum channel length of technology available.

# Summary Table

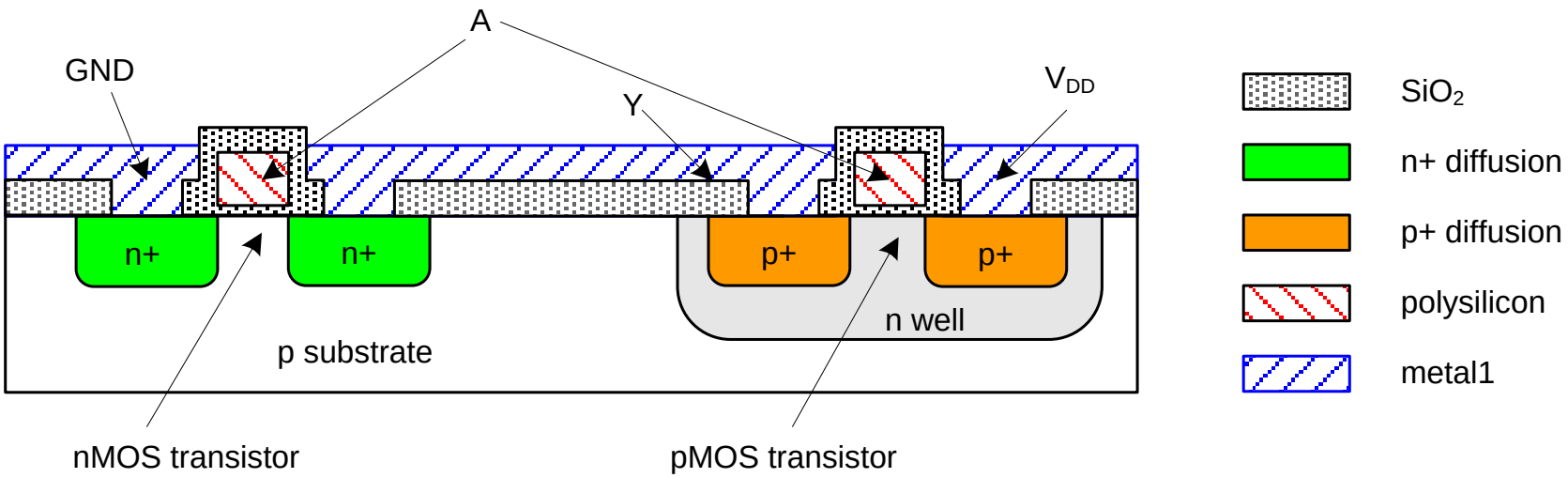


# CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

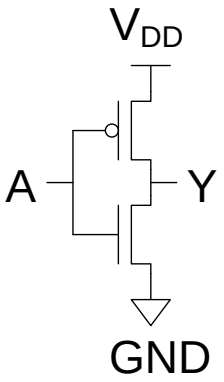
# Inverter Cross-section

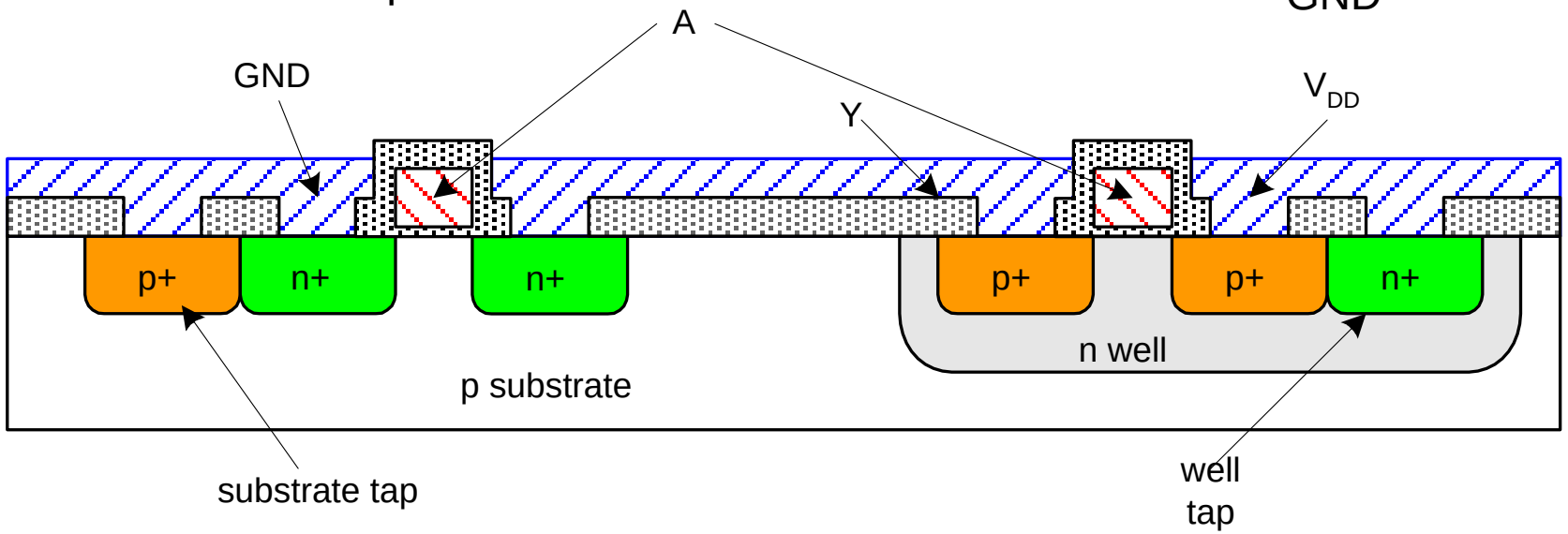
- p-type substrate is more common
- Requires n-well for body of pMOS transistors



# Well and Substrate Taps

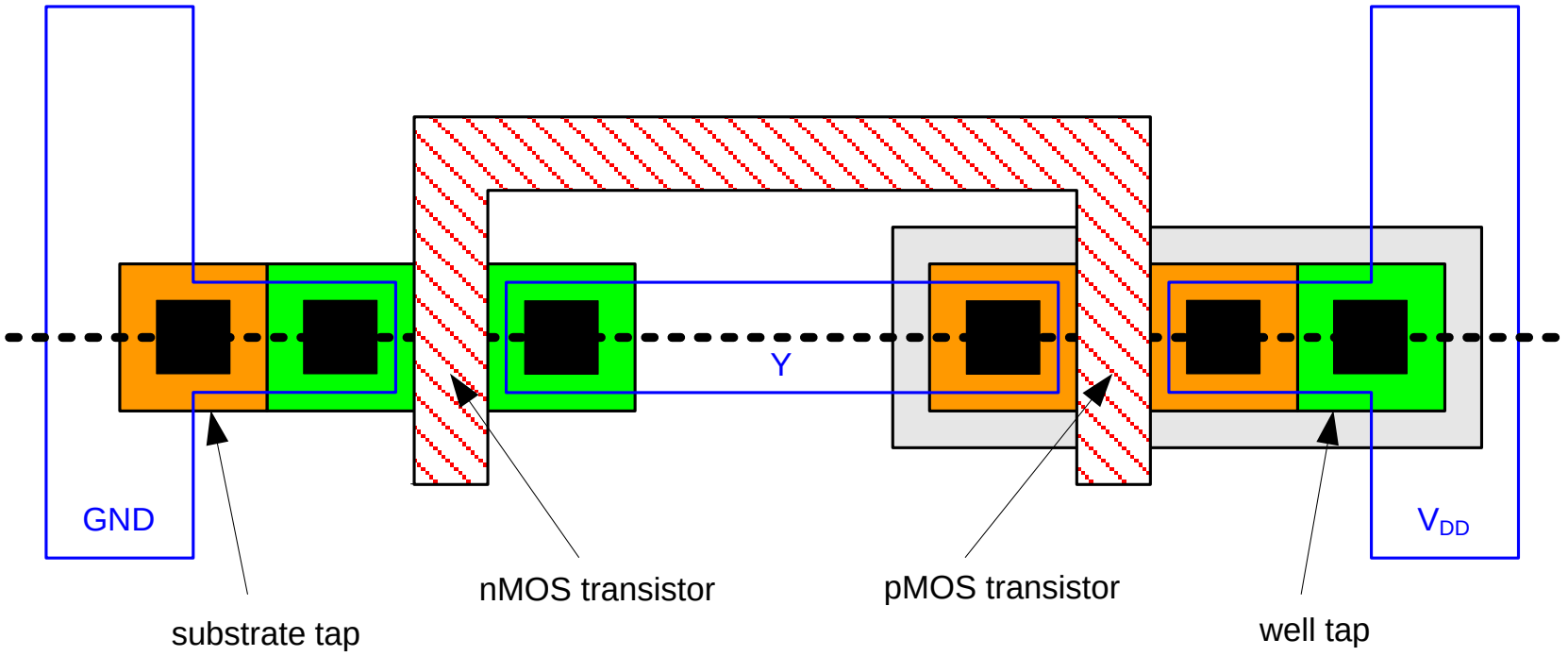
- Substrate must be tied to GND and n-well to $V_{DD}$
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



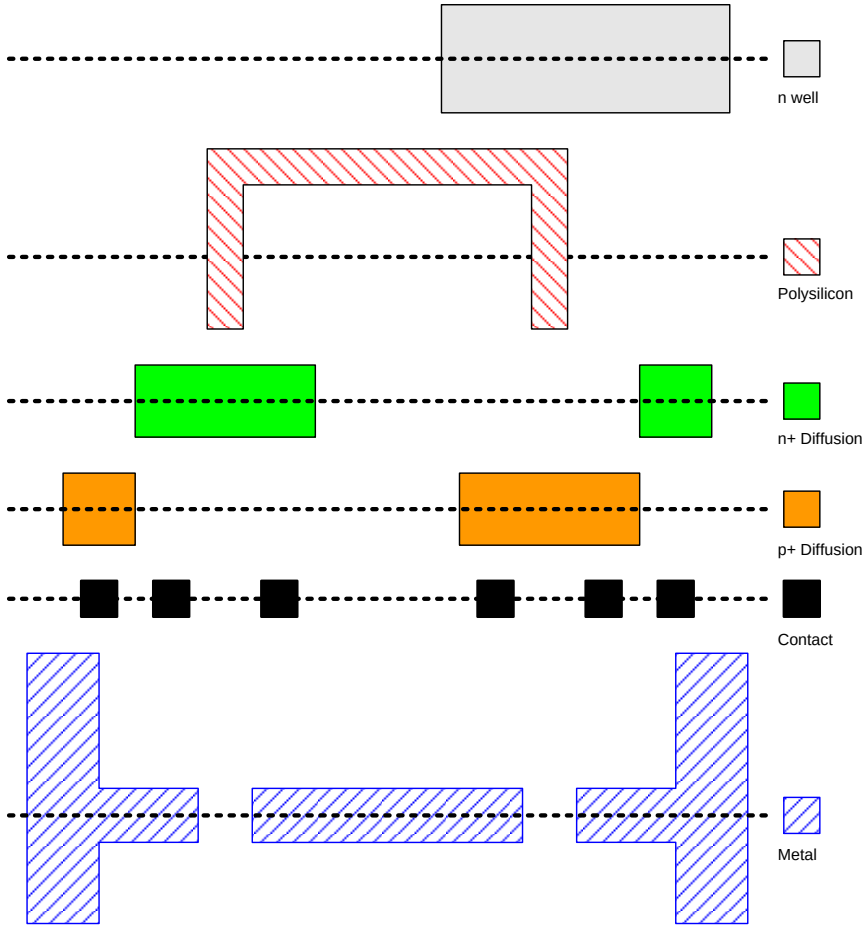
# Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



# Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



# Fabrication

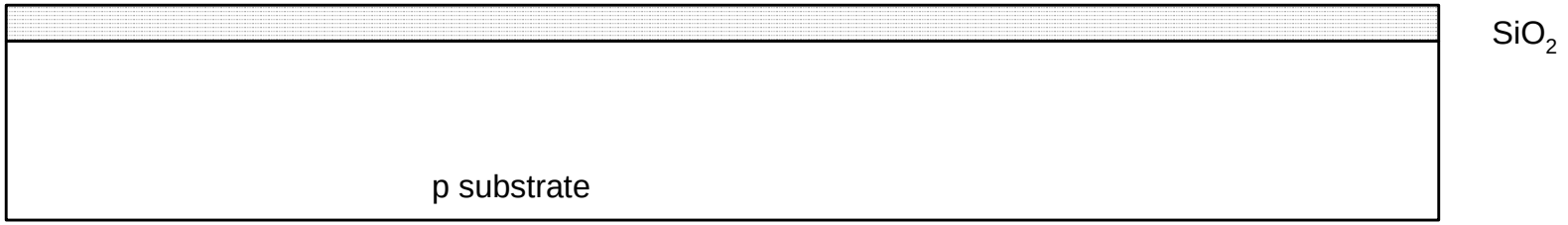
- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

# Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of $SiO_2$ (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off $SiO_2$

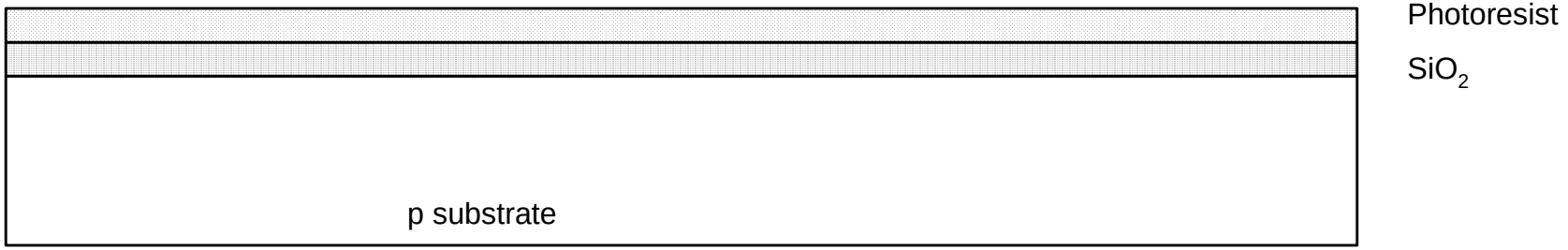
# Oxidation

- Grow $SiO_2$ on top of Si wafer
  - 900 – 1200 C with $H_2O$ or $O_2$ in oxidation furnace



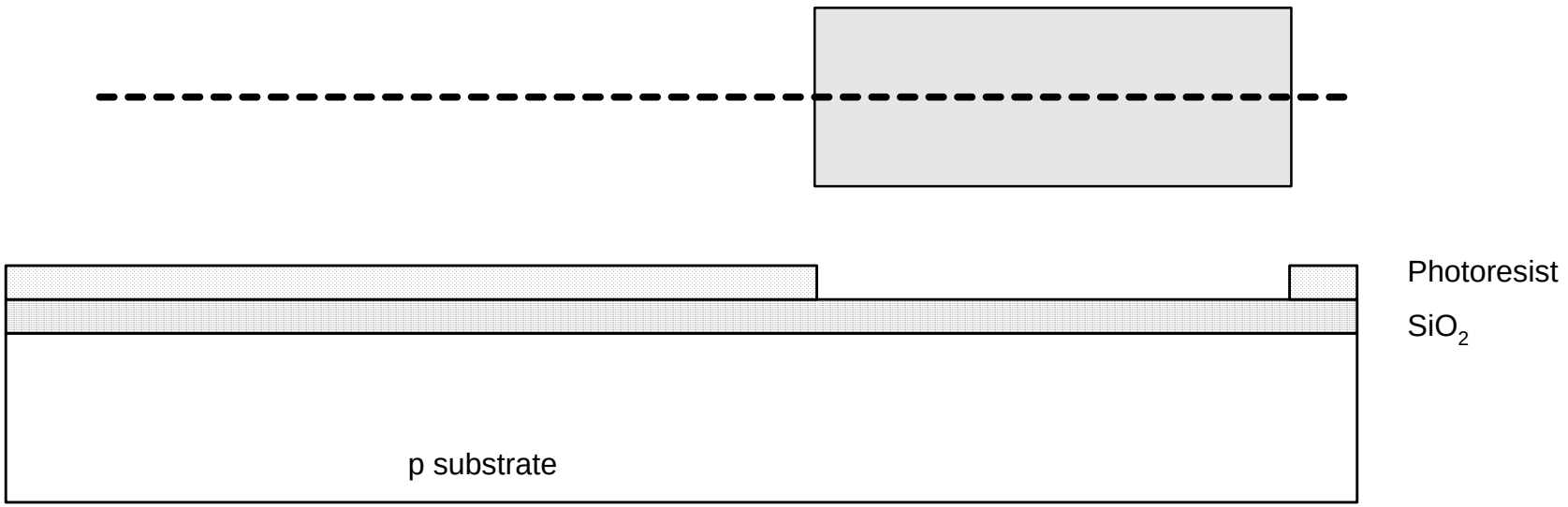
# Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



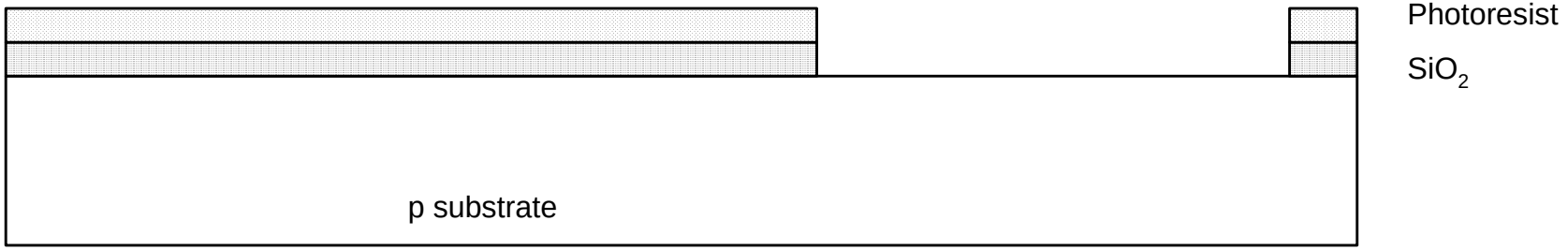
# Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



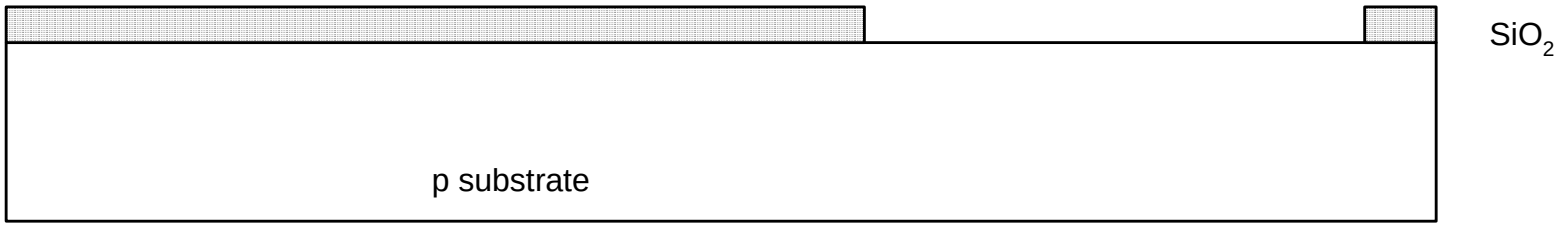
# Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



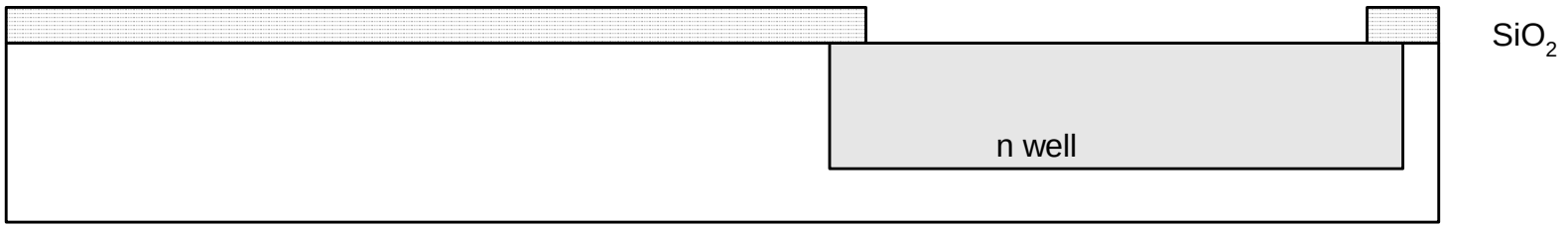
# Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



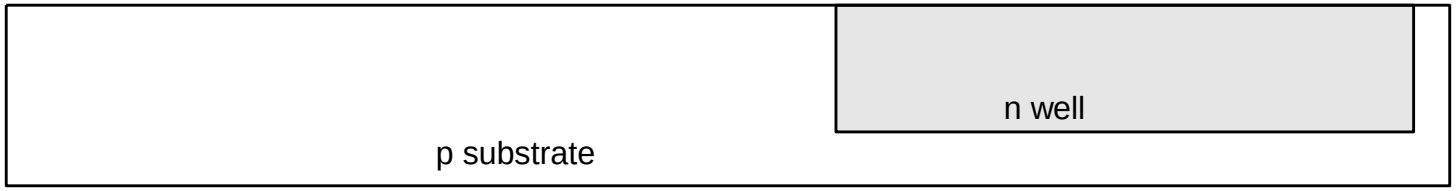
# n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implanatation
  - Blast wafer with beam of As ions
  - Ions blocked by $SiO_2$, only enter exposed Si



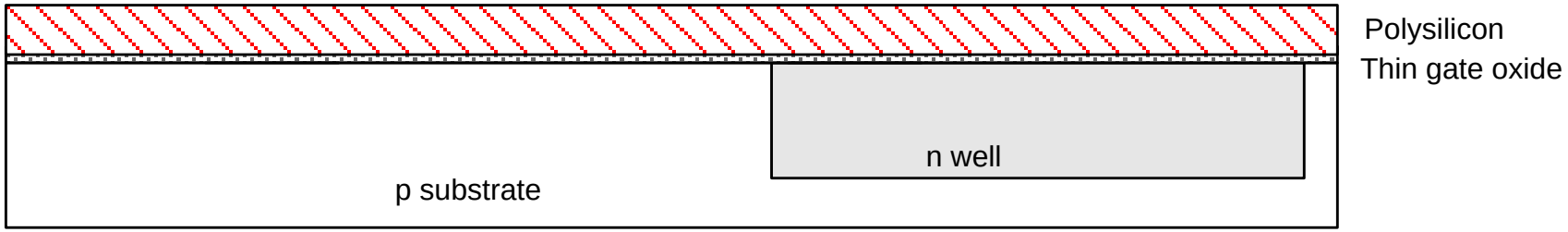
# Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



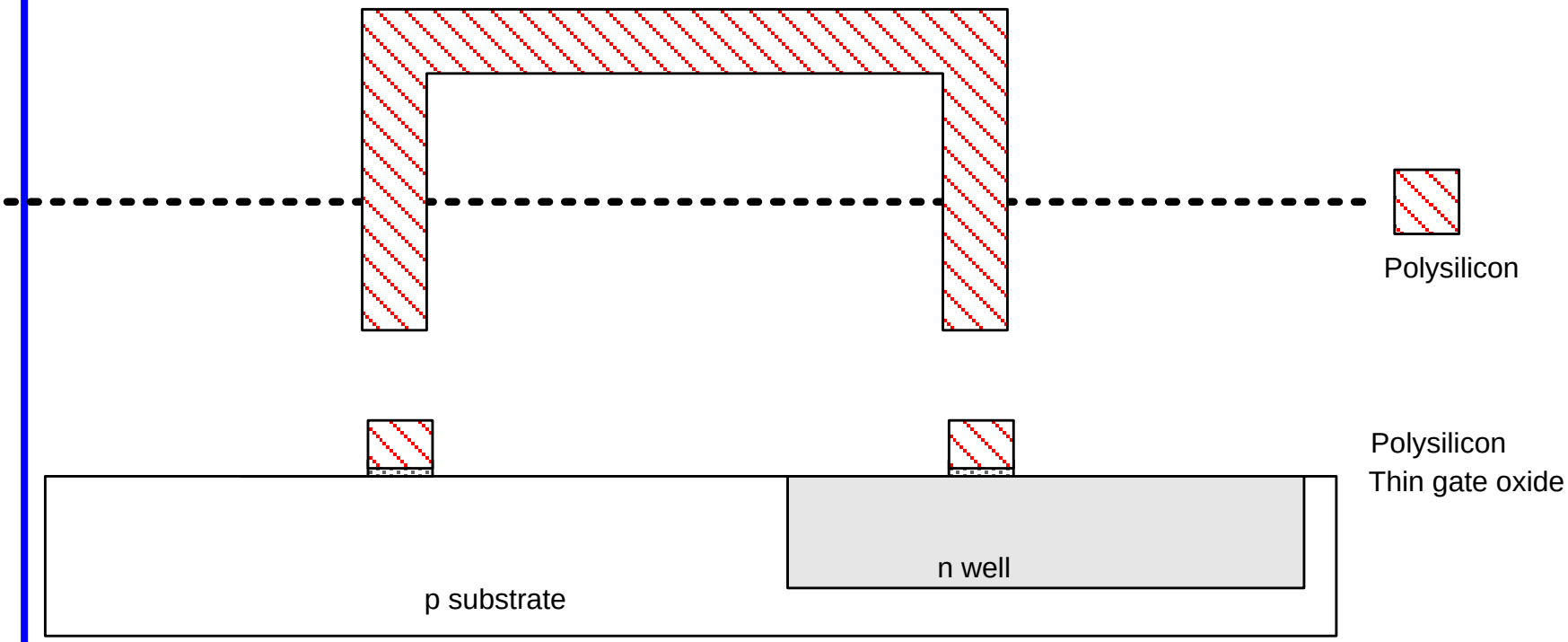
# Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas ($SiH_4$)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



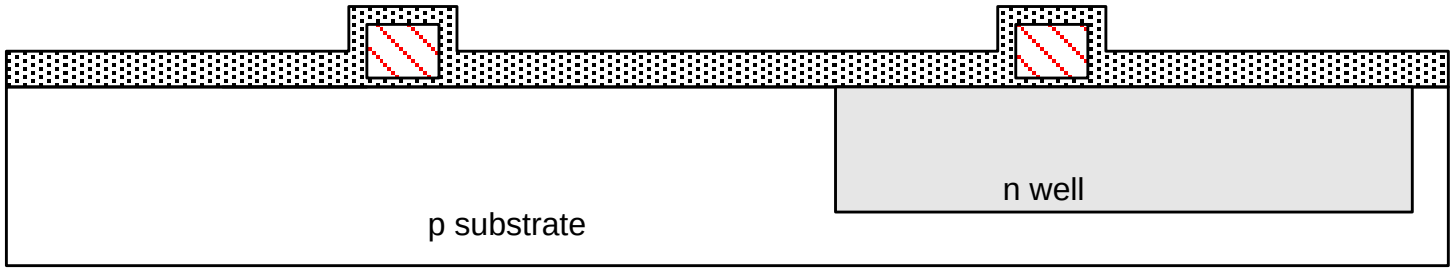
# Polysilicon Patterning

- Use same lithography process to pattern polysilicon



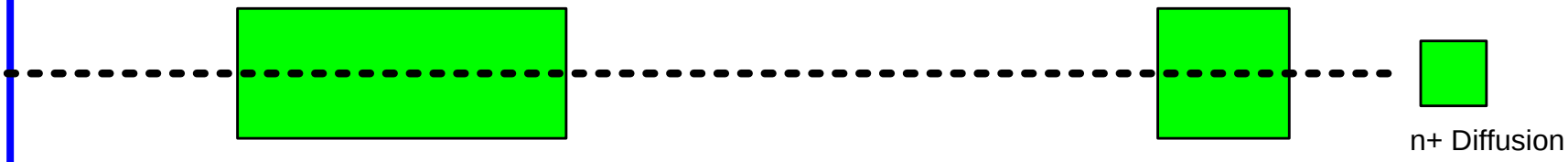
# Self-Aligned Process

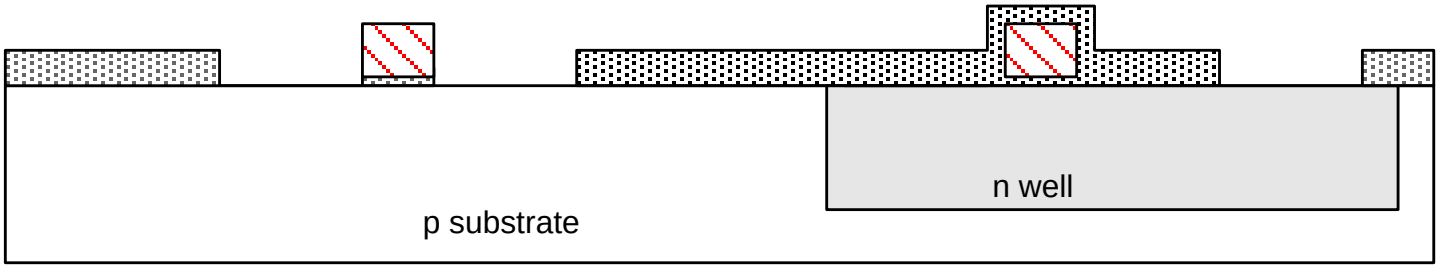
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



# N-diffusion

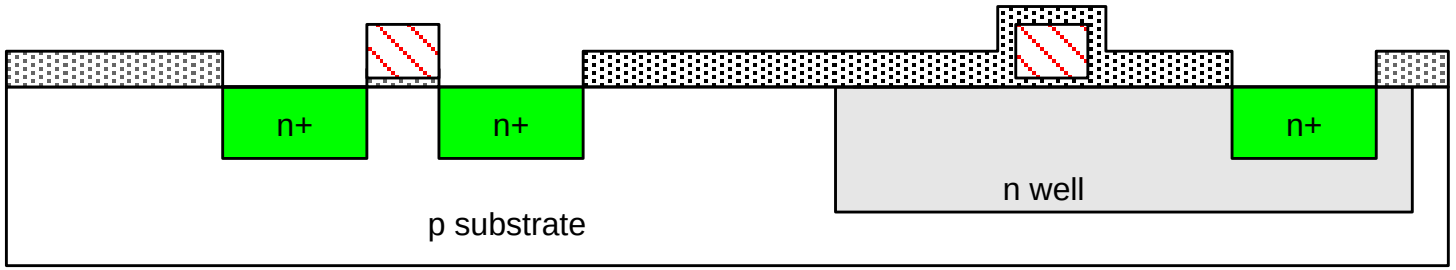
- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



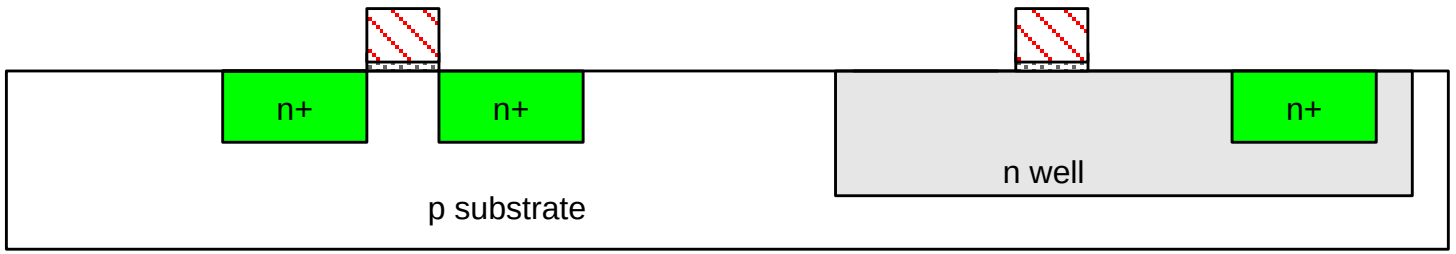
# N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



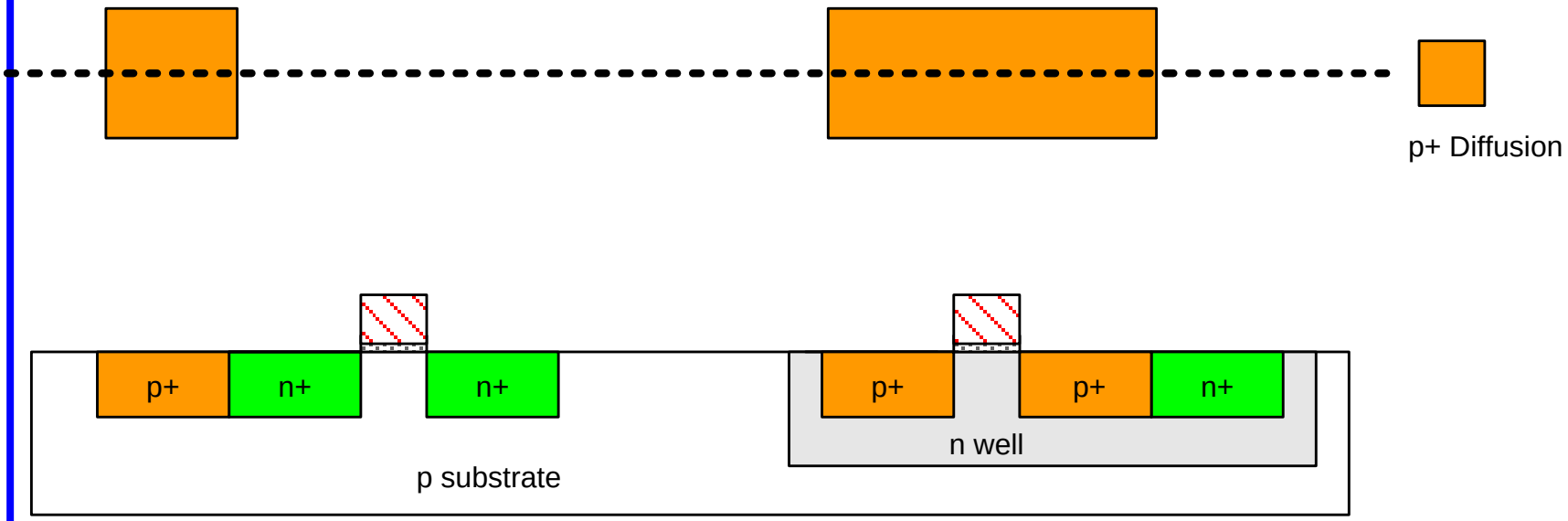
# N-diffusion cont.

- Strip off oxide to complete patterning step



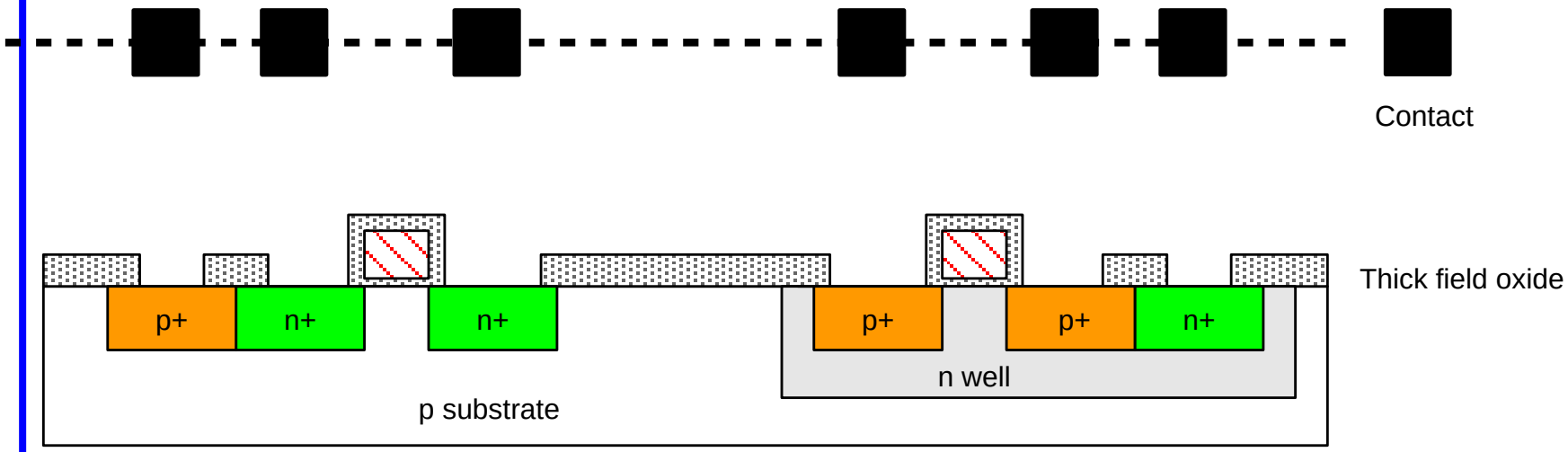
# P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



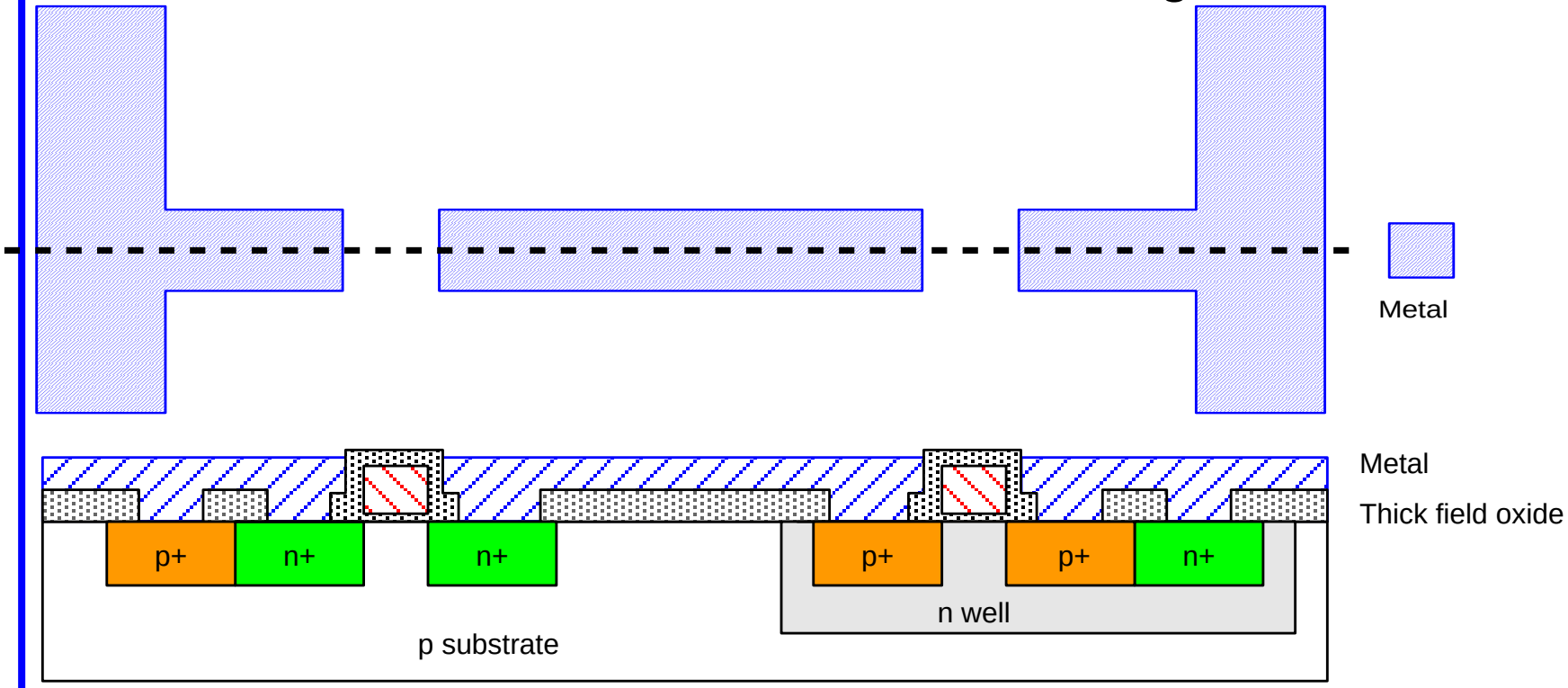
# Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



# Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



Thank You!

It was great having you in the class!

Best of luck!