7

FET Biasing

CHAPTER OUTLINE

In Chapter 4 we found that the biasing levels for a silicon transistor configuration can be obtained using the approximate characteristic equations $V_{BE} = 0.7\text{ V}$, $I_C = \beta I_B$, and $I_C \cong I_E$. The link between input and output variables is provided by β, which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between I_C and I_B. Doubling the value of I_B will double the level of I_C, and so on.

For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, whereas nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have a graphical orientation rather than use direct mathematical techniques.

Another distinct difference between the analysis of BJT and FET transistors is that:

The input controlling variable for a BJT transistor is a current level, whereas for the FET a voltage is the controlling variable.

In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$\boxed{I_G \cong 0\,\text{A}} \tag{7.1}$$

and

$$\boxed{I_D = I_S} \tag{7.2}$$

For JFETS and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2} \tag{7.3}$$

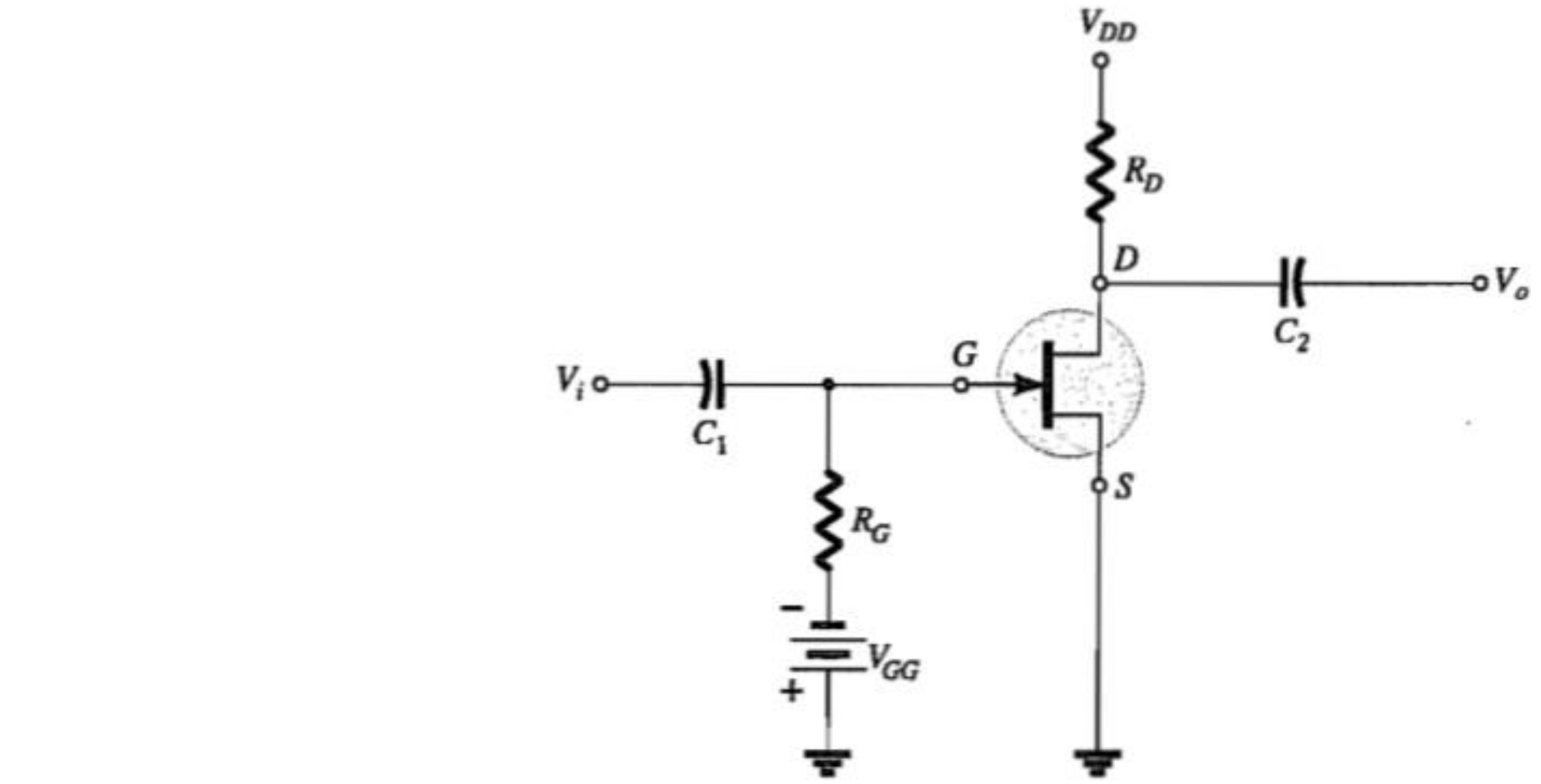
For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

$$\boxed{I_D = k(V_{GS} - V_T)^2} \tag{7.4}$$

It is particularly important to realize that all of the equations above are for the *device only*! They do not change with each network configuration so long as the device is in the active region. The network simply defines the level of current and voltage associated with the operating point through its own set of equations. In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and the network. The solution can be determined using a mathematical or graphical approach—a

7.2 FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the n-channel JFET appears in Fig. 7.1. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or a graphical approach. Both



The configuration of Fig. 7.1 includes the ac levels V_i and V_o and the coupling capacitors (C_1 and C_2). Recall that the coupling capacitors are "open circuits" for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis (Chapter 8). For the dc analysis,

$$I_G \cong 0\text{ A}$$

and
$$V_{R_G} = I_G R_G = (0\text{ A})R_G = 0\text{ V}$$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 7.2, specifically redrawn for the dc analysis.

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 7.2 results in

$$-V_{GG} - V_{GS} = 0$$

and
$$\boxed{V_{GS} = -V_{GG}} \tag{7.5}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation "fixed-bias configuration."

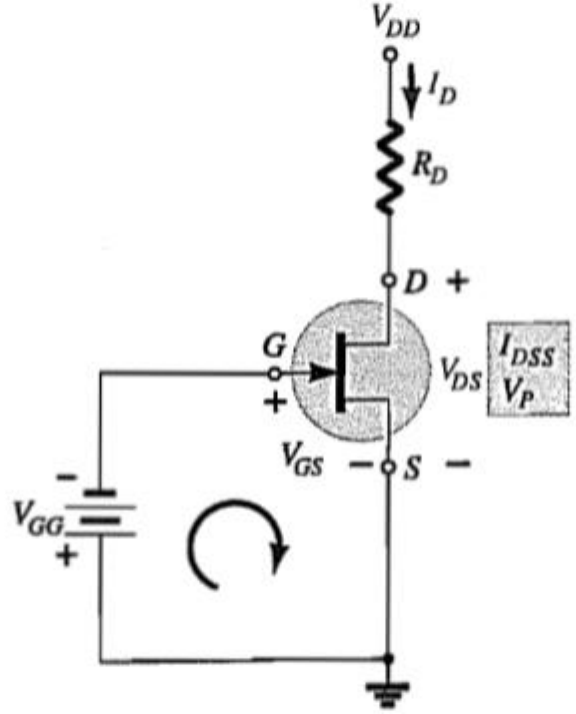
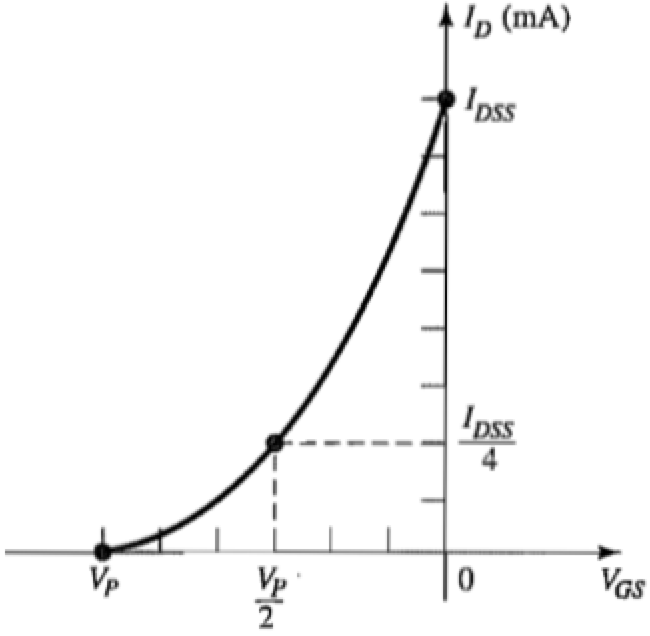


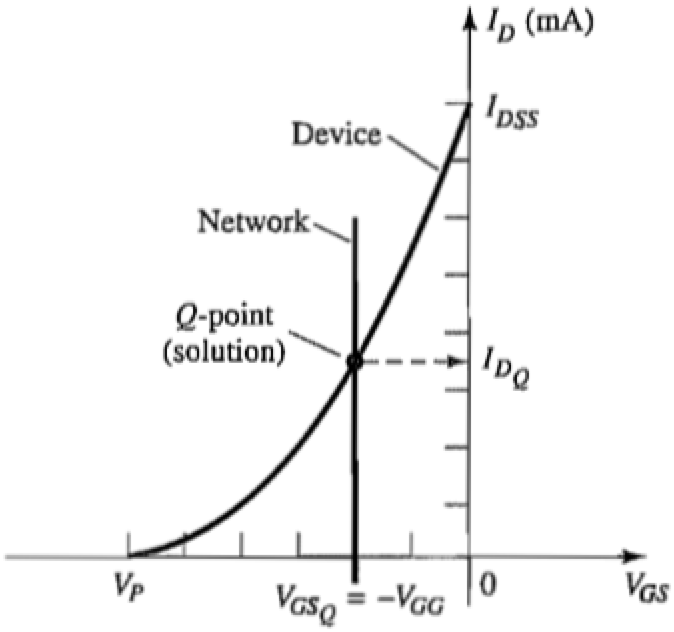
FIG. 7.2
Network for dc analysis.

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

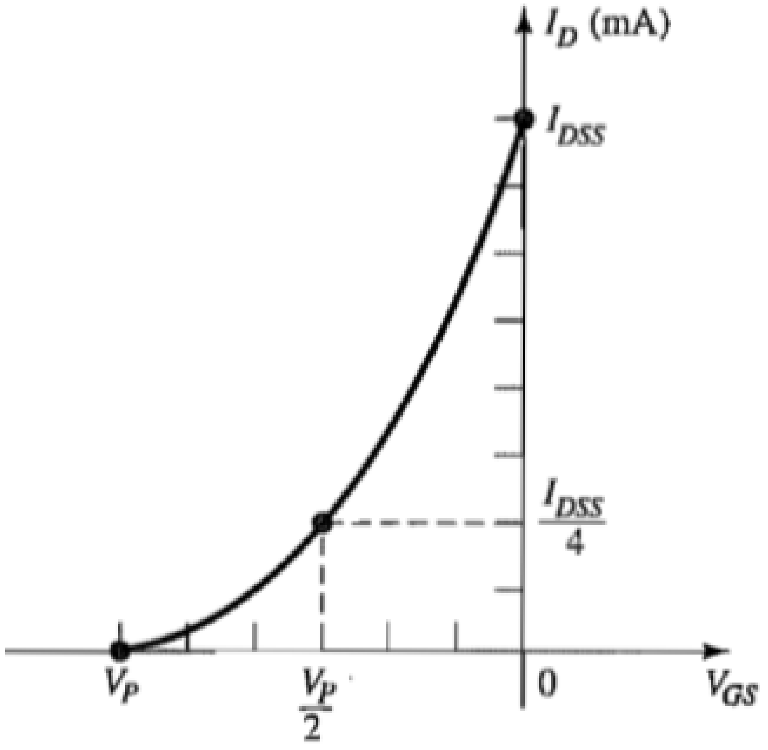
Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

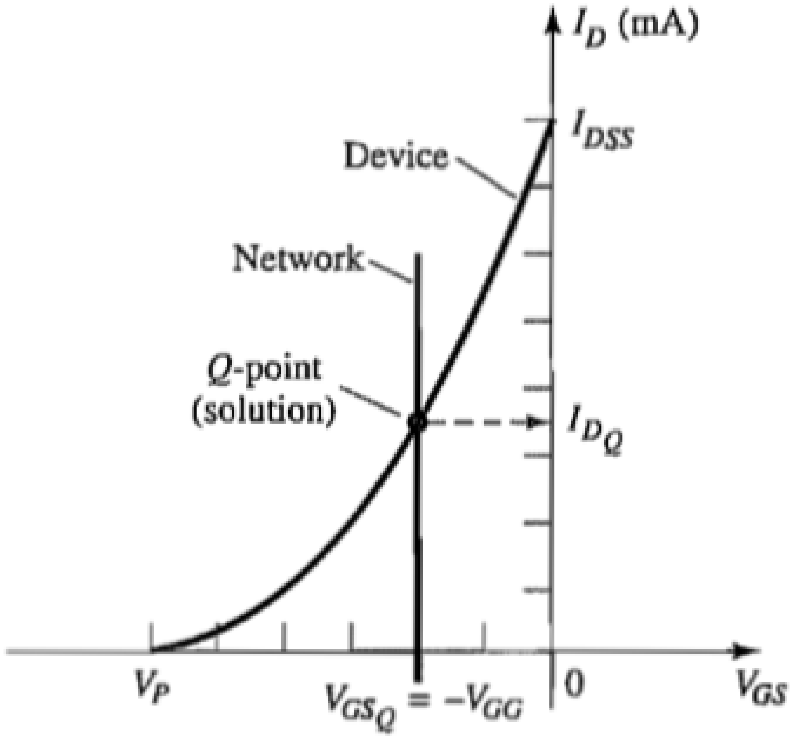




In Fig. 7.4, the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$—the level of I_D must simply be determined on this vertical line. The point where the two curves intersect

is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point.* The subscript Q will be applied to drain current and gate-to-source voltage to identify their levels at the Q-point. Note in Fig. 7.4 that the quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis. It is





The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \tag{7.6}$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 7.2,

$$\boxed{V_S = 0\,\text{V}} \tag{7.7}$$

Using double-subscript notation, we have

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0\,\text{V}$$

and

$$\boxed{V_D = V_{DS}} \tag{7.8}$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0\,\text{V}$$

and

$$\boxed{V_G = V_{GS}} \tag{7.9}$$

The fact that $V_D = V_{DS}$ and $V_G = V_{GS}$ is fairly obvious from the fact that $V_S = 0$ V, but the derivations above were included to emphasize the relationship that exists between double-subscript and single-subscript notation. Since the configuration requires two dc sup-

EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

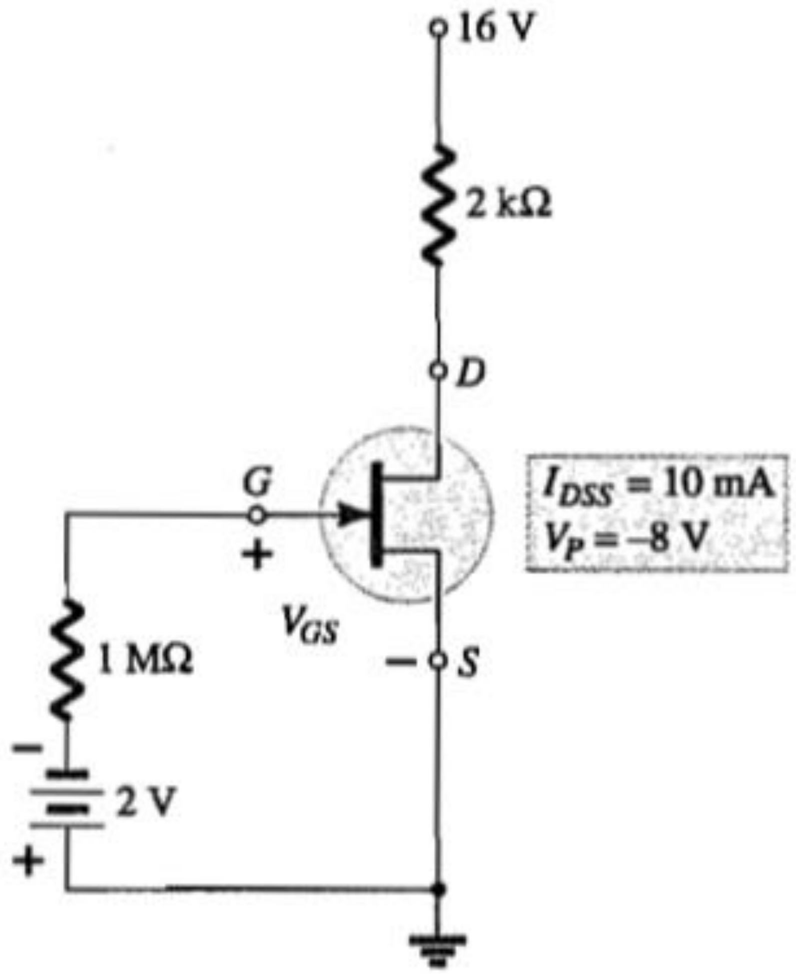


FIG. 7.6
Example 7.1.

Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\,V}$

b. $I_{D_Q} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 = 10\,\text{mA}\left(1 - \dfrac{-2\,\text{V}}{-8\,\text{V}}\right)^2$

$$= 10\,\text{mA}(1 - 0.25)^2 = 10\,\text{mA}(0.75)^2 = 10\,\text{mA}(0.5625)$$

$$= \mathbf{5.625\,mA}$$

c. $V_{DS} = V_{DD} - I_D R_D = 16\,\text{V} - (5.625\,\text{mA})(2\,\text{k}\Omega)$

$$= 16\,\text{V} - 11.25\,\text{V} = \mathbf{4.75\,V}$$

d. $V_D = V_{DS} = \mathbf{4.75\,V}$

e. $V_G = V_{GS} = \mathbf{-2\,V}$

f. $V_S = \mathbf{0\,V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 7.7 is quite acceptable.

a. Therefore,

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\,V}$$

b. $I_{D_Q} = \mathbf{5.6\,mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\,\text{V} - (5.6\,\text{mA})(2\,\text{k}\Omega)$

$= 16\,\text{V} - 11.2\,\text{V} = \mathbf{4.8\,V}$

d. $V_D = V_{DS} = \mathbf{4.8\,V}$

e. $V_G = V_{GS} = \mathbf{-2\,V}$

f. $V_S = \mathbf{0\,V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

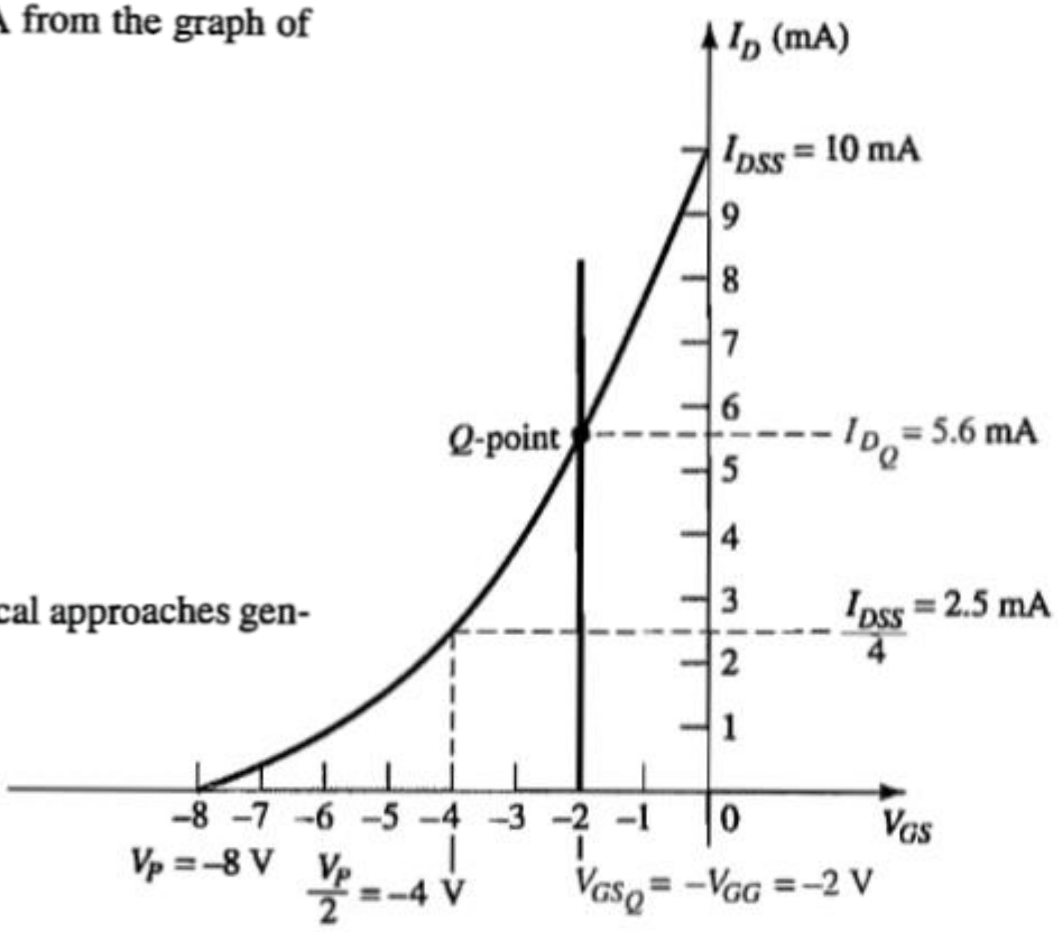


FIG. 7.7
Graphical solution for the network of Fig. 7.6.

7.3 SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 7.8.

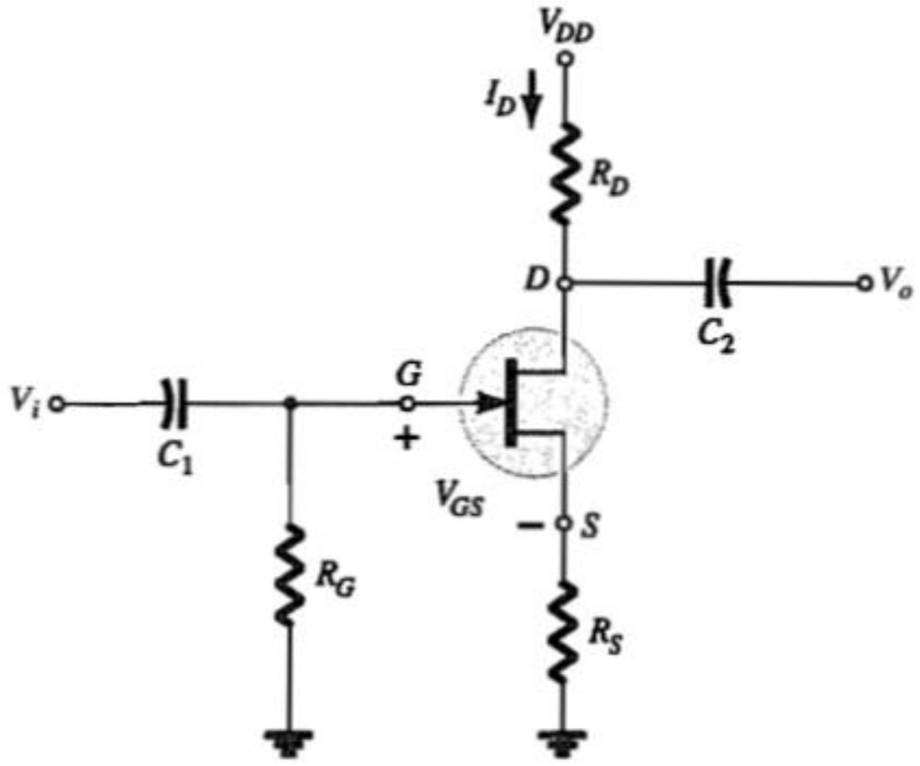


FIG. 7.8
JFET self-bias configuration.

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A. The result is the network of Fig. 7.9 for the important dc analysis.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 7.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$\boxed{V_{GS} = -I_D R_S} \tag{7.10}$$

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

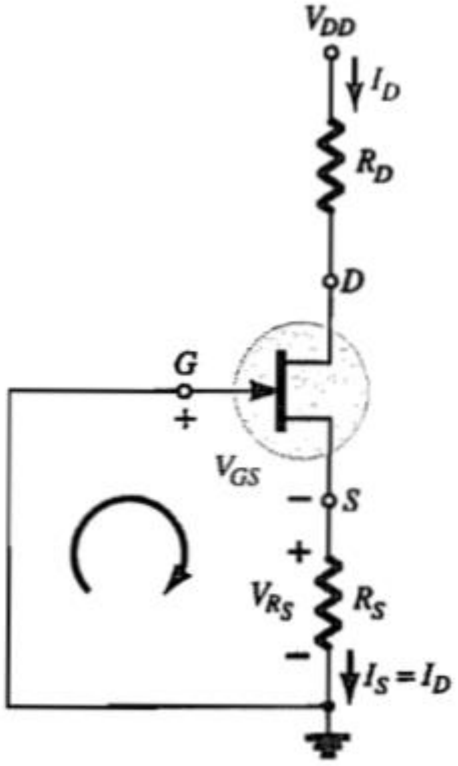


FIG. 7.9
DC analysis of the self-bias configuration.

A mathematical solution could be obtained simply by substituting Eq. (7.10) into Shockley's equation as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

or

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, we obtain an equation of the following form:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D.

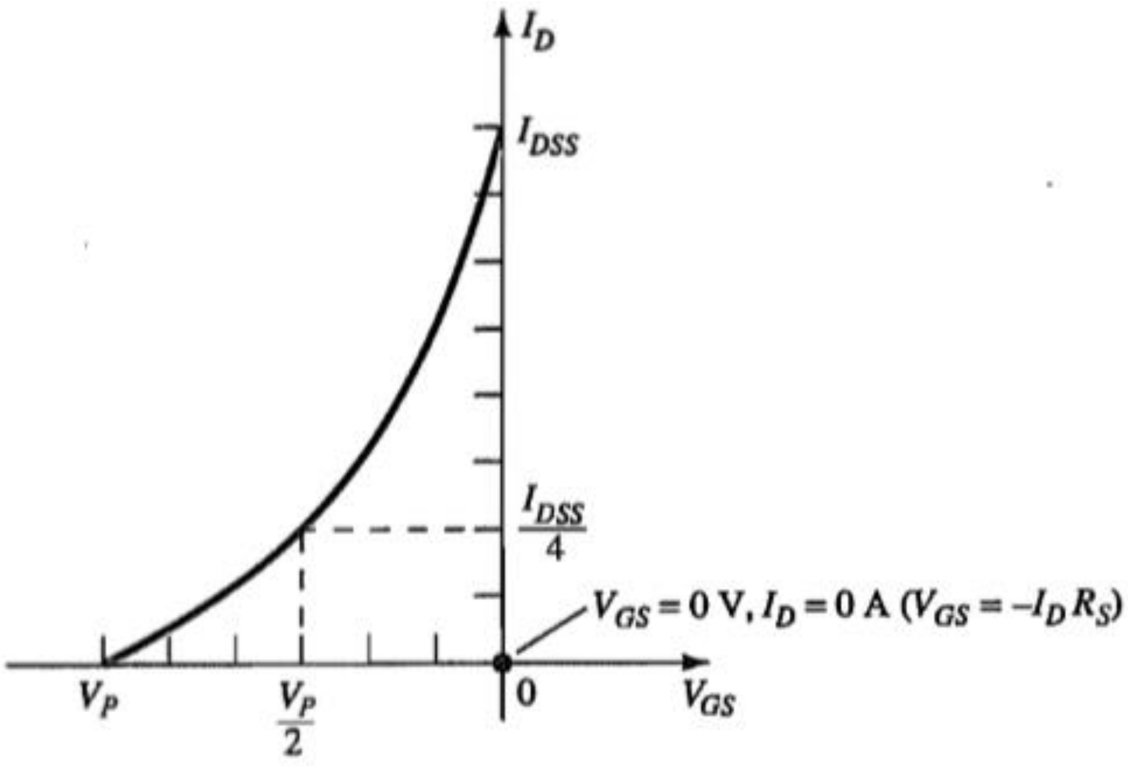


FIG. 7.10

Defining a point on the self-bias line.

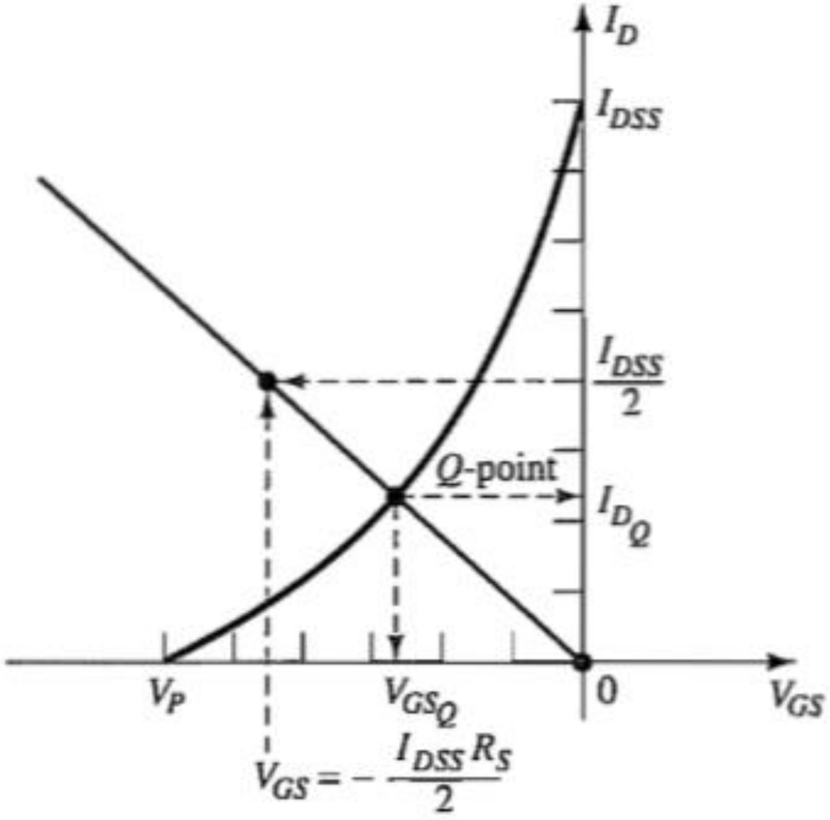


FIG. 7.11

Sketching the self-bias line.

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

$$I_D = I_S$$

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)}$$

$$\boxed{V_S = I_D R_S}$$

$$\boxed{V_G = 0\,\text{V}}$$

$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}}$$

EXAMPLE 7.2 Determine the following for the network of Fig. 7.12:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

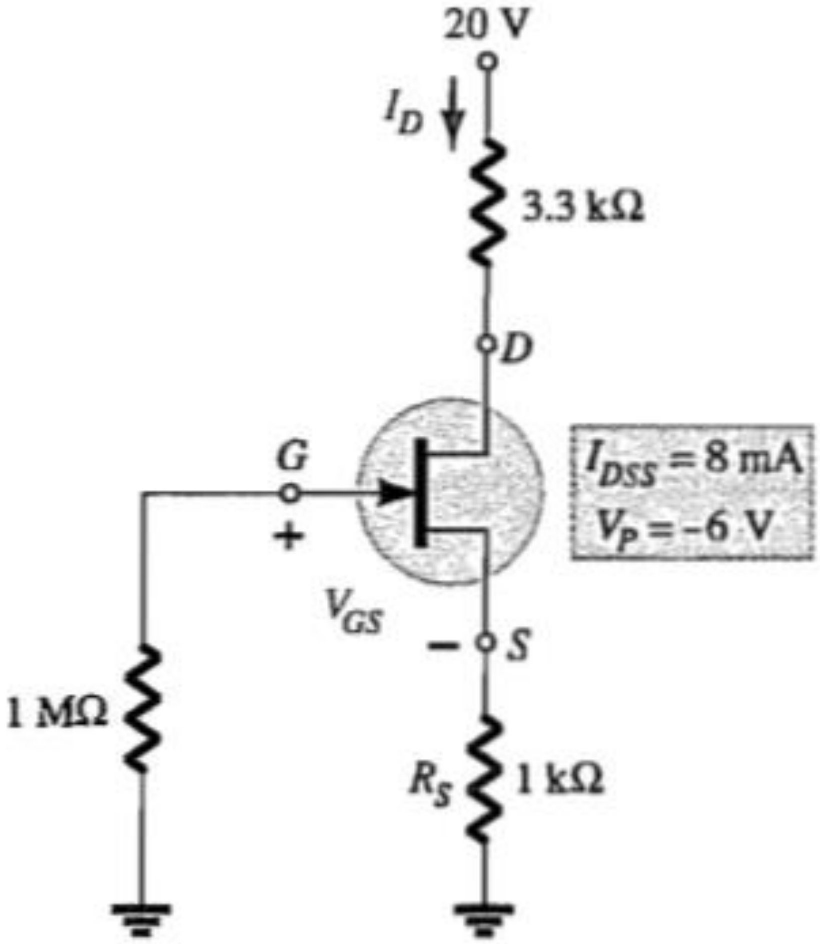


FIG. 7.12
Example 7.2.

Solution:

a. The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4\text{ mA}$, we obtain

$$V_{GS} = -(4\text{ mA})(1\text{ k}\Omega) = -4\text{ V}$$

The result is the plot of Fig. 7.13 as defined by the network.

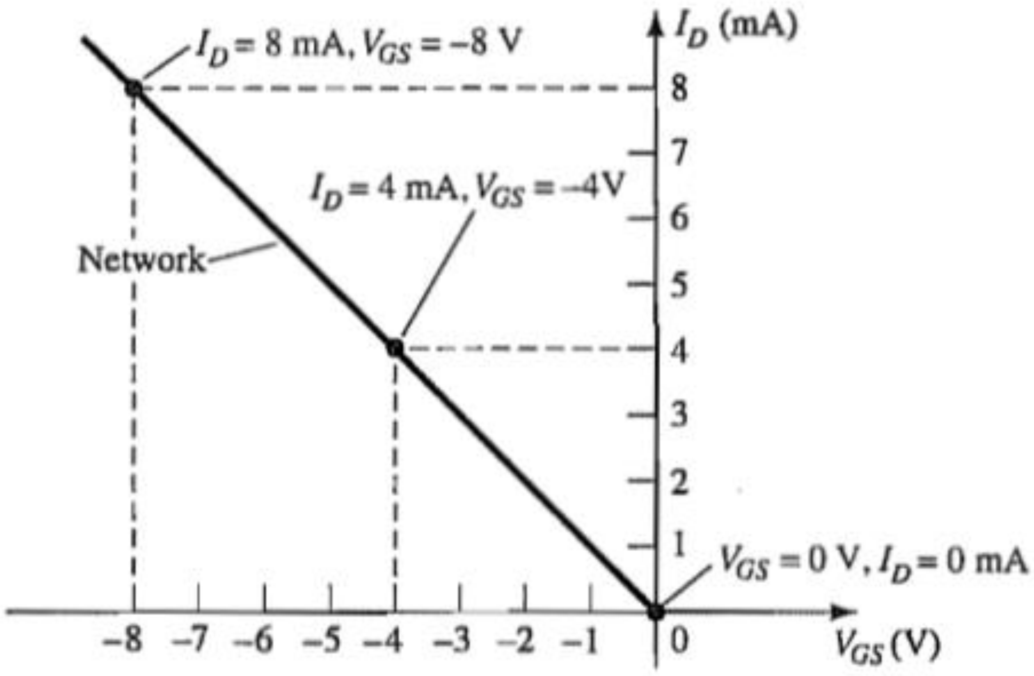


FIG. 7.13

Sketching the self-bias line for the network of Fig. 7.12.

$$V_{GS_Q} = -2.6 \text{ V}$$

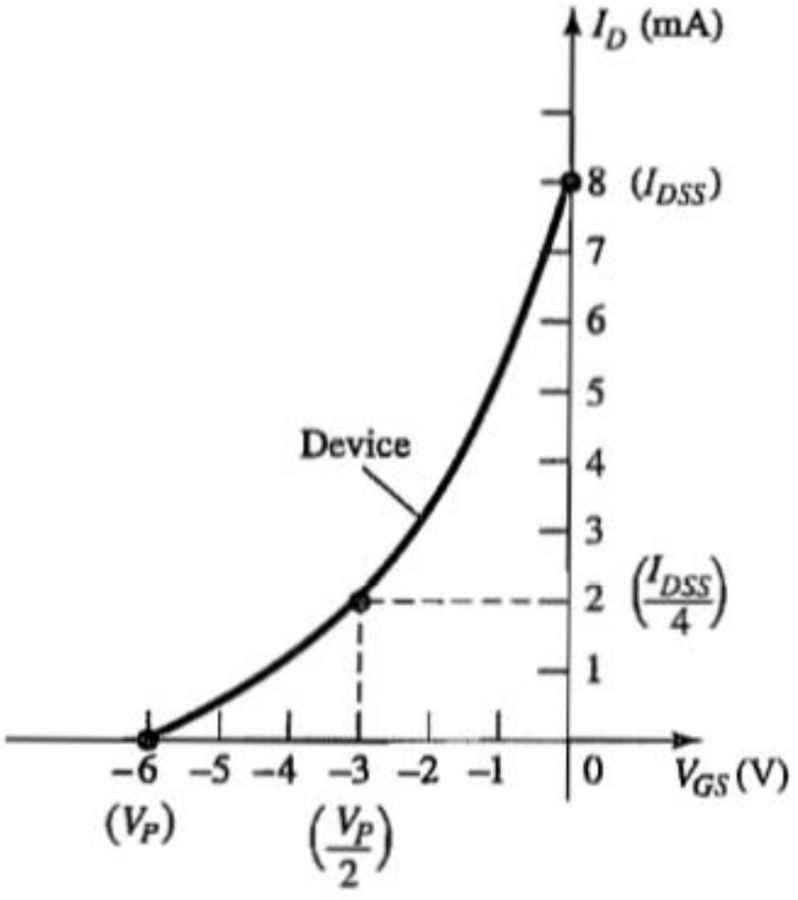


FIG. 7.14
Sketching the device characteristics for the JFET of Fig. 7.12.

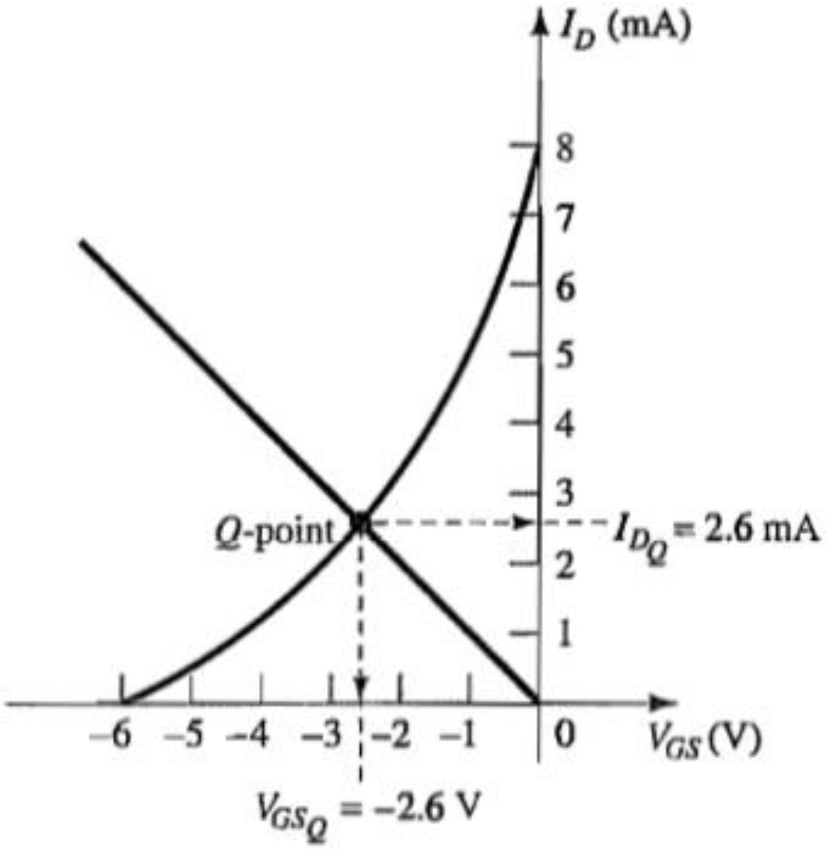


FIG. 7.15
Determining the Q-point for the network of Fig. 7.12.

b. At the quiescent point

$$I_{D_Q} = \mathbf{2.6\,mA}$$

c. Eq. (7.11):
$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ &= 20\,\text{V} - (2.6\,\text{mA})(1\,\text{k}\Omega + 3.3\,\text{k}\Omega) \\ &= 20\,\text{V} - 11.18\,\text{V} \\ &= \mathbf{8.82\,V} \end{aligned}$$

d. Eq. (7.12):
$$\begin{aligned} V_S &= I_D R_S \\ &= (2.6\,\text{mA})(1\,\text{k}\Omega) \\ &= \mathbf{2.6\,V} \end{aligned}$$

e. Eq. (7.13): $V_G = \mathbf{0\,V}$

f. Eq. (7.14): $V_D = V_{DS} + V_S = 8.82\,\text{V} + 2.6\,\text{V} = \mathbf{11.42\,V}$

or $V_D = V_{DD} - I_D R_D = 20\,\text{V} - (2.6\,\text{mA})(3.3\,\text{k}\Omega) = \mathbf{11.42\,V}$

EXAMPLE 7.3 Find the quiescent point for the network of Fig. 7.12 if:

a. $R_S = 100\,\Omega$.
b. $R_S = 10\,\mathrm{k}\Omega$.

Solution: Note Fig. 7.17.

a. With the I_D scale,

$$I_{D_Q} \cong \mathbf{6.4\,mA}$$

From Eq. (7.10),

$$V_{GS_Q} \cong \mathbf{-0.64\,V}$$

b. With the V_{GS} scale,

$$V_{GS_Q} \cong \mathbf{-4.6\,V}$$

From Eq. (7.10),

$$I_{D_Q} \cong \mathbf{0.46\,mA}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis, whereas increasing levels of R_S bring the load line closer to the V_{GS} axis.

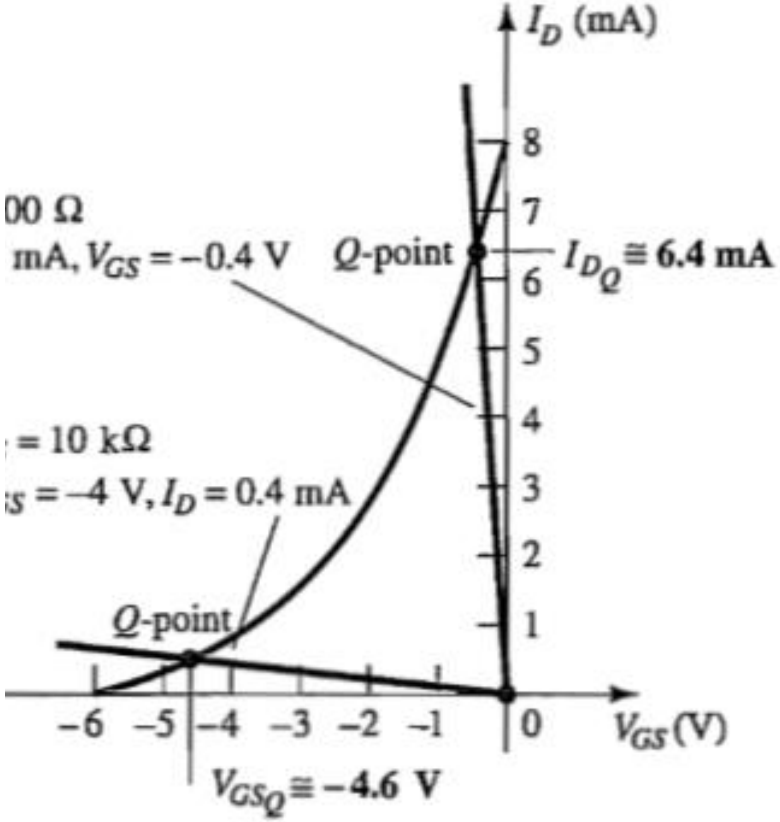


FIG. 7.17
Example 7.3.

EXAMPLE 7.4 Determine the following for the common-gate configuration of Fig. 7.18:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_D.
d. V_G.
e. V_S.
f. V_{DS}.

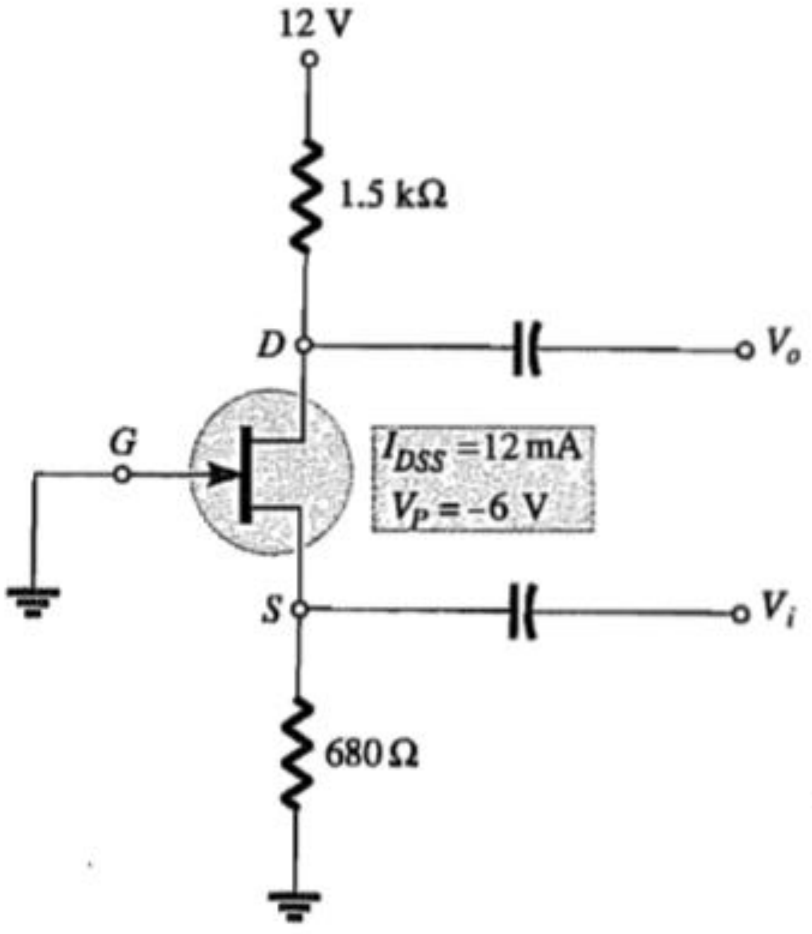


FIG. 7.18
Example 7.4.

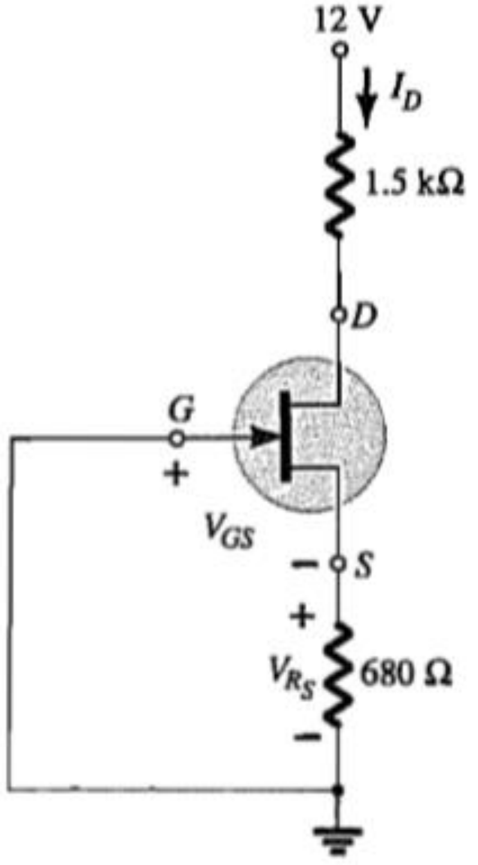


FIG. 7.19
Sketching the dc equivalent of the network of Fig. 7.18.

a. The transfer characteristics and load line appear in Fig. 7.20. In this case, the second point for the sketch of the load line is determined by choosing (arbitrarily) $I_D = 6\text{ mA}$ and solving for V_{GS}. That is,

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

as shown in Fig. 7.20. The device transfer curve is sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA}$$

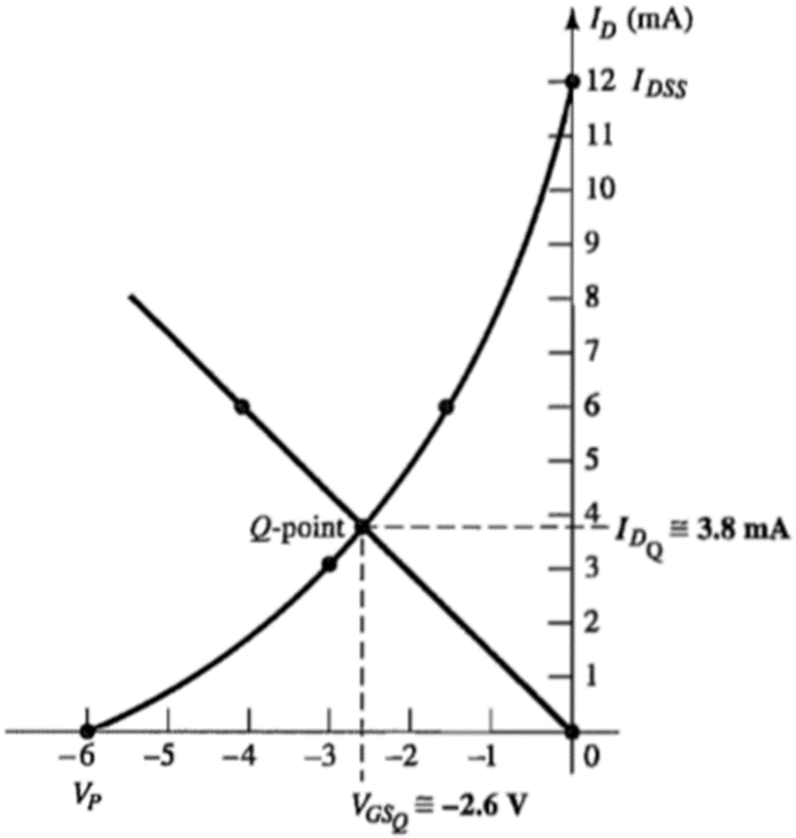


FIG. 7.20
Determining the Q-point for the network of Fig. 7.18.

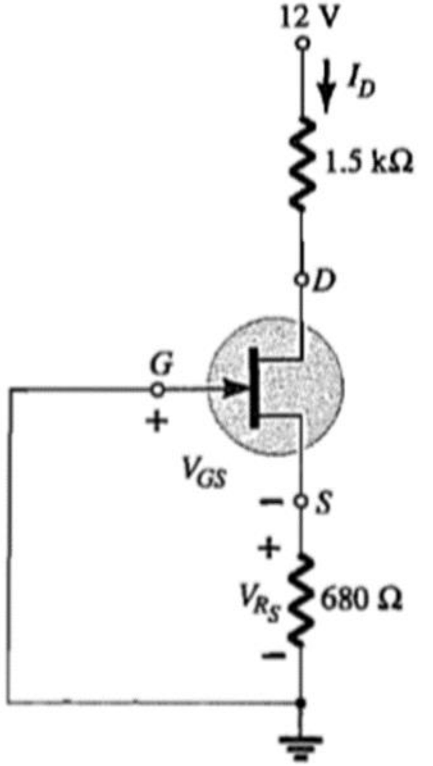


FIG. 7.19
Sketching the dc equivalent of the network of Fig. 7.18.

and the associated value of V_{GS},

$$V_{GS} = \frac{V_P}{2} = -\frac{6\text{ V}}{2} = -3\text{ V}$$

as shown on Fig. 7.20. Using the resulting quiescent point

$$V_{GS_Q} \cong \mathbf{-2.6\ V}$$

b. From Fig. 7.20,

$$I_{D_Q} \cong \mathbf{3.8\ mA}$$

c. $V_D = V_{DD} - I_D R_D$

$= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V}$

$= \mathbf{6.3\ V}$

d. $V_G = \mathbf{0\ V}$

e. $V_S = I_D R_S = (3.8\text{ mA})(680\ \Omega)$

$= \mathbf{2.58\ V}$

f. $V_{DS} = V_D - V_S$

$= 6.3\text{ V} - 2.58\text{ V}$

$= \mathbf{3.72\ V}$

7.4 VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 7.21. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0$ A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provides the link between input and output circuits for the BJT voltage-divider configuration, whereas V_{GS} does the same for the FET configuration.

The network of Fig. 7.21 is redrawn as shown in Fig. 7.22 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent. In addition, the source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network. Since $I_G = 0$ A, Kirchhoff's current law requires that $I_{R_1} = I_{R_2}$, and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule as follows:

$$\boxed{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}} \tag{7.15}$$

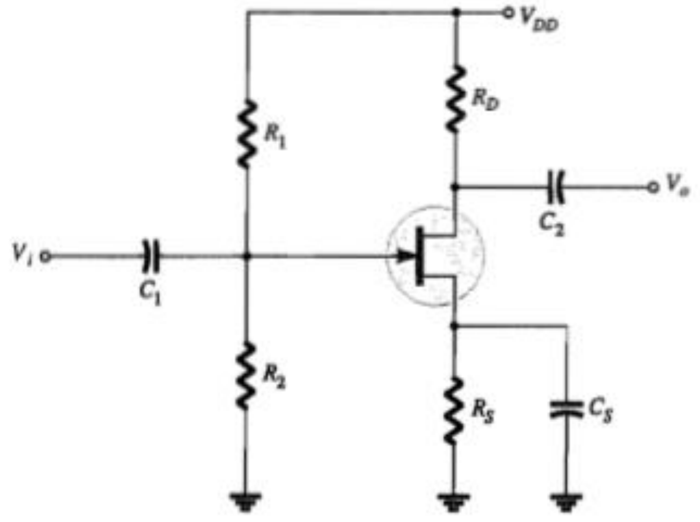


FIG. 7.21
Voltage-divider bias arrangement.

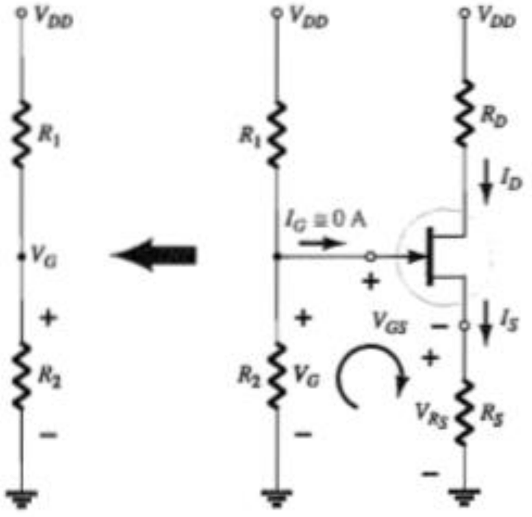


FIG. 7.22
Redrawn network of Fig. 7.21 for dc analysis.

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 7.22 results in

$$V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

$$\boxed{V_{GS} = V_G - I_D R_S} \tag{7.16}$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D. The quantities V_G and R_S are fixed by the network construction. Equation (7.16) is still the equation for a straight line, but the origin is no longer a point in the plotting of the line. The procedure for plotting Eq. (7.16) is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that anywhere on the horizontal axis of Fig. 7.23 the current $I_D = 0$ mA. If we therefore select I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0$ mA into Eq. (7.16) and finding the resulting value of V_{GS} as follows:

$$\begin{aligned} V_{GS} &= V_G - I_D R_S \\ &= V_G - (0\,\text{mA})R_S \end{aligned}$$

and

$$\boxed{V_{GS} = V_G\big|_{I_D = 0\,\text{mA}}} \tag{7.17}$$

The result specifies that whenever we plot Eq. (7.16), if we choose $I_D = 0$ mA, the value of V_{GS} for the plot will be V_G volts. The point just determined appears in Fig. 7.23.

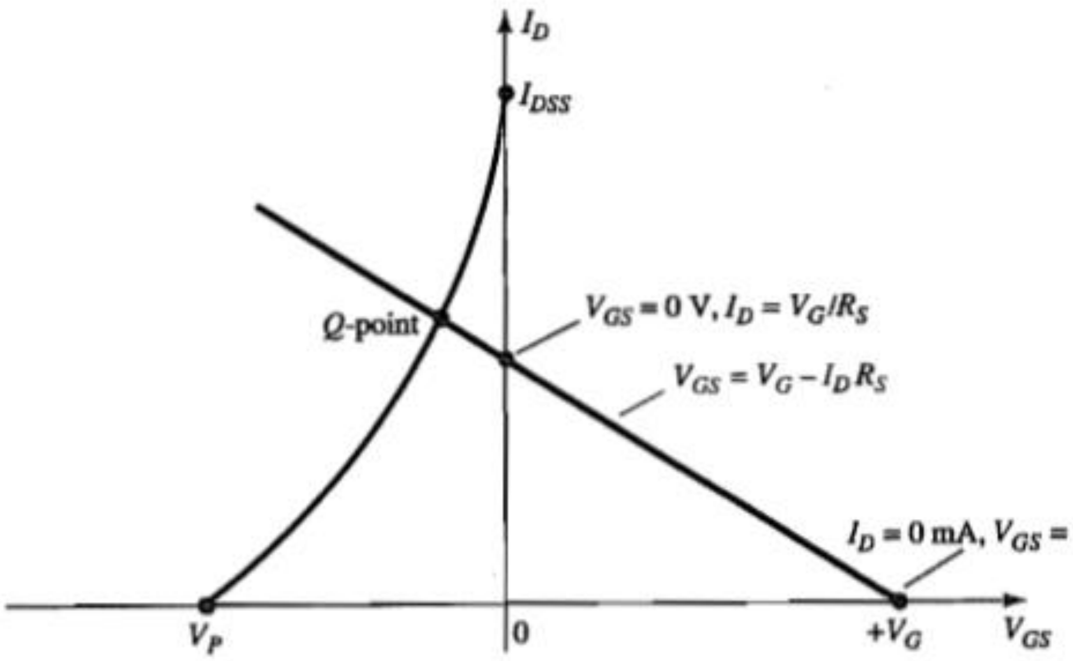


FIG. 7.23
Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0\text{ V}$ and solve for the resulting value of I_D:

$$V_{GS} = V_G - I_D R_S$$
$$0\text{ V} = V_G - I_D R_S$$

and
$$\boxed{I_D = \left.\frac{V_G}{R_S}\right|_{V_{GS}=0\text{ V}}} \tag{7.18}$$

Once the quiescent values of I_{D_Q} and V_{GS_Q} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)} \tag{7.19}$$

$$\boxed{V_D = V_{DD} - I_D R_D} \tag{7.20}$$

$$\boxed{V_S = I_D R_S} \tag{7.21}$$

$$\boxed{I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}} \tag{7.22}$$

EXAMPLE 7.5 Determine the following for the network of Fig. 7.25:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.

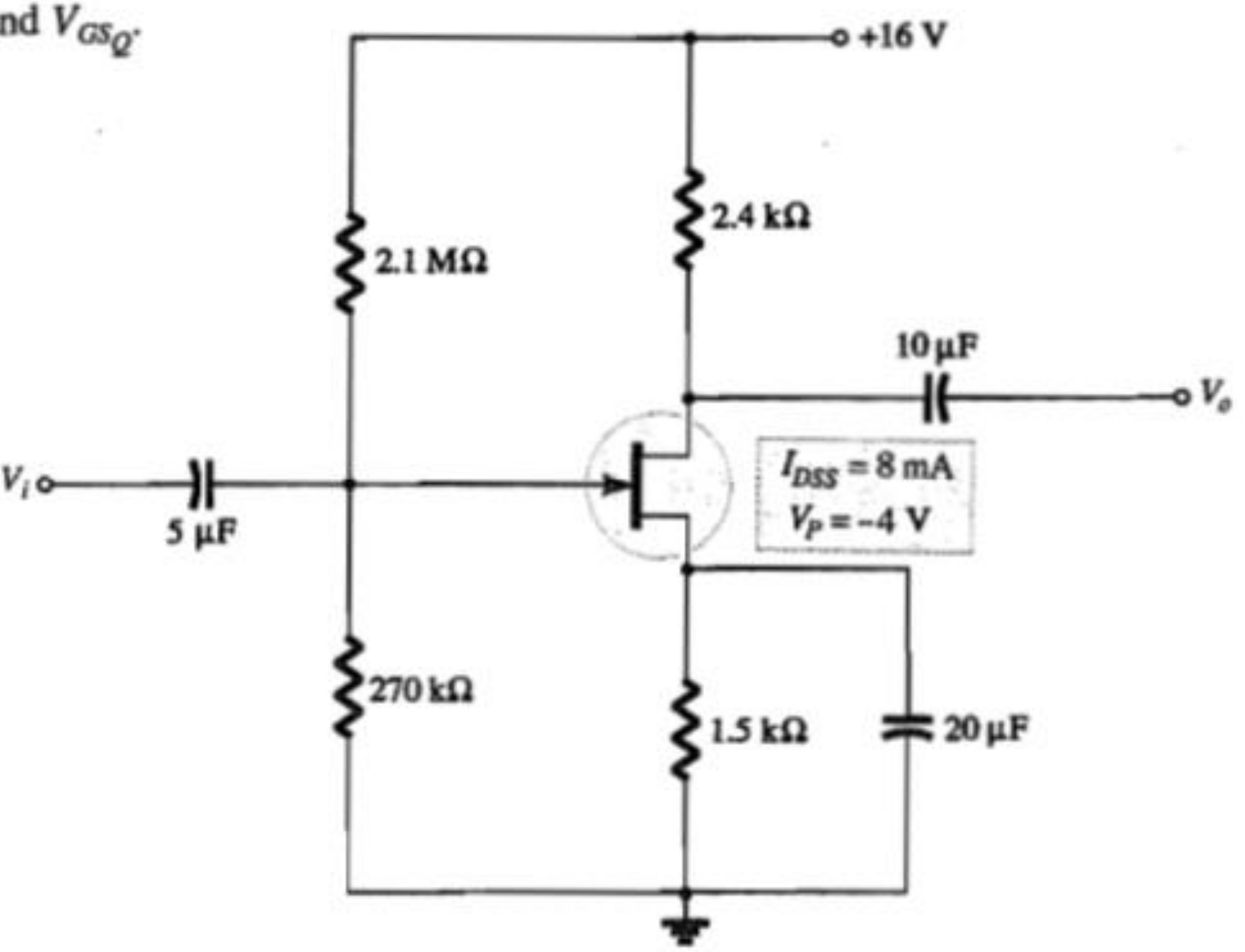


FIG. 7.25
Example 7.5.

Solution:

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2\text{ mA}$, then $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$. The resulting curve representing Shockley's equation appears in Fig. 7.26. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

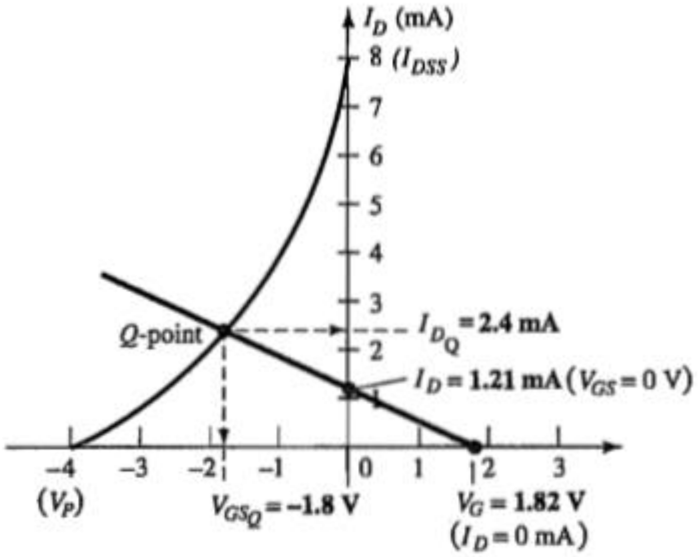
$$= \frac{(270\text{ k}\Omega)(16\text{ V})}{2.1\text{ M}\Omega + 0.27\text{ M}\Omega}$$

$$= 1.82\text{ V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\text{ V} - I_D(1.5\text{ k}\Omega)$$



When $I_D = 0\,\text{mA}$,

$$V_{GS} = +1.82\,\text{V}$$

When $V_{GS} = 0\,\text{V}$,

$$I_D = \frac{1.82\,\text{V}}{1.5\,\text{k}\Omega} = 1.21\,\text{mA}$$

The resulting bias line appears on Fig. 7.26 with quiescent values of

$$I_{D_Q} = \mathbf{2.4\,mA}$$

and

$$V_{GS_Q} = \mathbf{-1.8\,V}$$

b. $V_D = V_{DD} - I_D R_D$

$\quad = 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega)$

$\quad = \mathbf{10.24\,V}$

c. $V_S = I_D R_S = (2.4\,\text{mA})(1.5\,\text{k}\Omega)$

$\quad = \mathbf{3.6\,V}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$\quad = 16\,\text{V} - (2.4\,\text{mA})(2.4\,\text{k}\Omega + 1.5\,\text{k}\Omega)$

$\quad = \mathbf{6.64\,V}$

or $V_{DS} = V_D - V_S = 10.24\,\text{V} - 3.6\,\text{V}$

$\quad = \mathbf{6.64\,V}$

e. Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G$$

$$= 10.24\,\text{V} - 1.82\,\text{V}$$

$$= \mathbf{8.42\,V}$$

7.5 DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

The only undefined part of the analysis is how to plot Shockley's equation for positive values of V_{GS}. How far into the region of positive values of V_{GS} and values of I_D greater than I_{DSS} does the transfer curve have to extend? For most situations, this required

EXAMPLE 7.7 For the n-channel depletion-type MOSFET of Fig. 7.30, determine:

a. I_{D_Q} and V_{GS_Q}.
b. V_{DS}.

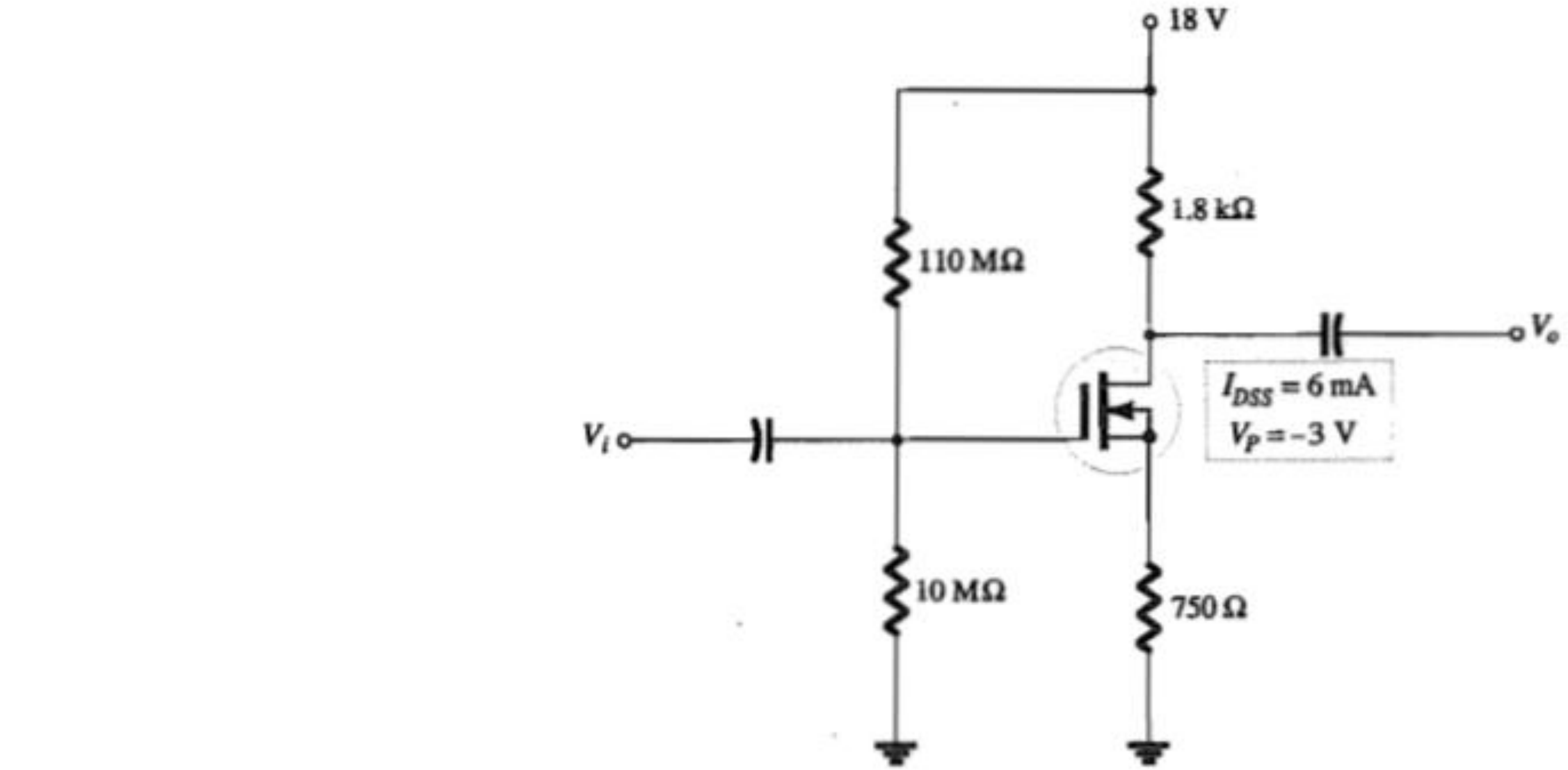


FIG. 7.30
Example 7.7.

Solution:

a. For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\,\text{mA}/4 = 1.5\,\text{mA}$ and $V_{GS} = V_P/2 = -3\,\text{V}/2 = -1.5\,\text{V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\,\text{V}$. Substituting into Shockley's equation yields

$$\begin{aligned} I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \\ &= 6\,\text{mA}\left(1 - \frac{+1\,\text{V}}{-3\,\text{V}}\right)^2 = 6\,\text{mA}\left(1 + \frac{1}{3}\right)^2 = 6\,\text{mA}(1.778) \\ &= 10.67\,\text{mA} \end{aligned}$$

The resulting transfer curve appears in Fig. 7.31. Proceeding as described for JFETs, we have

$$\text{Eq. (7.15):}\quad V_G = \frac{10\,\text{M}\Omega(18\,\text{V})}{10\,\text{M}\Omega + 110\,\text{M}\Omega} = 1.5\,\text{V}$$

$$\text{Eq. (7.16):}\quad V_{GS} = V_G - I_D R_S = 1.5\,\text{V} - I_D(750\,\Omega)$$

Setting $I_D = 0\,\text{mA}$ results in

$$V_{GS} = V_G = 1.5\,\text{V}$$

Setting $V_{GS} = 0\,\text{V}$ yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\,\text{V}}{750\,\Omega} = 2\,\text{mA}$$

The plot points and resulting bias line appear in Fig. 7.31. The resulting operating point is given by

$$I_{D_Q} = \mathbf{3.1\,mA}$$
$$V_{GS_Q} = \mathbf{-0.8\,V}$$

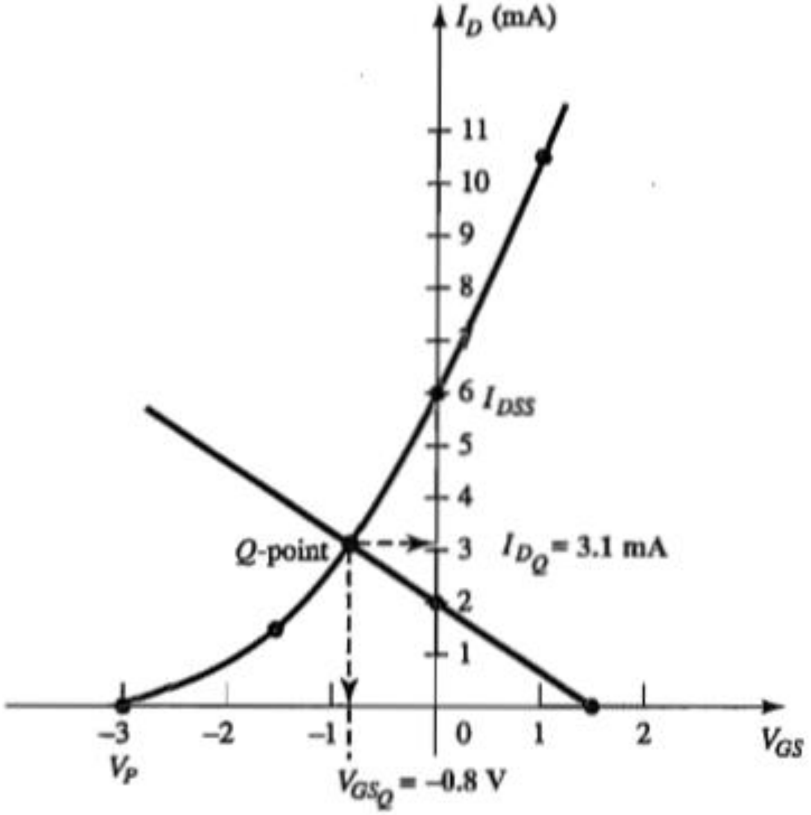


FIG. 7.31
Determining the Q-point for the network of Fig. 7.30.

b. Eq. (7.19):

$$
\begin{aligned}
V_{DS} &= V_{DD} - I_D(R_D + R_S) \\
&= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega) \\
&\cong \mathbf{10.1\ V}
\end{aligned}
$$

EXAMPLE 7.8 Repeat Example 7.7 with $R_S = 150\ \Omega$.

Solution:

a. The plot points are the same for the transfer curve as shown in Fig. 7.32. For the bias line,

$$V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(150\ \Omega)$$

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5\text{ V}$$

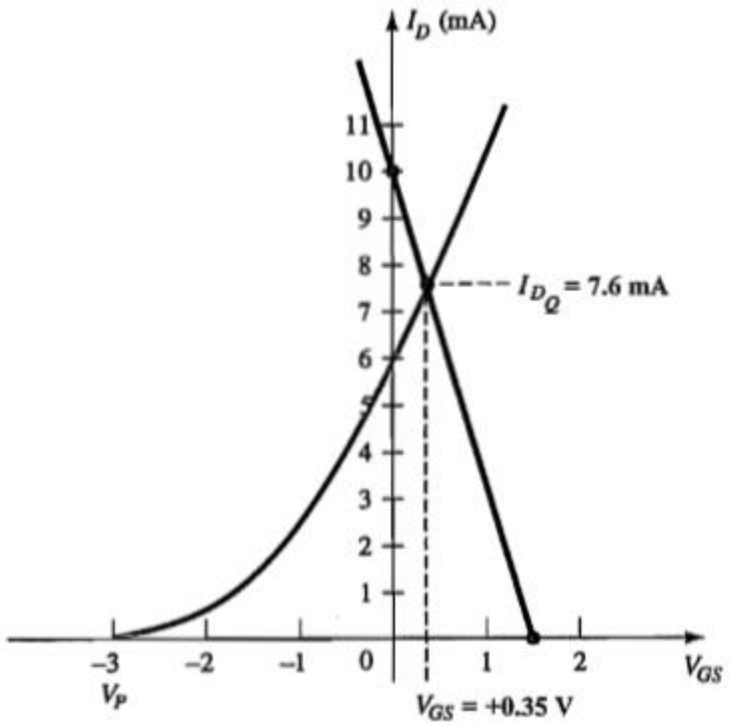


FIG. 7.32
Example 7.8.

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{150\ \Omega} = 10\text{ mA}$$

The bias line is included on Fig. 7.32. Note in this case that the quiescent point results in a drain current that exceeds I_{DSS}, with a positive value for V_{GS}. The result is

$$I_{D_Q} = \mathbf{7.6\ mA}$$
$$V_{GS_Q} = \mathbf{+0.35\ V}$$

b. Eq. (7.19):

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_D + R_S) \\ &= 18\text{ V} - (7.6\text{ mA})(1.8\text{ k}\Omega + 150\ \Omega) \\ &= \mathbf{3.18\ V} \end{aligned}$$

EXAMPLE 7.9 Determine the following for the network of Fig. 7.33:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.

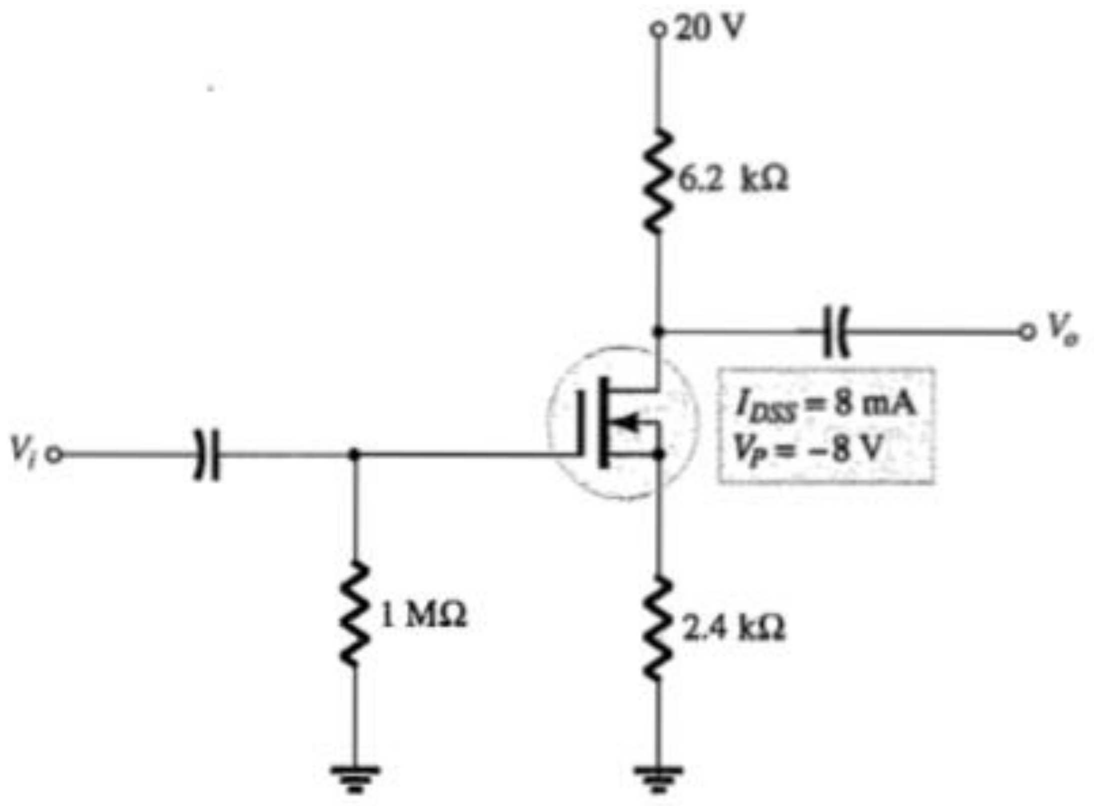


FIG. 7.33
Example 7.9.

Solution:

a. The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for $V_{GS} < 0$ V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8\text{ mA}}{4} = 2\text{ mA}$$

and
$$V_{GS} = \frac{V_P}{2} = \frac{-8\text{ V}}{2} = -4\text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2\text{ V}$$

and
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\text{ mA}\left(1 - \frac{+2\text{ V}}{-8\text{ V}}\right)^2$$

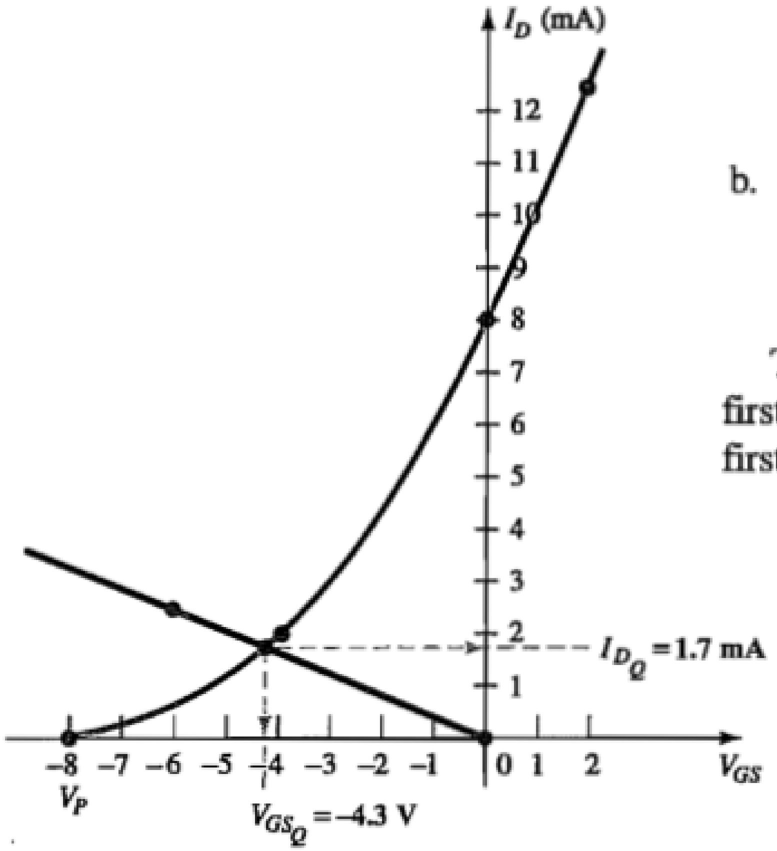
$$= 12.5\text{ mA}$$

The resulting transfer curve appears in Fig. 7.34. For the network bias line, at $V_{GS} = 0\,\text{V}$, $I_D = 0\,\text{mA}$. Choosing $V_{GS} = -6\,\text{V}$ gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\,\text{V}}{2.4\,\text{k}\Omega} = 2.5\,\text{mA}$$

The resulting Q-point is given by

$$I_{D_Q} = \mathbf{1.7\,mA}$$
$$V_{GS_Q} = \mathbf{-4.3\,V}$$



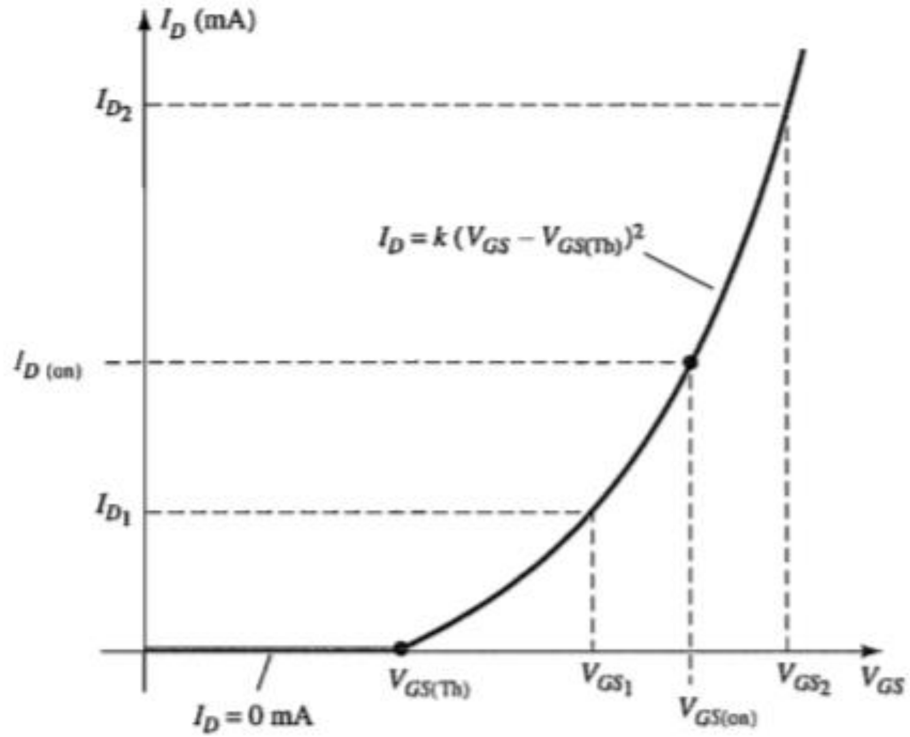
b. $V_D = V_{DD} - I_D R_D$
$= 20\,\text{V} - (1.7\,\text{mA})(6.2\,\text{k}\Omega)$
$= \mathbf{9.46\,V}$

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

7.6 ENHANCEMENT-TYPE MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from those of the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(Th)}$, as shown in Fig. 7.36. For levels of V_{GS} greater than $V_{GS(Th)}$, the drain current is defined by

$$\boxed{I_D = k(V_{GS} - V_{GS(Th)})^2} \tag{7.25}$$



Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(\text{on})}$) and its corresponding level of $V_{GS(\text{on})}$, two points are defined immediately as shown in Fig. 7.36. To complete the curve, the constant k of Eq. (7.25) must be determined from the specification sheet data by substituting into Eq. (7.25) and solving for k as follows:

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$
$$I_{D(\text{on})} = k(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$$

and

$$\boxed{k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}} \tag{7.26}$$

Once k is defined, other levels of I_D can be determined for chosen values of V_{GS}. Typically, a point between $V_{GS(\text{Th})}$ and $V_{GS(\text{on})}$ and one just greater than $V_{GS(\text{on})}$ will provide a sufficient number of points to plot Eq. (7.25) (note I_{D_1} and I_{D_2} on Fig. 7.36).

FIG. 7.42
Determining the Q-point for the network of Fig. 7.40.

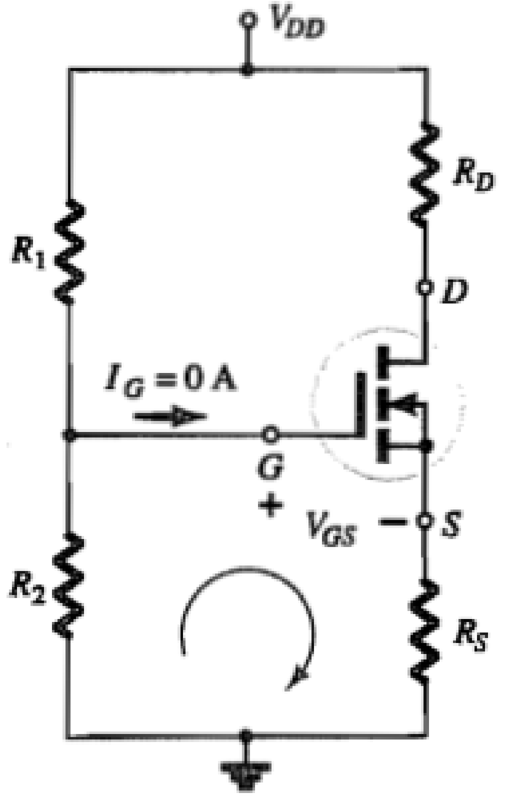


FIG. 7.43
Voltage-divider biasing arrangement for an n-channel enhancement MOSFET.

Voltage-Divider Biasing Arrangement

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 7.43. The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$\boxed{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}} \tag{7.31}$$

Applying Kirchhoff's voltage law around the indicated loop of Fig. 7.43 results in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$\boxed{V_{GS} = V_G - I_D R_S} \tag{7.32}$$

For the output section,

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \tag{7.33}$$

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (7.32) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{D_Q} and V_{GS_Q} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

EXAMPLE 7.12 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.44.

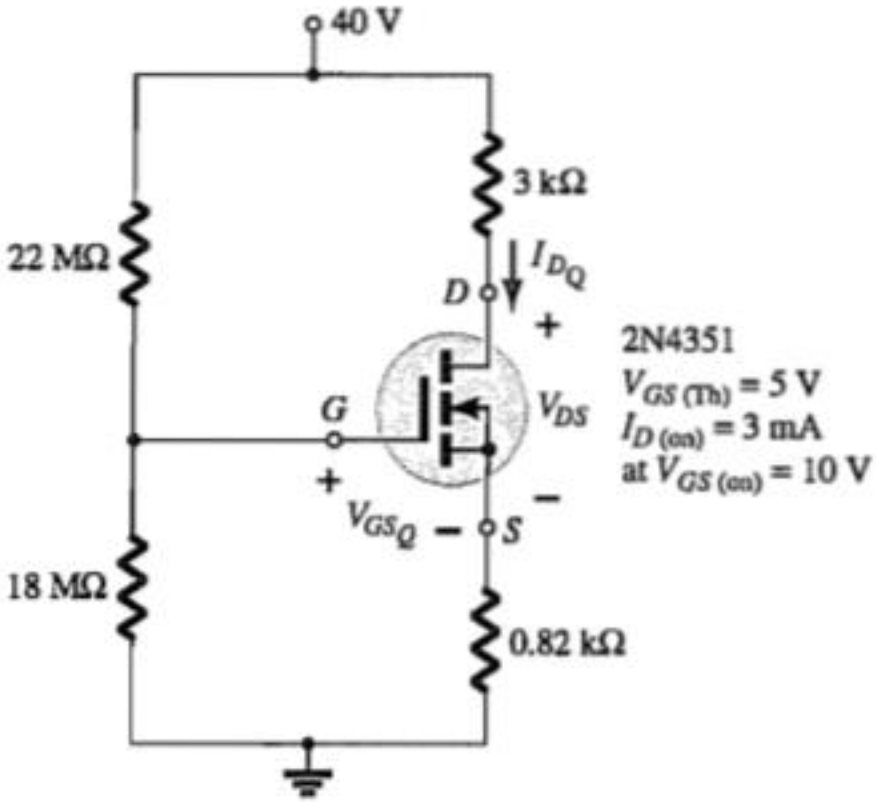


FIG. 7.44
Example 7.12.

Solution:

Network

$$\text{Eq. (7.31):}\quad V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\,\text{M}\Omega)(40\,\text{V})}{22\,\text{M}\Omega + 18\,\text{M}\Omega} = 18\,\text{V}$$

$$\text{Eq. (7.32):}\quad V_{GS} = V_G - I_D R_S = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

When $I_D = 0$ mA,

$$V_{GS} = 18\,\text{V} - (0\,\text{mA})(0.82\,\text{k}\Omega) = 18\,\text{V}$$

as appearing on Fig. 7.45. When $V_{GS} = 0$ V,

$$\begin{aligned} V_{GS} &= 18\,\text{V} - I_D(0.82\,\text{k}\Omega) \\ 0 &= 18\,\text{V} - I_D(0.82\,\text{k}\Omega) \\ I_D &= \frac{18\,\text{V}}{0.82\,\text{k}\Omega} = 21.95\,\text{mA} \end{aligned}$$

as appearing on Fig. 7.45.

Device

$$V_{GS(\text{Th})} = 5\,\text{V},\qquad I_{D(\text{on})} = 3\,\text{mA with } V_{GS(\text{on})} = 10\,\text{V}$$

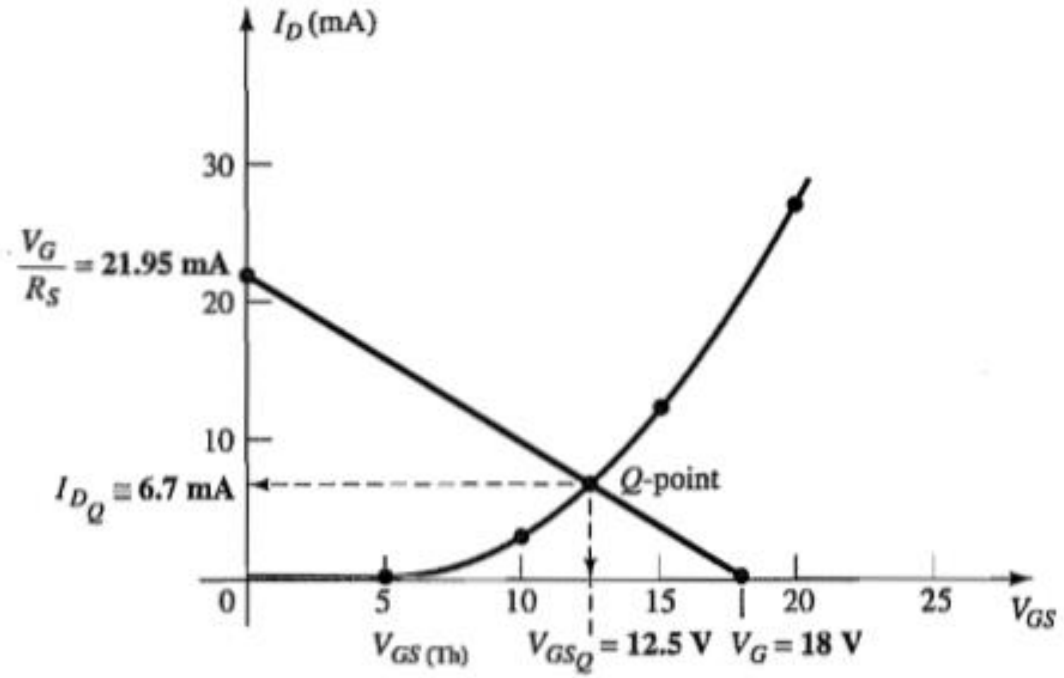


FIG. 7.45
Determining the Q-point for the network of Example 7.12.

$$\text{Eq. (7.26):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

which is plotted on the same graph (Fig. 7.45). From Fig. 7.45,

$$I_{D_Q} \cong \mathbf{6.7\text{ mA}}$$

$$V_{GS_Q} = \mathbf{12.5\text{ V}}$$

$$\text{Eq. (7.33):} \quad V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\text{ V} - (6.7\text{ mA})(0.82\text{ k}\Omega + 3.0\text{ k}\Omega)$$

$$= 40\text{ V} - 25.6\text{ V}$$

$$= \mathbf{14.4\text{ V}}$$

Thank You!