

North South University
Department of Electrical & Computer Engineering

PROJECT

Seven-Segment Display Using Sequential Circuit
on
EEE-211

Submitted to:
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Course: CSE231
Section: 10

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Introduction

In this project we are displaying 'EEE-211' on seven segment display using sequential circuit. For displaying on seven segment display at first we have done the truth table for 'EEE-211'. Then we got the equation using minterm(SOP) and maxterm(POS). But the minterm and maxterm equation are large. So we use K-map to simplify the equations. Then we implement the circuit in logic ~~with~~ SOP equation, POS equation, NAND gate and NOR gate individually. Finally for sequential circuit we used a 3 bit counter using JK-flipflop. Here for continuous clock pulse we used 555 timer. Which change our circuit state after certain period of time and displays our desired 'E','E','E','-','2','1','1' sequentially.

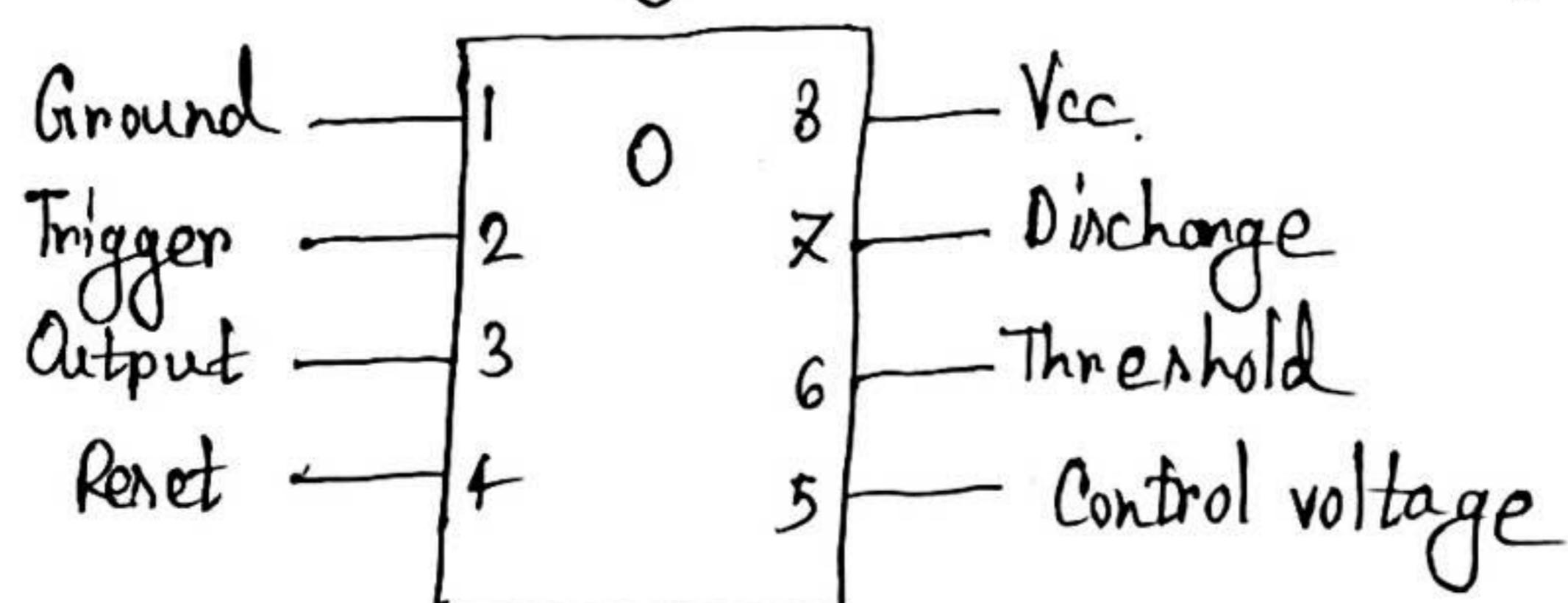
Seven Segment Display

Seven segment displays are the output display device that provide a way to display information in the form of image or text or decimal numbers which is an alternative to the more complex dot matrix displays. It is widely used in digital clock, basic calculators, and other electronics devices that display numerical information.

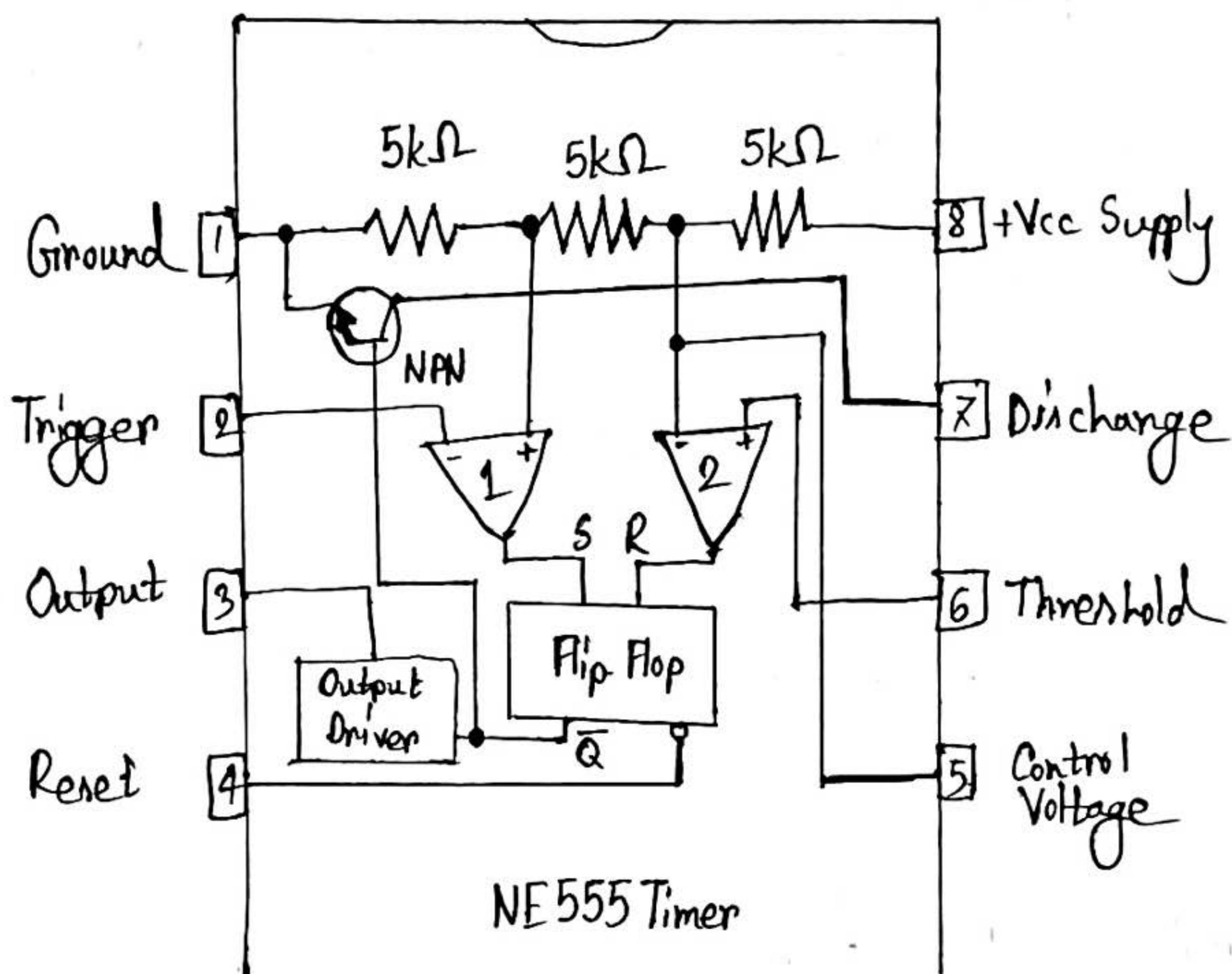
It consists of seven segments of light emitting diodes(LED) which is assembled like numerical 8.

555 Timer

The 555 is a single chip version of a commonly used circuit called a multivibrator, which is useful in a wide variety of electronic circuits. The 555 timer is probably the most popular integrated circuit ever made. Figure of 555 timer chip below:



The 555 timer is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if defined. In the time delay mode of operation, the timer is precisely controlled by one external resistor and capacitor.



- 555 timer block diagram -

Explanation of each connecting pins -

- Pin 1 - Ground: The ground pin connects the 555 timer to the negative (0_v) supply rail.
- Pin 2 - Trigger: The negative input to comparator No 1. A negative pulse on this pin 'sets' the internal flip-flop when the voltage drops below $1/3 V_{cc}$ causing the output to switch from a 'Low' to a 'High' state.
- Pin 3 - Output: The output pin can drive any TTL circuit and is capable of sourcing or sinking up to $200mA$ of current at an output voltage equal to approximately $V_{cc} - 1.5V$ so small speakers, LED's or motors can be connected directly to the output.
- Pin 4 - Reset: The pin is used to 'reset' the internal flip-flop controlling the state of output, pin 3. This is an active-low input and is generally connected to a logic '1' level when not used to prevent any unwanted resetting of the output.
- Pin 5 - Control voltage: This pin controls the timing of the 555 by overriding the $2/3 V_{cc}$ level of the voltage divider network. By applying voltage to this pin the width of the output signal can be varied independently.

of the RC timing network. When not used it is connected to ground via a 10nF capacitor to eliminate any noise.

- Pin 6 - Threshold: The positive input to comparator No 2. This pin is used to reset the Flip-flop when the voltage applied to it exceeds $2/3 V_{cc}$ causing the output to switch from 'High' to 'Low' state. This pin connects directly to the RC timing circuit.
- Pin 7 - Discharge: The discharge pin is connected directly to the Collector of an internal NPN transistor which is used to 'discharge' the timing capacitor to ground when the output at pin 3 switches 'Low'.
- Pin 8 - Supply $+V_{cc}$: This is the power supply pin and for general purpose TTL 555 timers is between 4.5 V and 15V.

Combinational circuit

Combinational circuit is a circuit in which we combine the different gates in the circuit, for example, encoder, decoder, multiplexer. Some of the characteristics of combinational circuits are,

- the output of combinational circuit at any instant of time, depends only on the levels present at input terminals.
- the combinational circuit do not use any memory. The previous state of input does not have any effect on the present state of the circuit.
- A combinational circuit can have an n number of inputs and m numbers of outputs.

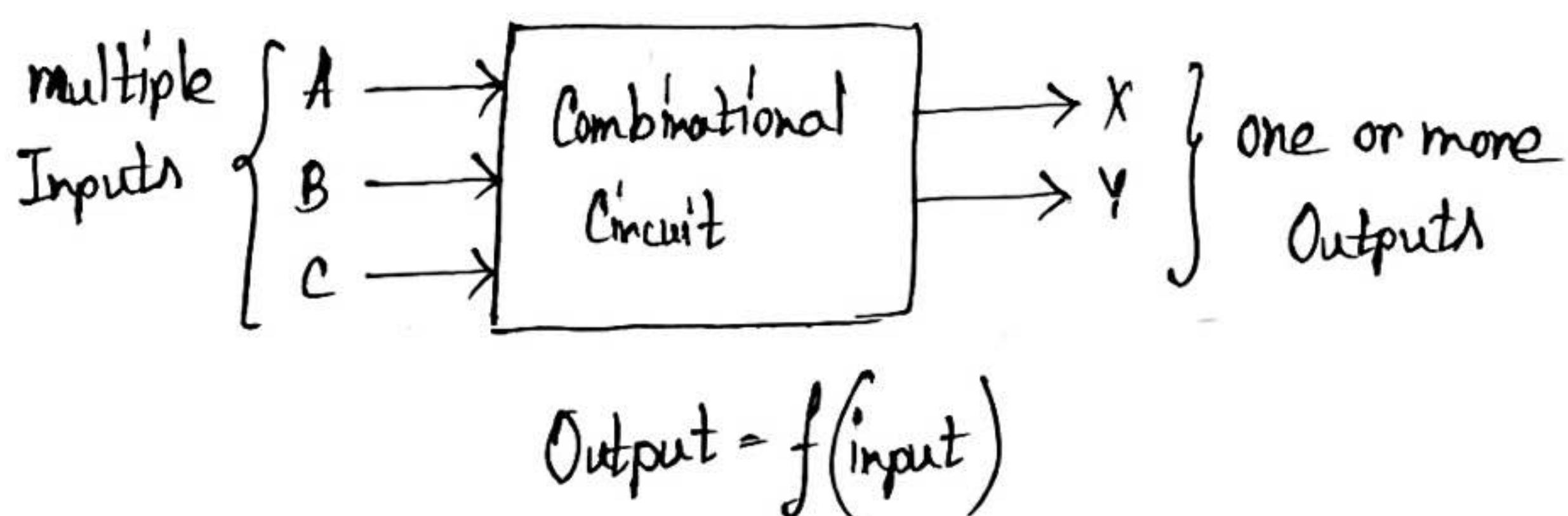


fig: Logic diagram of combinational circuit

Sequential circuit

Sequential circuit is a combinational circuit that produces an output based not only input variables, it produces an output based on current input and previous input variables. That means sequential circuits include memory elements which are capable of storing binary information. That binary information defines the state of the sequential circuit at that time.

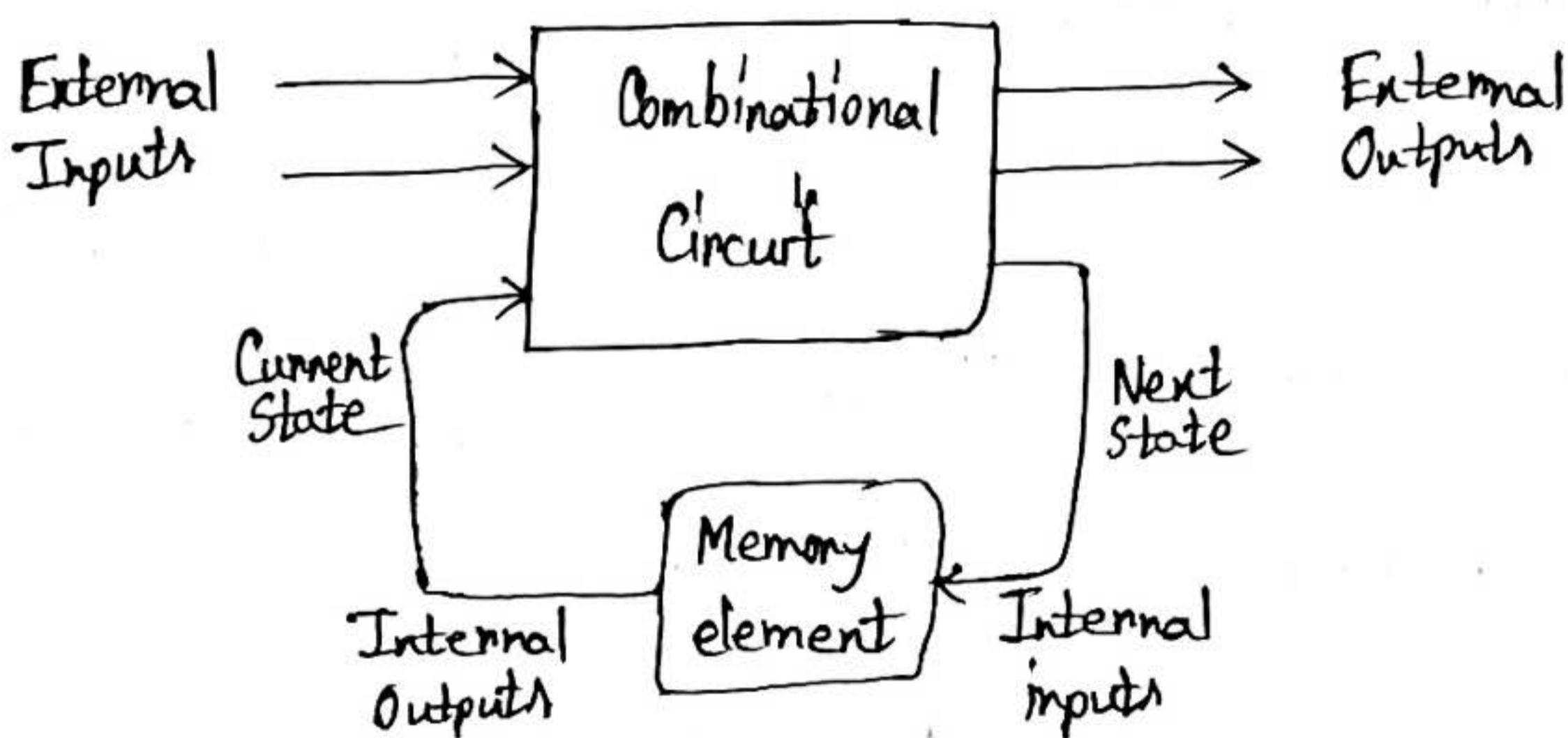


fig: Logic diagram of Sequential circuit

• There are two types of sequential circuit :

① Asynchronous sequential circuit : These circuit do not use a clock signal but uses the pulses of the inputs.

These circuit are faster than synchronous sequential circuit because there is clock pulse and change their state immediately when there is a change in the input signal.

② Synchronous sequential circuit : These circuit uses clock signal and level inputs. The output pulse is the same duration as the clock pulse for the clocked sequential circuits. Since they wait for the next clock pulse to arrive to perform the next operation, these circuits are bit slower compared to asynchronous. Level output changes state at the start of an input pulse and remains in that until next input or clock pulse.

For our project we are using synchronous sequential circuit. In our project we are portrayed "EEE-211" on seven segment display.

From the truth table we will see that for displaying 'EEE-211' we need 7 combinations (000, 001, 010, 011, 100, 101 and 110), and then it will recycle.

So it's a three bit irregular count sequence.

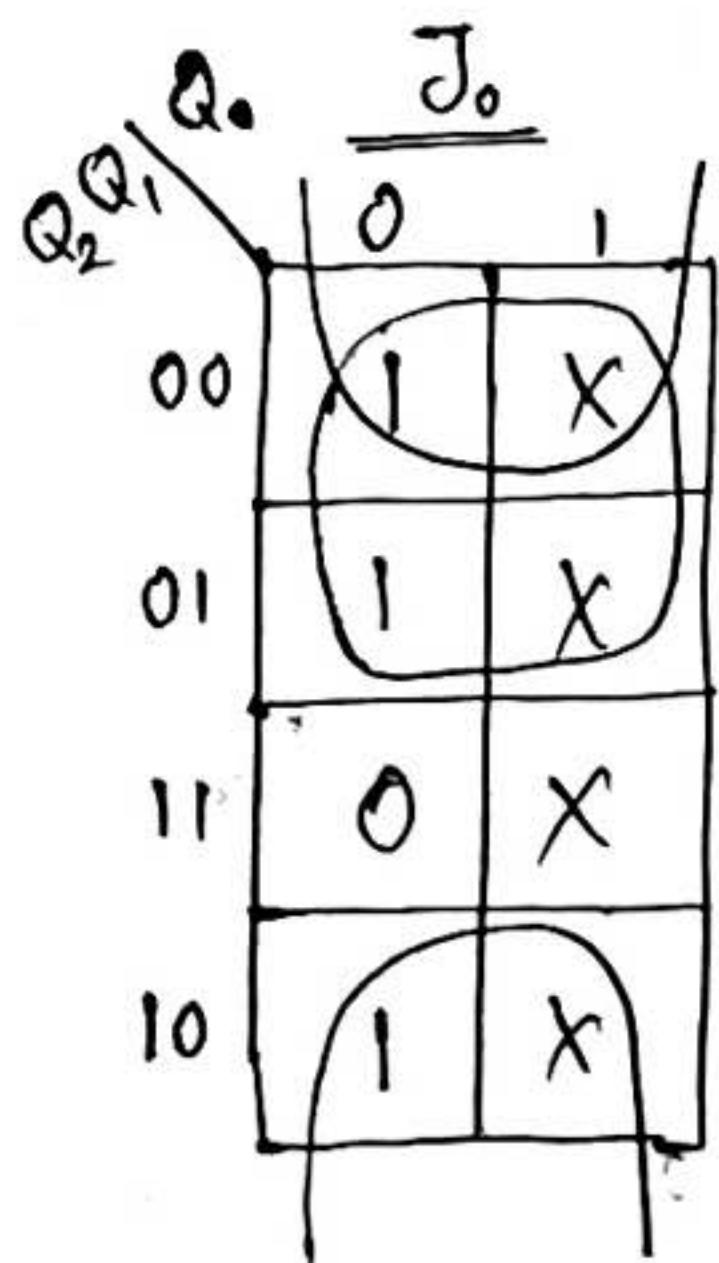
We can design this synchronous sequential circuit using JK flip flop. And the process given below:

	Present State			Next State		
	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	1
1	0	0	1	0	1	0
2	0	1	0	0	1	1
3	0	1	1	1	0	0
4	1	0	0	1	0	1
5	1	0	1	1	1	0
6	1	1	0	0	0	0

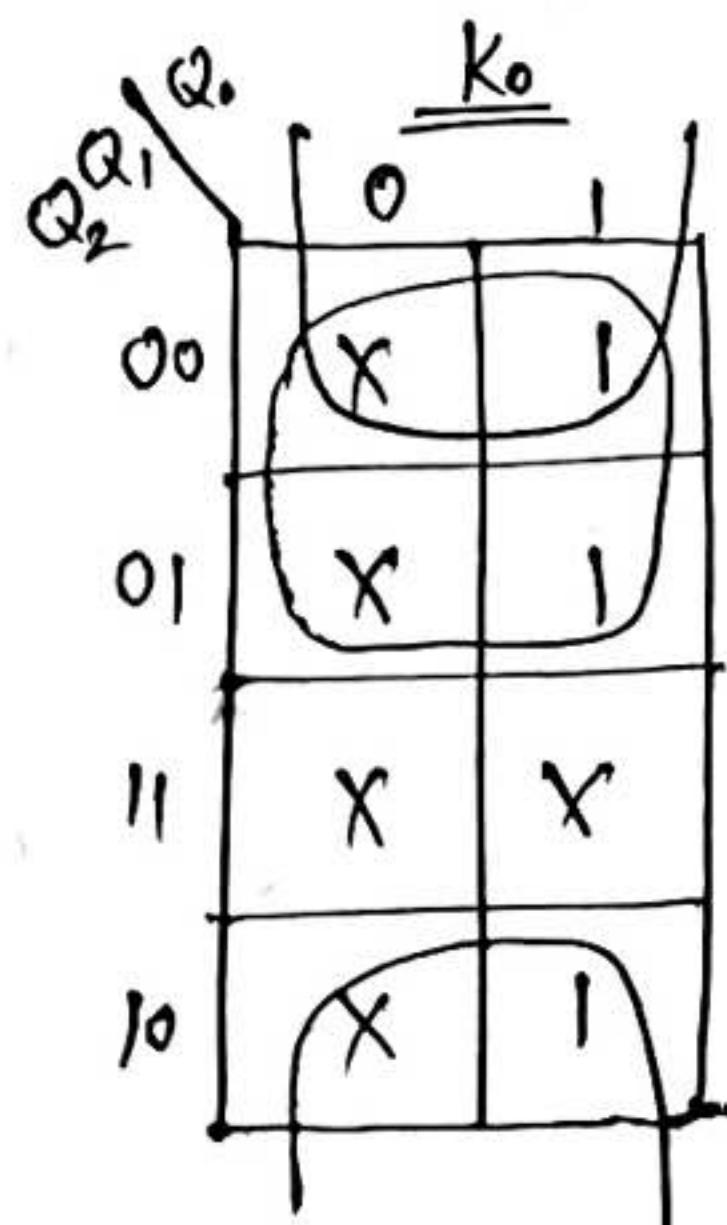
J_2	K_2	J, K_1	J_0, K_0
0	x	0x	1x
0	x	1x	x1
0	x	x0	1x
1	x	x1	x1
x	0	0x	x1
x	0	1x	1x
x	1	x1	0x

all other states are don't care.

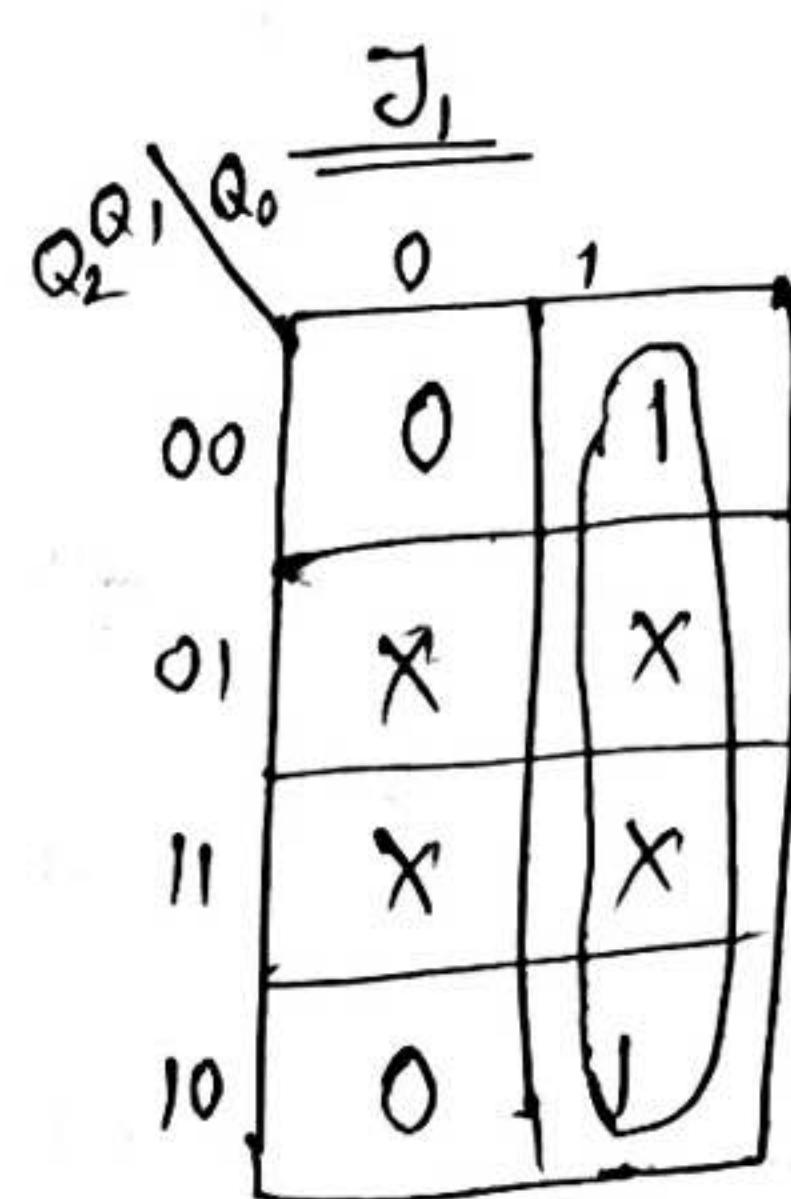
Now, K-map for $J_0, k_0, \bar{J}_1, k_1, J_2, k_2$,



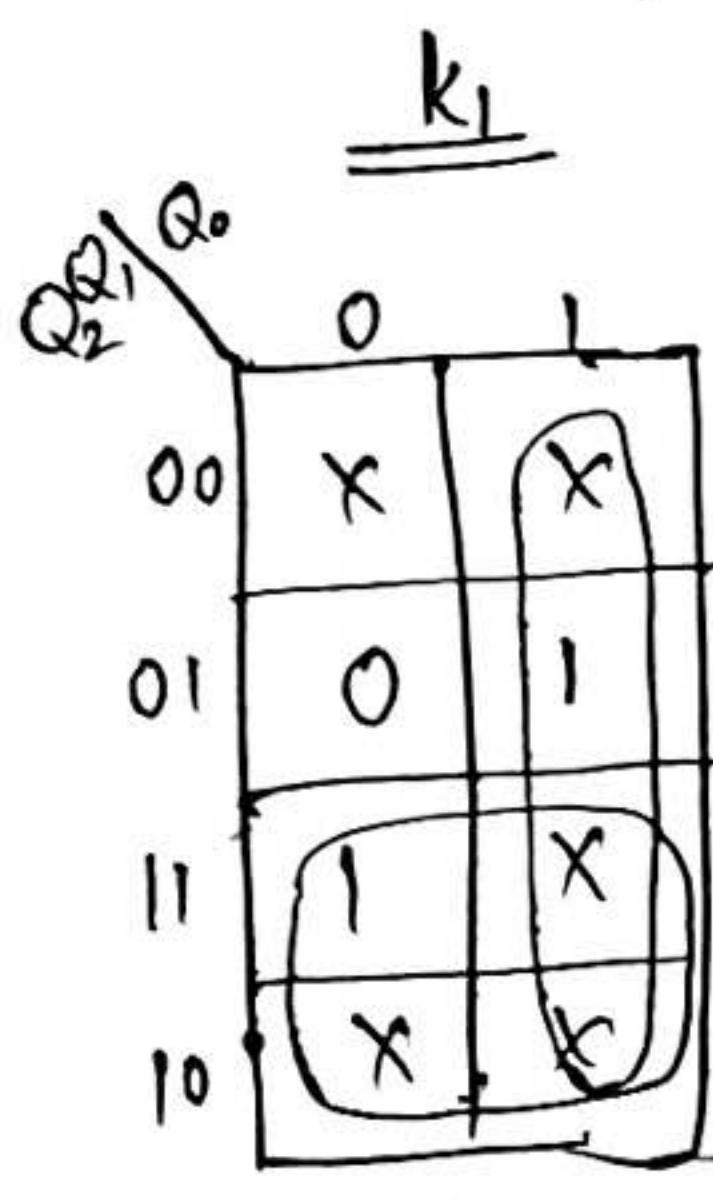
$$\therefore J_0 = \overline{Q}_1 + \overline{Q}_2$$



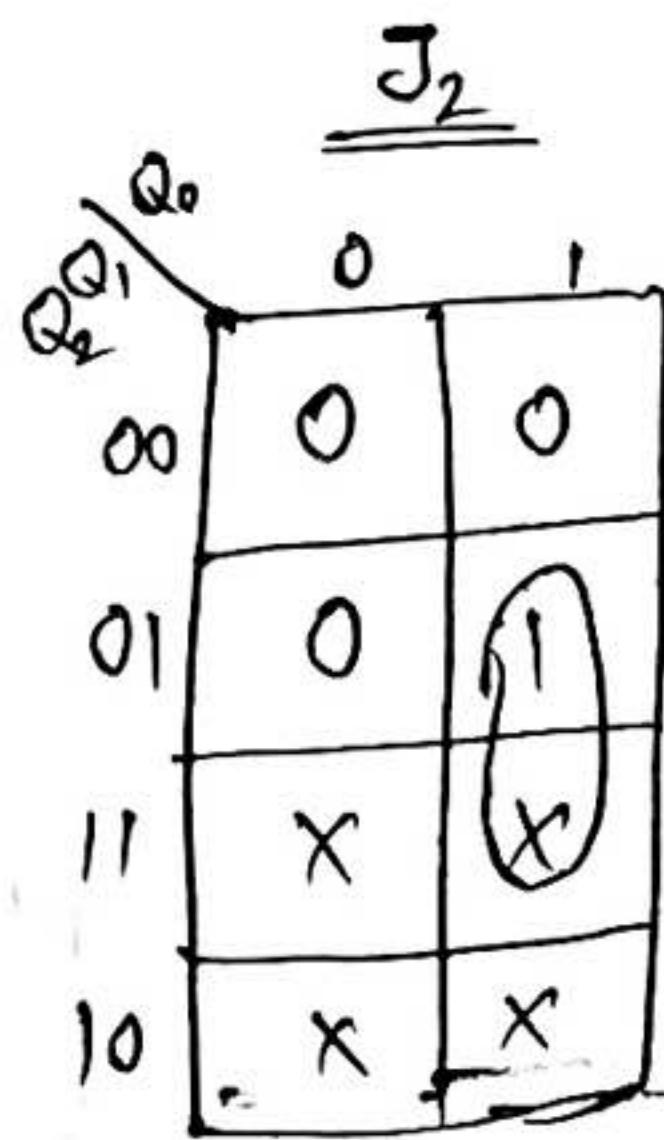
$$\therefore k_0 = \overline{Q}_1 + \overline{Q}_2$$



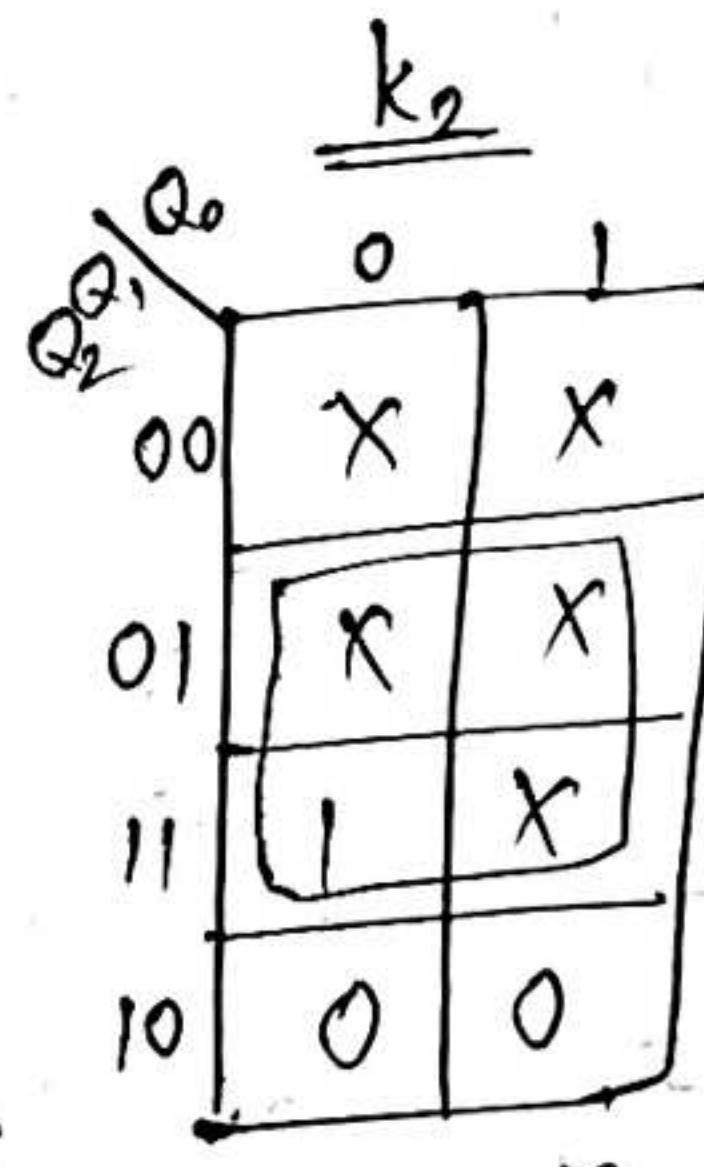
$$\therefore J_1 = Q_0$$



$$\therefore k_1 = Q_2 + Q_0$$

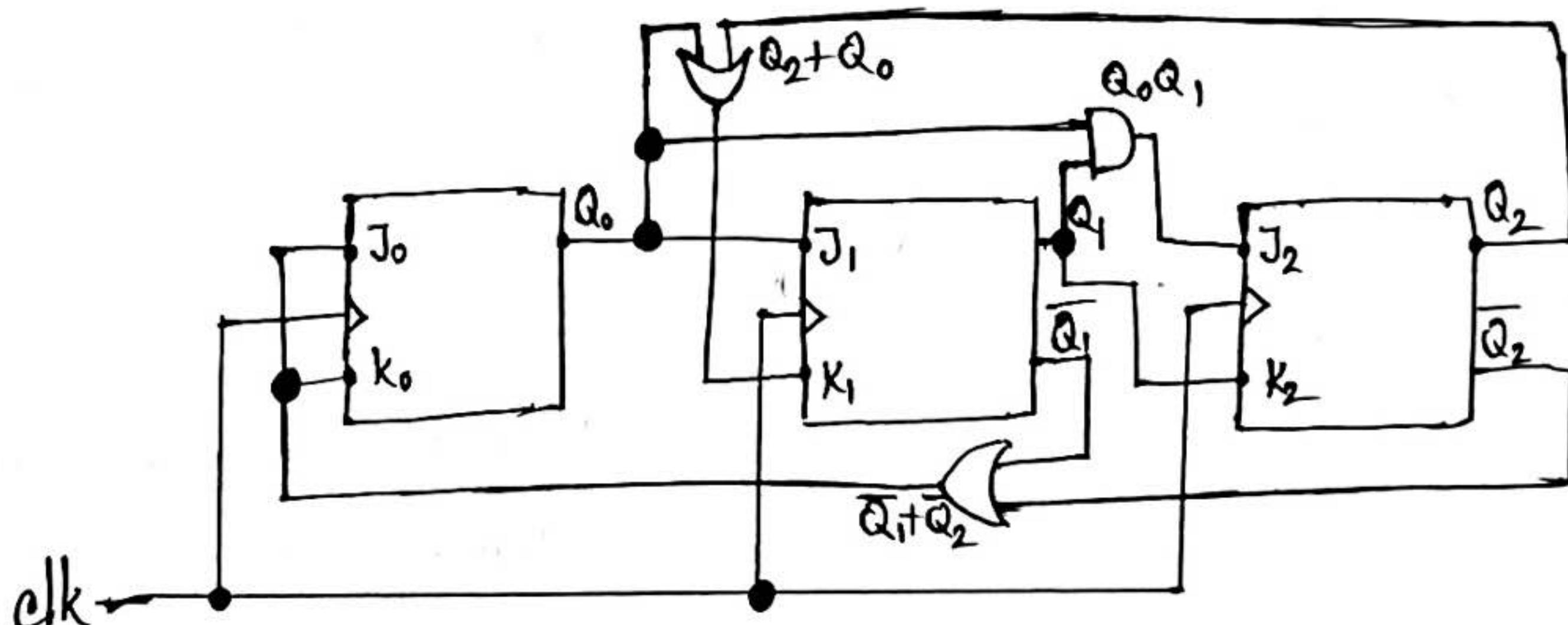


$$\therefore J_2 = Q_0 Q_1$$

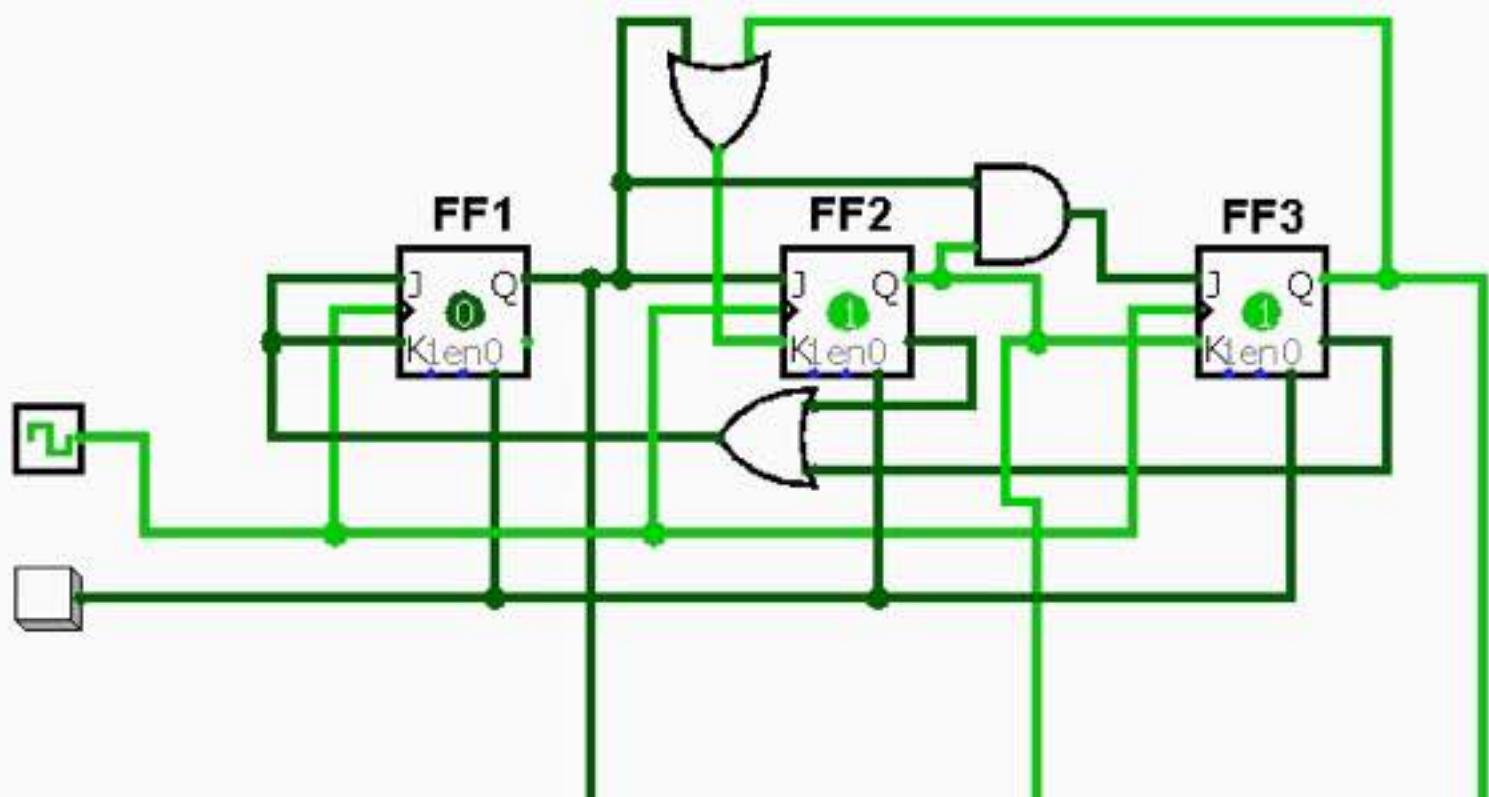


$$\therefore k_2 = Q_1$$

So, the 3-bit synchronous counter for our circuit will,



3 bit Synchronous counter for our project



Combinational circuit using NAND

Our project on 'EEE-211'. let's point it,

$$E \rightarrow f \bar{f} \frac{\sigma}{e \bar{e} g}$$

$$E \rightarrow f \overline{l}^a - g \overline{l}^b$$

$$E \rightarrow f_1 = a \\ e_1 = g$$

- → -g

$$2 \rightarrow \frac{a}{l^b} e l^{\frac{a}{l}}$$

$$1 \rightarrow \begin{matrix} 1_b \\ 1_c \end{matrix}$$

$$1 \rightarrow \frac{1}{1}^b c$$

Truth Table :

Derive the equation using Sum Of Product (SOP):

$$a = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + xy\bar{z}$$

$$b = x\bar{y}\bar{z} + x\bar{y}z + xy\bar{z}$$

$$c = x\bar{y}z + xy\bar{z}$$

$$d = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + xy\bar{z}$$

$$e = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + xy\bar{z}$$

$$f = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z}$$

$$g = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + \bar{x}yz + xy\bar{z}$$

But by using the SOP, the equations are too large to simplify. So, we can convert the into small equation using the K-Map.

For a:

$$a = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}\bar{z} + \bar{x}y\bar{z} + x\bar{y}\bar{z}$$

K-map

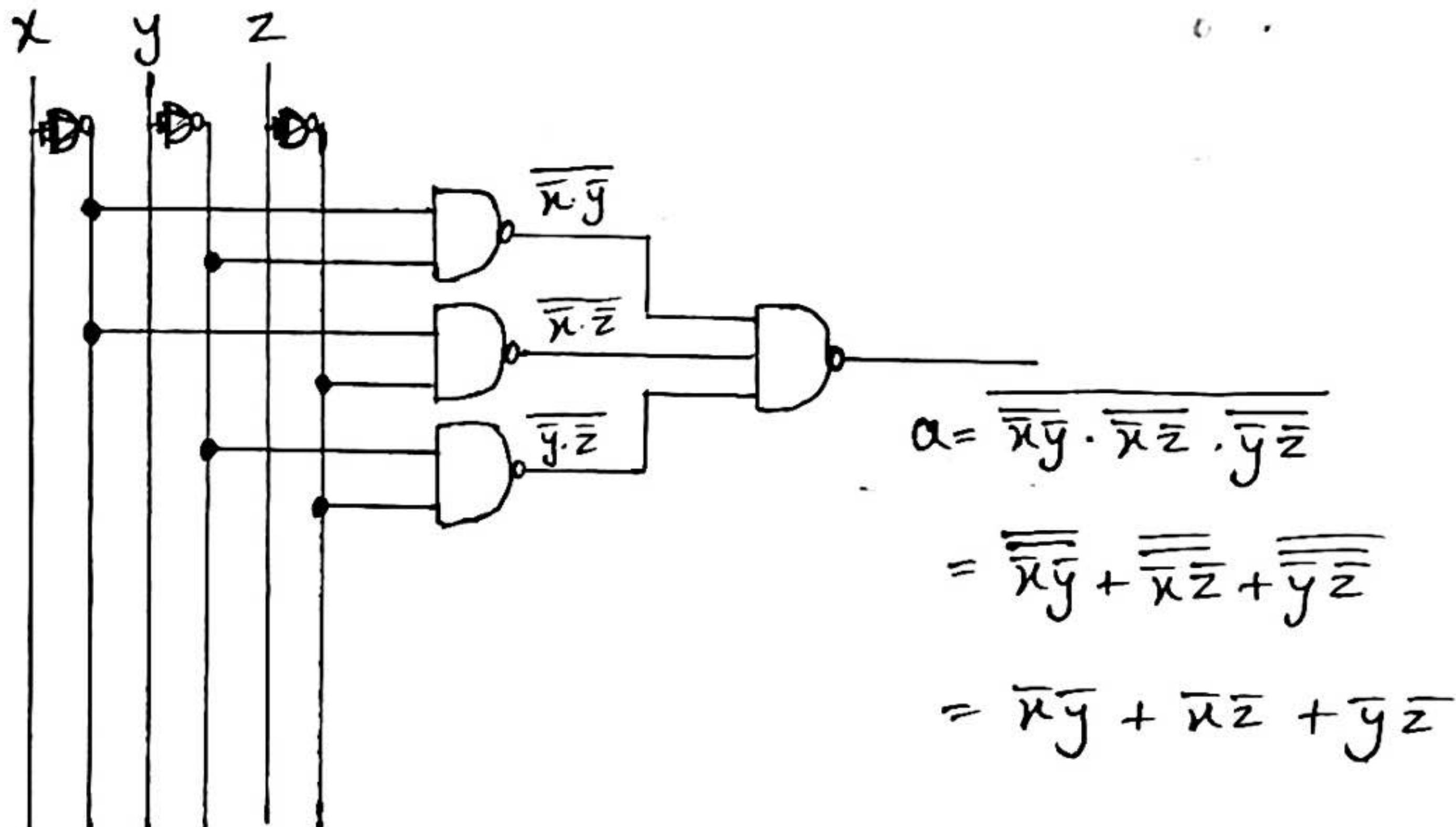
		yz	00	01	11	10	.
		x	0	1	1	0	1
		0	1	1	0	1	
		1	1	0	x	0	

$$\therefore a = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$

Circuit diagram using NAND

$$a = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$

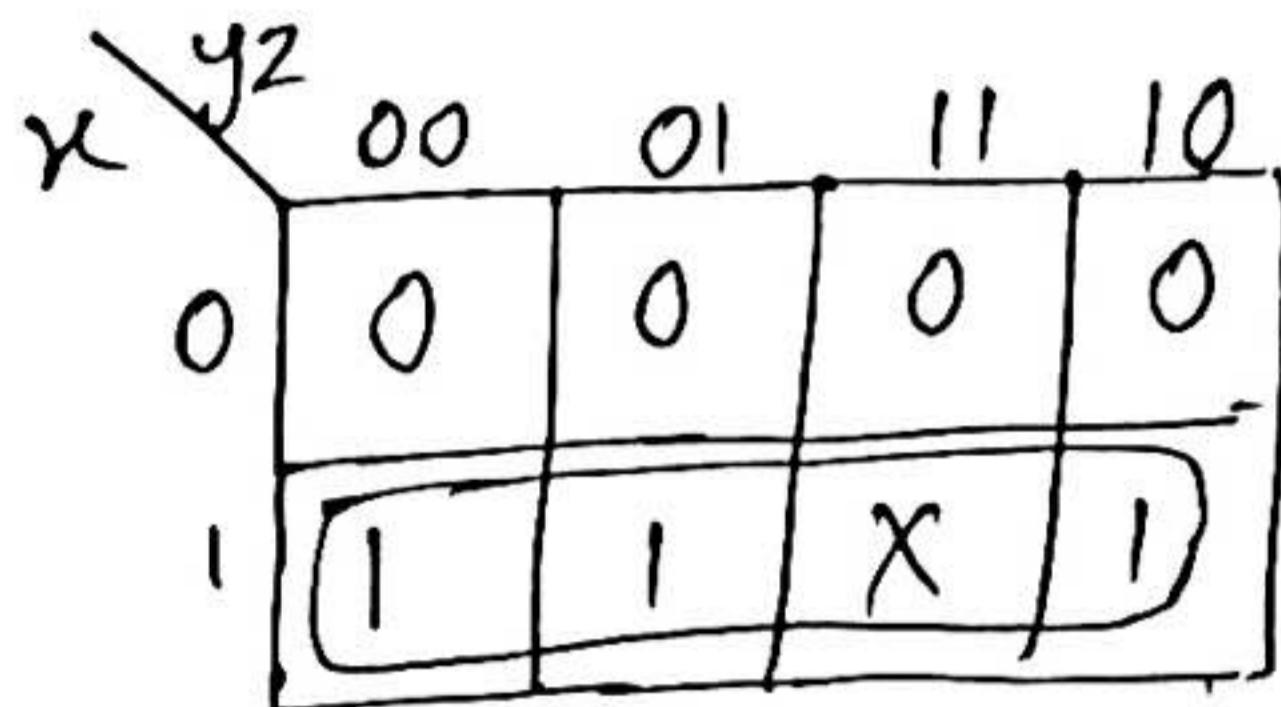
$$= \overline{\overline{x}\bar{y}} \cdot \overline{\overline{x}\bar{z}} \cdot \overline{\bar{y}\bar{z}}$$



For b:

$$b = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + xy\bar{z}$$

K-map

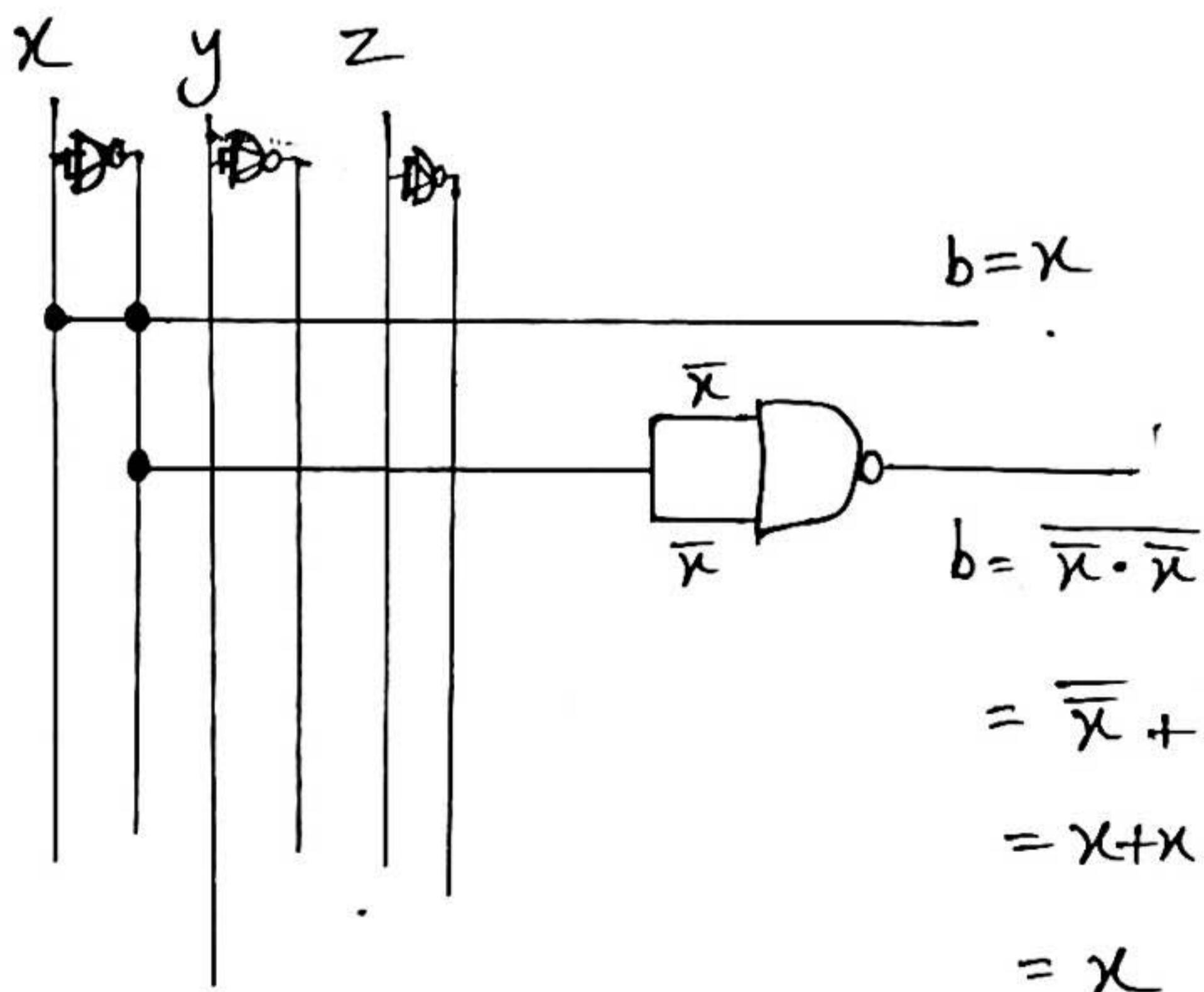


$$\therefore b = x$$

Circuit diagram using NAND

$$b = x = x + x$$

$$= \bar{x} + \bar{x} = \overline{\bar{x} \cdot \bar{x}}$$



For C

$$C = \bar{x}\bar{y}z + xy\bar{z}$$

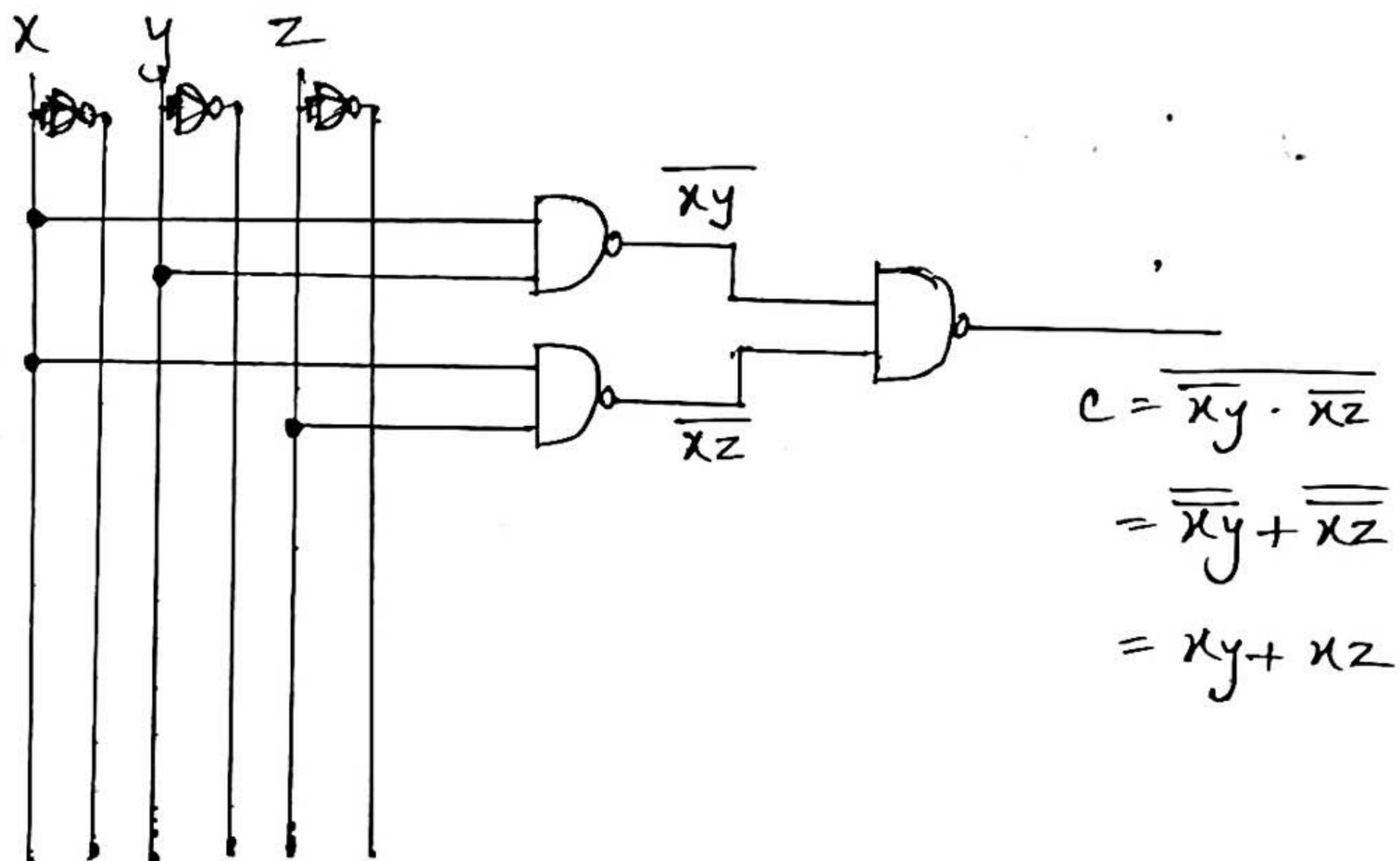
K-map

		yz	00	01	11	10
		x	0	0	0	0
		1	0	1	X	1

$$\therefore C = \bar{x}y + xz$$

Circuit diagram using NAND

$$\begin{aligned}C &= \bar{x}y + xz \\&= \overline{\overline{x}\bar{y}} \cdot \overline{\overline{x}z}\end{aligned}$$



For d

$$d = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + xy\bar{z}$$

K-map

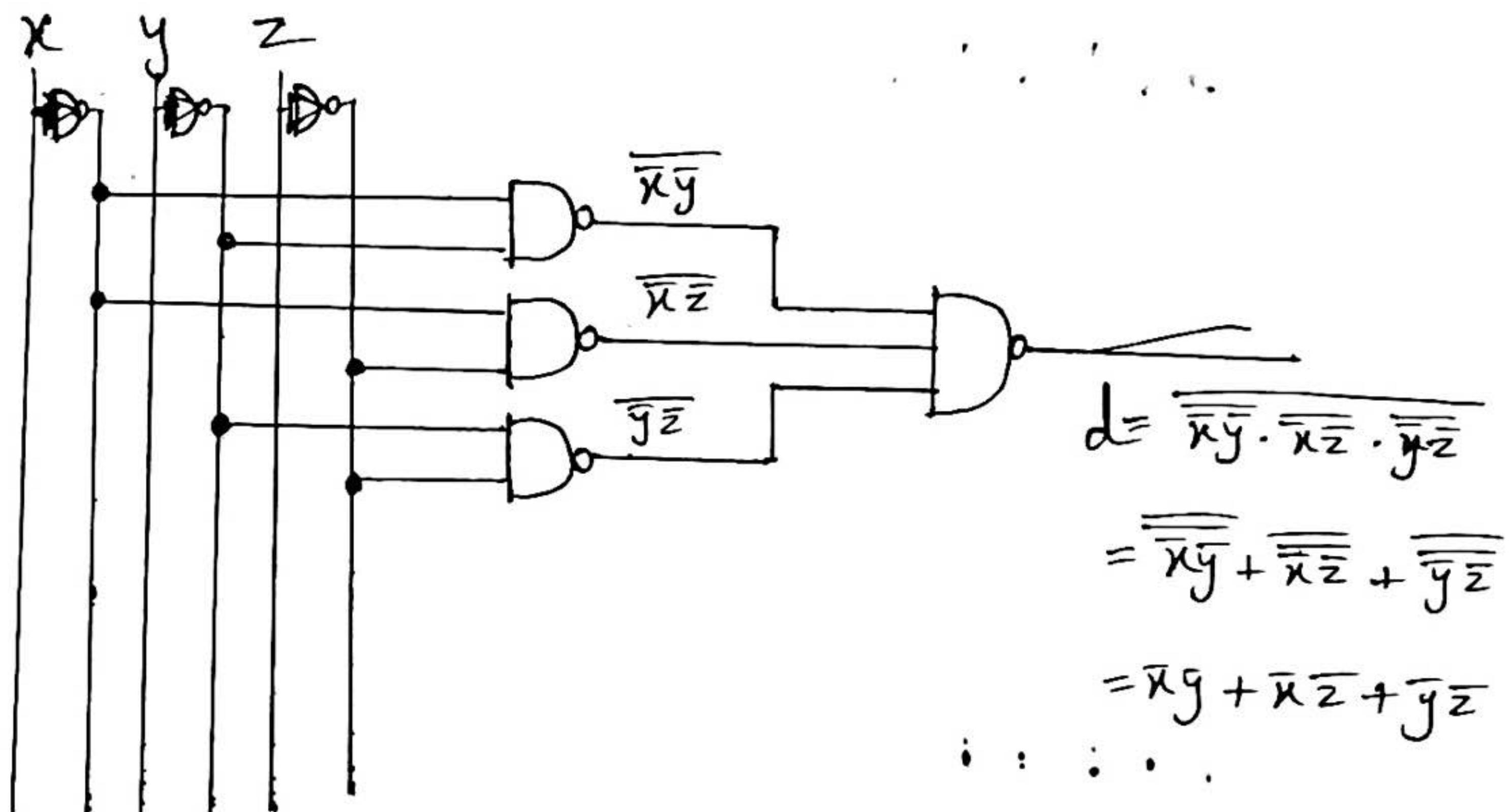
		yz	00	01	11	10
		x	0	1	0	1
y	z	0	1	0	X	0
		1	0	0	X	0

$$\therefore d = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$

Circuit diagram using NAND

$$d = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$

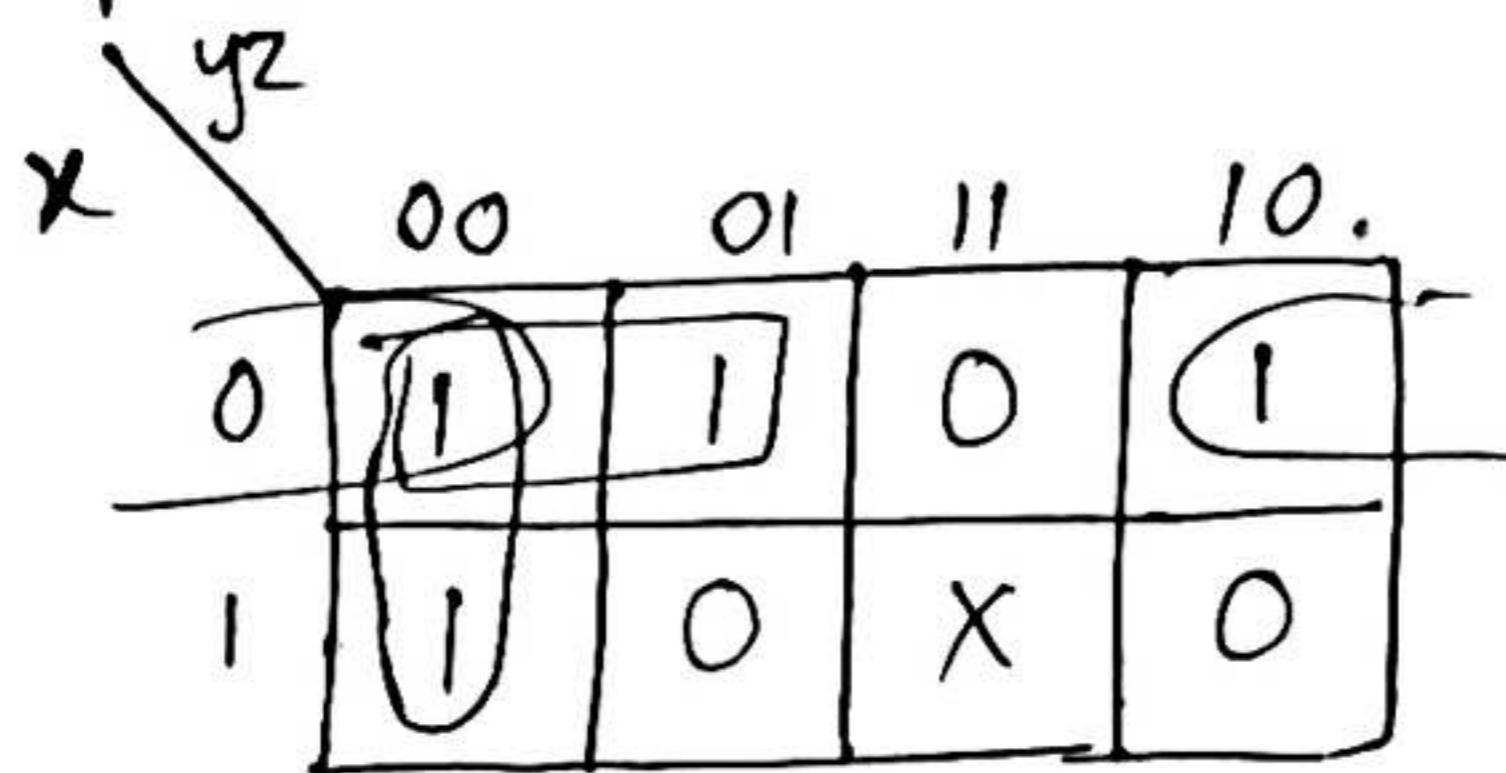
$$= \overline{\overline{x}\bar{y}} \cdot \overline{\overline{x}\bar{z}} \cdot \overline{\overline{y}\bar{z}}$$



For e

$$e = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}yz + xy\bar{z}$$

K-map

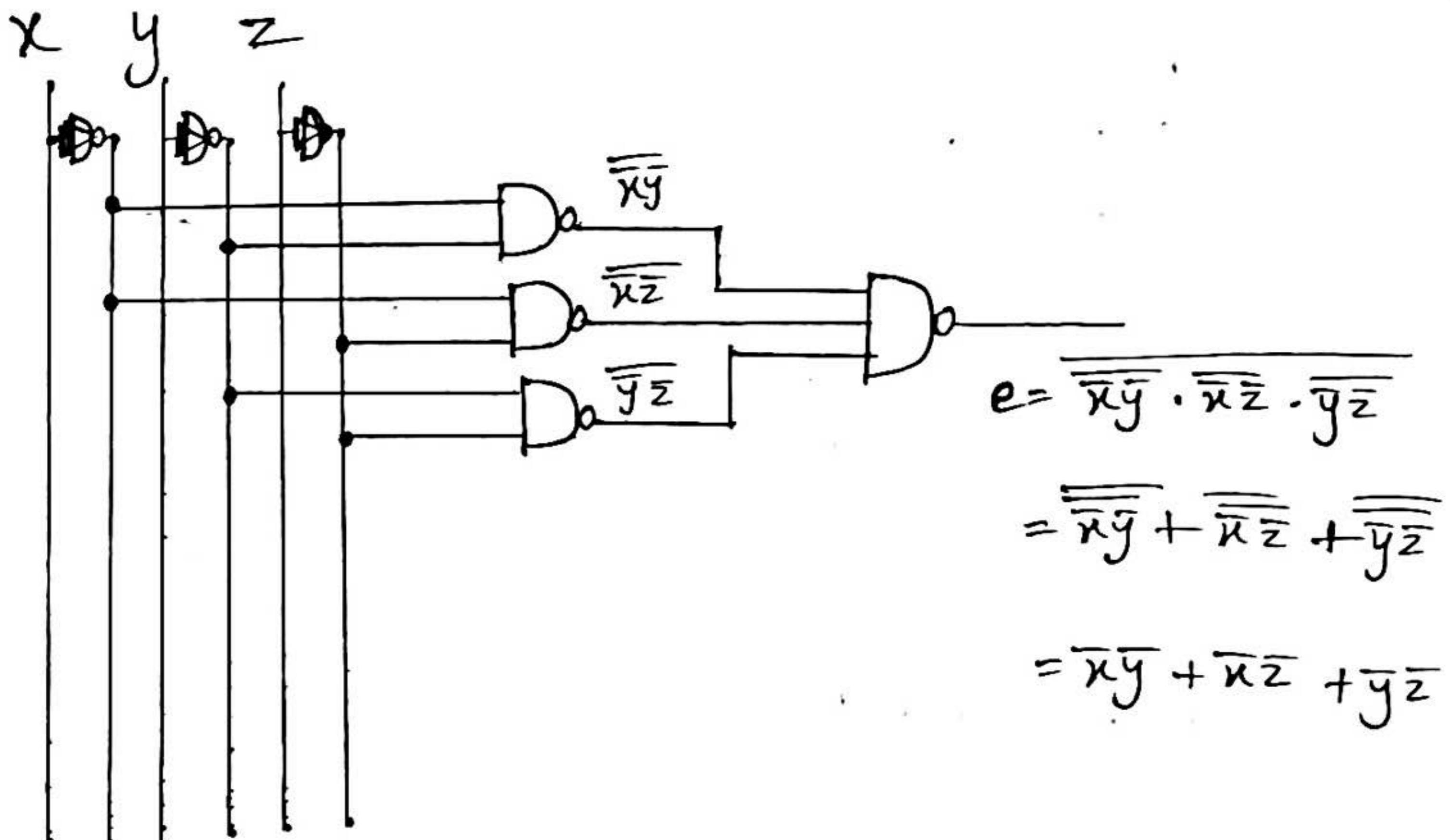


$$\therefore e = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$

Circuit diagram using NAND

$$e = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$

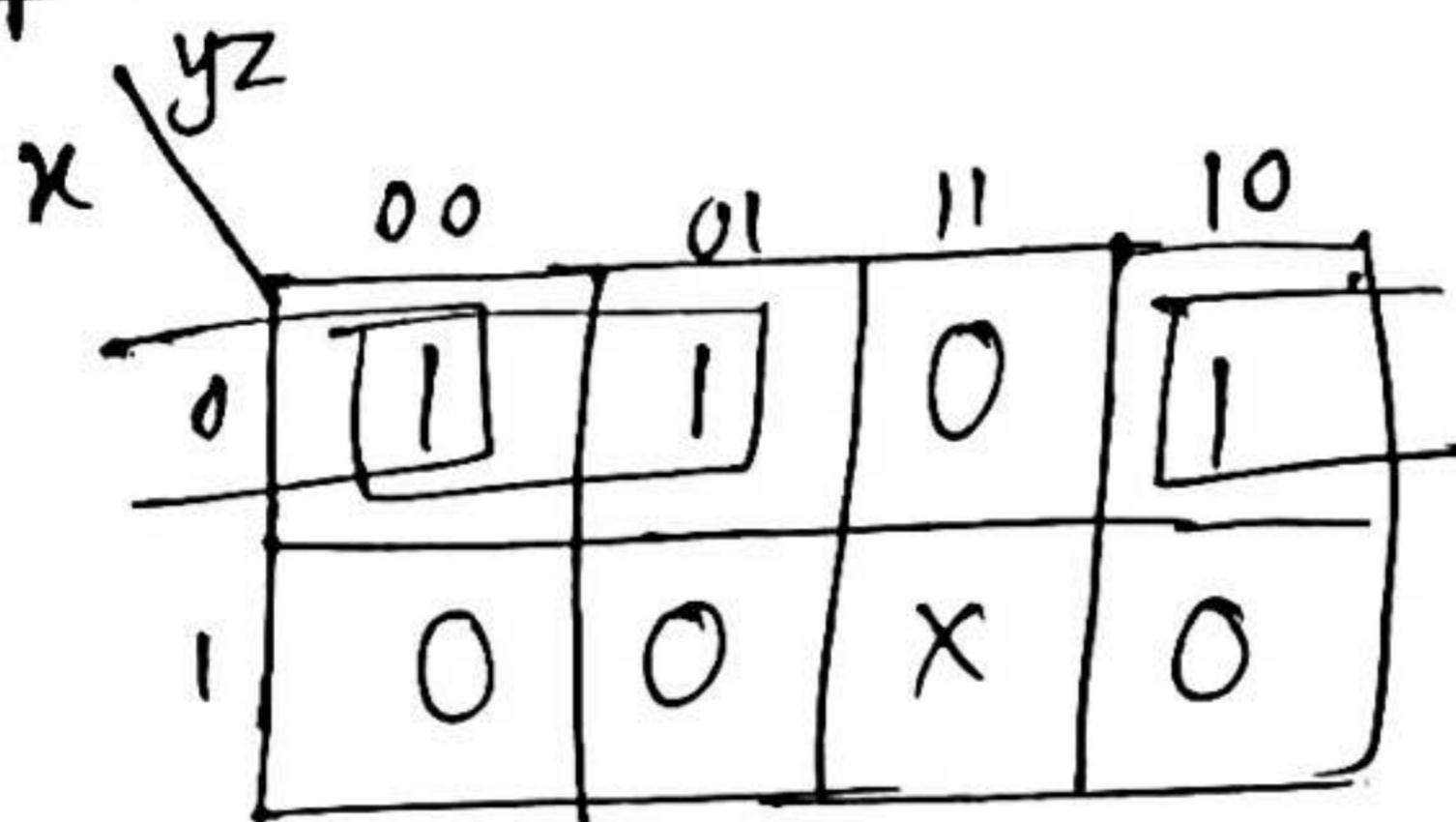
$$= \overline{\overline{\bar{x}\bar{y}}} \cdot \overline{\overline{\bar{x}\bar{z}}} \cdot \overline{\overline{\bar{y}\bar{z}}}$$



For f

$$f = \overline{x}\overline{y}\overline{z} + \overline{x}\overline{y}z + \overline{x}yz$$

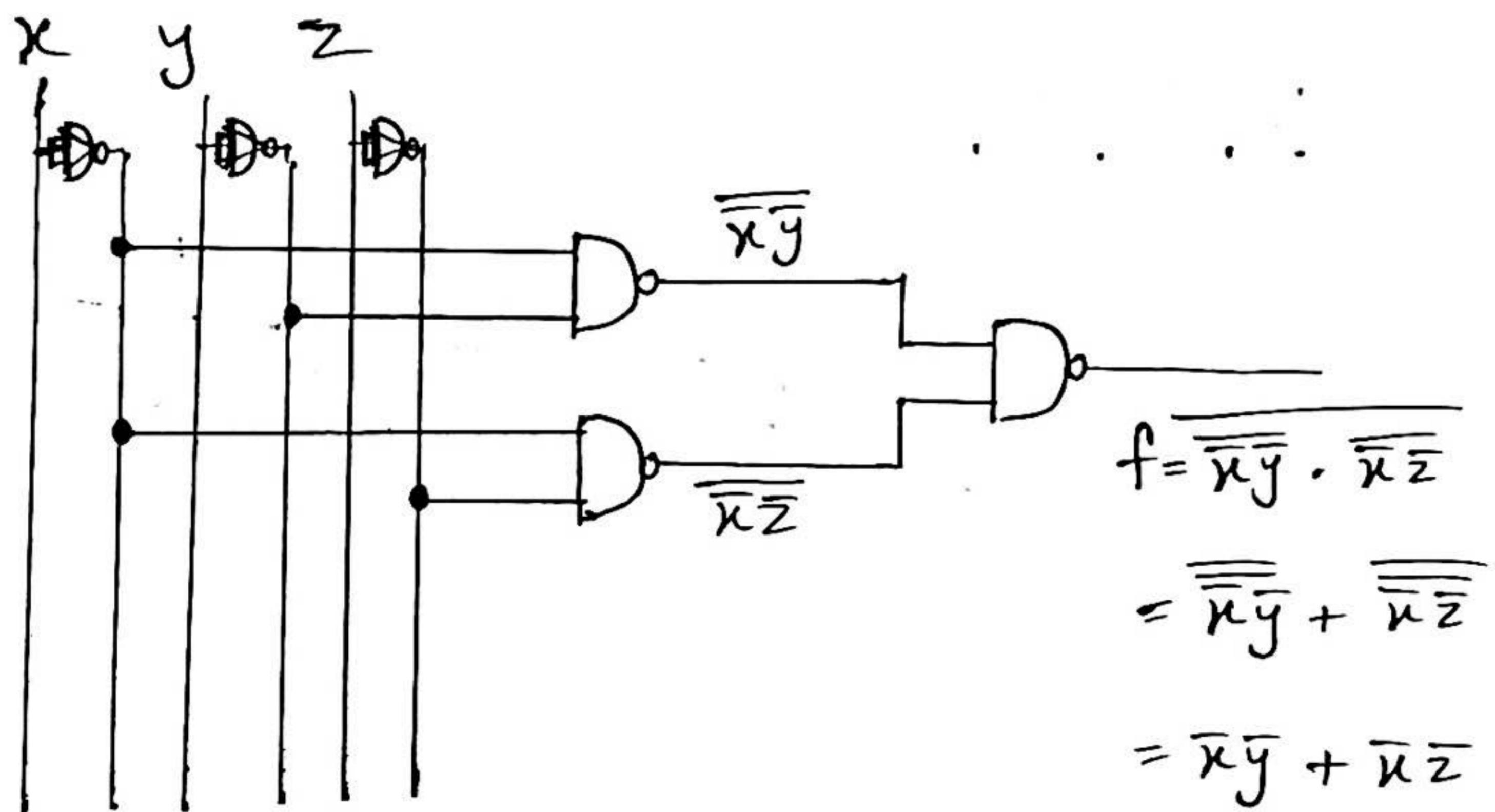
K-map



$$\therefore f = \overline{x}\overline{y} + \overline{x}\overline{z}$$

Circuit diagram using NAND

$$\begin{aligned}f &= \overline{x}\overline{y} + \overline{x}\overline{z} \\&= \overline{\overline{x}\overline{y}} \cdot \overline{\overline{x}\overline{z}}\end{aligned}$$



For g

$$g = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}yz + \bar{x}yz + x\bar{y}\bar{z}$$

K-map

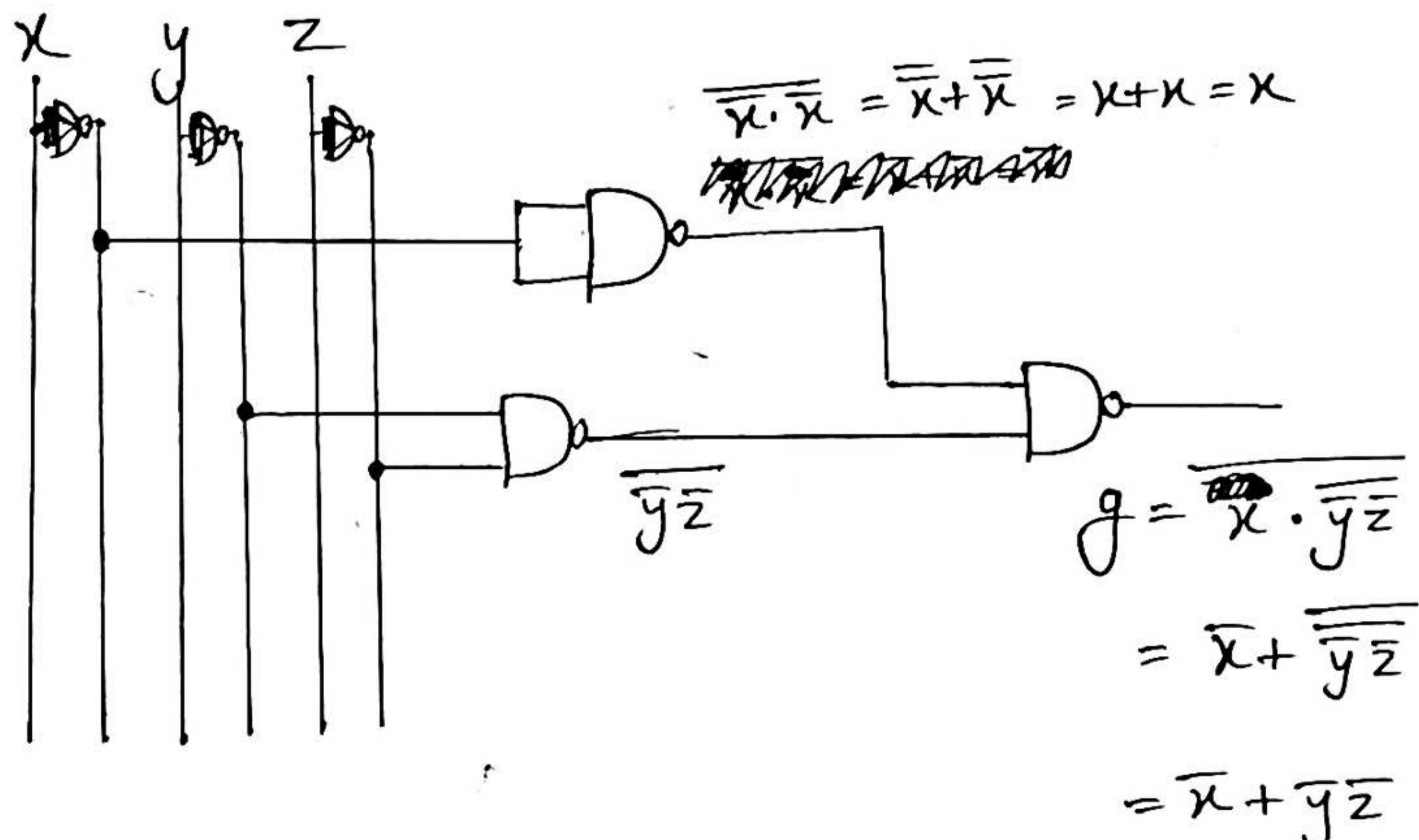
		00	01	11	10
		0	1	1	1
		1	0	x	0
x	yz				

$$\therefore f = \bar{x} + \bar{y}\bar{z}$$

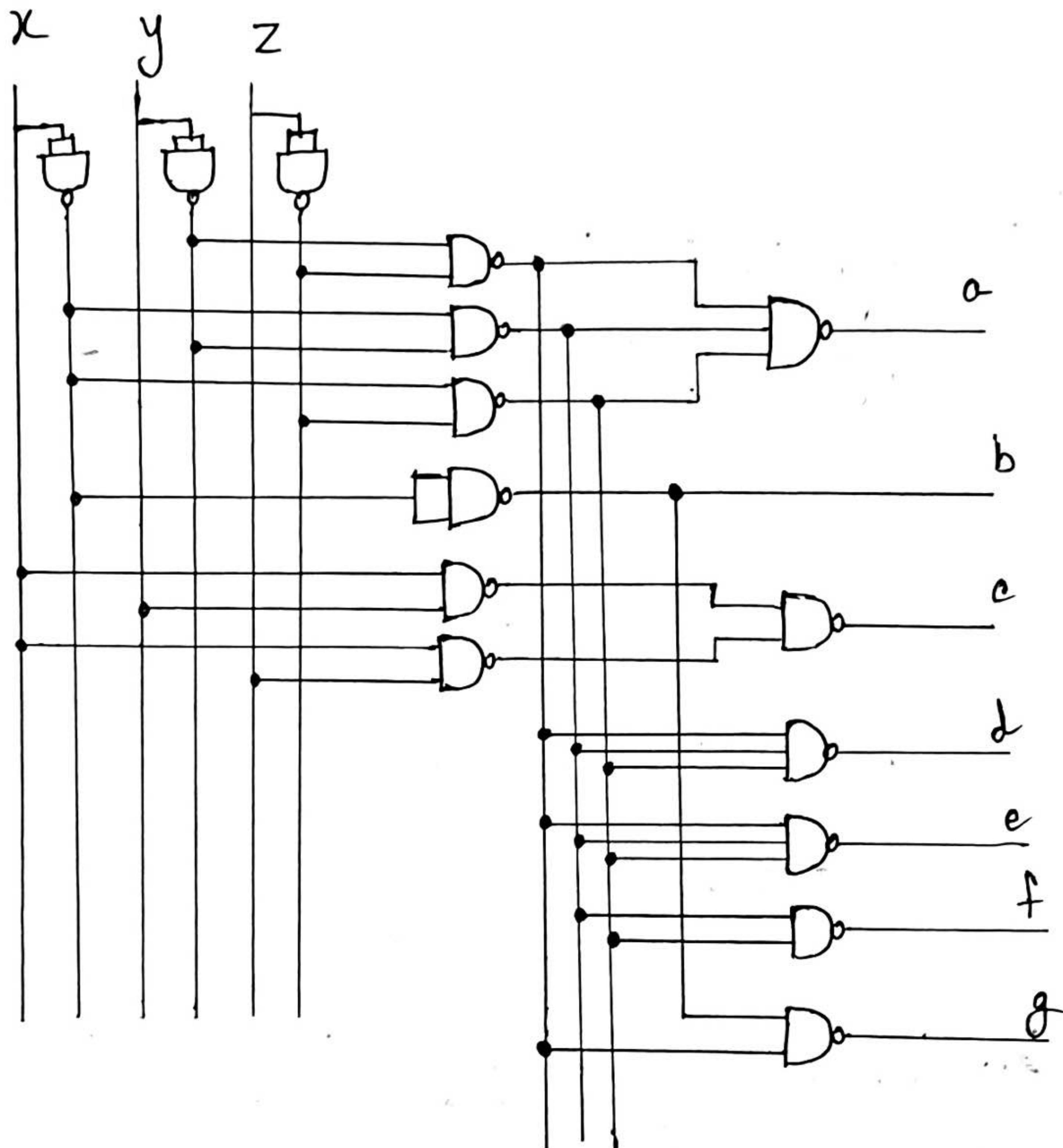
Circuit diagram using NAND

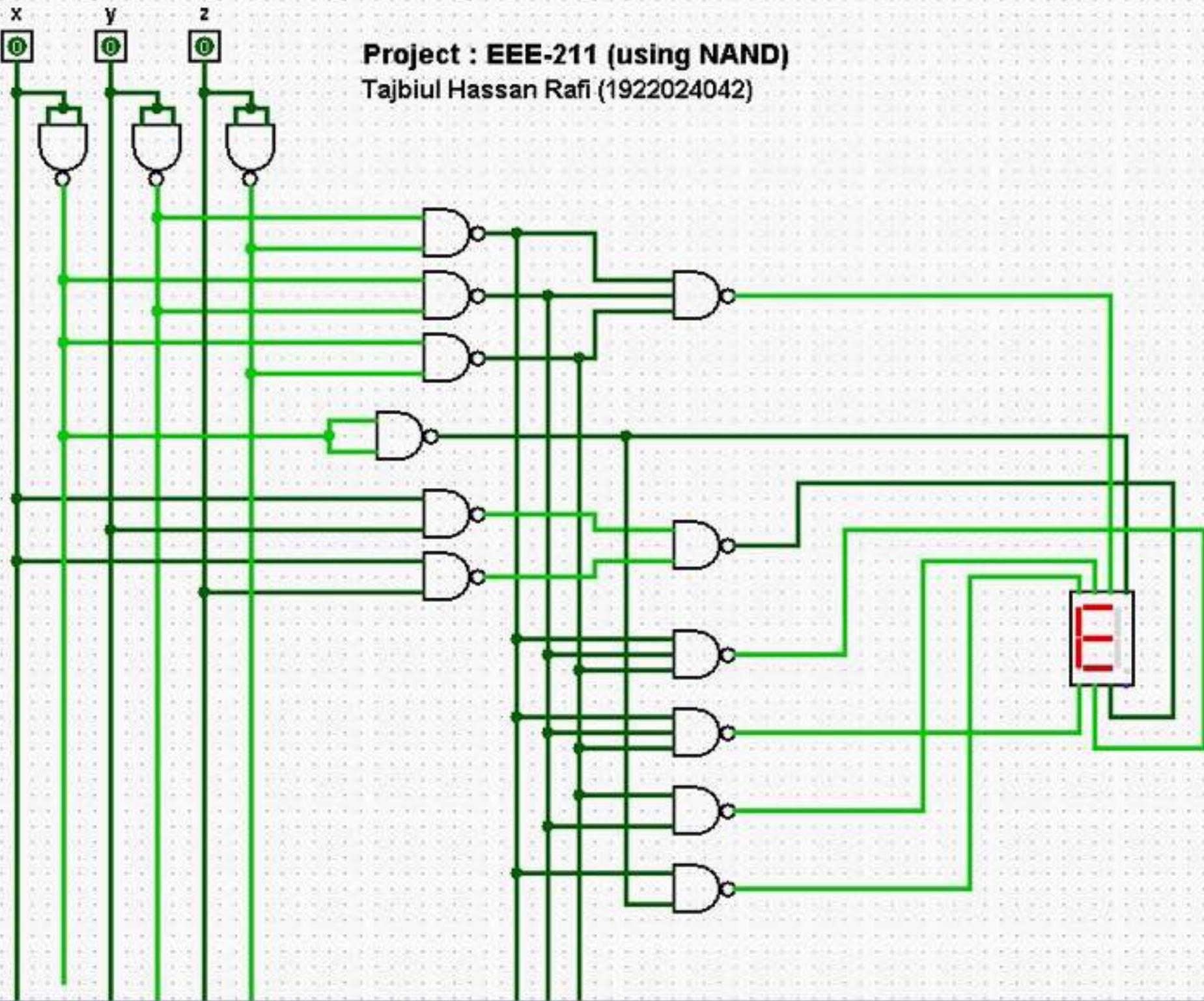
$$f = \bar{x} + \bar{y}\bar{z} = \overline{\overline{x} \cdot \overline{x}} \cdot \overline{\bar{y}\bar{z}}$$

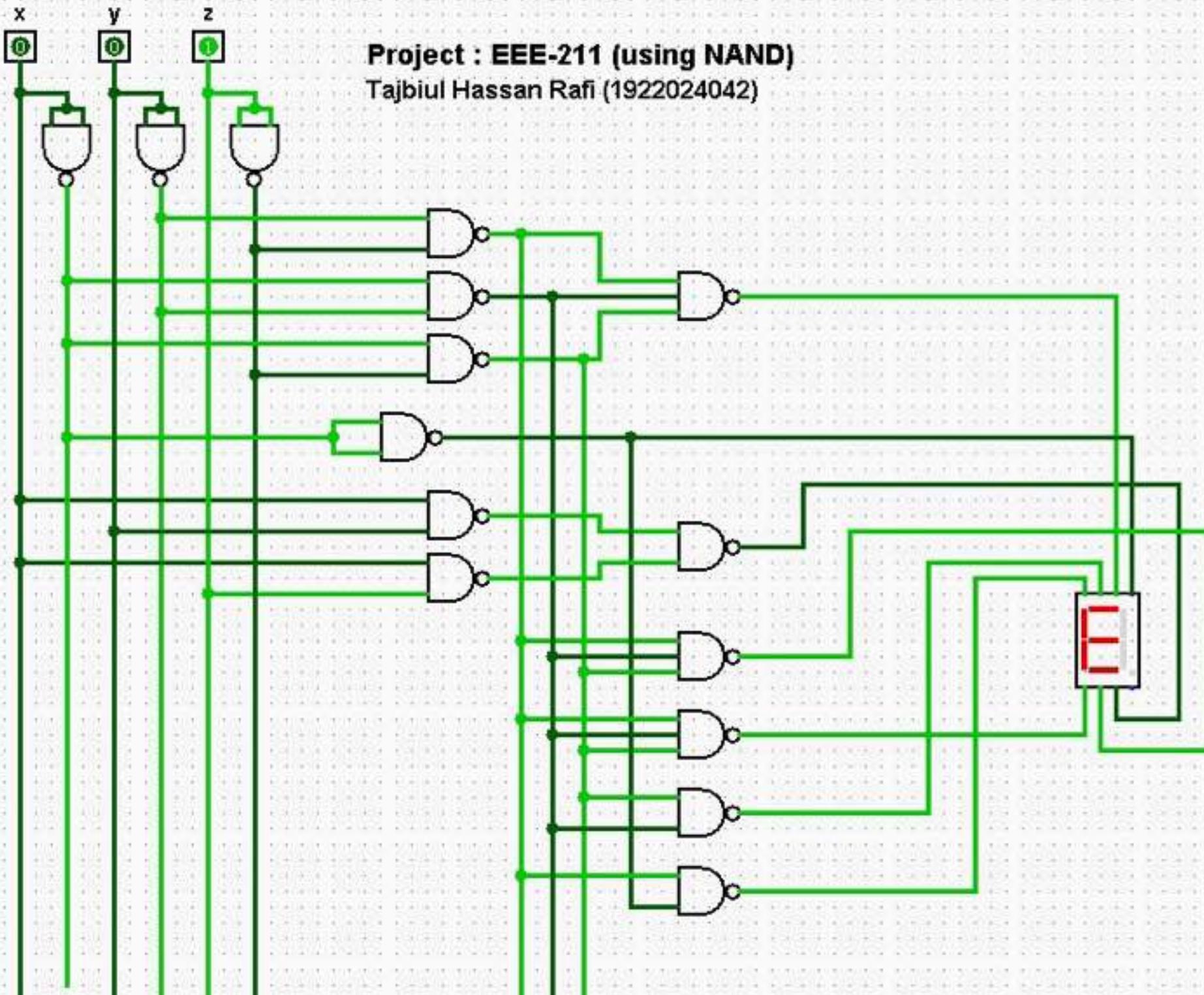
~~XXXXXXXXXX~~



Circuit diagram: Using Universal (NAND) gate.

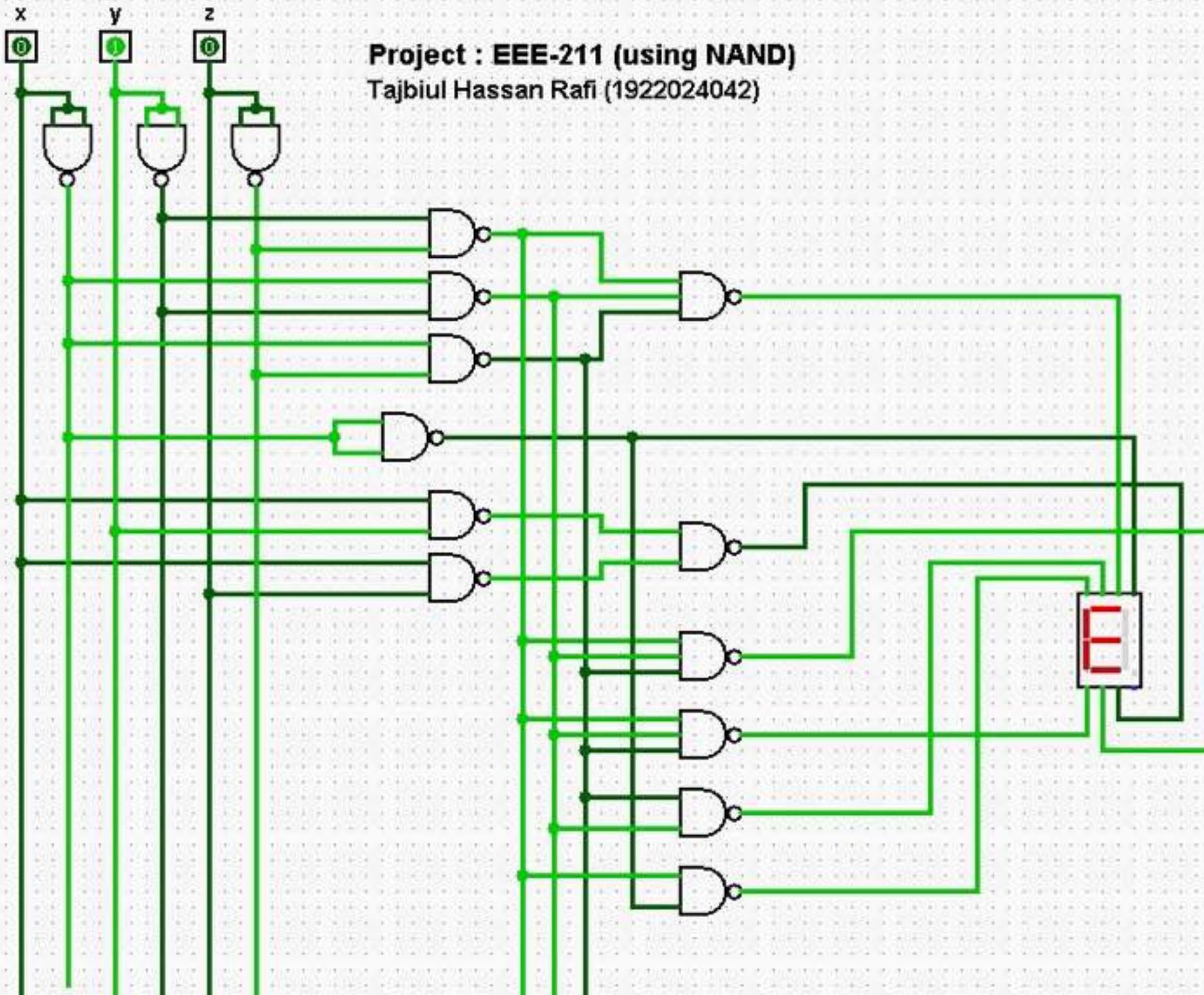


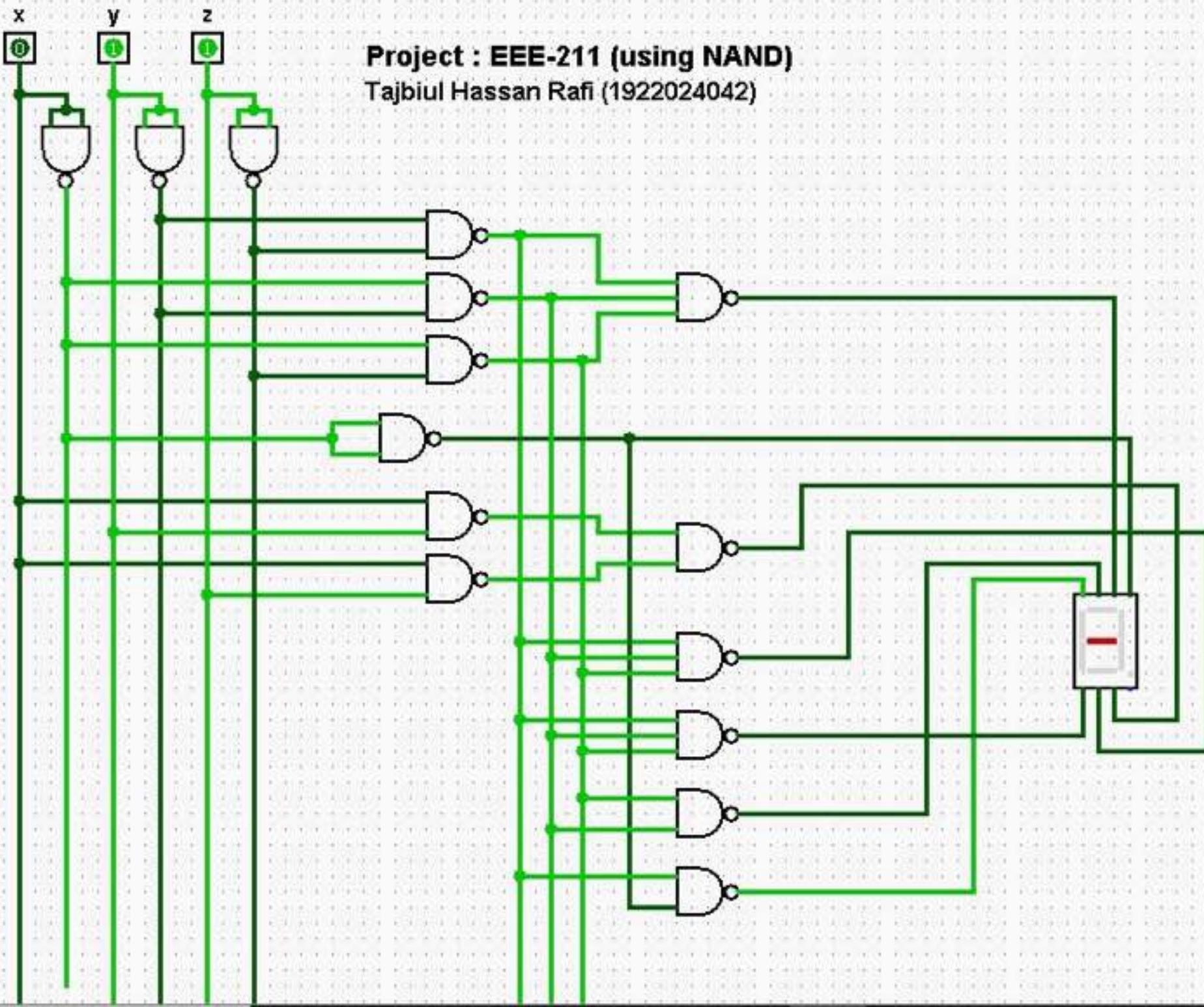


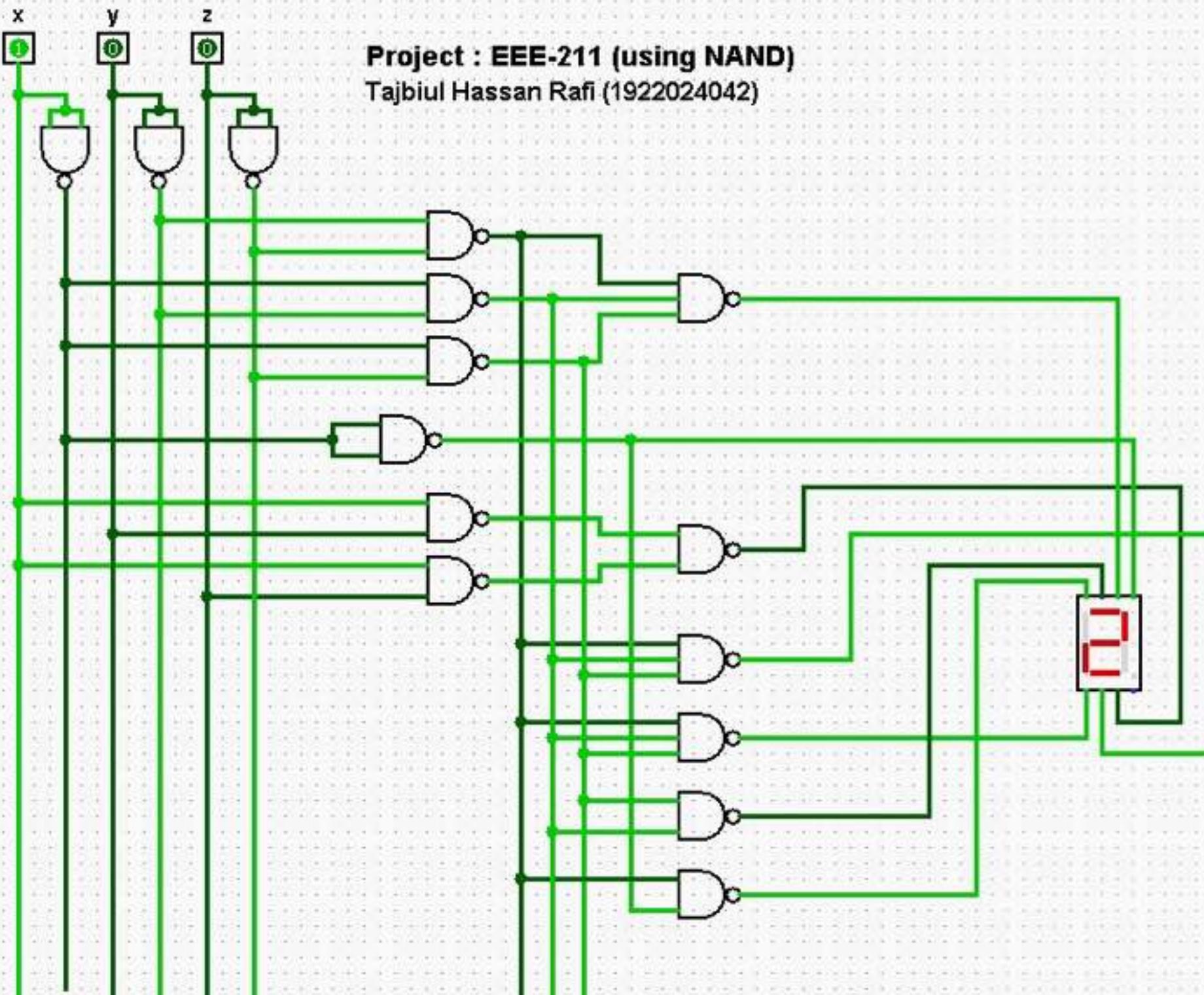


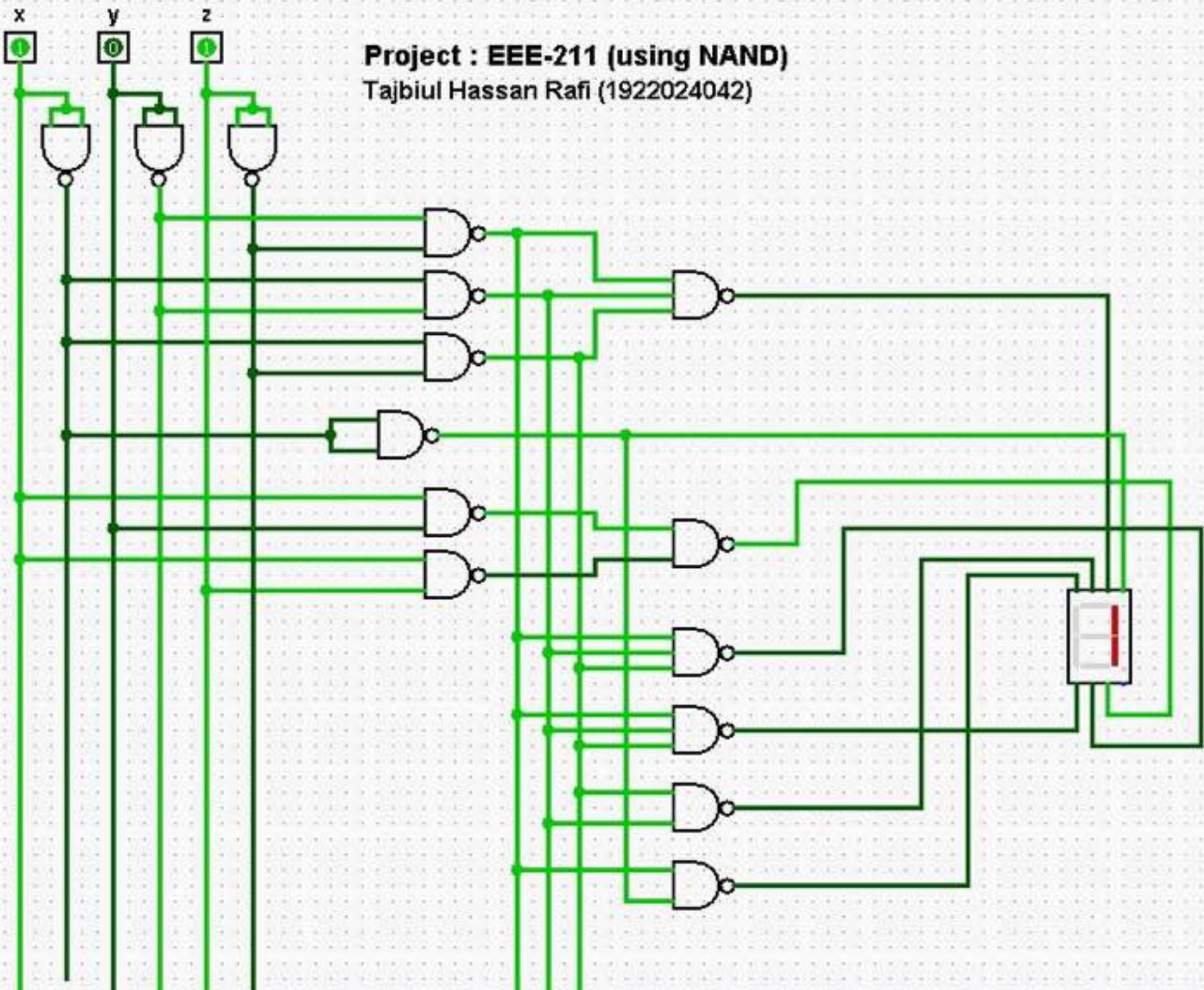
Project : EEE-211 (using NAND)

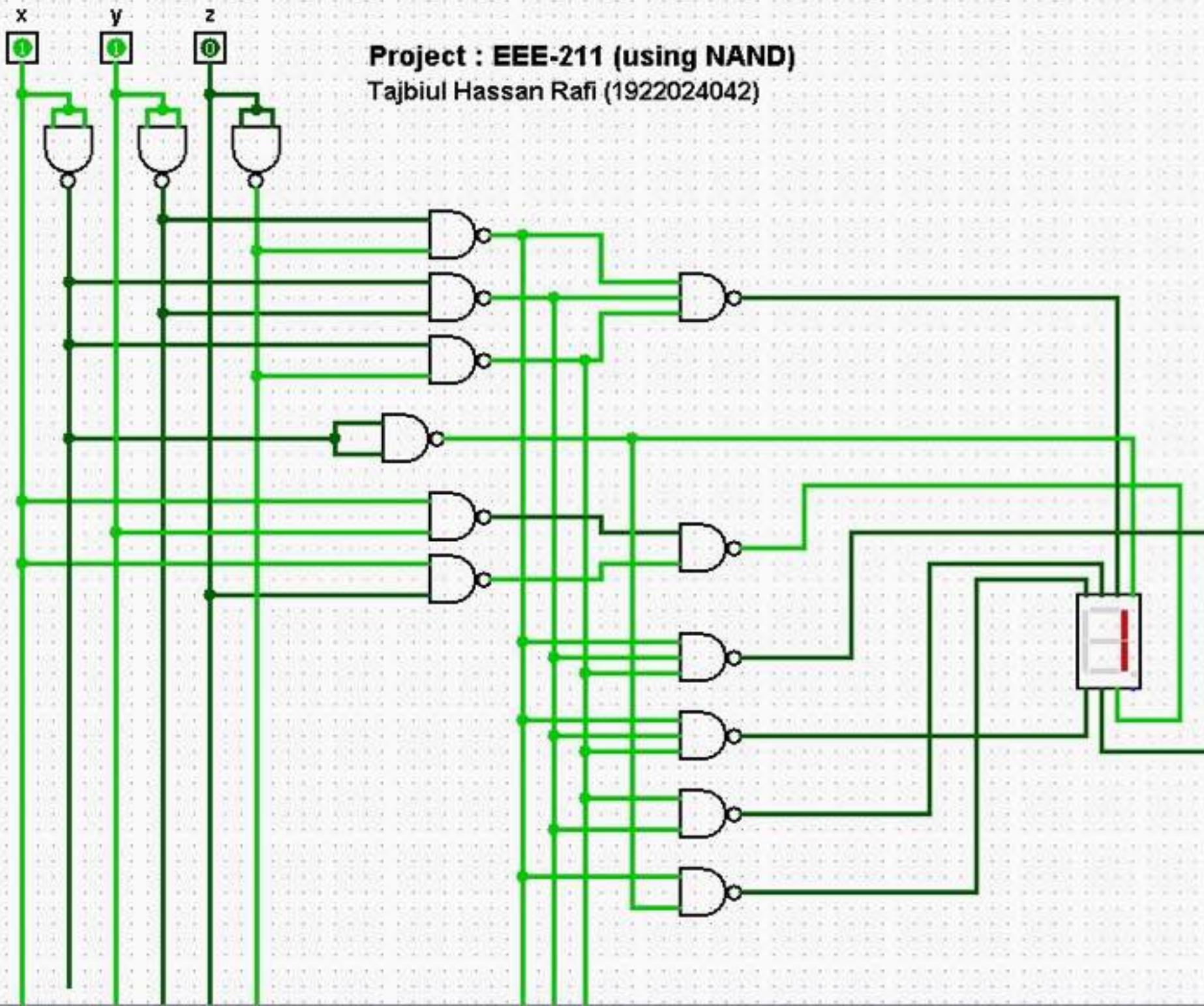
Tajbiul Hassan Rafi (1922024042)



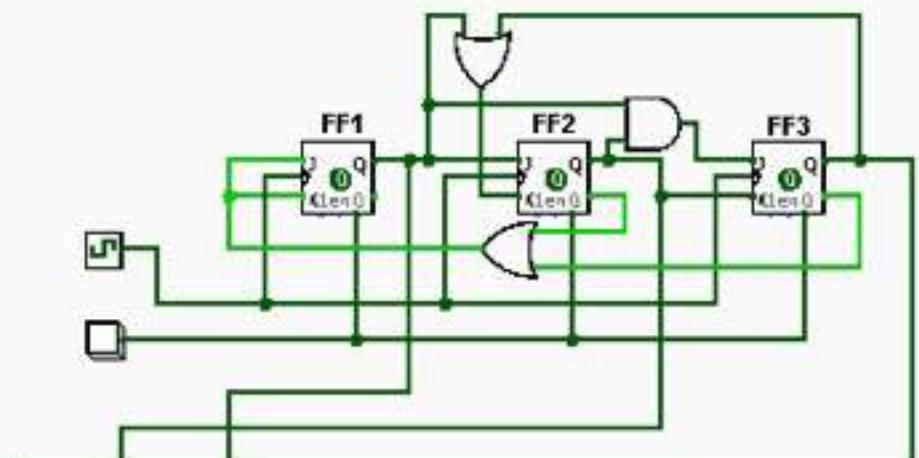




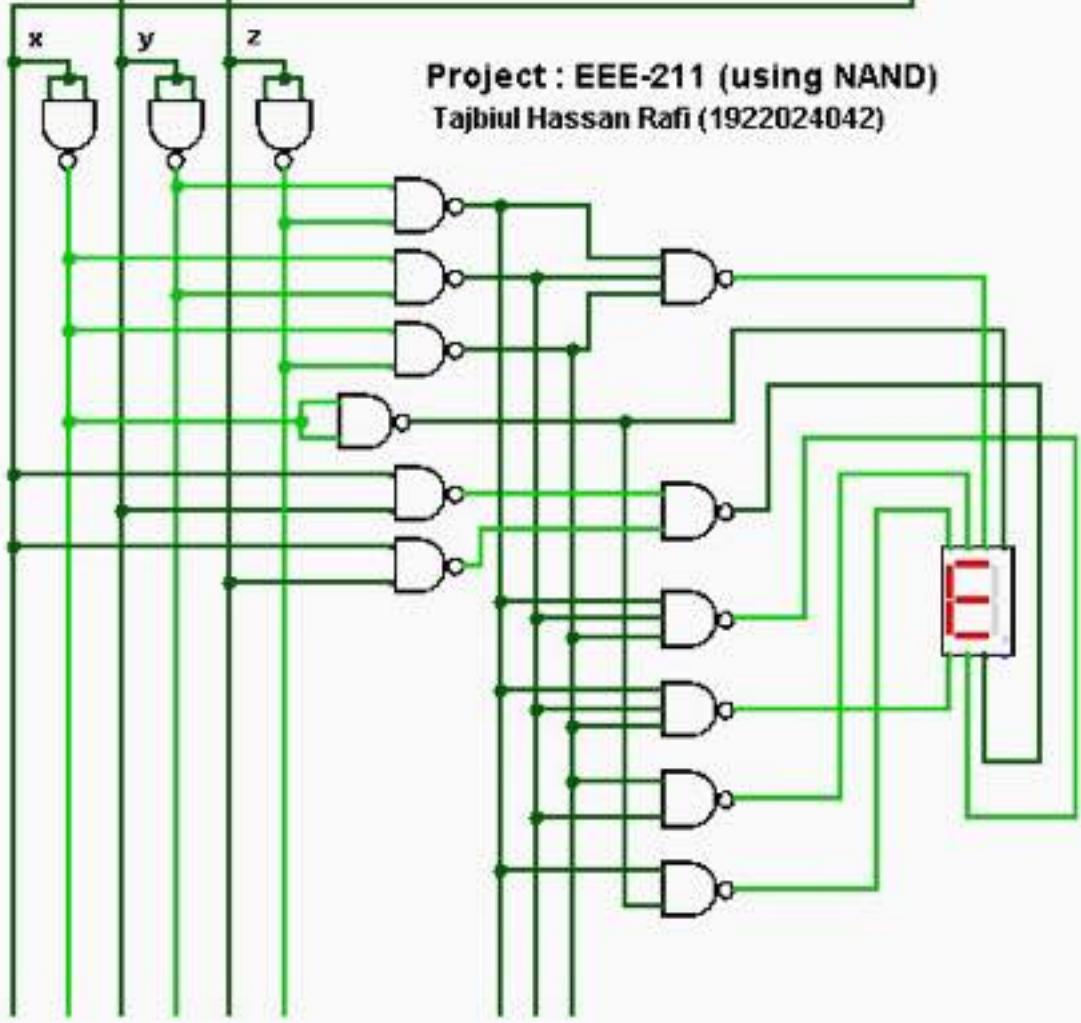


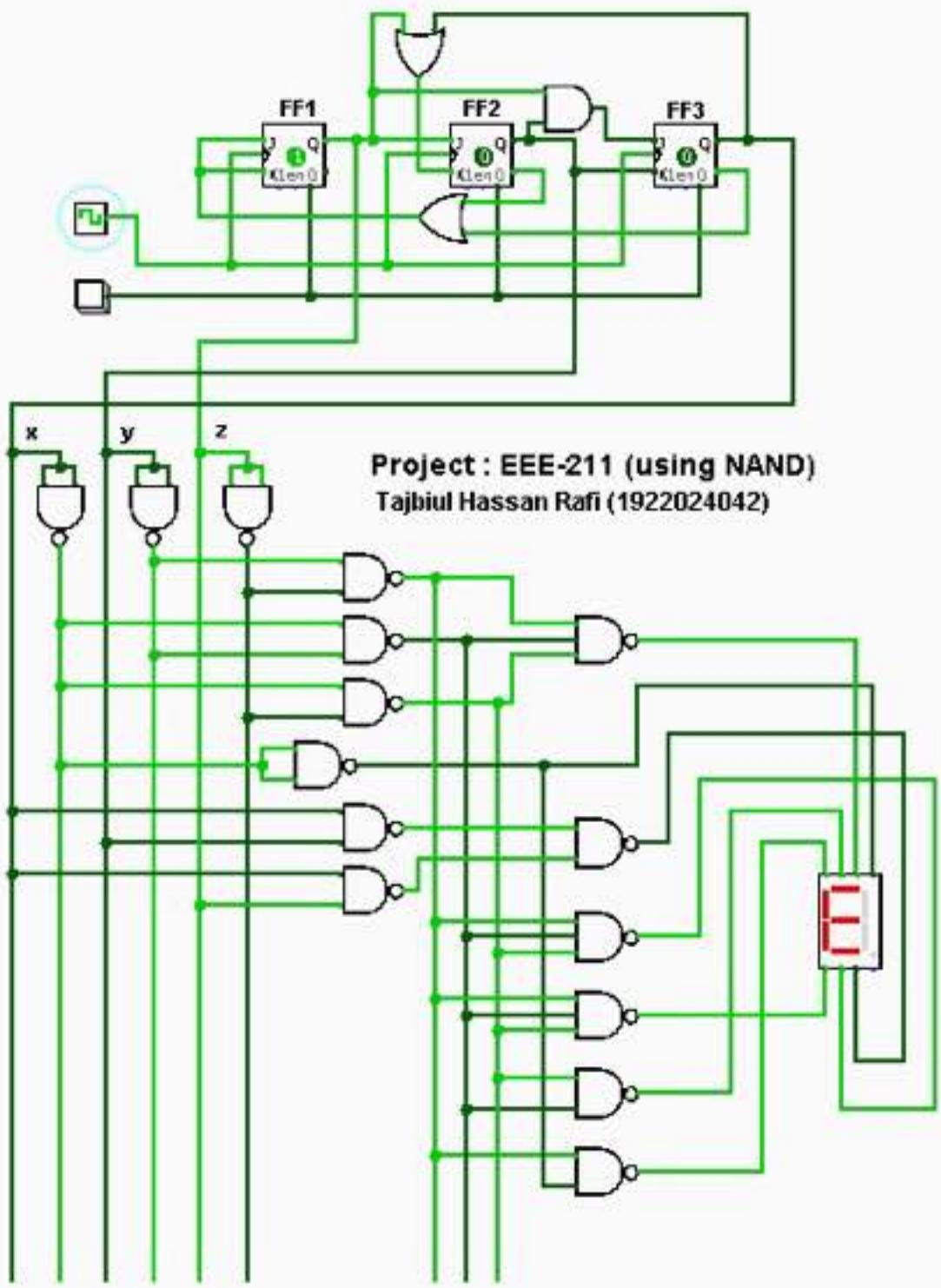


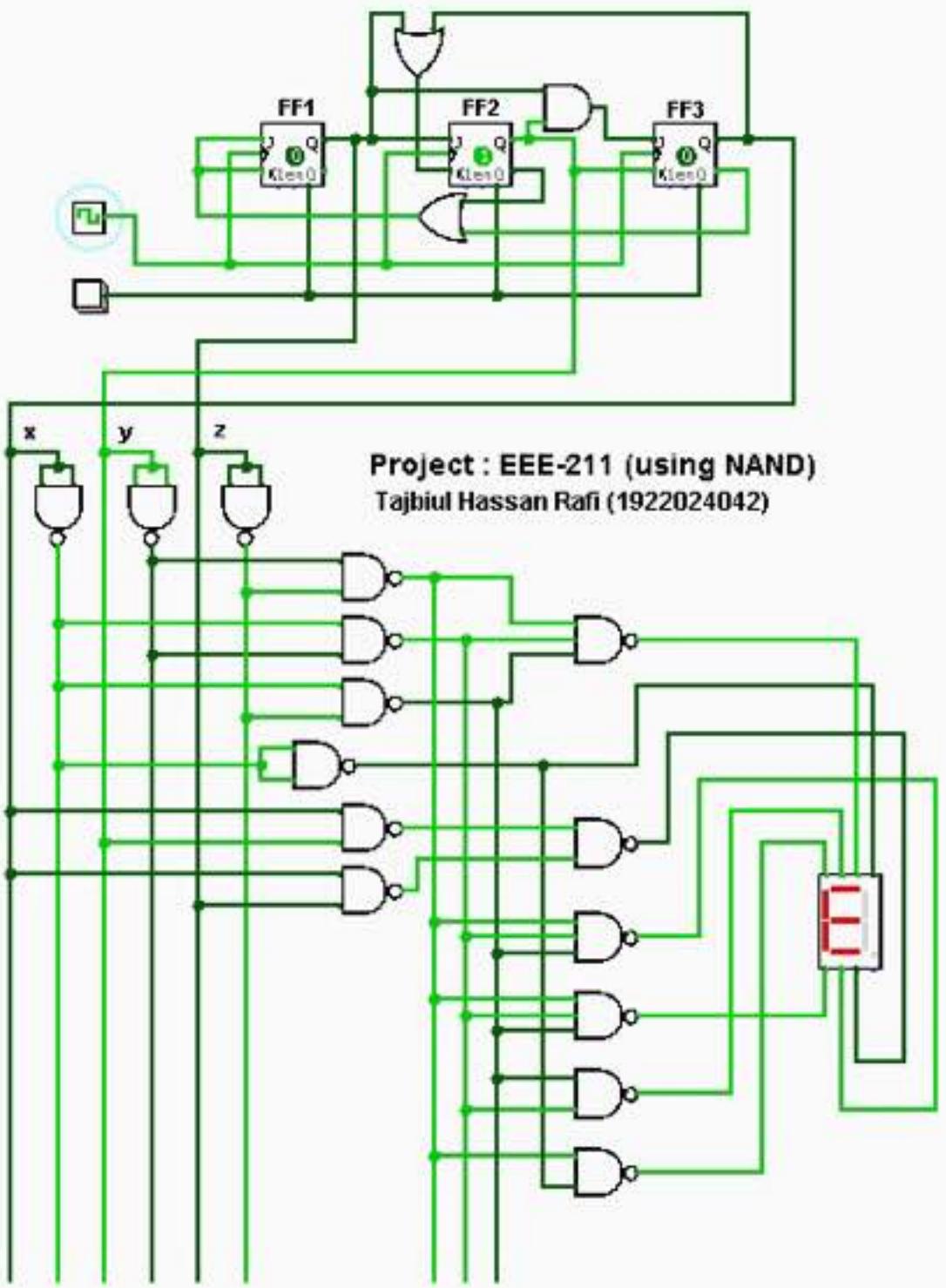
Sequential circuit using NAND

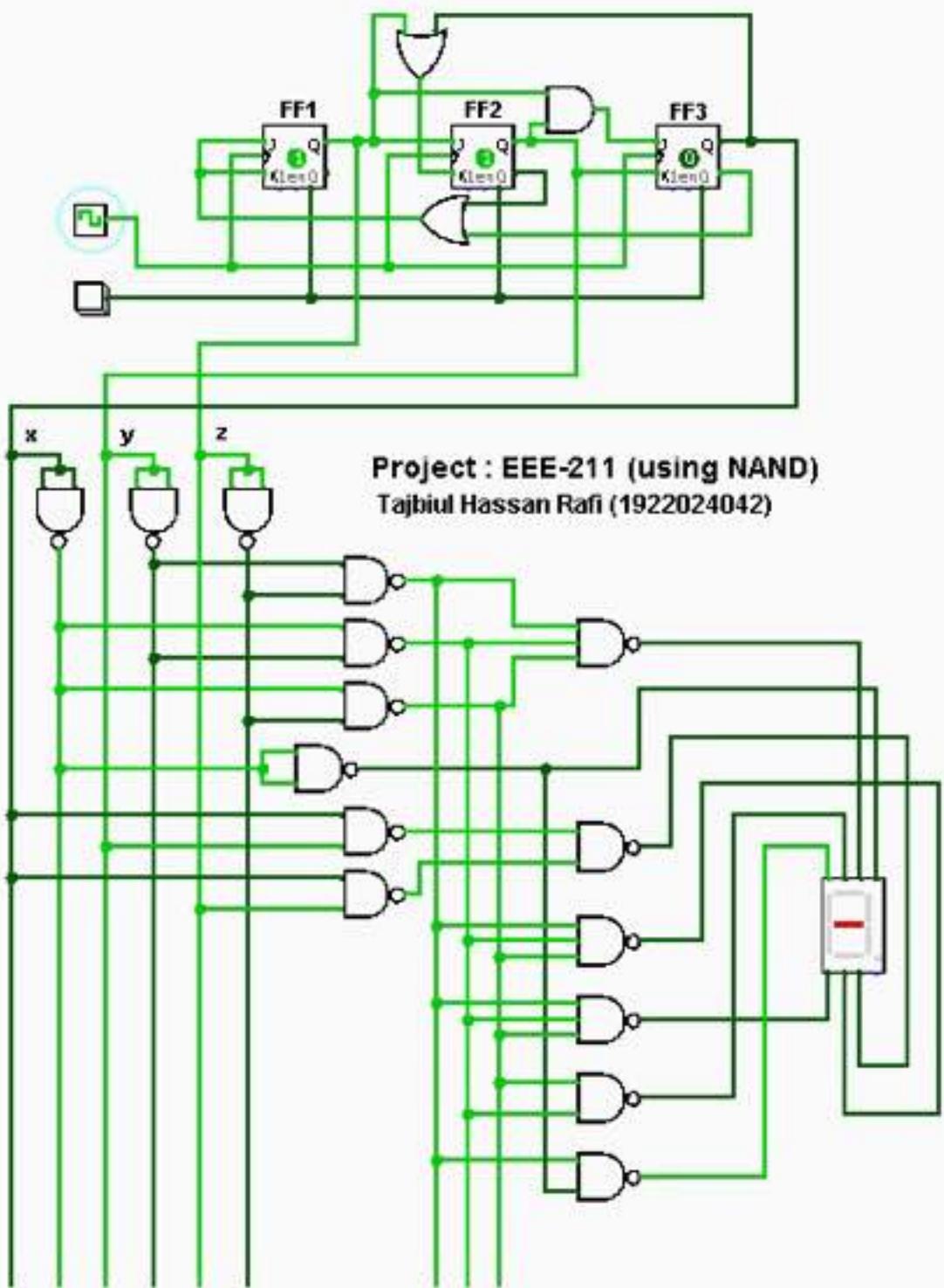


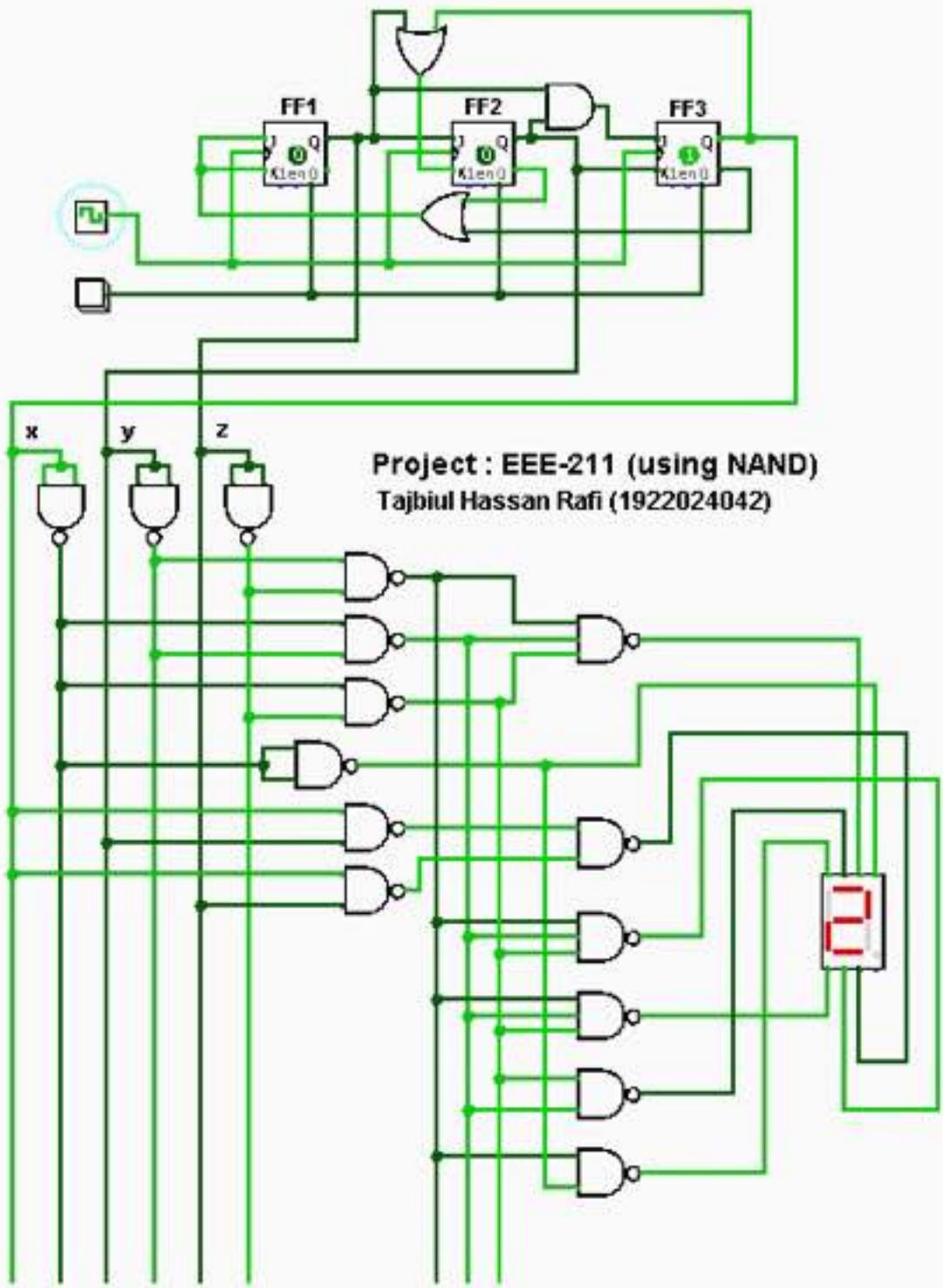
Project : EEE-211 (using NAND)
Tajbiul Hassan Rafi (1922024042)

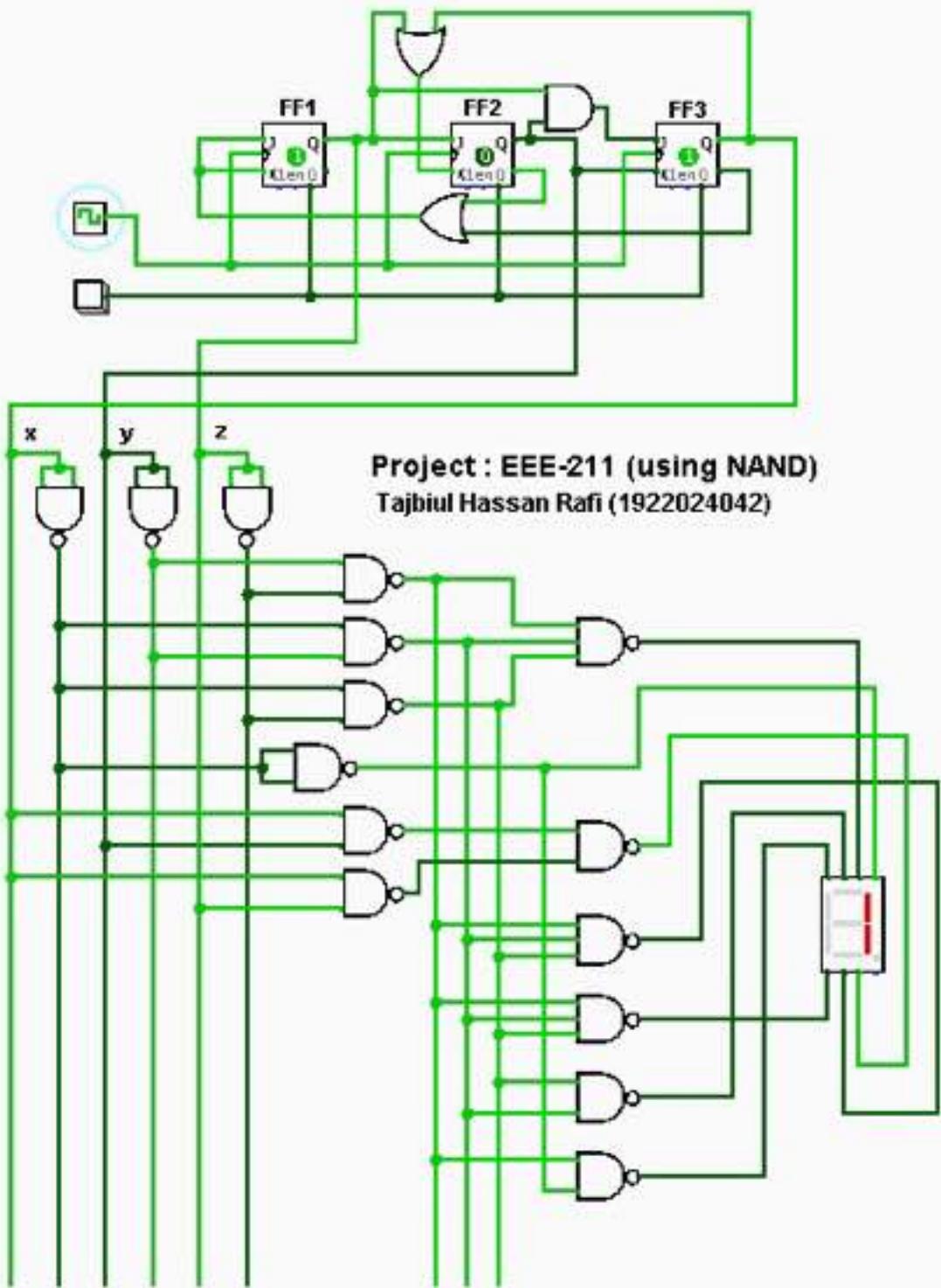




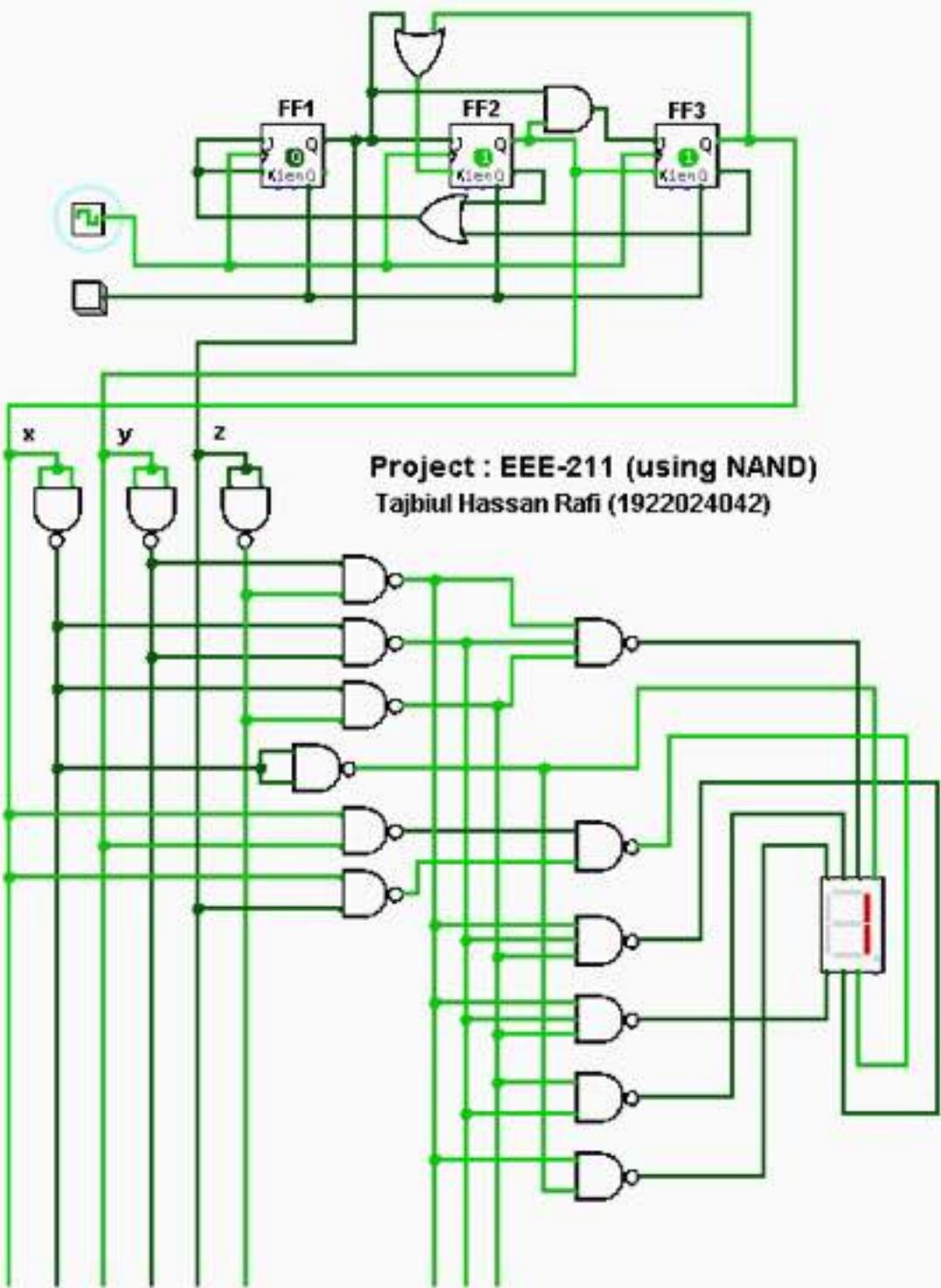








Project : EEE-211 (using NAND)
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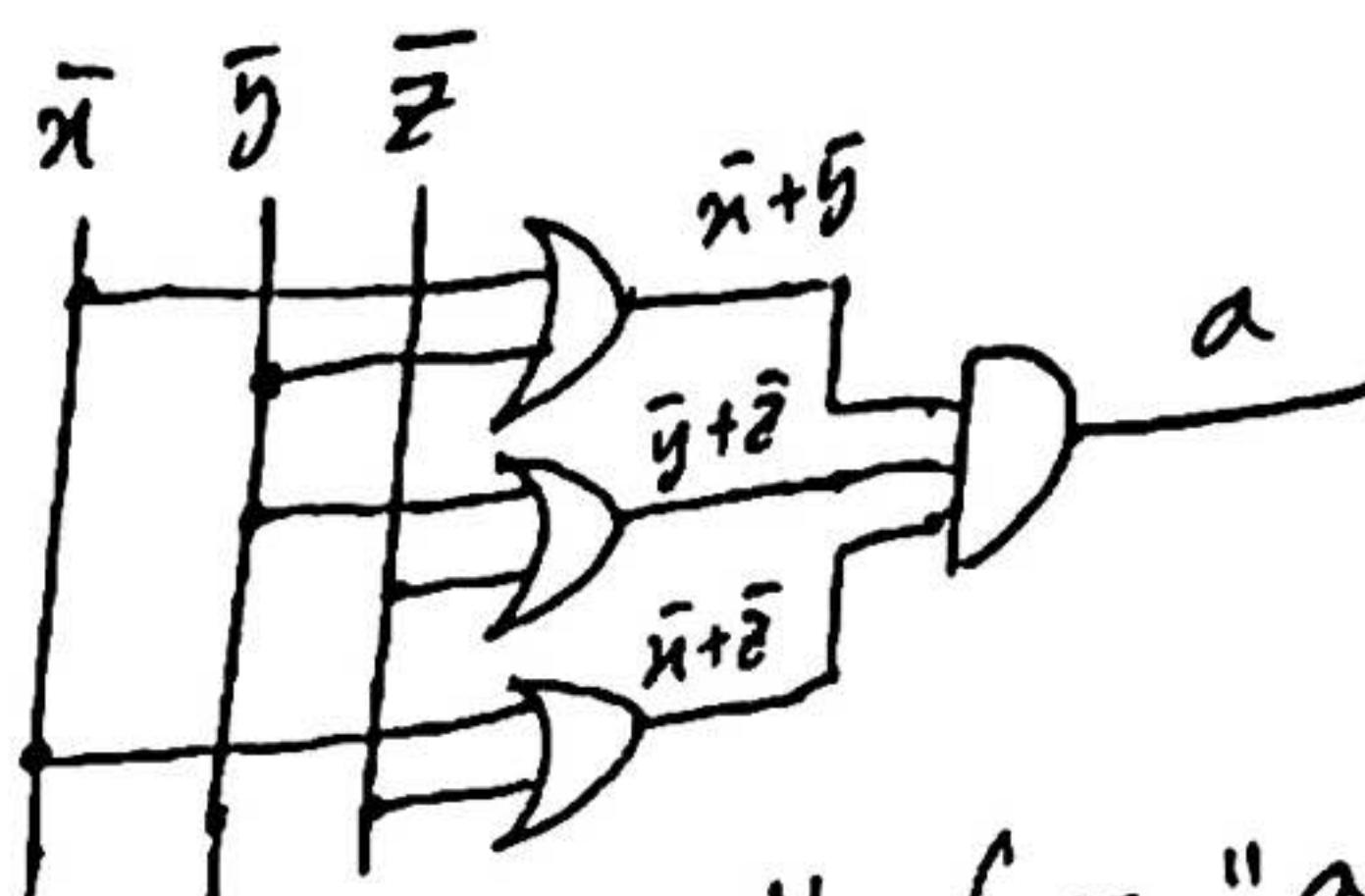
Combinational circuit using POS

For POS Expression (MD.Zihad Hossain)

$$a = (\bar{x} + y + z)(x + \bar{y} + z)(\bar{x} + y + \bar{z})$$

K-map

	$\bar{y}\bar{z}$	00	01	11	10
x	1	1	0	1	
y	1	0	x	0	
z					



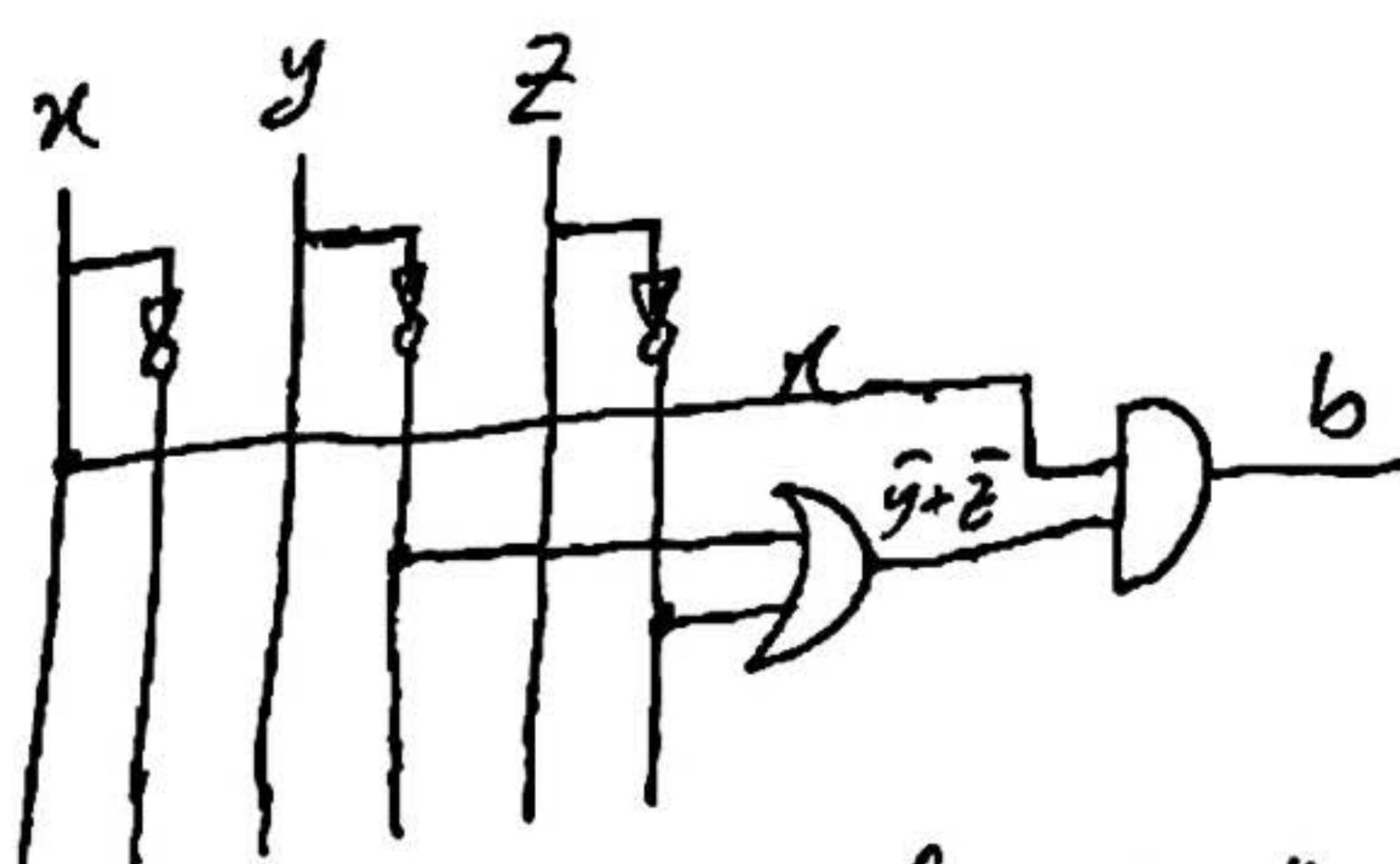
Circuit for "a"

$$\text{So, } a = (\bar{x} + \bar{y})(\bar{y} + \bar{z})(\bar{z} + x)$$

b = $(\bar{x} + \bar{y} + \bar{z})(\bar{x} + \bar{y} + z)(\bar{x} + y + \bar{z})(\bar{x} + y + z)$

K-map

	$\bar{y}\bar{z}$	00	01	11	10
x	0	0	0	0	
y	1	1	1	x	1
z					

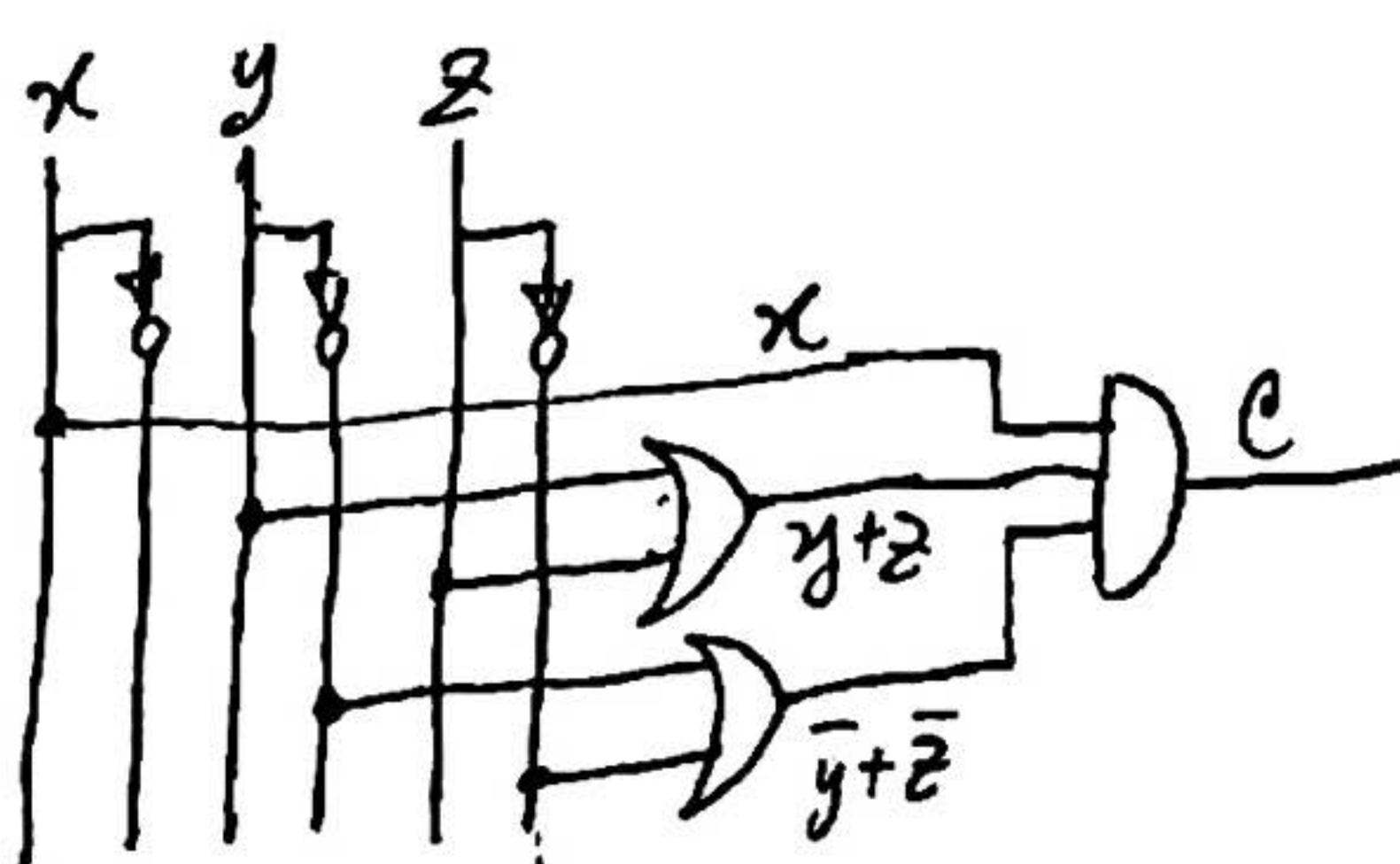


Circuit for "b"

c = $(\bar{x} + \bar{y} + \bar{z})(\bar{x} + \bar{y} + z)(\bar{x} + y + \bar{z})(\bar{x} + y + z)$

K-map

	$\bar{y}\bar{z}$	00	01	11	10
x	0	0	0	0	
y	0	1	x	1	
z					



$$\text{So, } c = x(y + z)(\bar{y} + \bar{z})$$

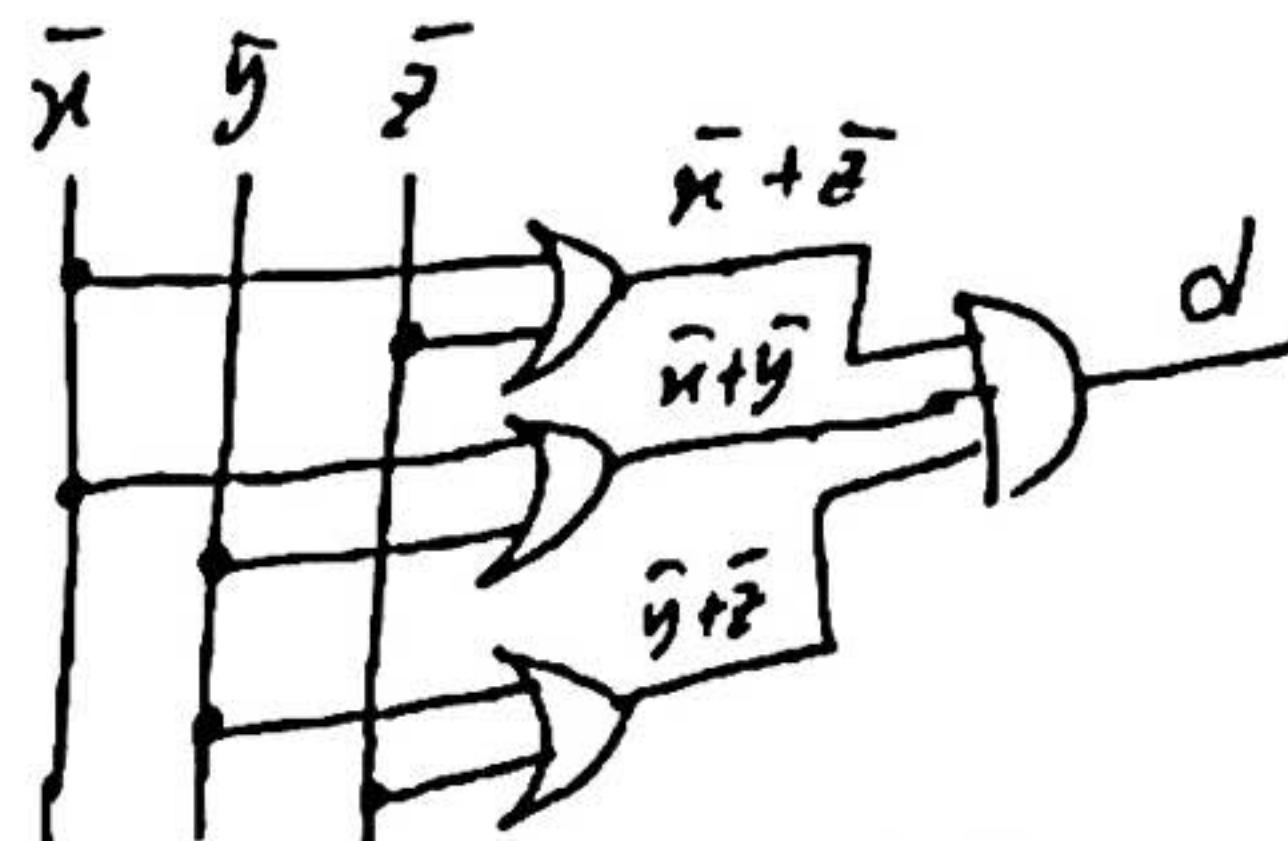
Circuit for "c"

$d = (\bar{x} + y + z)(x + \bar{y} + z)(x + y + \bar{z})$

K-map

$x \backslash yz$	00	01	11	10
0	1	1	0	1
1	1	0	X	0

so, $d = (\bar{x} + \bar{z})(\bar{x} + \bar{y})(\bar{y} + \bar{z})$



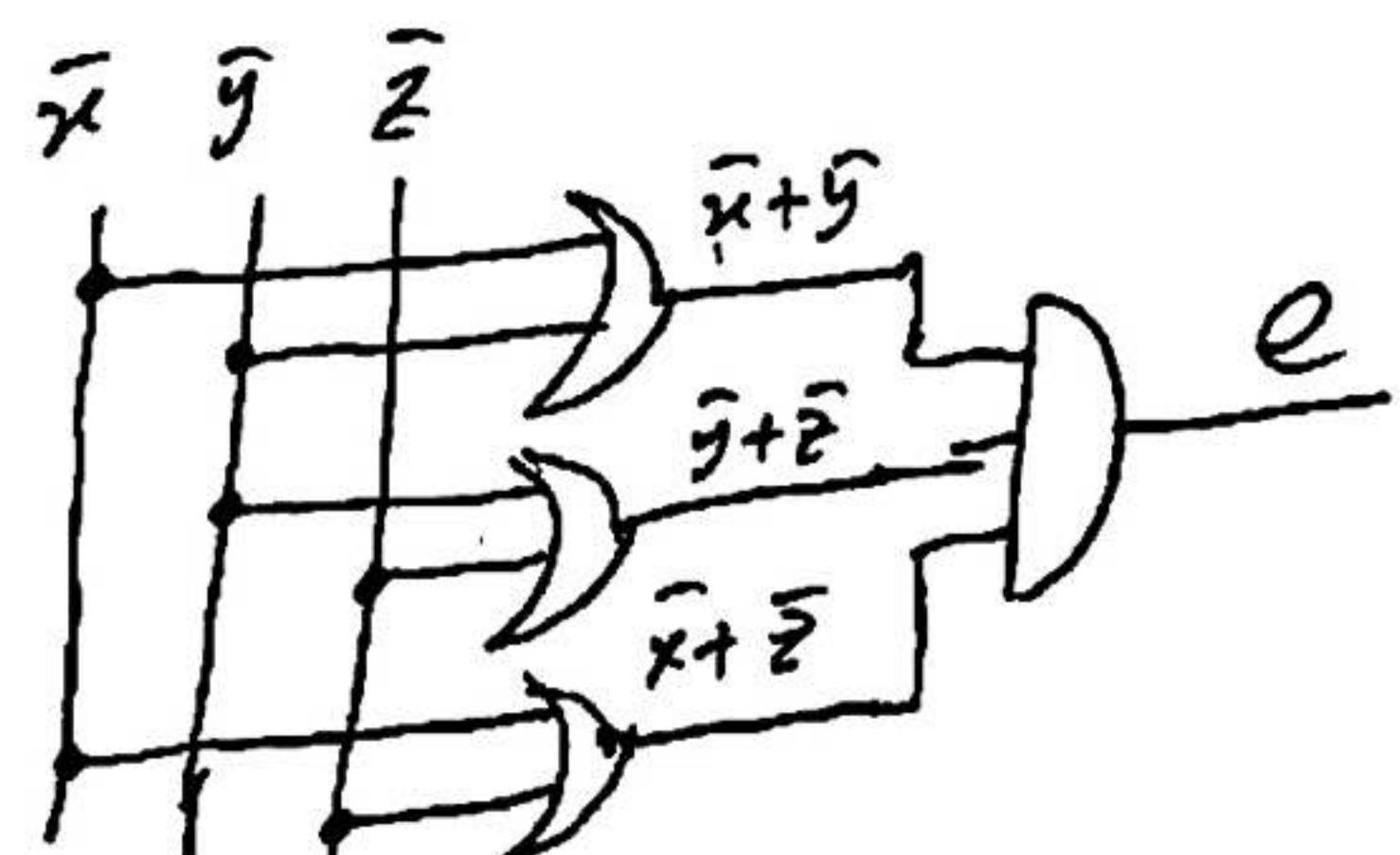
Circuit for "d"

$e = (\bar{x} + y + z)(x + \bar{y} + z)(x + y + \bar{z})$

K-map

$x \backslash yz$	00	01	11	10
0	1	1	0	1
1	1	0	X	0

so, $e = (\bar{x} + \bar{y})(\bar{y} + \bar{z})(\bar{x} + \bar{z})$



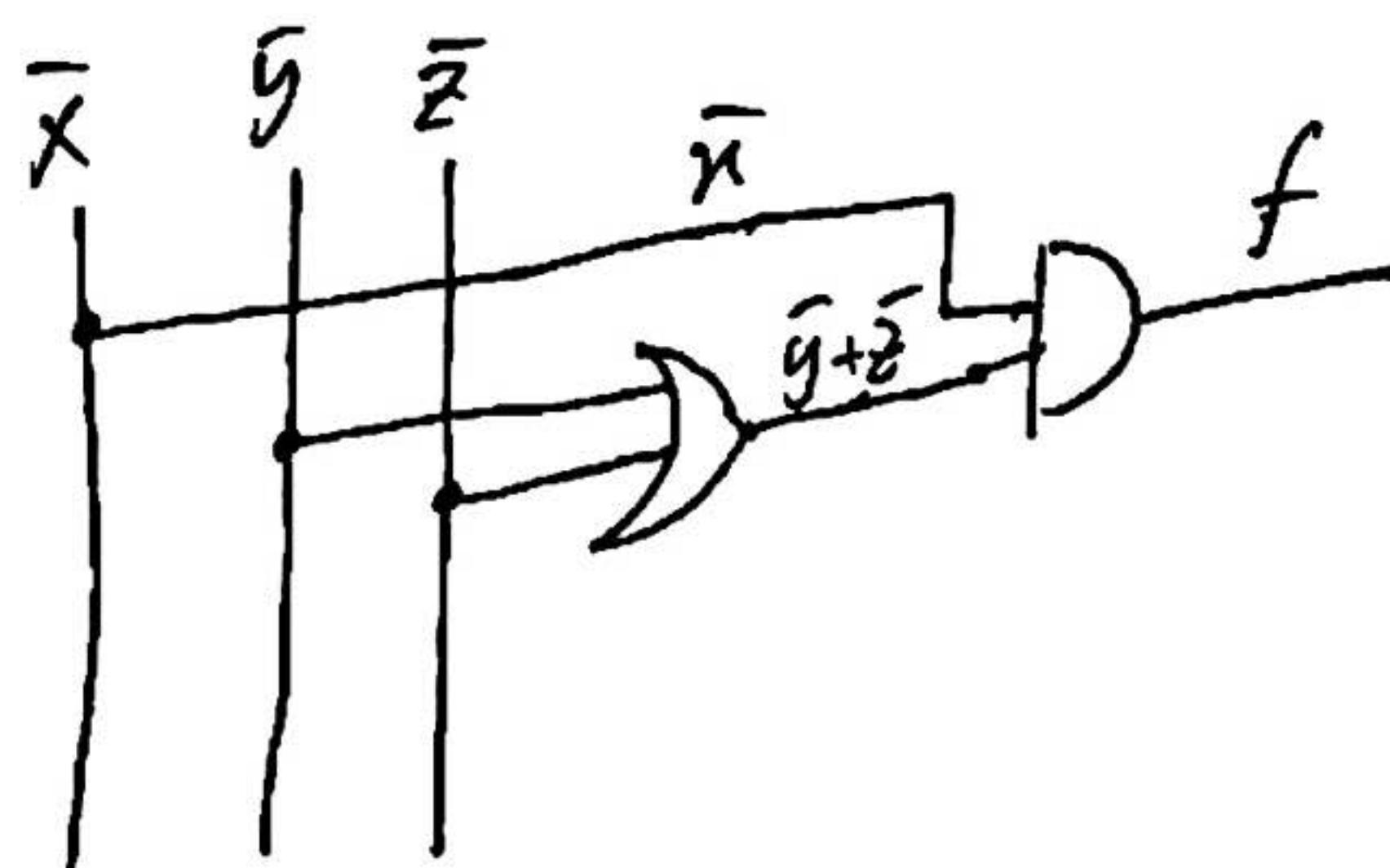
circuit for "e"

$f = (\bar{x} + y + z)(x + \bar{y} + \bar{z})(x + \bar{y} + z)(x + y + \bar{z})$

K-map

$x \backslash yz$	00	01	11	10
0	1	1	0	1
1	0	0	X	0

$f = \bar{x}(\bar{y} + \bar{z})$

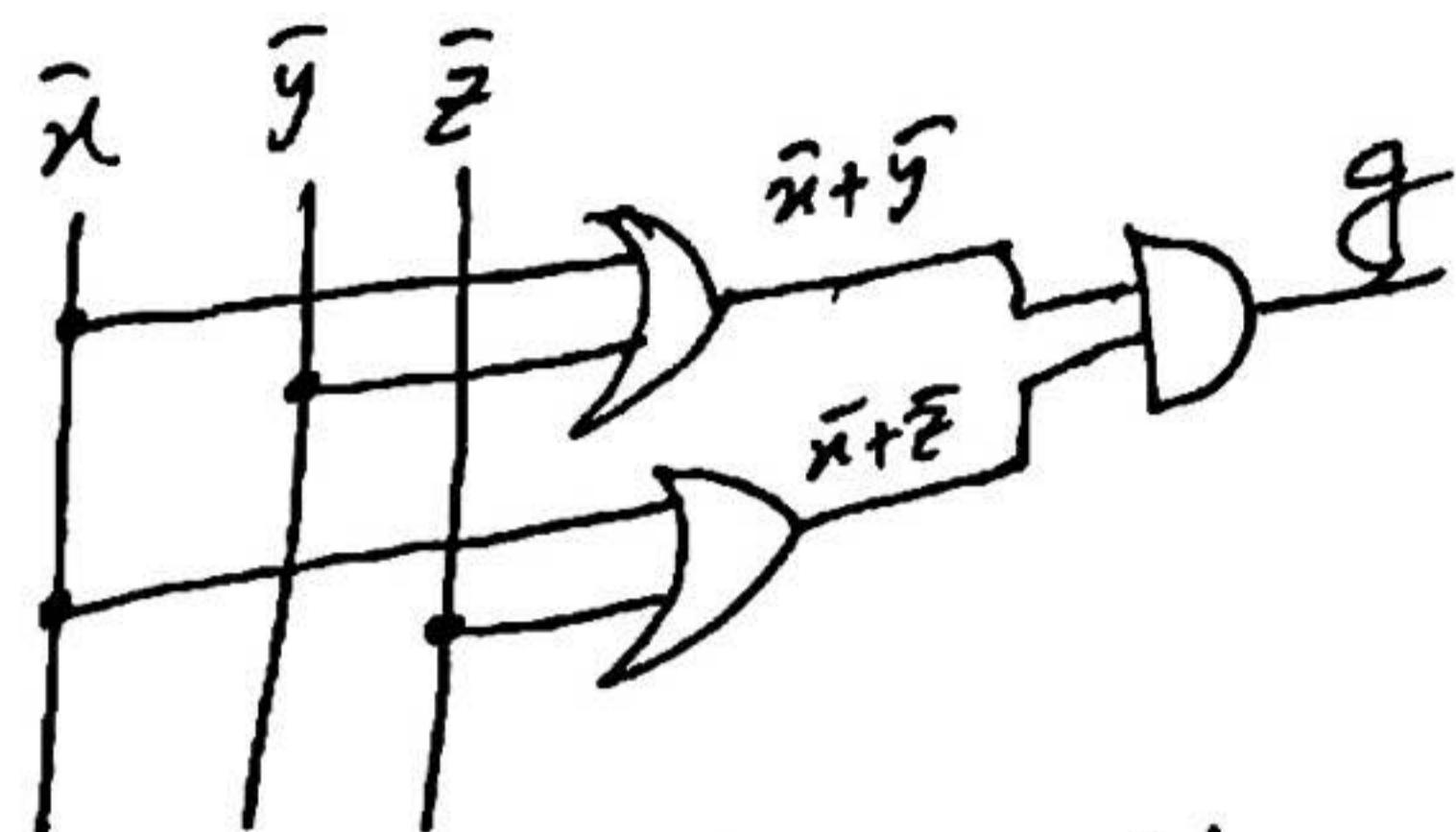


$$\text{Q1} \quad g = (x + \bar{y} + z)(x + y + \bar{z})$$

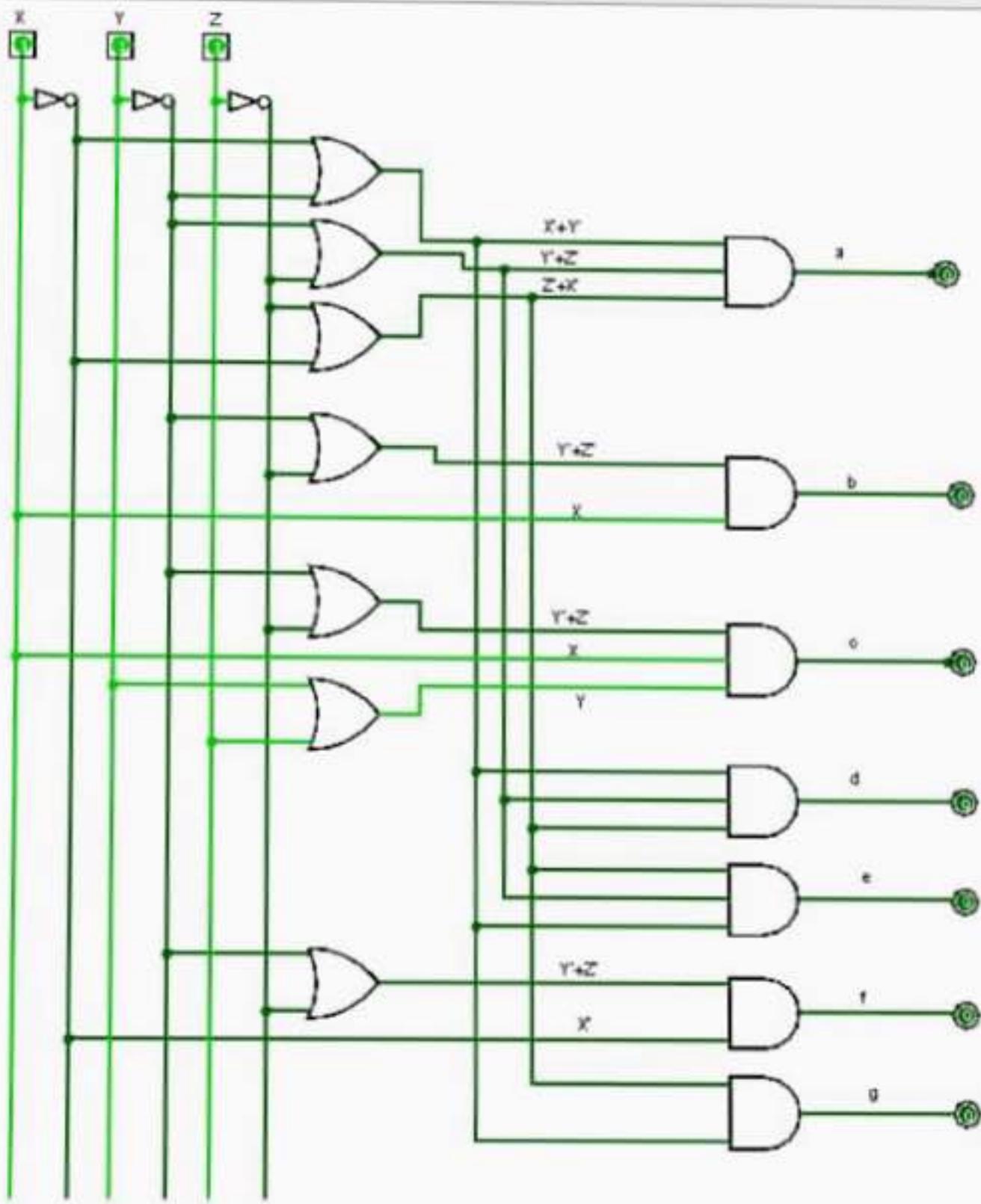
K-map

$x \backslash yz$	00	01	11	10
0	1	1	1	1
1	1	0	(X)	0

$$\text{so, } g = (\bar{x} + \bar{z})(\bar{x} + \bar{y})$$

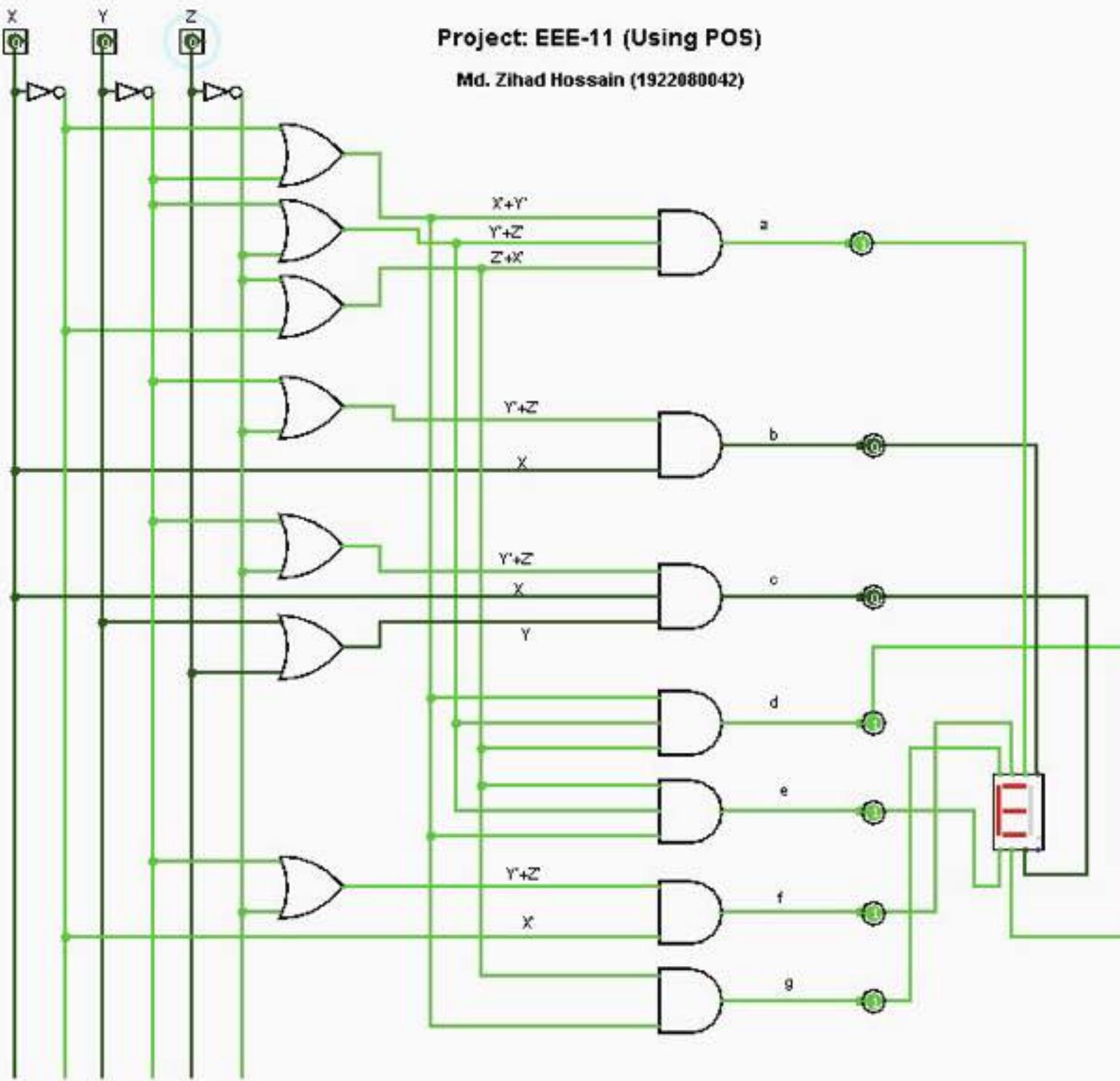


Circuit for "g"



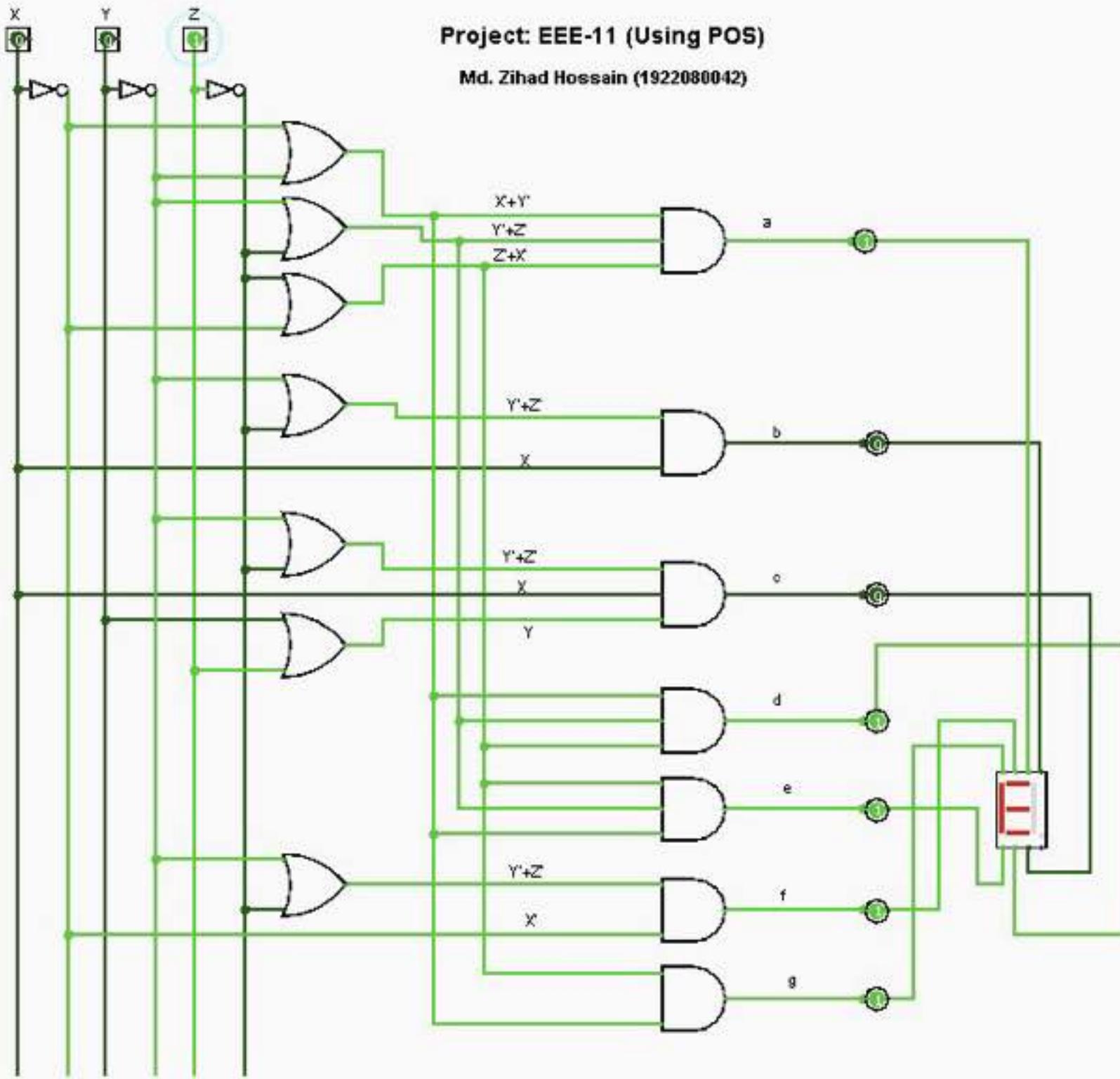
Project: EEE-11 (Using POS)

Md. Zihad Hossain (1922080042)



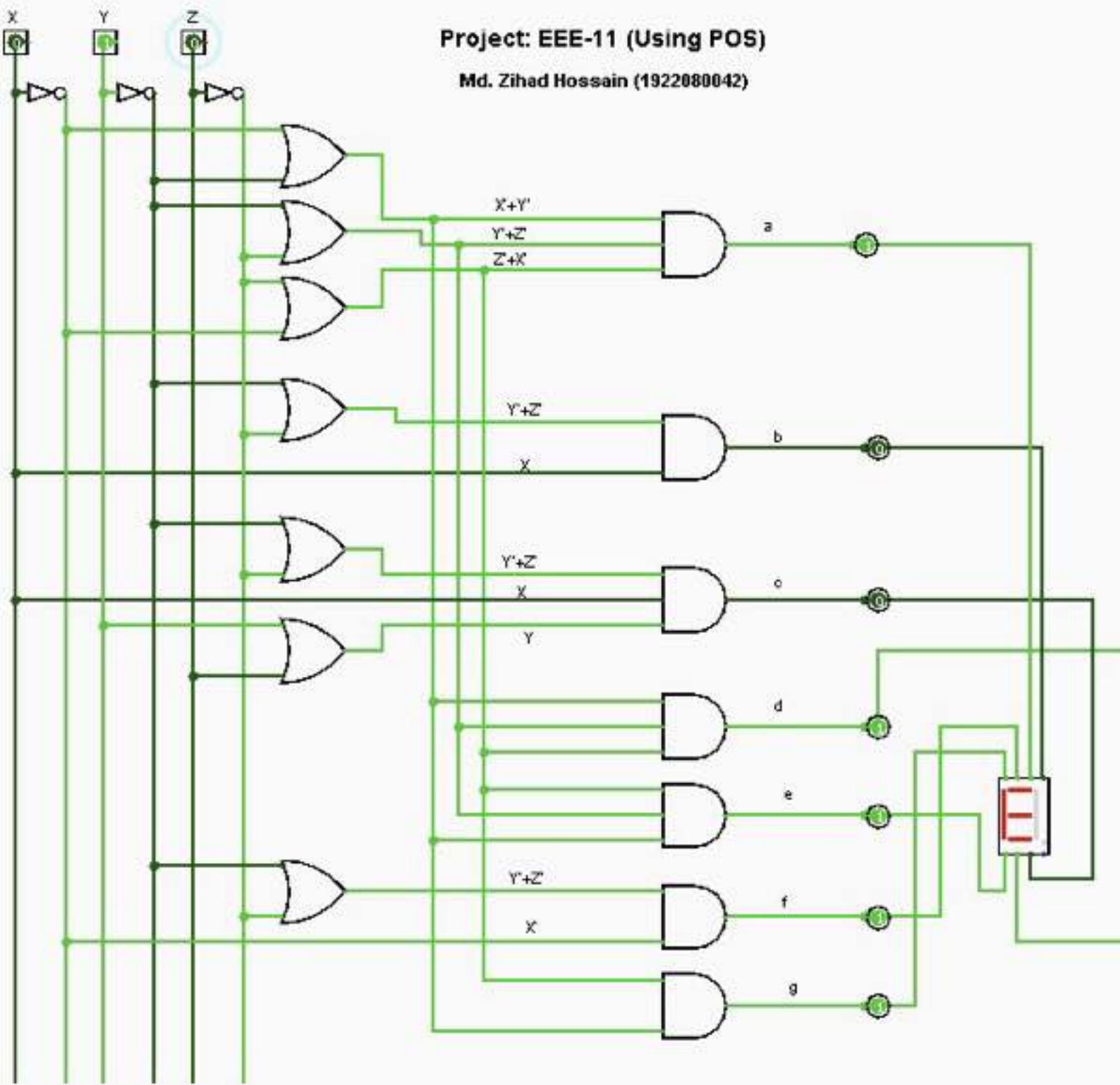
Project: EEE-11 (Using POS)

Md. Zihad Hossain (1922080042)



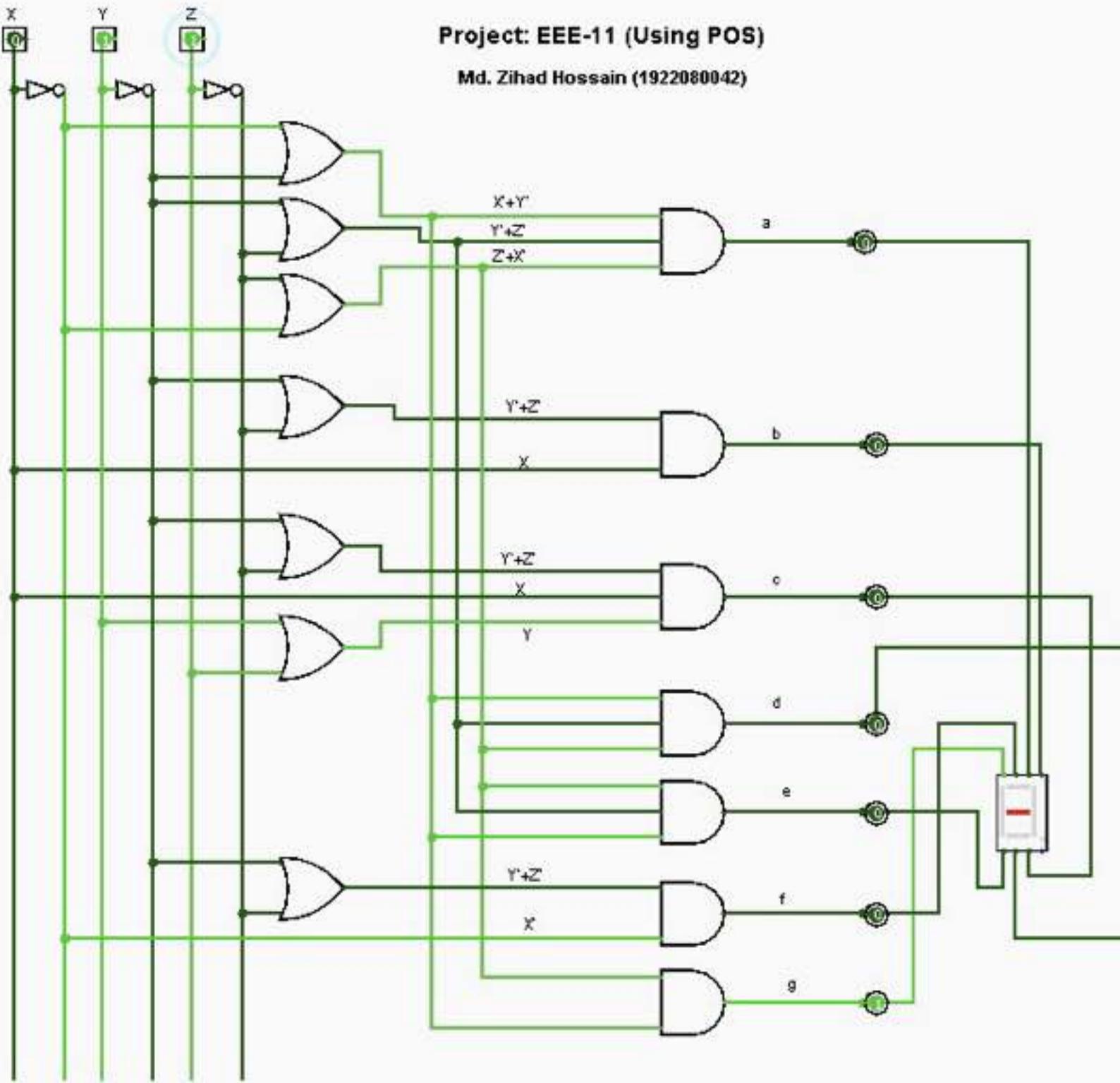
Project: EEE-11 (Using POS)

Md. Zihad Hossain (1922080042)



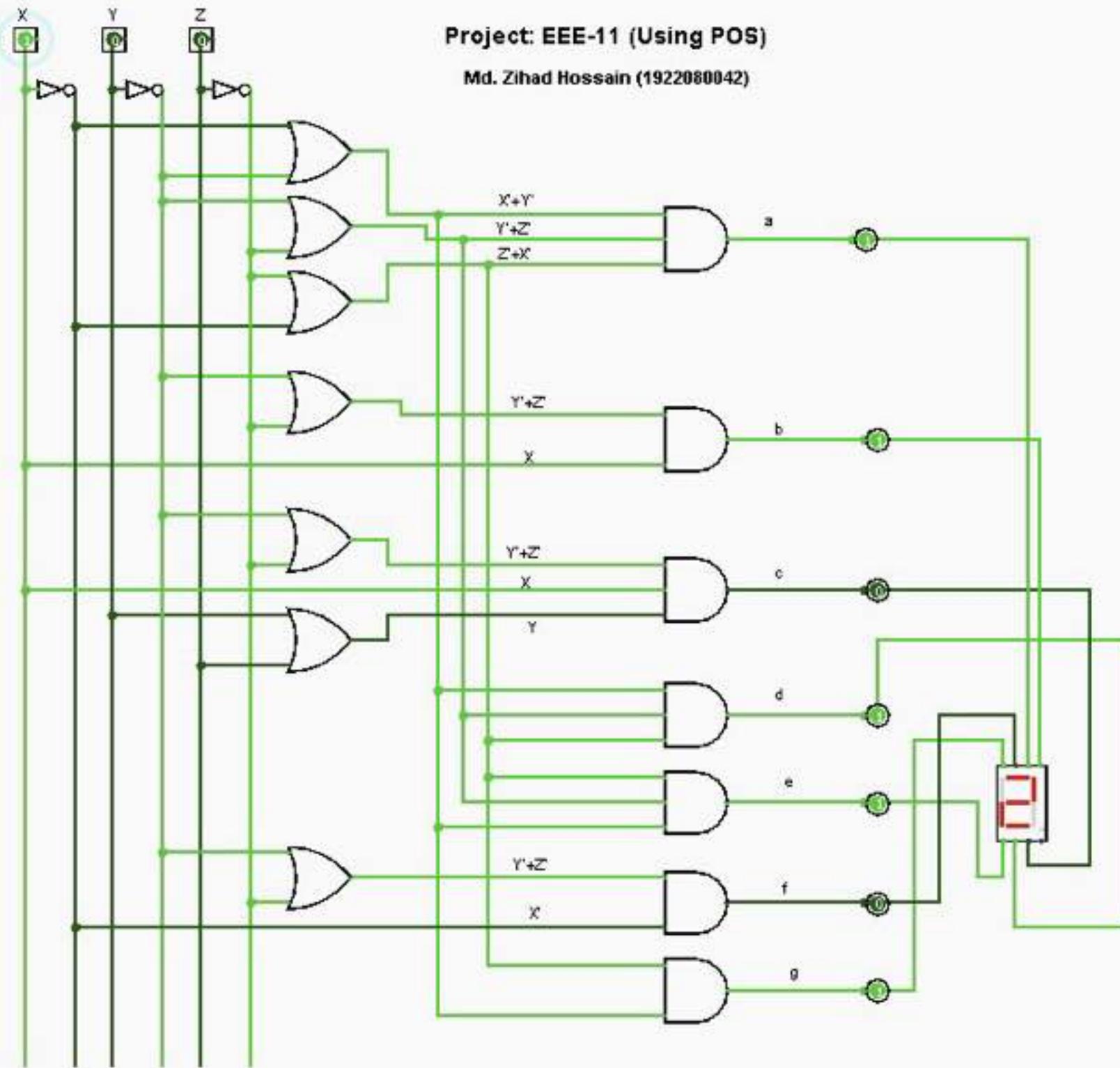
Project: EEE-11 (Using POS)

Md. Zihad Hossain (1922080042)



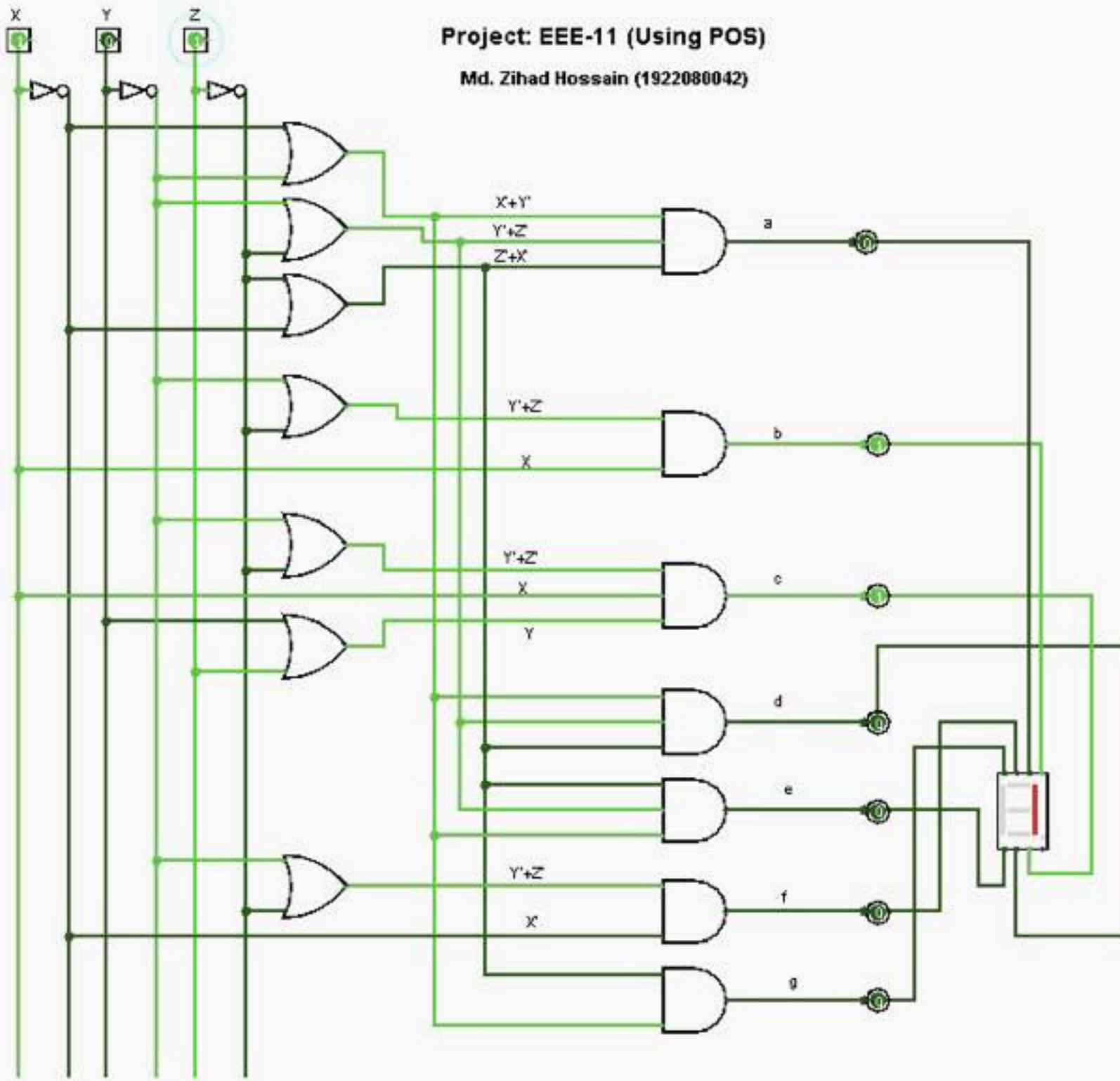
Project: EEE-11 (Using POS)

Md. Zihad Hossain (1922080042)



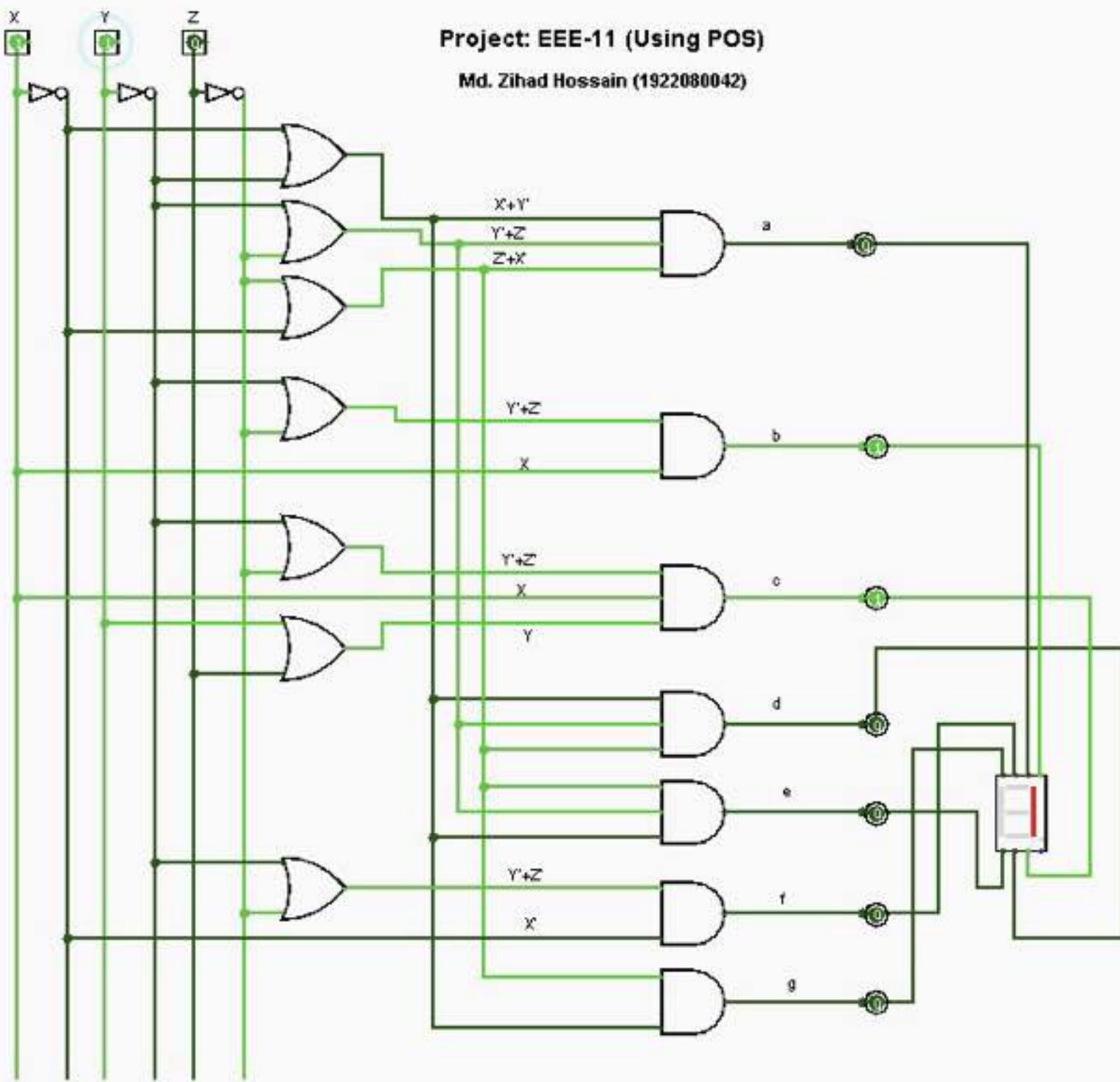
Project: EEE-11 (Using POS)

Md. Zihad Hossain (1922080042)

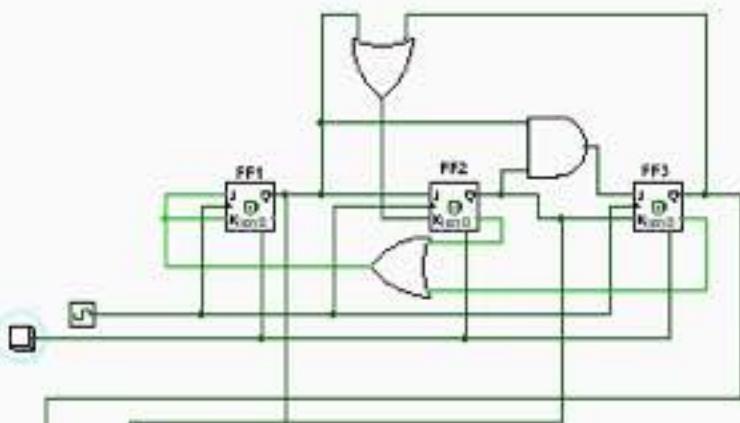


Project: EEE-11 (Using POS)

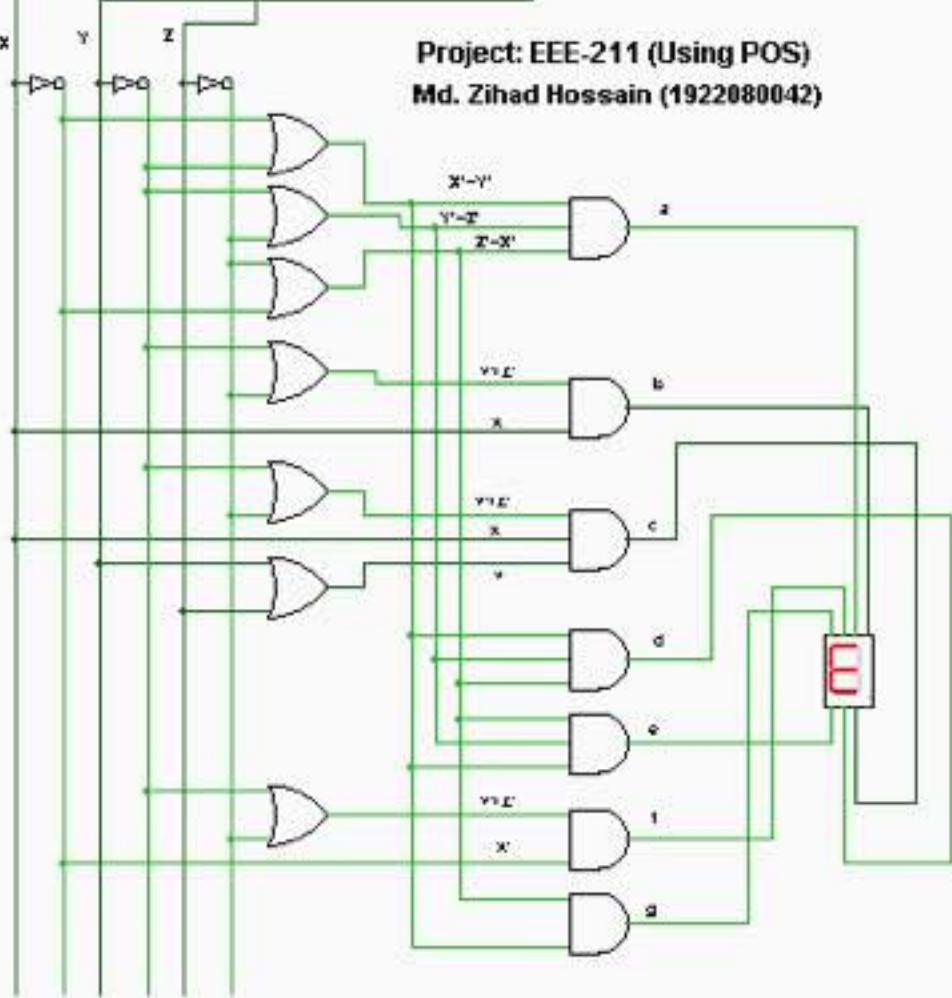
Md. Zihad Hossain (1922080042)

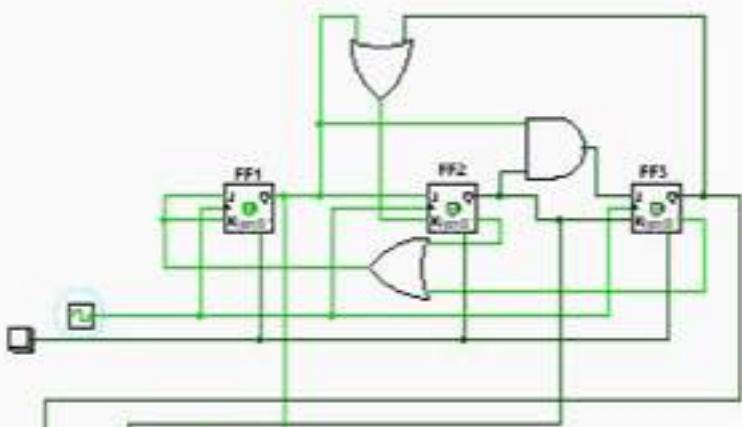


Sequential circuit using | POS



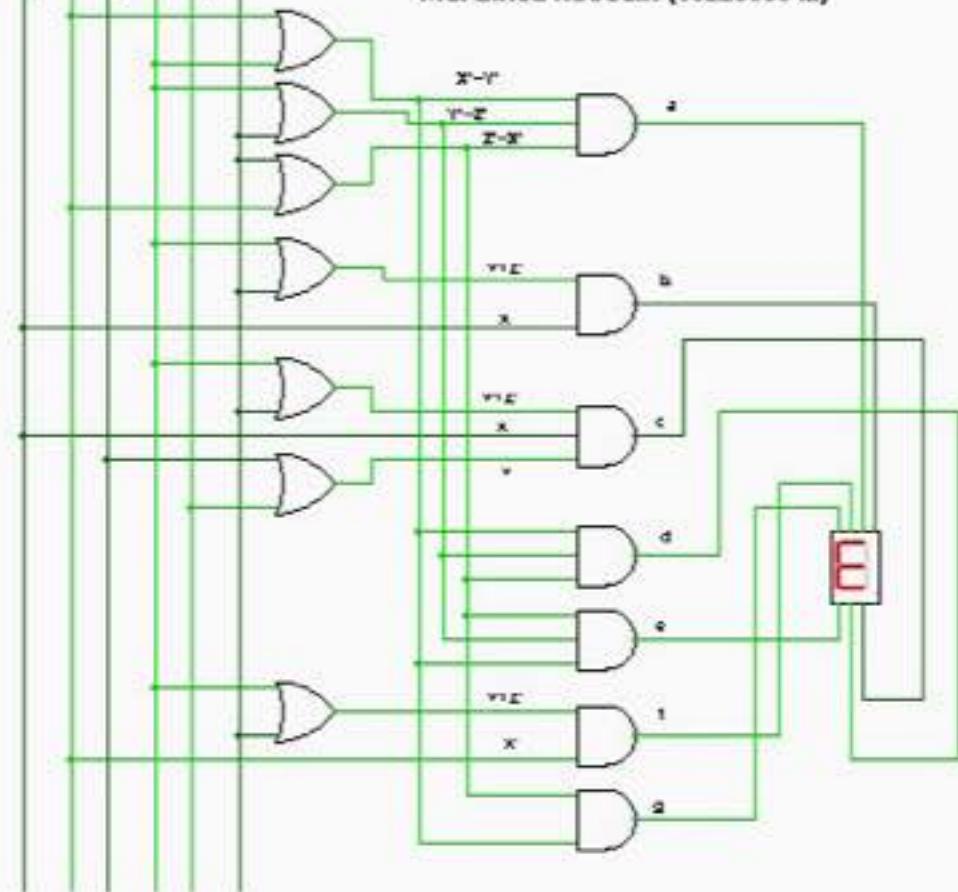
Project: EEE-211 (Using POS)
Md. Zihad Hossain (1922080042)

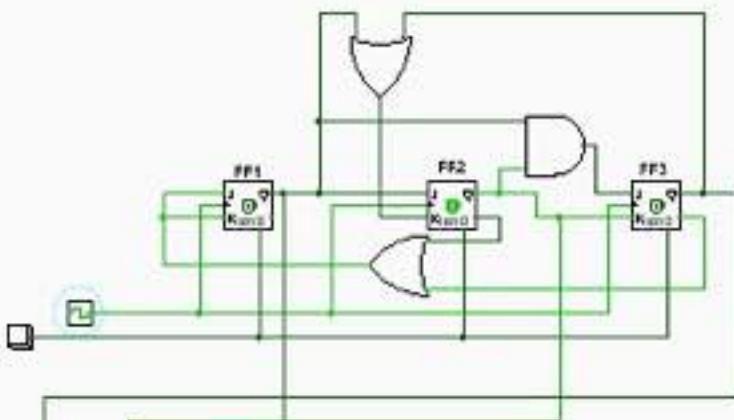




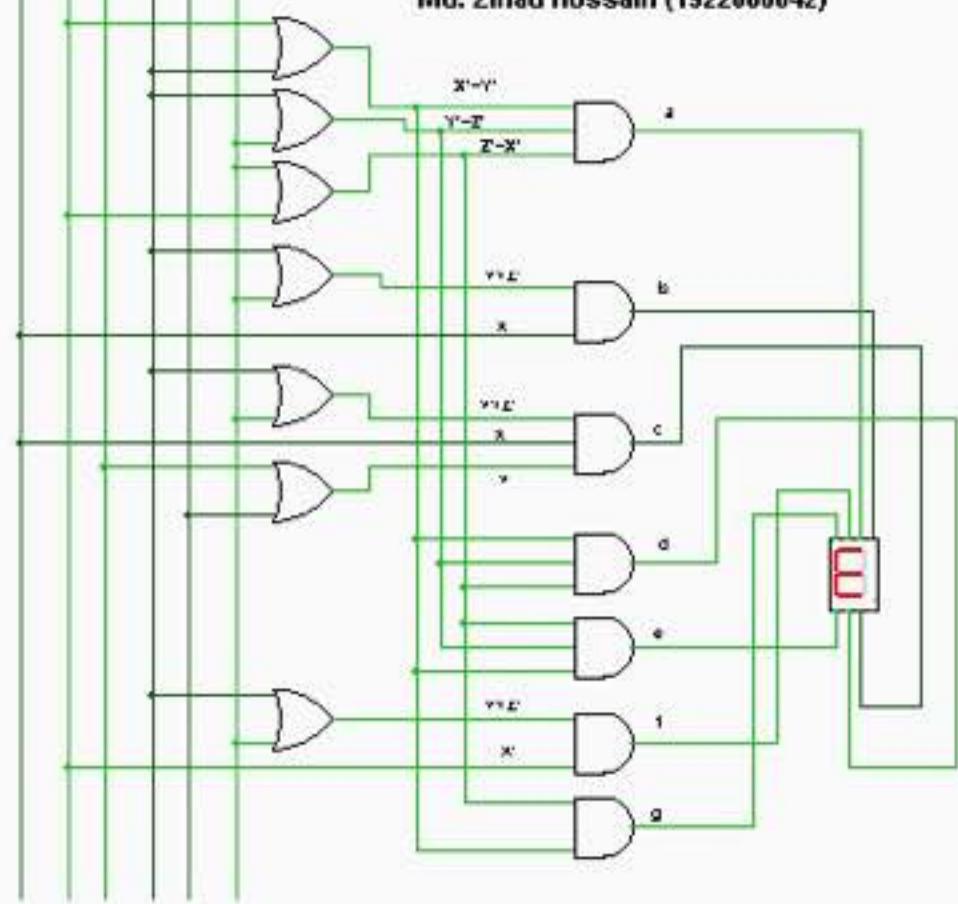
Project: EEE-211 (Using POS)

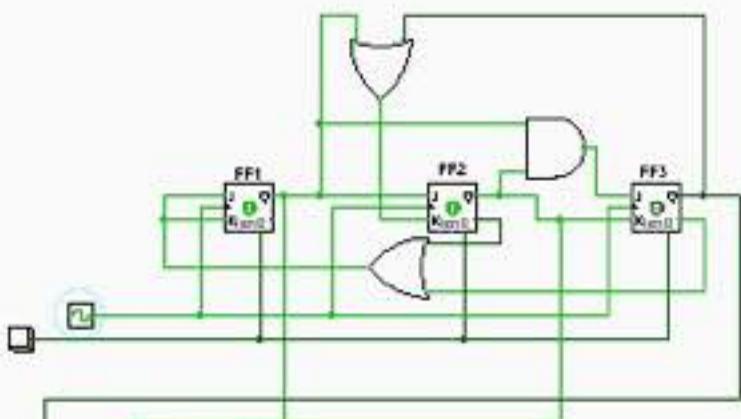
Md. Zihad Hossain (1922080042)



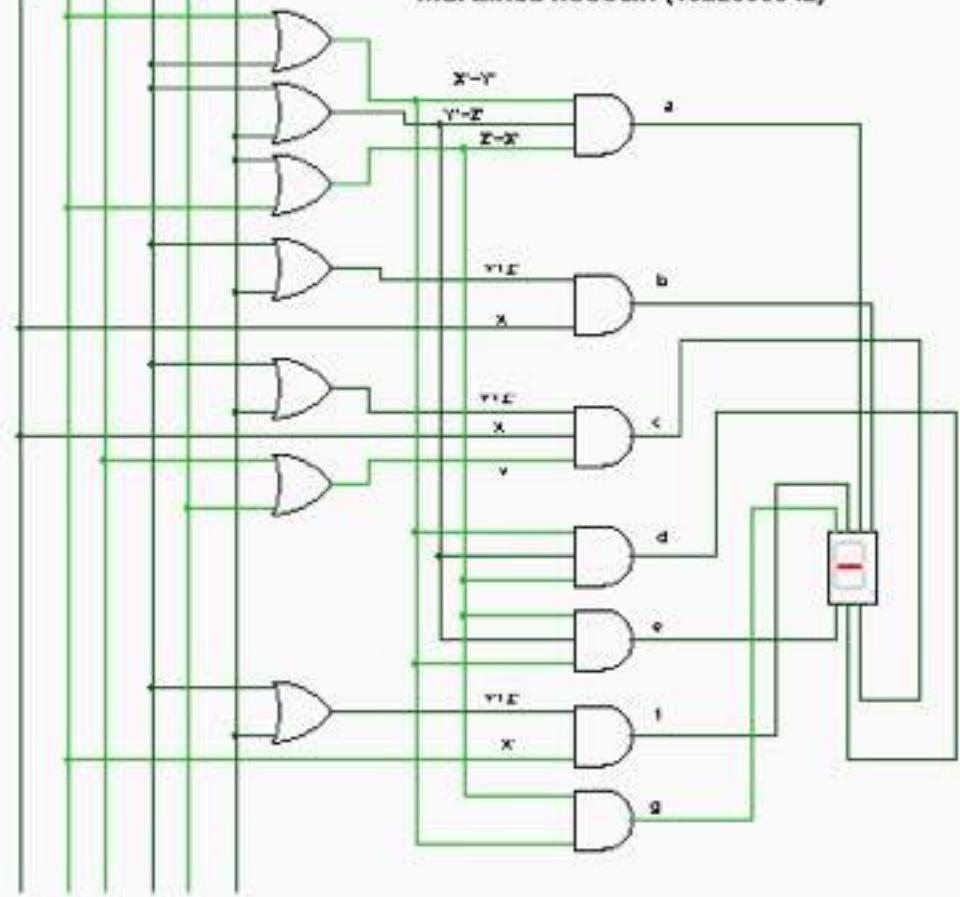


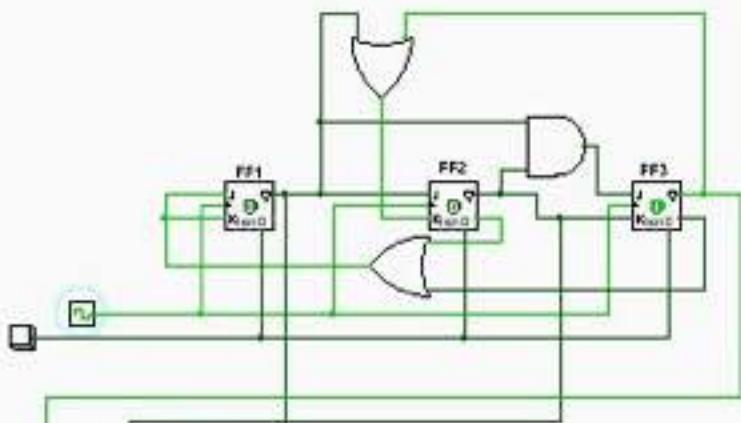
Project: EEE-211 (Using POS)
Md. Zihad Hossain (1922080042)



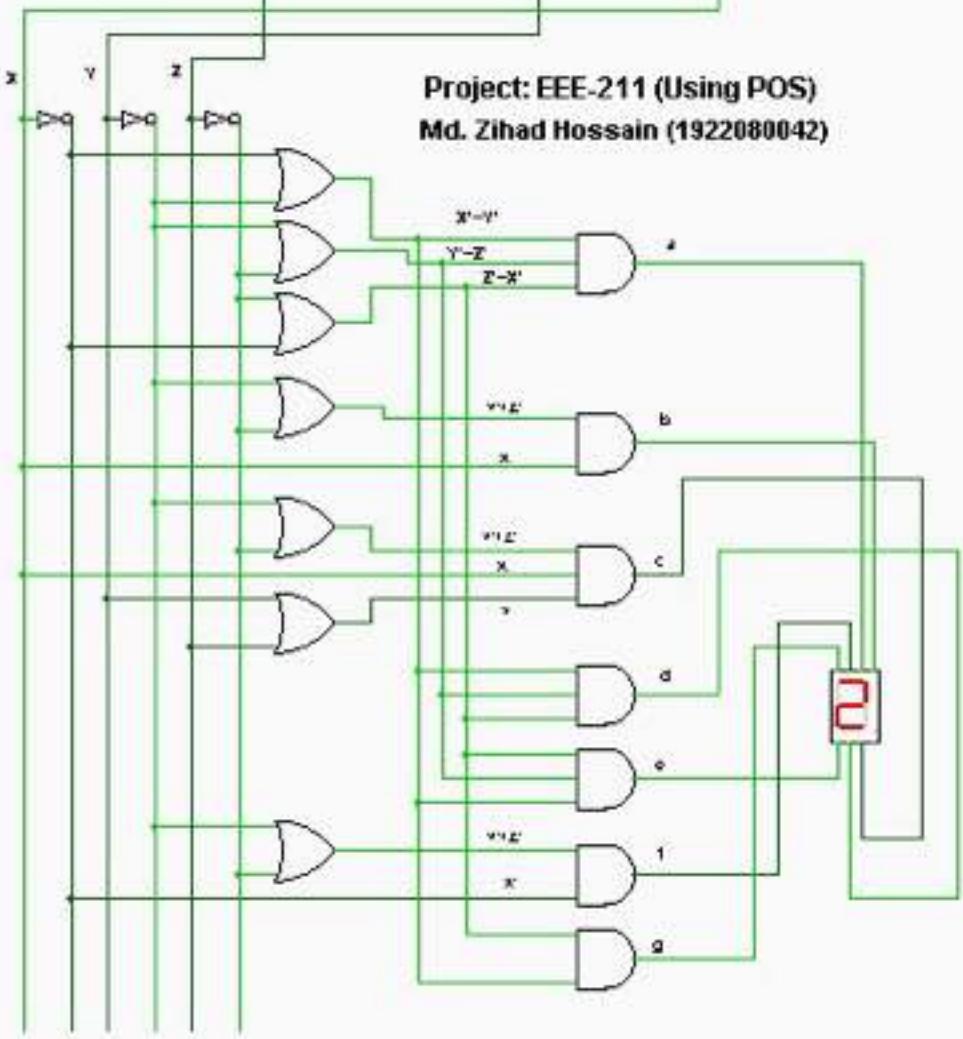


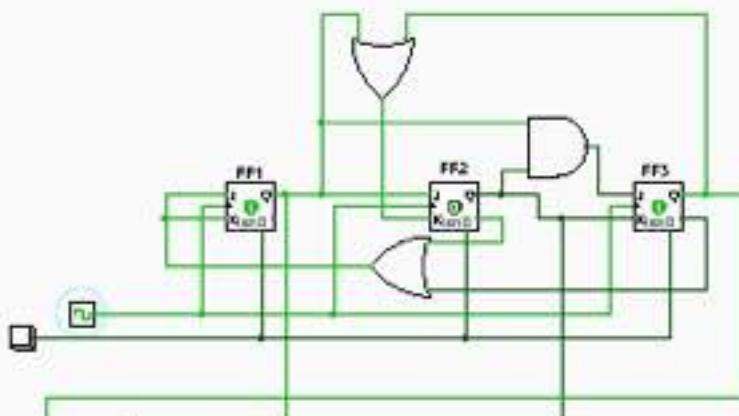
Project: EEE-211 (Using POS)
Md. Zihad Hossain (1922080042)



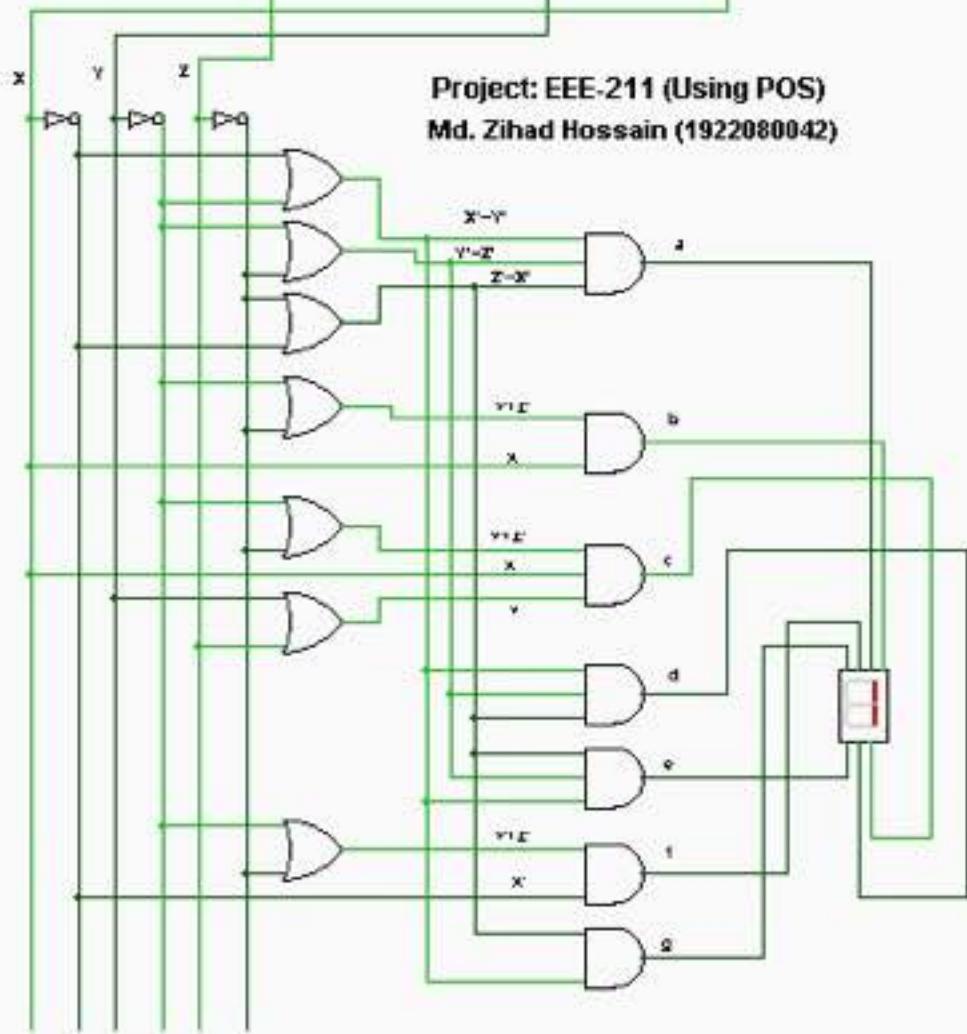


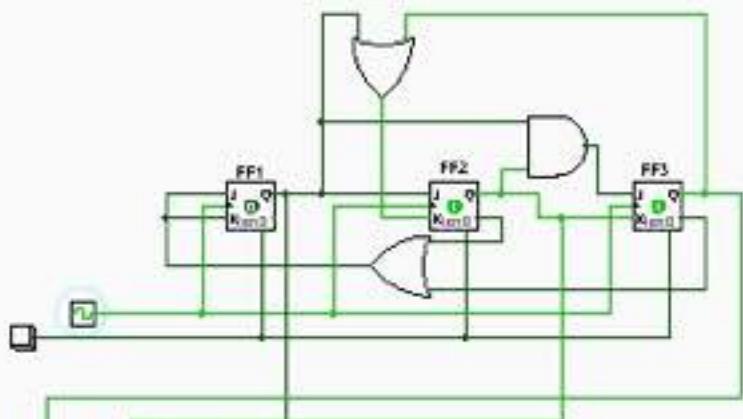
Project: EEE-211 (Using POS)
Md. Zihad Hossain (1922080042)



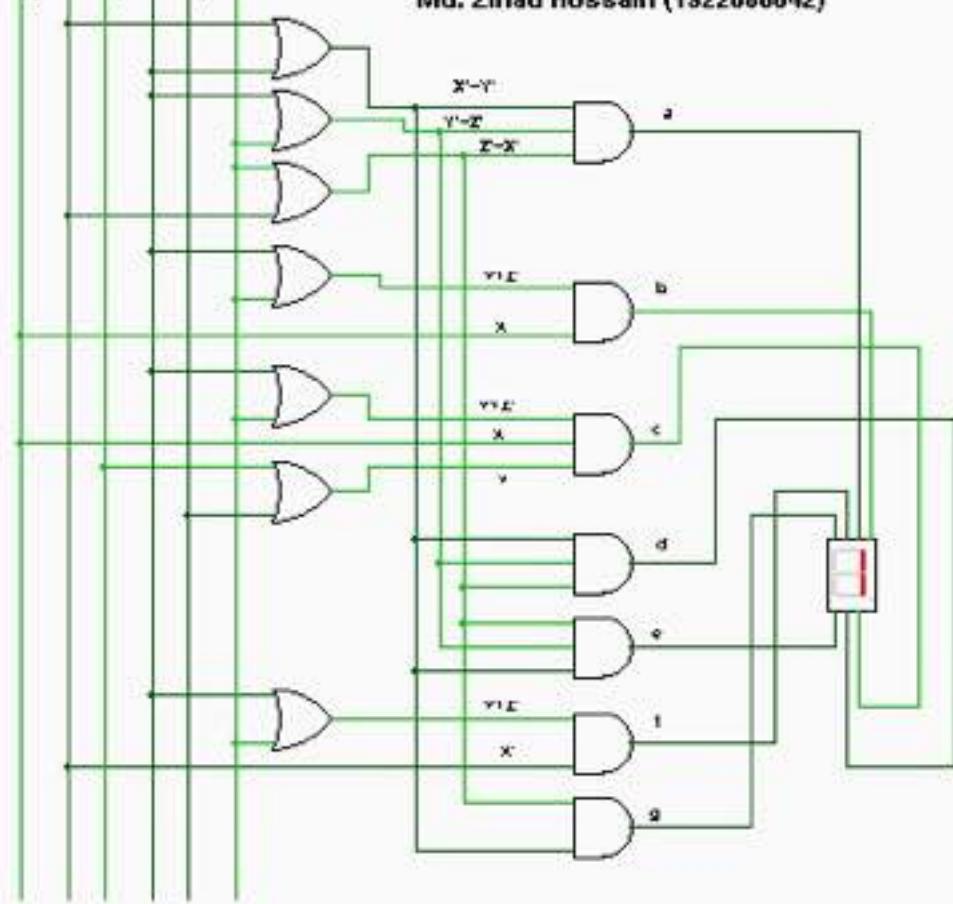


Project: EEE-211 (Using POS)
Md. Zihad Hossain (1922080042)





Project: EEE-211 (Using POS)
Md. Zihad Hossain (1922080042)



Combinational circuit using SOP

Ashwin Mobashira Shifa.

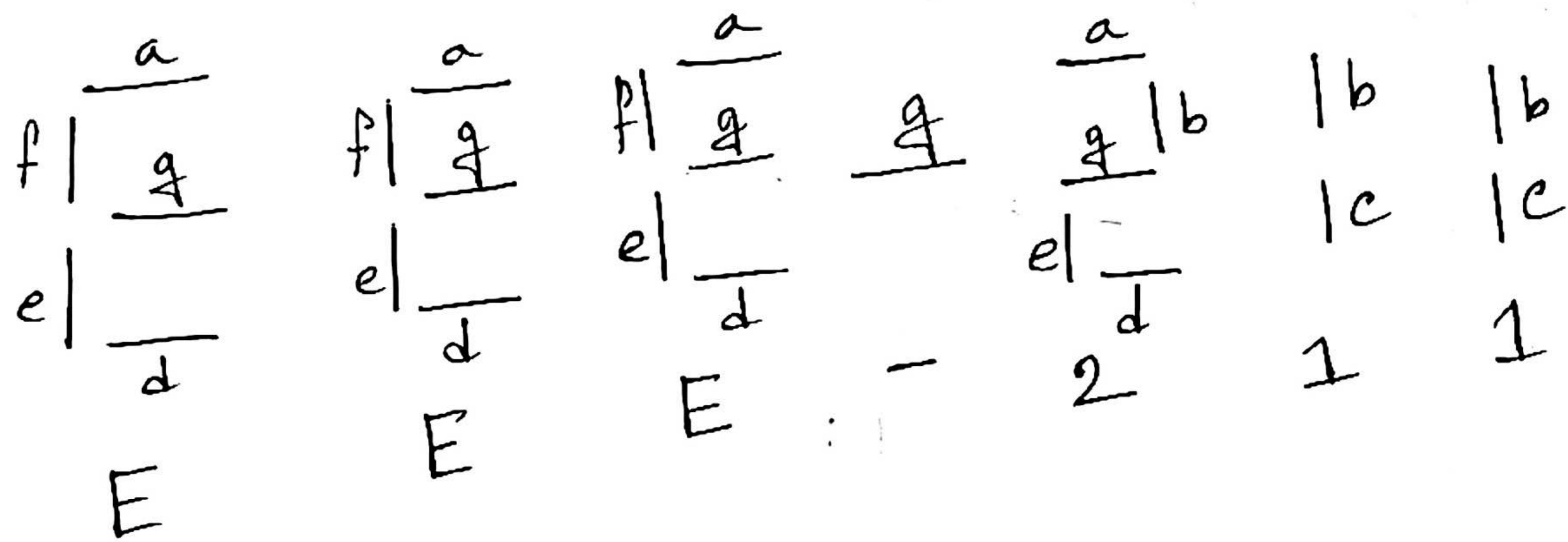
ID: 1922216642

Sec: 10

Course: CSE 231

Group : 06

Project on displaying EEE-211 using 7 segment.



Truth table:

Equations: (SOP)

$$a = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$b = A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$$

$$c = A\bar{B}C + ABC$$

$$d = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$e = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$f = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

$$g = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C}$$

K-map for $a = \sum(0, 1, 2, 4)$

A \ BC	00	01	11	10
0	1	D	0	1
1	1	0	X	0

$$a = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$$

K-map for $b = \sum(4, 5, 6)$

A \ BC	00	01	11	10
0	0	0	0	0
1	1	1	X	D

$$b = A$$

K-map for $c = \sum(5, 6)$

A \ BC	00	01	11	10
0	0	0	0	0
1	0	1	(X)	D

$$c = AC + AB$$

K-map for $d = \sum(0, 1, 2, 4)$

A\B\c	00	01	11	10
0	1	1	0	1
1	1	0	x	0

$$d = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$$

K-map for $e = \sum(0, 1, 2, 4)$

A\B\c	00	01	11	10
0	1	1	0	1
1	1	0	x	0

$$e = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$$

K-map for $f = \sum(0, 1, 2)$

A\B\c	00	01	11	10
0	1	1	0	1
1	0	0	x	0

$$f = \bar{A}\bar{B} + \bar{A}\bar{C}$$

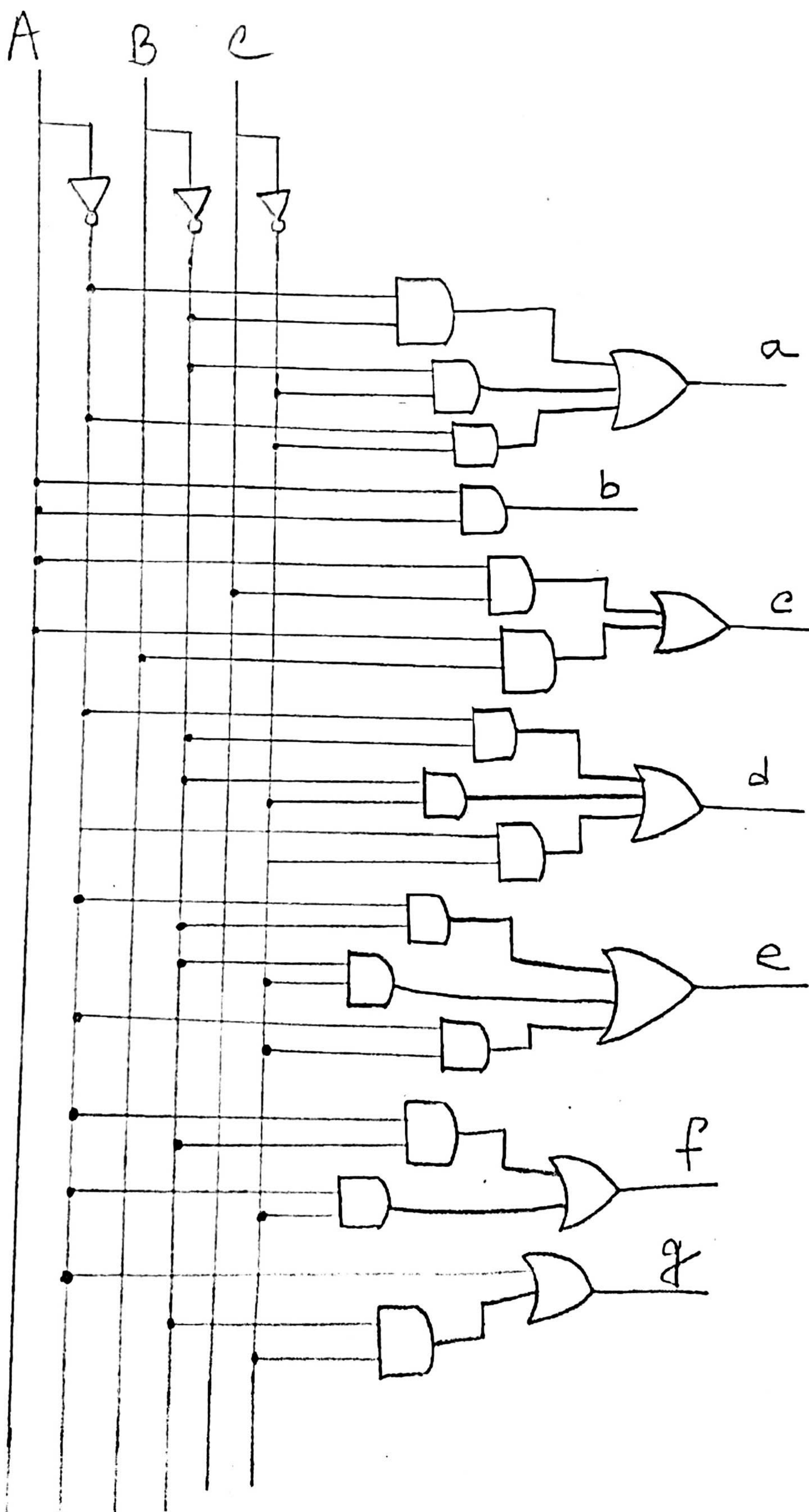
K-map for $g = \sum(0, 1, 2, 3, 4)$

A\B\c	00	01	11	10
0	1	1	1	1
1	1	0	x	0

$$g = \bar{A} + \bar{B}\bar{C}$$

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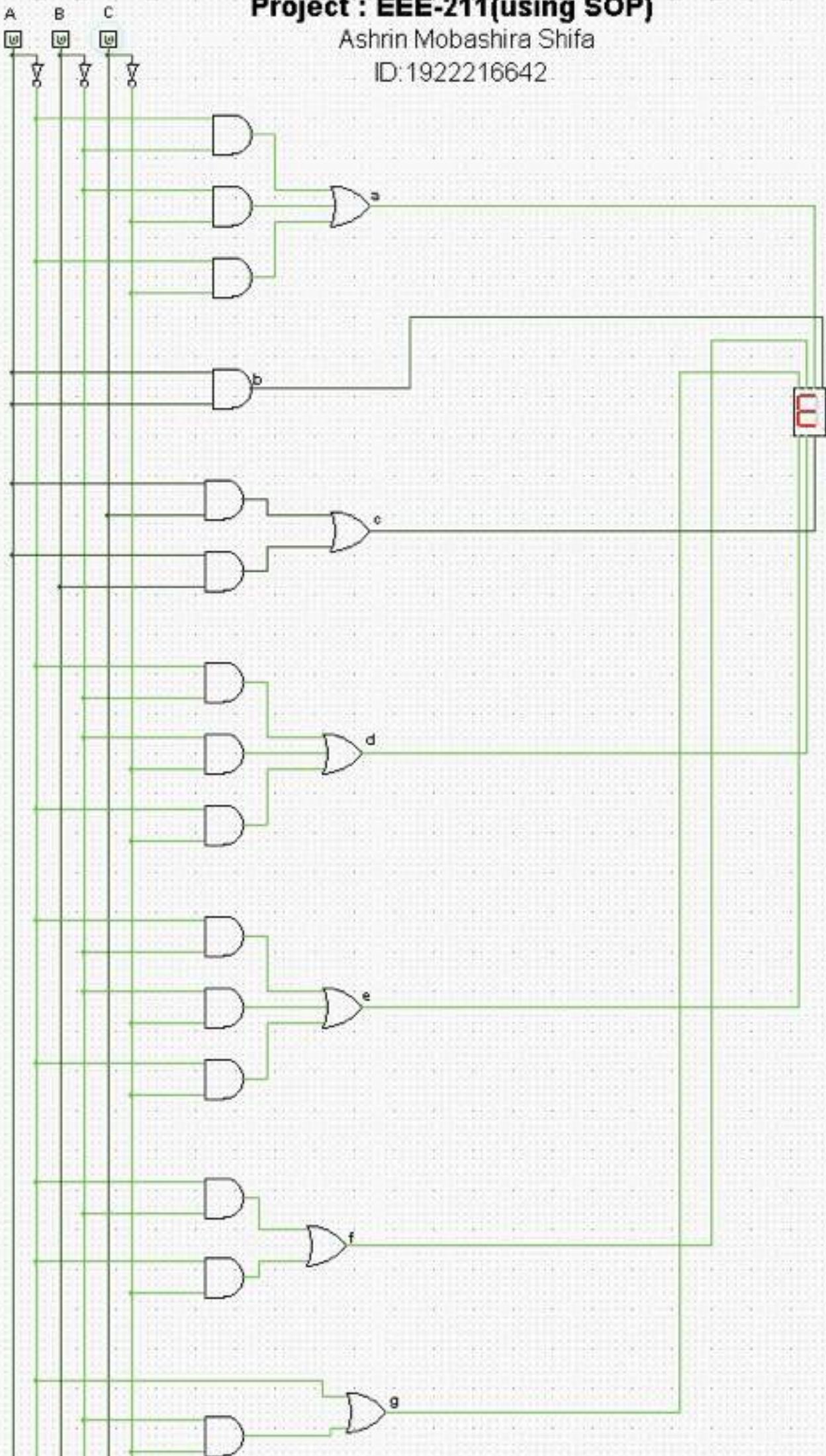
Circuit:



Project : EEE-211(using SOP)

Ashrin Mobashira Shifa

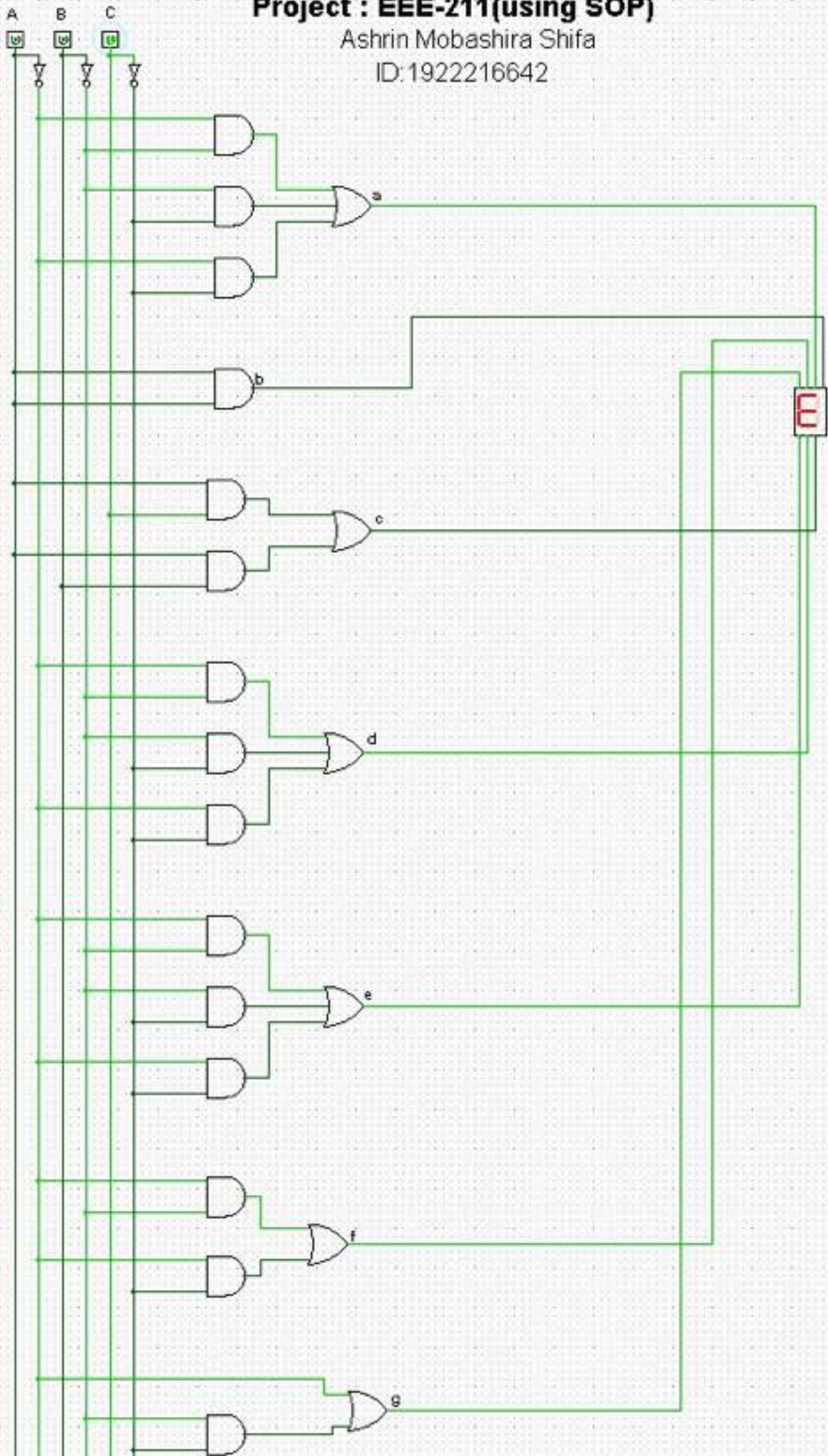
ID:1922216642



Project : EEE-211(using SOP)

Ashrin Mobashira Shifa

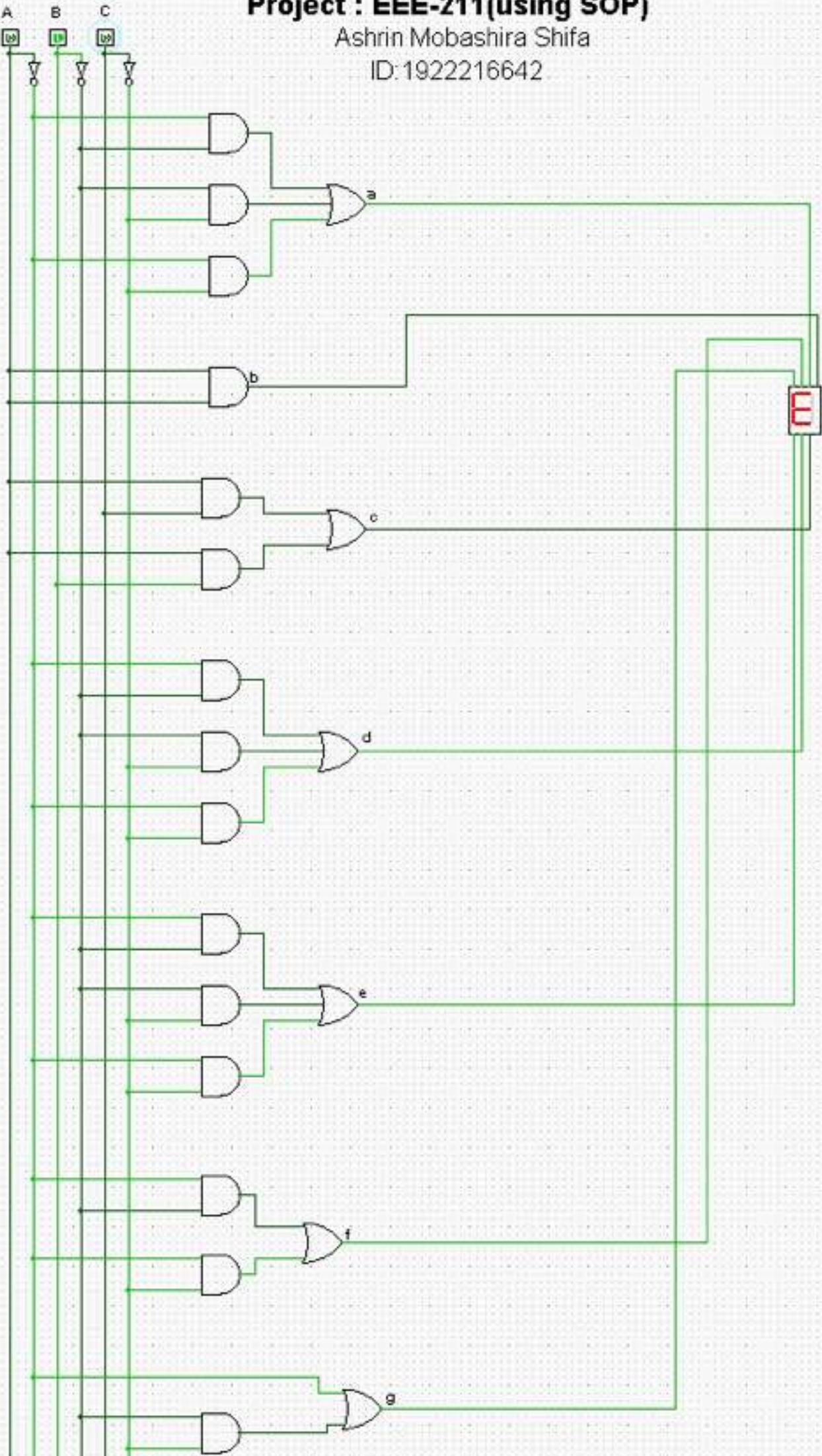
ID:1922216642



Project : EEE-211(using SOP)

Ashrin Mobashira Shifa

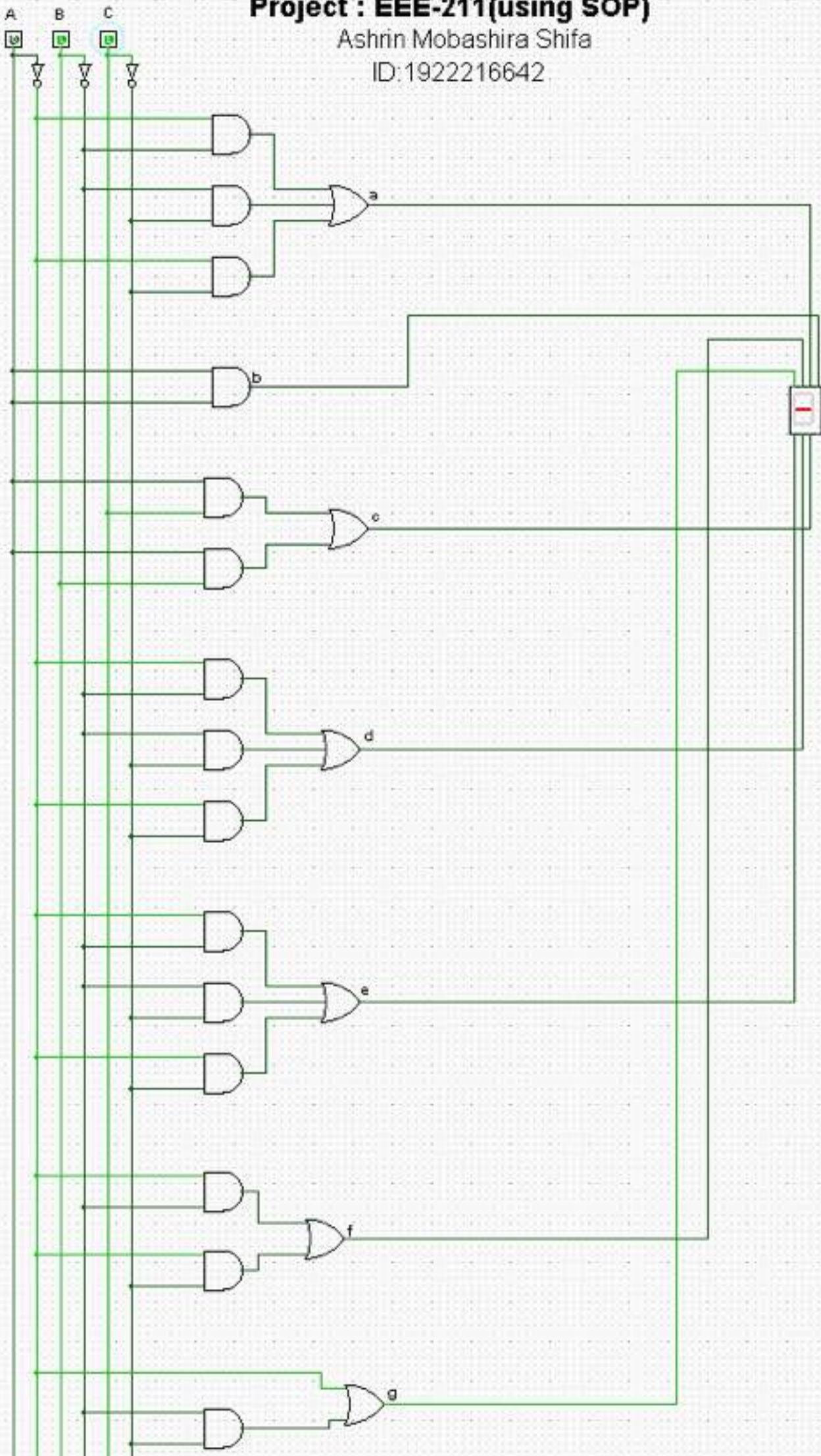
ID:1922216642



Project : EEE-211(using SOP)

Ashrin Mobashira Shifa

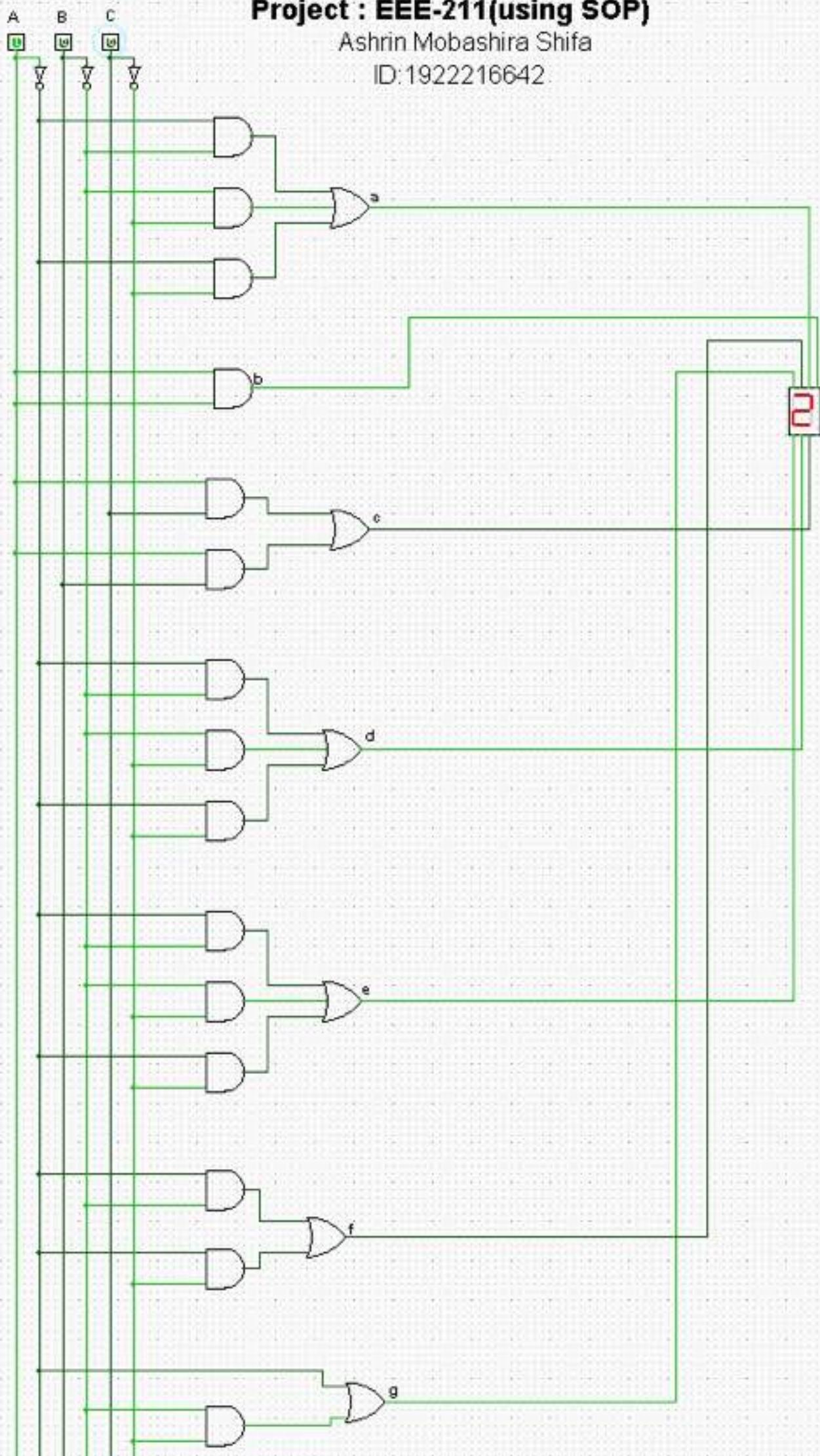
ID:1922216642



Project : EEE-211(using SOP)

Ashrin Mobashira Shifa

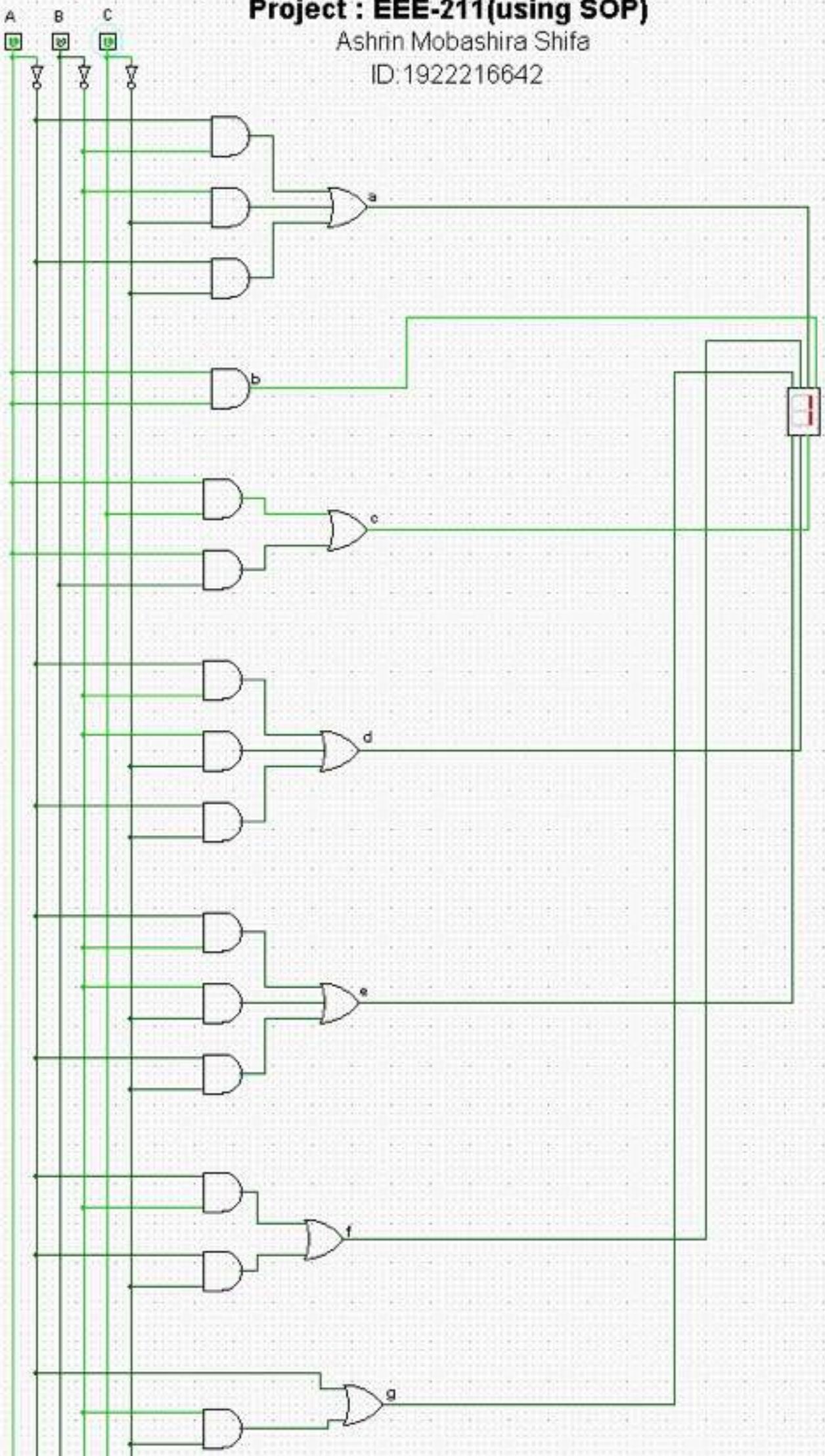
ID:1922216642



Project : EEE-211(using SOP)

Ashrin Mobashira Shifa

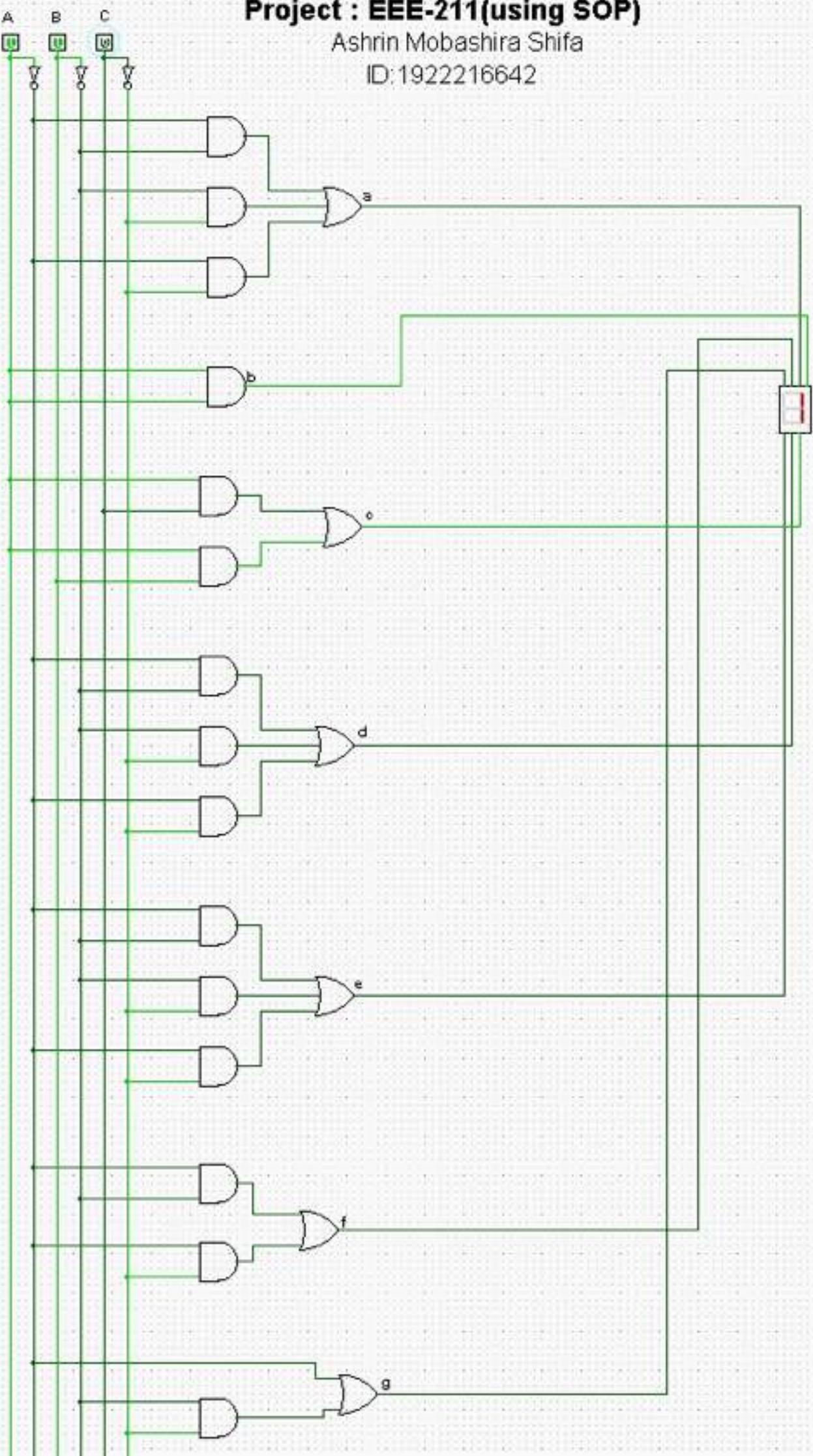
ID:1922216642



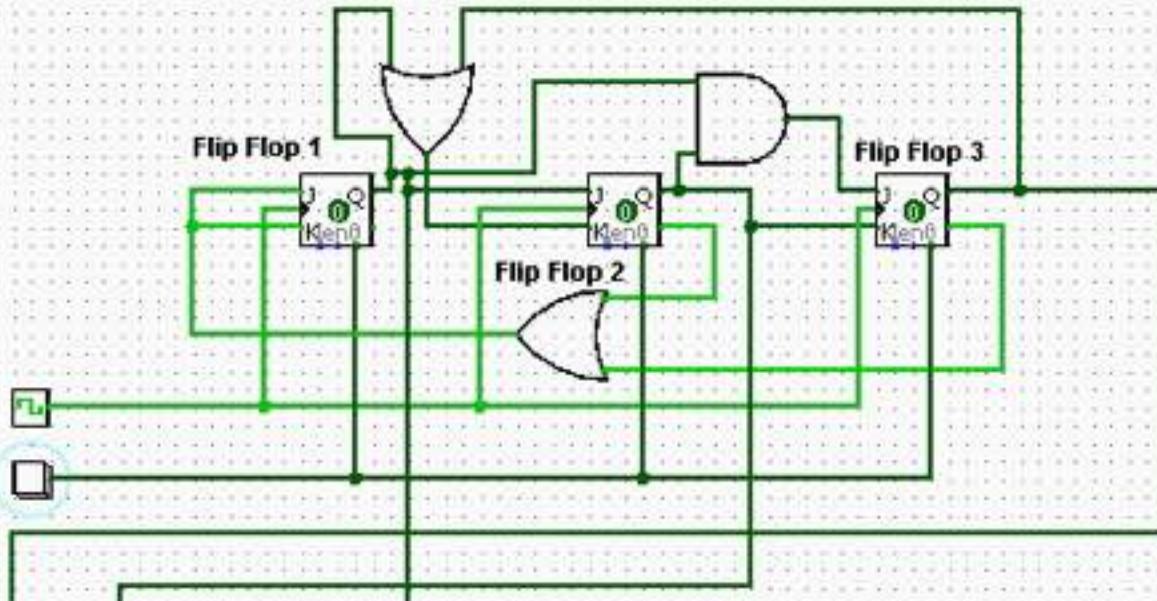
Project : EEE-211(using SOP)

Ashrin Mobashira Shifa

ID:1922216642



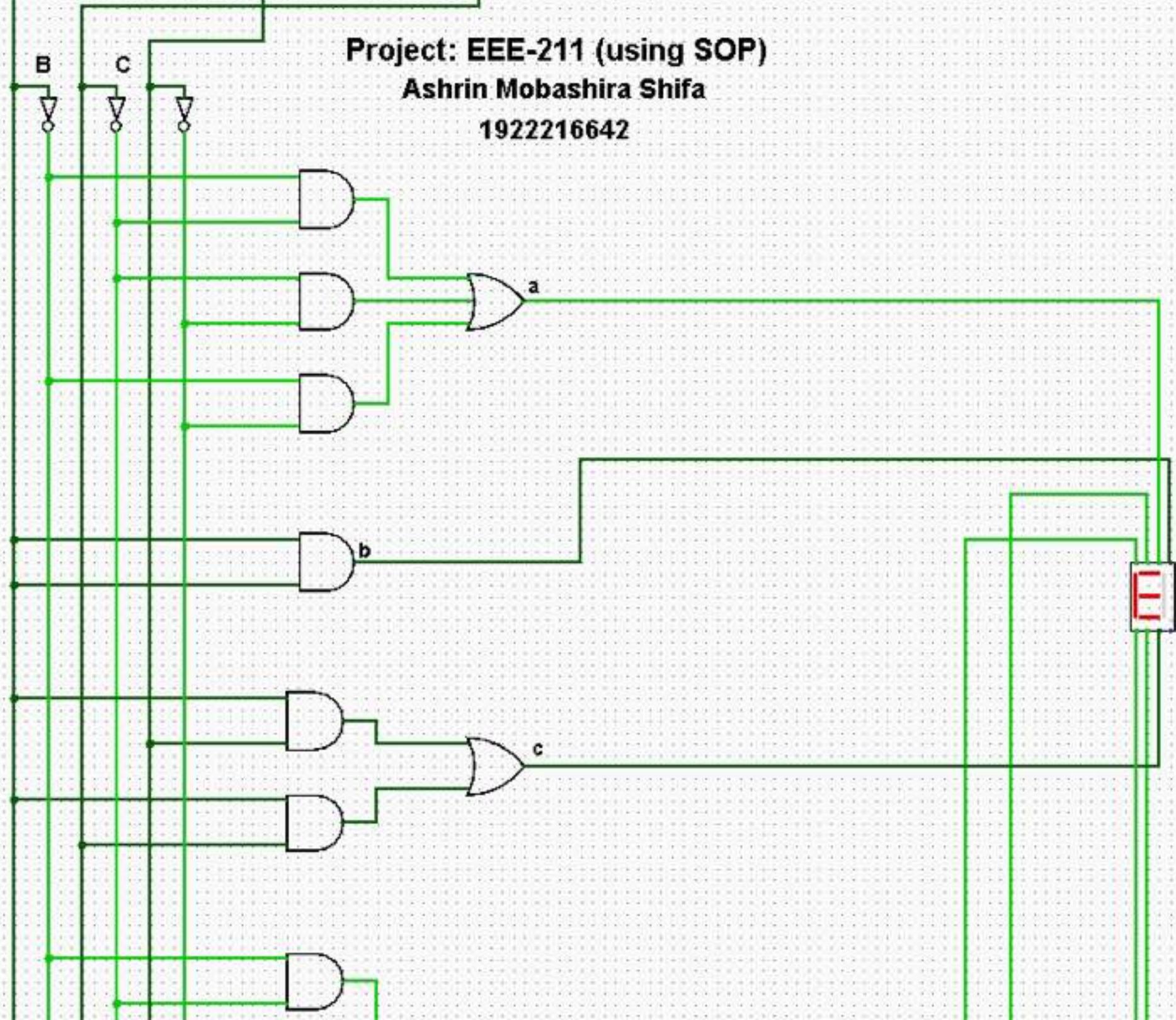
Sequential circuit using { SOP

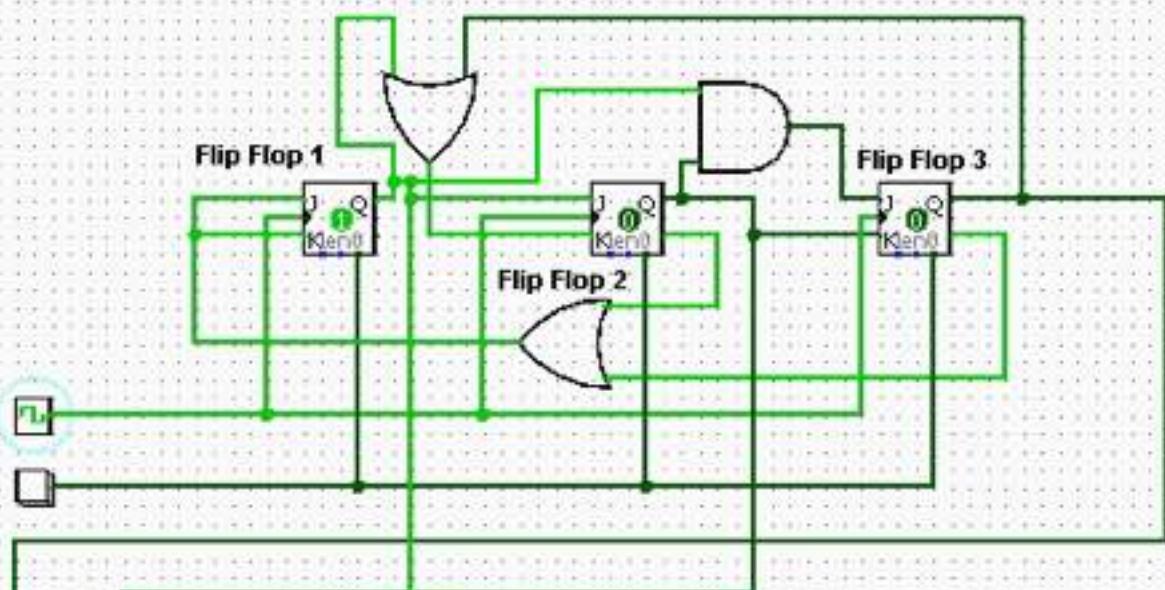


Project: EEE-211 (using SOP)

Ashrin Mobashira Shifa

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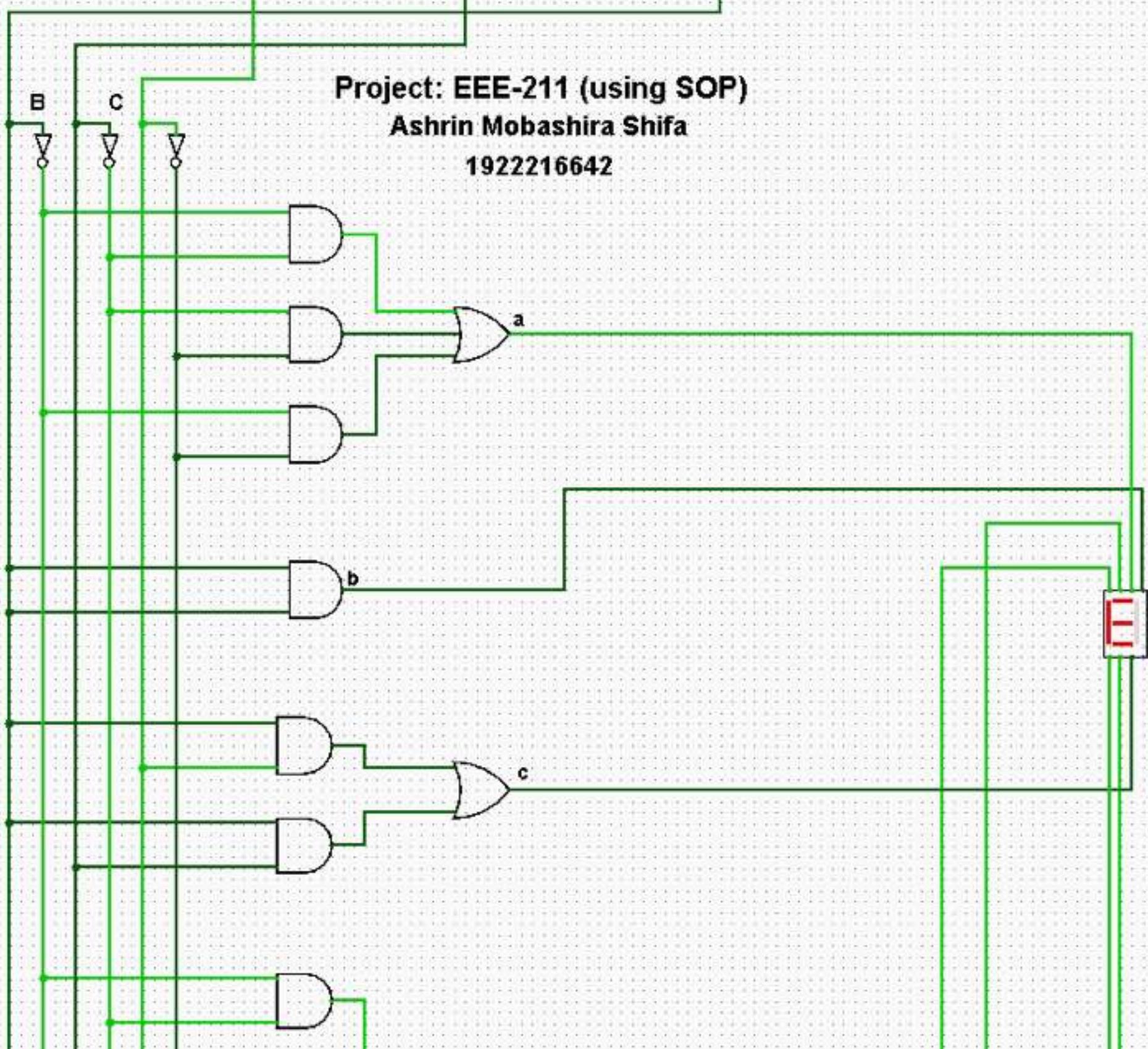


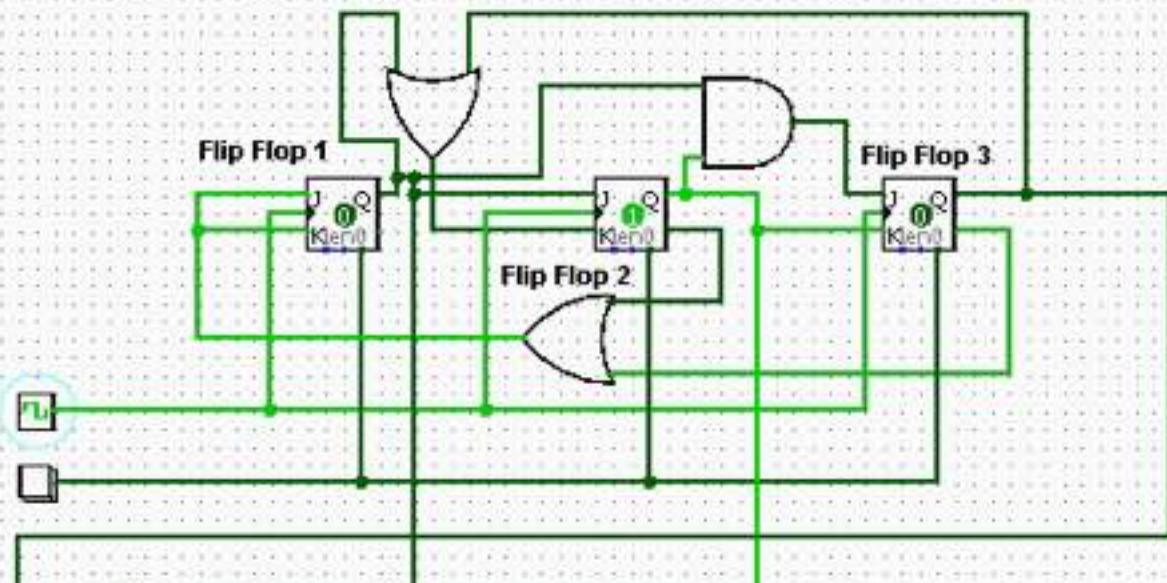


Project: EEE-211 (using SOP)

Ashrin Mobashira Shifa

1922216642

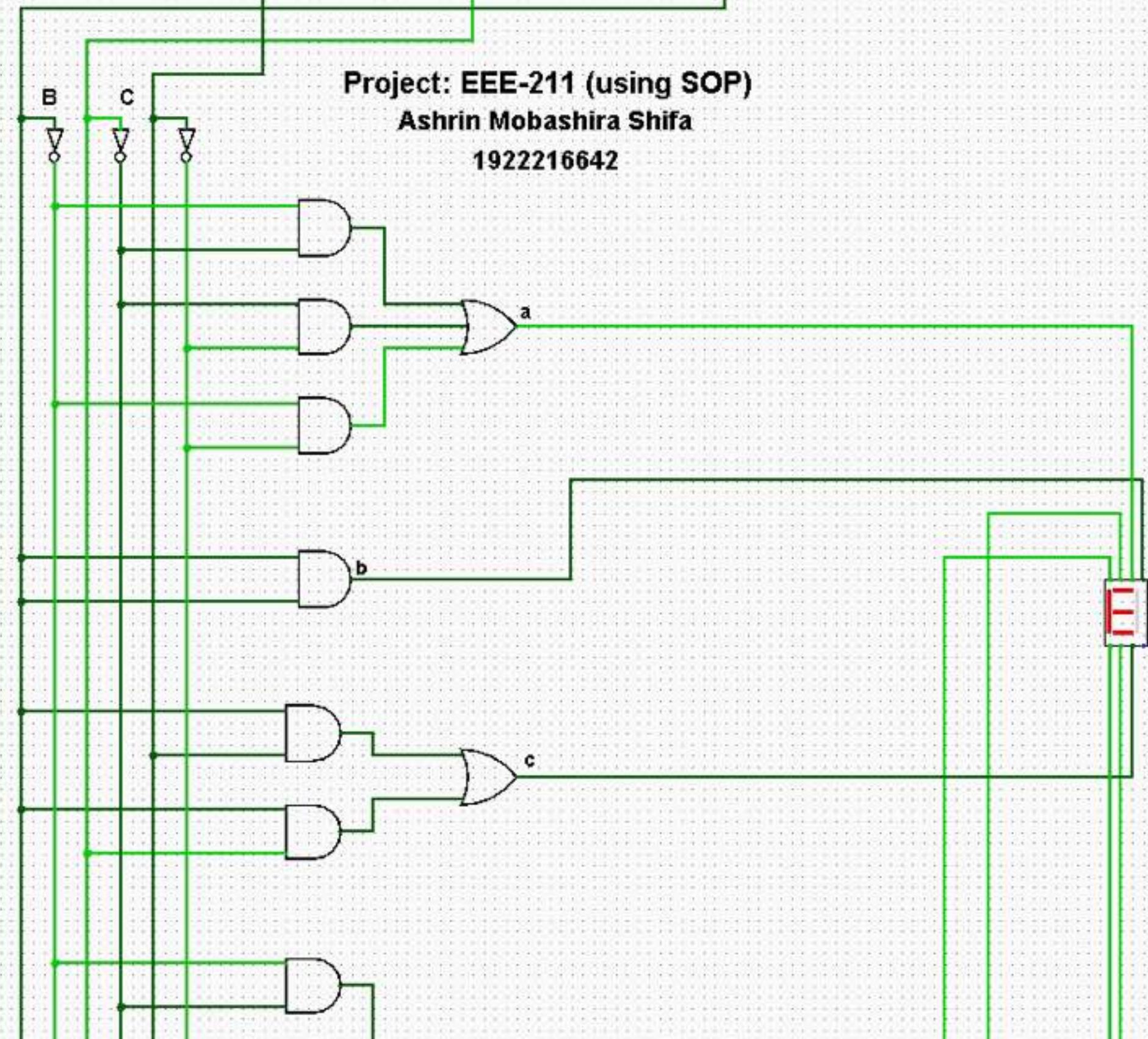


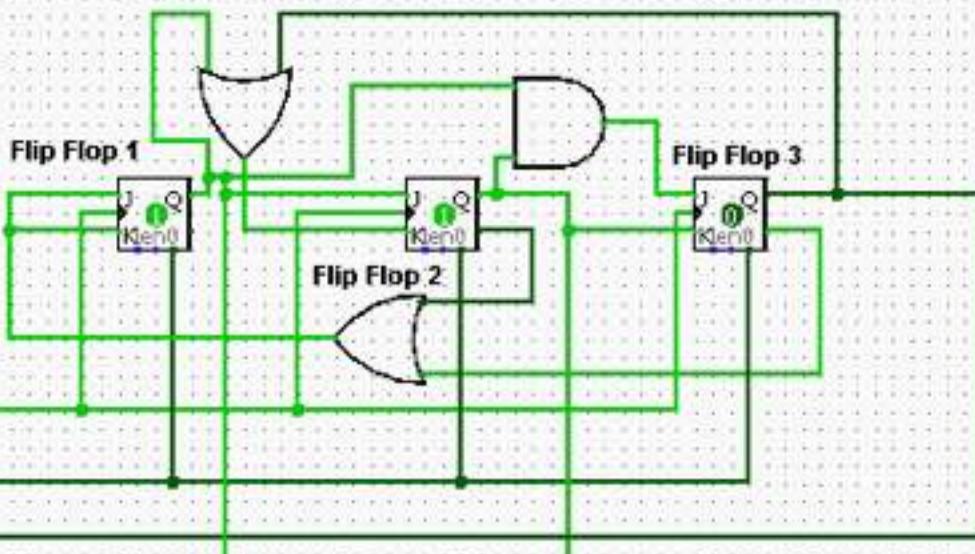


Project: EEE-211 (using SOP)

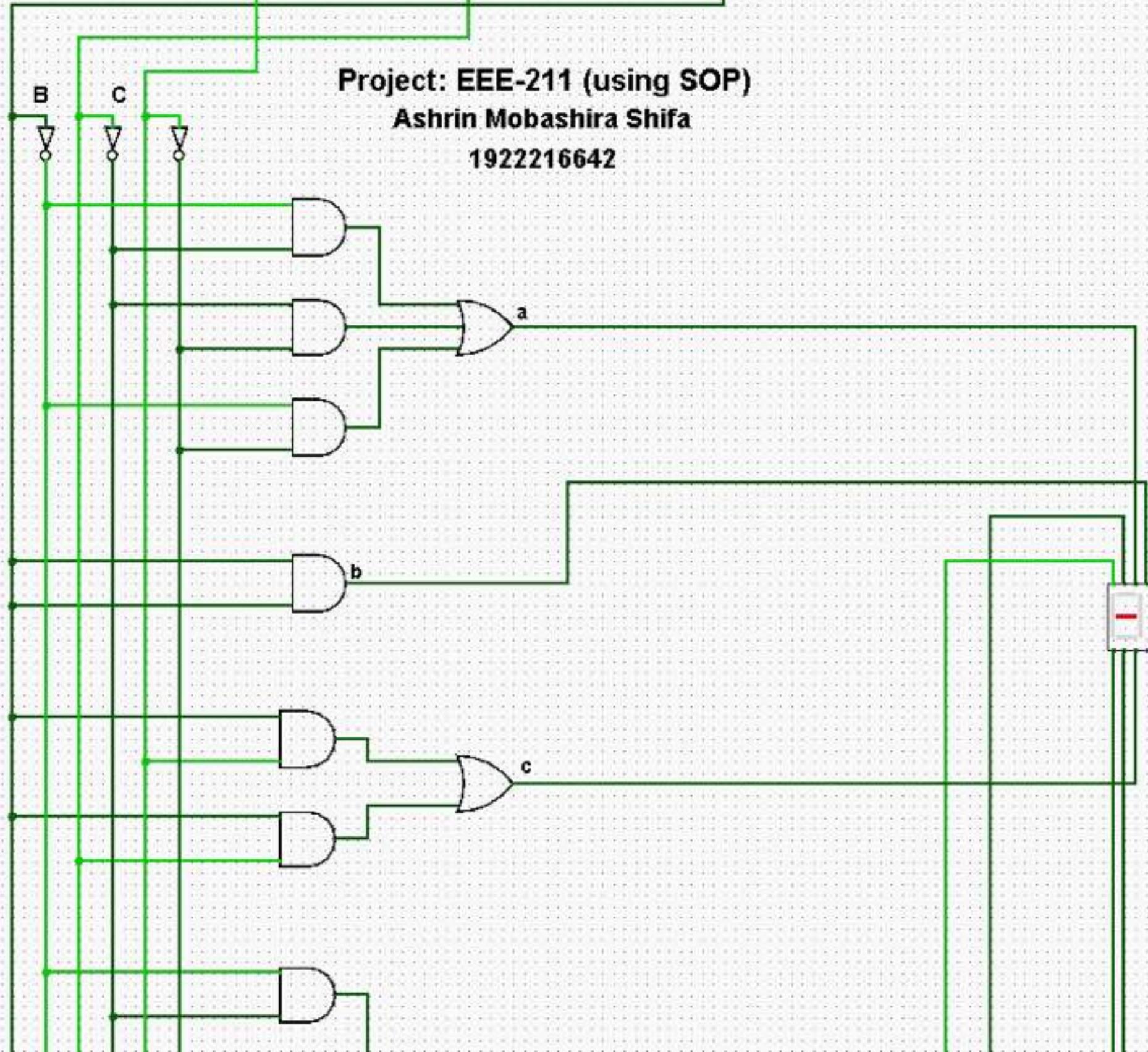
Ashrin Mobashira Shifa

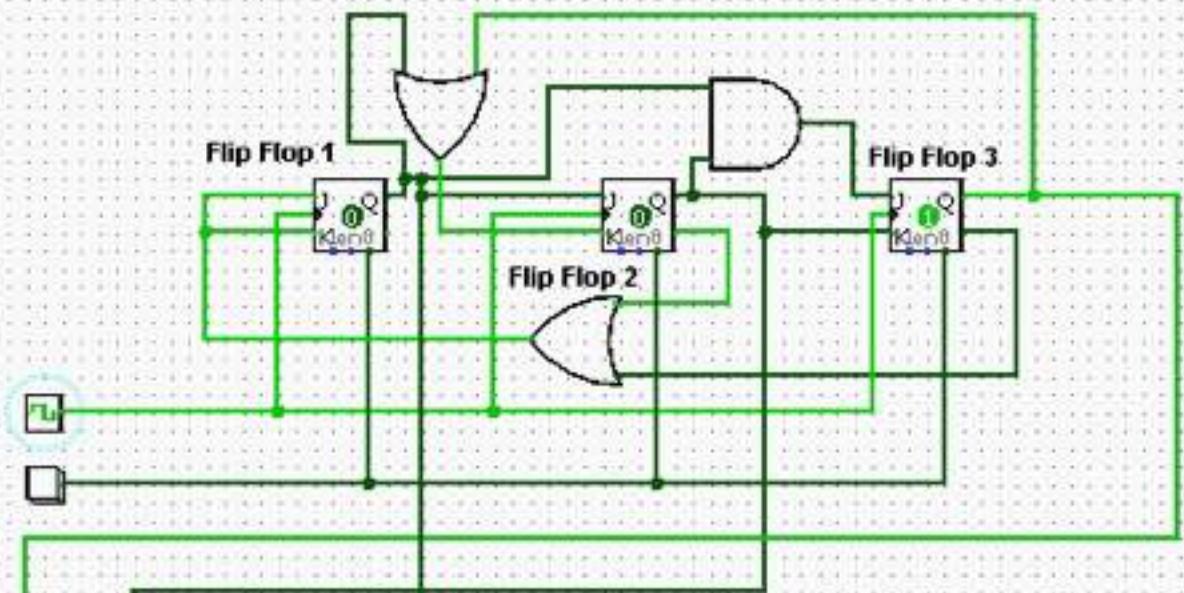
1922216642





Project: EEE-211 (using SOP)
Ashrin Mobashira Shifa
1922216642

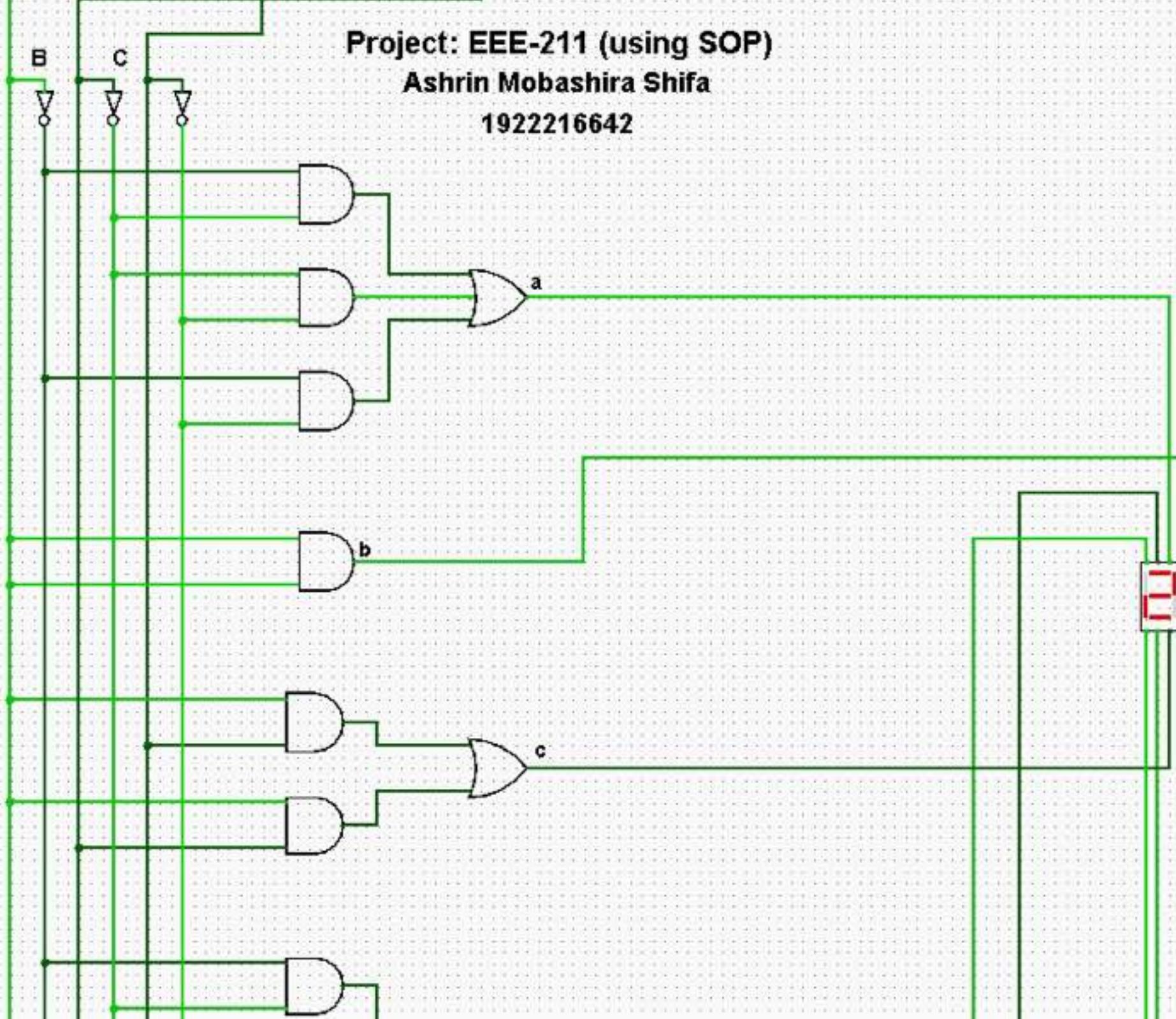


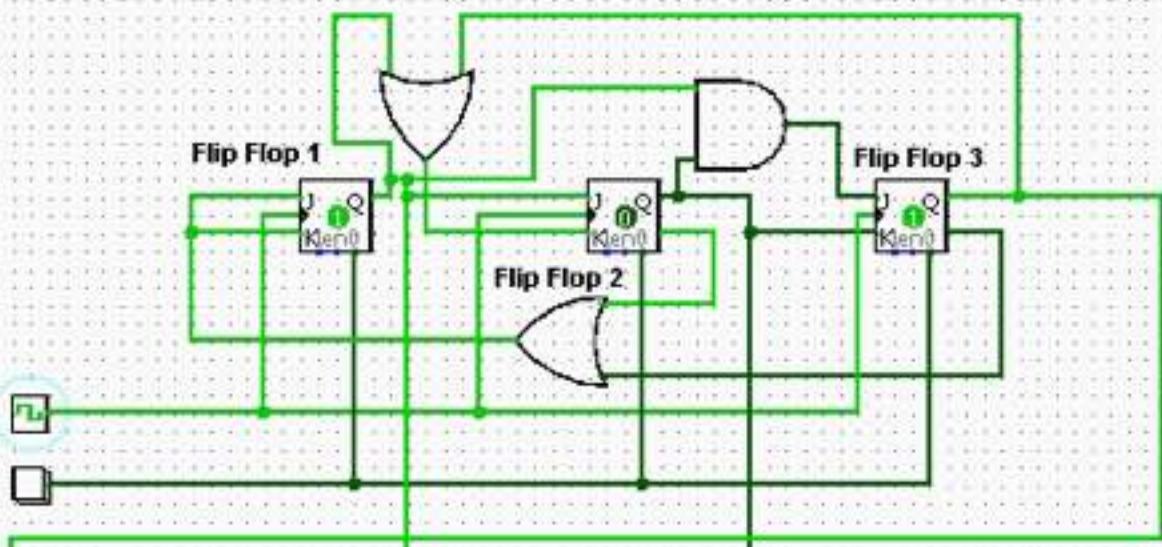


Project: EEE-211 (using SOP)

Ashrin Mobashira Shifa

1922216642

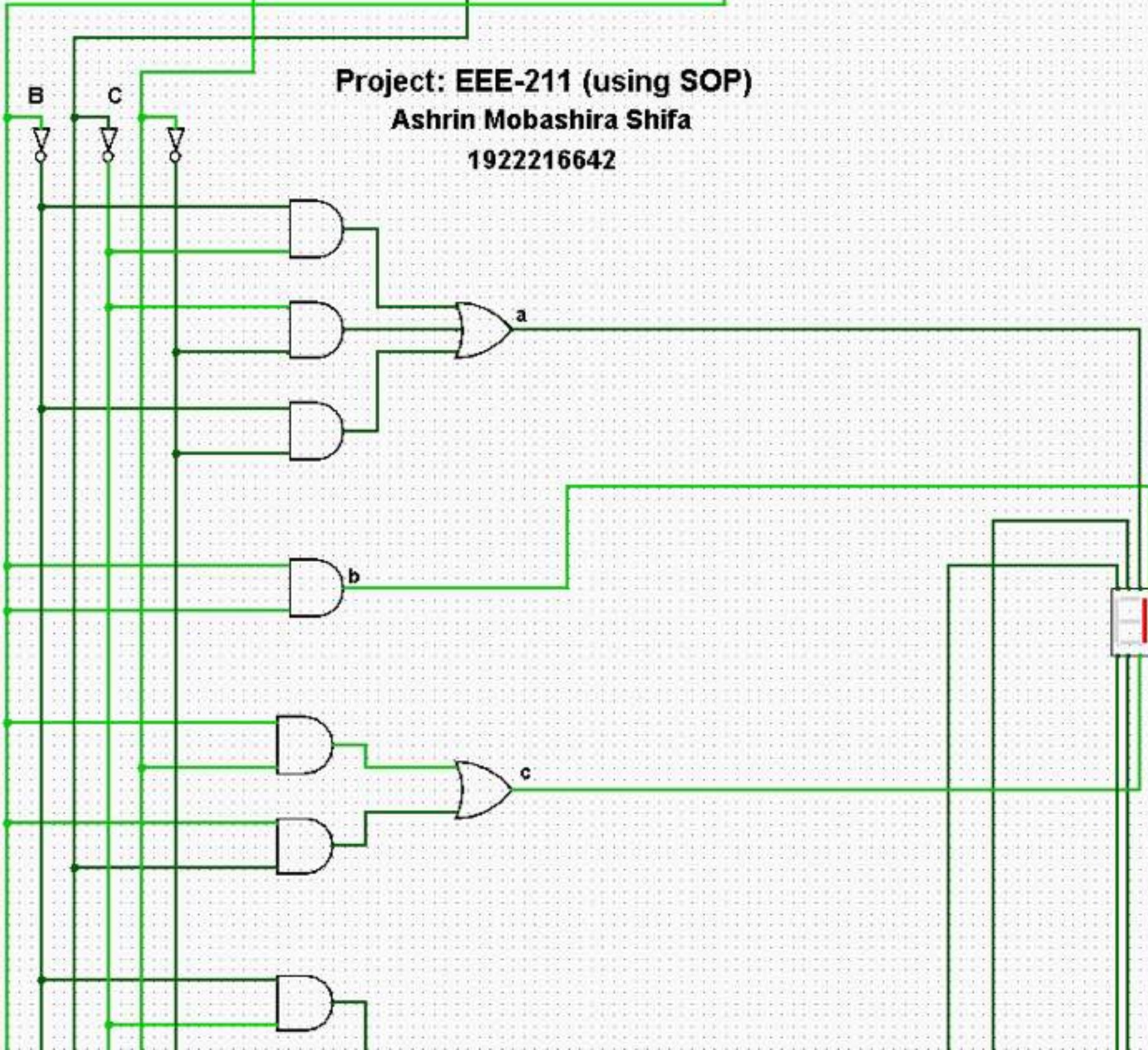


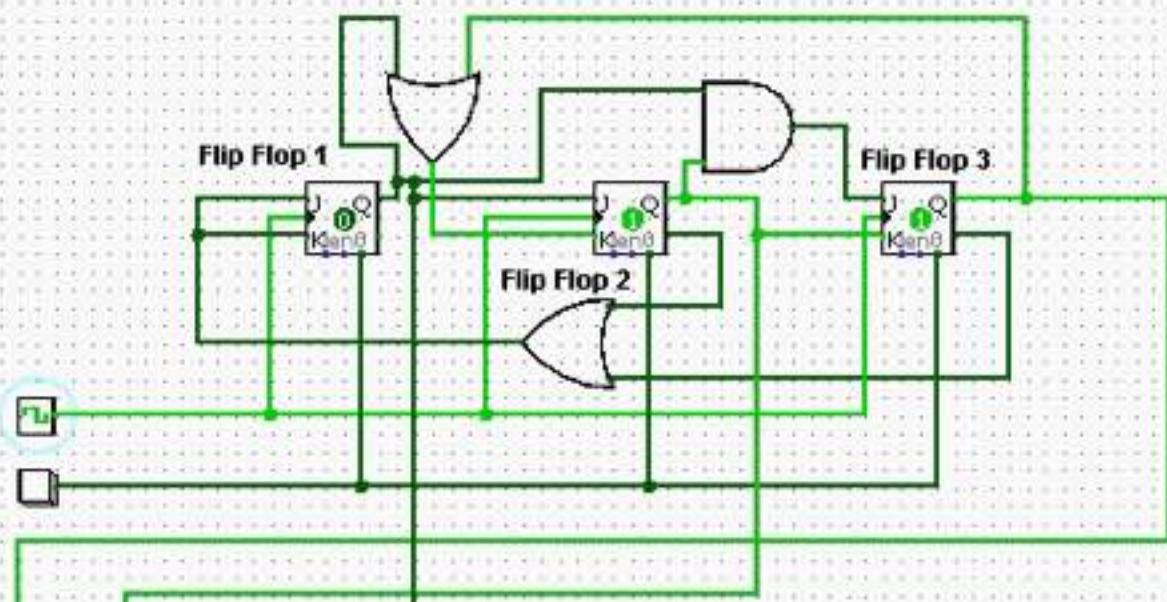


Project: EEE-211 (using SOP)

Ashrin Mobashira Shifa

1922216642

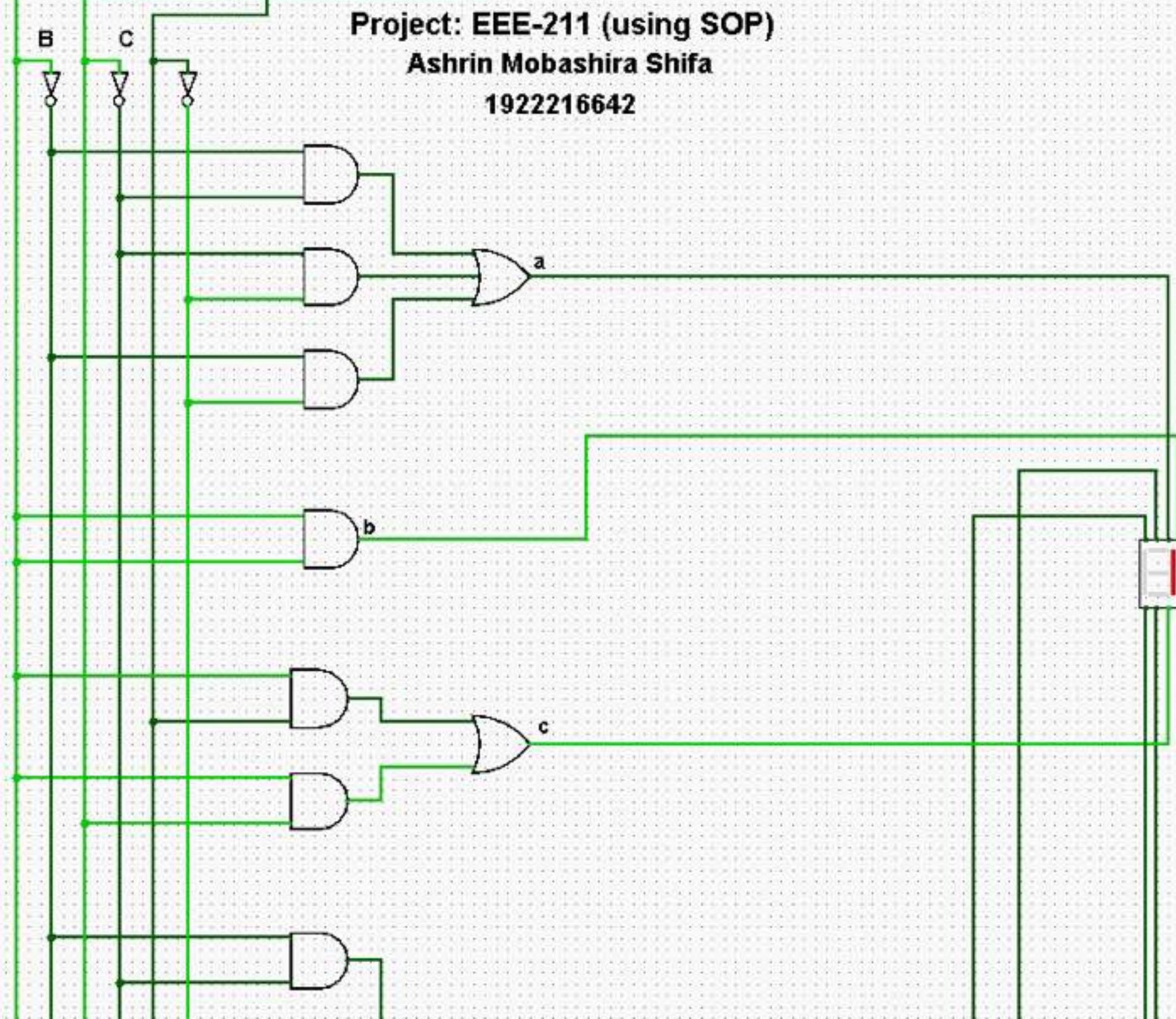




Project: EEE-211 (using SOP)

Ashrin Mobashira Shifa

1922216642

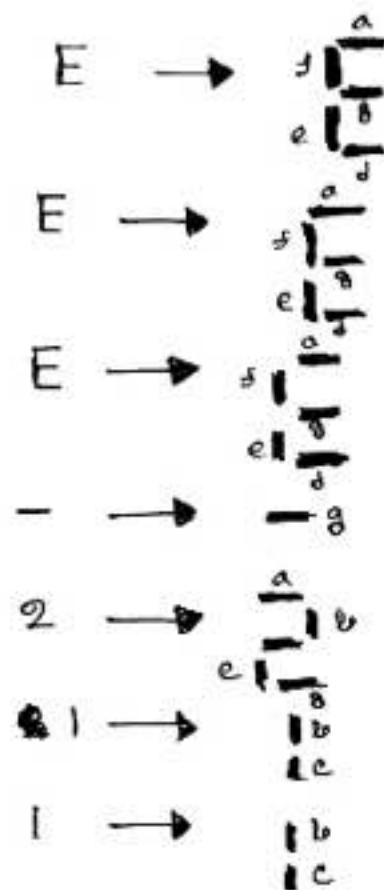


Combinational circuit using NOR

Name: Mohammad Hossain Chowdhury.
T.D.: 10210202

I D : 1931328042

EEE-211" is our project ▶



Truth Table

Deriving the equation Using sum of product(SOP):

$$a = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$b = A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$$

$$c = A\bar{B}C + AB\bar{C}$$

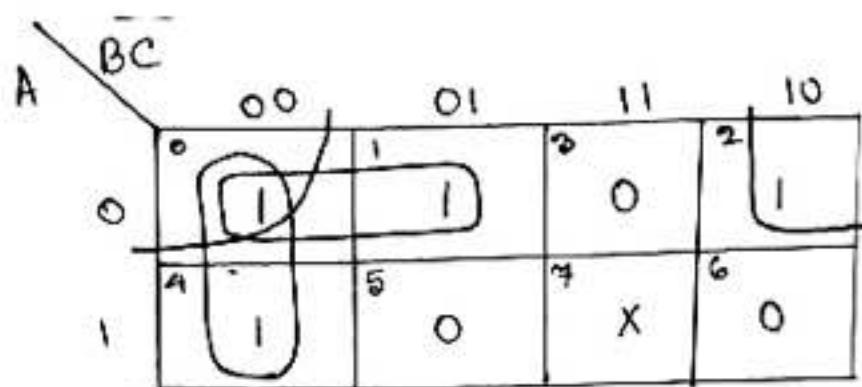
$$d = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$e = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$f = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

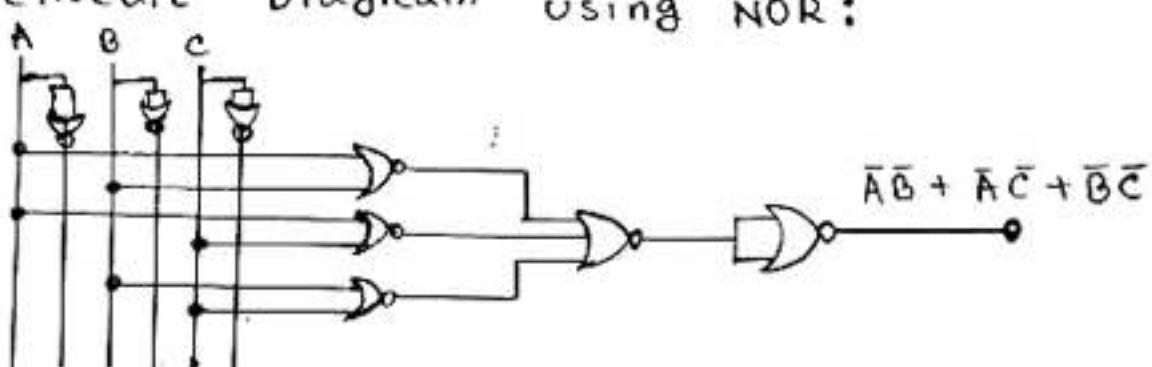
$$g = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C}$$

K-map for segment a:

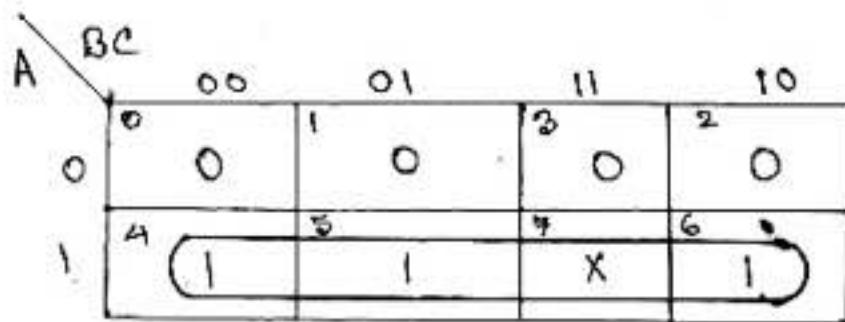


$$\therefore \text{Logic for segment } a = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$$

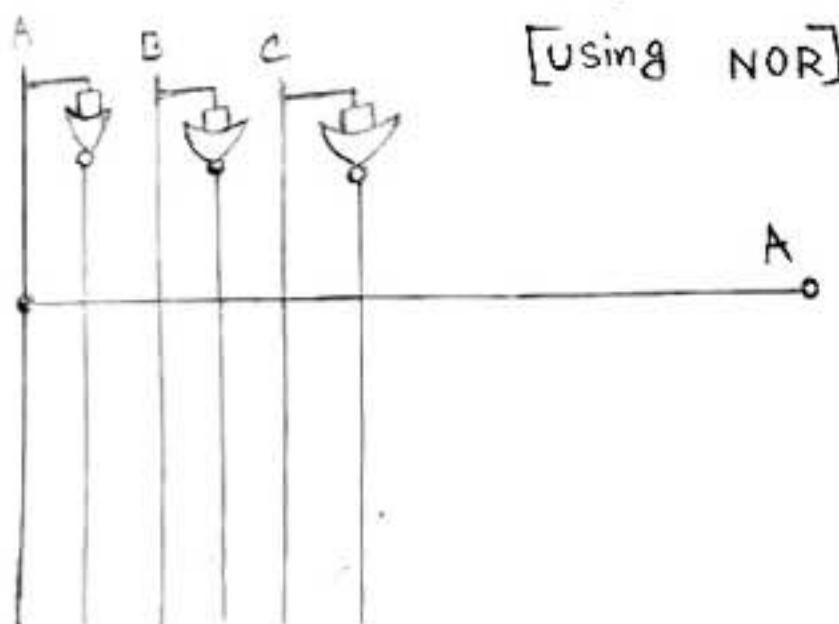
Circuit Diagram using NOR:



K-map for segment b:



$$\therefore \text{Logic for segment } b = A$$

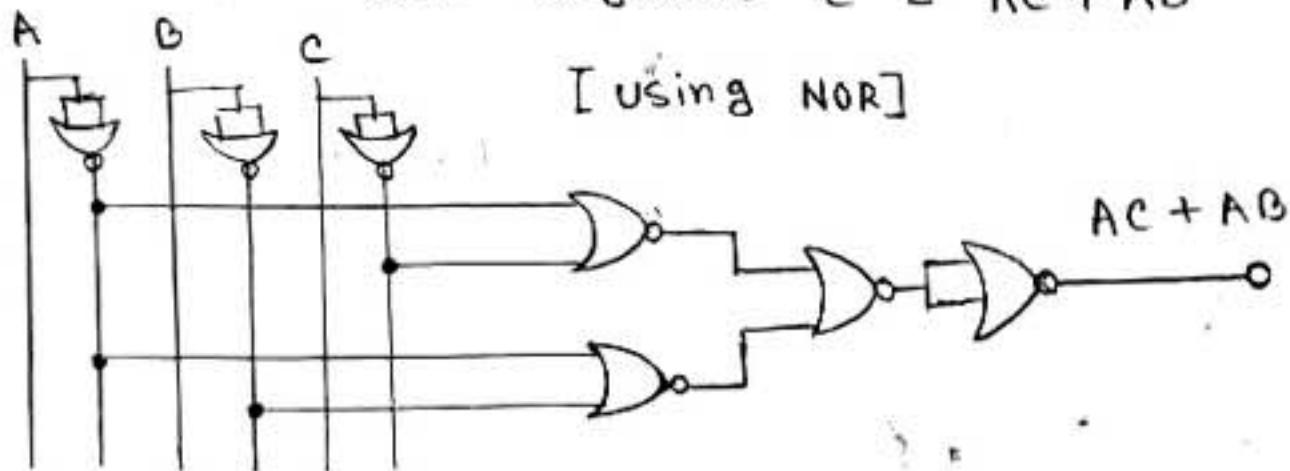


[using NOR]

K-map for segment C:

		BC	00	01	11	10
		A	0	0	0	0
			0	1	1	1
0	0	0	0	0	0	0
0	1	0	1	X	1	1
1	0	0	1	1	X	1
1	1	0	1	1	1	1

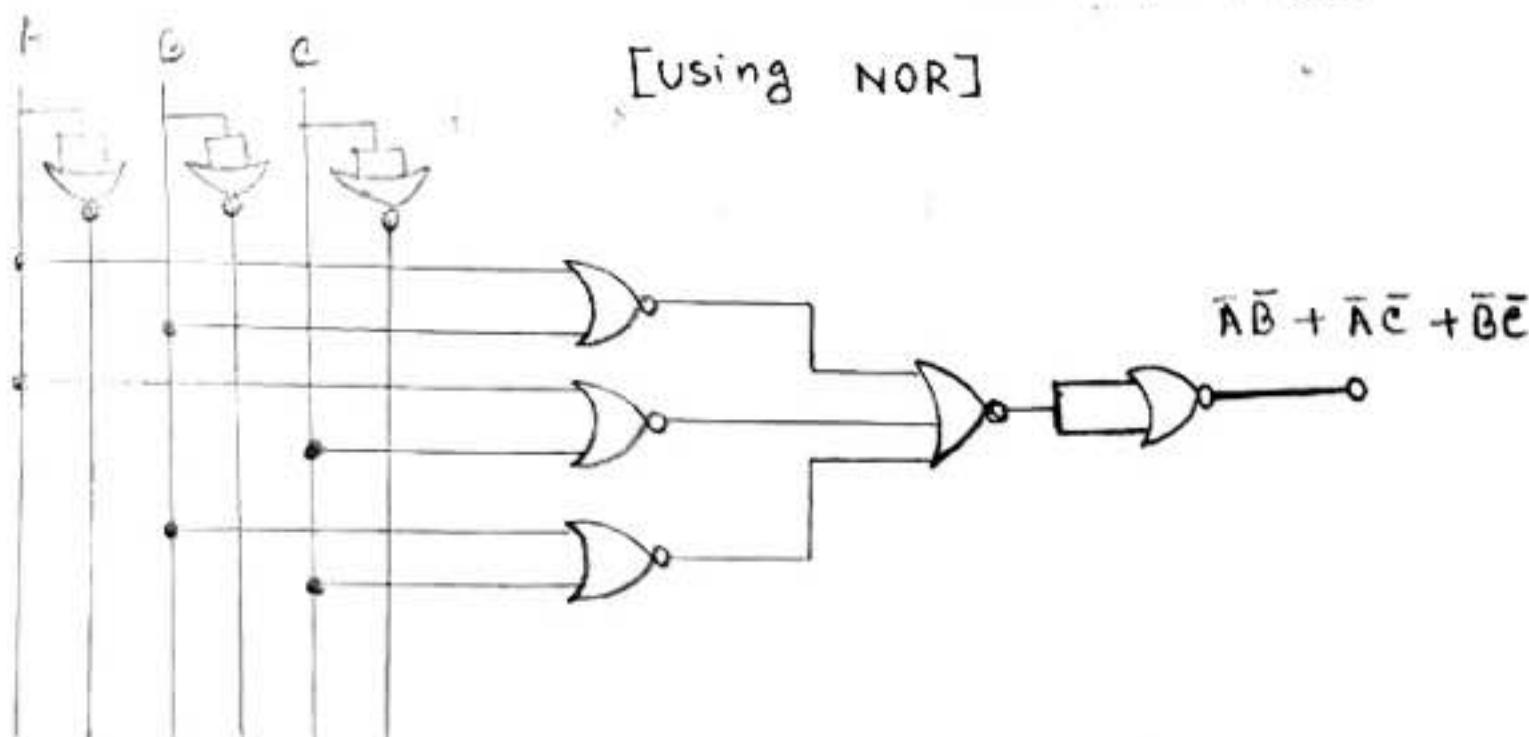
∴ Logic for segment C = AC + AB



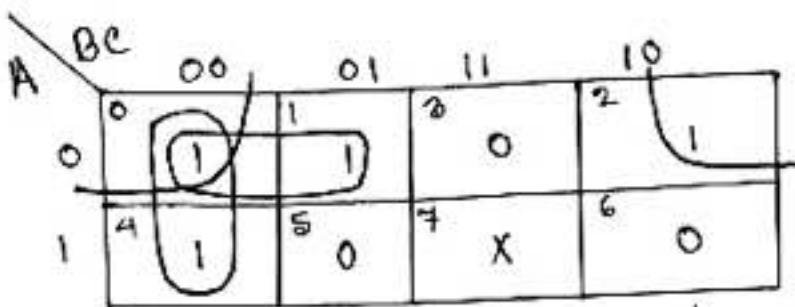
K-map for segment d:

		BC	00	01	11	10
		A	0	1	1	0
			1	0	X	0
0	0	1	1	1	0	0
0	1	0	1	1	X	0
1	0	1	0	X	0	0
1	1	0	0	0	0	0

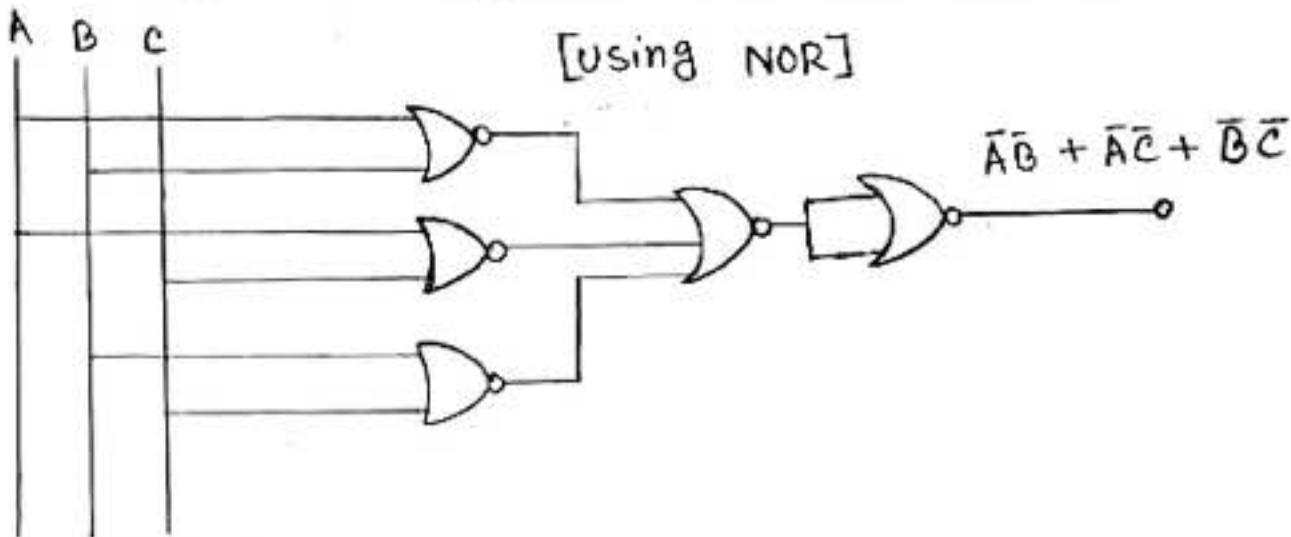
∴ Logic for segment d = $\bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$



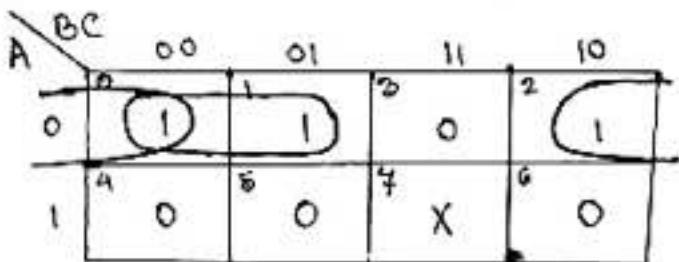
K-map for segment e:



$$\therefore \text{Logic for segment } e = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$$

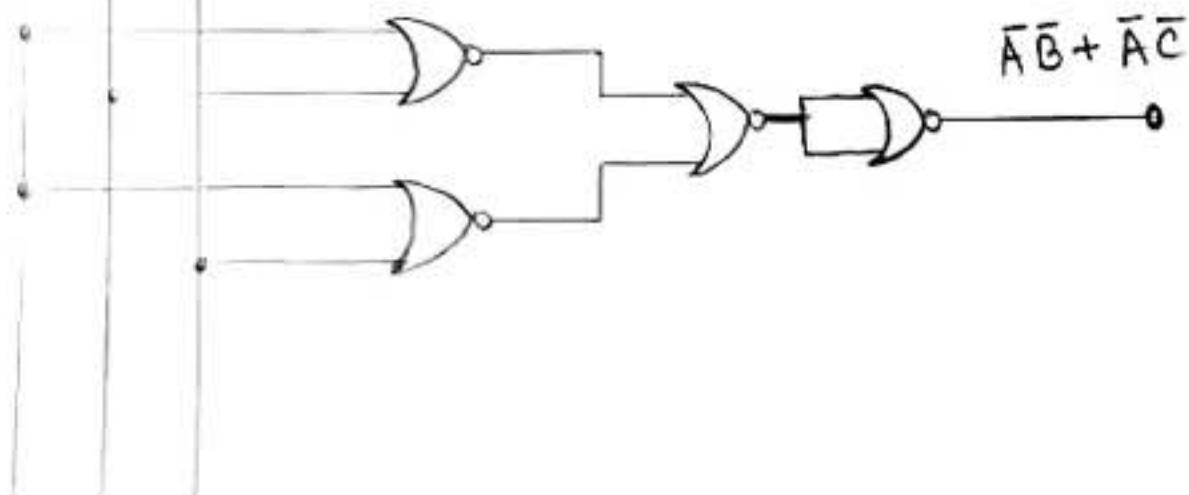


K-map for segment f:



$$\therefore \text{Logic for segment } f = \bar{A}\bar{B} + \bar{A}\bar{C}$$

[using NOR]

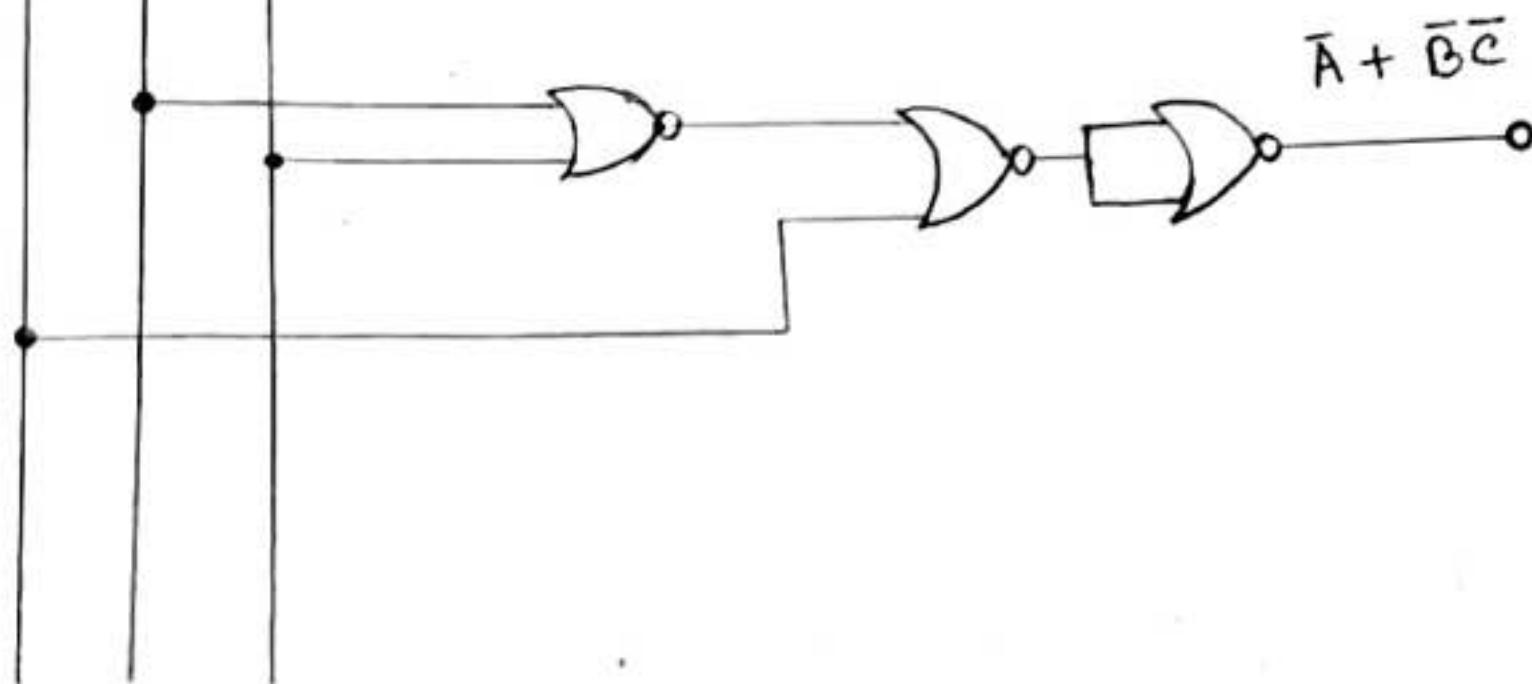


K-map for segment g:

0	1	2	3
4	1	1	1
5	0	X	0
6	1	0	0

∴ Logic for segment g = $\bar{A} + \bar{B}\bar{C}$

A B C [using NOR]

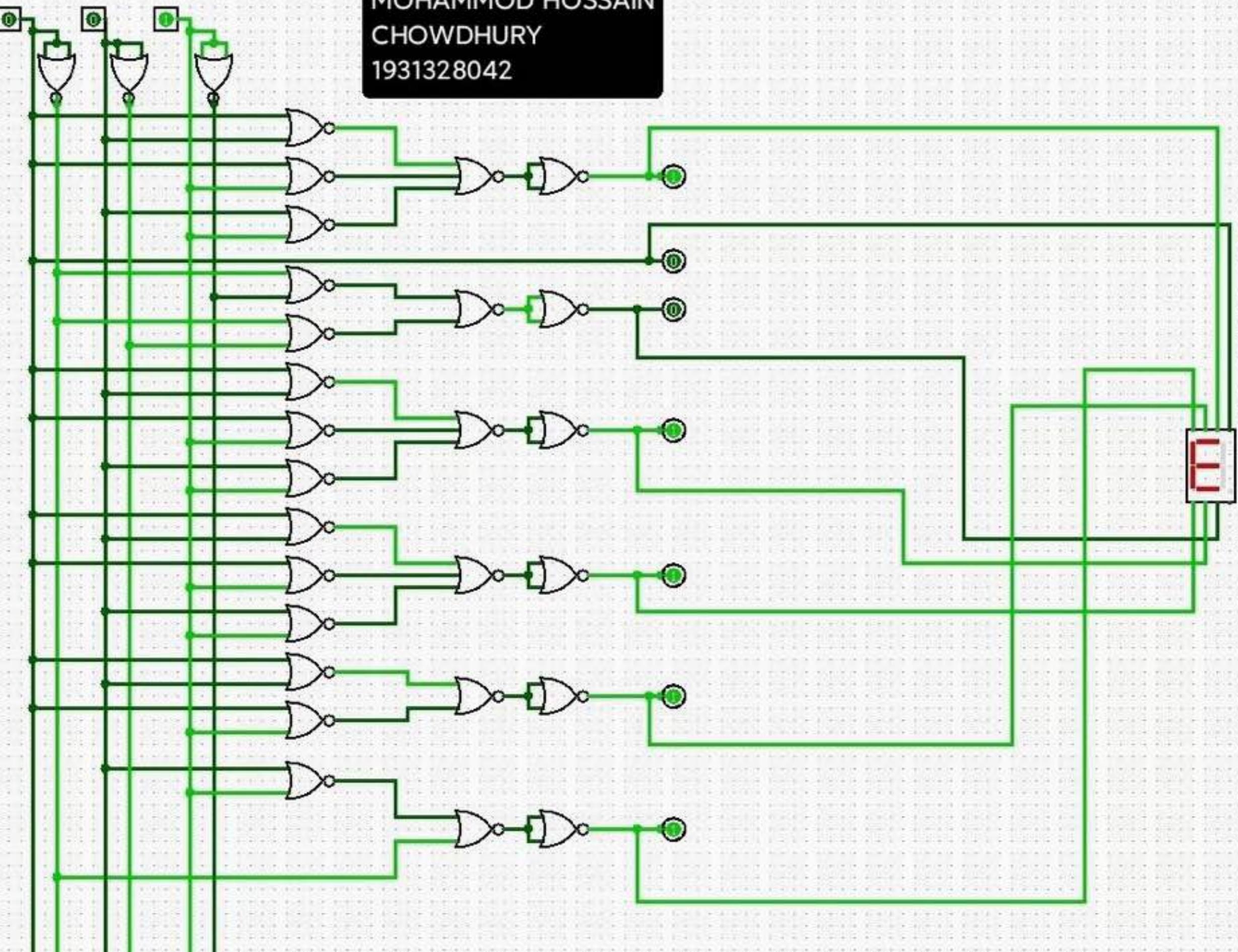


A

B

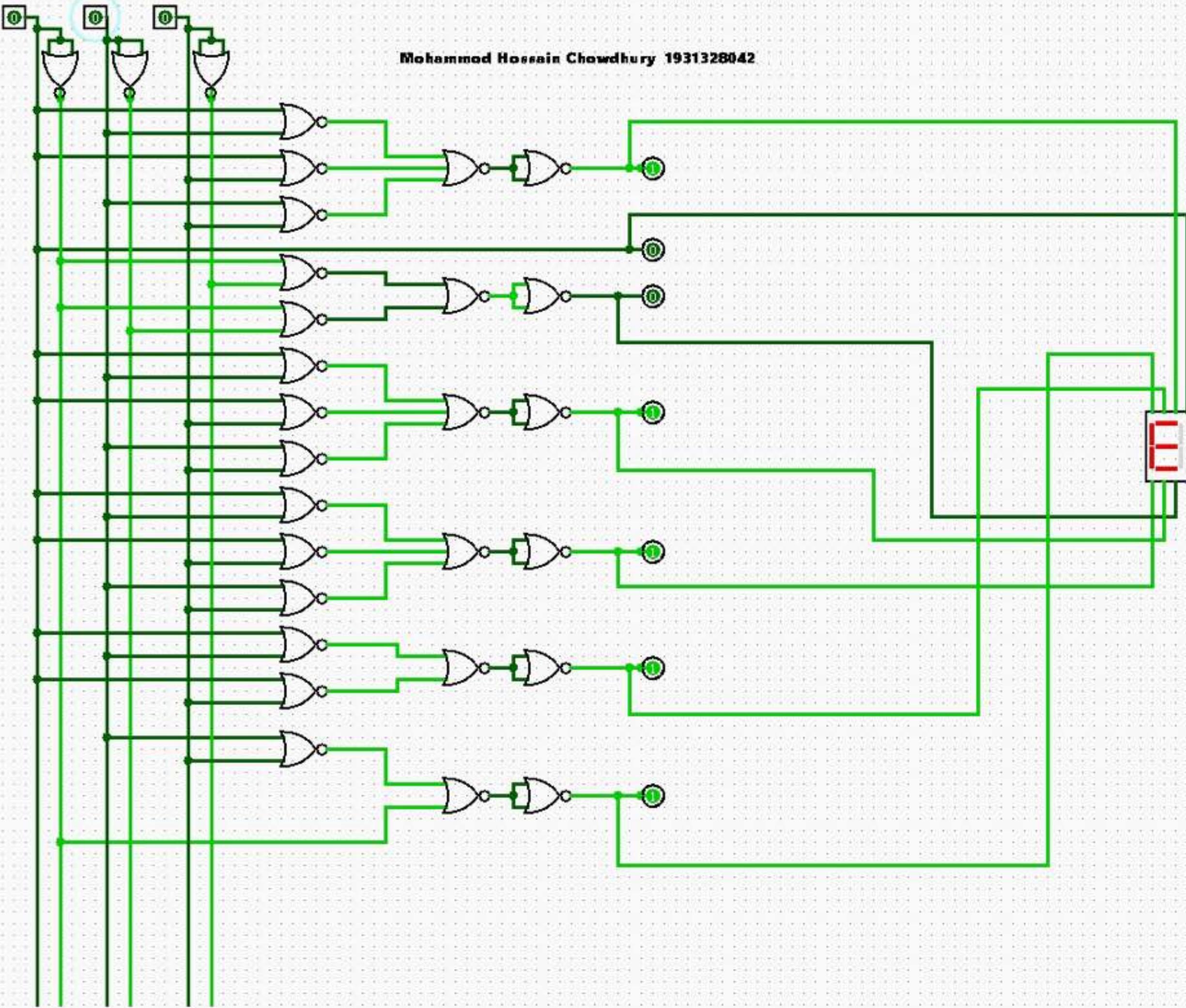
C

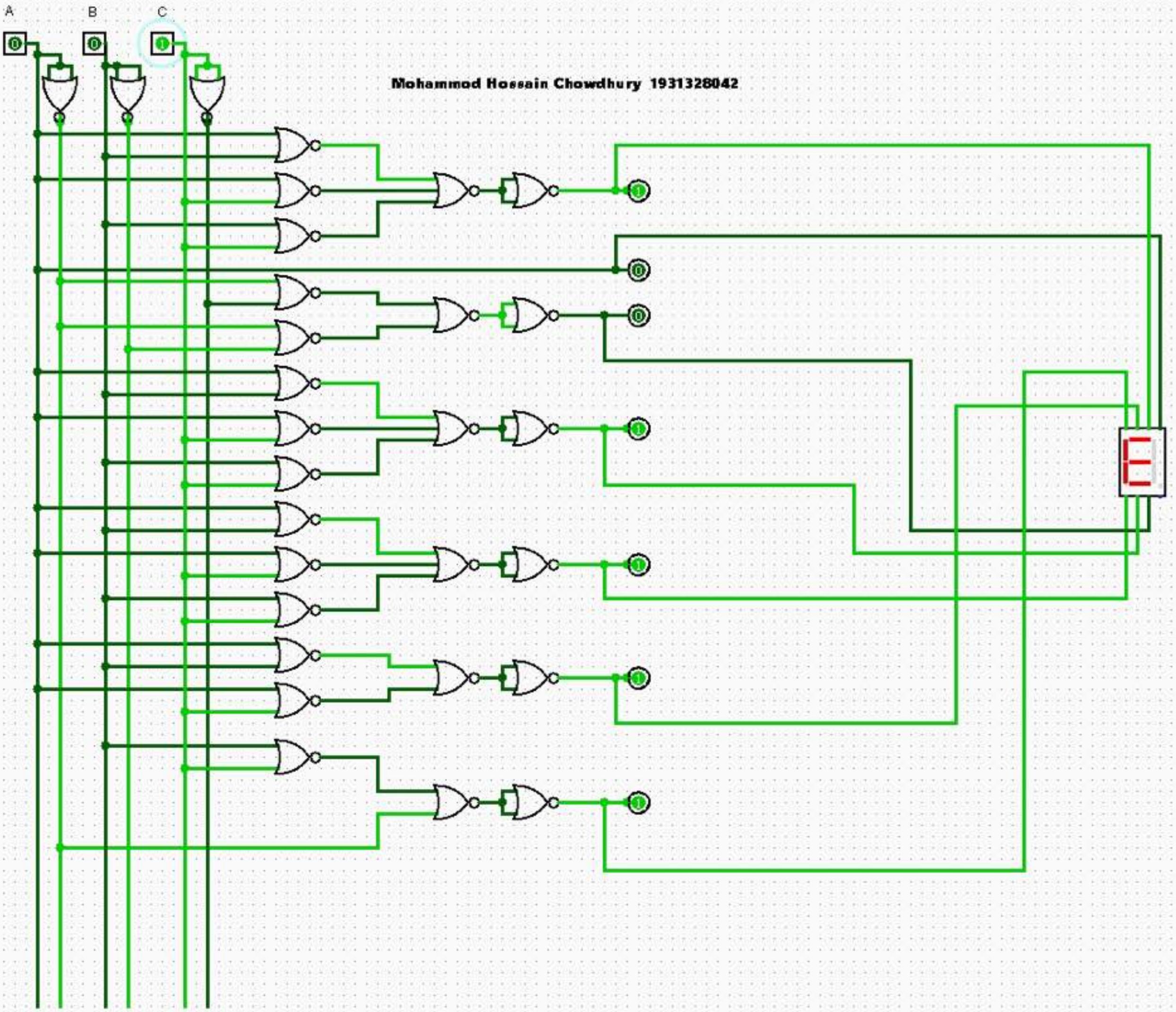
MOHAMMAD HOSSAIN
CHOWDHURY
1931328042

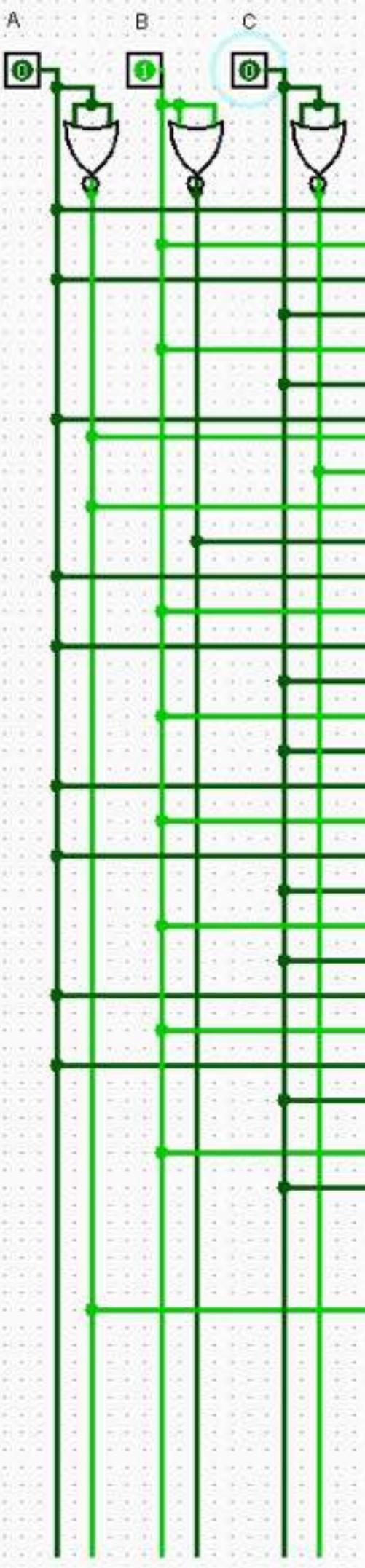


A B C

Mohammed Hossain Chowdhury 1931328042

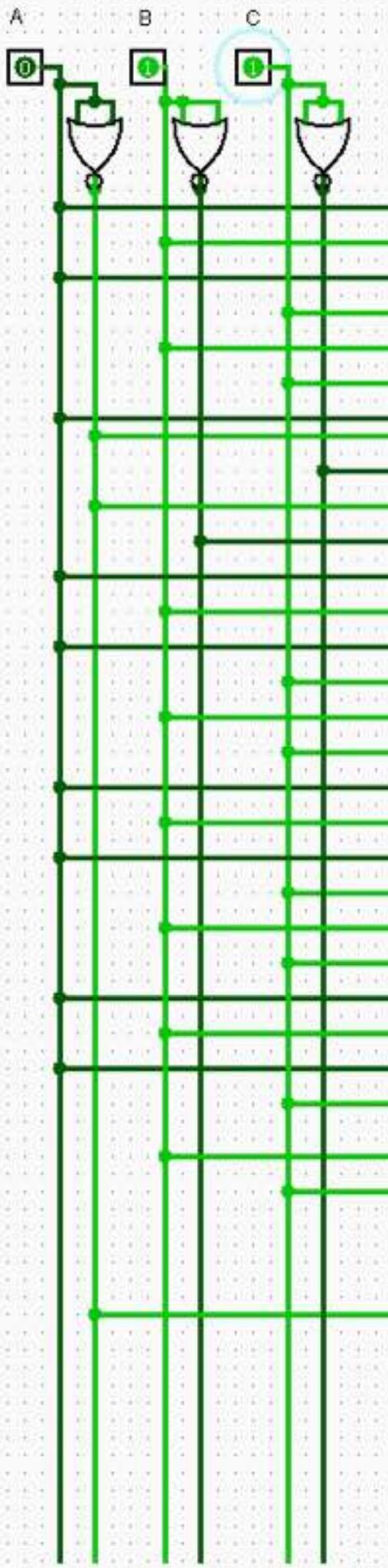






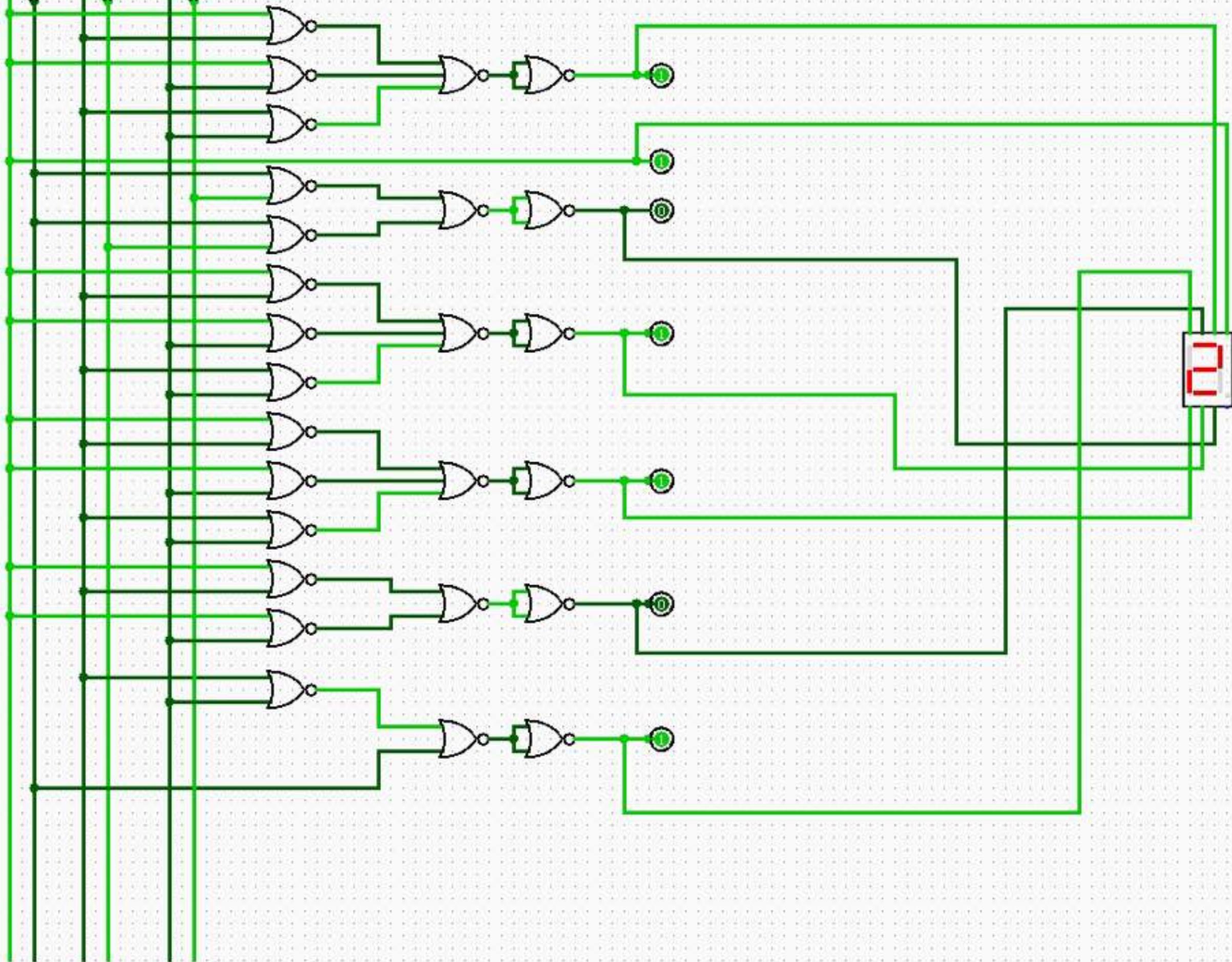
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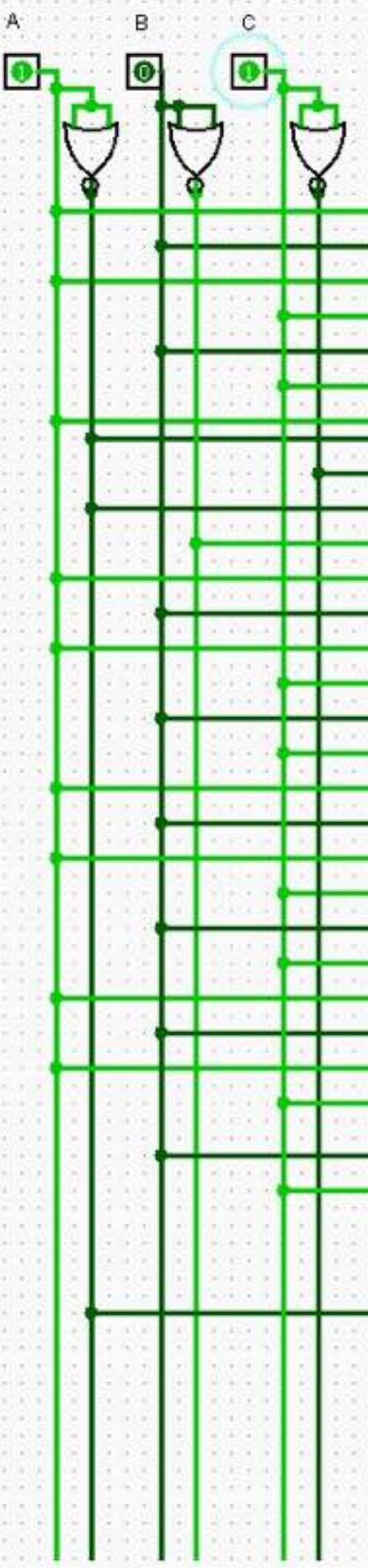
E

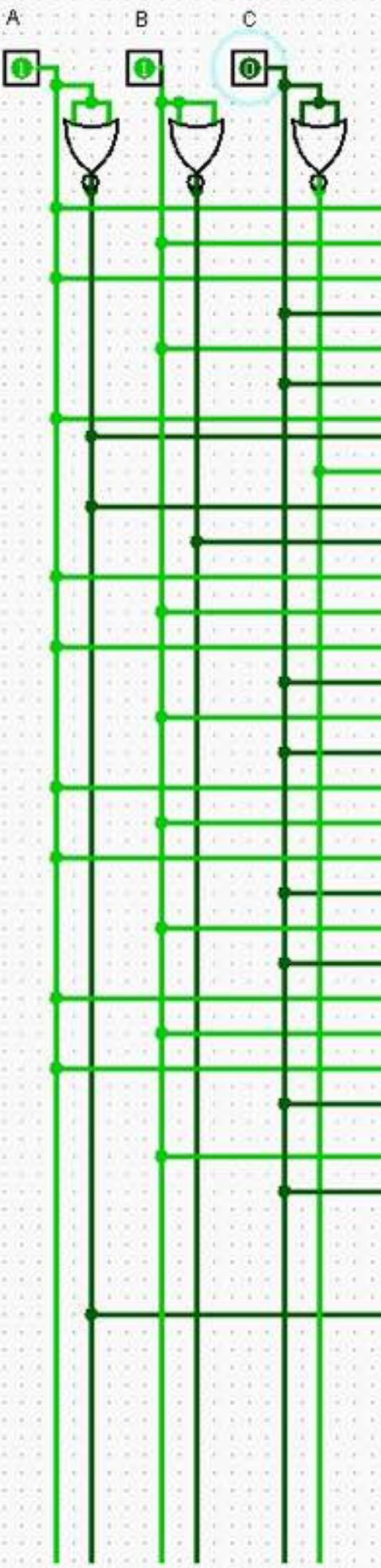


A diagram illustrating a network or sequence of three nodes labeled A, B, and C. Node A is on the left, node B is in the middle, and node C is on the right. They are interconnected by a series of green line segments forming a zigzag pattern. Specifically, node A connects to node B, which then connects to node C.

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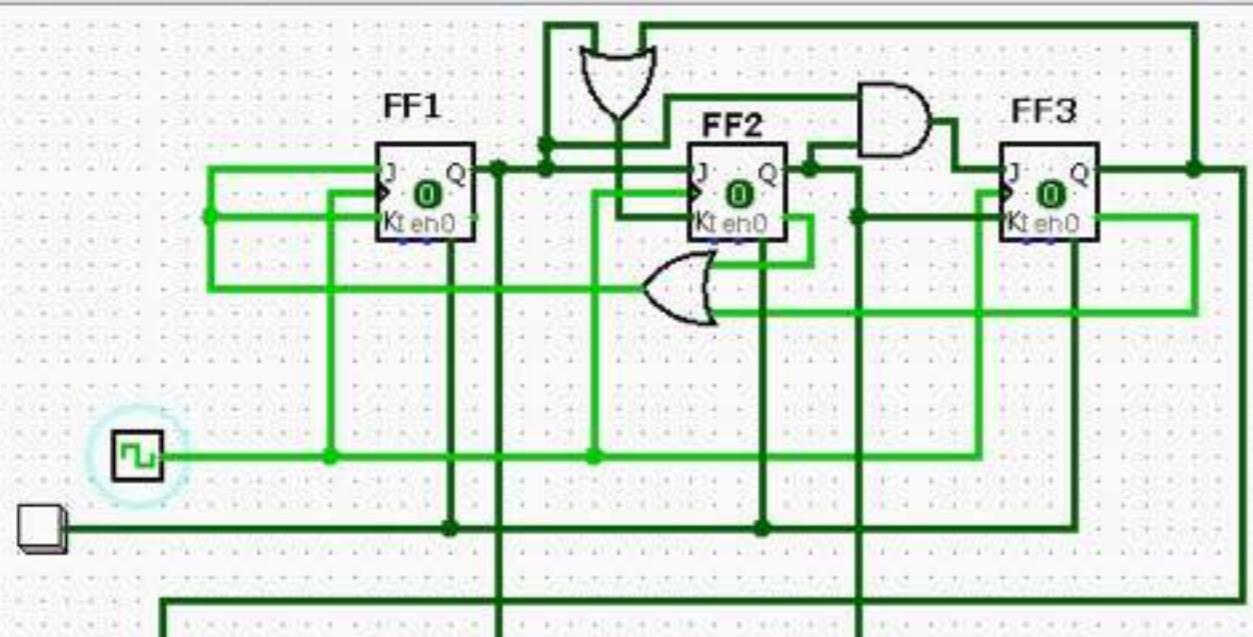




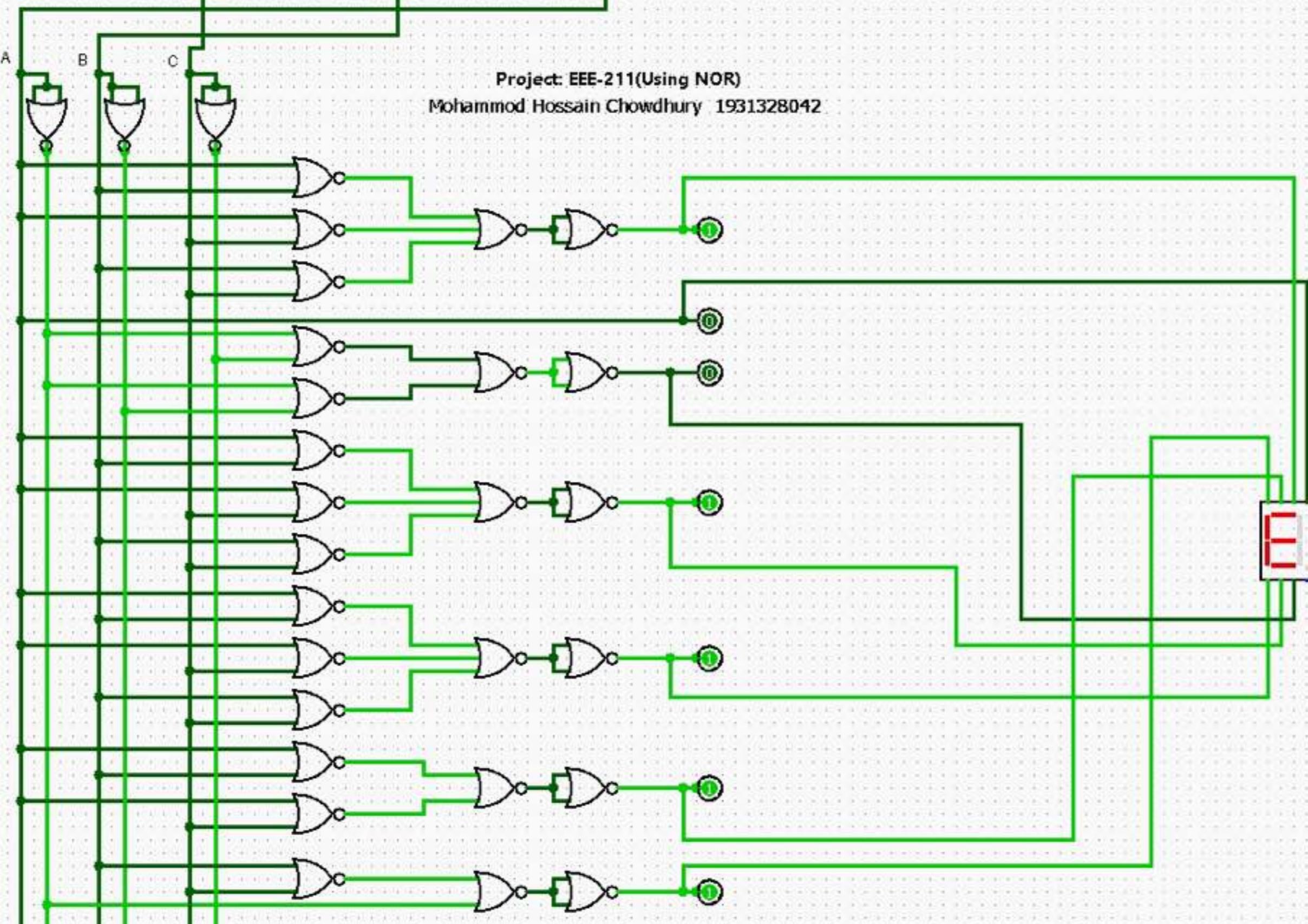


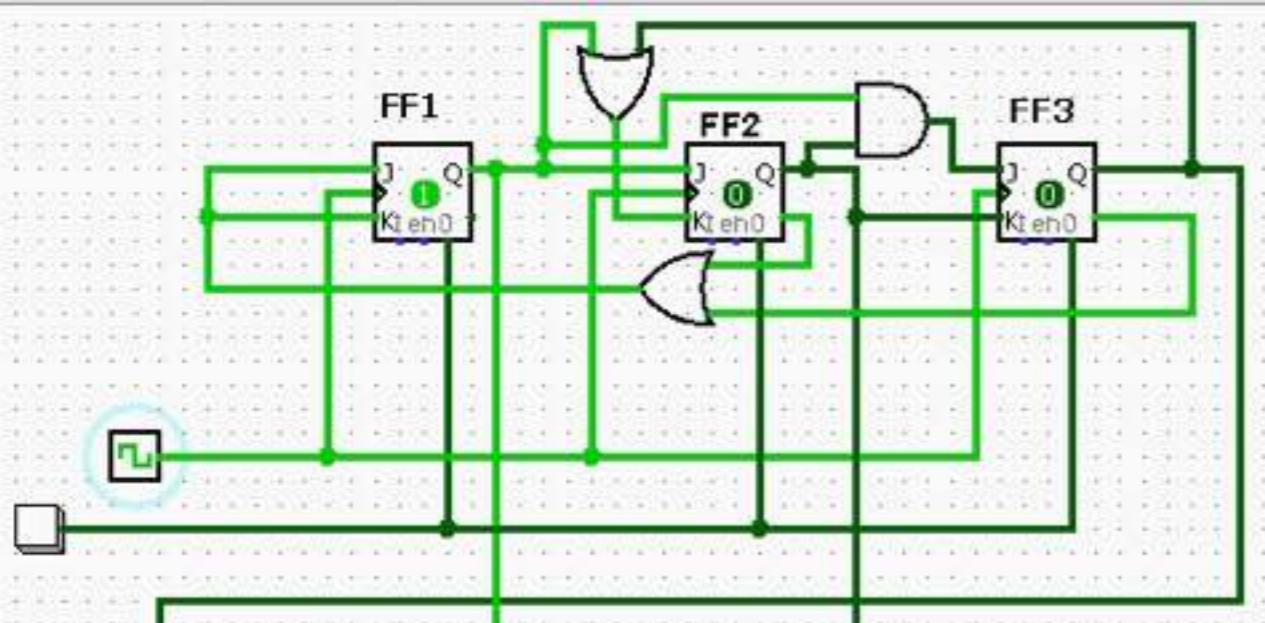
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Sequential circuit using NOR



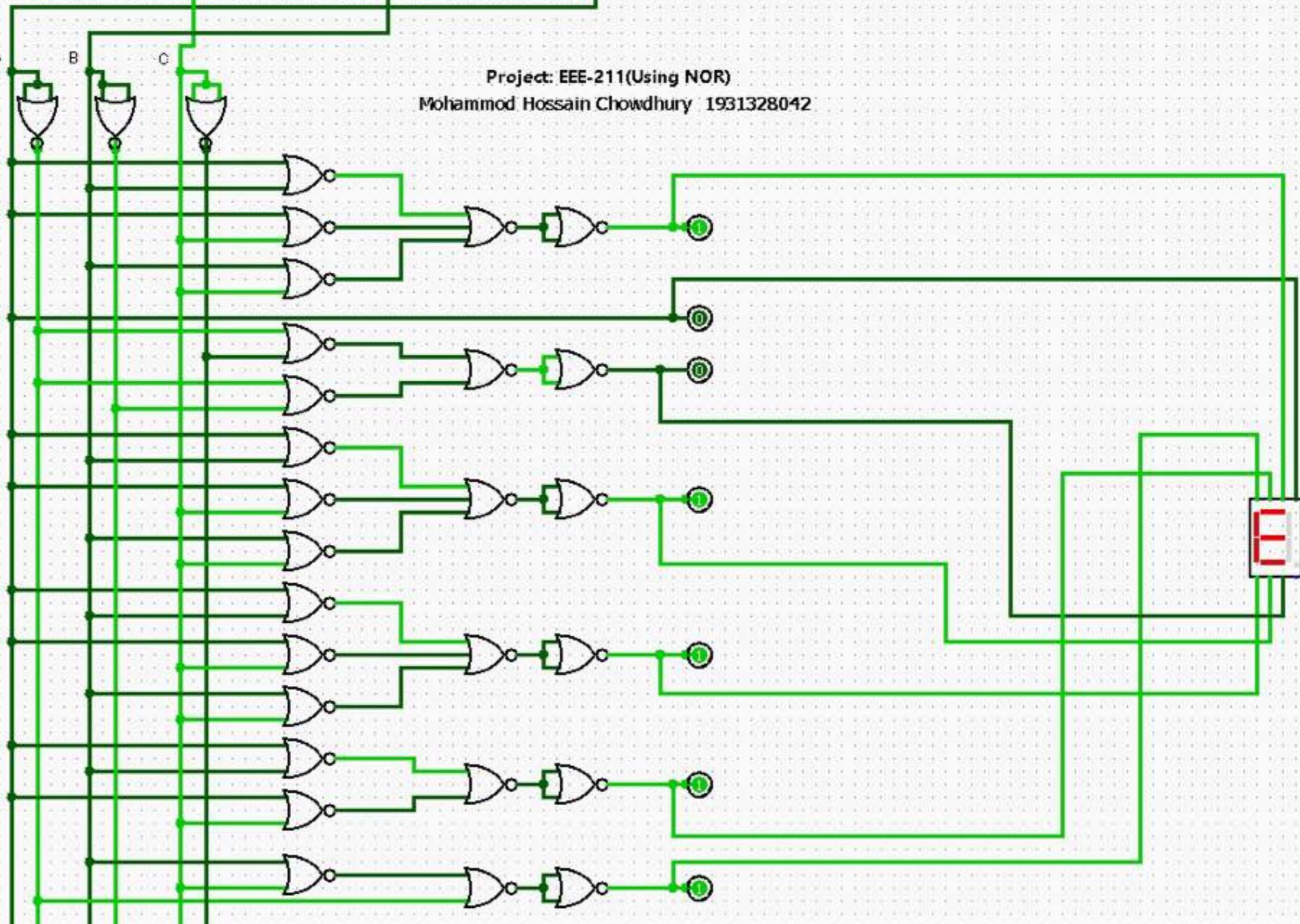
Project: EEE-211(Using NOR)
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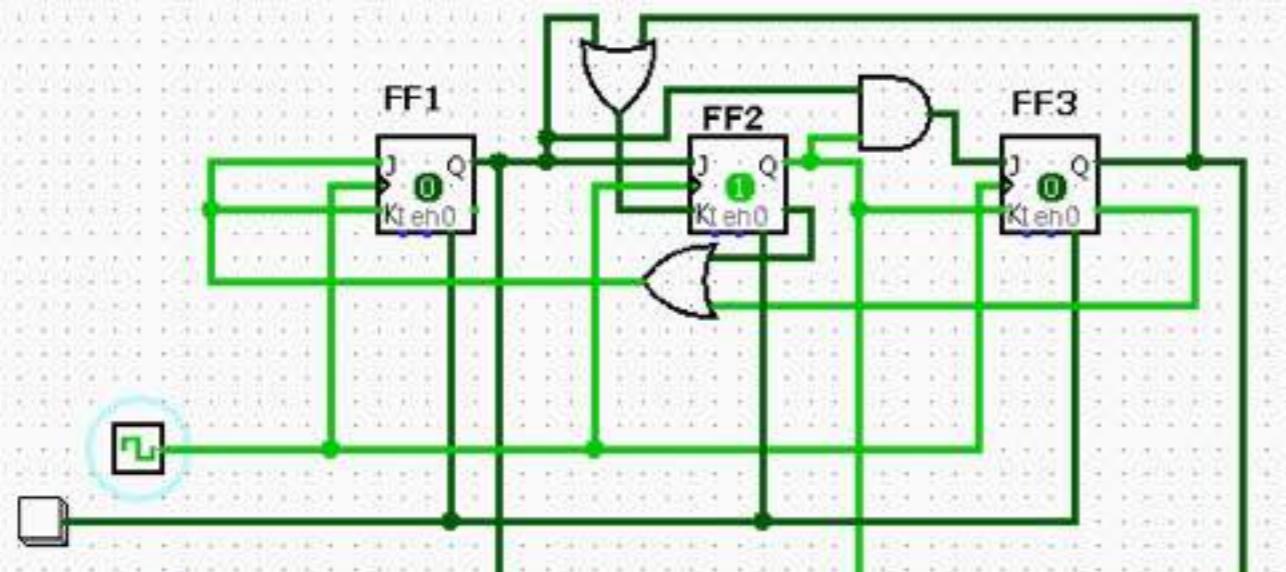




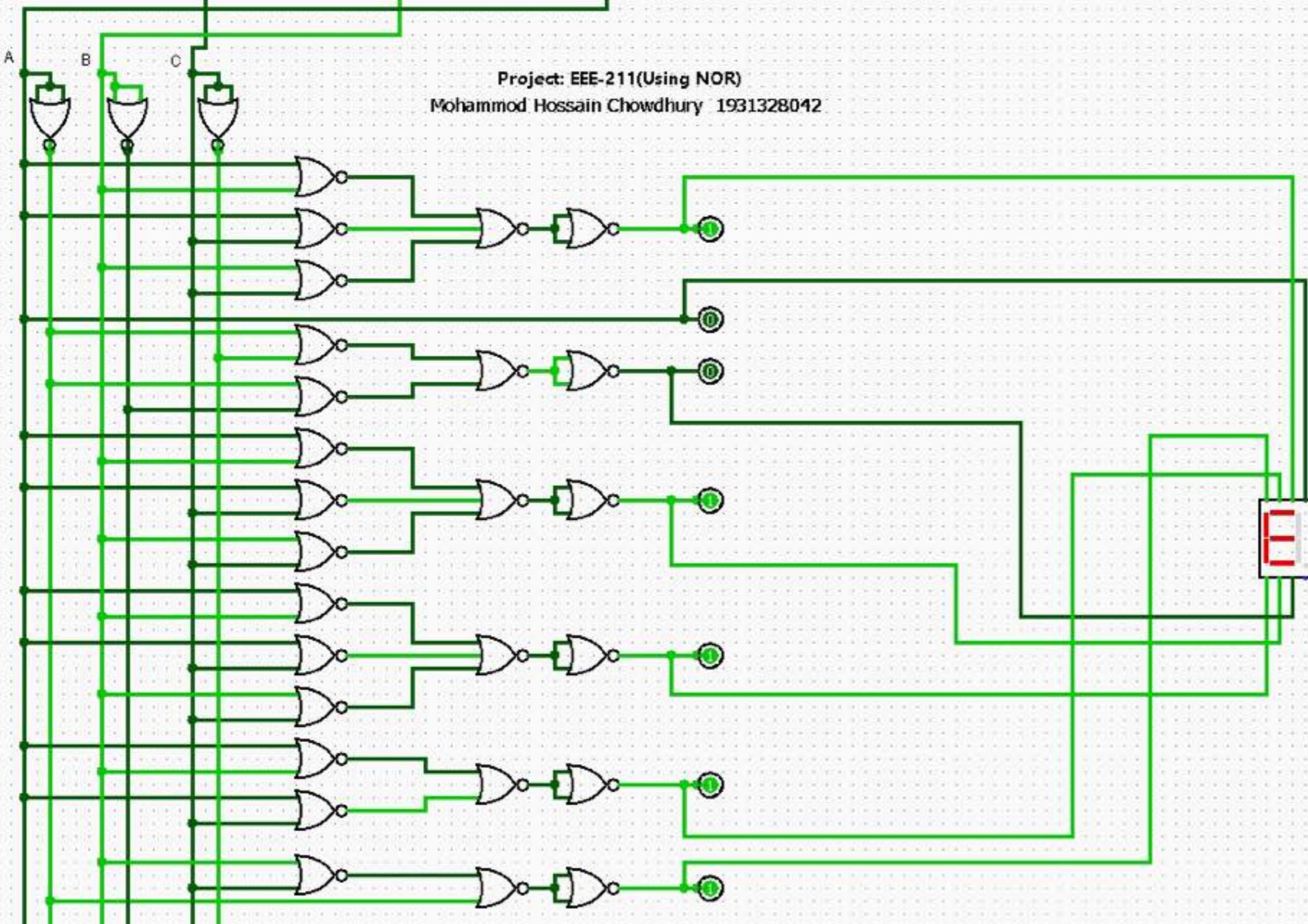
Project: EEE-211(Using NOR)

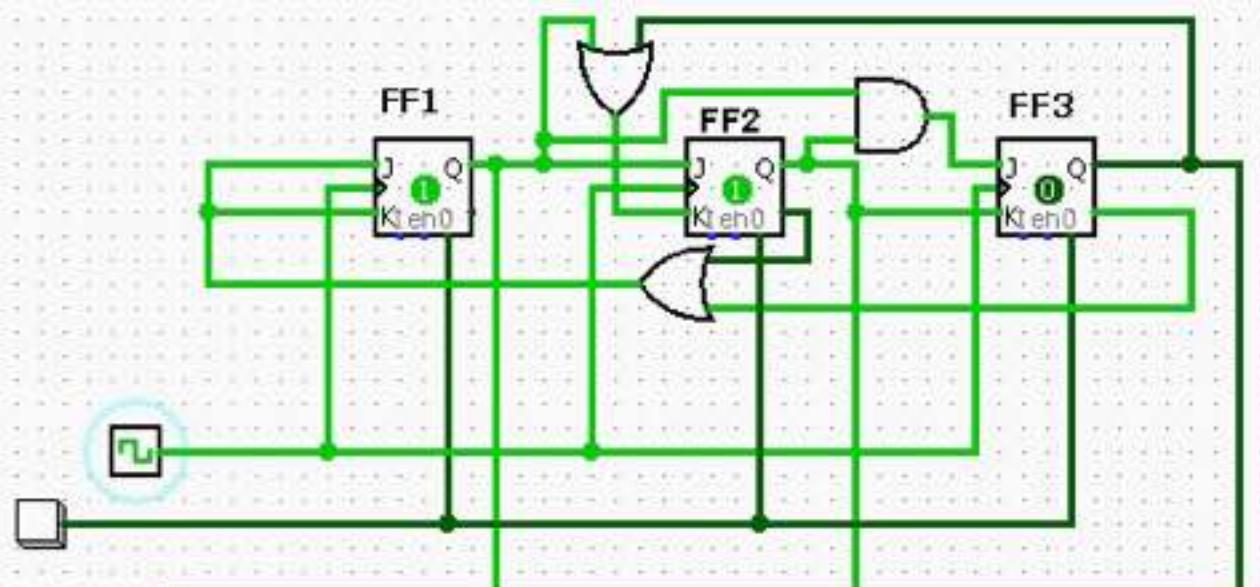
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