Fall 2021 EEE/ETE 141L

Electrical Circuits-I Lab(Sec-5)

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Lab No.: 03

Date of Performance: 17.11.2021

Date of Submission : 24.11.2021

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Experiment Name: Loading Effect of Voltage Divider Circuit

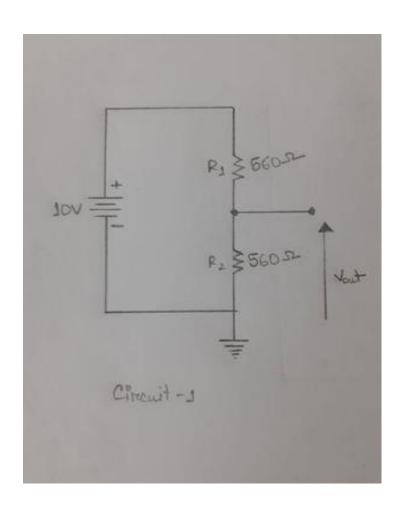
Objective:

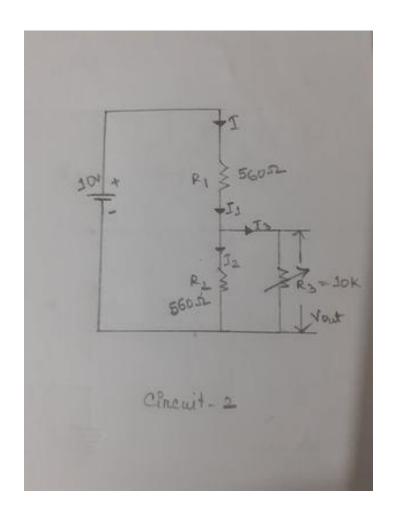
- We have to analyze how the voltage divider circuit behaves when there is no load resistance connected.
- We have to evaluate the performance of voltage divider circuit due to loading.

List of Equipment:

- Trainer Board
- DMM
- $2 \times 560\Omega$ resistors
- $1 \times (0-10k\Omega)$ variable resistor
- Multisim

Circuit Diagram:





Data Table:

Table 1:

RL	Vout (Measured)	Vout (Calculated)	%Error
No resistor	5V	5V	0%
1k	3.906V	3.91V	0.102%
4k	4.673V	4.67V	0.064%
7k	4.808V	4.81V	0.0416%
10k	4.864V	4.86V	0.082%

Results:

% Error = (Theoretical value – Experimental Value) / Theoretical Value

For no register:

$$RT = R1+R2 = (560+560) Ohm = 1120 Ohm$$

 $I = 10/1120 = 8.92mA$
 $Vout = 5V$

For 1k register:

For 4k register:

$$RT = R1 + (R2||R3) = 560 + ((1/560) + (1/4000)) \text{ Ohm} = (560 + 491) \text{ Ohm}$$

$$= 1051 \text{ Ohm}$$

$$I = 10/1051 = 9.51 \text{ mA}$$

$$Vout = 4.67V$$

$$\% Error = (|(4.67 - 4.673)|/4.67) * 100\% = 0.064\%$$

For 7k register:

$$RT = R1 + (R2||R3) = 560 + ((1/560) + (1/7000)) \ Ohm = (560 + 518) \ Ohm \\ = 1078Ohm \\ I = 10/1078 = 9.27mA \\ Vout = 4.81V \\ \%Error = (|(4.81 - 4.808)|/4.81) * 100\% = 0.0416\%$$

For 10k register:

$$RT = R1 + (R2||R3) = 560 + ((1/560) + (1/10000)) \text{ Ohm} = (560 + 530) \text{ Ohm}$$

$$= 1090 \text{ Ohm}$$

$$I = 10/1090 = 9.2 \text{mA}$$

$$Vout = 4.86 \text{V}$$

$$\% \text{ Error} = (|(4.86 - 4.864)|/4.86) * 100\% = 0.082\%$$

Question/Answer:

1. Explain the loading effect of your circuit (i.e explain how does your Vout vary with increasing Load resistor)

Answer:

Initially the Vout was 5V, total resistance was 11200hm and the current flow was 8.92mA, when there was no load register.

After adding load register the total resistance decreases so the current flow Increases.

As the Value of the load register is increasing the value of Vout is also increasing.

From the table when Load Resistor is 1k the Vout is 3.91 and finally when the Load Resistor is 10k the Vout is 4.86.

2. Showing all steps in details, theoretically calculate the value of Vout for each load resistor.

Answer:

For no register:

$$RT = R1+R2 = (560+560) \text{ Ohm} = 1120 \text{ Ohm}$$

 $I = 10/1120 = 8.92\text{mA}$
 $Vout = (Vin*(R2||R3))/(R1+(R2||R3)) = (10*560)/1120 \text{ V} = 5\text{V}$

For 1k register:

$$RT = R1 + (R2||R3) = 560 + ((1/560) + (1/1000)) \text{ Ohm} = (560 + 358.97) \text{ Ohm}$$

$$= 918.97 \text{ Ohm}$$

$$I = 10/918.97 = 10.88 \text{mA}$$

$$Vout = (Vin*(R2||R3))/(R1 + (R2||R3)) = (10*358.97)/918.97 \text{ V} = 3.91 \text{ V}$$

For 4k register:

$$RT = R1 + (R2||R3) = 560 + ((1/560) + (1/4000)) Ohm = (560 + 491) Ohm = 1051Ohm$$

$$I = 10/1051 = 9.51 \text{mA}$$

 $Vout = (Vin*(R2||R3))/(R1+(R2||R3)) = (10*491)/1051 \text{ V} = 4.67 \text{V}$

For 7k register:

$$RT = R1 + (R2||R3) = 560 + ((1/560) + (1/7000)) \ Ohm = (560 + 518) \ Ohm$$

$$= 1078 Ohm$$

$$I = 10/1078 = 9.27 mA$$

$$Vout = (Vin*(R2||R3))/(R1 + (R2||R3)) = (10*518)/1078 = 4.81 V$$

For 10k register:

$$RT = R1 + (R2||R3) = 560 + ((1/560) + (1/10000)) \text{ Ohm} = (560 + 530) \text{ Ohm}$$

$$= 1090 \text{Ohm}$$

$$I = 10/1090 = 9.2 \text{mA}$$

$$Vout = (Vin*(R2||R3))/(R1 + (R2||R3)) = (10*530)/1090 = 4.86 \text{V}$$

3. Comparing the theoretical data to the experimental data, comment how far the loading effect of your circuit supports the theory.

Answer:

According to the Data table, Our Percentage error for,

1k is 0.102%

4K is 0.064%

7k is 0.0416%

10k is 0.082%

Therefore, from all these percentages, errors are minimal percentage errors we can clearly said that, our loading effect supports the theory.

Discussion:

From the lab 3, we learned about Voltage divider circuit and Loading effect.

As, it was an online lab, we had to use multisim to do the experiments. So, we didn't have to face many errors or faults. We could find the theoretical values easily.

If we would have done the lab offline, we could have faced many errors such human errors, environmental errors or mechanical errors. Also, we could have faces errors using DMM, cables, breadboard connection etc.