CSE231
SEC: 06

Project

Seven-Segment Display
on
BABAFAFA
2nd Part
555 timer & sequential circuit

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About 555 timer:-

The 555 is a single-chip version of a commonly used circuit called a multivibrator, which is useful in a wide variety of electronic circuits. The 555 timer chips probably the most popular integrated circuit ever made.

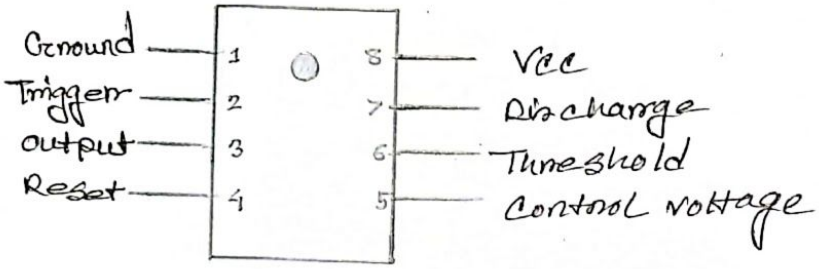

Figure: A 555-timer chip

The 555-timer is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the timer is precisely controlled by one external resistor and capacitor.

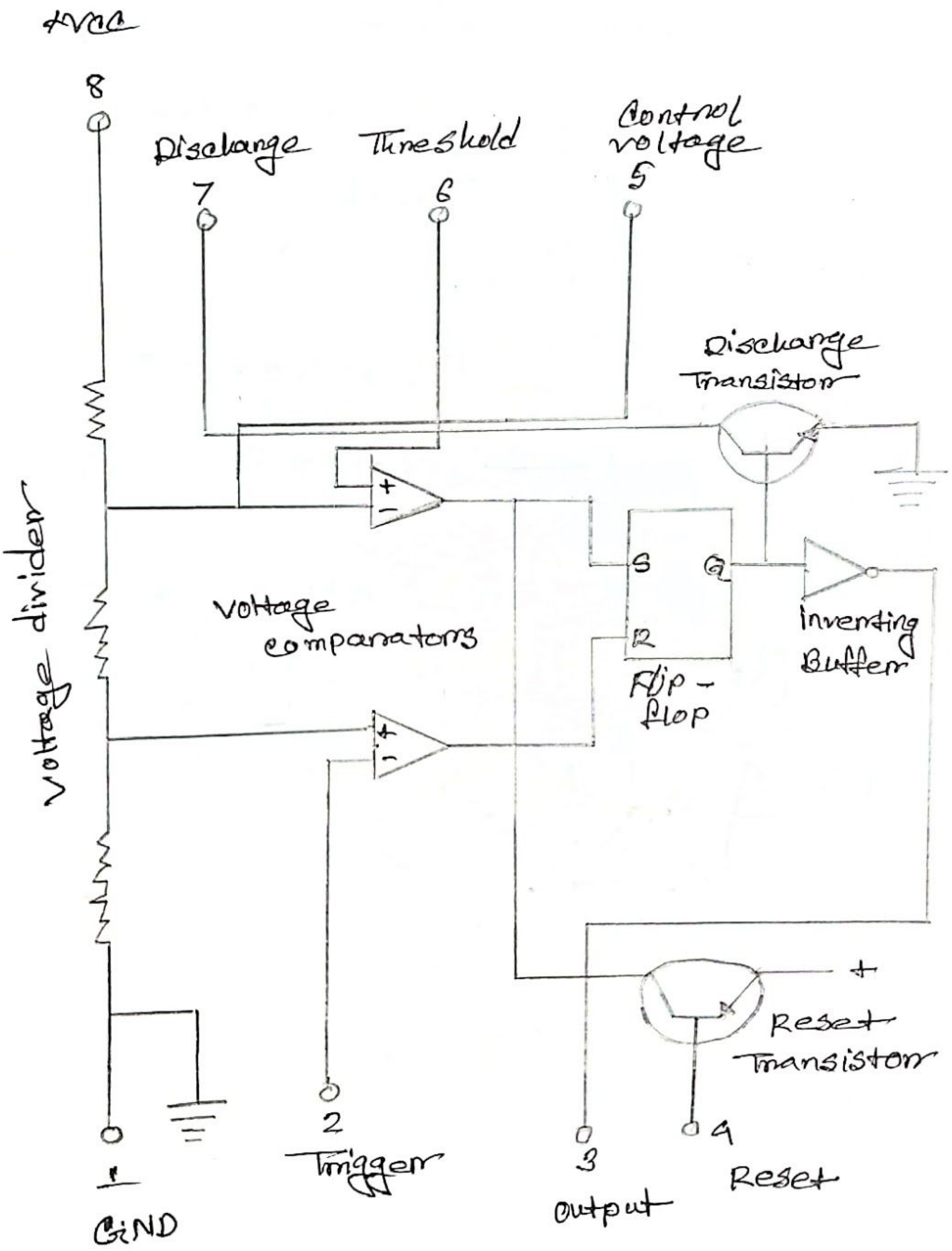

Figure: Internal Construction Of 555 Timer

How all 8 pins are working:—

Pin 1 : In the grounded terminal all the voltages are mesured with respect to this terminal.

Pin 2 : Trigger terminal is an inverting input to a comparator that is responsible for transition of flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.

Pin 3 : Output of the timer is available at this pin. There are two ways in which a load can be connected to the output terminal either between pin 3 and ground pin (1) or between pin 3 and supply pin (8).

Pin-4 : (Reset terminal) To disable or reset the timer a negative pulse is applied to this pin due to the fact it is referred to as reset terminal. When this pin is not to be used for reset purpose, it should be connected to $+V_{cc}$ to avoid any possibility of false triggering.

Pin-5 : (Control voltage) The function of this terminal is to control the threshold and trigger levels. Thus either the external voltage or a pot connected to this pin determines the pulse width of the output waveform.

Pin-6 : Threshold terminal is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of $2/3\ V_{cc}$. The amplitude

of voltage applied to this terminal is responsible for the set state of flip-flop.

Pin-7 : Discharge Terminal is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharge through the transistor.

Pin-8 : It is a supply terminal. A supply voltage of +5V to +18 V is applied to this terminal with respect to the ground. (pin 1)

Asynchronous & Synchronous circuit :—

Sequential circuit is one of the major catagories of digital logic circuits. Based on the clock input, it is further classified into synchronous and asychronous circuits.

Synchronous sequential circuit : This circuits are digital circuits governed by clock signals. The transition from one state to another state takes place only by the application of specified clock signals, even if the input changes. Clocked flip-flops are used as memory elements in synchronous sequential circuits. The state of synchronous sequential circuits are always predictable and thus reliable. Also it is easy to design synchronous sequential circuits.

But synchronous sequential circuits are slower in its operation speed. This is due to the propagation delay of clock signal in reaching all elements of the circuit. The distributed clock signal consums large power and dissipates large amount of heat.

Asynchronous sequential circuit: This circuits are digital circuits that are not driven by clock. They can be called as self-timed circuit. The transition from one state to another takes places immediately once the inputs change. There are chances for the asynchronous circuit to enter into a wrong state because of the time difference between the arrivals of inputs. It is hard to make a asynchronous circuit but it is less power-hungry than synchronous and

also they are comparatively faster than Synchronous circuits.
For,
All of these reasons we are going to build our sequential circuit using the asynchronous circuit.

Table :

clock Pulse	Q_2	Q_1	Q_0	Display	a	b	c	d	e	f	g
Initially	0	0	0	8	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1
2	0	1	0	8	1	1	1	1	1	1	1
3	0	1	1	1	1	1	1	0	1	1	1
4	1	0	0	F	1	0	0	0	1	1	1
5	1	0	1	1	1	1	1	0	1	1	1
6	1	1	0	F	1	0	0	0	1	1	1
7	1	1	1	1	1	1	1	0	1	1	1
8	0	0	0	x	x	x	x	x	x	x	x

Figure: Table

$B \rightarrow \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}$

$A \rightarrow \overline{Q_0}\ \overline{Q_1}\ Q_2$

$B \rightarrow \overline{Q_0}\ Q_1\ \overline{Q_2}$

$A \rightarrow \overline{Q_0}\ Q_1\ Q_2$

$F \rightarrow Q_0\ \overline{Q_1}\ \overline{Q_2}$

$A \rightarrow Q_0\ \overline{Q_1}\ Q_2$

$f \rightarrow Q_0\ Q_1\ \overline{Q_2}$

$A \rightarrow Q_0\ Q_1\ Q_2$

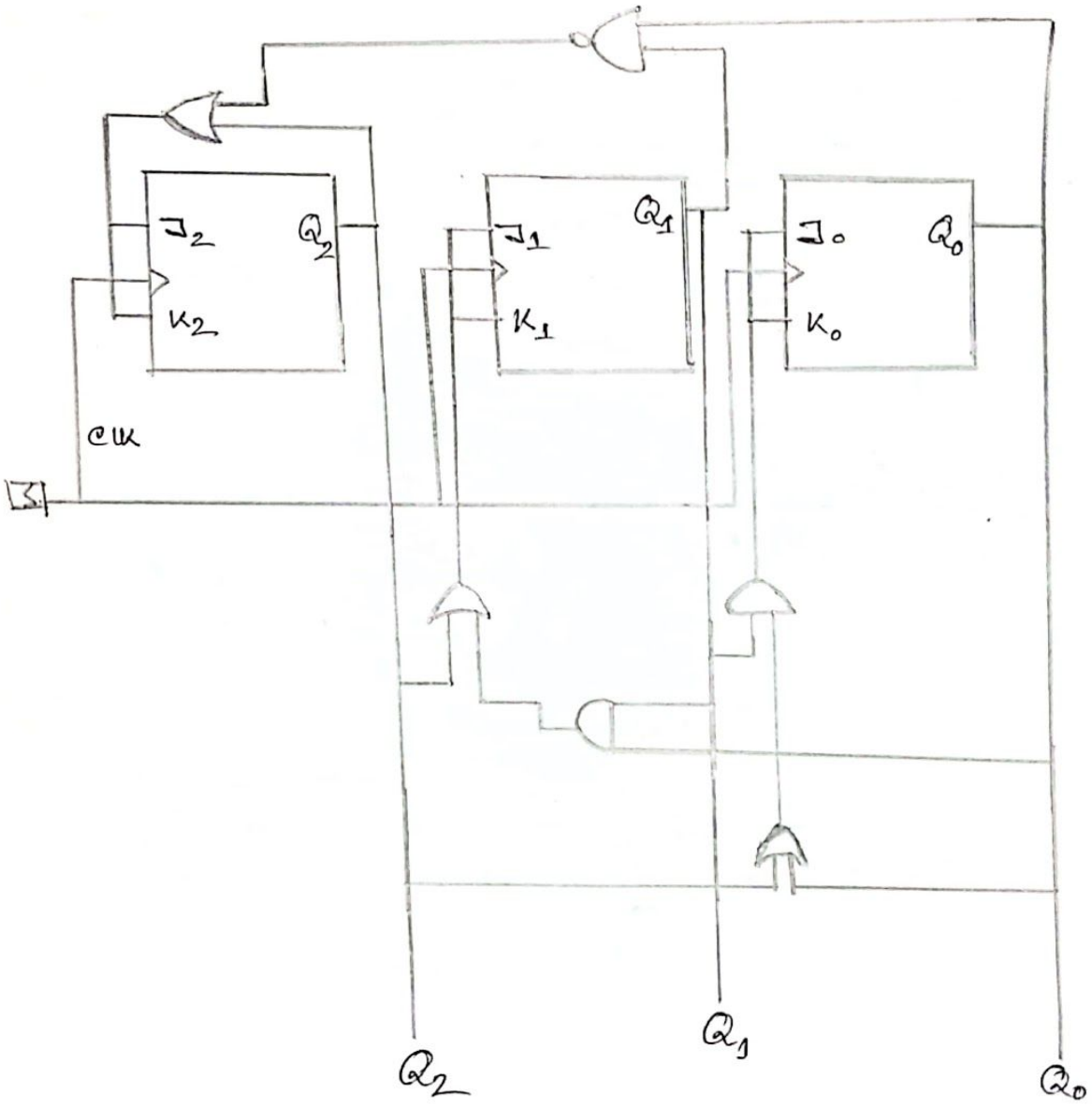

Figure: Sequential circuit Diagram

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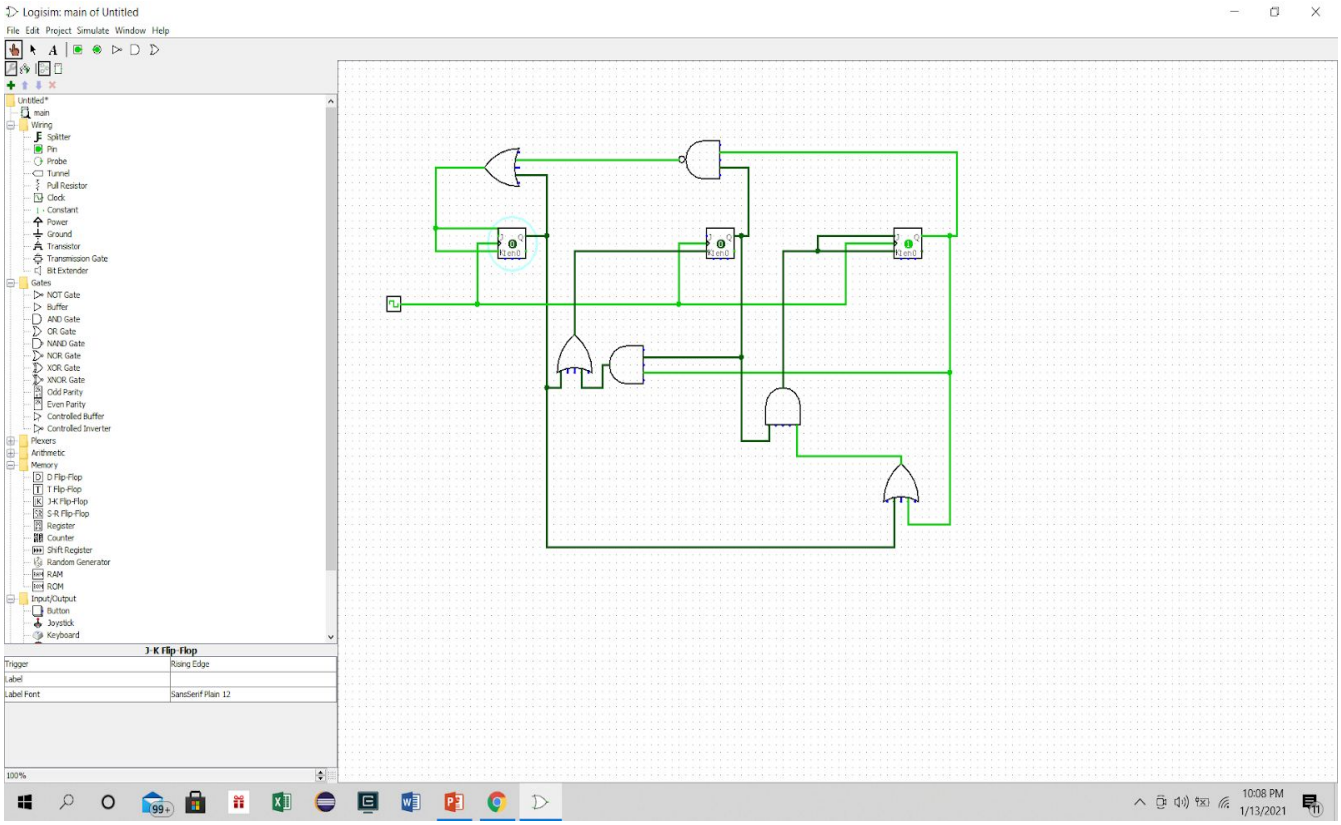
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J-K Flip-Flop
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