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North South University

Department of Electrical and Computer Engineering

Final Exam, Spring 2019

Semiconductor Devices Technology (EEE 313.01/ETE 411.01/EEE 410.01/ETE 443.01)

Time: 70 minutes | Full marks: 30

<u>There are three questions. Attempt answers to all. Individual marks are indicated at the right margin.</u>

1 (a) How built-in voltage V_{bi} is related to diode on current? If V_{bi} of a diode is higher or lower, how does it impact the magnitude of diode on current?

(b) A silicon pn junction at T = 300 K has the following parameters: $N_A = 4\times10^{15}$ cm^{-3}, $N_D = 7\times10^{16}$ cm^{-3}, $D_n = 25$ cm^2/s, $D_p = 15$ cm^2/s, $\tau_{n0} = 7.9\times10^{-7}$ s and $\tau_{p0} = 3.8\times10^{-7}$ s. The cross sectional area is $A = 4\times10^{-4}$ cm^2 and the forward bias voltage is $V_a = 0.6$ V. Calculate the total current I_{diode} (A) in the p-n junction diode. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}.

[4+6=10]

Useful equations:

$$J_{Diode} = q\left(\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right)\left(exp^{\left(\frac{V_a}{V_T}\right)} - 1\right) \quad (A/cm^2) \qquad L_p^2 = D_p \tau_{p0}$$

$$L_n^2 = D_n \tau_{n0} \qquad V_T = \frac{kT}{q} \qquad V_{bi} = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right)$$

2. (a) At flat band voltage V_{FB}, is the surface band bending $\psi_s = 0$ or <0 or >0. Explain.

(b) How can you achieve a low enhancement mode $V_T > 0$ for an n-MOS capacitor ? (Hint: write the V_T equation and identify the parameters that affect V_T).

(c) For a n-MOS silicon capacitor, at T = 300 K, the substrate doping is $N_A = 3.2\times 10^{16}/cm^3$.

(i) What is bulk potential, φ_B ?

(ii) At inversion condition what is ψ_s? (Hint: φ_s is total band bending at the surface).

(iii) For $\varphi_m = 4.45$ eV and $\chi = 4.01$ eV (for silicon), what is the flatband voltage $V_{FB} = \varphi_{ms}$?

(iv) Find the maximum depletion width x_{dT} (μm) at the inversion condition of the surface. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}.

[2+2+1.5 x4=10]

Useful equations:

$$x_{dT} = \left(\frac{2\varepsilon_s \psi_s}{qN_A}\right)^{1/2} \qquad \varepsilon_s = 11.7\,\varepsilon_0 \qquad \varphi_B = \frac{kT}{q} ln\left(\frac{N_A}{n_i}\right)$$

3. (a) Suppose for a n-channel MOSFET, drain current at a particular V_T is in the linear mode operation. Consider two cases: (i) high V_{gs}, low V_{ds} and (ii) high V_{gs}, high V_{ds} ? Which case will produce higher value of drain current? Explain. (Hint: use the MOSFET drain current equation for linear mode).

(b) An ideal n-channel MOSFET has the following parameters: $V_T = 0.42$ V, $\mu_n = 730$ $cm^2/V\text{-}s$, $t_{ox} = 10.4$ nm, W = 11 μm and L = 1.2 μm. Find the drain current I_{ds} for this MOSFET when

[3+2+2.5x2 =10]

(i) $V_{gs} = 0.25$ V and $V_{ds} = 0.15$ V.

(ii) $V_{gs} = 1.6$ V and $V_{ds} = 0.4$ V.

(iii) $V_{gs} = 1.8$ V and $V_{ds} = 2.4$ V.

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Department of Electrical and Computer Engineering

Final Exam, Spring 2019

Semiconductor Devices Technology (EEE 313.02/ETE 411.02/EEE 410.02/ETE 443.02)

Time: 70 minutes Full marks: 30

There are three questions. Attempt answers to all. Individual marks are indicated at the right margin.

1 (a) Using the diode current equation, show that for a p-n junction diode, electron current density is enhanced if p-side doping is lower than n-side doping. Explain. Why D_n is higher than D_p ?

(b) A silicon pn junction at T = 300 K has the following parameters: $N_A = 5\times10^{15}$ cm^{-3}, $N_D = 7.5\times10^{16}$ cm^{-3}, $D_n = 24$ cm^2/s, $D_p = 14$ cm^2/s, $\tau_{n0} = 7.8\times10^{-7}$ s and $\tau_{p0} = 3.7\times10^{-7}$ s. The cross sectional area is A = 4.5×10^{-3} cm^2 **and the forward bias voltage is V_a = 0.6 V. Calculate the total current I_{diode} (A)** in the p-n junction diode. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}.

[4+6=10]

Useful equations:

$$J_{Diode} = q\left(\frac{D_p p_{n0}}{L_p} + \frac{D_n n_{p0}}{L_n}\right)\left(exp^{\left(\frac{V_a}{V_T}\right)} - 1\right) \text{ (A/cm}^2\text{)} \quad L_p^2 = D_p\tau_{p0}$$

$$L_n^2 = D_n\tau_{n0} \qquad V_T = \frac{kT}{q} \qquad V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

2. (a) If at the threshold of inversion, electron concentration at the surface is $n_s = N_A$ which is at the bulk for n-MOS capacitor, then at (i) depletion and (ii) moderate inversion, comment whether $n_s > N_A$ or $n_s < N_A$.

(b) How can you achieve a low depletion mode $V_T < 0$ for an n-MOS capacitor ? (Hint: write the V_T equation and identify the parameters that affect V_T).

(c) For a n-MOS silicon capacitor, at T = 300 K, the substrate doping is $N_A = 3.5\times 10^{16}$/cm^3.

(i) What is bulk potential, φ_B ?

(ii) At inversion condition what is ψ_s? (Hint: φ_s is total band bending at the surface).

(iii) For $\varphi_m = 4.49$ eV and $\chi = 4.01$ eV (for silicon), what is the flatband voltage $V_{FB} = \varphi_{ms}$?

(iv) Find the maximum depletion width x_{dT} (μm) at the inversion condition of the surface. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}.

[2+2+1.5 x4=10]

Useful equations:

$$x_{dT} = \left(\frac{2\varepsilon_s\psi_s}{qN_A}\right)^{1/2} \qquad \varepsilon_s = 11.7\,\varepsilon_0 \qquad \varphi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

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3. (a) Suppose for a n-channel MOSFET, drain current at a particular V_T is in the saturation mode of operation. Consider two cases: (i) high V_{ds} (sat) and (ii) low V_{ds} (sat). Comment whether drain current for case (i) is higher or lower than case (ii). Explain. (Hint: use the MOSFET drain current equation for saturation mode).

(b) An ideal n-channel MOSFET has the following parameters: $V_T = 0.44$ V, $\mu_n = 725$ cm^2/V-s, $t_{ox} = 10.7$ nm, W= 11.3 μm and L = 1.3 μm. Find the drain current I_{ds} for this MOSFET when

(i) $V_{gs} = 0.22$ V and $V_{ds} = 0.14$ V.

[3+2+2.5x2 =10]

(ii) $V_{gs} = 1.4$ V and $V_{ds} = 0.45$ V.
(iii) $V_{gs} = 1.75$ V and $V_{ds} = 2.4$ V.

Make sure to apply the above bias conditions to determine cut-off, linear case and saturation case for calculation of drain current.

Useful equations:

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}\left\{(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}\right\}$$

$$I_{ds} = \mu_n C_{ox} \frac{W}{L} \frac{(V_{gs} - V_T)^2}{2}$$

North South University

Department of Electrical and Computer Engineering

Final Exam, Summer 2017

Semiconductor Devices Technology (EEE 313.01/ETE 411.01/EEE 410.01/ETE 443.01) *Full marks: 30*

Time: 70 minutes

<u>There are three questions. Attempt answers to all. Individual marks are indicated at the right margin.</u>

1. A silicon pn junction at T = 300 K has the following parameters: $N_A = 5\times10^{16}$ cm^{-3}, $N_D = 3\times10^{17}$ cm^{-3}, $D_n = 22$ cm^2/s, $D_p = 15$ cm^2/s, $\tau_{n0} = 5.5\times10^{-7}$ s and $\tau_{p0} = 2.2\times10^{-7}$ s. The cross sectional area is $A = 3\times10^{-4}$ cm^2 and the forward bias voltage is $V_a = 0.69$ V. Calculate the total current I_{diode} (A) in the p-n junction diode. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}. [10]

Useful equations:

$$J_{D\,Total} = q\left(\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right)\left(exp^{\left(\frac{V_a}{V_T}\right)} - 1\right) \text{ (A/cm}^2\text{)} \qquad L_p^2 = D_p\tau_{po}$$

$$L_n^2 = D_n\tau_{n0} \qquad V_T = \frac{kT}{q}$$

2. For a p-substrate silicon MOS capacitor, at T = 300 K, the substrate doping is $N_A = 7\times10^{16}$/cm^3.

(a) What is bulk potential, φ_B ?

(b) At inversion condition what is φ_s? (Hint: φ_s is total band bending at the surface).

(c) For $\varphi_m = 4.28$ eV and $\chi = 4.01$ eV (for silicon), what is the flatband voltage $V_{FB} = \varphi_{ms}$?

(d) Find the maximum depletion width x_{dT} (μm) at the inversion condition of the surface. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}. [5×2=10]

Useful equations:

$$x_{dT} = \left(\frac{2\varepsilon_s\varphi_s}{qN_A}\right)^{1/2} \qquad \varepsilon_s = 11.7\,\varepsilon_o \qquad \varphi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

3. An ideal n-channel MOSFET has the following parameters: $V_T = 0.42$ V, $\mu_n = 560$ cm^2/V-s, $t_{ox} = 10$ nm, W= 10 μm and L = 0.8 μm. Find the drain current I_{ds} for this MOSFET when

(a) $V_{gs} = 0.9$ V and $V_{ds} = 0.2$ V. [3.5]

(b) $V_{gs} = 1.6$ V and $V_{ds} = 1.5$ V. [3.5]

(c) $V_{gs} = 0.1$ V and $V_{ds} = 0.2$ V. [3.0]

Make sure to apply the above bias conditions to determine cut-off, linear case and saturation case for calculation of drain current.

Useful equations:

$$I_{ds} = \mu_n C_{ox}\frac{W}{L}\left\{(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}\right\} \qquad I_{ds} = \mu_n C_{ox}\frac{W}{L}\frac{(V_{gs}-V_T)^2}{2}$$

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Department of Electrical and Computer Engineering

Final Exam, Fall 2017

Semiconductor Devices Technology (EEE 313.01/ETE 411.01/EEE 410.01/ETE 443.01)

Time: 70 minutes   Full marks: 30

There are three questions. Attempt answers to all. Individual marks are indicated at the right margin.

1. A silicon pn junction at T = 300 K has the following parameters: $N_A = 7\times10^{16}$ cm^{-3}, $N_D = 1.5\times10^{17}$ cm^{-3}, $D_n = 20$ cm^2/s, $D_p = 13$ cm^2/s, $\tau_{n0} = 5.6\times10^{-7}$ s and $\tau_{p0} = 1.9\times10^{-7}$ s. The cross sectional area is $A = 3\times10^{-4}$ cm^2 and the forward bias voltage is $V_a = 0.15$ V. For recombination current calculation, $\tau_{n0r} = 7\times10^{-4}$ s, $\tau_{p0r} = 7\times10^{-4}$ s. Calculate the total current I_{diode} (A) in the p-n junction diode. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}. [10]

Useful equations:

$$J_{D\,Total} = q\left(\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right)\left(exp^{\left(\frac{V_a}{V_T}\right)} - 1\right) \text{ (A/cm}^2\text{)} \qquad L_p^2 = D_p\tau_{po}$$

$$L_n^2 = D_n\tau_{no} \qquad V_T = \frac{kT}{q} \qquad W = \sqrt{\left\{\frac{2\varepsilon_s(V_{bi}-V_a)}{q}\left[\frac{N_A+N_D}{N_AN_D}\right]\right\}}$$

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_AN_D}{n_i^2}\right) \qquad J_{rec} = \frac{qWn_i}{\tau_{por}+\tau_{nor}}exp^{\left(\frac{V_a}{2V_T}\right)} \qquad J_{diode} = J_{D\,Total} + J_{rec}$$

2. For a p-substrate silicon MOS capacitor, at T = 300 K, the substrate doping is $N_A = 5\times10^{16}$/cm^3.

(a) What is bulk potential, φ_B ?
(b) At inversion condition what is φ_s? (Hint: φ_s is total band bending at the surface).
(c) For $\varphi_m = 4.7$ eV and $\chi = 4.01$ eV (for silicon), what is the flatband voltage $V_{FB} = \varphi_{ms}$?
(d) Find the maximum depletion width x_{dT} (μm) at the inversion condition of the surface. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}. [4×2.5=10]

Useful equations:

$$x_{dT} = \left(\frac{2\varepsilon_s\varphi_s}{qN_A}\right)^{1/2} \qquad \varepsilon_s = 11.7\,\varepsilon_o \qquad \varphi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

3. An ideal n-channel MOSFET has the following parameters: $V_T = 0.48$ V, $\mu_n = 580$ cm^2/V-s, $t_{ox} = 10$ nm, W= 10 μm and L = 0.8 μm. Find the drain current I_{ds} for this MOSFET when

(a) $V_{gs} = 1.1$ V and $V_{ds} = 0.3$ V. [3.5]
(b) $V_{gs} = 1.4$ V and $V_{ds} = 1.8$ V. [3.5]
(c) $V_{gs} = 0.1$ V and $V_{ds} = 0.2$ V. [3.0]

North South University

Department of Electrical and Computer Engineering

Final Exam, Fall 2018

Semiconductor Devices Technology (EEE 313.01/ETE 411.01/EEE 410.01/ETE 443.01)

Time: 70 minutes

Full marks: 30

There are three questions. Attempt answers to all. Individual marks are indicated at the right margin.

1 (a) There are two p-n junction diodes A and B. Diode A has high p-side and n-side doping but diode B has low p-side and n-side doping. For both diodes, comment on the electric field E_{max} at $x = 0$ (whether E_{max} higher or lower). Plot E(x) versus x for both diodes where E(x) is electric field in the depletion region.

(b) A silicon pn junction at T = 300 K has the following parameters: $N_A = 2\times10^{15}$ cm^{-3}, $N_D = 5\times10^{16}$ cm^{-3}, $D_n = 26$ cm^2/s, $D_p = 16$ cm^2/s, $\tau_{n0} = 8.2\times10^{-7}$ s and $\tau_{p0} = 3.4\times10^{-7}$ s. The cross sectional area is $A = 3.2\times10^{-3}$ cm^2 and the forward bias voltage is $V_a = 0.6$ V. Calculate the total current I_{diode} (A) in the p-n junction diode. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}.

[4+6=10]

Useful equations:

$$J_{Diode} = q\left(\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right)\left(exp^{\left(\frac{V_a}{V_T}\right)} - 1\right) \text{ (A/cm}^2\text{)} \qquad L_p^2 = D_p\tau_{p0}$$

$$L_n^2 = D_n\tau_{n0} \qquad V_T = \frac{kT}{q} \qquad V_{bi} = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right)$$

2. (a) For a p-substrate MOS capacitor, suppose $V_{FB} = -3$ V and $V_G = -3$ V. What is the value of surface band bending φ_s?

(b) Suppose we have an enhancement mode (V_T>0) MOS-capacitor and a depletion mode (V_T<0) capacitor. We would like to reduce inversion charge formation at $V_G = -1$ V. Which capacitor type will allow that? Explain.

(c) For a p-substrate silicon MOS capacitor, at T = 300 K, the substrate doping is $N_A = 1.3\times10^{16}$/cm^3.

(i) What is bulk potential, φ_B ?

(ii) At inversion condition what is φ_s? (Hint: φ_s is total band bending at the surface).

(iii) For $\varphi_m = 4.35$ eV and $\chi = 4.01$ eV (for silicon), what is the flatband voltage $V_{FB} = \varphi_{ms}$?

(iv) Find the maximum depletion width x_{dT} (μm) at the inversion condition of the surface. Value of n_i at T = 300 K is 1.5×10^{10} cm^{-3}.

[2+2+1.5 x4=10]

Useful equations:

$$x_{dT} = \left(\frac{2\varepsilon_s\varphi_s}{qN_A}\right)^{1/2} \qquad \varepsilon_s = 11.7\,\varepsilon_0 \qquad \varphi_B = \frac{kT}{q} ln\left(\frac{N_A}{n_i}\right)$$

3. (a) Suppose for a n-channel MOSFETs, drain current is measured by saturation current. If V_{gs}, W and L are fixed for this device, how can you increase $I_{ds}(sat)$ for this device? Consider all parameters that are essential for computation of $I_{ds}(sat)$.

(b) An ideal n-channel MOSFET has the following parameters: $V_T = 0.4$ V, $\mu_n = 740$ cm^2/V-s, $t_{ox} = 10.9$ nm, W= 9 μm and L = 0.9 μm. Find the drain current I_{ds} for this MOSFET when

(i) V_{gs} = 0.2 V and V_{ds} = 0.15 V. [3+2+2.5x2 =10]
(ii) V_{gs} = 1.5 V and V_{ds} = 0.4 V.
(iii) V_{gs} = 1.8 V and V_{ds} = 2.2 V.

Make sure to apply the above bias conditions to determine cut-off, linear case and saturation case for calculation of drain current.

Useful equations:

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}\left\{(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}\right\}$$

$$I_{ds} = \mu_n C_{ox} \frac{W}{L} \frac{(V_{gs}-V_T)^2}{2}$$