

North South University
Department of Electrical & Computer Engineering
LAB REPORT

Course Code : EEE211. L

Course Title: Digital Electronics

Section: 01

Experiment Number: 01

Experiment Name: Combinational Logic Design

Experiment Date: 16th of November 2020

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Course Instructor: FHE

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Experiment Name:

Combinational Logic Design.

Objective:

- Familiarize with the analysis of combinational logic network.
- Learn the implement of networks using the two canonical forms.
- Devise combinational logic ^{circuits} using universal logic gates.
- Acquaint with basic binary arithmetic circuits - the half & full adders.

Theory:

Combinational logic is a type of digital logic which is implemented by Boolean circuits, where the output is a pure function of the present input only.

Minterm is a Boolean expression resulting in 1 for the output of a single cell & 0s for all other cells in a truth table. Maxterm is Boolean expression resulting in a 0 for the output of a single cell expression & 1s for all other cells in a truth table.

Two dual canonical forms of any Boolean function are, a "sum of minterms" & "a product of maxterm".

Apparatus:

- Trainer Board.
- 7411 IC Triple 3-input AND gates.
- 7432 IC Quadruple 2-input OR gates.
- 7404 IC Hex inverters (NOT gates).

Truth Table:

Input Reference	A	B	C	F	Minterm	Maxterm
0	0	0	0	0	$A'B'C'$	$A+B+C$
1	0	0	1	1	$A'B'C$	$A+B+C'$
2	0	1	0	1	$A'BC'$	$A+B'+C$
3	0	1	1	0	$A'BC$	$A+B'+C'$
4	1	0	0	0	$AB'C'$	$A'+B+C$
5	1	0	1	0	$AB'C$	$A'+B+C'$
6	1	1	0	1	ABC'	$A'+B'+C$
7	1	1	1	0	ABC	$A'+B'+C'$

Figure: Truth Table to a combinational circuit.

	Shorthand Notation	Function
1 st Canonical Form	$F = \sum(1, 2, 6)$	$F = (A'B'C) + (A'BC') + (ABC')$
2 nd Canonical Form	$F = \prod(0, 3, 4, 5, 7)$	$F = (A+B+C) \cdot (A+B'+C) \cdot (A'+B+C) \cdot (A'+B'+C)$

For Table, 1st & 2nd Canonical forms of Combinational Circuit.

Circuit Diagram:

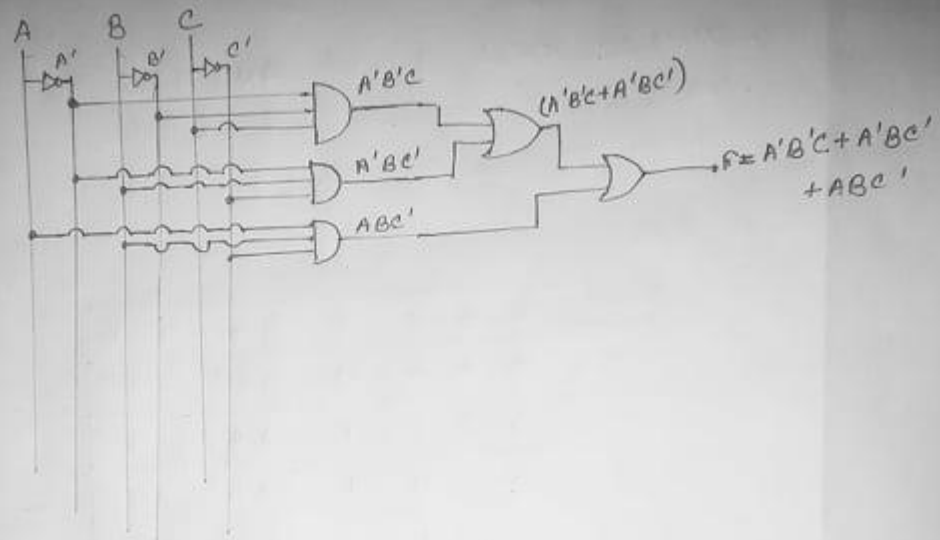


Figure: 1st Canonical form.

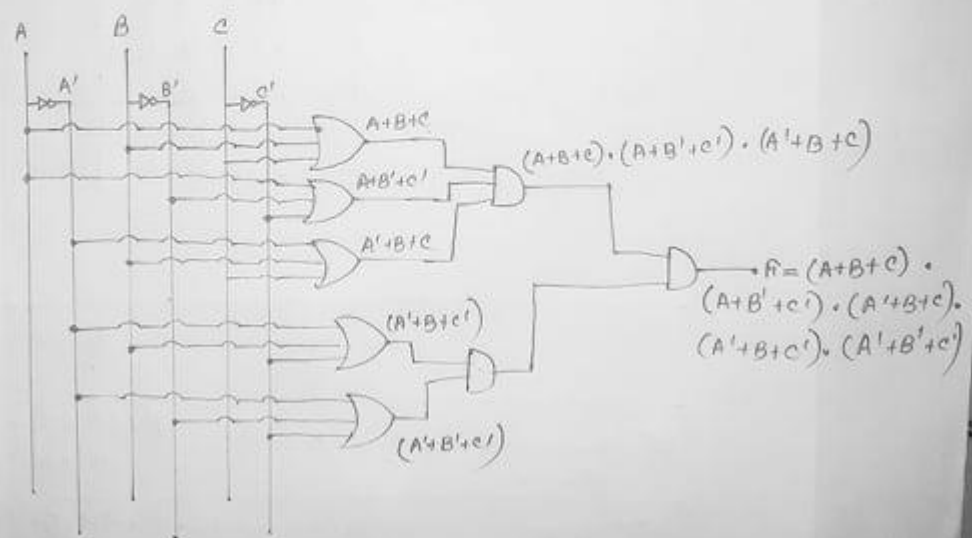


Figure: 2nd Canonical form $[F = (A+B+C) \cdot (A+B'+C') \cdot (A'+B+C) \cdot (A'+B'+C')]$

Simulation:

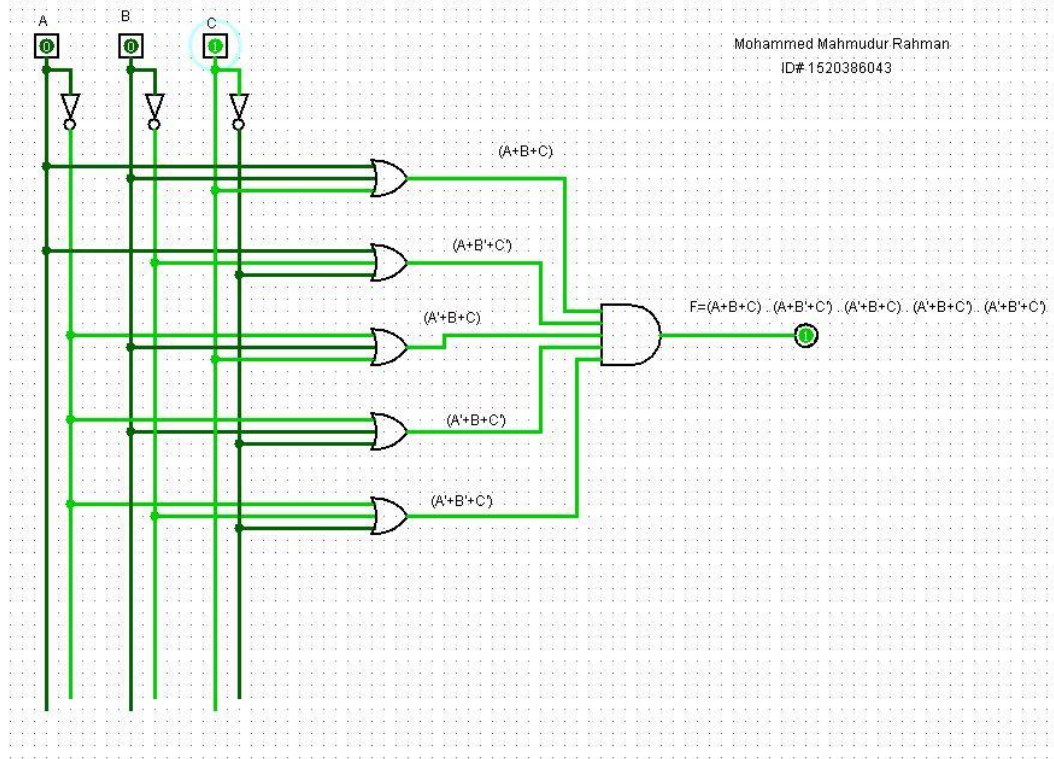


Figure 1:Simulation for Input 0 0 1

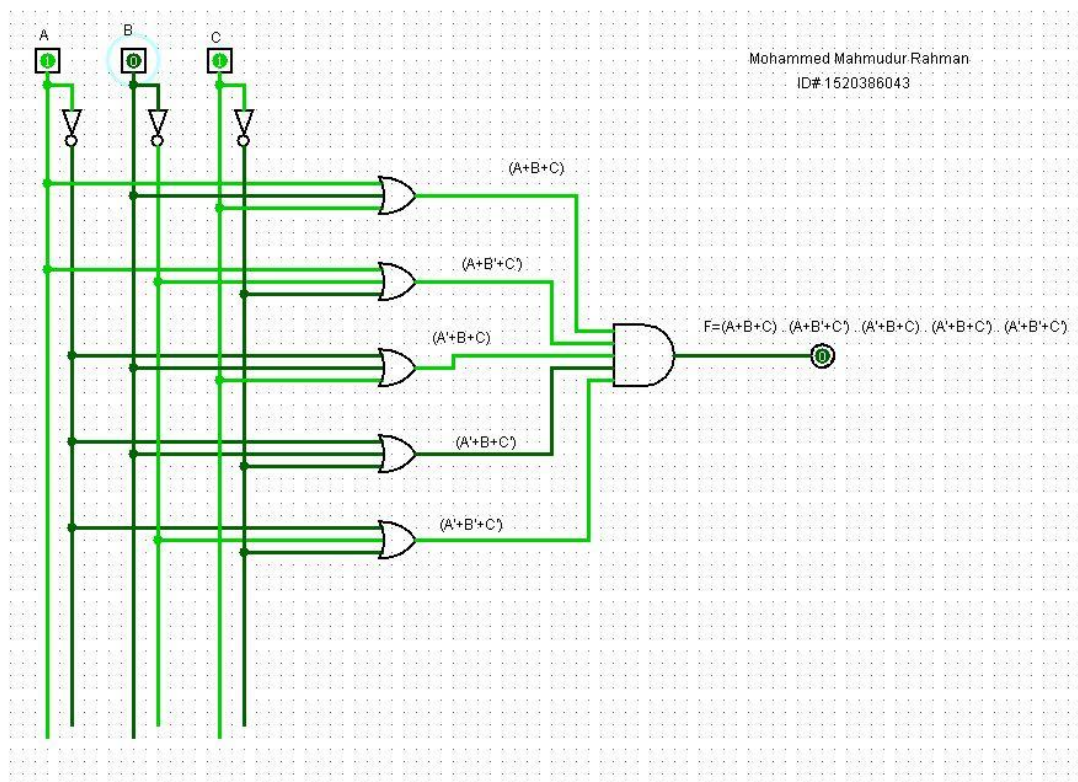


Figure 2: Simulation for Input 1 0 1

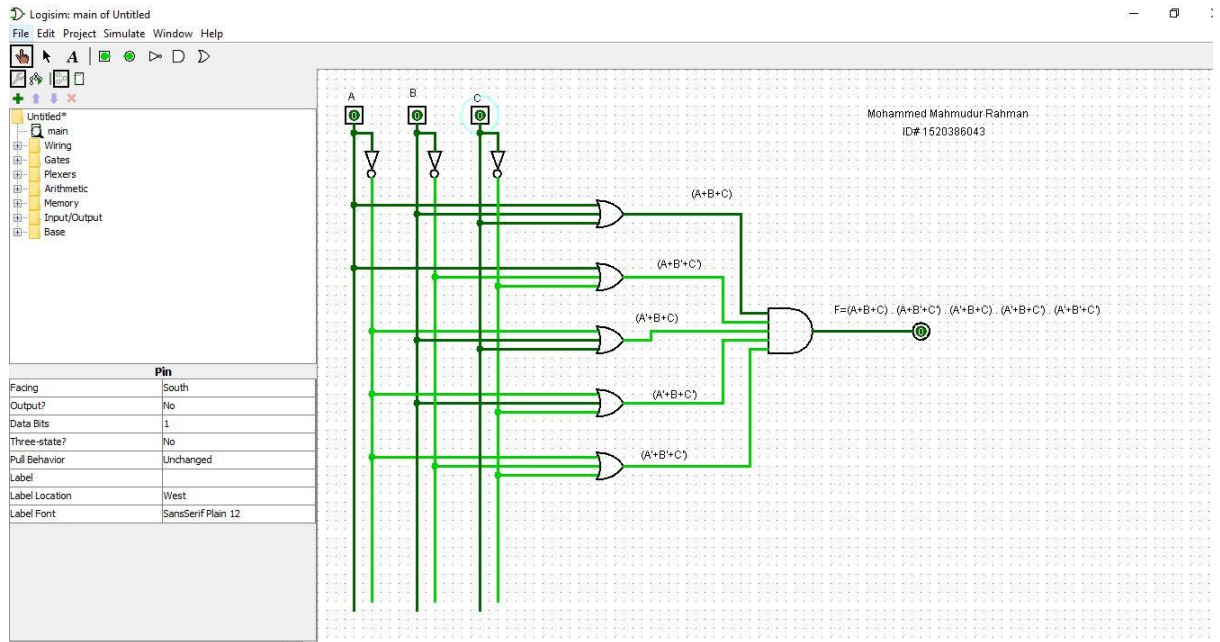


Figure 3: Simulation for input 0 0 0