Lab 2: Universal Gates

A.   Objectives

- Understand the concept of Universal Gates (NAND & NOR)
- Implement the basic logic gates using universal gates
- Implement boolean functions using universal gates
- Understand gate level minimization

B.   Apparatus

- Trainer Board
- IC 7400 Quadruple 2-input NAND gates
- IC 7402 Quadruple 2-input NOR gates

C.   Theory

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

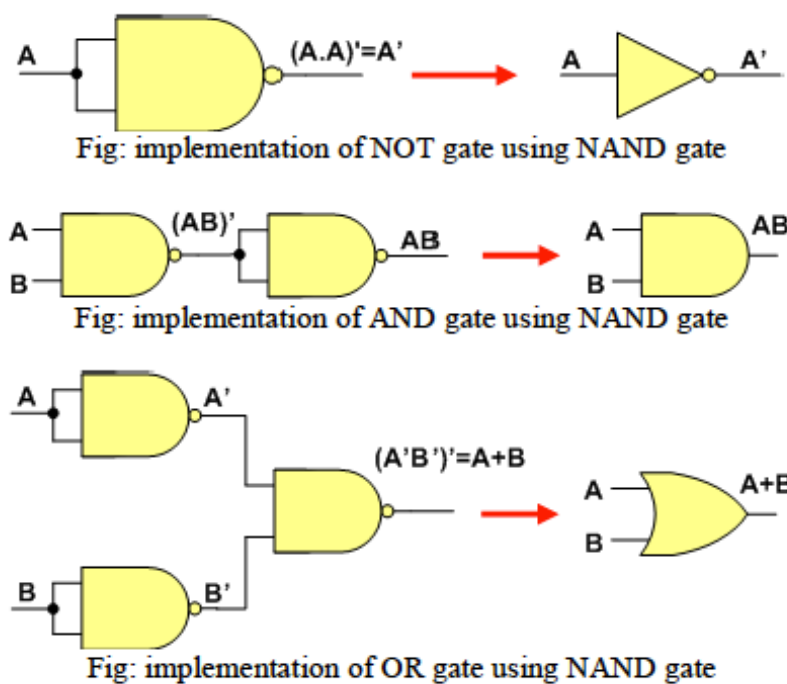**Figure C1** shows the implementation of NOT, AND & OR gates using only NAND gates.

Fig: implementation of NOT gate using NAND gate

Fig: implementation of AND gate using NAND gate

Fig: implementation of OR gate using NAND gate

Figure C1: NAND as a universal gate

D.   Procedure

1. Verify each of the NAND gate equivalent circuits in **Figure C1** to perform the same operations of the basic gates.
2. Design, construct and test the implementations of XOR and XNOR gates using NAND gates only. Show the circuits in **Figure F1** (Section F), clearly labeling the pin numbers.
3. Design, construct and test the implementations of NOT, AND, OR, XOR and XNOR gates using NOR gates only. Show the circuits in **Figure F2** (Section F), clearly labeling the pin numbers.
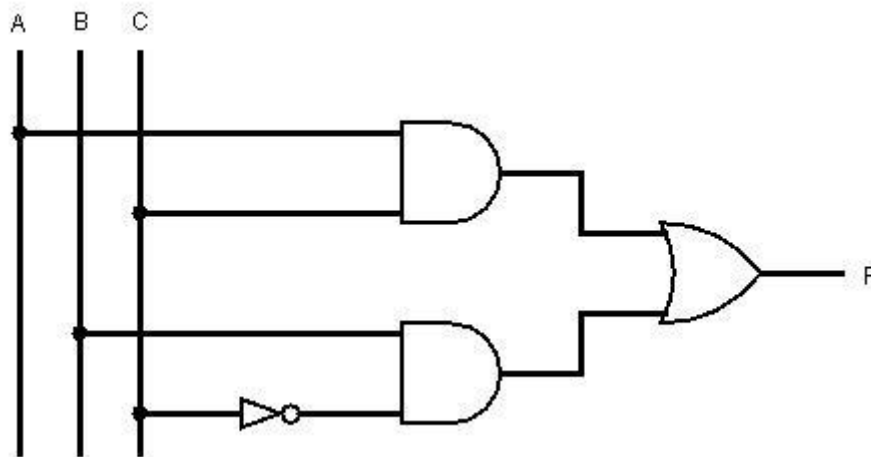
Figure D2: A combinational circuit

4. Complete the truth table for the circuit in **Figure D2** in Table F1 (Section F).
5. Convert the circuit in **Figure D2** to a NAND gate equivalent circuit, showing the steps involved and clearly labeling the pin numbers in the final circuit design. Show your work in **Figure F3** (Section F).
    (i) **Part 1** - Replace each of the gates with its NAND gate equivalent.
    (ii) **Part 2** - Identify any inversions that are compensated (i.e. one inverter followed by another) in part 1 and redraw the final circuit in part 2.
6. Validate the operation of the universal gate circuit from the truth table.

E. Report

1. Draw the IC diagram for the circuit in **Figure F3 – Step 2**.

2. Simulate the circuit in Figure F3 – Step 2 using Logisim. Provide a screenshot of the Logisim circuit schematic and truth table with your report.

F.   Experimental Data

XOR	XNOR

Figure F1: Implementation of XOR and XNOR using NAND gates

NOT	AND	OR

XOR	XNOR

Figure F2: Implementation of NOT, AND, OR, XOR and XNOR using NOR gates

A B C	I_1 = AC	I_2 = BC'	$F = I_1 + I_2$
0 0 0			
0 0 1			
0 1 0			
0 1 1			
1 0 0			
1 0 1			
1 1 0			
1 1 1			

Table F1: Truth table of combinational circuit in Figure B2

Part 1

Part 2

Figure F3: Universal (NAND) gate implementation of the circuit of Figure D2