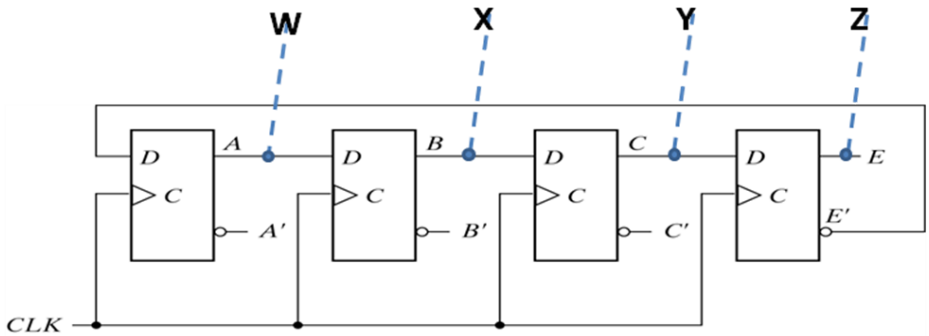
CSE 231 – Digital Logic Design
Quiz 3
Department of Electrical and Computer Engineering
North South University

Term: SPRING 2021
Total Marks: 15
Total Time: 20 min

1. Design a synchronous counter with J K flip-flops that count the following binary sequence: 0, 1, 2, 3, 4,5, 6, 7. Please show the detail design procedure. Truth table, equation for inputs. **(5 marks)**

2. (a) Consider the following switch-trail ring counter/Johnson counter. If the initial output value WXYZ = 0000, what would be value of WXYZ after 2 successive CLK cycles. show value for each cycle **(4 marks)**



3. (a) How many address lines are needed for each memory below? Also specify the total number of bytes stored in each memory. **(3*2=6 marks)**
   (i) 256K x 32
   (ii)16M x 16
   (iii) 8K x 8

   (b) How many D flip flops are rquired for each memoery devices?