# North South University

## CSE231L

## Experiment # 7

Name of Experiment: **Introduction to Flip-Flops and Shift Registers**

Date of Performance: 20 November, 2019

Date of Submission: 27 November, 2019

Section: 13

Group: 3

**Submitted To: Farhana Saleh**

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## Objectives

- We have to learn about the concepts of states in digital logic and how Flip-Flop circuits can be used to store state information.
- We have to understand the internal logic of J-K Flip-Flops and implement one using basic logic gates.
- We have to understand the relationship between J-K, T and D Flip-Flops and observe the characteristics of all three.
- We have to implement a shift register using D Flip-Flops and analyze its operation.

## Equipments

- Trainer Board.
- IC 7402 2-input NOR gates.
- IC 7411 3-input AND gates.
- IC 7404 Hex Inverter (NOT gates).

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## Theory=

A flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-Flops and latches are a fundamental building block of digital electronics systems used in computers, communications and many other types of systems. JK, D and T are three common types of flip-flops used in digital ~~tog~~ logic circuits. In a stable state, the output of a flip-flop is either 0 or 1. The output can only change when a clock pulse is supplied to the flip flop. The value that is stored in a flip-flop when the clock pulse occurs is determined by the inputs to the flip-flop at that time or the values presently stored in the flip-flop. The new value is stored when a pulse of the clock signal occurs.

A storage element in a digital circuit can maintain a

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binary state indefinitely, until directly by an input signal to switch states. The major differences among various types of storage elements are in the number of inputs they possess and in the manner in which the inputs affect the binary state.

| Characteristic Table | | | | Excitation Table | | | |
|---|---|---|---|---|---|---|---|
| J | K | $Q_{next}$ | | Q | $Q_{next}$ | J | K |
| 0 | 0 | Q | | 0 | 0 | 0 | X |
| 0 | 1 | 0 | | 0 | 1 | 1 | X |
| 1 | 0 | 1 | | 1 | 0 | X | 1 |
| 1 | 1 | $\bar{Q}$ | | 1 | 1 | X | 0 |

Table:- JK flip-flop: Characteristic and Excitation Tables.

| Characteristic Table | | | Excitation Table | | |
|---|---|---|---|---|---|
| T | $Q_{next}$ | | Q | $Q_{next}$ | T |
| 0 | Q | | 0 | 0 | 0 |
| | | | 0 | 1 | 1 |
| 1 | $\bar{Q}$ | | 1 | 0 | 1 |
| | | | 1 | 1 | 0 |

Table:- T flip-flop: Characteristic and Excitation Tables.

| Characteristic Table | | | Excitation Table | | |
|---|---|---|---|---|---|
| D | $Q_{next}$ | | Q | $Q_{next}$ | D |
| 0 | 0 | | 0 | 0 | 0 |
| | | | 0 | 1 | 1 |
| 1 | 1 | | 1 | 0 | 0 |
| | | | 1 | 1 | 1 |

Table:- D flip-flop: Characteristic and Excitation Tables.

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# Circuit Diagram

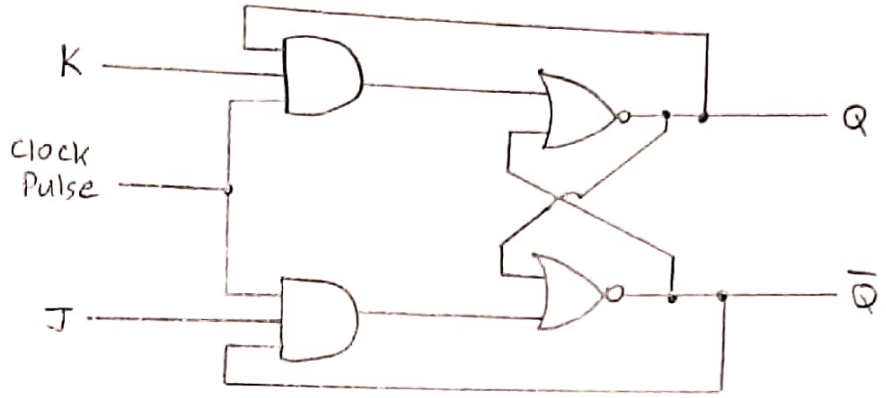


Figure:- JK Flip-Flop implemented using AND and NOR gates.

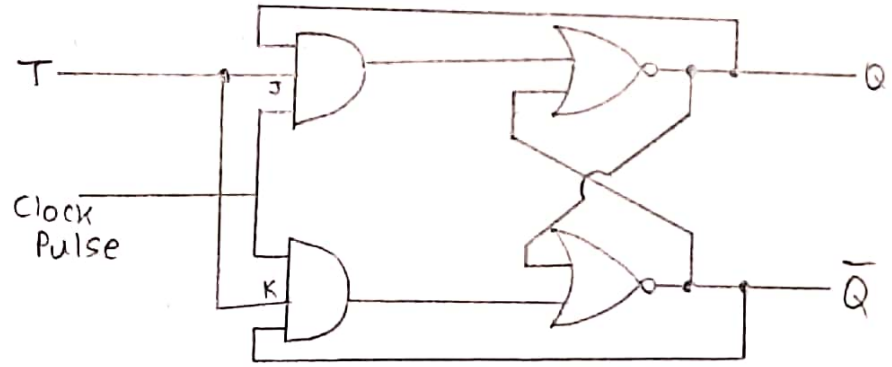


Figure:- T flip-flop constructed using JK flip-flop.

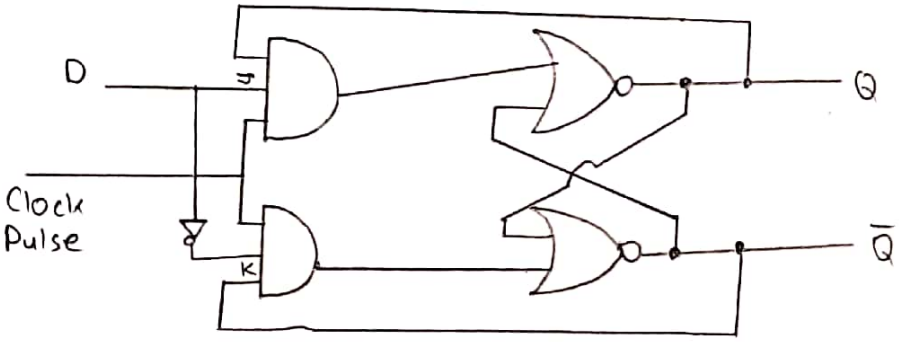


Figure:- D flip-flop constructed using JK flip-flop.

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# Results

| J | K | Q(n) | Q(n+1) |
|---|---|---|---|
| 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Table F.1.1

| T | Q(n) | Q(n+1) |
|---|---|---|
| 0 | Q | |
| 1 | $\overline{Q}$ | |

Table F.2.1

| D | Q(n) | Q(n+1) |
|---|---|---|
| 0 | 0 | |
| 1 | 1 | |

Table F.2.2

# Questions

## 21

T flip-flop is a one terminal combination of JK flipflop.

D flip-flop is a one terminal combination of SR flipflop.

D flipflop is a data flipflop which store either 0 or 1 when input 0 or 1; which mean what ever ~~the input~~;

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the output is same as input (stores).

T flipflop which gives toggles output for input 1; and it stores 0 for input 1.

D flipflop is data/delay type flipflop means its output only follow input but in synchronisation with clock and hence delayed by a clock. Its output doesn't change if clock is disabled.

## Discussion

Due to human error and equipment error, we didn't find our expected results.

In this lab, we learned about flip-flops. Our trainer board had errors. The clock pulse was not working properly. But our lab instructor checked our circuit and said that it was okay.

But when experimenting with T flip-flop and D flipflop the clock pulse worked and we were successful in those experiments.

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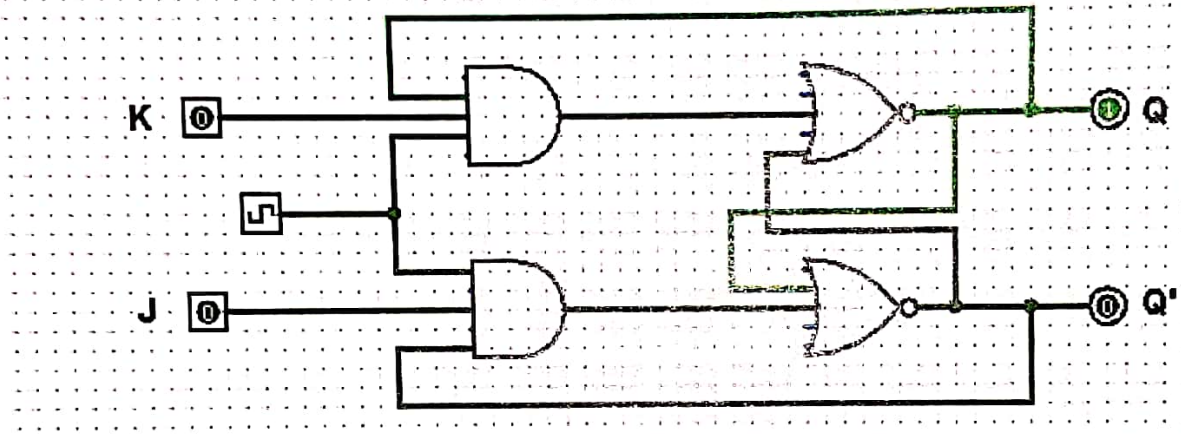


**Figure: JK Flip-Flop implemented using AND and NOR gates**

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# CSE231L/EEE211L
## Lab 7 – Flip-Flops and Shift Registers

Data Sheet:

| Section: 13 | Group No.: 3 | Instructor's Signature: ..... |
|---|---|---|
| | | Date: 20 November, 2019 |

**F.1 Experimental Data (JK Flip-Flop using AND and NOR gates):**

| J | K | Q(n) | Q(n+1) |
|---|---|---|---|
| 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | | |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Table F.1.1

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**F.2 Experimental Data (T and D Flip-Flops using J-K Flip-Flops):**

| T | Q(n) | Q(n+1) |
|---|---|---|
| 0 | Q | |
| 1 | $\overline{Q}$ | |

Table F.2.1

| D | Q(n) | Q(n+1) |
|---|---|---|
| 0 | 0 | |
| 1 | 1 | |

Table F.2.2

**F.3 Experimental Data (Right shift register using D Flip-Flops):**

| States | Input | Output |
|---|---|---|
| Initial State | X | XXXX |
| T1 | 1 | 1XXX |
| T2 | 0 | 10XX |
| T3 | 1 | 101X |
| T4 | 0 | 1010 |

Table F.3.1



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