Fall 2021

EEE/ETE 141L

Electrical Circuits-I Lab(Sec-5)

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Lab No. : 02

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Lab2: KCL, Current Divider Rule with Parallel and Ladder Circuit.

Experiment 1

Objectives

• We have to connect a parallel circuit on a breadboard.

• We have to validate the current divider rules.

• We have to verify Kirchhoff's current law.

• We have to verify KCL and KVL in ladder circuit.

List of Components:

• Trainer board

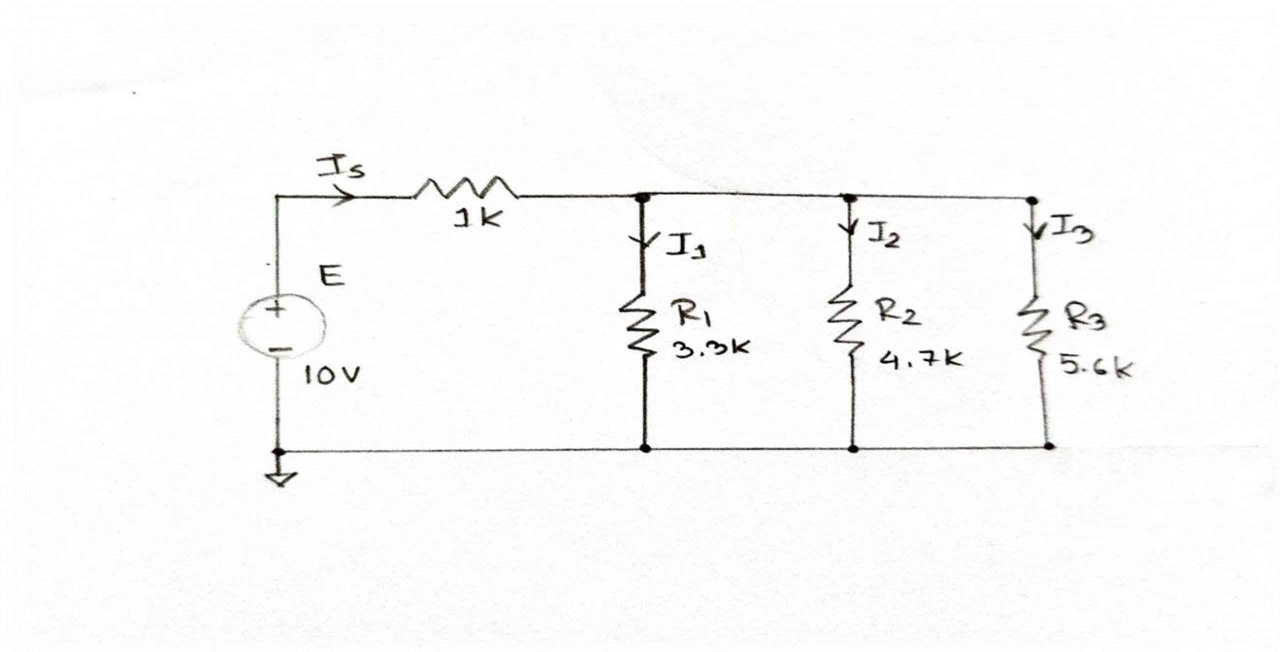
• Resistors (1K, 3.3k, 4.7 KΩ, 5.6K, 10K)

• Digital Multimeter (DMM)

• Connecting Wire

•Multisim

Circuit Diagram:



circuit 1

Data Table:

Table 1:

Resistance using colour coding							
Band 1	**Band 2**	**Band 3**	**Band 4**		**Resistance ±tol**	**Resistance using DMM**	**% Error**
Brown	Black	Red	Gold		1 kΩ +-5%	1 kΩ	0%
Orange	Orange	Red	Gold		3.3 kΩ +-5%	3.3 kΩ	0%
Yellow	Violet	Red	Gold		4.7 kΩ +-5%	4.7 kΩ	0%
Green	Blue	Red	Gold		5.6 kΩ +-5%	5.6 kΩ	0%
Brown	Black	Orange	Gold		10 kΩ +-5%	10 kΩ	0%

Table 2:

Experimental readings				Theoretical values			
I_S	IR1	IR2	IR3	I_S	IR1	IR2	IR3
4.098mA	1.788mA	1.256mA	1.053mA	4.1mA	1.8mA	1.258mA	1.06mA
% Error							
I_S	IR1		IR2			IR3	
0.0079%	0.017%		0.00158%			0.0060%	

Table 3:

I_S	4.098	Is Total Current equal to sum individual current?
Sum of individual Current (I_{R1} + I_{R2} + I_{R3})	(1.788+1.256+1.053)k=4.098k	Yes

Table 4:

Experimental Req	Theoretical Req	% Error
2.44k	2.44k	0%

Result:

From table 2,

Here,

R_T =3.3k//4.7k//5.6k= 1.44k

I_s= 10V/2.44k=4.1mA

R_{eq}=1.44k+1k=2.44k

Now using $I_X = Is*R_T / R_X$ we get theoretical values ,

I_{R1}= (4.1 *1.44)/3.3k =1.8 mA

I_{R2}= (4.1*1.44)/4.7k= 1.258 mA

I_{R3}=(4.1* 1.44)/ 5.6k = 1.06 mA

Again using % Error = (Theoretical value – Experimental Value) / Theoretical Value we get,

% Error of I_s= (4.1mA-4.098mA)/4.1mA= 0.0079%

% Error of I_{R1}=(1.8mA-1.788mA)/1.8mA=0.017%

% Error of I_{R2}=(1.258mA-1.256mA)/1.258mA=0.00158%

% Error of I_{R3}=(1.06mA-1.053mA)/ 1.06mA=0.0060%

From table 3,

I_s =4.098

Sum of individual Current (I_{R1} + I_{R2} + I_{R3})= (1.788+1.256+1.053

)mA= 4.098mA or 4.1mA

From table 4,

Experimental Req=2.44k

Now Theoretical Req,

R_T =3.3k//4.7k//5.6k= 1.44k

R_{eq}=1.44k+1k=2.44k

So,

Experimental Req= Theoretical Req with 0% Error.

Experiment 2

Objectives

- We have to connect a parallel circuit on a breadboard.

• We have to validate the current divider rules.

• We have to verify Kirchhoff’s current law.

• We have to verify KCL and KVL in ladder circuit.

List of Components:

• Trainer board

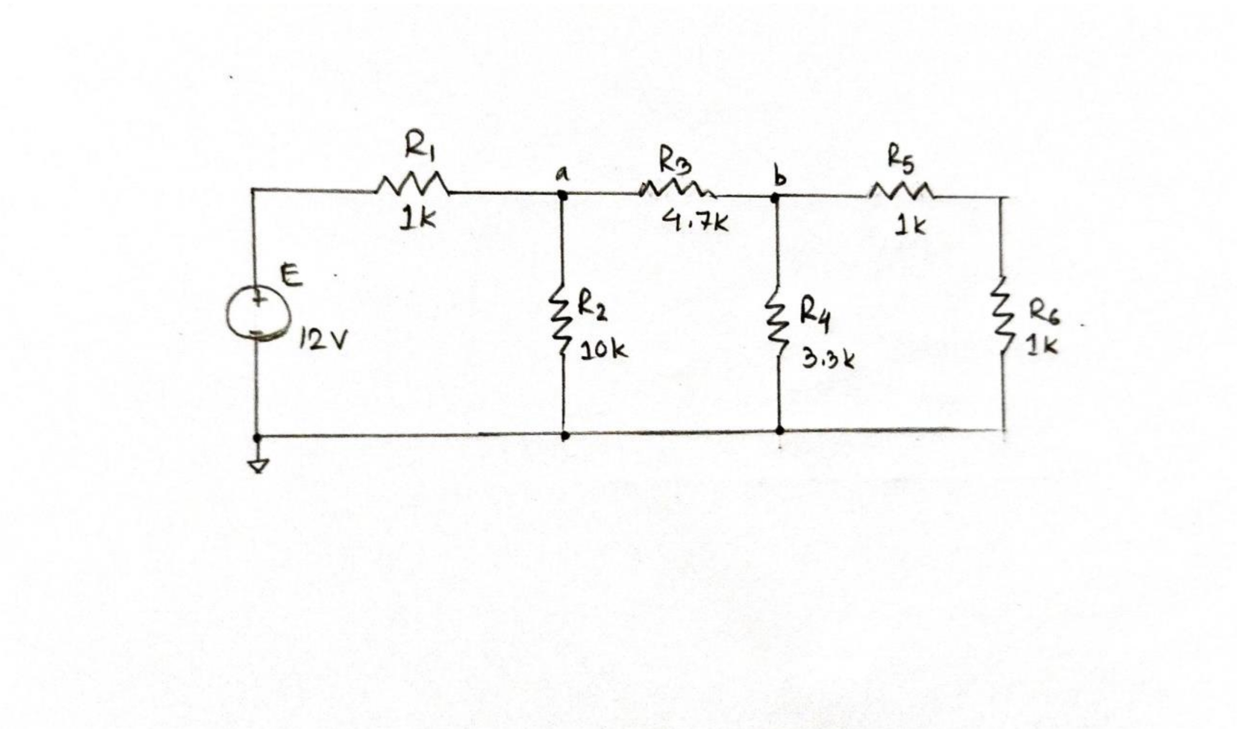
• Resistors (1K, 3.3k, 4.7 KΩ, 5.6K, 10K)

• Digital Multimeter (DMM)

• Connecting Wire

•Multisim

Circuit Diagram:



Circuit 2

Table 5:

Component	Voltage	Current
E	12	2.538A
R1	2.538V	2.538A
R2	9.462V	946.223uA
R3	7.48V	1.592mA
R4	1.982V	600.586uA
R5	990.967mV	990.996uA
R6	990.967mV	990.996uA

Question/Answer

1. State the current division rule.

Answer: Current Division rule states that the entire current separated into either of the parallel combination of two resistance or impedance is conversely corresponding to the esteem of resistance. It fundamentally tells us how the current is isolated within the parallel associated resistance.

2.State the Kirchhoff's current law (KCL).

Answer: Kirchhoff's Current Law (KCL) states that "the algebraic sum of the currents entering and leaving a node is equal to zero." This law is utilized to depict how a charge enters and takes off a wire junction point or node on a wire.

3. With the experimental data, verify Kirchhoff's voltage law in Circuit 1 within each independent closed loop of the circuit.

Answer: We have to Kirchhoff's voltage law in Circuit 1 within each independent closed loop of the circuit.
Here, V=10V

Now,

(10-Vx)/1k=Vx/3.3k+Vx/4.7k+Vx/5.6k

→10-Vx=(1/3.3k+a/4.7k+1/5.6kk)

→ 10=Vx(1+0.303k+0.21276k+0.17857k)

So, Vx=5.90 V

I_s=(10-5.902)/1k= 4.098mA

Again, I=Vx/3.3k

I_{R1}=5.902V/3.3k=1.788mA

I_{R2}=5.902V/4.7k = 1.256mA

I_{R3}=5.902V/4.7k= 1.053 mA

4.With the experimental data, verify Kirchhoff's current law at nodes *a* and *b* of circuit 2.

Answer:We have to apply KCL at node a,

2.538mA =0.946mA+1.592mA
→2.538mA = 2.538mA

So, Input current =Output Current

KCL is verified at node a.

Now, We have to apply KCL at node b,

→1.592 = 600.5+990.9
→1.592 = 1591.4

1.592 = 1.592

So, Input current = Output Current

KCL is verified at node b.

We can say that,Kirchhoff's current law is verified at nodes *a* and *b* of circuit 2.

Because output Current is equal to input Current.

5.Showing all steps, calculate the theoretical values in Table 2. Compare theoretical values to your experimental values and explain whether your circuit follows KCL or not.

Answer: We have to calculate the theoretical values in Table 2.
Here,

R_T =3.3k//4.7k//5.6k= 1.44k I_s= 10V/2.44k=4.1 mA

R_{eq}=1.44k+1k=2.44k

Now using $I_X = Is*R_T / R_X$ we get theoretical values ,

I_{R1}= (4.13 *1.44)/3.3k =1.8 mA

I_{R2}= (4.13*1.44)/4.7k= 1.258 mA

I_{R3}=(4.13 * 1.44)/ 5.6k =1.06mA

Sum of individual Current($I_{R1} + I_{R2} + I_{R3}$) of theoretical value=(1.8mA+1.258mA+1.06mA)=4.1 mA=I_s

Now we can get the experimental values using multisim. They are,

I_s= 4.1 mA

I_{R1}=1.778 mA

I_{R2}= 1.256 mA

I_{R3}=1.053mA

Sum of individual Current($I_{R1} + I_{R2} + I_{R3}$) of experimental value=(1.778mA+1.258mA+1.053mA)= 4.098mA or 4.1mA =I_s

So, analyzing the theoretical values and experimental values we can say that the circuit follows KCL.

6.Showing all the steps, theoretically calculate Req of circuit 1. Compare with the experimental value.

Answer: Experimental Req=2.44k

Now Theoretical Req,

R_T =3.3k//4.7k//5.6k= 1.44k

R_{eq}=1.44k+1k=2.44k

After analyzing the experimental Req and theoretical Req , we can say that both has same value and it is 2.44k which means there are 0% error.

Discussion:

From the lab 2, we learned about Kirchoff's Current law or KCL, Current Divider Rule using Parallel and Ladder Circuit.

As, it was an online lab, we had to use multisim to do the experiments. So, we didn't have to face many errors or faults. We could find the theoretical values easily.

If we would have done the lab offline, we could have faced many errors such human errors, environmental errors or mechanical errors. Also, we could have faces errors using DMM, cables, breadboard connection etc.