Department of Electrical & Computer Engineering

North South University

Final Project

Displaying the word ‘FEnCE05’

Submitted By : Group 2

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Course: Digital Electronics

Course Code: EEE211

Section: 01

Faculty Advisor:

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Combinational Part

Sat Sun Mon Tue Wed Thu Fri

Date :
Time :

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EEE/ETE 211
Project

Given word is 'FEnCE05'. I have to show each letter and digit in a 7 segment display.

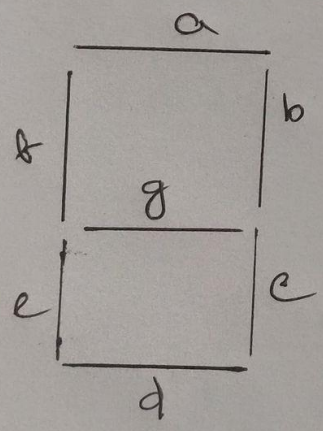


Figure : 7 segment display

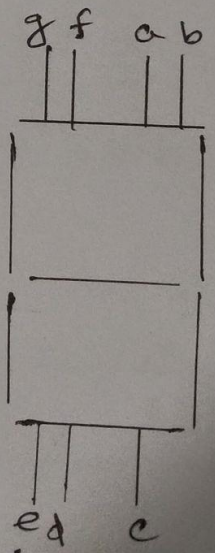


Figure : Pin connection of 7 segment display

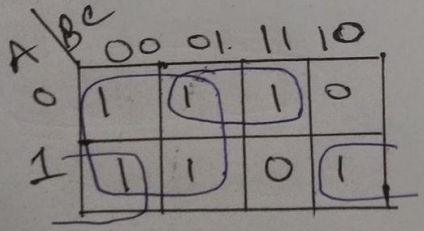
Rejuan Ahmed Khan
ID: 1231121043 Date:
Sat Sun Mon Tue Wed Thu Fri Time:

Truth Table:

Input			DISPLAY	Output						
A	B	C		a	b	c	d	e	f	g
0	0	0	F	1	0	0	0	1	1	1
0	0	1	E	1	0	0	1	1	1	1
0	1	0	n	0	0	1	0	1	0	1
0	1	1	C	1	0	0	1	1	1	0
1	0	0	E	1	0	0	1	1	1	1
1	0	1	O	1	1	1	1	1	1	0
1	1	0	5	1	0	1	1	0	1	1
1	1	1		0	0	0	0	0	0	0

Now, I have to determine the k-map for 7-segment pins (a, b, c, d, e, f, g) to find their respective equations.

k-map



$$\therefore a = \bar{B} + \bar{A}C + A\bar{C}$$

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A \ BC	00	01	11	10
0	0	0	0	0
1	0	1	0	0

$\therefore b = A\bar{B}C$

A \ BC	00	01	11	10
0	0	0	0	1
1	0	1	0	1

$\therefore C = B\bar{C} + A\bar{B}C$

A \ BC	00	01	11	10
0	0	1	1	0
1	1	1	0	1

$\therefore d = \bar{A}C + A\bar{B} + A\bar{C}$

A \ BC	00	01	11	10
0	1	1	1	1
1	1	1	0	0

$\therefore e = \bar{A} + \bar{B}$

A \ BC	00	01	11	10
0	1	1	1	0
1	1	1	0	1

$\therefore f = \bar{B} + \bar{A}C + AC$

A \ BC	00	01	11	10
0	1	1	0	1
1	1	0	0	1

$\therefore g = \bar{A}\bar{B} + \bar{C}$

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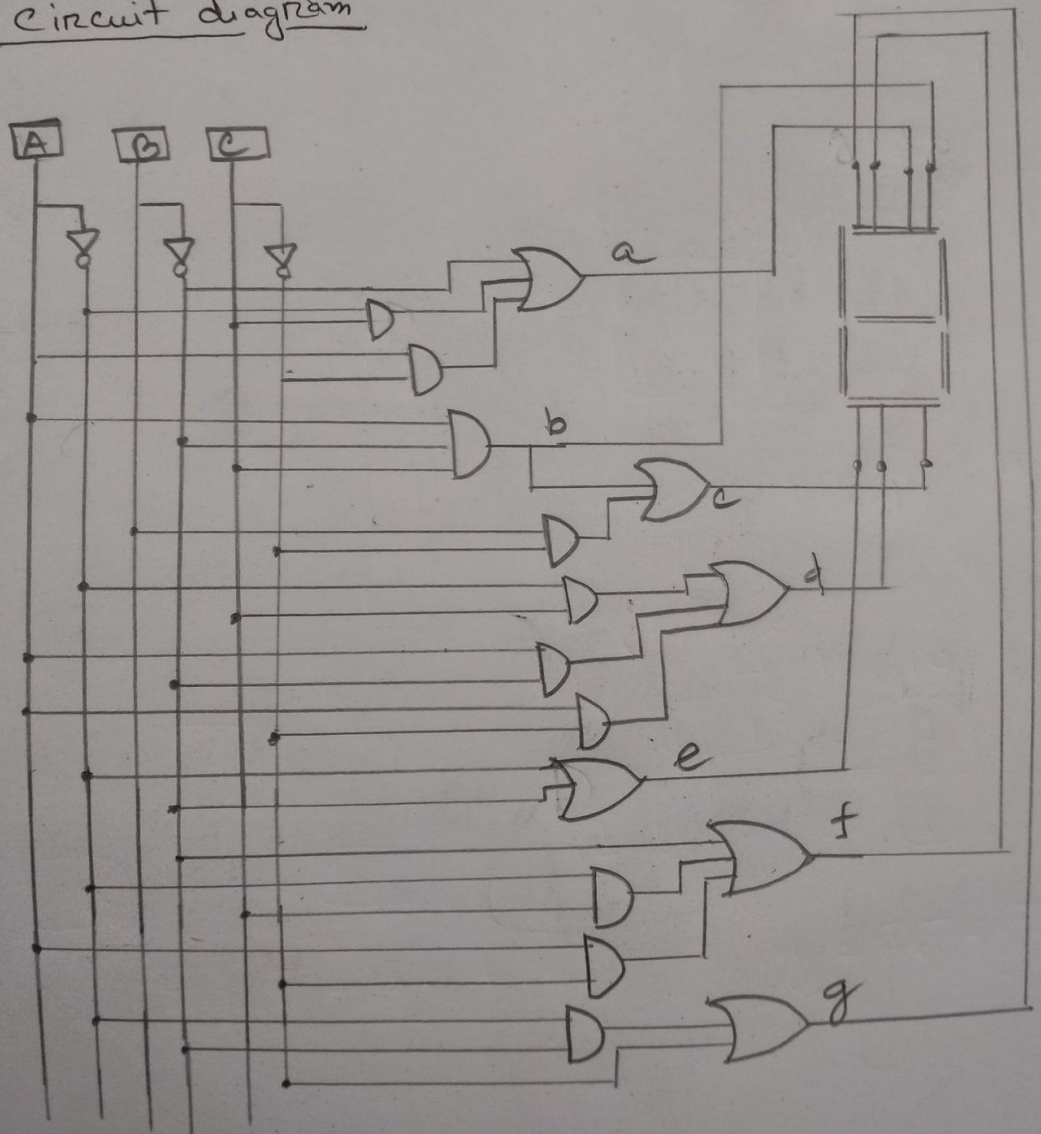
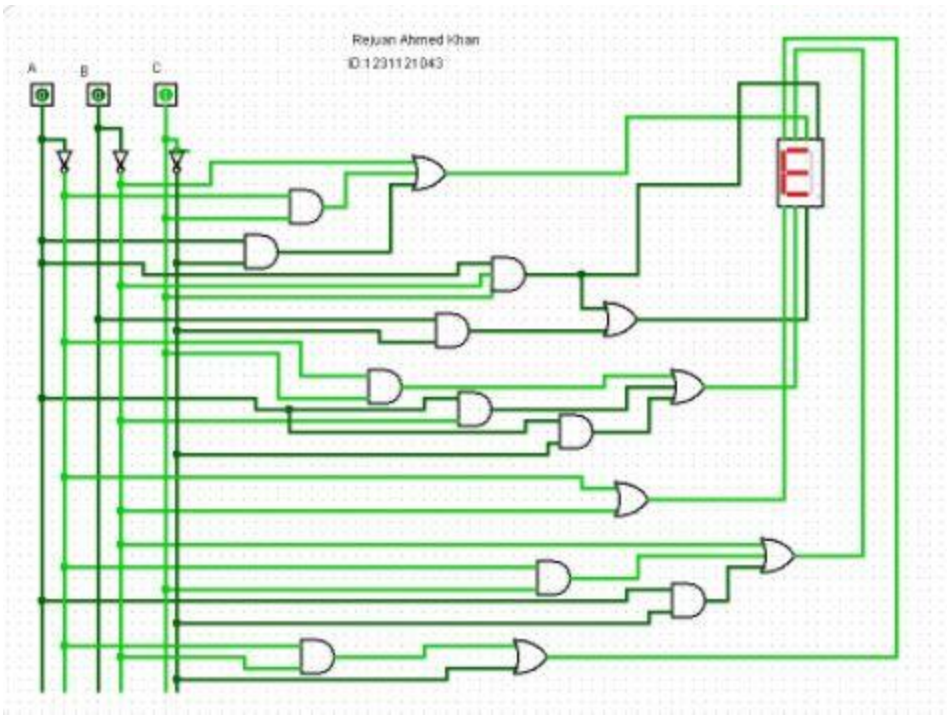
Now, from the determined pin equations I have to draw the circuit diagram using basic gates.

Circuit diagram

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A
B
C
E

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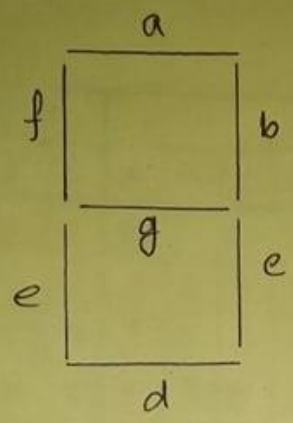
Group code: FENCE05

Universal gate: Universal gate is the type of gate by which we can implement any bolean function. We can replace any gate by universal gate but the operation will remain same. Using universal gate in a circuit is very much cost effective because when we use universal ~~circui~~ gate then we need just 1 type IC. There are two types of Universal gate. Nand and Nor.



In this project, we will use seven segment display to show output. In a seven segment display there are 7 differen LEDs such as a, b, c, d, e, f, g.

Inputs			Outputs							Output
x	y	z	a	b	c	d	e	f	g	Display
0	0	0	1	0	0	0	1	1	1	F
0	0	1	1	0	0	1	1	1	1	E
0	1	0	0	0	1	0	1	0	1	n
0	1	1	1	0	0	1	1	1	0	L
1	0	0	1	0	0	1	1	1	1	E
1	0	1	1	1	1	1	1	1	0	D
1	1	0	1	0	1	1	0	1	1	S
1	1	1	0	0	0	0	0	0	0	0

Truth table

x \ yz	00	01	11	10
0	1	1	1	0
1	1	1	0	1

$\therefore a = \bar{y} + \bar{x}z + x\bar{z}$

Name : Md. Shahriar Zahan Rejon

b

x \ yz	00	01	11	10
0	0	0	0	0
1	0	1	0	0

$b = x\bar{y}z$

c

x \ yz	00	01	11	10
0	0	0	0	1
1	0	1	0	1

$c = y\bar{z} + x\bar{y}z$

d

x \ yz	00	01	11	10
0	0	1	1	0
1	1	1	0	1

$d = x'z + xy' + x\bar{z}$

e

x \ yz	00	01	11	10
0	1	1	1	1
1	1	1	0	0

$e = x' + y'$

f

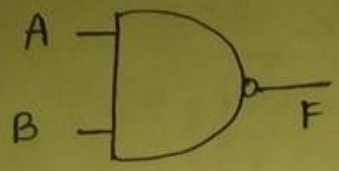
x \ yz	00	01	11	10
0	1	1	1	0
1	1	1	0	1

$f = \bar{y} + \bar{x}z + x\bar{z}$

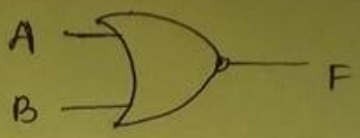
g

x \ yz	00	01	11	10
0	1	1	0	1
1	1	0	0	1

$g = x'y' + z'$



Nand



Nor

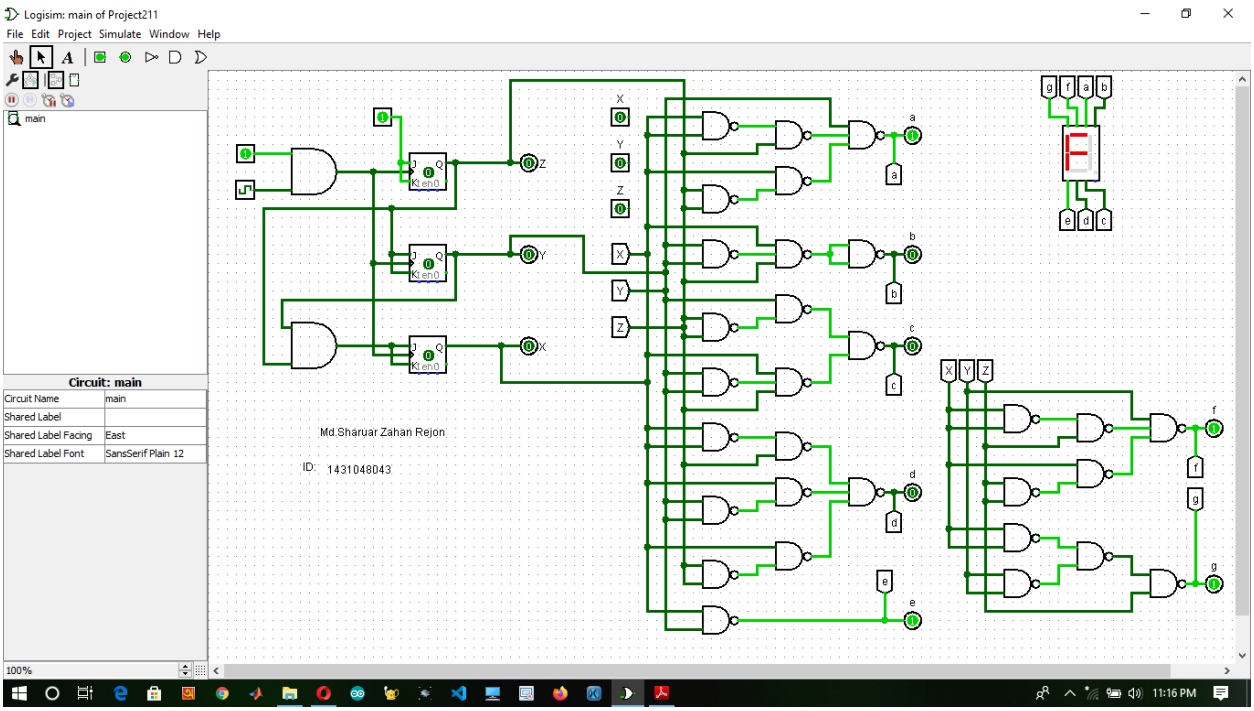
Truth Table For Nand

Input		Output
A	B	$X = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Truth table for NOR

Inputs		Output
A	B	$X = \overline{(A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

By using a bubble in the Output side we express universal gate.


Logisim: main of Project211
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main
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Md.Sharuar Zahan Rejon
ID: 1431048043
100%
11:16 PM

The Names Mohammed Mahmudur Rahman.
Student ID : 1520386043.

The combinational logic circuit is a type of digited logic circuit implemented using Boolean function, where the output of logic circuit is a pure functions of the presents inputs only.

A binary decoder is combination of logical circuit that converts binary information from the n coded inputs to a maximum 2^n unique outputs. Decoder circuit changes a code into a set of signals. It has maximum of 2^n output lines. One of these outputs will be active high based on the combination of present inputs.

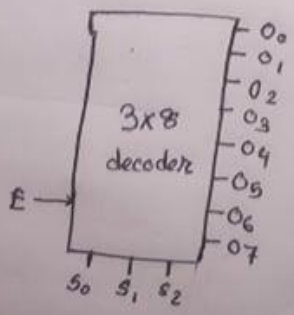

Figure: 3x8 decoder.

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Here, given word to show in a 7 segment display is 'FETICE05'. I have completed the decoder part.

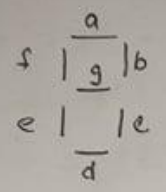

Figure: 7-segment display.

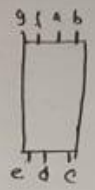

Figure: Pin-out of a 7-segment display in logisim.

There ~~was~~ was 6 or 8 digit in ~~any~~ our assigned word. To ~~display~~ show all of them in a single display I had to ~~do~~ build a truth table. If we can ~~only~~ use 7 different display for decoder no truth table would be required. So, here is my truth table:

Decimal value	X	Y	Z	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	1	1	1
1	0	0	1	0	0	0	1	1	1	1
2	0	1	0	0	0	1	0	1	0	1
3	0	1	1	0	0	0	1	1	1	0
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	1	1	1	1	1	1	0
6	1	1	0	0	0	1	1	0	1	1
7	1	1	1	0	0	0	0	0	0	0

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ID : 1620386043

Expression for 7 pin of the display:

$a = y' + x'z + xz'$

$b = xy'z$.

$c = yz' + xy'z$.

$d = x'z + xy' + zz'$

$e = x' + y'$

$f = y' + x'z + xz'$

$g = x'y' + z'$

a (0, 1, 3, 4, 5, 6)

b (5)

c (2, 5, 6)

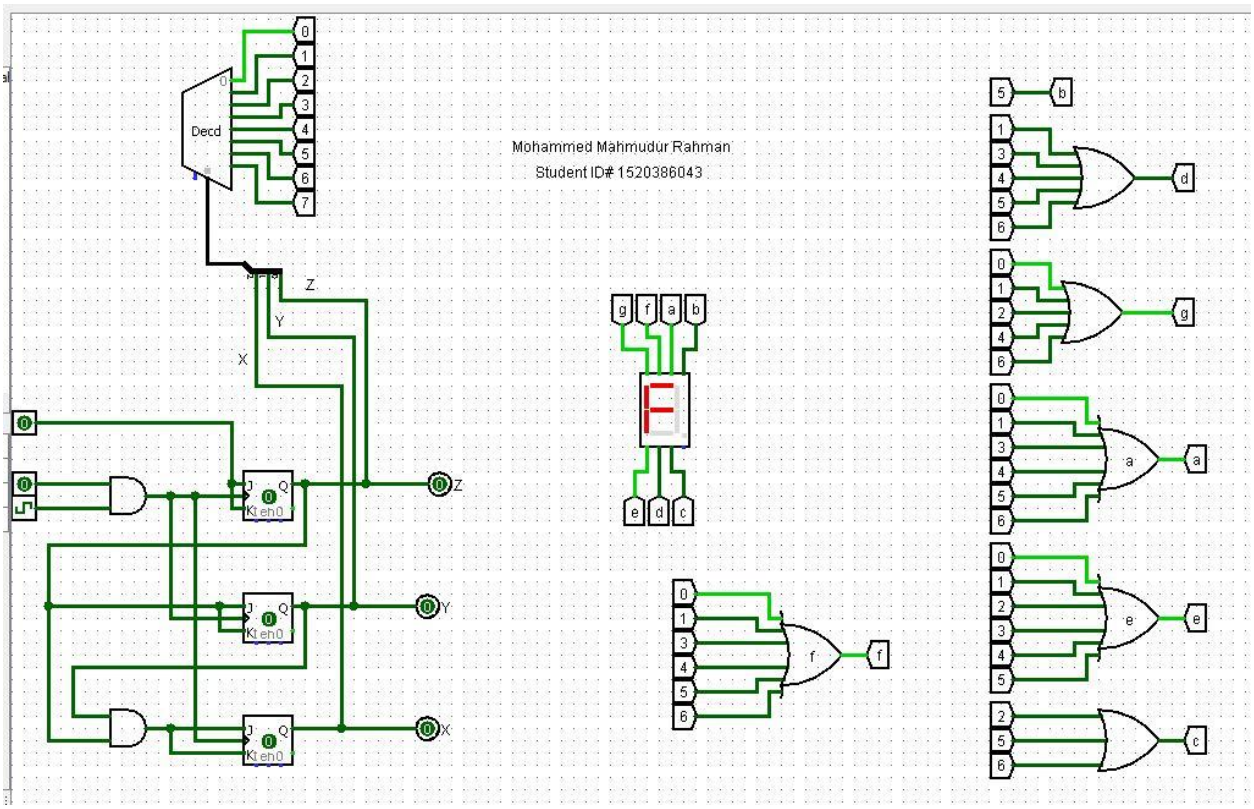
d (1, 3, 4, 5, 6)

e (0, 1, 2, 3, 4, 5)

f (0, 1, 3, 4, 5, 6).

g (0, 1, 2, 4, 6).

To show the mentioned word I have used a 3x8 decoder as there are 7 word alphabet in that word. As we don't required the 8th output we left it as an open connection ; so that no unwanted alphabet comes at the last.


Mohammed Mahmudur Rahman
Student ID# 1520386043
Decd
Z
Y
X
J
Q
Ken0
g
f
a
b
e
d
c
5
b
d
g
a
e
c

Report :- TAMIMA NUR KHAN
153000 9045

My part in this project was to design a seven segment display using a multiplexer. In designing this I have taken a 4×1 multiplexer. Truth table for this MUX was derived along with the seven digits from a to g. Later expressions were developed for the MUX inputs I_0, I_1, I_2, I_3. in terms of 1, 0, and C or $\bar{C}$. and then designed in the logisim.

A	B	C	a	b	c	d	e	f	g	
0	0	0	1	0	0	0	1	1	1	F
0	0	1	1	0	0	1	1	1	1	E
0	1	0	0	0	1	0	1	0	1	n
0	1	1	1	0	0	1	1	1	0	C
1	0	0	1	0	0	1	1	1	1	E
1	0	1	1	1	1	1	1	1	0	0
1	1	0	1	0	1	1	0	1	1	5
1	1	1	0	0	0	0	0	0	0	x

$I_0 = 1$
$I_1 = \bar{c}$
$I_2 = 1$
$I_3 = \bar{c}$
} for a

$I_0 = 0$
$I_1 = \bar{c}$
$I_2 = c$
$I_3 = \bar{c}$
} for c

$I_0 = 0$
$I_1 = 0$
$I_2 = c$
$I_3 = 0$
} for b

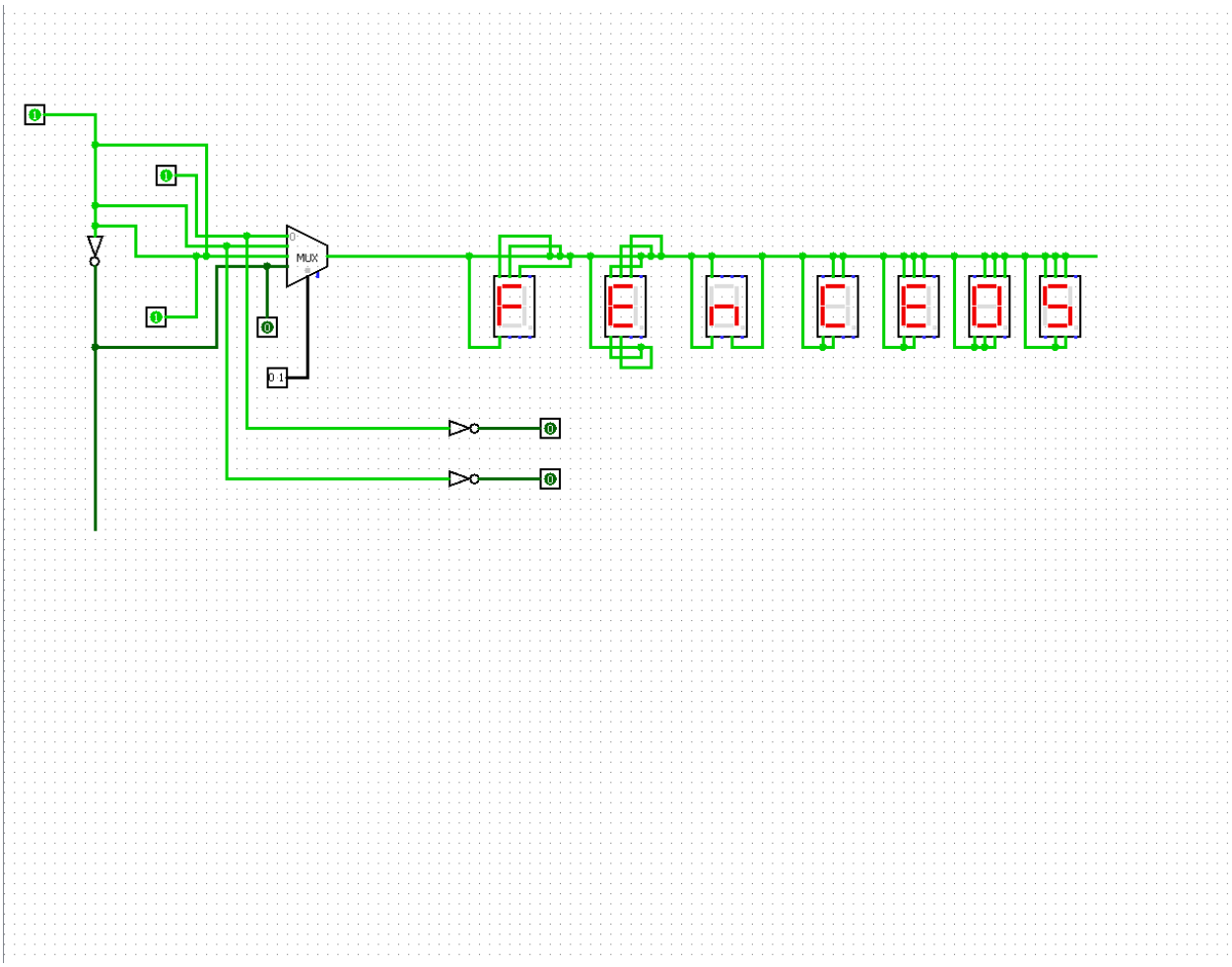
$I_0 = c$
$I_1 = c$
$I_2 = 1$
$I_3 = \bar{c}$
} for d

$I_0 = 1$
$I_1 = 1$
$I_2 = 1$
$I_3 = 0$
} for e

$I_0 = 1$
$I_1 = c$
$I_2 = 1$
$I_3 = \bar{c}$
} for f

$I_0 = 1$
$I_1 = \bar{c}$
$I_2 = \bar{c}$
$I_3 = \bar{c}$
} for g

TAMIMA NUR KHAN
1530009045.


MUX
0 1

Sequential Part

Sequential circuit design report:

A sequential circuit executes one or more inputs & produce one or more outputs. Sequential circuit requires a state table for it's execution. These states are related to some definite rules which it depends & generates by it by its previous states.

To design a sequential circuit we followed some basic steps. Firstly we have created a state ~~tab~~ transition diagram. Then determined the state transition table. Thirdly, we choose flip-flops & ~~then~~ created excitation table with state transition table. We have choosen T flip-flop for this design. By shorting J & K of JK ff we have made T flip flop.

Flip-flop is a basic building block of a sequential circuit. It is a storage device that can store one bit of data. It has two inputs & two outputs. As in sequential circuit for state transition we need to consider previous state then for storing that info we must need to

use a flip-flop for sequential circuit.

The J-K flip-flop that we used in the most versatile of the basic flip-flops. It has input following character of the clocke D flip-flop but has two iput labeled as J & K.

The J-K flip-flop is basically an SR flip-flop with feedback which enables only one of its two input terminals, either set or reset to be activate at one time. Therefore it eliminates the invalid condition which is found in SR flip-flop circuit.

The T-flip-flop is an edge triggered device. The low to high or high to low transitions on a clock signal of narrow triggers that is provided as input will cause the change in output state of flip-flop

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

fig: Excitation Table of T-flipflop.

T	Q^+
0	Q(t)
1	Q'(t)

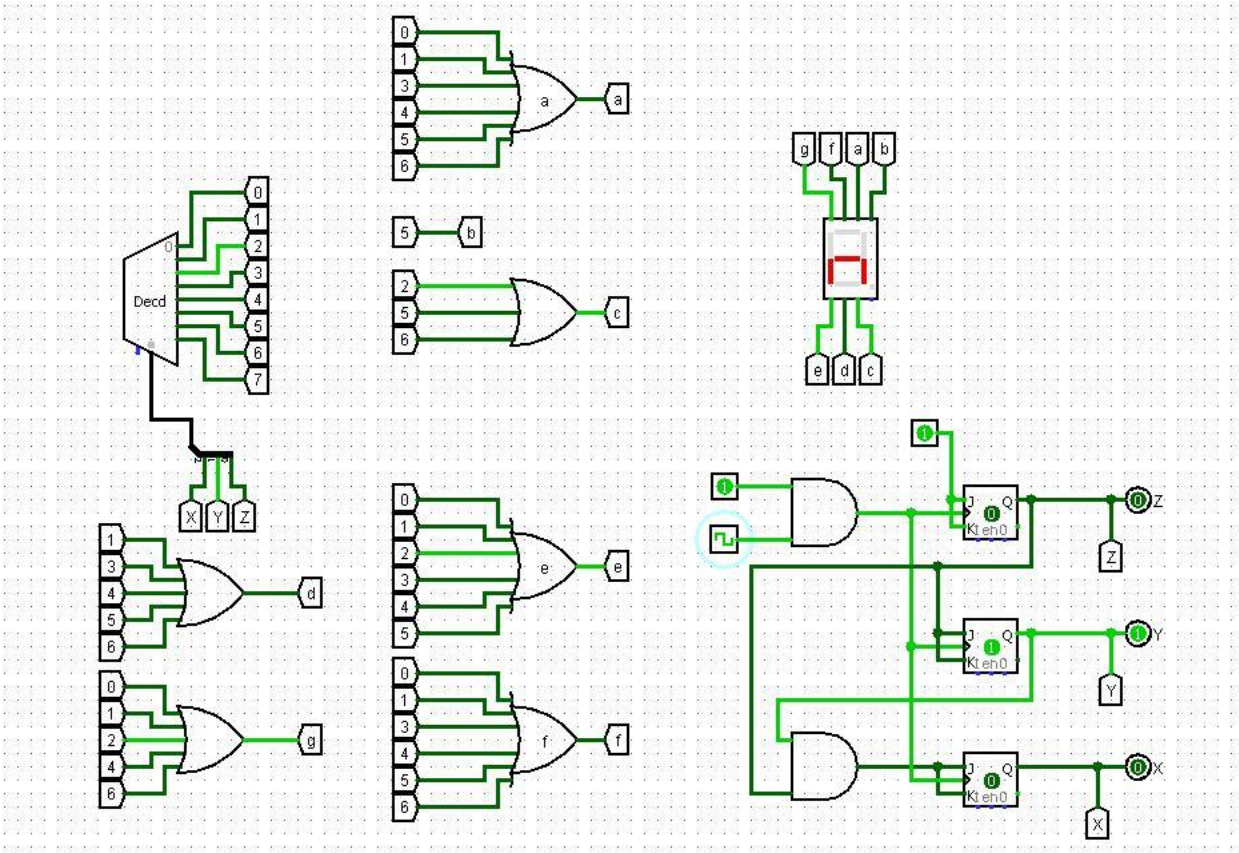
fig: Characteristics table of T flip-flop.

Sequential circuit: We have made a counter of 3 bits by using T flip flop. T flip-flop is a toggle flip flop. It changes it's output when it gets clock pulse.

Present state			Next state			Flip Flop inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

Here we have used JK flipflop to make T flip flop. Here J and K are shorted to make T flip flop.

P-


Decd
X
Y
Z
a
b
c
d
e
f
g
J
Q
K
en
Z
Y
X