NORTH SOUTH UNIVERSITY
Department of ECE
CSE 231: Digital Logic Design

Lab 8: Introduction to Flip-Flop and Register circuit.

Objectives

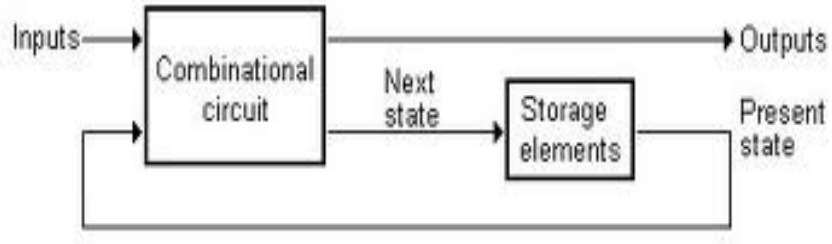
- Familiarize with the analysis of Flip-Flop & Register circuits.
- Learn the implementation of Flip-Flop & Register circuits using gates and ICs.
- Verify the Flip-Flop & Register circuits with the Truth table.

Apparatus

- Trainer Board
- IC 7411, 7402
- IC 7474(D flip-flop)
- Wires for connection

Theory

Digital electronic circuit is classified into combinational logic and sequential logic. Combinational logic output depends on the inputs levels, whereas sequential logic output depends on stored levels and also the input levels.



The storage elements (Flip -flops) are devices capable of storing 1-bit binary info. The binary info stored in the memory elements at any given time defines the state of the Sequential circuit. The input and the present state of the memory element determine the output. Storage elements next state is also a function of external inputs and present state.

Flip-Flop

A flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

We'll design JK flip-flop, T flip-flop and D flip-flop in this experiment.

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JOB 1: Design of a J-K Flip-flop using AND & NOR gates only.

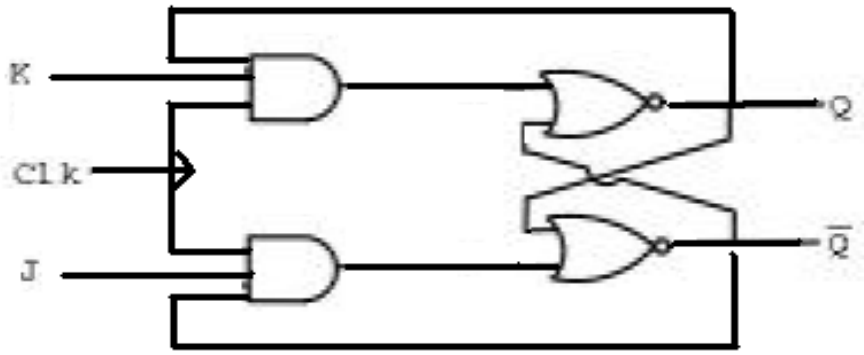
Procedure

1. Fill up the Table with different combination of inputs.
2. Implement the logic diagram of J-K Flip-flop using 3-input AND & 2-input NOR gates.
3. Verify the circuit with the truth table.

Truth Table

J	K	Q	Q'
1	0		
0	0		
0	1		
0	0		
1	1		
1	0		
1	1		

Circuit diagram:



JOB 2: Design of a T Flip-flop using J-K Flip-flop only.

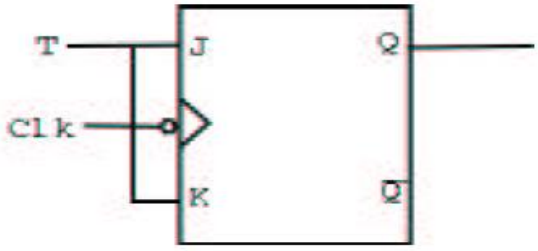
Procedure

1. Fill up the Table with different combination of inputs.
2. Implement the logic diagram of T Flip-flop using J-K Flip-flop.
3. Verify the circuit with the truth table.

Truth Table

T	Q	Q'
0		
1		

Circuit diagram:



JOB 3: Design of a D Flip-flop using J-K Flip-flop only.

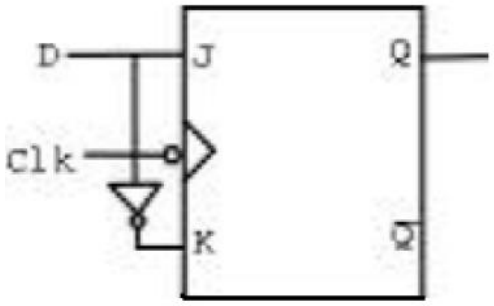
Procedure

1. Fill up the Table with different combination of inputs.
2. Implement the logic diagram of D Flip-flop using J-K Flip-flop.
3. Verify the circuit with the truth table.

Truth Table

D	Q	Q'
0		
1		

Circuit diagram:



Report

Write down your observations of the results from the implementation of flip-flop circuits.

Register

A register is a group of flip-flops. Each flip-flop is capable of storing one bit of information. An n-bit register contains a group of n flip-flops capable of storing n bits of binary information. In addition to flip-flops, a register may have combinational gates that perform certain data processing tasks. In broadest definition, a register consist of a group of flip-flops and gates that effect their transition. The flip-flop holds binary information and the gates determine how the information is transferred into the registers.

A register is capable of shifting its binary information either to its right or its left is called a shift register. The logical configuration of a shift register consists of a chain of flip-flops connected in cascade, with the output of one flip flop connected to the input of the next flip-flop. All flip-flops receive a common pulse which causes the shift from one stage to the next.

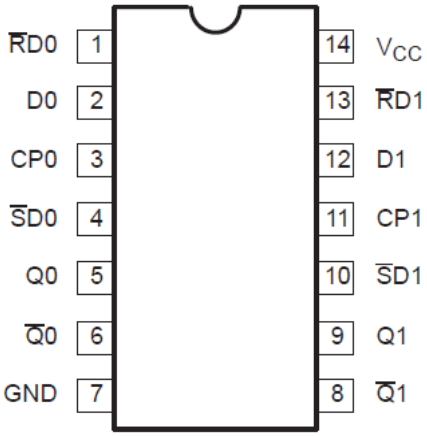
In this experiment, you will use D flip-flop to construct a 4 bit right shift register.

JOB 4: Design of a 4 bit Right Shift Register circuit using D Flip-flop.

Procedure

1. Construct the circuits according to the given diagrams and pin configuration of the IC7474. .
2. Observe the outputs and verify the Register circuit according to the truth table.

Layout diagram of IC 7474



PINS	DESCRIPTION
D0, D1	Data inputs
CP0, CP1	Clock inputs (active rising edge)
$\overline{S}D0$, $\overline{S}D1$	Set inputs (active low)
$\overline{R}D0$, $\overline{R}D1$	Reset inputs (active low)
Q0, Q1, $\overline{Q}0$, $\overline{Q}1$	Data outputs

Circuit diagram

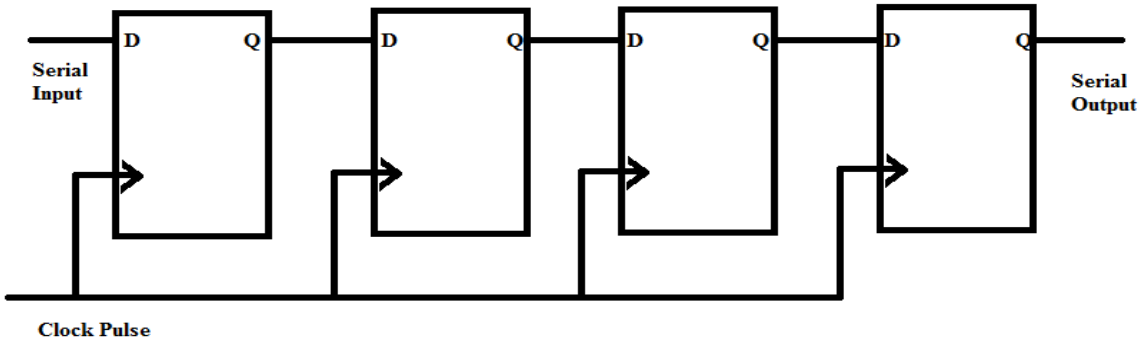


Figure: Shift Register

State Table

States	Input	Output
Initial State	X	XXXX
T1	1	1XXX
T2	0	01XX
T3	1	101X
T4	0	0101

Report

Write down your observations of the results from the 4 bit Right Shift Register circuit.

Assignment

Draw the logic diagram of SR flip-flop with Truth Table and also draw the logic diagram of D & T flip-flop.

Simulation

- Simulate the logic diagram of SR, JK, D, T flip-flop circuits.
- Simulate the logic diagram of 4 bit Right Shift Register circuit.