North South University
Department of Electrical Engineering & Computer Science
Assignment, Spring 2021
CSE 231 (Digital Logic Design)

Total Marks: 70

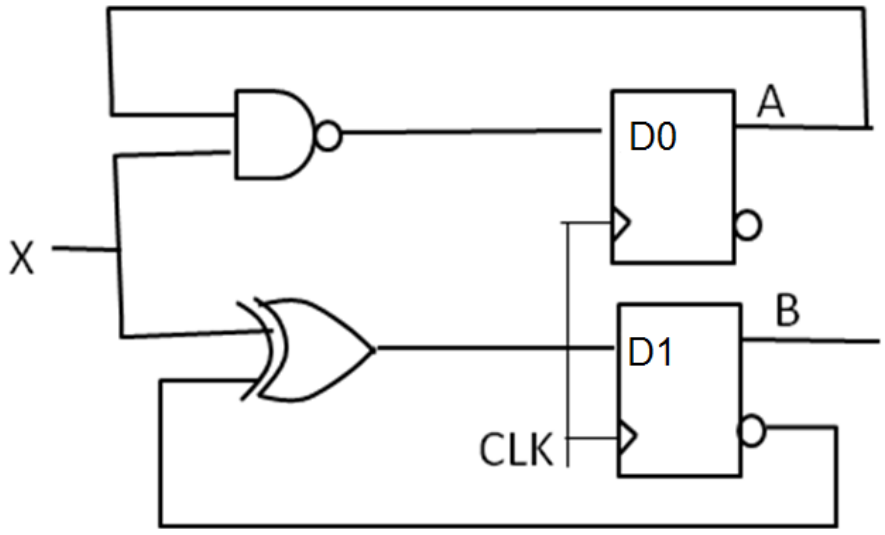
Answer all questions. You must show all steps of your works. Individual marks are indicated at the right margin.

STUDENT's NAME:

STUDENT's ID: _____
SECTION: ____10_____

---

1. Analyze the following sequential circuit. Derive the (a) state equations (b) state table and (c) state diagram of the following sequential circuit. [**15 points**]



2. Design a synchronous counter with JK flip-flops that count the following binary repeated sequence: 0, 4, 2, 5, 3, 1. Please show the detail design procedure as state transition table, state diagram, logic equations and logic diagram **[15 Marks]**

3. A 32 Kilobyte RAM has a word size of 8 bits. **(20 Marks)**

(a) How many address bits does the RAM require?

(b) How many D Flip Flop does the RAM require?

(c) Draw a clearly labeled logic diagram of a binary storage cell and describe.

(d) Explain the concept of read and write for a memory unit.

9. Consider the following set of Boolean functions: **[10 Marks]**

$W(p, q, r) = \sum(0,1, 5,7)$

$X(p, q, r) = \sum(0, 3, 5, 7)$

$Y(p, q, r) = \sum(2, 3)$

(a) Deduce the optimal ROM truth table for the above functions.

(b) Draw the ROM logic diagram to implement the circuit.

10. Consider the following switch-trail ring counter. If the initial output value WXYZ = 0000, what would be value of WXYZ after four successive CLK cycles. Please also complete the given timing diagram **[10 Marks]**