North South University

Department of Electrical and Computer Engineering

CSE231L – Digital Logic Design Lab
Lab Outline

Instructor:
Md. Anisur Rahman Asif
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Student consultation hour/s:
Saturday: 12:30pm - 02:30pm

Office room: LIB600(C1)
***For extra consultation hour, make an appointment through text or email.**

Tentative Class Plan:

Week	Topic	Assessment
1,2	Digital Logic Gates and Boolean Functions	
3,4	Universal Logic Gates	
5,6	Combinational Logic Design (Canonical Form)	
7,8	Combinational Logic Design (K Maps)	Quiz-1 (week-7)
9,10	Binary Arithmetic	
11,12	Multiplexer and Decoder	Midterm (week-12)
13,14	Flip-Flops - Registers	
15,16	Synchronous Sequential Circuits	Quiz-2 (week-15)
17		Setup Test, Viva, Final

Tentative Marking Rubric:

Category	Marks (in %)
Attendance	**10**
Class Performance	**5**
Lab Report (groupwise) & Simulation (Individual)	**20**
Quiz (Written)	**15**
Midterm Exam (Written)	**20**
Final Exam (Written)	**20**
Setup-test (Individual)	**10**
Total	**100**

Lab Report Marks Distribution (20 Points):

- **Cover Page-0.5**
- **Experiment Name-0.5**
- **Objective-0.5**
- **Apparatus-0.5**
- **Theory-1**
- **Circuit Diagram-1**
- **Experimental Procedure-1**
- **Results-2**
- **Question/Answer-4**
- **Discussion-3**
- **Data Sheet-1**
- **Simulation-5**

***Check the file - 'Lab Report Instructions' for further details.**