Lab 4: Combinational Logic Design

Objective:

• Design a complete minimal combinational logic system from specification to implementation.
• Minimize combinational logic circuits using Karnaugh maps.
• Learn various numerical representation systems.
• Implement circuits using canonical minimal forms.

Apparatus:

- Trainer Board
- 1 x IC 4073 Triple 3-input AND gates
- 1 x IC 4075 Triple 3-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)
- 1 x IC 7400 2-input NAND gates
- 2 x IC 7408 2-input AND gates

Theory:

A combinational logic circuit consists of logic gates whose outputs at any time are determined directly from the present combination of inputs without regard to previous inputs. In other words, the combinational logic circuits do not have the ability to memorize their past. On the other hand, a sequential logic circuit consists of not only logic gates but also memory elements. Therefore, the outputs of sequential logic circuits depend not only on the present values of the inputs but also on the input's previous values. In other words, the outputs of a sequential logic circuit are functions of its present inputs and the previous state of its memory elements.
Gate-level minimization is the design task of finding an optimal gate-level implementation of the Boolean functions describing a digital circuit. However, the procedure of minimization is awkward because it lacks specific rules to predict each succeeding step

in the manipulative process. The map method, on the other hand, provides a simple, straightforward procedure for minimizing Boolean functions. This method may be regarded as a pictorial form of a truth table. The map method is also known as the Karnaugh map or K-map.

Karnaugh maps is a tool for representing Boolean functions of up to six variables. K-maps are tables of rows and columns with entries represent 1`s or 0`s of SOP and POS representations. An n-variable K-map has 2 n cells with each cell corresponding to an n-variable truth table value. K-map cells are labeled with the corresponding truth-table row. K-map cells are arranged such that adjacent cells correspond to truth rows that differ in only one bit position.

F. Experimental Data

Decimal Digit	Binary Coded Decimal (BCD)				Excess-3			
	W	X	Y	Z	A	B	C	D
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table F1: Truth table - BCD to Excess-3

Number of inputs bits:	4	**Input variables**	WXYZ
Number of outputs bits:	4	**Output variables**	ABCD

Table F2: System analysis

0	0	0	0
0	1	1	1
X	X	X	X
1	1	X	X

F= W+X(Z+Y)

0	1	1	1
1	0	0	0
X	X	X	X
0	1	X	X

F=X + (Z+Y)

1	0	1	0
1	0	1	0
X	X	X	X
1	0	X	X

F=Y'Z' + YZ

1	0	0	1
1	0	0	1
X	X	X	X
1	0	X	X

F=Z'

Figure F1: K-Maps

Figure F2: Minimal 1st canonical circuit of BCD to Excess-3 converter

Figure F3: Minimal universal gate implementation of BCD to Excess-3 converter