

North South University

Department of Electrical & Computer Engineering

LAB REPORT

Course Code: EEE/ETE 241 L

Course Title: Electrical Circuit 2

Course Instructor: NNP

Experiment Number: 03

Experiment Name:

Series RLC Circuit

Date of Experiment: May, 2020

Date of Submission: January, 2021

Section: 02

Group Number: 04

	Student Name	ID	
2.	Kaniz Fatema	1520064045	
3.	Mohammed Mahmudur Rahman	1520386043	

Objective: To analyze the relationship between the voltage and phase of reactive relements and the source in series FC, FL and FLC ci periets.

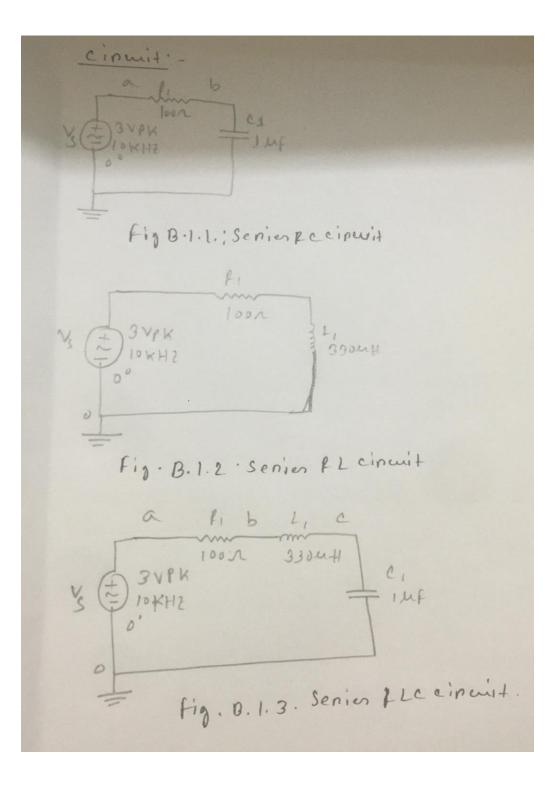
Background: -

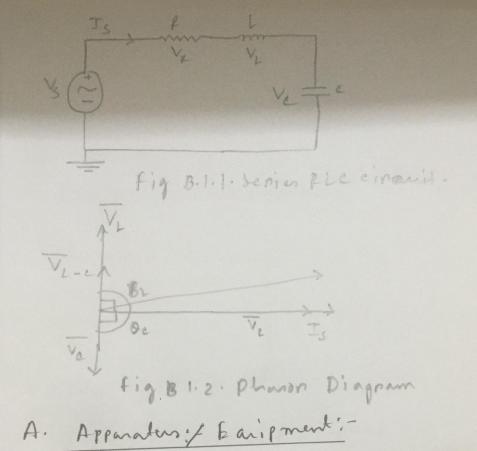
B. I Voltage and went in an Accircuit:

An PLC circuit is an electrical circuit consisting of a perinter, an inductor, and a capacitor, connected in series or in parallel. The complen impedence in an Ac circuit 10 represented by 2 and engrened in cartesian torm by formula 2 = R + in where the real part of impedance is the peristance I and the imaginary part is the peachance . Here, impedance can also be enpressed in magnitude and Phone form 12/10 where O is the Phone difference between the voltage and the current. The magnitude of the Impedence can be responded as 17] = V ++ xx and the phase can be enpressed as, 0: tan't. Ohm's law is true for Accircuits and the current flow coursed by a voltage v can be given by: -

す=マ

Here. Vs is the Voltage Source and Is in the Source current and Vp, VL and Va the voltage acron the periston inductor and capacitor perpectively.





components	Instruments
· feriator: 1x 100 r · capacitor: 1x 1luf · Anductor: 1x 33041	1 X Bread board 1 X function brenerate 1 X digital Storage Oscillos cope (DSO) -connecting wines and Probes.

Table 7.1.

R (measured)	(Comerouved)	Xa = 1 P	Z - \\R2+x2	Z = (for 1 / R)	
1002	1 MF	13.92	101.26	9.05.	

Table 1:2.

	V Peak (Theory)	(Theory)	Delay Delay OT (Practical	Peak Practical	& (Practical) &TXFX360	y. Diff	N.D.H
1 vc	WA TO DEV	86°	80024us	467.5mV	86.4	0.47%.	6.5%.
1000	5.2 ME 3.1	180	1	The second secon	18	oy.	0.55%

Logic Etrevit Inglemented wing Seelen

Toble: 13. may To mountain a of abogain

do ton	Umaswed)	4 (measure)	(2 MfL) Q	z . SR4x2 (a)	2 · [tin x/2]
	100		20.73		11.71

To	ble 1.4		alugas"	Immorana			
	VPeak (Theory)	(theory)	"Peak (Practical	Delay 47 (Practical)	O (Amedical) DT Xf X366	v.D:33	V.Ofference
~	₹ 6com	357°	608mV	09245	357.12	0.037.	1.16Y.
VR	N405.4V	5311	5 382V	3.345	11.88	7.2%	0.33%.

Figure 3x8 decoder.

50 51 52

Teble:115.

k(2)	C(F)	4(1)	1/2 Afe (I)	Xu (Theory)	Z - VR23 x Z	$z = tan^{-1}(x/R)$
1002	BJUF	330MH	15.92	20.73	106.505	20-13

Table: 1.6

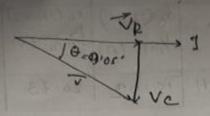
	(Practical)	(Practical)	(Practical)		
VL	820 mV	\$28.3US	101.88		
VR	6.06V	6.06 W	10.08 4 30.		
Vc	475.028mV	2743	97.200		

Quantion - Answers:

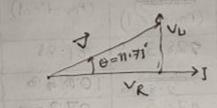
On step 6 we have used a Math function to obtain the voltage drop in the resisten by at substituting Vc from Vs. It we'd switched the position of resister & capacitor then, we would get the voltage drop across the capacitor again through Math function of ChI-Ch2.

house disperse for the circuiti

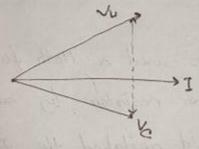
Phasos diagram for RC elecuité



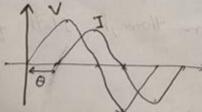
> Phasors diagram for Rt circuit:



- Phason d'agram for RLC circuit:

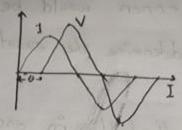


11) For Series Ru circuit;



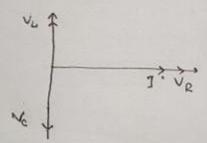
to, if we increas the frequency here asper (T=)

I will get smaller which will reduce the of eventually.



In this case, we can see current leads the voltage by O. So, if we increase. Of frequency the leading angle avoid decrease.

For series RLC Circuit:



Hone, when xe > X4, voltage will lag the cerrent.

dey O.

And for (xe(X4), voltage will lead the current ley O.

By isomraising the frequency we can decrease the angle

0.

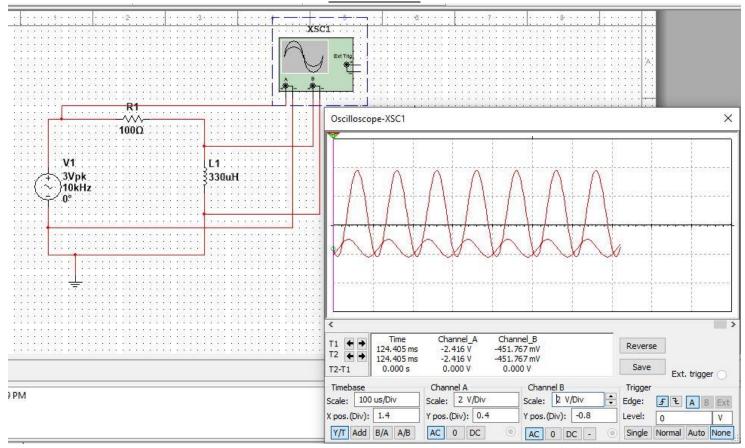
1 As we have completed software simulation sue to pandemic, we did not noticed man a huge difference between theoretical and practical values. Rather. it was an acceptable differences error. The course that may be for this error would be: @ We couldn't determine the exact peak values using curson. 19 There was a fluctuation in oncilloscope values. O Unavoidable human error.

Due to pandemic, we have completed the lab in online. Through software simulation we've completed the circuit & measured the value. The measurement procedure was a bit complex best we've learned from youtube & i honourable imptructor. As, the experiment was done in software thus, value of the component was a some as theory & our

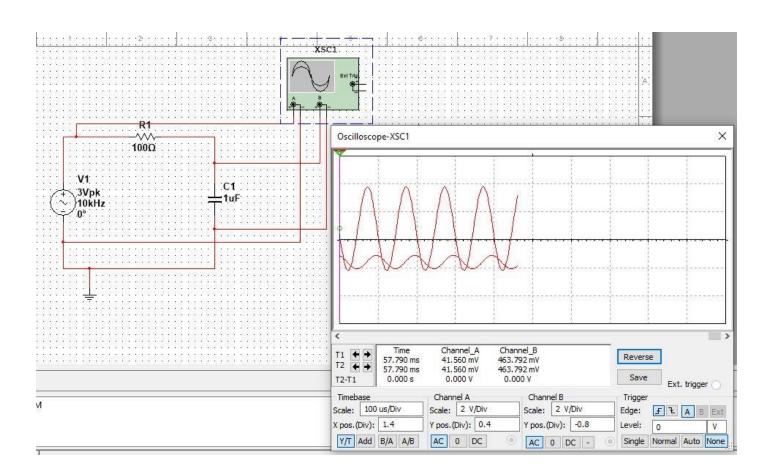
Discussion;

measured cealure was set had also minimum parcentage of

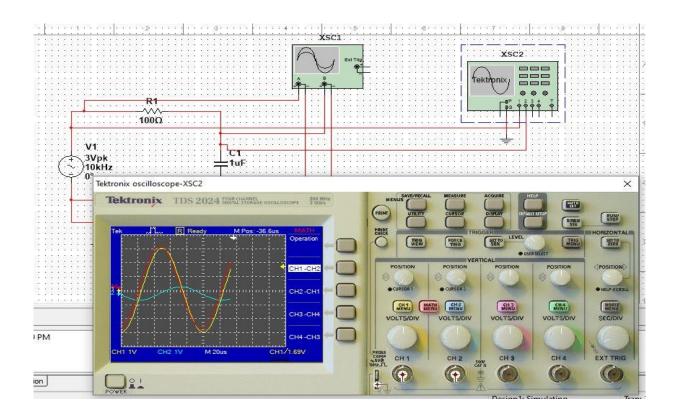
RL Circuit



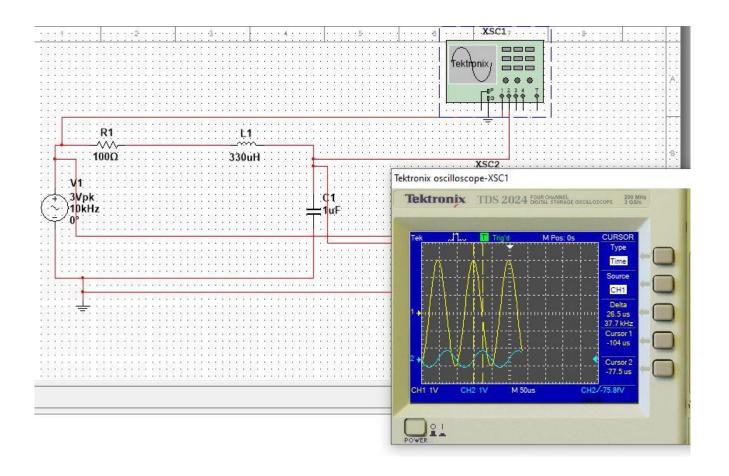
RC Circuit



Math Generated Signal in RC Circuit



Calculating Del-T for RLC Circuit:



Measuring Del-T for Inductor in RLC Series Circuit

