



**North South University**  
Department of Electrical & Computer Engineering

**LAB REPORT**

Course Name: CSE231L

Section: 10

Experiment Number: **04**

Experiment Name: **Combinational Logic Design**

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Remarks:	

## Name : Combinational Logic Design

### A. Objectives :

- Design a complete minimal combinational logic system from specification to implementation.
- Minimize combinational logic circuits using Karnaugh maps.
- Learn various numerical representation systems.
- Implement circuits using canonical minimal forms.

### B. Theory :

Computers can accept only binary values whereas we usually need to work with

decimal numbers. Therefore, we must represent the decimal digits by means of a code that contains 1's and 0's in order for computers to understand the values and perform operations using them. The code most commonly used for the decimal digits is the straight binary assignment. This scheme is called binary-coded decimal and is commonly referred to as BCD. A decimal number in BCD is the same as its equivalent binary number only when the number is between 0 and 9.

Excess-3 is another decimal code in which each coded combination is obtained from the corresponding binary value plus 3.

Gate-level minimization is the design task of finding an optimal gate-level implementation of the boolean functions describing a digital circuit. However, the procedure of minimization is awkward because it lacks specific rules to predict each succeeding step in the manipulative process. The map method, on the other hand, provides a simple, straightforward procedure for minimizing Boolean functions. This method may be regarded as a pictorial form of a truth table. The map method is also known as the karnaugh map or K-map.



A k-map is a diagram made up of squares with each square representing one minterm of the function that is to be minimized.

In fact, the map presents a visual diagram of all possible ways a function may be expressed in standard form. By recognizing various patterns, it is possible to derive alternative algebraic expressions for the same function, from which the simplest can be selected.

w	x	y	$\bar{z}$	A
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1

Table : B1

Figure B1 shows the minterm positions on the K-map for 4 input variables and 1 output variable.

Example :

Table B1 shows the truth table for the function  $A = w\bar{x} + \bar{x}y\bar{z} + w\bar{z} + \bar{x}\bar{y}$  where

$wxyz$  goes from binary 0 to 3.

Figure B2 shows the K-Map for the function.

We can use the K-map to minimize the function to  $A = \bar{x}\bar{y} + xyz$

$\backslash yz$	00	01	11	10
$\backslash wx$	$w\bar{y}\bar{z}$	$w\bar{y}z$	$w\bar{y}z$	$w\bar{y}\bar{z}$
00	$w\bar{y}\bar{z}$	$w\bar{y}z$	$w\bar{y}z$	$w\bar{y}\bar{z}$
01	$wx\bar{y}\bar{z}$	$wx\bar{y}z$	$wxyz$	$wxy\bar{z}$
11	$wx\bar{y}\bar{z}$	$wx\bar{y}z$	$wxyz$	$wxyz$
10	$wx\bar{y}\bar{z}$	$wx\bar{y}z$	$wxyz$	$wxyz$

$y$

$z$

Figure B1

$\backslash yz$	00	01	11	10
$\backslash wx$	1	1	0	0
00	1	1	0	0
01	0	0	0	1
11	x	x	x	x
10	1	1	x	x

$y$

$z$

Figure B2

### C. Apparatus

- + Trainer Board
- + 1x IC 4073 Triple 3-input AND gates.
- + 1x IC 4075 Triple 3-input OR gates.
- + 1x IC 7404 Hex Inverters (NOT gates).
- + 1x IC 7400 2-input NAND gates.
- + 2x IC 7408 2-input AND gates.

F. Experimental Data :

Decimal Digit	Binary Coded Decimal (BCD)				Excess - 3			
	W	X	Y	Z	A	B	C	D
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table F1 : Truth Table - BCD to Excess-3

Number of inputs bits:	4	Input variables:	WXYZ
Number of outputs bits:	4	Output variables:	ABCD.

Table F2 : System analysis.

<del>w</del>	<del>y</del>	<del>z</del>	00	01	11	10	<del>w</del>	<del>y</del>	<del>z</del>	00	01	11	10
w	00	00	0	0	0	0	00	01	11	0	1	1	1
w	01	0	1	1	1	1	01	1	0	0	0	0	0
w	11	X	X	X	X	X	11	X	X	X	X	X	X
w	10	1	1	X	X	X	10	0	1	X	X	X	X

$$F = w + xz + xy$$

$$F = x\bar{y}\bar{z} + \bar{x}z + \bar{x}y$$

<del>w</del>	<del>y</del>	<del>z</del>	00	01	11	10	<del>w</del>	<del>y</del>	<del>z</del>	00	01	11	10
w	00	1	0	1	0	0	00	1	0	0	0	1	1
w	01	1	0	1	0	0	01	1	0	0	1	0	1
w	11	X	X	X	X	X	11	X	X	X	X	X	X
w	10	1	0	X	X	X	10	1	0	X	X	X	X

~~w~~

$$F = \bar{y}\bar{z} + yz$$

~~w~~

$$F = \bar{y}z + y\bar{z}$$

$$= z(\bar{y} + y)$$

$$= \bar{z} \cdot 1 \quad [\because \bar{y} + y = 1]$$

$$\therefore A = W + XZ + XY.$$

$$\therefore B = \bar{X}\bar{Y}\bar{Z} + \bar{X}Z + \bar{X}Y.$$

$$\therefore C = \bar{Y}\bar{Z} + Y\bar{Z}.$$

$$\therefore D = \bar{Z}.$$

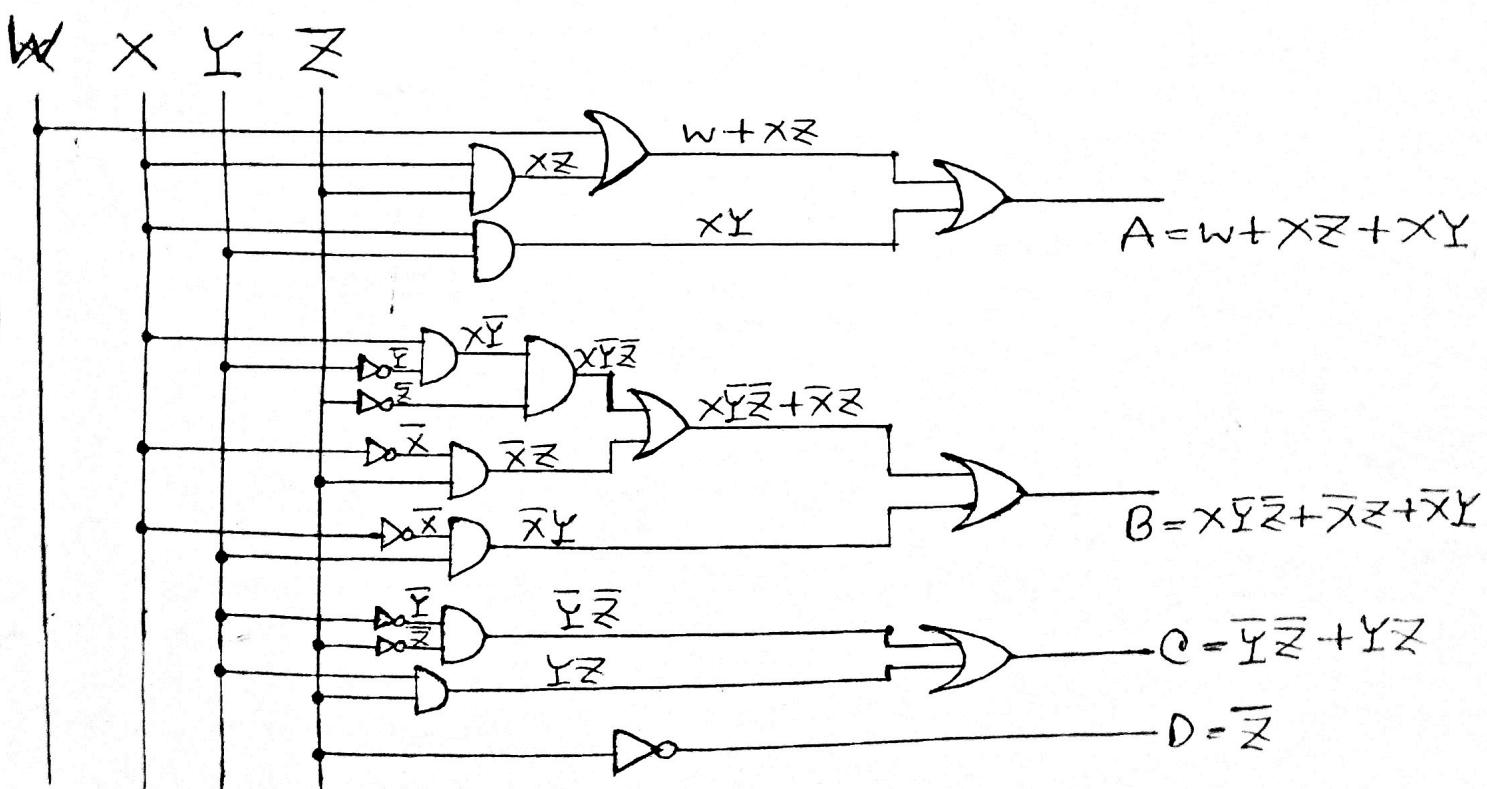


Figure F2 : Minimal 1st Canonical circuit of BCD to Encm-3 converter.

Figure F3: Minimal universal gate implementation of BCD to Exor-3 converter.

