CSE 231 Lab | Digital Logic Design Lab

Course Faculty:	Dr. Mohammad Monirujjaman Khan (KMM)
Lab Instructor:	Tasmina Imam
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Office Room:	TBA
Office Hours:	T: 11:20- 5:50; T: 2:40- 5:50
Lab Section:	06

Required Software Knowledge: Logisim

Lab Outline

Lab 1	Digital Logic Gates and Boolean Functions
Lab 2	Universal Logic Gates
Lab 3	Combinational Logic Design (Canonical Form)
Lab 4	Combinational Logic Design (K Maps)
Lab 5	Binary Arithmetic
Lab 6	Mux and Decoder
Lab 7	Flip-Flops – Registers
Lab 8	Synchronous Sequential Circuits
Final Exam	

Marks Distribution

Attendance and Lab Performance:	20 %
Lab Report:	20 %
Quiz	10%
Viva	5 %
Final Setup & Simulation Test	20 %
Final Exam:	20 %

RULES:

- Do not talk during the class.
- If any lab is missed, one will get 0% in *Attendance, Lab performance* and *Lab report Submission* for that particular lab class.
- Use of mobile phones during the class is strictly prohibited.
- Lab Report copied from others will be marked negatively.
- You must bring printed lab manuals to the class.
- No Late Submissions will be accepted whatever may be the reason.
- Only use the cover page as instructed in the class, using cover page of any other form will lead to rejection of your submission.
- All information in the cover page must be typed; handwritten cover pages will be rejected.
- All submissions are due at the beginning of the class.
- Ensure that your group prints all necessary materials well ahead of the class.
- Grading will be done according to NSU Grading Policy.