North South University

Department of Electrical & Computer Engineering

LAB REPORT

Course Name: CSE231L

Section: 10

Experiment Number: **07**

Experiment Name: **Introduction to Multiplexer & Decoder**

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Group Number: N/A

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Remarks:	

Name : Introduction to Multiplexer & Decoder.

Objectives :

+ Familiarize with the analysis of Multiplexer & Decoder circuits.

+ Learn the implementation of Multiplexer & Decoder using gates.

+ Verify the Multiplexer & Decoder with the Truth Table.

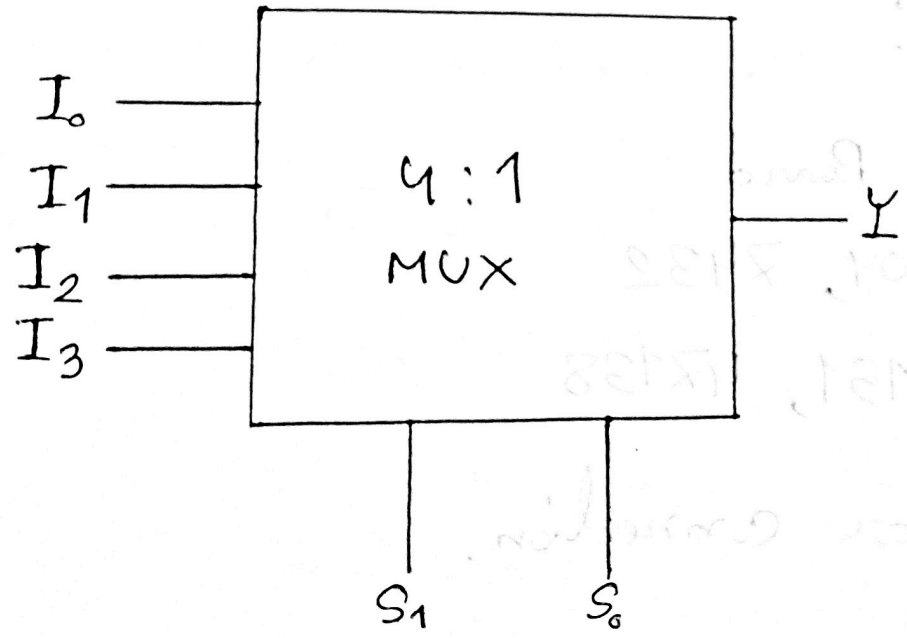
Apparatus :

+ Trainer Board
+ IC 7404, 7432
+ IC 74151, 47138
+ Wires for connection.

Theory:

Multiplexers have the most important attributions of digital circuitry in communication hardware. These digital switches enable us to achieve the communication network we have today. In this experiment the students will have to construct MUX (multiplexers) with simple logic gates.

JOB 1: 4 to 1 MUX

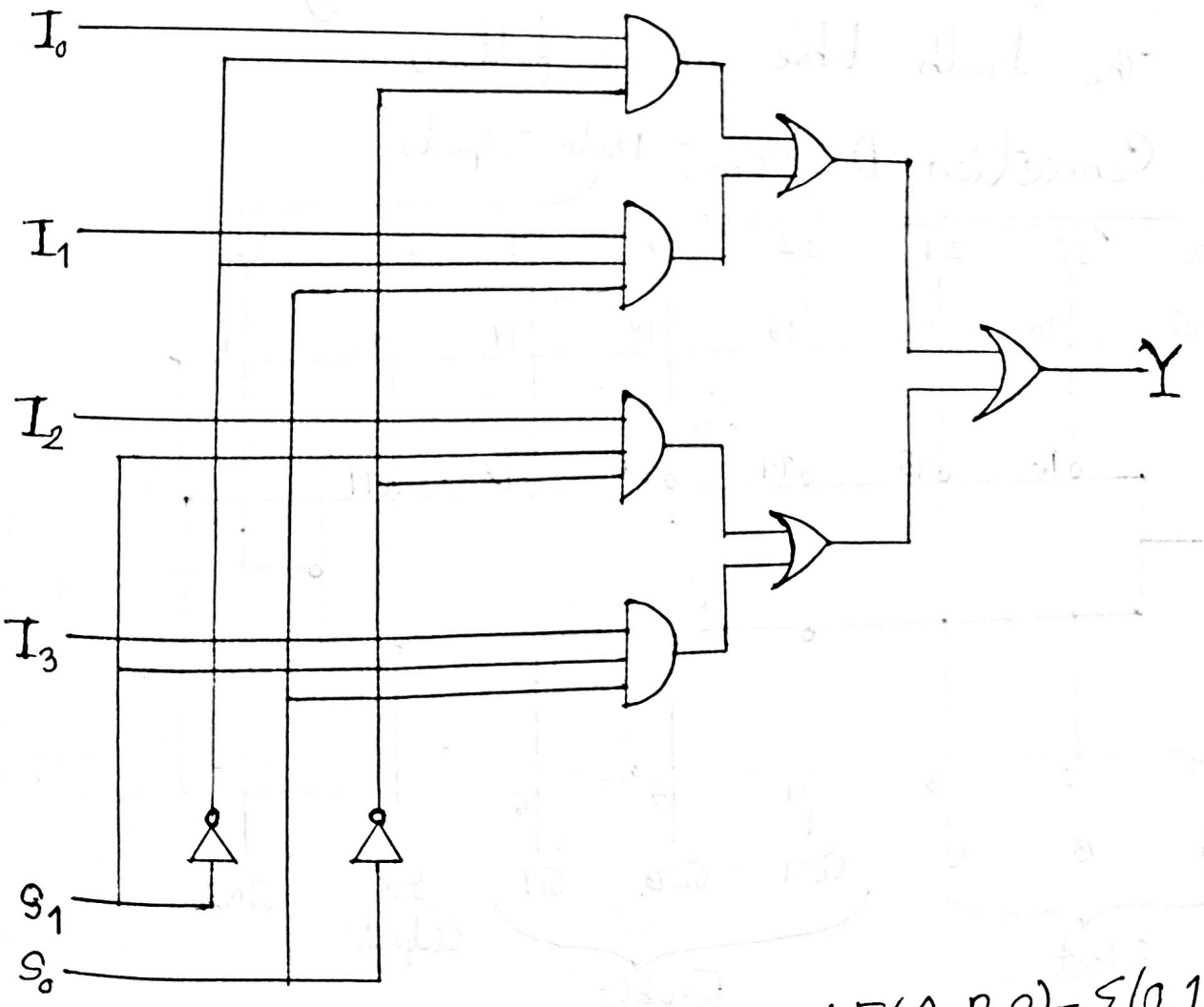


Truth Table:

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = I_0 \bar{S}_1 \bar{S}_0 + I_1 \bar{S}_1 S_0 + I_2 S_1 \bar{S}_0 + I_3 S_1 S_0$$

Circuit digram:

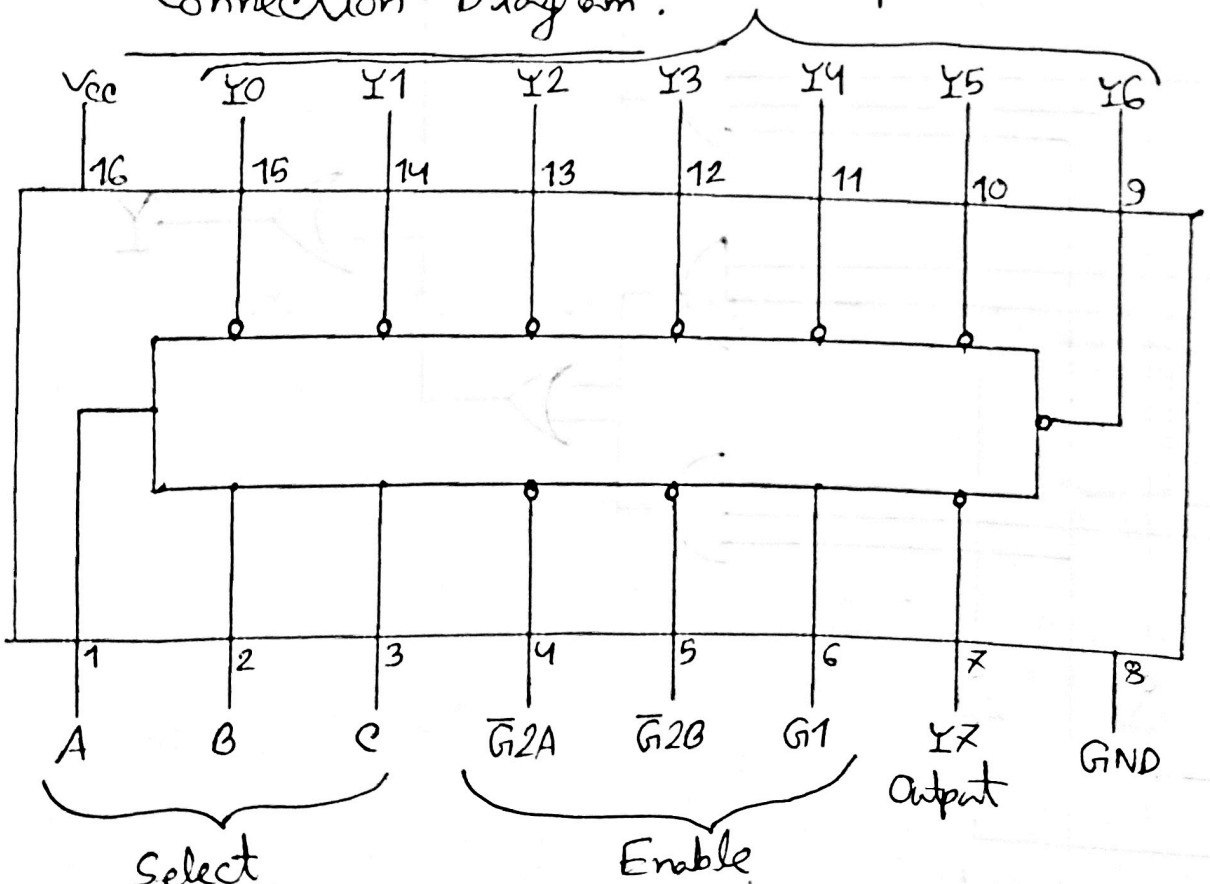


Implement the function using 4:1 MUX; $F(A,B,C) = \Sigma(0,1,5,7)$
[take A as input]

JOB 3: 3 to 8 line Decoder:

It uses all AND gates and therefore, the outputs are active-high. For active-low outputs, NAND gates are used. It has 3 inputs lines and 8 output lines. It is also called as binary to octal decoder it takes a 3bit binary input code and activates one of the 8(octal) outputs corresponding to that code. The truth table is as follows:

Connection Diagram:



Function Table:

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$ (Note 1)	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1 : $\overline{G2} = \overline{G2A} + \overline{G2B}$

Assignment :

$F(A, B, C, D) = \Sigma(0, 1, 3, 5, 8, 9, 14, 15)$

[take B as input]

A	B	C	D	F	Data Inputs
0	0	0	0	1	$I_0 = 1$
0	0	0	1	1	
0	0	1	0	0	$I_1 = 1$
0	0	1	1	1	
0	1	0	0	0	$I_2 = 0$
0	1	0	1	1	
0	1	1	0	0	$I_3 = \bar{B}$
0	1	1	1	0	
1	0	0	0	1	$I_4 = 0$
1	0	0	1	1	
1	0	1	0	0	$I_5 = \bar{B}$
1	0	1	1	0	
1	1	0	0	0	$I_6 = B$
1	1	0	1	0	
1	1	1	0	1	$I_7 = B$
1	1	1	1	1	

Table : Truth table for 8 : 1 MUX.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{B}$	(0)	(1)	2	(3)	4	(5)	6	7
B	(8)	(9)	10	11	12	13	(14)	(15)
	1	1	0	$\bar{B}$	0	$\bar{B}$	B	B

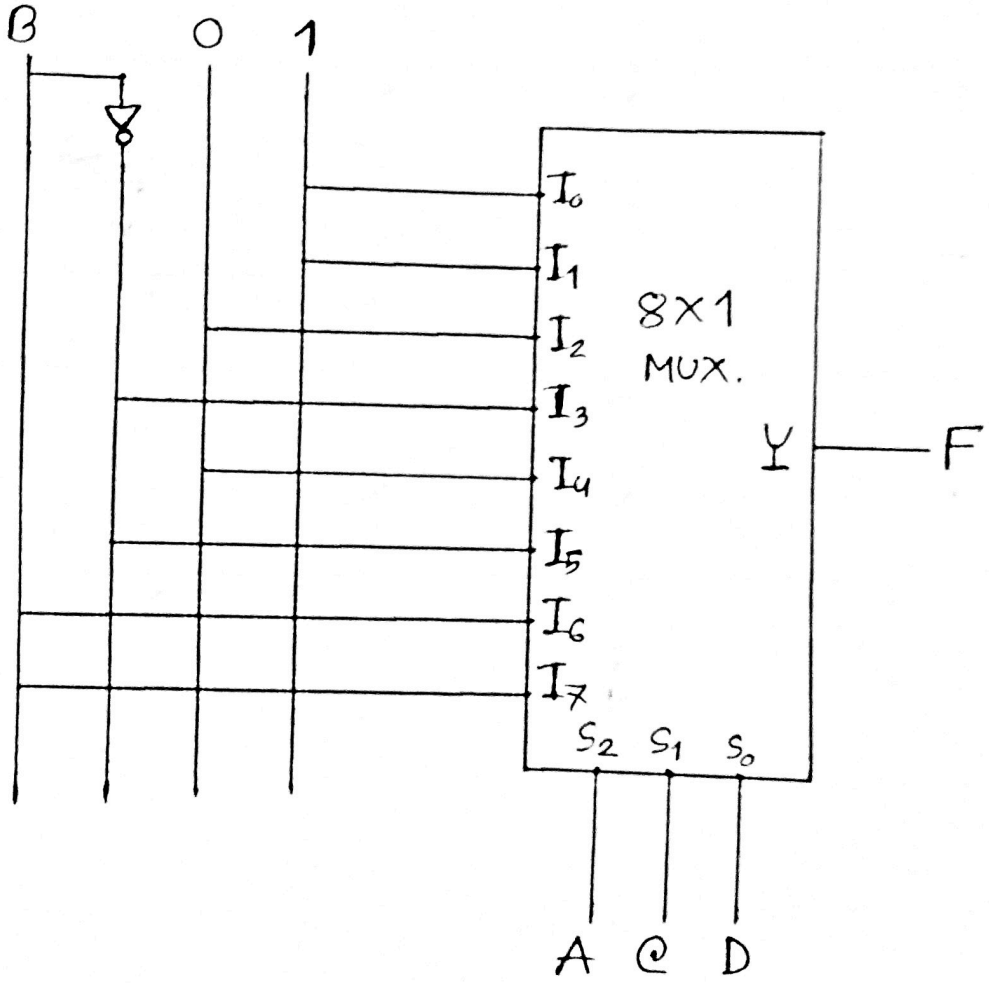


Figure : Logic diagram for 8:1 MUX.