

ASSIGNMENT - 08

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Course : CSE231

Section : 10.

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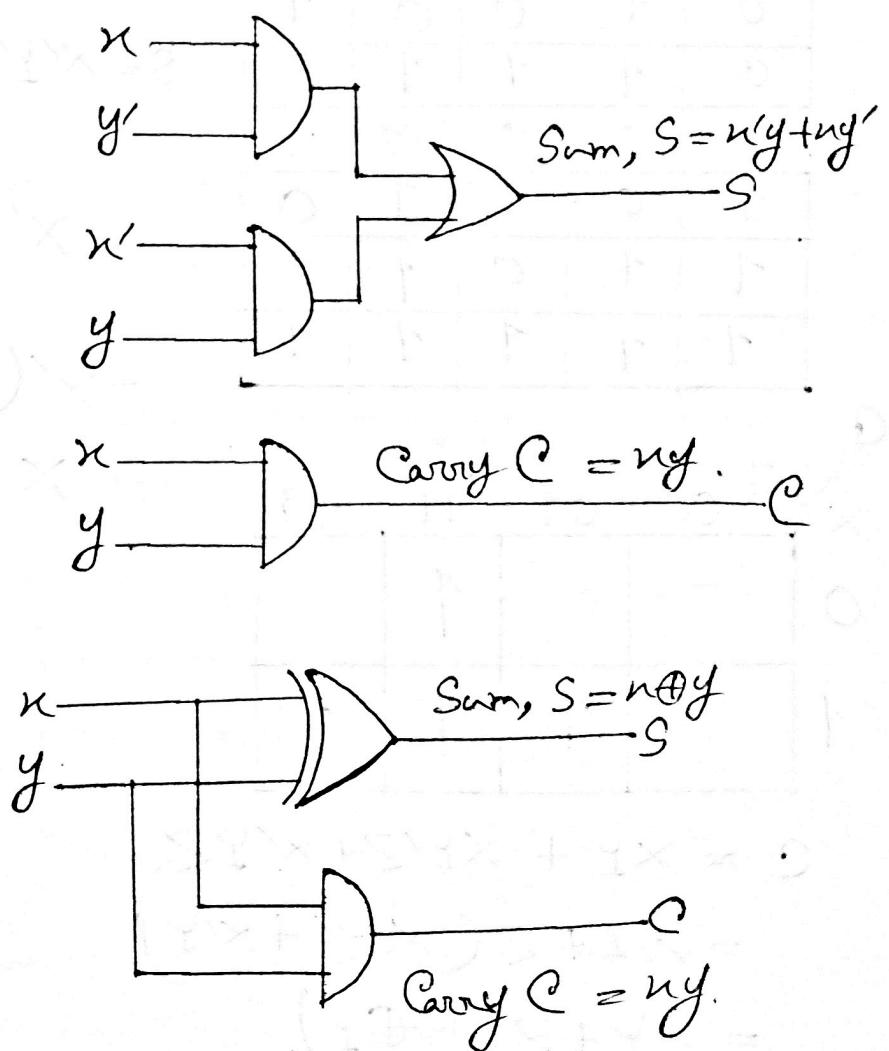
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Binary Adder-Subtractor

- A combinational circuit that performs the addition of two bits is called a half adder.
- The truth table for the half adder is listed below:

Truth table - Half Adder

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Full-Adder

* Performs the addition of three bits (two significant bits and a previous carry).

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

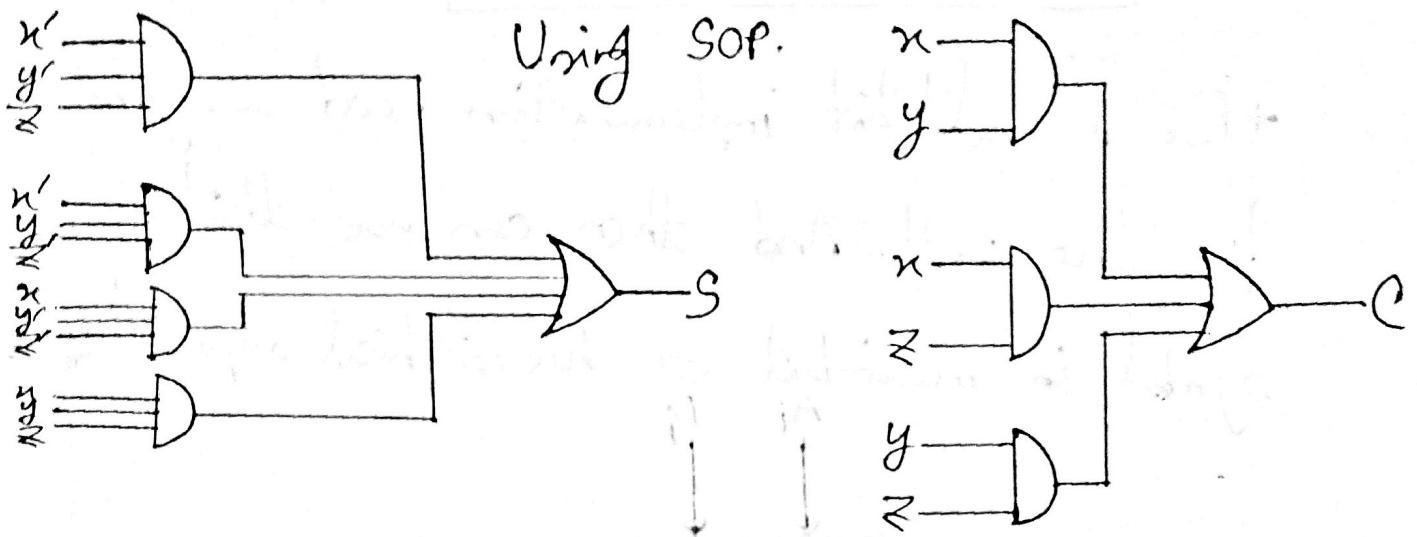
X Y Z	00	01	11	10
S	0	1	1	1
	1	1	1	

$$\begin{aligned}
 S &= X'Y'Z + X'YZ' + XY'Z' + \\
 &\quad XYZ \\
 &= X'(Y'Z + YZ') + X(YZ + \\
 &\quad Y'Z') \\
 &= X'(Y \oplus Z) + X(Y \oplus Z) \\
 &= X \oplus Y \oplus Z.
 \end{aligned}$$

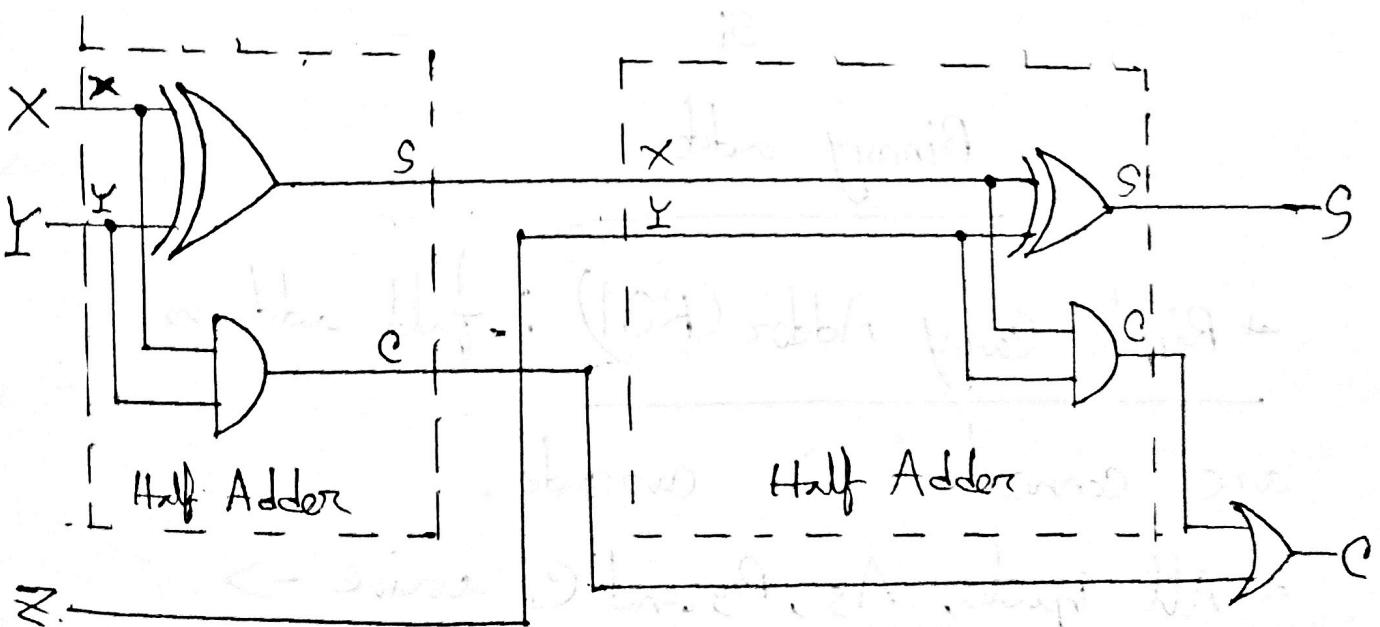
X Y Z	00	01	11	10
C			1	
		1	1	1

$$\begin{aligned}
 C &= XY + XYZ + X'YZ \\
 &= XY + Z(XY + X'Y) \\
 &= XY + Z(X \oplus Y).
 \end{aligned}$$

Full adder Implementation

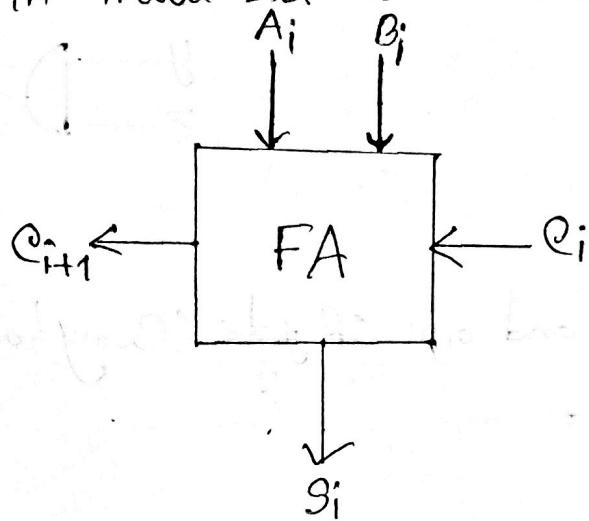


Using two half adders and one OR gate (Carry Look-Ahead adder)



Full Adder Symbol

+ For a multibit implementation need a symbol for the unit. And then can use that symbol in multi-bit or hierarchical representations.



Binary adder

+ Ripple Carry Adder (RCA) : full adders

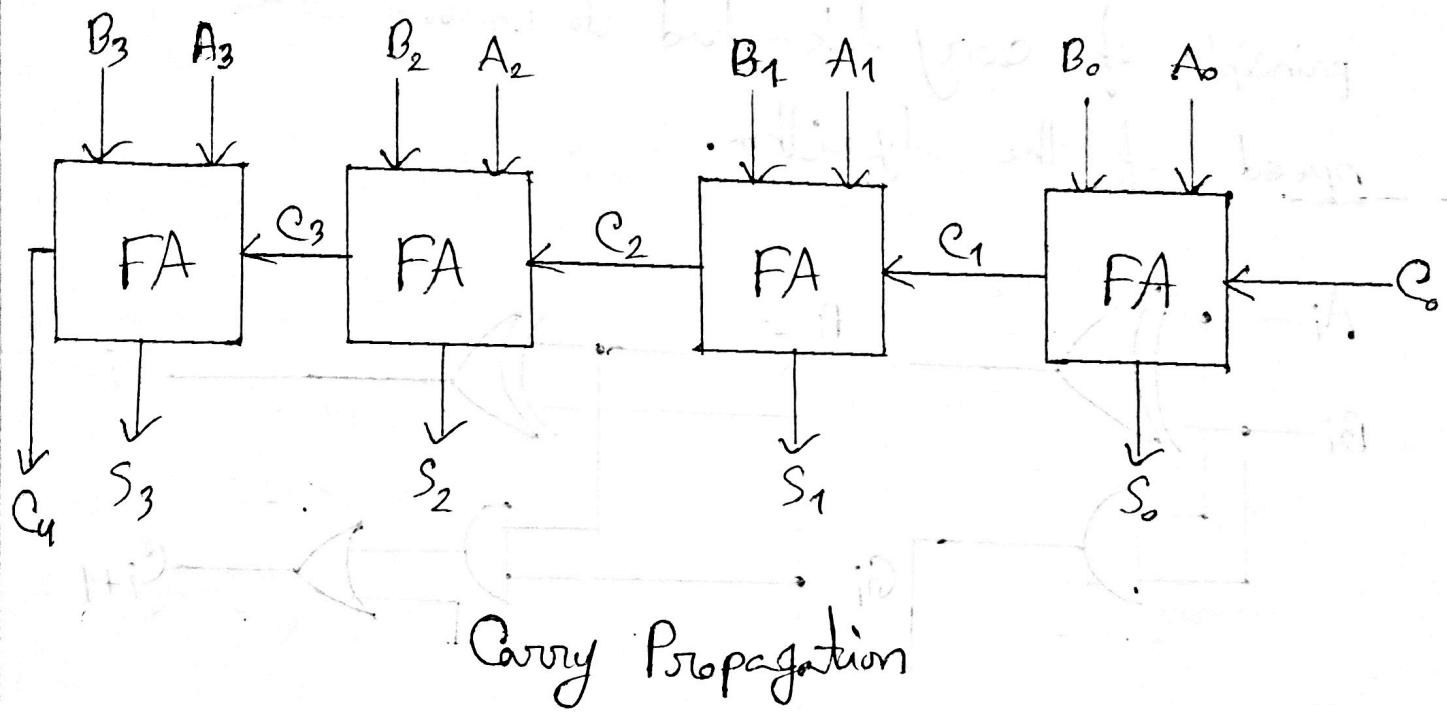
are connected in cascade.

All inputs, A_3, B_3 and C_0 arrive \rightarrow

C_1 becomes valid $\rightarrow C_2$ becomes valid $\rightarrow C_3$

becomes valid $\rightarrow C_4$ becomes valid.

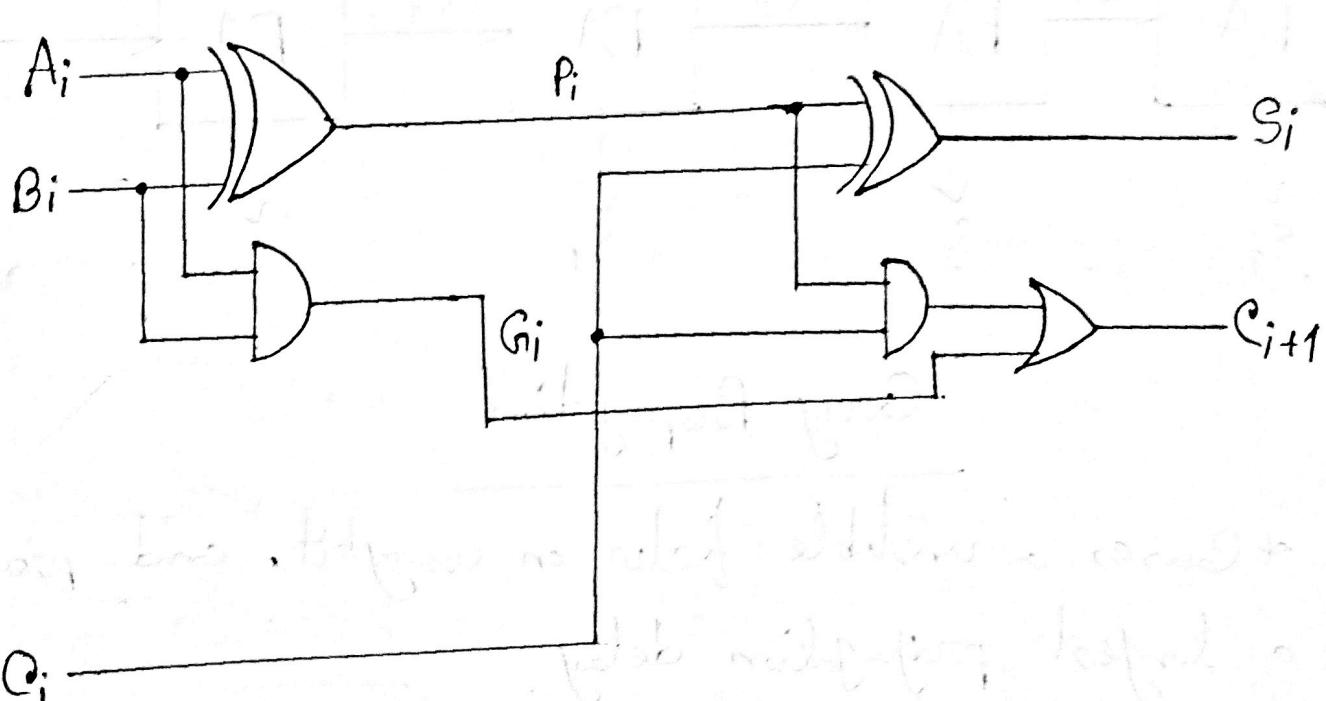
Subscript i:	3	2	1	0	
Input carry	0	1	1	0	c_i
Augend	1	0	1	1	A_i
Addend	0	0	1	1	B_i
Sum	1	1	1	0	S_i
Output carry	0	0	1	1	c_{i+1}



- * Causes an unstable factor on carry bit, and produces a largest propagation delay.
- * The signal from c_1 to the output carry c_{i+1} propagates through an AND and OR gates, so, for an n-bit RCA, there are $2n$ gate levels for the carry to propagate from input to output.

* Because the propagation delay will affect the output signals on different time, so the signals are given enough time to get the precise and stable outputs.

* The most widely used technique employs the principle of carry look-ahead to improve the speed of the algorithm.



Boolean functions of CLA-Adder

$$P_i = A_i \oplus B_i \quad \text{steady state value}$$

$$G_i = A_i B_i \quad \text{steady state value}$$

Output sum and carry

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

G_i : carry generate P_i : carry propagate.

C_o = input carry.

$$C_1 = G_0 + P_0 C_o$$

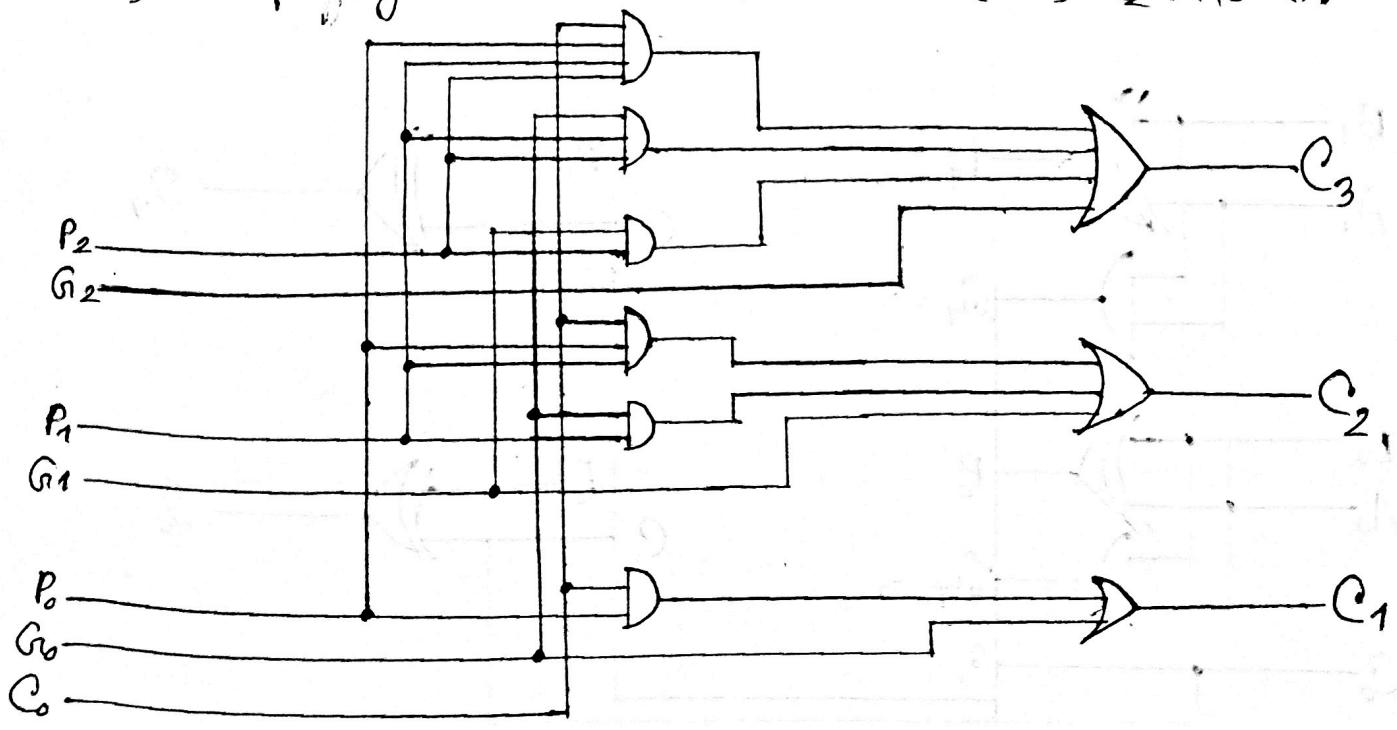
$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0 + P_1 P_0 C_o$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_o$$

$+ C_3$ does not have to wait for C_2 and C_1 to propagate.

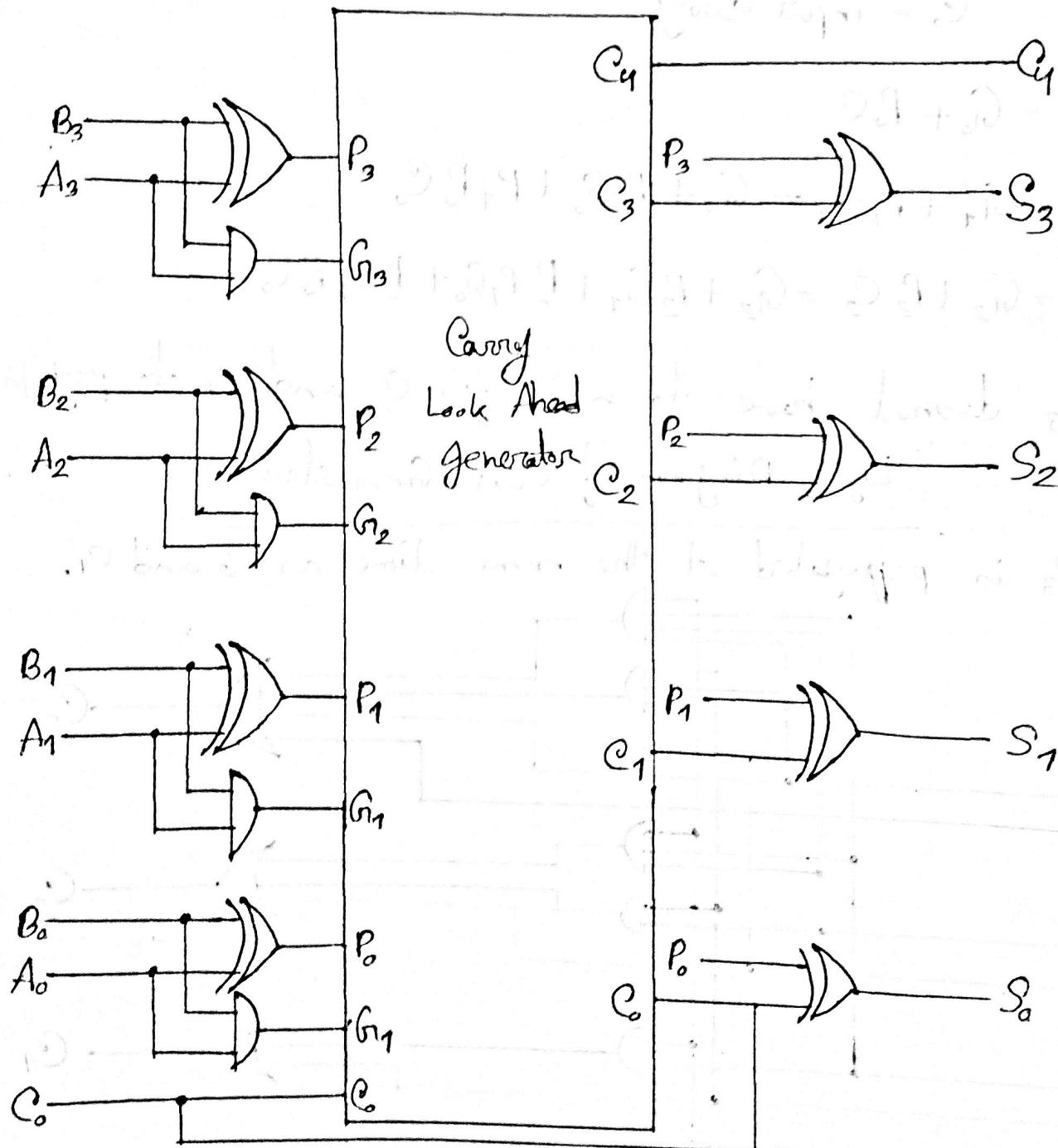
Logic Diagram of PLA Generator ..

* C_3 is propagated at the same time as C_2 and C_1 .



4-bit CLA-Adder

* Delay time of nbit CLAA = $xOR + (AND + OR) + XOR$.



Binary Adder-Subtractor

$M = 1 \rightarrow \text{subtractor}$;

$M = 0 \rightarrow \text{adder}$.

