NORTH SOUTH UNIVERSITY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

Experiment No: 06

Name of the Experiment: The BJT Biasing Circuits.

Objective: Study of the fixed biased and voltage divider biasing circuits and compare their stability.

Theory:

In analog circuits, the BJT is operated in the active mode. For this purpose a biasing circuit is employed. A transistor is biased by supply voltages and resistors; that is, they establish a specific set of dc terminal voltages and currents, thus determining a point of active-mode operation (called the quiescent point or Q point). After setting the DC operating point for the circuit, when ac signal is applied, usually the quiescent values are unchanged, and the ac signal is superimposed over dc and causes an output signal with the same waveform but with the DC shift determined by the Q-point. Now the question is where to set the Q-point in the BJT characteristics curve? If the operating point is set in the middle, you get a faithful reproduction of the input signal. If the Q-point is set closer to saturation region, it results in clipping of positive portion of the output, whereas for Q-point set closer to cut-off region results in clipping of a portion of negative part of output. In many amplifier circuits, like class B and Class C amplifiers the Q-point is set such that it results in clipping of output. For full output swing, Q-point has to be set in the middle.

There are different types of biasing circuits. However, in the laboratory, we will study only the fixed bias and voltage-divider bias circuit. We will try setting the Q-point in three positions: Cut-off, Center of active region, and saturation, and see how the output signal changes. Moreover, we will find β for

Next, we will simulate common emitter voltage divider circuit and fixed biased circuit and see which one is more stable. Fixed biased circuits are known to be sensitive with variation of β, whereas voltage divider bias circuits are quite stable.

Experimental Setup (PSpice):

- **DC ANALYSIS:**

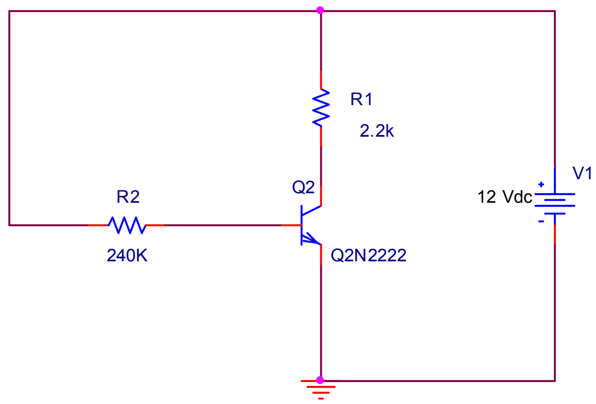


Fig1: Fixed Biased Circuit

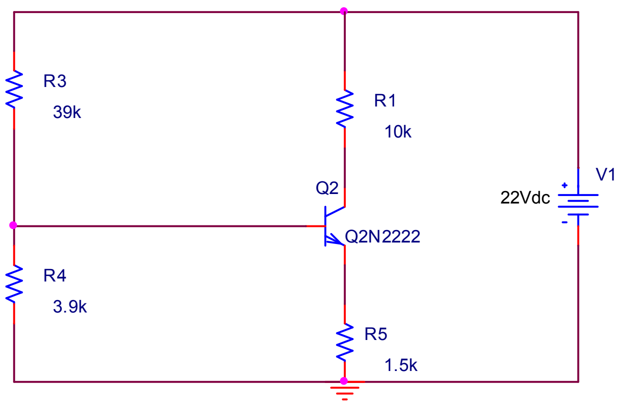


Fig2: Voltage Divider Bias

Procedure:

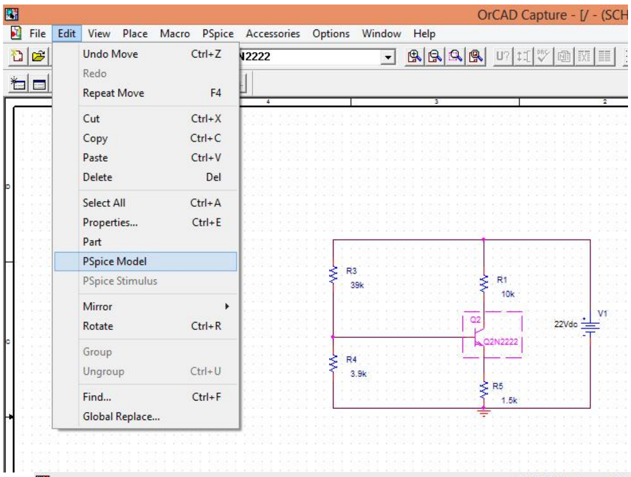
1. Construct Fig 1.
2. Do Bias Point Analysis for Beta: 255.9 (which is the default value of beta for Q2N2222) and note down the I_C and V_{CE}in table below.
3. Repeat for Beta = 50.
4. Repeat for Fig 2.
5. Compare the sensitivity of circuits with the changes in Beta.

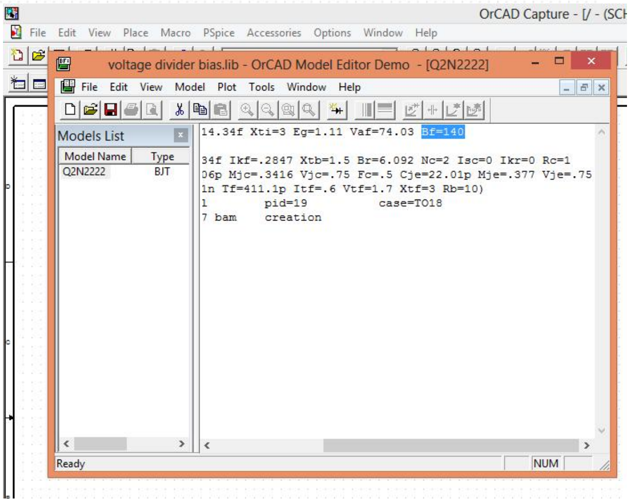
Data Collection:

FIXED BIASED		
Beta	**I_C (mA)**	**V_{CE} (V) [$=V_C$ as $V_E = 0$]**
255.9		
50		

Voltage Divider biased		
Beta	I_C **(mA)**	V_{CE} **(V) [** V_C **-** V_E **]**
255.9		
50		

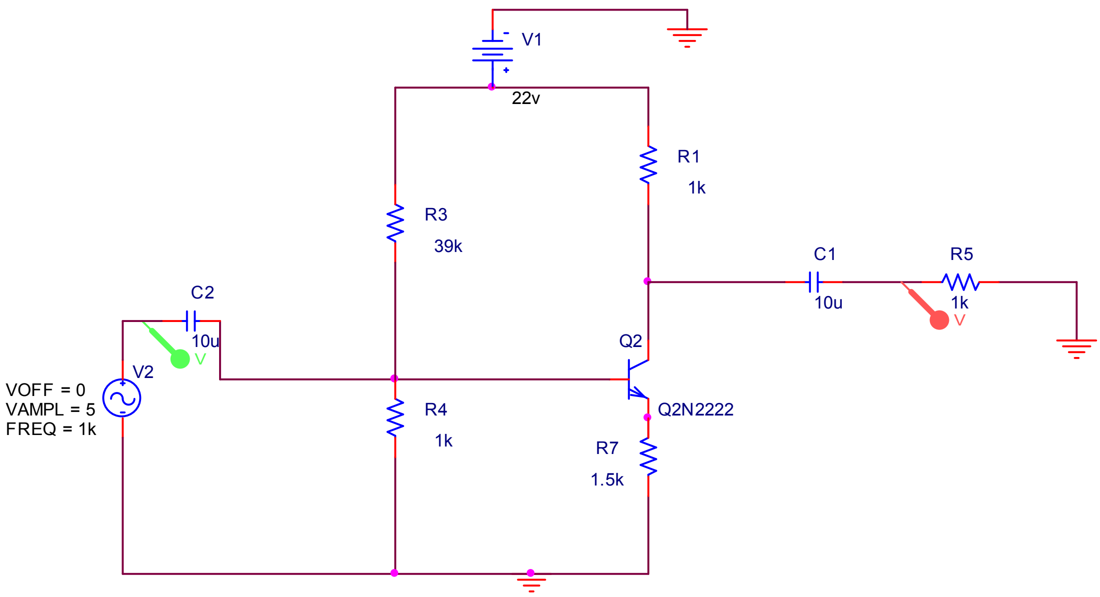
Follow the steps to change the value of Beta of a transistor:





** MAKE SURE TO SAVE AFTER CHANGING Bf

- **Transient Analysis**



Procedure:

1. Setup the circuit for Transient Analysis.
2. Calculate the load line. (Isat and Vsat)
3. Run the simulation and observe the waveform. Note down IB, IC,VCE.
4. Take screenshot of the graph.
5. Continue for different values of R4 .

Data Collection:

Signature of instructor:

$I_{sat} = \frac{Vcc}{Rc+R_E} =$

$V_{sat} = Vcc =$

R4	I_B	I_C	V_{CE}	Waveform
1k				
3.9k				
5k				
20k				

35k				
40k				
50k				

Report:

1. Which resistor values set the Q-point in cutt off, Center, and Saturation?
2. How did your waveform change as your Q-point changed?
3. From PSpice simulation results, explain which biasing circuit shows better stability?