Lab3:Combinational Logic Design

A. Objectives

- Become familiarized with the analysis of combinational logic networks.
- Learn the implementation of networks using the two canonical forms.

B. Theory

Minterms and Maxterms:
A binary variable may appear either in its normal form (x) or in its complement form (x'). Now consider two binary variables x and y combined with an AND operation. Since each variable may appear in either form, there are four possible combinations: x'y', x'y, xy', and xy. Each of these four AND terms is called a minterm, or a standard product. If we have n variables, they can be combined to form 2^nminterms.

In a similar fashion, n variables forming an OR term, with each variable being primed or unprimed, provide 2^n possible combinations, called maxterms, or standard sums.

The four minterms and maxterms for 2 variables, together with symbolic designations, are listed in **Table 1**.

		Minterms		**Maxterms**	
x	**y**	**Term**	**Designation**	**Term**	**Designation**
0	0	$x'y'$	m_0	$x + y$	M_0
0	1	$x'y$	m_1	$x + y'$	M_1
1	0	xy'	m_2	$x' + y$	M_2
1	1	xy	m_3	$x' + y'$	M_3

Table 1

It is important to note that the maxterm with subscript *j* is a complement of the minterm with the same subscript *j* and vice versa.

That is, $\mathbf{m'_j = M_j}$

Canonical Forms:
Boolean functions expressed as a sum of minterms or product of maxterms are said to be in **1stCanonical Form**and **2nd Canonical Form** respectively**.** Functions in their canonical form can also be expressed in a brief notation. For example, the function **F = x'y' + xy'**(1st canonical form) can be expressed as **F(x,y) = Σ(0,2)** and the function **X = (A+B)(A+B')**(2nd canonical form) can be expressed as **X(A,B) = Π(0,1)**. The numbers following the sum and product symbols are the indices of the minterms and maxterms of the respective functions.

C. Apparatus

- Trainer Board
- 1 x IC 7411 Triple 3-input AND gates
- 2 x IC 4075 Triple 3-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)

D. Procedure

1. Write down all the min terms and max terms of three inputs ABC in Table F.1.
2. Use the given truth table to express the function F in 1st and 2nd Canonical Forms in in Table F.2. Write down both the brief and full expressions of the sum of minterms and product of maxterms expressions of the function.
3. Draw the circuits for the 1st and 2nd canonical forms of the function in Figure F.1, clearly indicating the pin numbers corresponding to the relevant ICs.
4. Construct the 1st canonical form of the circuit and test it with the truth table.
   i. Connect one min term at a time and check its output.
   ii. Once all min terms have been connected and verified, OR the min terms for the function output.
5. Construct the 2nd canonical form of the circuit and test it with the truth table.
   i. Connect one max term at a time and check its output.
   ii. Once all max terms have been connected and verified, AND the max terms for the function output.

E. Questions

1) What is meant by 'first canonical form'? Is the following expression in the first canonical form? Explain your answer.

$$F = AB' + ABC'$$

2) Use Logisim to simulate the **2nd canonical form** of the circuit in **Figure F.1** of the data sheet. Attach a printout of the Logisim circuit screenshot and truth table screenshot (on a single page) to your lab report.

3) Draw the IC diagram for the **1st canonical form** of the circuit in **Figure F.1** of the data sheet. All the ICs used must be labeled properly. The internal gates and pin numbers of the ICs must be shown and the wiring must be tidy and decipherable.

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Data Sheet: Instructor's Signature: ....

Section:	Group No.:	Date:

Input Reference	*A B C*	*F*	Min term	Max term
0	0 0 0	0		
1	0 0 1	1		
2	0 1 0	1		
3	0 1 1	0		
4	1 0 0	0		
5	1 0 1	0		
6	1 1 0	1		
7	1 1 1	0		

Table F.1 Truth table to a combinational circuit

	Shorthand Notation	Function
1st Canonical Form	$F = \Sigma$	$F =$
2nd Canonical Form	$F = \Pi$	$F =$

Table F.2 1st and 2nd canonical forms of the combinational circuit of Table F.1

1st Canonical Form
2nd Canonical Form

Figure F.1 1st and 2nd canonical circuit diagrams of the combinational circuit of Table F.1