



North South University

CSE231L

Experiment # 4

Name of Experiment: BCD to Excess-3 Converter

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Section: 13

Group: 3

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Objectives

- We have to learn various numerical representation systems.
- We have to design a complete minimal combinational logic system from specification to implementation.
- We have to minimize combinational logic circuits using Karnaugh maps.
- We have to implement circuits using minimal forms.

Equipments

- Trainer Board.
- 2x IC 7411 Triple 3-input AND gates.
- 2x IC 4075 Triple 3-input OR gates.
- 1x IC 7404 Hex Inverters (NOT gates)

Theory

A combinational circuit consists of logic gates whose outputs at any time are determined by the circuit input values. Each input and output variable is a binary variable. One possible binary value at the

output for each input combination. A truth table or boolean functions can be used to specify input output relation. The circuit operates is clearly expressed. Derivation of the truth table or the Boolean equations that define the relationship between inputs and outputs. K-map optimization of the truth table and draw the corresponding logic diagram. ~~Transform~~ Transform the logic diagram to a new diagram using the available implementation technology. Gate level minimization is the design test of finding an optimal gate level implementation of the boolean functions describing a digital circuit. A k-map is a diagram made by squares, with each square representing one minterm of the function that is to be minimized. Draw a logic diagram that represents the simplified boolean expression. Verify the design by analysing or simulating the circuit.

Circuit diagram

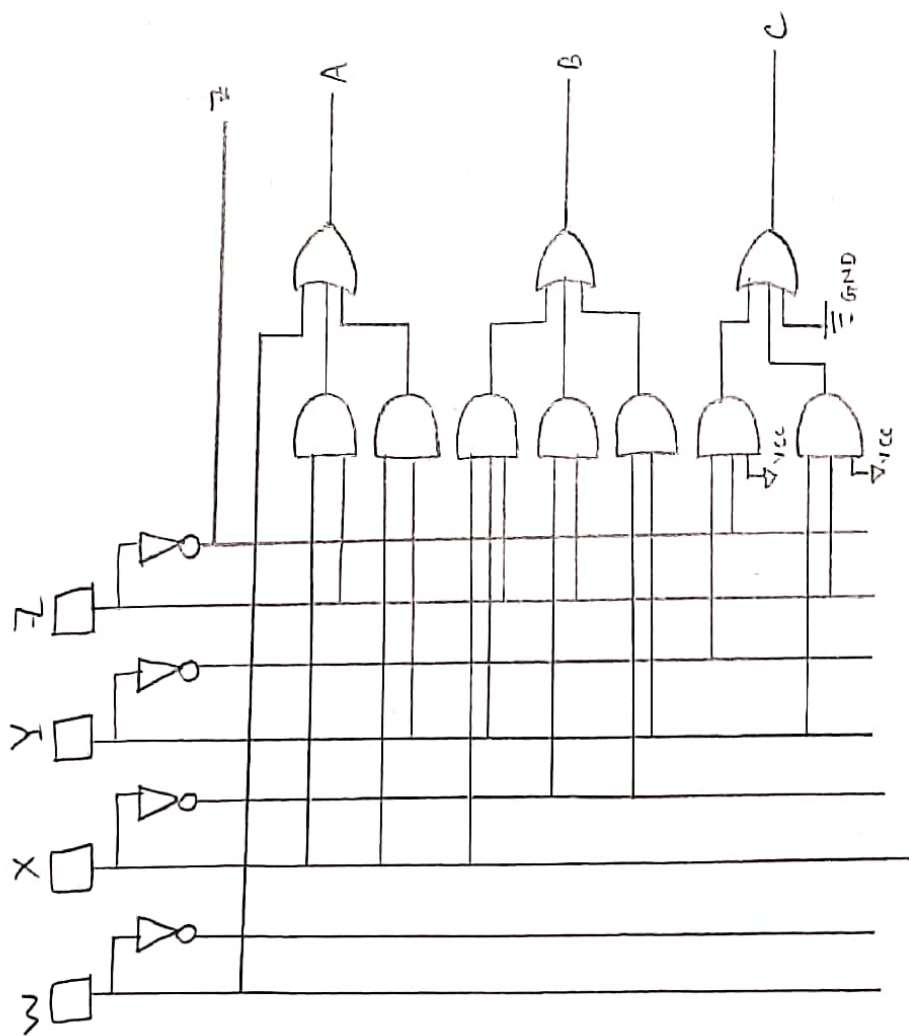


Figure F2: Minimal logic circuit of BCD to Excess-3 converter

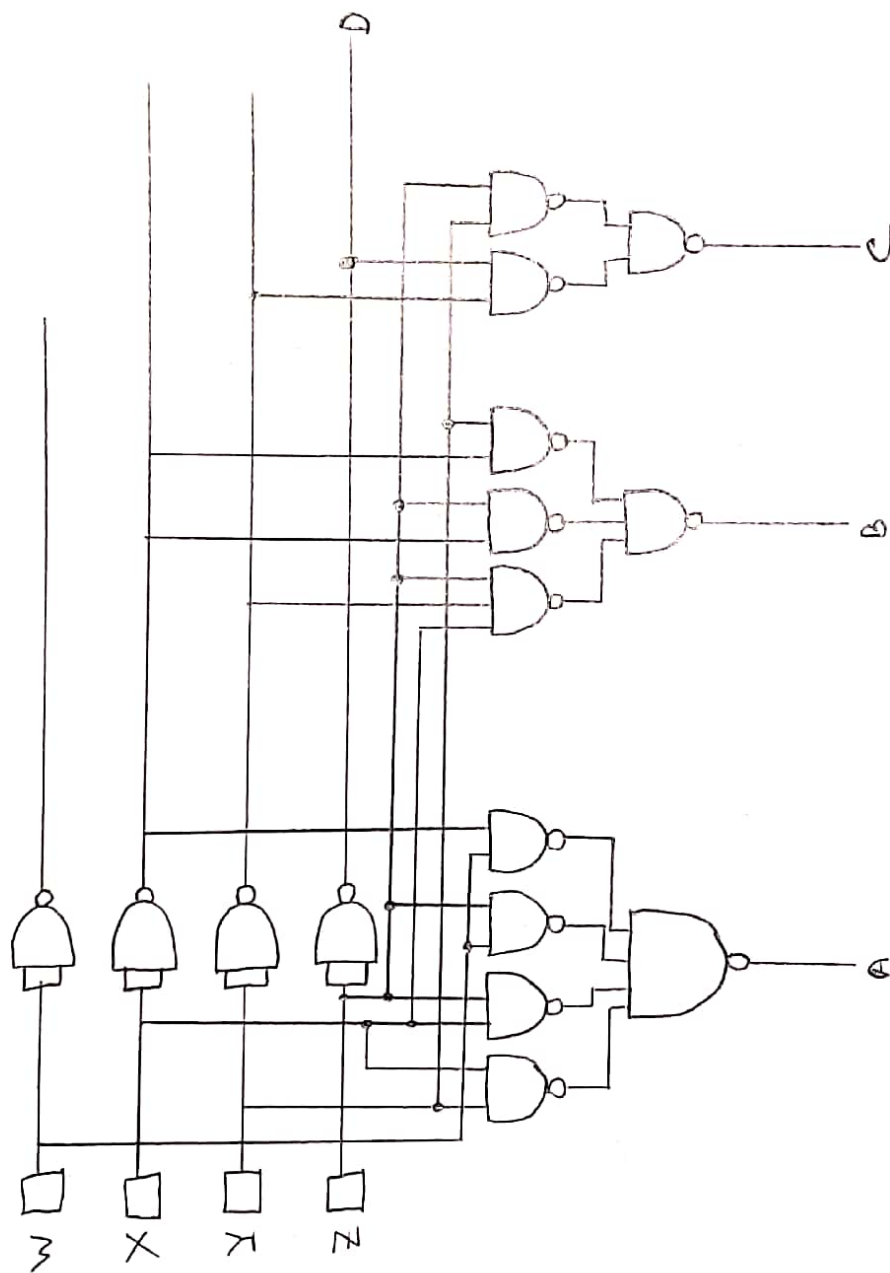


Figure F3: Minimal NAND gate implementation of BCD to Excess-3 converter

Table 8.3

Source Topic	Strongly agree				Disagree			
	1	2	3	4	5	6	7	8
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								
16								
17								
18								
19								
20								

Table 8.3: Source: ...

Number of input variables	4	Input constraints	1, 2, 3, 4
Number of output variables	4	Output constraints	1, 2, 3, 4

Table 8.4: System architecture

Question

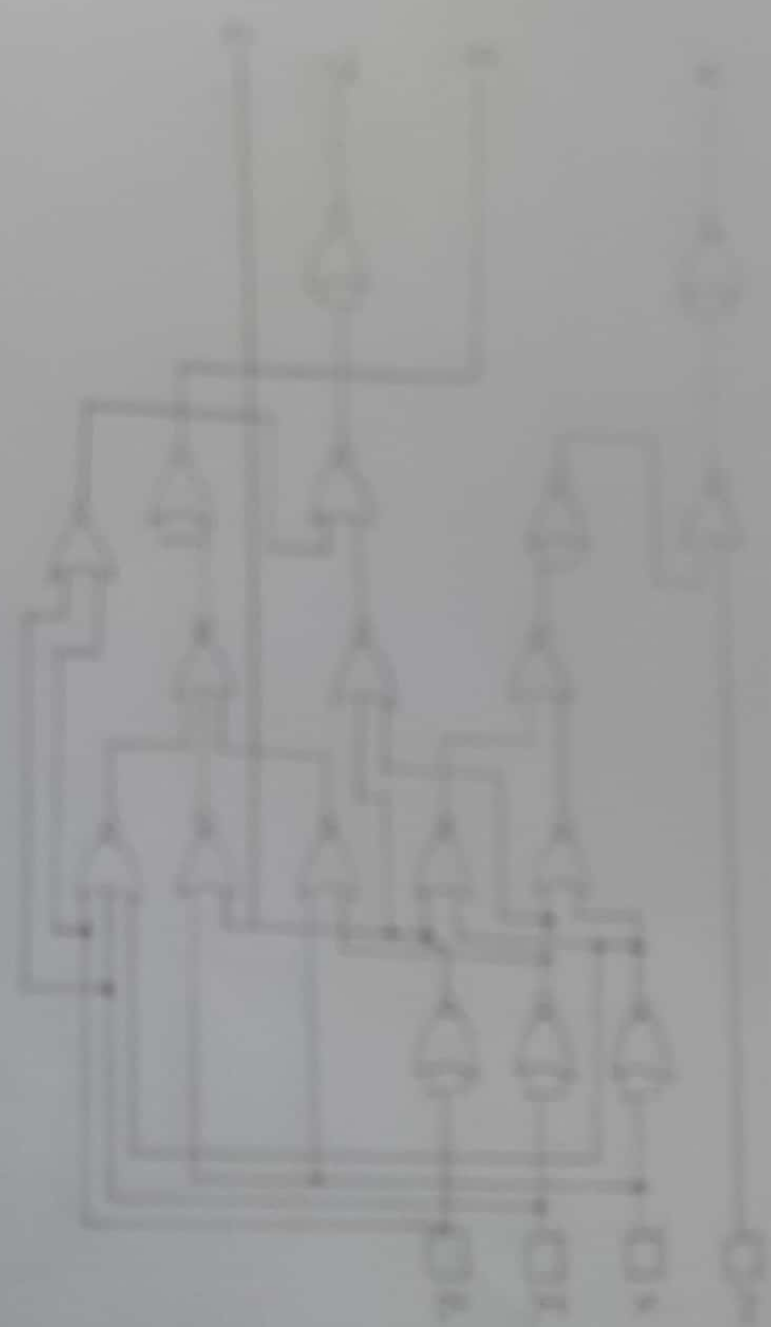
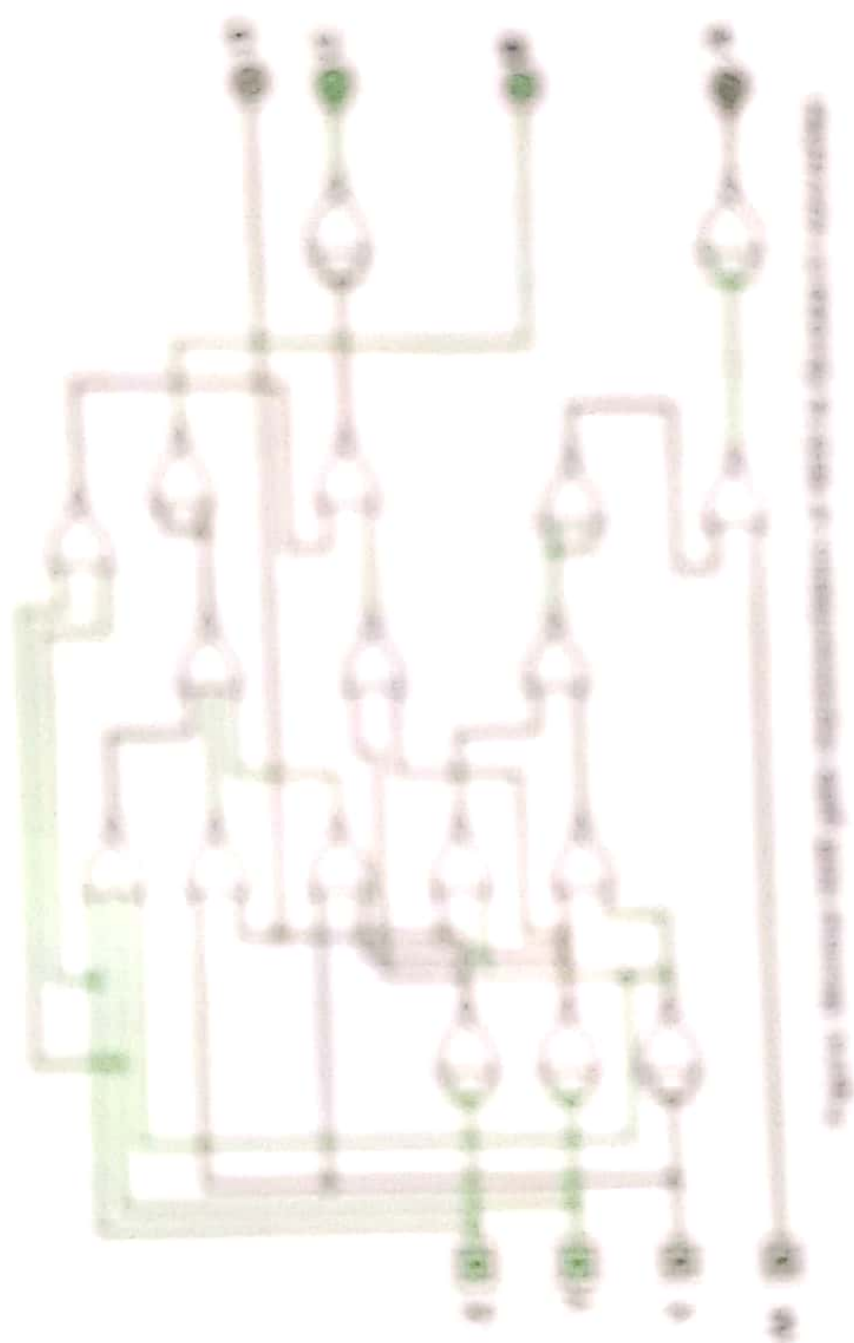


Figure 1: A logic circuit diagram showing the implementation of a function.



1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31. 32. 33. 34. 35. 36. 37. 38. 39. 40. 41. 42. 43. 44. 45. 46. 47. 48. 49. 50. 51. 52. 53. 54. 55. 56. 57. 58. 59. 60. 61. 62. 63. 64. 65. 66. 67. 68. 69. 70. 71. 72. 73. 74. 75. 76. 77. 78. 79. 80. 81. 82. 83. 84. 85. 86. 87. 88. 89. 90. 91. 92. 93. 94. 95. 96. 97. 98. 99. 100.

Discussion

Because of human error and equipment error, we didn't get our expected results. All our circuits were accurate, but no bulb were lightening because the machine had some unknown damage. In this experiment, we used three universal gates. IC 7408 Quadraple 2-input AND gate IC 7432 Quadraple 2-input OR gate and IC 7400 Quadraple 2-input NAND gate. We were asked to design a complete minimal combinational logic system from specification to implementation. We drew the circuit diagram and figured out the truth table. Finally, we drew the circuit diagram and checked the circuit with truth table.

