

North South University Department of Electrical & Computer Engineering

LAB REPORT

Course	Code	:	EEE211

Course Title: Digital Electronics

Section: 01

Experiment Number: 05

Experiment Name: Binary Arithmatic

Experiment Date: 07.12.2020

Date of Submission: 10.01.2021

Course Instructor: Fahimul Haque

Submitted To: Fatema Zahra

Experiment Name:

Birmary Arithmotic.

Objectives:

- Himmige combinational logic circuits using K-maps.

- Learn various numerical representations systems.

- Somplement circuit using 1 nd & 2 nd cononical minimal forms.

- Implement circuit using universal logic.

Theony +!

The addition & subtraction of the liming number system are similar to that of the decimal number system The only difference in that decimal ourober system consider the digit from 0-9 & their lease 10 whereas the bimary mumber system cominds only two digits (061) which make operation easier

Apparatus:

Trainer board.

\$ 1x 74831C (4 leit limory adder)

1 × 7486K quadruple 2 input XOR gater)

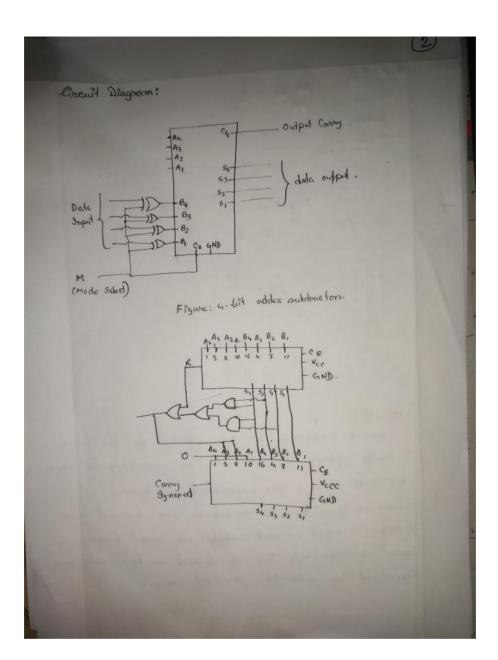


Table:

Operation M D 7+5 6 6 114 0101 6 1160 4+6 0 0100 0110 0 1010 9+11 0 1001 1011 1 0100 15+15 0 1111 1111 1 1100 7-5 1 0111 0101 1 0010 4-6 1 0106 0110 0 1110 11-2 1 1011 0010 1 1001 11-2 1 1011 1111 1111 1 0000			A	B	Cq	S4 93 82 S1
7+5 0 0100 0110 0 1010 9+11 0 1001 1011 1 0100 9+11 0 1111 1111 1 1110 15+15 0 1111 0101 1 0010 7-5 1 0111 0101 1 0010 4-6 1 0106 0110 0 1110 11-2 1 1011 0010 1 1001	operation	M			8	1166
4+6 0 1001 1011 1 0 0 0 0 0 0 0 0 0 0	7+5	6			0	1010
9+11 0 $15+15$ 0 1111 1111 1 0010 $1-5$ 1 0101 0101 0100 0110 0 0 0 0 0 0 0 0 0	4+6	0			1	0100
7-5 1 0111 0101 1 0010 4-6 1 0100 0110 0 1110 11-2 1 1011 0010 1 1001	9+11	0			1	1110
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	15+15	0			1	0010
4-6 1 0100 0110 11-2 1 1011 0010 1 1001 11-2 1 1111 1 1000	7-5	1				1110
11-2 1 9031 0000	4-6	1				
1111 1111	11 - 2	1	1011		A	
15-15	15-15	1	1111	1111		

				-
Operation	A	B	Over flow Correy	Sum
7+5	0111	0101	.0.	11 00
18+10	10016	100 11	1	00 101
72+83	1001006	101 0011	1	00 11 011
129+255	10000001	11 11 11 11	3	100 00 000

Operation	A	B	Overflow	Sum
9+0	1001	0006	0	1001
9+1	1001	0001	1	00000
9+2	1001	00 10	1	0001
9+3	1001	0011	1	0010
9+4	1001	0100	1	0011
9+5	1001	01 061	1	0100
0+6	1001	01 10	1	0101
9+7	1001	0111	1	011,0
9+8	1001	1000	1.	0111
9+9	1001	1001	1	1000

Observation Reports

Here M best used a made select which control the mode in this circuit, If For M=0, the circuit executes addition & for M=1, the circuit executes subtraction.

If in connected as imput in XOR. Truth Table for the XOR gates is:

A	B	output
0	0	0
0	1	1.
1	0	1 , 1
(1	1/	0

Here, But when B=M=0. then output would is either on the And, for M=J=B, output is A'=0 or 1.

Diencussion:

Due pandemic we rould not attend in practical lab session. But through some software simulation we have completed this lab. We have learned leinary addition & subtraction within at a time using adder-subtractor. Desides, we also learned BCD addition in cases where decimal number gre larger than 9 is at being used.

Simulation:

