Name_____ID_____Date_____

North South University
Department of Electrical and Computer Engineering
EEE211 lab FINAL

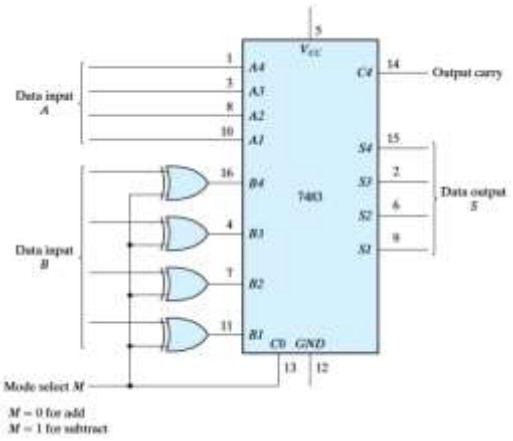
Total Marks: 50 **Time: 75 minutes and 15 minutes for submission**

Instructions:

1. Write your Name and ID on the answer sheet.
2. Answer all the questions in the Examination Booklet, clearly mention the question numbers.
3. Clearly label all the diagrams and truth tables.

Questions:

1. Subtract 1010 from 1110 using 2's compliment rule. **Explain** how the XOR gates work in the following circuit at the value M=1. [10]



2. Assume I_0, I_1, I_2 and I_3 in the following truth table are the Data Inputs of a 4:1 MUX. Find out the values of the Data Inputs for the function F(A, B, C) = Σ (0, 2, 5, 6). [10]

A	B	C	F	Data Inputs
0	0	0		I_0 =
0	0	1		
0	1	0		I_1 =
0	1	1		
1	0	0		I_2 =
1	0	1		
1	1	0		I_3 =
1	1	1		

3. **Design** a conversion process for **BCD to Excess-5** number system. This question incudes 3 parts.

COMBINATIONAL PART
This will include **truth table**, **karnaugh map**, **equations**.

[10]

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SEQUENTIAL PART
This will include **state table** using **T-FLIPFLOP**, **karnaugh map**, **equations**.

[10]

LOGISIM
Finally draw the complete **circuit diagram** including both the COMBINATIONAL and SEQUENTIAL part. Add you name and ID in simulation and submit screenshot of the complete circuit. .

[10]

Decimal Digit	Binary Coded Decimal (BCD)				Excess-5			
	W	X	Y	Z	A	B	C	D
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								