Department of Electrical & Computer Engineering (ECE)

North South University

Course Code: 231, Section: 6

Course Title: Digital Logic Design

Mid Exam, Fall 2018

Time: 75 Minutes Marks: 50

Please read the questions very carefully and answer accordingly. All the answers should be written in the answer script that is provided. Calculators/pens/pencils are allowed. Adopting any unfair means during the exam will automatically result in expulsion without any prior/post notice. You must return back your question paper with your answer script.

Q1. Please answer all the following questions:

[CO 1]

(a) Express the following output function F(x, y, z) in minterms and maxterms.

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- I. F(x, y, z) = x
- II. F(x, y, z) = x + xy
- (b) Draw the output function in relation to the inputs in a table and express the following output function in minterms.

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$$F(A, B, C) = M_0. M_2. M_4. M_7$$

(c) Write the expression of output function F(A, B, C) in maxterms for XNOR logic-gate.

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Q2. Please answer all the following questions:

[CO2]

- (a) Apply K-map to find out both Sum of Product (SOP) and Product of Sum (POS) for the following 16 functions:
 - $F(A,B,C,D) = \sum (0.5,10,15) + \sum d(2.7,8,13)$ i.
 - $F(A,B,C,D) = \sum (0,1,2,3,7,9,10,11,15)$ ii.
- $F(A,B,C,D) = (A + \overline{B} + C + \overline{D})(A + \overline{B} + \overline{C} + \overline{D})(\overline{A} + \overline{B} + C + \overline{D})(\overline{A} + \overline{B} + \overline{C} + \overline{D})$ iii.
- $F(A,B,C,D,E) = \prod (0,1,4,5,12,13,18,19,22,23,30,31)$ iv.
- (b) Find the **Prime Implicant (PI)** and **Essential Prime Implicants (EPI)** for the following functions and 4 also please indicate/mark clearly the **PI** and **EPI** in the K-map for the following functions.
 - I.
- $F(w,x,y,z) = \Sigma(0.1.5.7.10.14.15)$ II. $F(A,B,C,D) = \Pi(4.6.8.9.12.14)$

Q3. Please answer all the following questions:

[CO3]

(a) Draw the truth table of a full-subtractor and implement it using a decoder.

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(b) Implement a higher order decoder $n \times 2^n$, using lower order decoder $n \times 2^n$. Here, the order of n = 1, and 3.

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(c) Implement a three-input variable XOR gate using 4×1 multiplexer.

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(d) Draw the truth table for 8×3 priority encoder.

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(e) Implement the higher order multiplexer $2^n \times 1$ using lower order multiplexer $2^n \times 1$. Here, the order of n = 2, and 3. Basic gates i.e. AND, NOT, and OR gates can be incorporated with the design, if necessary.

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