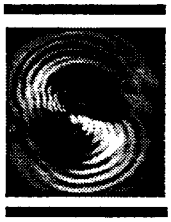

Solutions Manual

to accompany the text

Introduction to VLSI Circuits and Systems

by John P. Uyemura

Preliminary Draft
June, 2001

Note: This is the first draft of the Solutions Manual that was transcribed from tha author's hand-scratched notes. It has not been proofread, nor have the solutions been checked for completeness or accuracy. While most of them are reasonably accurate, errors will be found. The final version of the Solutions Manual will be available in the near future.

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Chapter 1

There are no problems in Chapter 1.

Chapter 2

[2.1] The nFET can pass any voltage in the range $[0, V_{max}]$ where $V_{max} = (V_G - V_{Tn})$ with V_G the voltage on the gate. With the stated values, $V_{max} = 5\text{-}0.7 = 4.3$ V. If $V_{in} > V_{max}$ then V_{out} is restricted to V_{max}. However, the nFET passes any voltage $V_{in} < V_{max}$. This gives the following answers.

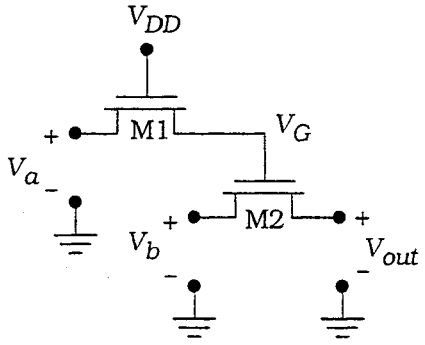
(a) $V_{in} = 2$ V, $V_{out} = 2$ V;
(b) $V_{in} = 4.5$ V, $V_{out} = 4.3$ V is limited;
(c) $V_{in} = 3.5$ V, $V_{out} = 3.5$ V;
(d) $V_{in} = 0.7$ V, $V_{out} = 0.7$ V.

The main idea is to show the effect of the threshold loss through an nFET.

[2.2] For $V_{in} < V_{max}$, then the input voltage is transmitted through the chain. If $V_{in} > V_{max}$, then a threshold drop occurs in the first transistor (only) and V_{max} makes it to the output. With the stated values, $V_{max} = 3.3\text{-}0.55 = 2.75$ V This gives the following answers.

(a) $V_{in} = 2.9$ V, $V_{out} = 2.75$ V (limited);
(b) $V_{in} = 3.0$ V, $V_{out} = 2.75$ V (limited);
(c) $V_{in} = 1.4$ V, $V_{out} = 1.4$ V;
(d) $V_{in} = 3.1$ V, $V_{out} = 2.75$ V (limited).

[2.3] The output of the upper FET M1 (with V_a applied) is used to control the gate voltage V_G of the lower transistor M2 (with V_a applied). Both are susceptible to threshold voltage



Problem [2.3]

drops so that max(V_G) = (V_{DD} - V_{Tn}) and max(V_{out}) = (V_G - V_{Tn}). Using max(V_G) = (3.3-0.6) = 2.7 V gives the following results.

(a) V_a = 3.3 V, V_b = 3.3 V: V_G = 2.7 V so V_{out} = 2.7 - 0.6 = 2.1 V.

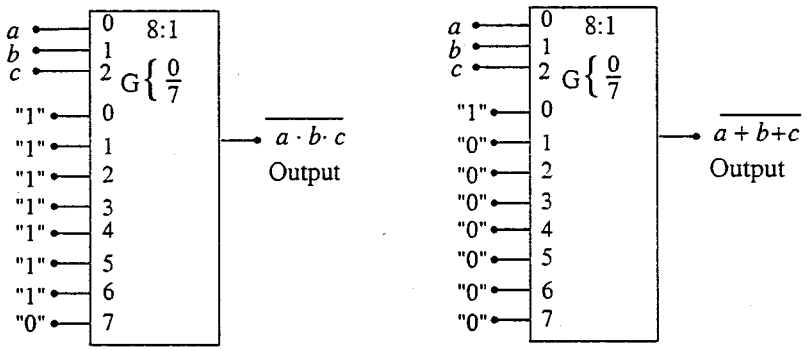
(b) V_a = 0.5 V, V_b = 3 V: V_G = 0.5 V so M2 is in cutoff. This makes V_{out} an unknown value since the transistor is an open circuit.

(c) V_a = 2 V, V_b = 2.5 V: V_G = 2 V so V_{out} = 2 - 0.6 = 1.4 V.

(d) V_a = 3.3 V, V_b = 1.8 V: V_G = 2.7 V so V_{out} = 1.8 V .

[2.4] NAND3 gate using an 8:1 MUX is shown in drawing below with Prob. [2.5] solution.

[2.5] NOR3 gate using an 8:1 MUX is shown in drawing below with Prob. [2.4] solution.

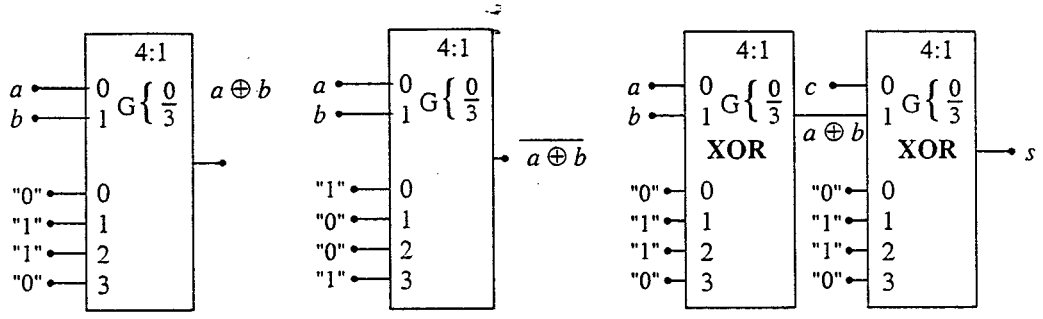


Problem [2.4] NAND 3 Problem [2.5] NOR 3

[2.6] The drawings below illustrate the XOR2 and XNOR2 MUX-based designs. To implement the full-adder sum expression, we use

$$s = (a \oplus b) \oplus c$$

which shows that s can be calculated using 2 XOR gates. This is shown in Figure (c) below.

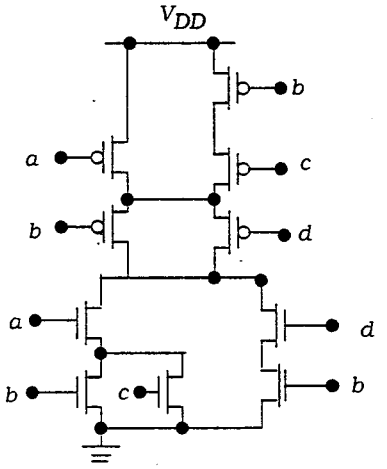


Problem [2.6]

[2.7] Rewrite the function to read

$$f = \overline{a \cdot (b + c) + b \cdot d}$$

to show that the function can be reduced to a simplified form. The gate is shown in the drawing.



Problem [2.7]

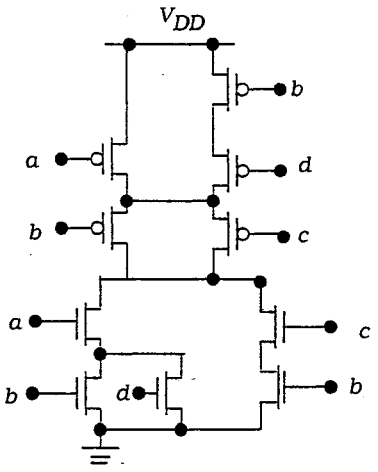
[2.8] The final design depends on the algebraic form selected. One approach is to first expand the terms as

$$\begin{aligned}(a+b)\cdot(a+c) &= a+a\cdot b+a\cdot c+b\cdot c\\ &= a\cdot(1+b)+a\cdot c+b\cdot c\\ &= a\cdot(1+c)+b\cdot c\\ &= a+b\cdot c\end{aligned}$$

Then

$$\begin{aligned}\overline{h} &= (a+b\cdot c)\cdot(b+d)\\ &= a\cdot b+b\cdot c+a\cdot d+b\cdot d\cdot c\\ &= a\cdot(b+d)+b\cdot c(1+d)\\ &= a\cdot(b+d)+b\cdot c\end{aligned}$$

This form of the logic function gives the AOI gate shown. Note that there are variations possible.

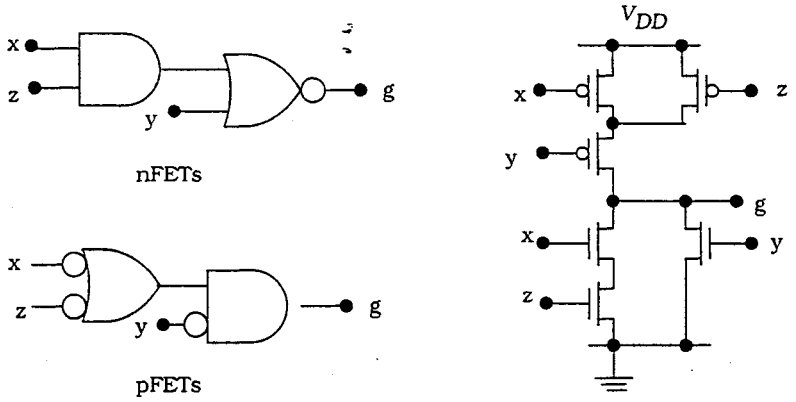


Problem [2.8]

[2.9] Write

$$\overline{g} = x\cdot(y+z)+y = x\cdot y+x\cdot z+y = y\cdot(1+x)+x\cdot z = y+x\cdot z$$

This gives the simplified logic diagrams, which are then used to design the logic gate as shown.

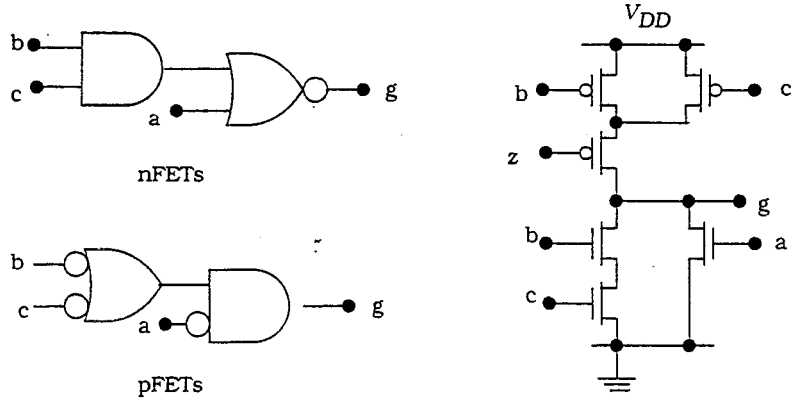


Problem [2.9]

[2.10] Write

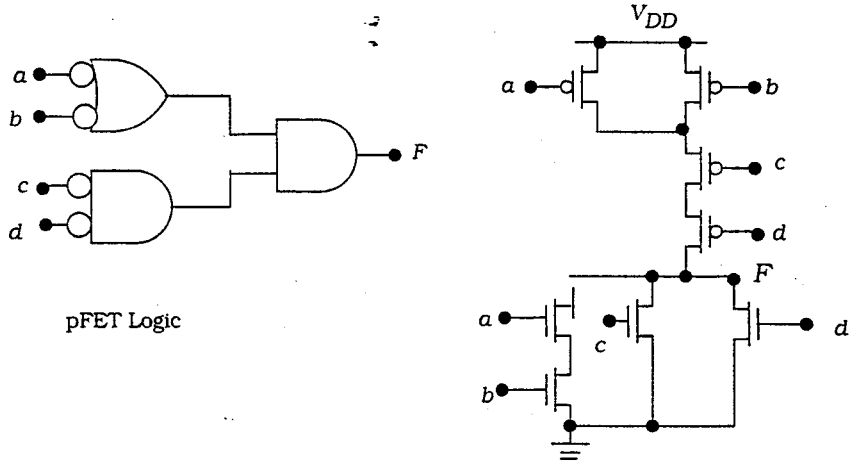
$$\overline{F} = a + b \cdot c + a \cdot b \cdot c = a \cdot (1 + b \cdot c) + b \cdot c = a + bc$$

After reducing we see that this is the same circuit as for Problem [2.4] with the inputs relabeled. This is shown for completeness



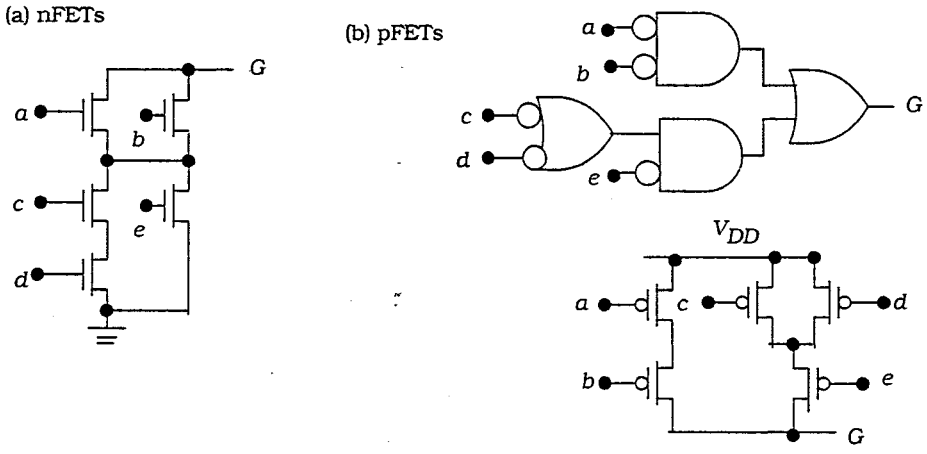
Problem [2.10]

[2.11] The pFET logic diagram and resulting gate are shown.



Problem [2.11]

[2.12] Solution is shown

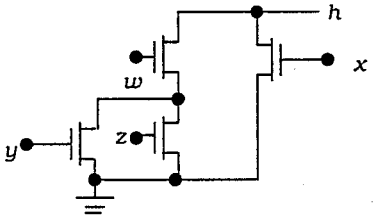


Problem [2.12]

[2.13] The logic expression is

$$\begin{aligned} h &= \bar{x} \cdot (\bar{y} \cdot \bar{z} + \bar{w}) \\ &= \bar{x} \cdot (\overline{y+z} + \bar{w}) \\ &= \bar{x} \cdot \overline{(y+z) \cdot w} \\ &= \overline{x + (y+z) \cdot w} \end{aligned}$$

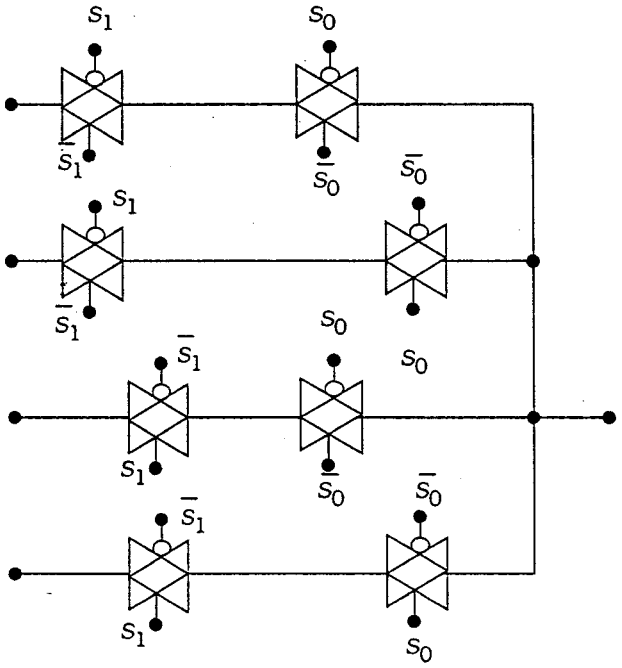
This leads to the nFET array shown. The circuit can be checked using series-parallel structuring.



Problem [2.13]

This example shows how the pFET logic equations can be used to describe a pFET network. The relationship to nFET equations is through the DeMorgan relations.

[2.14] The 4:1 circuit directly illustrates how TGs are used in switching.



Problem [2.14]

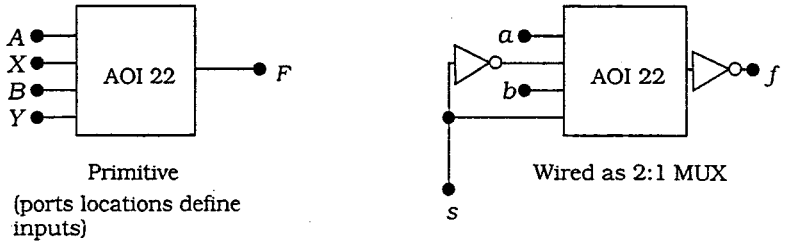
[2.15] The logic equation can be written as

$$f = a \cdot \bar{s} + b \cdot s$$

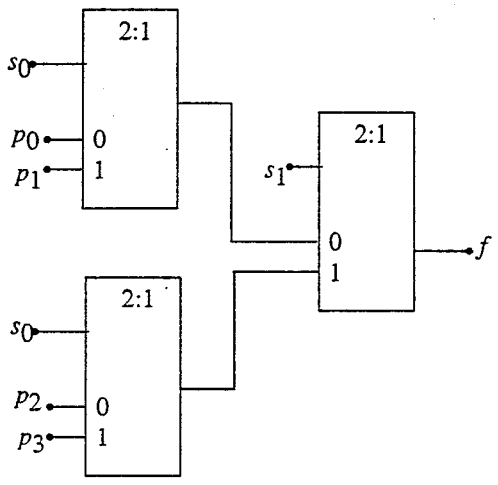
where a and b are the inputs, and s, $\bar{s}$ are the controls. An AOI22 gate would produce an output of

$$F = \overline{A \cdot X + B \cdot Y}$$

so we assign $a = A$, $b = B$, $X = \bar{s}$, and $Y = s$ and add an inverter. It is important to remember that the location of the ports define how the output function is formed.



[2.16] This can be designed by using two input 2:1 MUXes that are controlled by s_0, and the MUXing the outputs by a 2:1 that is controlled by s_1.



Problem [2.16]

[2.17] The period is

$$T = \frac{1}{f} = \frac{1}{2.1 \times 10^9} = 476 \text{ ps}$$

Why such an easy problem? To illustrate the time frame that logic gates in a high-speed digital system must operate. As we will see in Part 2, fast circuits (short logic delays) can be difficult to design.

[2.18] The smallest clock frequency is

$$f_{min} = \frac{1}{2t_{hold}} = \frac{1}{2(0.120)} = 4\text{Hz}$$

While this is very slow, it does show that the clock cannot be idled.

Chapter 3

[3.1] The resistance of the line is given by $R_{line} = R_s n$ where the number of squares can be divided into "normal" straight line contributions and corners. Let n_c be the contribution of a corner square. The number of square is given by tracing the line from A to B as

$$n = 15 + n_c + 12 + n_c + 14 + n_c + 4 + n_c + 22 + n_c + 9 = 76 + 56n_c = 79.125$$

so

$$R = 25(79.125) = 1,978.125\Omega$$

[3.2]The line resistance is $R_{line} = R_s n$. Fdor the polysilicon line

$$R_{line} = 25\left(\frac{275}{0.5}\right) = 1375\Omega$$

while the metal line is

$$R_{line} = 0.08\left(\frac{32.4}{0.8}\right) = 3.24\Omega$$

which is the smallest.

[3.3](a) The sheet resistance is

$$R_s = \frac{\rho}{t} = \frac{(4\times10^{-6})}{(1200\times10^{-8})} = 0.33\Omega$$

(b) The number of squares is given by

$$n = \frac{125}{0.6} = 156.25 \text{ squares}$$

so that the line resistance is

$$R_{line} = (0.33)(156.25) = 52.08\Omega$$

[3.4]We have units of the *RC* product of

$$RC = [\Omega][F] = \left[\frac{V}{A}\right]\left[\frac{C}{V}\right] = \left[\frac{C}{A}\right] = \left[\frac{C}{\frac{C}{\text{sec}}}\right] = [\text{sec}]$$

which shows that τ has units of sec as stated.

[3.5] (a) Use the line resistance formula

$$R_{line} = (25)\left(\frac{40}{0.5}\right) = 2k\Omega$$

(b) The line capacitance is

$$C_{line} = \frac{\varepsilon_{ox}(wl)}{T_{ox}} = \frac{(3.9)(8.854\times10^{-14})(0.5\times10^{-4})(40\times10^{-4})}{1000\times10^{-8}} = 6.906 \text{ fF}$$

(c) The line time constant is

$$\tau = R_{line}C_{line} = (2000)(6.906\times10^{-15}) = 13.81 \text{ ps}$$

[3.6] (a) For n-type material,

$$n_{n0} \approx N_d = 4\times10^{17}\text{cm}^{-3}$$

(b) The hole density is

$$p_{n0} = \frac{n_i^2}{n_n} = \frac{(1.45\times10^{10})^2}{(4\times10^{17})} = 525.6 \text{ cm}^{-3}$$

(c) The electron mobility is

$$\mu_n = 92 + \frac{1380-92}{1+\left(\frac{4\times10^{17}}{1.3\times10^{17}}\right)^{0.81}} = 433 \text{ cm}^2/\text{V-sec}$$

while the hole mobility is

$$\mu_p = 47.7(92) + \frac{495-47.7}{1+\left(\frac{4\times10^{17}}{1.6\times10^{14}}\right)^{0.76}} = 135.9 \text{ cm}^2/\text{V-sec}$$

The mobility is then given by

$$\sigma = q(\mu_n n + \mu_p p) \approx q\mu_n n_n = 27.71 \ [\Omega\text{-cm}]$$

since the majority electron concentration dominates.

[3.7] $N_a > N_d$, so the material is p-type. The majority carrier density is

$$p_{p0} \approx N_d - N_d = 5.98\times10^{18}\text{cm}^{-3}$$

and the minority carrier density is

$$n_{p0} = \frac{n_i^2}{p_{p0}} = \frac{(1.45\times10^{10})^2}{(5.98\times10^{18})} = 35.2 \ \text{cm}^{-3}$$

[3.8] (a) We have carrier densities of

$$p_{p0} \approx N_d = 4\times10^{14}\text{cm}^{-3} \qquad n_{p0} \approx \frac{n_i^2}{p_{p0}} = 5.26\times10^{5}\text{cm}^{-3}$$

(b) The mobilities are $\mu_n = 1373.36$ and $\mu_p = 485.6$ cm^2/V-sec so that the conductivity is calculated from

$$\sigma = (1.6\times10^{-19})[(5.26\times10^{5})](1373.36) + (4\times10^{14})(485.6)]$$

This gives

$$\sigma = 0.31 \qquad \rho = (1/\sigma) = 32.17[\Omega - cm]$$

(c) The resistance is

$$R = \left(\frac{100\times10^{-4}(32.17)}{1\times10^{-8}}\right) = 32.17\Omega$$

[3.9] (a) Start with

$$\sigma = q\left(\mu_n\frac{n_i^2}{p} + \mu_p p\right)$$

(b) Differentiate:

$$\frac{d\sigma}{dp} = \frac{d}{dp}\left(\mu_n\frac{n_i^2}{p} + \mu_p p\right) = -\mu_n\frac{n_i^2}{p^2} + \mu_p = 0$$

so we require

$$p = \sqrt{\frac{\mu_n}{\mu_p}}n_i > n_i$$

(c) The last equation shows that the highest resistively material is slightly p-type.

[3.10] (a) This is

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.854\times10^{-14})}{90\times10^{-8}} = 3.837\times10^{-7}\frac{F}{cm^2}$$

(b) $k'_n = \mu_n C_{ox} = 214.86\ \mu A/V^2$
(c) $\beta_n = k'_n (W/L) = 1.719\ mA/V^2$

[3.11] $\beta_n = k'_n (W/L)$ with

$$k_n' = \mu_n\left(\frac{(3.9)(8.854\times10^{-14})}{10\times10^{-7}}\right) = 172.65\mu A/V^2$$

(a) $\beta_n = k'_n (W/L) = 172.65(10/0.5) = 3.453 \times 10^{-7}\ A/V^2$. The resistance is $R_n = 111.39\ \Omega$
(b) The resistance is reduced to

$$R_n = \frac{1}{(1.7265\times10^{-6})\left(\frac{22}{0.5}\right)(3.3-0.8)} = 50.63\Omega$$

[3.12] (a) $k'_p = \mu_p C_{ox}$ so we calculate

$$k_p' = (220)\left(\frac{(3.9)(8.854\times10^{-14})}{11.5\times10^{-7}}\right) = 66.06\mu A/V^2$$

The resistance is then given by

$$R_p = \frac{1}{(66.06\times10^{-6})\left(\frac{14}{0.5}\right)(3.3-0.8)} = 216.25\Omega$$

[3.13] Start with

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 3.63\times10^{-7}\frac{F}{cm^2}$$

(a) $k'_n = \mu_n C_{ox} = 196.28\ \mu A/V^2$ and $k'_p = \mu_p C_{ox} = 79.97\ \mu A/V^2$. With the aspect ratios we have $\beta_n = 6.73\ mA/V^2$ and $\beta_p = 2.74\ mA/V^2$ so that $R_n = 56.1\ \Omega$ and $R_p = 142.48\ \Omega$ using the formulas.
(b) $R_p = 0.8\ R_n$ so

$$\frac{1}{\beta_p(3.3-0.65)} = 44.88\Omega$$

or

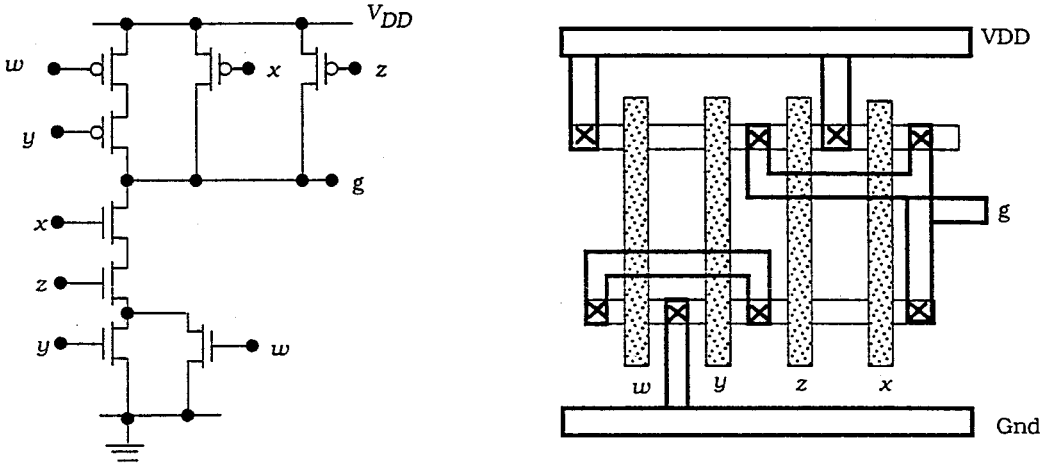
$$\beta_p = 8.408\times10^{-3} = k_p'\left(\frac{W}{0.35}\right)$$

which gives the value of W = 36.8 μm needed for the pFET.

[3.14] The function is

$$Out = \overline{x \cdot z \cdot (y + w)}$$

This leads to the following circuit.

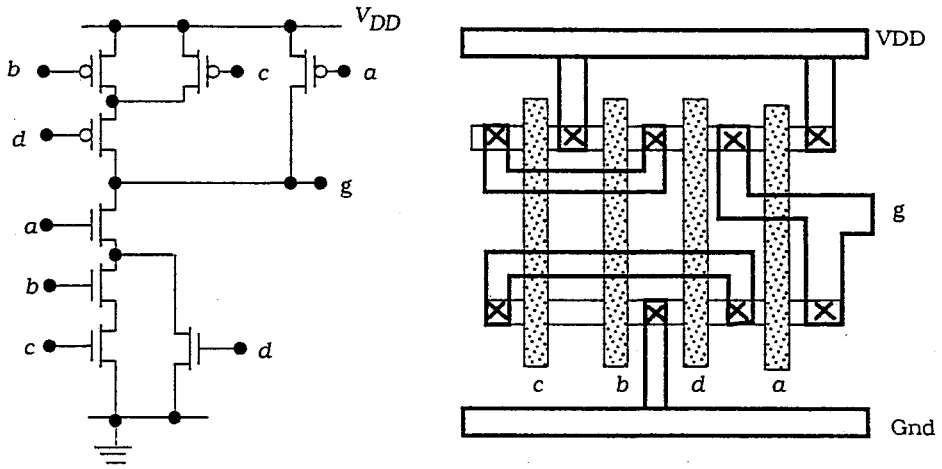


Problem [3.14]

[3.15] The function is

$$F = \overline{a \cdot b \cdot c + a \cdot d} = \overline{a \cdot (b \cdot c + d)}$$

which is shown in the circuit below.

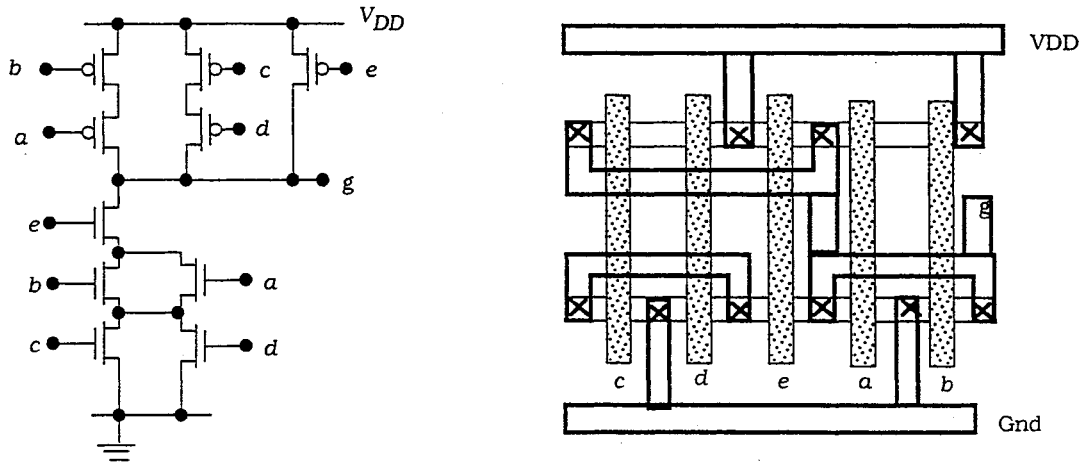


Problem [3.15]

[3.16] The OAI function is

$$g = \overline{(a+b)\cdot(c+d)\cdot e}$$

This is obtained from the CMOS circuit shown below. The placement of the inputs has be chosen to facilitate the layout.

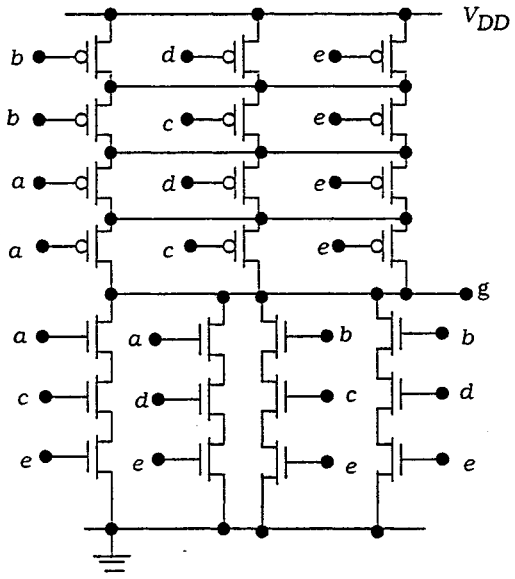


Problem [3.16] Circuit

[3.17] Expanding gives

$$\begin{aligned} g &= \overline{(a+b)\cdot(c+d)\cdot e} \\ &= \overline{(a\cdot c + a\cdot d + b\cdot c + b\cdot d)\cdot e} \\ &= \overline{a\cdot c\cdot e + a\cdot d\cdot e + b\cdot c\cdot e + b\cdot d\cdot e} \end{aligned}$$

The third line is an expanded AOI form, but uses excess transistors. This can be seen in the circuit below. Although we could do a somewhat messy layout, of the gate as-is, we can see by inspection that the expanded AOI form is not an efficient implementation of the logic function.



Problem [3.17]

[3.18] Yes, this is a functional gate. The function is

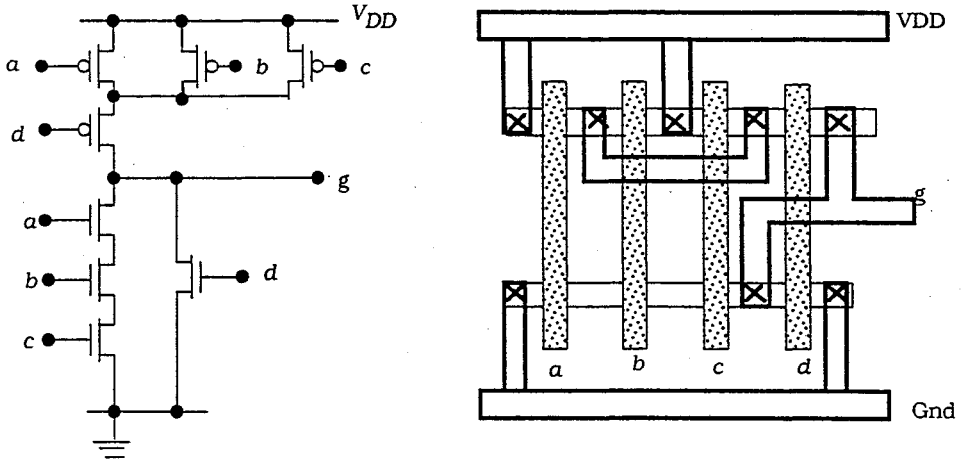
$$f = \overline{a\cdot b + c + d}$$

as can be verified by tracing the circuit.

[3.19] We start with

$$g = \overline{a \cdot b \cdot c + d}$$

The CMOS circuit and layout are drawn below.



Problem [3-19]

Chapter 4

There are no problems in Chapter 4.

Chapter 5

There are no problems in Chapter 5. However, the concepts can be illustrated by assigning layout problems using a CAD tool set. A suggested list of simple structures is

an nFET and a pFET with a minimum aspect ratio; scaled FETs; series connections that share drain/source regions for 2 FETs and 3 FETs; minimum size inverter; NAND2 and NOR2 gates with standard size transistors; a simple AOI and OAI gate.

Chapter 6

[6.1] (a) The oxide capacitance per unit area is

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.854\times10^{-14})}{100\times10^{-8}} = 3.45\times10^{-7}\frac{F}{cm^2} = 3.45\frac{fF}{\mu m^2}$$

(b) $k'_n = \mu_n C_{ox} = 189.92\ \mu A/V^2$ and $k'_p = \mu_p C_{ox} = 75.51\ \mu A/V^2$

[6.2] $\beta_n = 110\ (10/.35) = 3.143\ mA/V^2$

(a) $V_{sat} = 2 - 0.7 = 1.3\ V > V_{DS} = 1\ V$ so the transistor is non-saturated. The current is

$$I_D = \left(\frac{3.143}{2}\right)[2(1.3)1 - 1^2)] = 2.51mA$$

(b) Now $V_{sat} = 2 - 0.7 = 1.3\ V < V_{DS} = 2\ V$ so the transistor is saturated. The current is

$$I_D = \left(\frac{3.143}{2}\right)[1.3^2] = 2.66mA$$

[6.3]

(a) $V_{sat} = 1 - 0.76 = .24\ V < V_{DS} = 1\ V$ so the transistor is saturated. The current is

$$I_D = \left(\frac{2.3}{2}\right)[0.24^2] = 66.24\mu A$$

(b) $V_{sat} = 1\ .24\ V < V_{DS}$ so the transistor is saturated with a current

$$I_D = \left(\frac{2.3}{2}\right)[1.24^2] = 1.77mA$$

(c) $V_{sat} = 2.24 < V_{DS} = 2.5\ V$ so the transistor is saturated with

$$I_D = \left(\frac{2.3}{2}\right)[2.24^2] = 5.77mA$$

[6.4](a)

$$k'_p = (220)\frac{(3.9)(8.854\times10^{-14})}{60\times10^{-8}} = 126.61\times10^{-6}\frac{A}{V^2}$$

(b) $\beta_p = k'_p\,(W/L) = k'_p\,(12) = 1.519\ mA/V^2$

The resistance is

$$R_p = \frac{1}{(1.519\times10^{-3})(3.3-0.7)} = 254.7\Omega$$

[6.5]Start with

$$C_{ox} = \frac{(3.9)(8.854\times10^{-14})}{120\times10^{-8}} = 2.878\times10^{-7}\frac{F}{cm^2}$$

(a) The body bias coefficient is calculated from

$$\gamma = \frac{\sqrt{2q\epsilon_{Si}N_a}}{C_{ox}}$$

so

$$\gamma = \frac{\sqrt{2(11.8)(8.854\times10^{-14})(8\times10^{-14})}}{2.878\times10^{-7}} = 0.0568V^{\frac{1}{2}}$$

(a) We need

$$2|\phi_F| = 2(0.026)\ln\left[\frac{8\times10^{14}}{1.45\times10^{10}}\right] = 0.568V$$

Then

$$V_{Tn} = V_{T0n} + \gamma(\sqrt{2|\phi_F| + V_{SBn}} - \sqrt{2|\phi_F|})$$

so using the equation with a body bias of 2 V applied gives

$$V_T = 0.55 + (0.0568)(\sqrt{2.568} - \sqrt{0.568}) = 0.598V$$

(c) Now we have

$$V_T = 0.55 + (0.0568)(\sqrt{3.568} - \sqrt{0.568}) = 0.614V$$

so that V_{sat} = 3-0.614 = 2.386 V < V_{DS}. The FET is saturated, so

$$I_D = \left(\frac{540}{2}\right)[2.386^2] = 442.31\mu A$$

[6.6]The drawn channel length is L' = 0.5μm, so that electrical channel length is given by L = 0.5 - 2(0.05) = 0.4 μm. The area of the gate is $A_G = L'W$ = (6)(0.5) μm^2 = 3 μm^2. The gate capacitance is therefore

$$C_G = (2.70)(3) = 8.1fF$$

For hand estimates, we take

$$C_{GS} = C_{GD} = \frac{1}{2}C_G = 4.05 \text{ fF}$$

For the n+ capacitance we have a zero-bias value of

$$C_{n+} = (0.86)(2.05)(6) + (0.24)2[2.05 + 6] = 14.442\text{fF}$$

where we have combined the bottom and sidewall contributions. The total capacitance at the drain or source is

$$C_D = C_{GD} + C_{DB} = 14.442 + 4.05 = 18.492\text{fF} = C_S$$

by adding the contributions
The resistance is

$$R_n = \frac{1}{(150\times10^{-6})\left(\frac{6}{0.4}\right)(5-0.6)} = 101\Omega$$

[6.7]SPICE listing of the nFET

```
nFET Model
M1 20 10 0 0 nfet L=0.5U W=6U AD=18P PD=16U AS=18P PS=16U
.MODEL nfet NMOS (KP=150U VTO=0.6 TOX=1.28E-8 CJ= 8.6E-4 CJSW=2.4E-10)
```

A nested .DC command can be used to generate the I-V curve. This requires that we add drain and gate voltages of the form

```
VD 20 0 5volts
VG 10 0 1volts
.DC VD 0 5 0.1 VG 0 5 0.1
VG 10 0 1volts
```

[6.8]The poly resistance is estimated by including only the actual FET geometry as

$$R_{poly} = (26)\frac{6}{0.5} = 312\Omega$$

while the n+ resistance is

$$R_{n+} = (30)\frac{2.05}{6} = 10.25\Omega$$

This shows that R_{n+} is small, but R_{poly} can get large.

[6.9](a) $V_{sat} = V_{GS} - V_{Tn} < V_{DS}$ so the transistor is saturated

(b) Compute

$$I_D = \left(\frac{120(20/0.5)}{2}\right)(5-0.65)^2 = 45.4mA$$

The resistance at this point is

$$R_n = \frac{V_{DS}}{I_D} = \frac{5}{45.4\times10^{-3}} = 110\Omega$$

(c) Using the linearized approximation

$$R_n = \frac{1}{(4.8\times10^{-3})(5-0.65)} = 47.89\Omega$$

so that the LTI estimate is smaller than the actual value.

[6.10]We have

$$R_n = \frac{1}{k'_n(W/L)(V_{GS}-V_{Tn})}$$

so

$$\left(\frac{W}{L}\right) = \frac{1}{k'_nR_n(V_{GS}-V_{Tn})} = \frac{1}{(100\times10^{-6})(950)(3.3-7)} = 4.05$$

Chapter 7

[7.1] The β-ratio is

$$\frac{\beta_n}{\beta_p} = \frac{100(10)}{42(14)} = 1.7$$

so that the midpoint voltage is

$$V_M = \frac{3.3-0.8+\sqrt{1.7}(0.7)}{1+\sqrt{1.7}} = 1.48V$$

[7.2] Compute

$$\frac{\beta_n}{\beta_p} = \left(\frac{V_{DD}-V_M-|V_{Tp}|}{V_M-V_{Tn}}\right)^2 = \left(\frac{3-1.3-0.82}{1.3-6}\right)^2 = 1.58$$

so

$$\frac{\beta_n}{\beta_p} = \frac{k'_n(W/L)_n}{k'_p(W/L)_p} = 2.2\frac{(W/L)_n}{(W/L)_p} = 1.58$$

The two aspect ratios are related by

$$(W/L)_p = 1.39(W/L)_n$$

[7.3] (a) The transconductance ratio is

$$\frac{\beta_n}{\beta_p} = \frac{2.1}{1.8} = 1.162$$

The midpoint voltage is then

$$V_M = \frac{5 - 0.7 + \sqrt{1.162}(0.6)}{1 + \sqrt{1.162}} = 2.378\text{V}$$

(b) The resistances are

$$R_n = \frac{1}{(2.1\times10^{-3})(5 - 0.6)} = 108.23\Omega$$

$$R_p = \frac{1}{(1.8\times10^{-3})(5 - 0.7)} = 129.2\Omega$$

(c) The high-to-low and low-to-high times without any external load are

$$t_{HL} = 2.2R_nC_{out} = 2.2(108.23)(74\times10^{-15}) = 17.62\text{ps}$$

$$t_{LH} = 2.2R_pC_{out} = 2.2(129.20)(74\times10^{-15}) = 21.03\text{ps}$$

(d) With the external load, $C_{out} = 74 + 115 = 189$ fF. Then

$$t_{HL} = 2.2R_nC_{out} = 2.2(108.23)(189\times10^{-15}) = 45.0\text{ps}$$

$$t_{LH} = 2.2R_pC_{out} = 2.2(129.20)(189\times10^{-15}) = 53.72\text{ps}$$

(e) In general, we can write the equations as

$$t_{HL} = 17.62 + 0.238C_L$$

$$t_{LH} = 21.03 + 0.284C_L$$

where C_L is in fF.

[7.4] The transconductance ratio is

$$\frac{\beta_n}{\beta_p} = \frac{150(4)}{60(8)} = 1.25$$

The midpoint voltage is then

$$V_M = \frac{5 - 0.7 + \sqrt{1.25}(0.6)}{1 + \sqrt{1.25}} = 2.347\text{V}$$

[7.5] The (electrical) channel length is $L = 0.8$ μm, and the drawn channel length is $L' = 1.0$ μm.

(a) The input capacitance is

$$C_{in} = (2.70)(1)(8+4) = 32.4\text{fF}$$

(b) The LTI resistances are

$$R_n = \frac{1}{(150\times10^{-6})(4/0.8)(5-0.6)} = 303.03\Omega$$

$$R_p = \frac{1}{(60\times10^{-6})(8/0.8)(5-0.7)} = 387.6\Omega$$

(c) $C_{out} = C_{FET} + C_L = 50.45+80 = 130.45$ fF, so the switching times are

$$t_{HL} = 2.2R_nC_{out} = 87.04\text{ps}$$

$$t_{LH} = 2.2R_pC_{out} = 111.24\text{ps}$$

[7.6] SPICE simulation

[7.7] (a) We write

$$\sqrt{\frac{\beta_N}{\beta_P}} = \sqrt{\frac{2}{1}}$$

so

$$V_M = \frac{5-0.7+\left(\frac{1}{2}\right)\sqrt{2}(0.6)}{1+\left(\frac{1}{2}\right)\sqrt{2}} = 2.77\text{V}$$

(b) For a NOT gate with the same relative dimensions,

$$V_M = \frac{5-0.7+\sqrt{2}(0.6)}{1+\sqrt{2}} = 2.13\text{V}$$

[7.8] The midpoint voltage for the simultaneous switch case is

$$V_M = \frac{3.3-0.8+(2)\sqrt{\frac{1}{2.2}}(0.65)}{1+(2)\sqrt{\frac{1}{2.2}}} = 1.47\text{V}$$

[7.9] For a NAND3 gate, we follow the same treatment as in the text to write the KCL equation

$$\frac{(\beta_n/3)}{2}(V_M - V_{Tn})^2 = \frac{3\beta_p}{2}(V_{DD} - V_M - |V_{Tp}|)^2$$

so

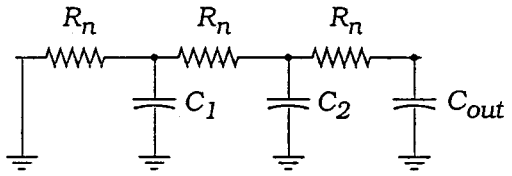
$$\beta_p = \frac{\beta_n}{9}\left(\frac{V_M - V_{Tn}}{V_{DD} - V_M - |V_{Tp}|}\right)^2 = \frac{120(4)}{9}\left(\frac{2.4 - 0.55}{5 - 2.4 - 0.9}\right)^2 = 63.16\mu A/V^2$$

[7.10] (a) The resistance of a FET is

$$R_n = \frac{1}{(2\times10^{-3})(3.3 - 0.7)} = 192.31\Omega$$

The time constant for the output capacitor is obtained from the Elmore formula as

$$\begin{aligned}\tau_n &= 3R_nC_{out} + 2R_nC_2 + R_nC_1 \\ &= R_n[3C_{out} + 2C_2 + C_1] \\ &= 192.31[(3)130 + (2)36 + 36]\times10^{-15} \\ &= 95.77 \text{ ps}\end{aligned}$$



Problem [7.10]

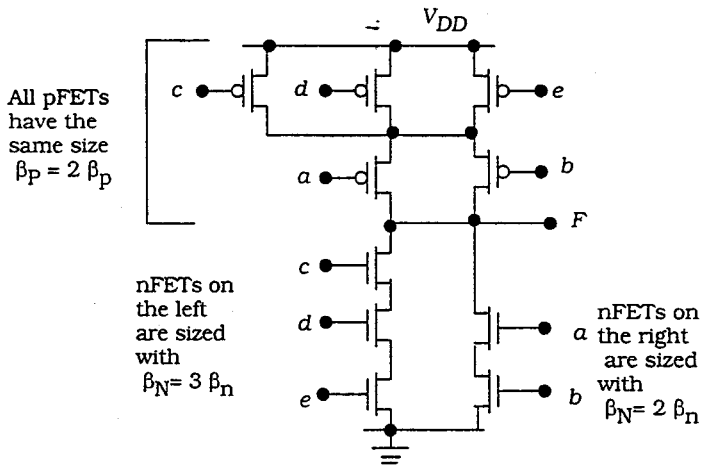
(b) If we ignore C_1 and C_2,

$$\tau_n = 3R_nC_{out} = 75 \text{ ps}$$

which gives a percentage error of

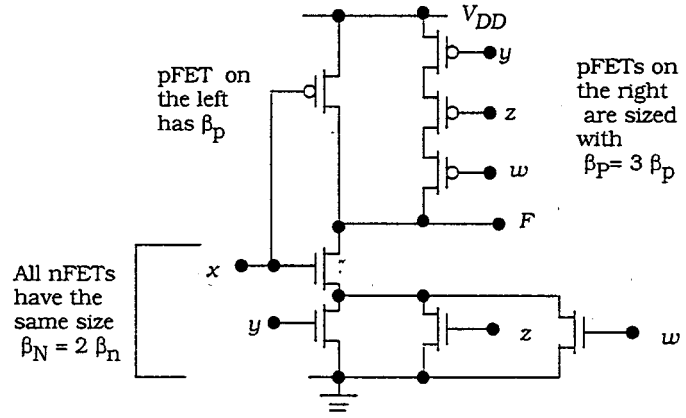
$$\% \text{ Error} = \left(\frac{95.77 - 75}{95.77}\right)\times 100\ \% = 21.6\ \%$$

[7.11] The circuit and the relative device sizes are shown in the drawing.



Problem [7.12]

[7.12] The circuit and the relative device sizes are shown in the drawing.



Problem [7.12]

Chapter 8

[8.1] The general form of the rise time equation is

$$t_r = t_{r0} + \alpha C_L$$

so the information gives the two equations

$$123.75\times10^{-12} = t_{r0} + \alpha(100\times10^{-15})$$

$$138.6\times10^{-12} = t_{r0} + \alpha(115\times10^{-15})$$

(a) Subtracting the top equation from the bottom one gives

$$14.85\times10^{-12} = \alpha(15\times10^{-15})$$

so

$$\alpha = 0.99\times10^{3} = 2.2R_n$$

Thus, $R_n = 450\Omega$.

(b) Use either equation to find t_{r0}:

$$123.75\times10^{-12} = t_{r0} + \alpha(100\times10^{-15}) = t_{r0} + 990(100\times10^{-15})$$

so

$$t_{r0} = 2.475\times10^{-11} = 2.2R_nC_{FET}.$$

This gives

$$C_{FET} = \frac{2.475\times10^{-11}}{990} = 25\text{fF}$$

Thus, we can write the general expressions

$$t_r = 24.75 + 0.99C_L \text{ ps} = t_f$$

where C_L is in units of fF.
(c) With a scaling factor of 3.2×, t_{r0} is the same but α is scaled to (.99/3.2)=0.309. This gives the expression

$$t_r = t_r = 24.75 + 0.309C_L \text{ ps}$$

[8.2]The delay through the 3-stage chain is

$$t_d = 2t_r + t_f$$

where

$$t_r = 430 + 3.68(45) = 595.6 \text{ ps}$$

$$t_f = 300 + 2.56(45) = 415.2 \text{ ps}$$

so

$$t_d = 2(595.6) + 415.2 = 1.606 \text{ ns}$$

[8.3]We estimate the delay by adding times

$$t_d = t_{f,\,not} + t_{r,\,nor2} + t_{f,\,nand2} + t_{r,\,not}$$

where we assume that a switch occurs at every gate. Using the formulas for the specified m-values gives

$$t_d = [t_{f0} + \alpha_{nu}(2C_{min})] + [3t_{r0} + 2\alpha_{pu}(4C_{min})] + [3t_{f0} + 2\alpha_{nu}(3C_{min})] + \left[t_{f0} + \frac{\alpha_{pu}}{3}(10C_{min})\right]$$

Grouping,

$$t_d = 4t_{f0} + 8\alpha_{nu}C_{min} + 4t_{f0} + \frac{80}{3}\alpha_{pu}C_{min}$$

[8.4](a) The input capacitance is

$$C_{in} = C_{ox}LW(1 + r) = C_{ox}(0.4)(2.2)(1 + 2.6) = 25.344 \text{ fF}$$

(b) The number of stages is

$$N = \ln\left(\frac{C_L}{C_{in}}\right) = \ln\left(\frac{38\times10^{-12}}{25.344\times10^{-15}}\right) = 7.31$$

so we select $N = 7$.

(c) The reference resistance is $R_{1\mu m} = 1725\ \Omega$, so $R_{2.2x} = (1725/2.2) = 784.1\ \Omega$. Since

$$S = \left(\frac{C_L}{C_{in}}\right)^{\frac{1}{N}} = 2.85$$

the total delay is

$$\tau_d = NS\tau_r = 7(2.85)(784.1)(25.344\times10^{-15}) = 396.45 \text{ ps}$$

for the simplified analysis.

[8.5]We calculate the number of stages as

$$N = \ln\left(\frac{C_L}{C_{in}}\right) = \ln\left(\frac{40\times10^{-12}}{50\times10^{-15}}\right) = \ln(800) = 6.68$$

so we select $N = 6$. The scaling factor is

$$S = \left(\frac{C_L}{C_{in}}\right)^{\frac{1}{N}} = 3$$

so that we start with β_1 (known), and calculate the driver sizes as

$$\beta_2 = 3\beta_1,\ \beta_3 = 9\beta_1,\ \beta_4 = 27\beta_1,\ \beta_5 = 81\beta_1,\ \beta_6 = 243\beta_1$$

[8.6]The line capacitance is

$$C_{line} = c'l = (0.86)(272) = 233.92 \text{ fF}$$

so the number of stage is

$$N = \ln\left(\frac{233.92}{52}\right) = 1.5$$

is $N = 2$ for a non-inverting design. The scaling factor is estimated by

$$S = \left(\frac{233.92}{52}\right)^{\frac{1}{2}} = 2.1$$

which is accurate enough for a rough design. Thus, if the first stage has a size β_1, then the second (driver) stage has a size of $2.1\beta_1$.

[8.7]The transcendental equation is

$$S\ln((2)-1) = 0.72$$

Trial and error gives S ≈ 3.37.

[8.8]We first calculate the path effort with $r = 2.5$

$$F = GH = g_1g_2g_3g_4\tilde{H} = \left(\frac{5.5}{3.5}\right)\left(\frac{4.5}{3.5}\right)\left(\frac{6}{3.5}\right)1\left(\frac{10C}{C}\right) = 34.64$$

so that the stage value is

$$\hat{f} = (34.64)^{\frac{1}{4}} = 2.43$$

This is used to calculate the input capacitance to each stage, which can in turn be used to find the scale factors if desired.

Starting with the last stage we have

$$h_4 = \frac{\hat{f}}{g_4} = \frac{2.43}{1} = \frac{10C}{C_4}$$

so $C_4 = (10/2.43)C = 4.12C$. For the third stage,

$$h_3 = \frac{\hat{f}}{g_3} = \frac{2.43}{(6/3.5)} = \frac{4.12C}{C_3}$$

so $C_3 = 2.91C$. For the second stage,

$$h_2 = \frac{\hat{f}}{g_2} = \frac{2.43}{(4.5/3.5)} = \frac{2.91C}{C_2}$$

so $C_2 = 1.54C$. For the input stage,

$$h_1 = \frac{\hat{f}}{g_1} = \frac{2.43}{(4.5/3.5)} = \frac{1.54C}{C_1}$$

so $C_1 = C$ as required.

[8.9]This path has a branching factor that we compute as

$$B = \frac{(2(2)+r)+(3(3)+r)}{(2(2)+r)} = \frac{13+2r}{4+r} = 2.77$$

The path effort is then

$$F = GHB = g_1 g_2 B g_3 H = \left(\frac{6}{3.5}\right)\left(\frac{4.5}{3.5}\right)(2.77)\left(\frac{6}{3.5}\right)\left(\frac{10C}{C}\right) = 104.66$$

so that the stage value is

$$\hat{f} = (104.66)^{\frac{1}{3}} = 4.71$$

This is used to calculate the input capacitance to each stage, which can in turn be used to find the scale factors if desired.

Starting with the last stage we have

$$h_3 = \frac{\hat{f}}{g_3} = \frac{4.71}{(6/3.5)} = \frac{10C}{C_3}$$

so $C_3 = 3.64C$. For the second stage,

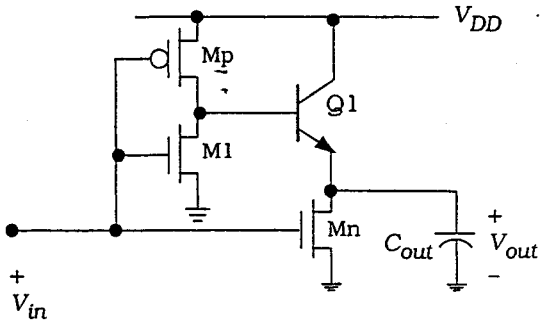
$$h_2 = \frac{\hat{f}}{b_2 g_2} = \frac{4.71}{(2.77)(4.5/3.5)} = \frac{3.64C}{C_2}$$

so $C_2 = 2.75C$. For the first stage,

$$h_1 = \frac{\hat{f}}{g_1} = \frac{4.71}{(6/3.5)} = \frac{3.64C}{C_1}$$

which gives $C_1 = C$ as required.

[8.10]The circuit is shown below.



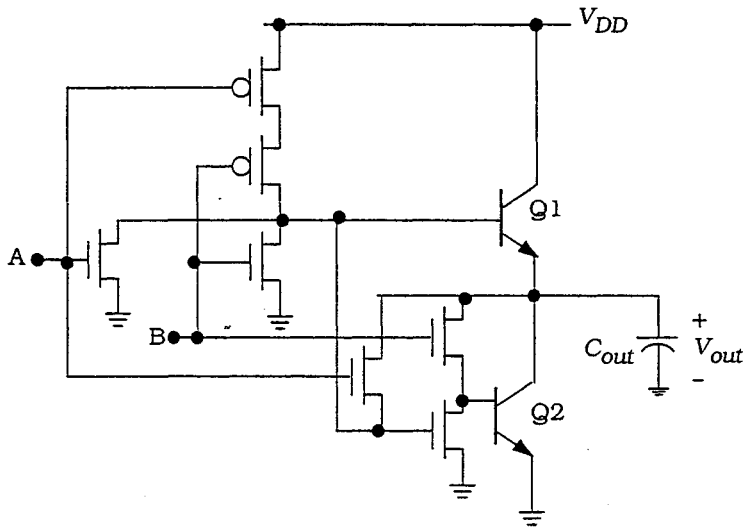
Problem [8.10]

The output swing is computed from

$$V_{OH} = V_{DD} - V_{BE}$$
$$V_{OL} = 0$$

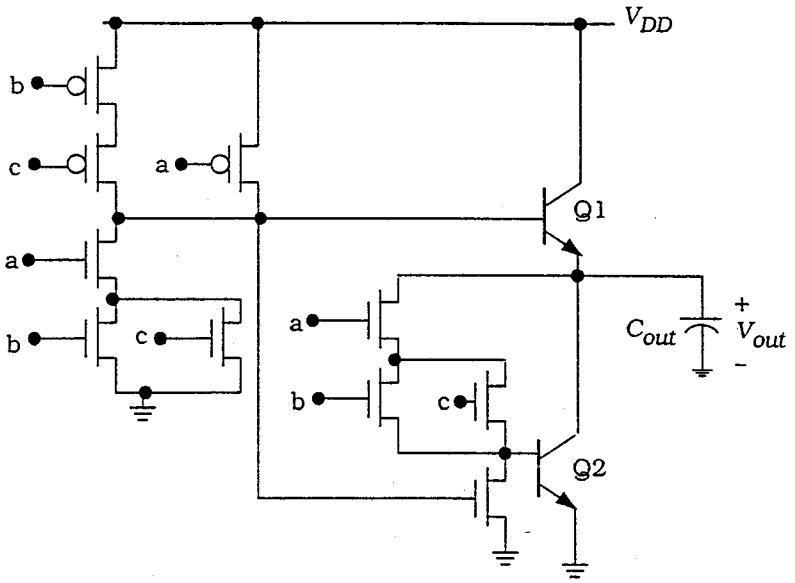
as V_{OH} because the nFET allows the output to discharge to 0 V.

[8.11]The NOR2 circuit is shown below. It illustrates how the static gate is used to drive the upper BJT, while only the nFET logic section is needed for the lower BJT.



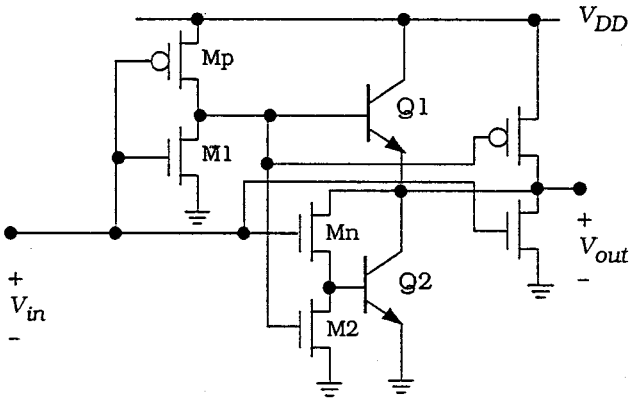
Problem [8.11]

[8.12]This is designed by using the static CMOS gate to control the upper bipolar output transistor, and the nFET logic section between the base and collector of the lower BJT. The lower BJT also has a pull-down FET on the base to drain off charge.



Problem [8.12]

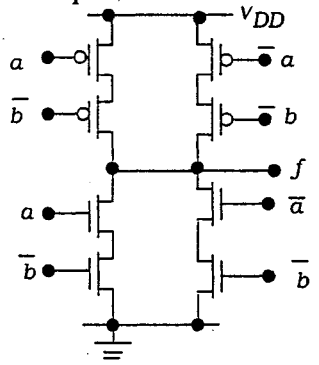
[8.13] We can wire a pair of FETs at the output (although this introduces other problems).



Problem [8.13]

Chapter 9

[9.1] (a) Yes. The circuit is shown. It is based on the symmetry in the truth table where 2 input combinations yield a 0 output, while the other two give a logic 1.



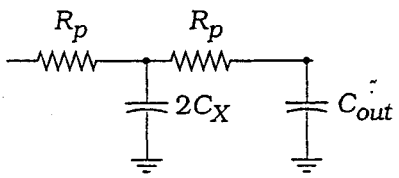
Problem [9.1]

(b) No, this is not an intelligent choice (although it is an iteresting circuit). Why not? Use the function table to write the SOP expression

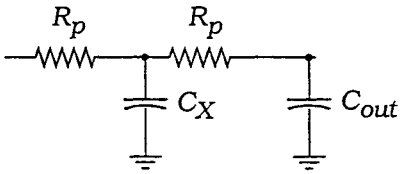
$$\begin{aligned} f &= \bar{a} \cdot b + a \cdot b \\ &= (\bar{a} + a) \cdot b \\ &= b \end{aligned}$$

so no gate is needed at all! This is a useful point, as some may try to build a complicated logic gate without looking for the simplest solution.

[9.2] For the standard circuit, we use the RC equivalent shown in (a), while the charge chain for the mirror circuit is shown in (b). The difference between the two is effect of the 48 fF capacitor: it is shared with the other branch in (a), doubling the value at that node.



(a) AOI has $2C_X$ due to other 2 pFETs



(b) Mirror only has C_X

Problem [9.2]

The resistance is

$$R_p = \frac{1}{(250\times10^{-6})(2.65)} = 1,509.4\Omega$$

(i) For the standard circuit,

$$t_{LH} = 2.2[(2R_p)C_{out} + 2R_pC_{pX}] = 1.8\text{ns}$$

(ii) For the mirror circuit,

$$t_{LH} = 2.2[(2R_p)C_{out} + R_pC_{pX}] = 1.32\text{ns}$$

[9.3] (a) Using equation (9.3) of the text allows us to write

$$\frac{\beta_n}{\beta_p} = \frac{(V_{DD} - |V_{Tp}|)^2}{2(V_{DD} - V_{Tn})V_{OL} - V_{OL}^2} = \frac{(4.15)^2}{2(4.3)(0.3) - (0.3)^2} = 6.92$$

This means

$$\frac{\beta_n}{\beta_p} = 6.92 = \frac{k'_n(4)}{k'_p(W/L)_p} = \frac{(120)(4)}{(55)(W/L)_p}$$

so that the pFET aspect ratio must have $(W/L)_p = 1.26$.

(b) Now we have

$$\frac{\beta_n}{\beta_p} = \frac{k'_n(4)}{k'_p3} = 2.91$$

so

$$V_{OL} = 4.3 - \sqrt{4.3^2 - \frac{(4.15)^2}{2.91}} = 1.54\text{ V}$$

Note that this is too large to be interpreted as a logic 0 as the input to an identical stage.

[9.4] The NOT gate is defined by

$$\frac{\beta_n}{\beta_p} = \frac{120(W/L)_n}{55(2)} = 6.92$$

which gives $(W/L)_n = 6.34$. For a NAND2 gate, the each nFET should have an aspect ratio of

$$\left(\frac{W}{L}\right)_N = 2\left(\frac{W}{L}\right)_n = 12.68$$

while a NAND3 gate would use nFETs of size

$$\left(\frac{W}{L}\right)_N = 3\left(\frac{W}{L}\right)_n = 19.02$$

To compare the area, let us normalize the channel length to $L = 1$ unit and compare gate areas. For the NAND2, the gate area of the nFETs is

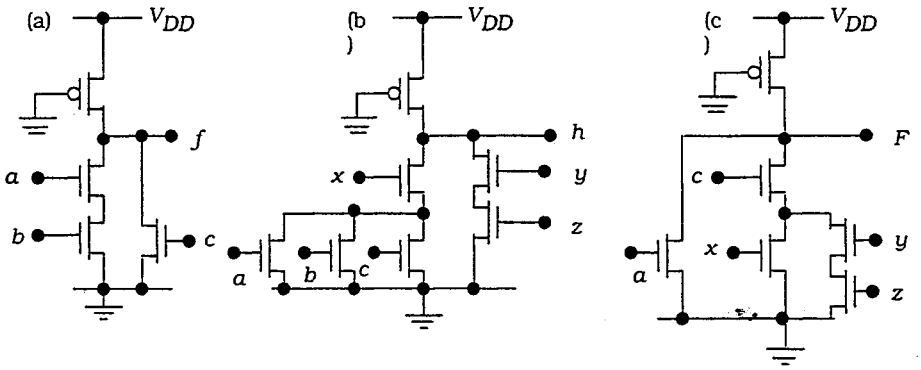
$$A = 2(12.68) = 25.36 \text{ square units}$$

while the area of the nFETs is

$$A = 3(19.02) = 51.06 \text{ square units}$$

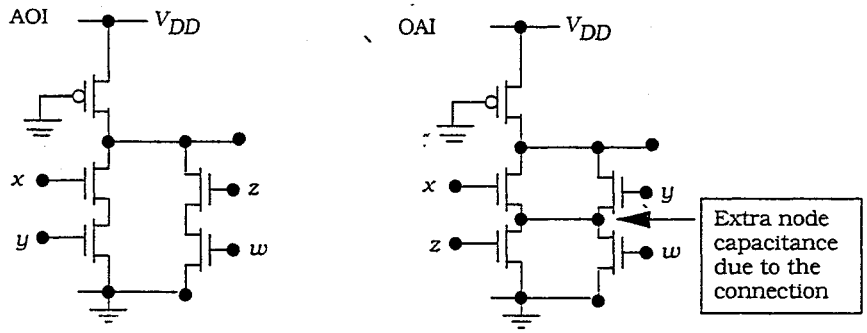
Since the pFET sizes can be the same for both gates, this illustrates that the nFET gate area will increase by a factor of about 2 when a NAND2 gate is changed to a NAND3.

[9.5] The circuits are shown below.



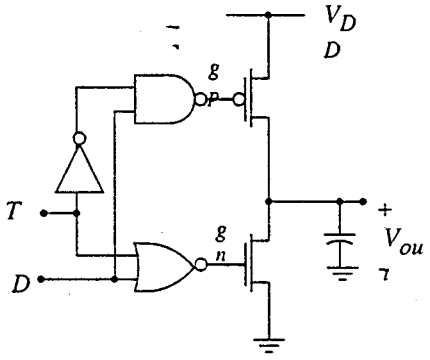
Problem [9.5]

[9.6] The AOI and OAI circuits are shown below. The OAI will have a slower discharge because of the higher capacitance at the node indicated, so the AOI is preferred for fast switching (t_{HL}).



Problem [9.6]

[9.7] One circuit is shown below.



The input logic forms to variables that control the output FETs

$$g_p = \overline{\overline{T} \cdot D} = T + \overline{D}$$

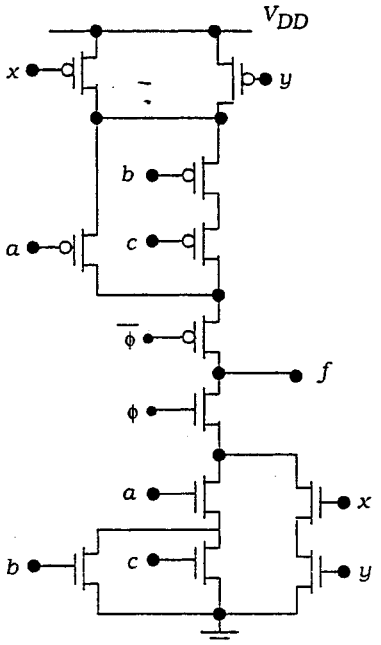
$$g_n = \overline{T + D} = \overline{T} \cdot \overline{D}$$

When $T = 1$, $g_n = 0$ (which turns off the nFET) and $g_p = 1$ which turns off the pFET. When $T = 0$, the control signals are $g_n = \overline{D} = g_p$. If $D = 0$, then the nFET is on and the output is 0, while $D = 1$ turns on the pFET at gives a 1 at the output.

[9.8] A C^2MOS circuit for the function

$$f = \overline{a \cdot (b + c) + x \cdot y}$$

is constructed by designing a standard CMOS logic gate, and then inserting clocked transistors between the output and the respective FET logic arrays.



Problem [9.8]

[9.9] The leakage is expressed by

$$i_n - i_p = - C_{out}\frac{dV_{out}}{dt}$$

which has the solution

$$V_{out}(t) = V_{out}(0) - \frac{i_n - i_p}{C_{out}}t$$

Hold times are computed by solving for time:

$$t_h = \left(\frac{C_{out}}{i_n - i_p}\right)[V_{DD}(0) - V_1]$$

where V_1 is the minimum logic 1 voltage.

(a) With the values given

$$t_h = \left(\frac{76\times10^{-15}}{0.46\times10^{-6} - 0.127\times10^{-6}}\right)[5 - 2.4] = 593.4 \text{ ns}$$

(b) Repeating with a lower power supply voltage gives

$$t_h = \left(\frac{76\times10^{-15}}{0.46\times10^{-6} - 0.127\times10^{-6}}\right)[3.3 - 2.4] = 205.41 \text{ ns}$$

The hold times are short because of the small capacitance and the relatively large nFET leakage current stated.

[9.10] (a) We start with the capacitor I-V equation in the form

$$I_L = B\left(\frac{V}{V_0}\right) = -C_{out}\frac{dV}{dt}$$

then rearrange and integrate:

$$\int_{V_0}^{V(t)} \frac{dV}{V} = -\frac{B}{C_{out}V_0}\int_0^t dt$$

Solving

$$\ln\left(\frac{V(t)}{V_0}\right) = -\frac{B}{C_{out}V_0}t$$

or

$$V(t) = V_0 e^{-t/\tau}$$

where the time constant is

$$\tau = \frac{C_{out}V_0}{B}$$

(b) Write

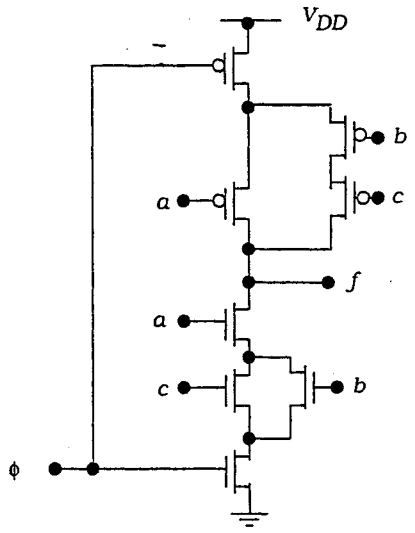
$$t = \frac{C_{out}V_0}{B}\ln\left(\frac{V_0}{V(t)}\right)$$

For the hold time, $V(t_h) = 0.4\ V_0$ so

$$t_h = \frac{C_{out}V_0}{B}\ln\left(\frac{V_0}{0.4V_0}\right) = \frac{C_{out}V_0}{B}\ln(2.5) = \frac{C_{out}V_0}{B}(0.816)$$

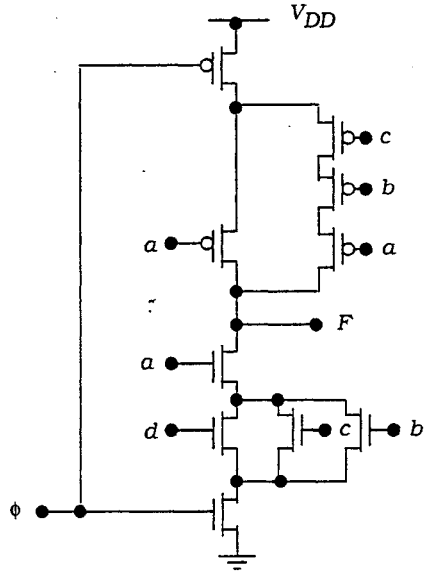
is the estimate.

[9.11] The dynamic circuit is shown below.



Problem [9.11]

[9.12] The dynamic circuit has the usual structure: an nFET logic array sandwiched between a clocked complementary pair.



Problem [9.12]

[9.13] The total charge in the initial configuration is

$$Q_T = 5(100) = 500 \text{ fC}$$

so equating this to the final distribution gives

$$Q_T = (100 + 37)V_f = 500 \text{ fC}$$

Solving,

$$V_f = \left(\frac{100}{137}\right)5 = 3.65 \text{ V}$$

[9.14] (a) The charge sharing calculation is

$$\begin{aligned} Q_T &= 2(37)V_{max} \\ &= [(37)(3) + 85]V_f \end{aligned}$$

where $V_{max} = 4.25$ V (ignoring body bias). Then

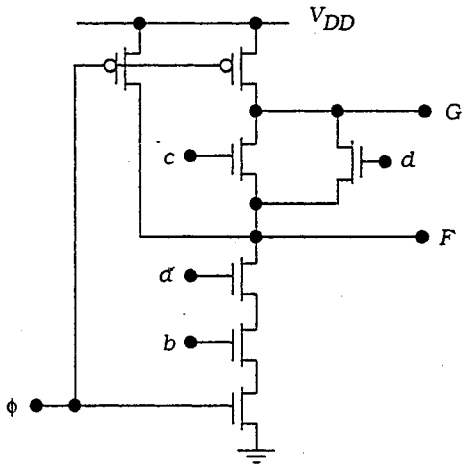
$$V_f = \left(\frac{74}{196}\right)4.25 = 1.60 \text{ V}$$

(b) For this problem, note that only the charge on two of the initially-charged capacitors contribute to the final sharing problem. Equating initial and fiinal values gives

$$\begin{aligned} Q_T &= 2(37)V_{max} \\ &= [(37)(2) + 85]V_f \end{aligned}$$

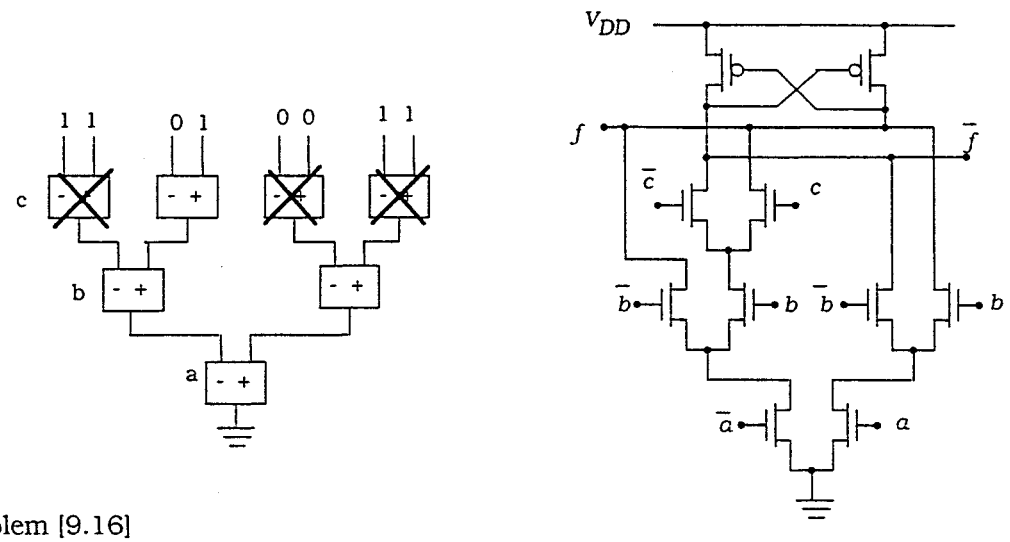
which gives $V_f = 1.98$ V.

[9.15] Construct the logic arrays separately, then embed them in the general circuit. This gives the circuit shown.



Problelm [9.15]

[9.16] Using the technique discussed in the book, we start with the general tree and then reduce. The pairs marked in bold X's are eliminated because the input pairs are identical. The resulting nFET tree has only 4 pairs. Translating the tree to circuits and adding a pFET latch gives the final circuit.



Problem [9.16]

Chapter 10

It should be noted that there are usually several ways to construct the Verilog code for any given problem. The solutions listed here are written in the style introduced in the text.

[10.1]

```
module Prob_1 (F1, F2, a, b, c, d) ;
   input a, b, c, d ;
   output F1, F2 ;
   wire w1 ;
   nor (F1, a, b) ;
   and a1 (w1, a, b, c) ;
   and a2 (F2, w1, d) ;
endmodule
```

[10.2]

```
module Prob_2 (out_1, out_2, a, b, c ) ;
   input a, b, c ;
```

```
    output out_1, out_2 ;
    wire w1 ;
    xor (w1, a, b) ;
    xnor(out_1, w1, c) ;
    and(out_2, a, b, c ) ;
endmodule
```

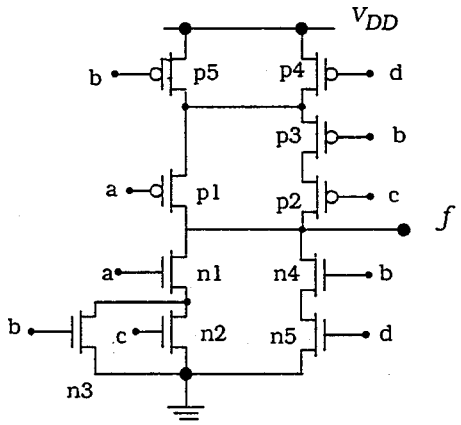
[10.3]

```
module sr_nand (out, not_out, in_1, in_2) ;
    input in_1, in_2 ;
    output out, not_out;
    nand #2 g1 (out, in_1, not_out), #2 g2 (not_out, in_2, out) ;
endmodule
```

[10.4]

```
module decoder (d0, d1, d2, d3, s_1, s_0) ;
    input s_1, s_0 ;
    output d0, d1, d2, d ;
    wire not_s0, not_s1 ;
    not #1 inv0 (not_s0, s_0) ;
    not #1 inv1 (not_s1, s_1) ;
    and #2 a0 (d0, not_s0, not_s1) ;
    and #2 a1 (d1, s_0, not_s1) ;
    and #2 a2 (d2, not_s0, s1) ;
    and #2 a3 (d3, s0, s1) ;
endmodule
```

[10.5]The circuit diagram for the static gate is shown in the drawing. The FETs are

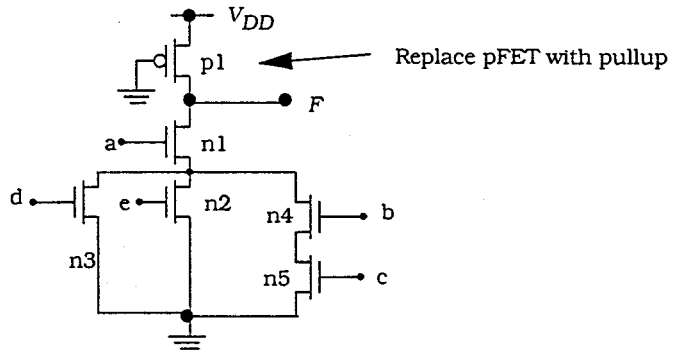


Problem [10.5]

labeled to identify them in the code.

```
module AOI_gate(f, a, b, c, d) ;
   input a, b, c, d ;
   output f ;
   wire wn1, wn2, wp1, wp2 ;
   supply1 vdd ;
   supply0 gnd ;
   nmos n1 (f, wn1, a) ,
        n2 (wn1, gnd, b) ,
        n3 (wn1, gnd, c) ,
        n4 (f, wn2, b) ,
        n5 (wn2, gnd, d) ;
   pmos p1 (f, vdd, a) ,
        p2 (f, wp1, a) ,
        p3 (wp1, wp2, b) ,
        p4 (vdd, wp2, d) ,
        p5 (vdd, wp2, b) ;
   endmodule
```

[10.6]The circuit diagram for the static gate is shown in the drawing using FET labels to help write the Verilog listing.




```
module AOI_gate_ex (F, a, b, c, d, e) ;
    input a, b, c, d, e;
    output F;
    wire wn1, wn2, wp1, wp2 ;
    supply1 vdd ;
    suppliy0 gnd ;
    nmos n1 (f, wn1, a) ,
            n2 (wn1, gnd, d) ,
            n3 (wn1, gnd, e) ,
            n4 (wn1, wn2, b) ,
            n5 (wn2, gnd, c) ;
    pullup (f) ; // This is a simple resistor model in place of the pFET
    /* The pFET would be included using
        pmos p1 (f, vdd, 0);
    in the code in place of the pullup */
    endmodule
```

[10.7]The TG MUX listing is constructed below.

```
module CMOS_MUX (F, p0, p1, s, s_not) ;
    input p0, p1, s, s_not;
    output F;
    cmos #2 tg0 (F, p0, s_not, s ) ;
    cmos #2 tg1 (F, p1, s, s_not) ;
endmodule
```

[10.8]

```
module two_phase_clock (clk, clk_bar) ;
    output clk, clk_bar ;
    reg clk, clk_bar ;
initial
    begin
        clk = 0 ;
        clk_bar = 1 ;
    end
always
    begin
        # 40 ;
            clk = ~ clk_bar ;
            clk_bar = ~ clk ;
    end
endmodule
```

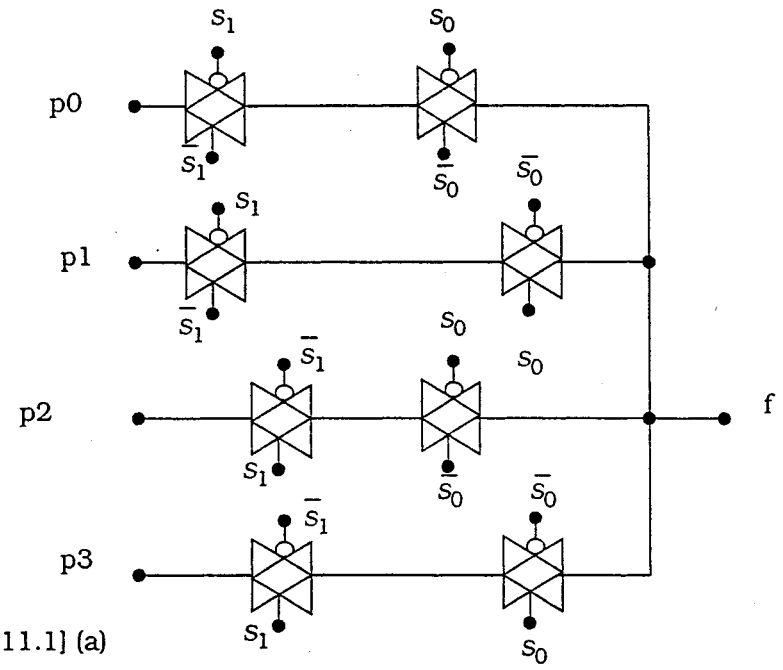
[10.9]We will write this in a style that illustrates how descriptive levels can be mixed.

```
module logic (q, a, b, c, e, f ) ;
    output f ;
    input a, b, c, e, f ;
    reg clk;
    not n1 (a_bar, a ) ,
         n2 (c_bar, c ) ;
    assign
        A = (a_bar & b) | (c & e) | (c_bar & f) ;
endmodule

module clock (clk) ;
    reg clk ;
    initial
        clk = 0 ;
    always
        begin
        # 5
        clk = ~ clk ;
        end
endmodule
module dff (q, A, clk) ;
    output q ;
    input A, clk ;
    always @ (posedge clk ) ;
        q = A ;
endmodule
```

Chapter 11

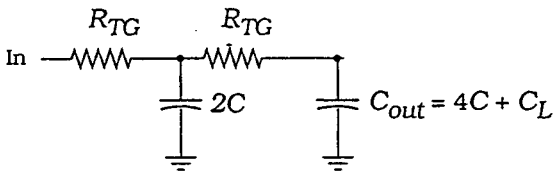
[11.1] (a) The TG mux circuit is shown below (taken from Problem [2/14])



Problem [11.1] (a)

```
module TG_MUX (f, p0, p1, p2, p3, s1, s1_not, s2, s2_not) ;
    input p0, p1, p2, p3, s1, s1_not, s2, s2_not ;
    output f ;
    wire w0, w1, w2, w3, ;
    cmos tg0_0 (p0, w0, s1_not, s1 ) ;
    cmos tg0_1 (f, w0, s0_not, s0 ) ;
    cmos tg1_0 (p1, w1, s1_not, s1 ) ;
    cmos tg1_1 (f, w1, s0, s0_not ) ;
    cmos tg2_0 (p2, w2, s1, s1_not ) ;
    cmos tg2_1 (f, w2, s0_not, s0) ;
    cmos tg3_0 (p3, w3, s1, s1_not ) ;
    cmos tg3_1 (f, w3, s0, s0_not ) ;
endmodule
```

(c) Each path has two series-connected TGs giving the equivalent circuit shown below. The value of $2C$ in between the resistors is due to a C contribution from each side. The output capacitance C_{out} consists of the right side of 4 TGs (one from each path) and the external load C_L.



Problem [11.2] (c)

The time constant for a path is

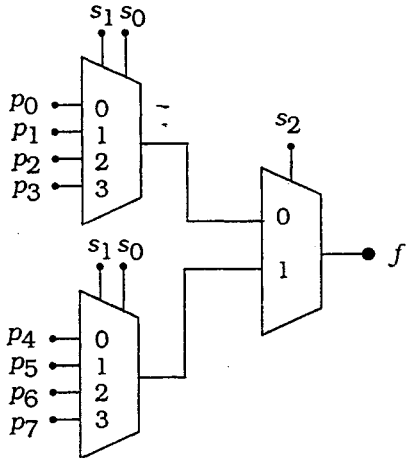
$$\begin{aligned}\tau_n &= C_{out}(2R_{TG}) + (2C)R_{TG} \\ &= (C_L + 4C)(2R_{TG}) + 2CR_{TG} \\ &= 2R_{TG}C_L + 10R_{TG}C\end{aligned}$$

This indicates that the TG circuit may be slow. The actual values depend on the aspect ratios and process parameters.

[11.2] For a 16:1 MUX, we may use a high-level approach to obtain the following.

```
module mux_16 (out, sel, p0, p1, p2, p3, p4, p5, p6, p7, p8, p9, p10, p11, p12,
      p13, p14, p15) ;
input p0, p1, p2, p3, p4, p5, p6, p7, p8, p9, p10, p11, p12, p13, p14, p15 ;
input [ 3 : 0 ] sel ;
output out ;
assign out = (sel == 2'b0000) ? p0 :
             (sel == 2'b0001) ? p1 :
             (sel == 2'b0010) ? p2 :
             (sel == 2'b0011) ? p3 :
             (sel == 2'b0100) ? p4 :
             (sel == 2'b0101) ? p5 :
             (sel == 2'b0110) ? p6 :
             (sel == 2'b0111) ? p7 :
             (sel == 2'b1000) ? p8 :
             (sel == 2'b1001) ? p9 :
             (sel == 2'b1010) ? p10 :
             (sel == 2'b1011) ? p11 :
             (sel == 2'b1100) ? p12 :
             (sel == 2'b1101) ? p13 :
             (sel == 2'b1110) ? p14 :
             p15 ;
endmodule
```

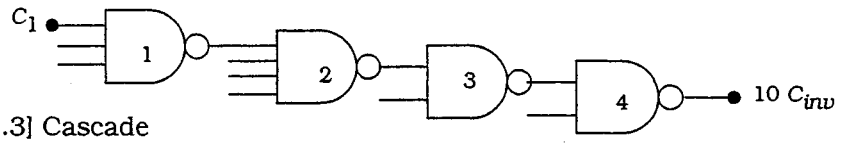
[11.3] (a) The 8:1 MUX is shown below.



Problem [11.3]

(b) The easiest implementations are the NAND circuits shown in Figures 11.1 and 11.4 of the text (not reproduced here). TGs could also be used, but they will be harder to apply to the Logical Effort calculation in part (c) of the problem.

(c) Using the NAND gates, the cascade is a NAND3 to a NAND4 (for a 4:1), and then a NAND2 to a NAND2 (for the 2:1). The cascade is shown below.



Problem [11.3] Cascade

The input to the NAND3 gate is C_1. We can write

$$G = g_1 g_2 g_3 g_4 = \left(\frac{5}{3}\right)\left(\frac{6}{3}\right)\left(\frac{4}{3}\right)\left(\frac{4}{3}\right) = 5.926$$

where we have assumed that $r = 2$ for simplicity. The electrical effort is

$$H = \frac{10 C_{inv}}{C_1}$$

so

$$\hat{f} = \left(59.26 \frac{C_{inv}}{C_1}\right)^{\frac{1}{4}}$$

For a NAND3 gate, the input capacitance scales as $(3\times 3+r)C_{unit}$. If we define the NAND3 unit as $C_{unit} = C_{inv}$ we obtain

$$\hat{f} = \left(\frac{59.26}{11}\right)^{\frac{1}{4}} = 1.52$$

which provides all the values needed to complete the Logical Effort scaling of each stage.

To complete the problem, we work from the last stage towards the input.

$$h_4 = \frac{\hat{f}}{g_4} = \frac{1.52}{4/3} = 1.14 = \frac{10C_{inv}}{C_{in4}}$$

so $C_{in4} = 8.77C_{inv}$. Similarly,

$$h_3 = \frac{\hat{f}}{g_3} = \frac{1.52}{4/3} = 1.14 = \frac{8.77C_{inv}}{C_{in3}}$$

gives $C_{in3} = 7.69C_{inv}$. For the second stage

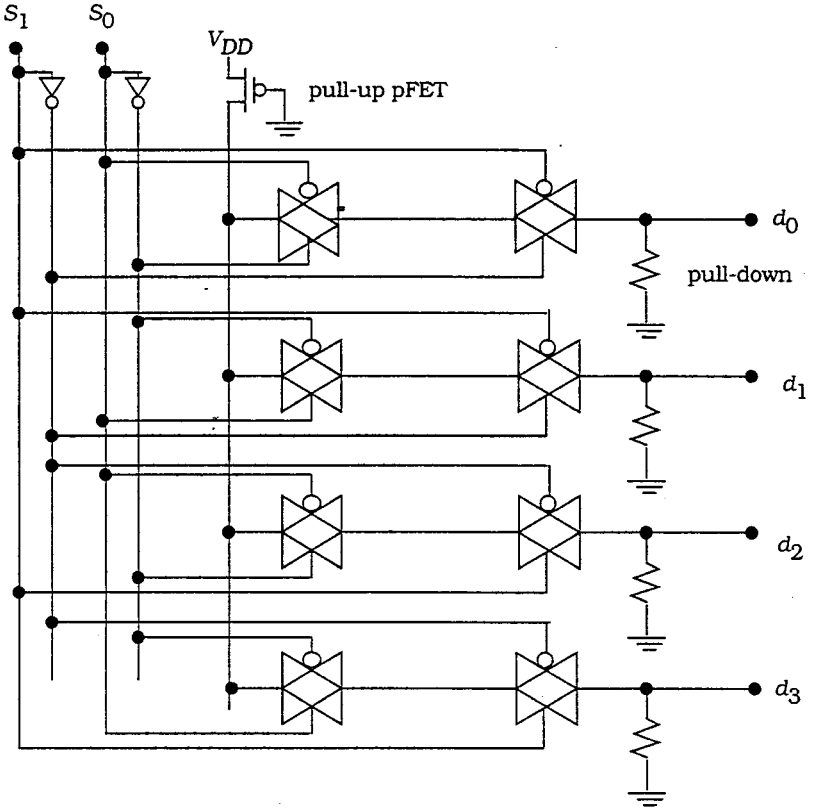
$$h_2 = \frac{\hat{f}}{g_2} = \frac{1.52}{6/3} = 0.76 = \frac{7.69C_{inv}}{C_{in2}}$$

so $C_{in2} = 10.12C_{inv}$. Finally,

$$h_1 = \frac{\hat{f}}{g_1} = \frac{1.52}{5/3} = 0.912 = \frac{10.12C_{inv}}{C_{in2}}$$

gives us $C_{in1} = 11.1C_{inv}$. These values, along with the input capacitance equations, provide the sizing of each stage in the chain.

[11.4] The TG circuit is shown below. Note that pull-down resistors are used at the output to insure that the voltages can reach 0.

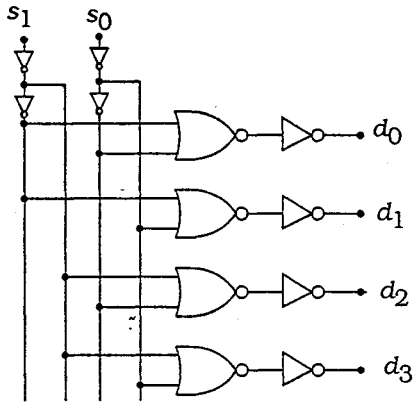


Problem [11.4]

For the Verilog listing, we can write

```
module TG_decoder (d0, d1, d2, d3, s1, s1_not, s2, s2_not) ;
input s1, s1_not, s2, s2_not ;
output d0, d1, d2, d3 ;
wire w0, w1, w2, w3, wp;
supply1 vdd ;
supply0 gnd ;
pmos pu (vdd, wp, gnd ) ;
cmos tg0_0 (wp, w0, s1_not, s1 ) ;
cmos tg0_1 (d0, w0, s0_not, s0 ) ;
cmos tg1_0 (wp, w1, s1_not, s1 ) ;
cmos tg1_1 (d1, w1, s0, s0_not ) ;
cmos tg2_0 (wp, w2, s1, s1_not ) ;
cmos tg2_1 (d2, w2, s0_not, s0) ;
cmos tg3_0 (wp, w3, s1, s1_not ) ;
cmos tg3_1 (d3, w3, s0, s0_not ) ;
pulldown (d0) , (d1), (d2), (d3) ;
endmodule
```

[11.5] The simplest way to design this is to just add inverters to an active-high circuit!



Problem [11.5]

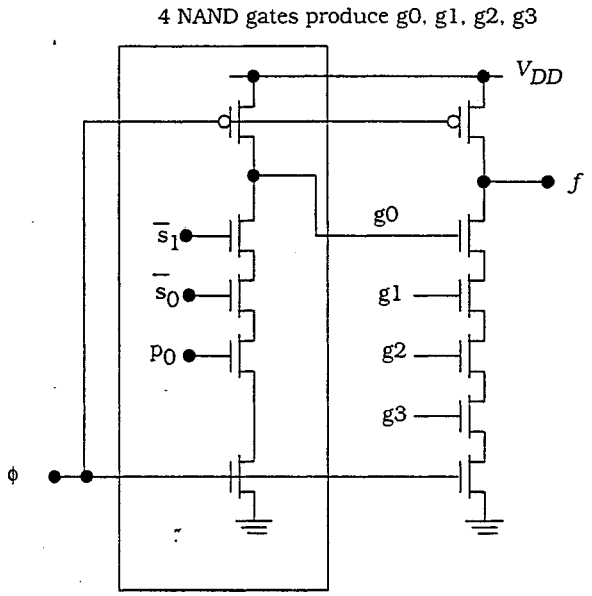
(a) The Verilog listing is

```
module decode_4_low (d0, d1, d2, d3, s0, s1) ;
input s0, s1 ;
output d0, d1, d2, d3 ;
wire w0, w1, w2, w3 ;
nor    (w3, ~s0, ~s1) ,
       (w2, ~s0, s1) ,
       (w1, s0, ~s1) ,
       (w0, s0, s1) ;
not (d0, w0 ),
```

```
        (d1, w1 ),
        (d2, w2 ),
        (d3, w3 );
endmodule
```

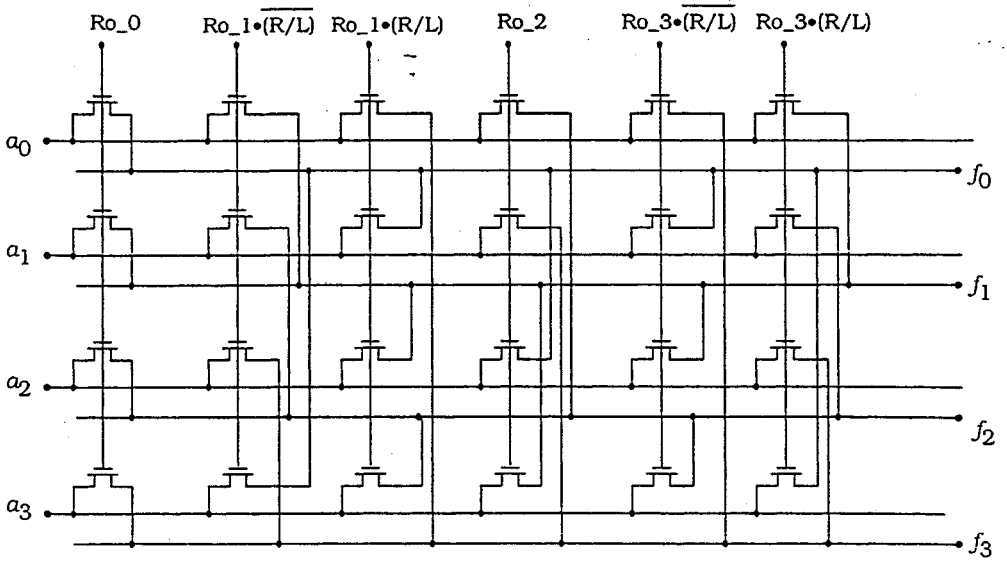
(b) To modify the circuit to include an enable control, we can expand the NOR gates to 3-inputs and add the En to each. When En =1, every output is at a logic 1. Alternately, we could put tri-state not gates to isolate the outputs. The variation on either is straightforward and not shown explicitly here.

[11.6] The circuit shown here uses dynamic logic and is based on the logic diagram in Figure 11.4(b). Four NAND3 gates are used for the inputs (only one is shown in the circuit) to produce outputs g0, g1, g2, g3; these are fed into a NAND4 gate which has the MUXed output f.



Problem [11.6]

[11.7] A design for the switching array is shown below. This combines the rotate right



Problem [11.7]

and rotate left arrays and eliminates the redundancy for rotate 0 and 2. The control signals can be produced by a simple active high decoder with the outputs ANDed with the *(R/L)* signal to specify right or left rotation.

[11.8] A structural listing is a little tedious, as it shows every gate and connection.

```
module equality (Equal, a, b );
input [ 7 : 0 ] a, b ;
output Equal ;
wire w0, w1, w2, w3, w4, w5, w6, w7 ;
wire wa, wb ;
xnor   g0 (w0, a[0], b[0] ),
       g1 (w1, a[1], b[1] ),
       g2 (w1, a[2], b[2] ),
       g3 (w2, a[3], b[3] ),
       g4 (w4, a[4], b[4] ),
       g5 (w5, a[5], b[5] ),
       g6 (w6, a[6], b[6] ),
       g7 (w7, a[7], b[7] );
nand n1 (wa, w0, w1, w2, w3 );
nand n2 (wb, w4, w5, w6, w7 );
nor (Equal, wa, wb 0;
endmodule
```

[11.9] This listing is a high-level description that uses a 4 bit register called bit_reg that stores the bits and then shifts with the clock edge. The Verilog concantenation and shift operations are used to achieve the bit movement

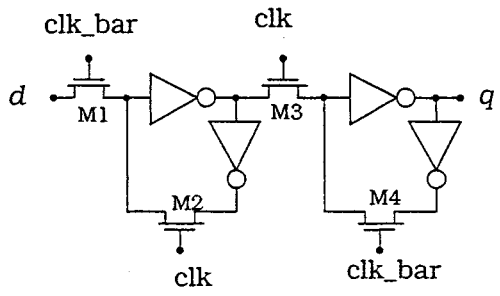
```
module shift_reg_4b (d_out, d_in , clk );
input d_in, clk ;
output d_out ;
reg [ 0 : 3 ] bit_reg ;
assign d_out = bit_reg[ 3 ] ;
assign @ (posedge clk )
   begin
   bit_reg <= { d_in, bit_reg[1:3] } ;
   end
endmodule
```

A more straighforward approach is to define a DFF module and then instance it into the structural code. For example

```
module dff (q, d, clk );
input d, clk ;
output q;
always @ (posedge clk)
   q = d ;
endmodule

module shift4 (d_out, d_in, clk );
input d_in, clk ;
output d_out ;
wire w0, w1, w2 ;
reg w0, w1, w2, d_out ;
dff g0 (w0, d_in, clk );
dff g1 (w1, w0, clk );
dff g2 (w2, w1, clk );
dff g3 (d_out, w2, clk );
endmodule
```

(b) A CMOS switch-level circuit is shown below.



Problem [11.9]

(c) For the FF shown, we can define one module by

```
module cmos_dff (q, d, clk, clk_bar ) ;
input d, clk, clk_bar ;
output q ;
reg q ;
nmos (w1, d, clk_bar );
not g1 (w2, w1 ) ;
not g2 (wf1, w2 ) ;
nmos (w1, wf1, clk ) ;
nmos (w2, d, clk );
not g3 (q, w2 ) ;
not g4 (wf2, q) ;
nmos (w3, wf2, clk ) ;
endmodule
```

This can be instanced into the shift register by allowing for the clk_bar signal.

[11.10] A simple listing is

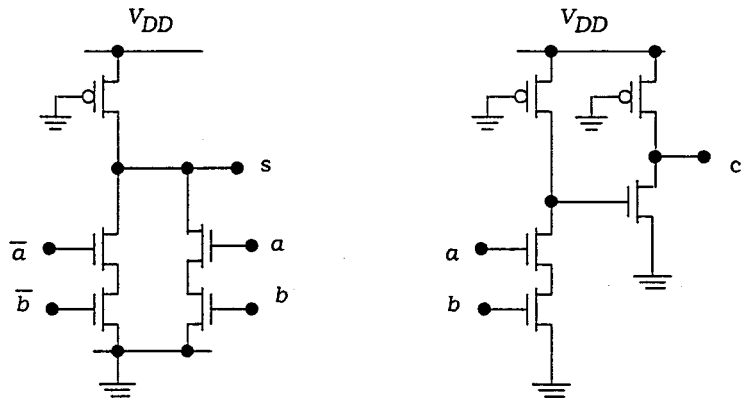
```
module reg8b (q, d, clk, En );
output [ 7 : 0 ]q ;
input [ 7 : 0 ] d ;
input clk, En ;
reg [ 7 : 0 ] q ;
initial q = 0 ;
always @ ( (posedge clk) and En )
      q = d ;
   else
      q = 0 ;
endmodule
```

[11.11] The code below uses resistive nmos switches since the transistors are used as pass devices.

```
module register (Qa, Qb, D, WE, Re_a, Re_b);
input D, WE, Re_a, Re_b ;
output Qa, Ql ;
wire win, ws, wo ;
rnmos (win, D, WE );
not g1 (ws, win ), g2 (win, ws ),g3 (wo, ws );
rnmos (Qa, wo, Re_a );
rnmos (Qb, wo, Re_b );
endmodule
```

Chapter 12

[12.1] The simplest gates are shown below.



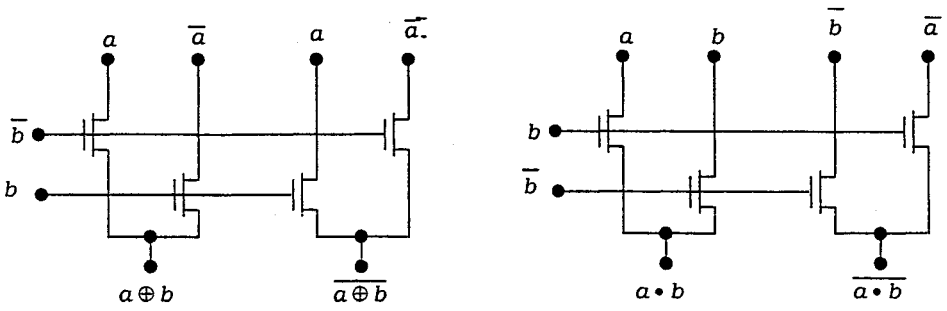
Problem [12.1]

These can be described by the following Verilog listings.

```
module sum (sum, a, b ) ;
input a, b ;
output sum ;
wire wn1, wn2, wn3 ;
supply1 vdd ;
supply0 gnd ;
nmos n1 (sum, wn1, ~a ) ,
        n2 (wn1, gnd, ~b) ,
        n3 (sum, wn2, a) ,
        n4 (wn2, gnd, b) ;
pmos p1 (s, vdd, gnd) ;
endmodule

module carry (c, a, b ) ;
input a, b ;
output c;
wire wn1, wn2 ;
supply1 vdd ;
supply0 gnd ;
nmos n1 (wn1, wn2, a ) ,
        n2 (wn2, gnd, b) ;
pmos p1 (wn1, vdd, gnd);
nmos  n3 (c, gnd, wn1) ;
pmos p2 (c, vdd, gnd) ;
endmodule
```

[12.2] (a) The CPL circuits needed for the sum and carry are shown below.



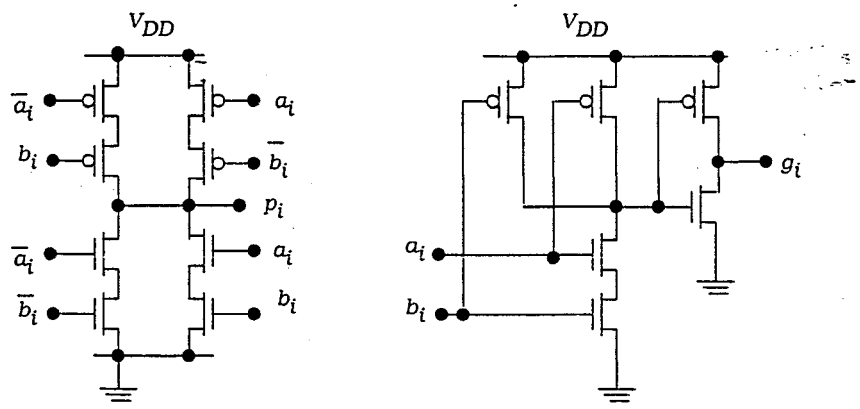
Sum circuit

Carry circuit

(b) A Verilog description for a two-input array is as follows

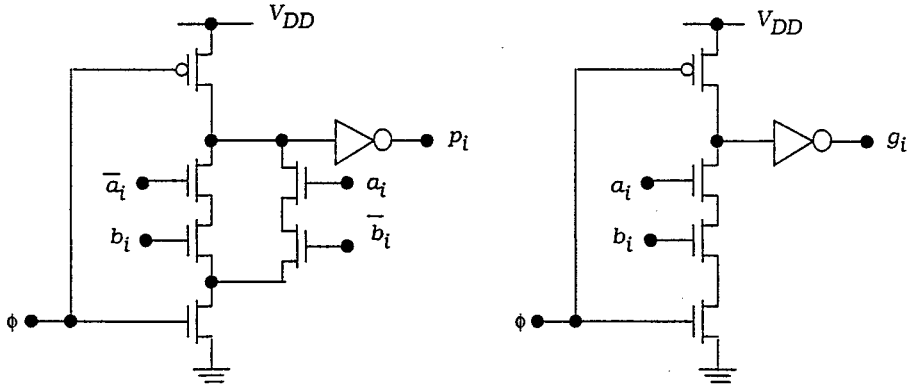
```
module CPL_2 (f1, f2, A, B, C, D) ;
input A, B, C, D;
output f1, f2 ;
nmos n1 (A, f1, a ) ,
       n2 (wn2, gnd, b) ;
nmos  n3 (c, gnd, wn1),
       n4 (wn2, gnd, b);
endmodule
```

[12.3] (a) The static circuits are



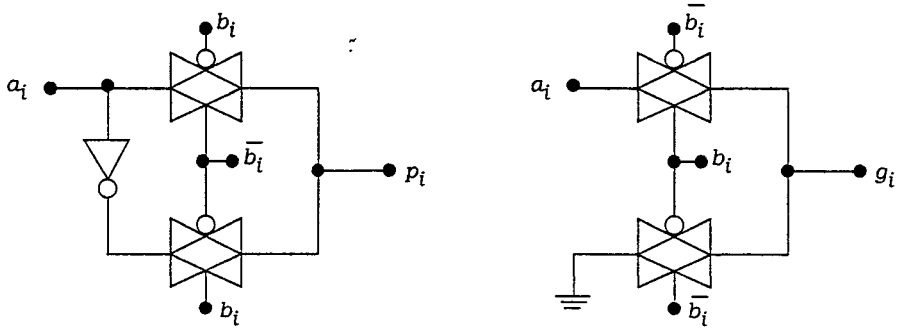
Problem [12.3] (a)

(b) Domino designs give a similar structure



Problem [12.3] (b)

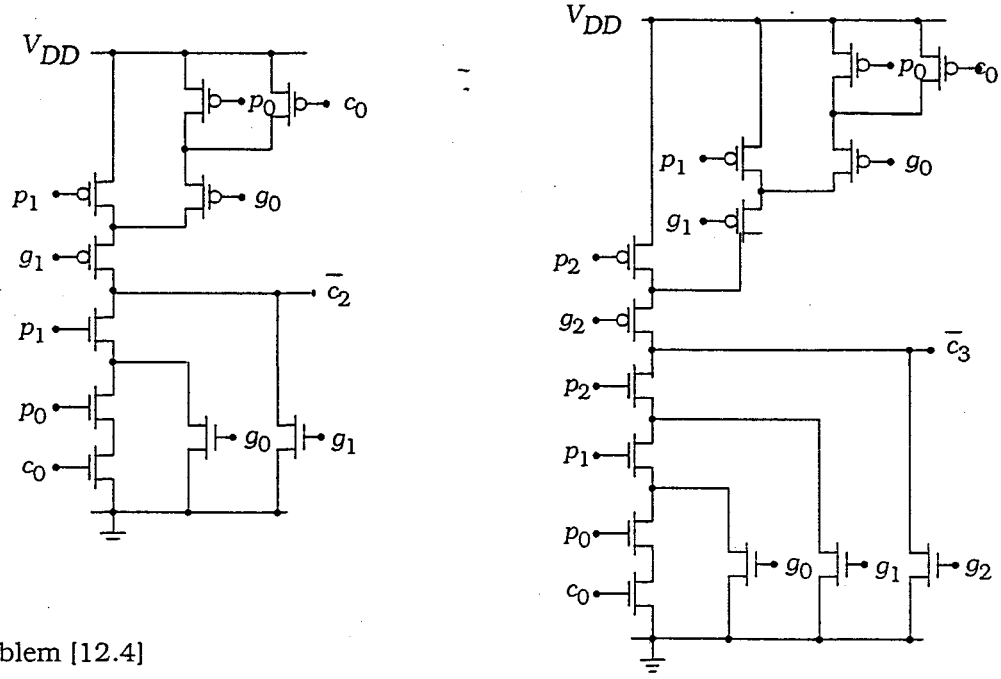
(c) The TG designs are based on a 2:1 MUX design (although others are possible). Note



Problem [12.3] (b)

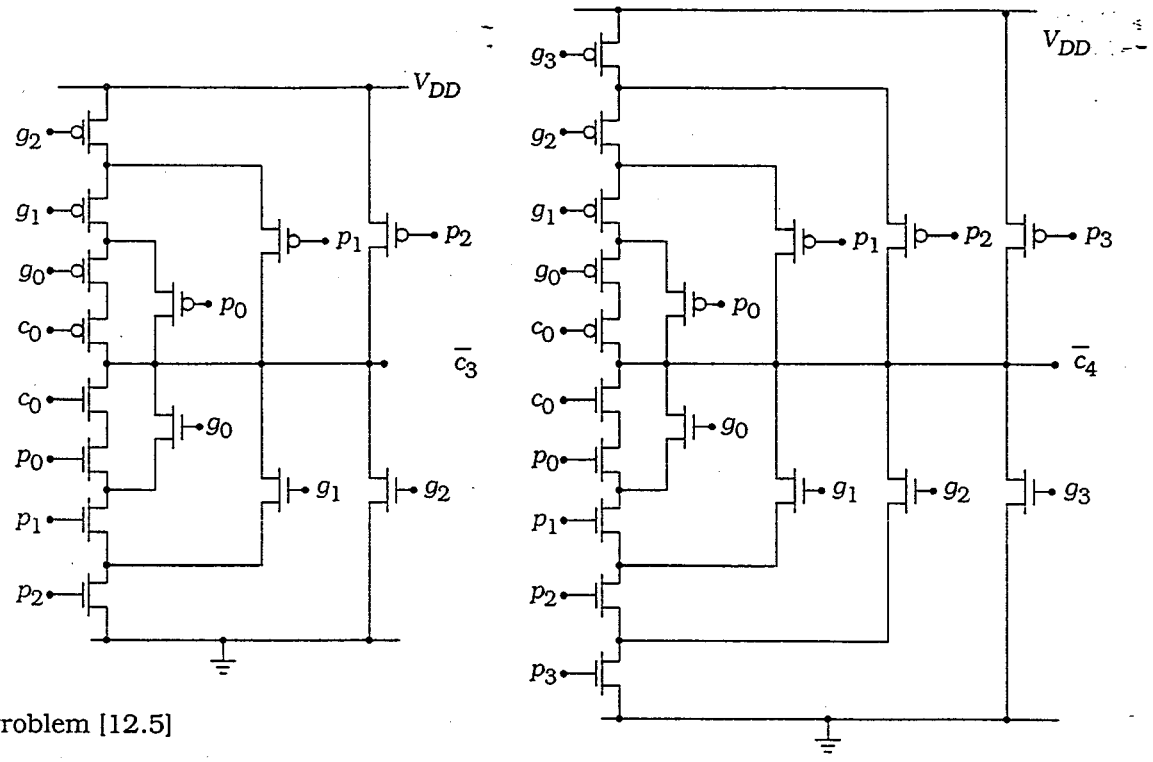
that the generate circuit produces an output of a_i if $b_i = 1$, and an automatic output of 0 if $b_i = 0$. This is the AND operation.

[12.4]



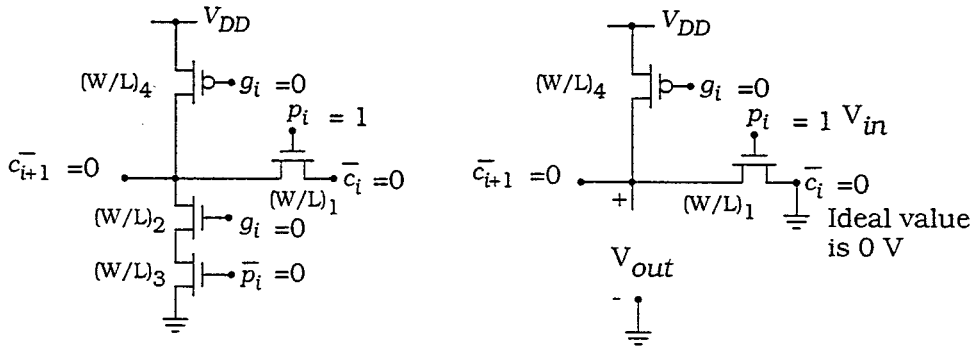
Problem [12.4]

[12.5] The mirror circuits are constructed as shown in the figure.



Problem [12.5]

[12.6] Sizing enters the problem when $\overline{c}_i = 0$ and p_i=1as shown in the left side of the drawing. Eliminating the FETs that are OFF yields the pseudo-nMOS circuitry shown on the right. The ratio of FETs M1 and M4 determines the output voltage V_{out} for $\overline{c}_{i+1}$. We



Problem [12.6]

will assume that the propagate voltage representing p_i has an ideal value of $V_{in} = V_{DD}$, and that $\bar{c}_i = 0$ is a perfect ground.

To design the circuit, we use the pseudo-nMOS ratio equation for a reasonable value of V_{OL}, say, $V_{OL} = 0.2$ V.

$$\frac{\beta_{n1}}{\beta_{p4}} = \frac{(V_{DD} - |V_{Tp}|)^2}{2(V_{DD} - V_{Tn})V_{OL} - V_{OL}^2} = \frac{(2.3)^2}{2(2.3)(0.2) - (0.2)^2} = 6.01$$

This means

$$\frac{\beta_{n1}}{\beta_{p4}} = 6.01 = \frac{k'_n(W/L)_{n1}}{k'_p(W/L)_{p4}} = \frac{r(W/L)_{n1}}{(W/L)_{p4}}$$

so that the two are sized according to

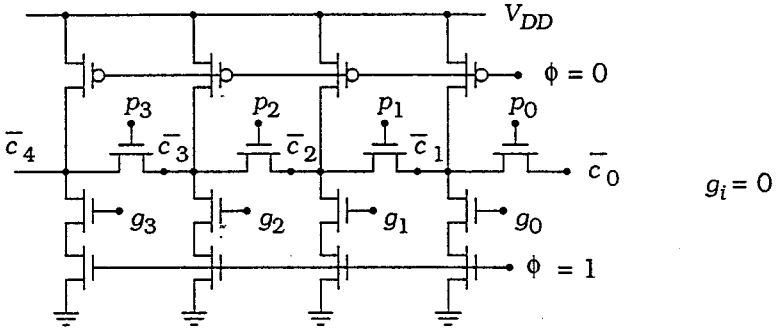
$$(W/L)_{n1} = 2.4(W/L)_{p4}$$

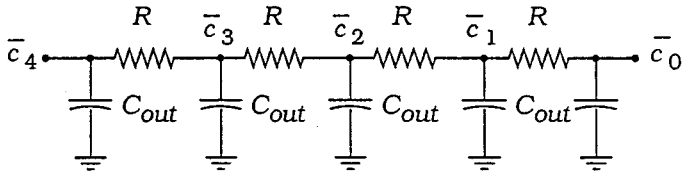
The values will changed if the input conditions are different, but the procedure is the same.

[12.7] (a) The evolution of the ladder is shown for the case where the carry-in propagates all the way through the chain. If any generate bit is a 1, the corresponding propagate bit is a 0 and the carry chain is opened.

(b) Since every stage precharges at the same time, the voltage at $\bar{c}_4$ is V_{DD} corresponding to a carry-out of $c_4 = 0$.

The g-input nFETs are off for a propagation event





Problem [12.3](a)

(c) Suppose that $p_i = 1$ and $g_i = 0$ for all i. Every node must store charge and is subject to a charge leakage from the OFF transistors. However, in this case the input bit $\bar{c}_0$ is provided by a static inverter (see drawing in the text) which provides hard support to the power supply or ground. The inverter is able to maintain the value on the right side of the chain so that charge leakage will have minimal effects. If the propagation is stopped

at any point with $p_i = 0$ and $g_i = 1$, the $\overline{c}_{i+1} = 0$ through the nFETs, and this provides a connection to ground.

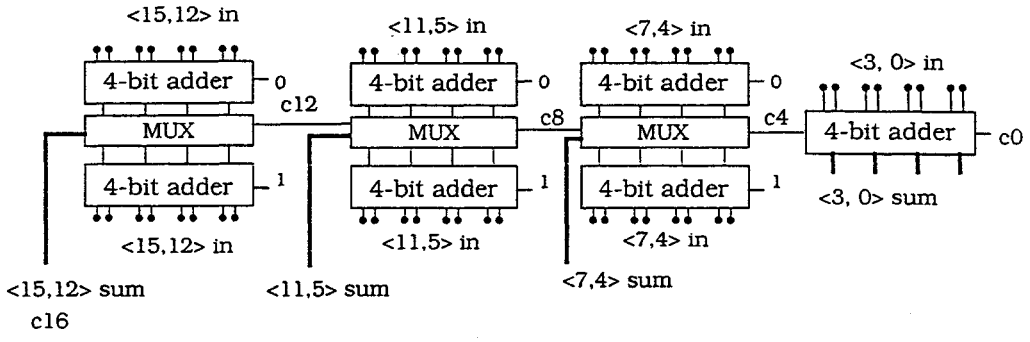
[12.8] Using equation (12.37) we have

64-bit: Average carry chain length = $\log_2(64) = \log_2(2^6) = 6$ bits

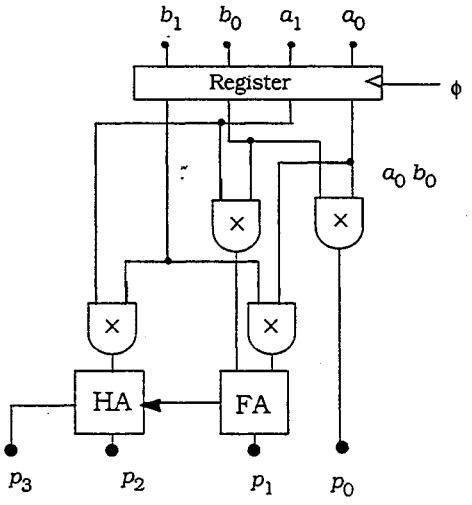
128-bit: Average carry chain length = $\log_2(128) = \log_2(2^7) = 76$ bits

---

[12.9] The block diagram is shown. Each 4-bit group produces a carry-out bit that is used to select the next 4-bit group.



[12.10] A block diagram is shown.



Problem [12.10]

The Verilog module can be written in various ways depending on the amount of structural detail desired. A high-level description of the basic array is quite simple:

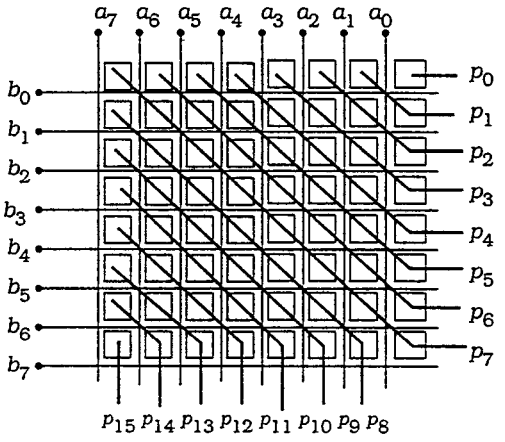
```
module 2x2_mult (p, a, b) ;
input [ 1:0 ] a, b ;
output [ 3:0 ] p;
assign
   p = a*b ;
endmodule
```

Alternates include bit-level or function level descriptions. The input latch can be added with a clocking signal. There are a large number of multiplier descriptions that can be constructed, and the interested reader is directed to the literature.

[12.11] An 8 x 8 multiplier would have the same basic form, but cannot easily be constructed using the 4x4 as a primitive. This is due to the fact that the 8x8 would require that the HA and FA locations altered depending upon their bit locations in the array. The basic cells (AND, HA) or (AND, FA) could be used. Note that the 8x8 will exhibit a long worst-case delay due to the increased length of the critical data path.

[12.12]

For an 8x8 array multiplier, we use the simple block placement demonstrated in the 4 x 4. The placement of each cell in the matrix implies the connections. For example, the upper right corner cell has inputs a_0, b_0 and multiply to produce p_0. The first diagonal in the upper right has a cell with inputs a_1, b_0 and another with inputs a_0, b_1 to produce a_0. There are also implied carry-out bits from one diagonal to the next. This illustrates how basic cells can be tiled to create the array.



[12.13] (a) for 10110011 the encoded digits are determined by writing 101 110 001 110 giving -1, -1, +1, -1.
(b) 01101101 is parsed as 011 101 110 010 to give +2, -1, -1, +1
(c) 01010010 is parsed as 010 010 001 $\bar{1}$01 to give +1, +1, +1, -1

Chapter 13

[13.1]

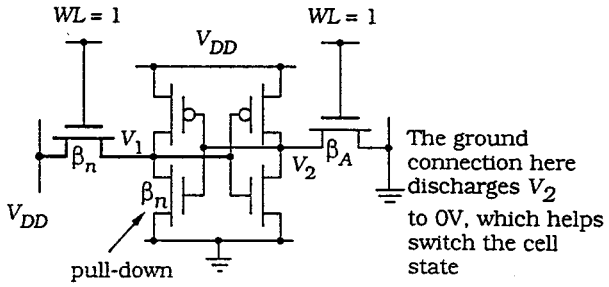
```
\\ 6-T cell
module ram_6T (bit, bit_bar, wordline) ;
    input bit, bit_bar, wordline;
    output bit, bit_bar ;
    wire wa1, wa2 ;
    supply1 vdd ;
    suppliy0 gnd ;
    nmos na1 (bit, wa1, wordline);
    nmos n1 (wa1, gnd, wa2);
    pmos p1 (wa1, vdd, wa2);
    nmos na2 (bit_bar, wa2, wordline);
    nmos n2 (wa2, gnd, wa1);
    pmos p2 (wa2, vdd, wa1);
    endmodule

\\ 4-T cell
module ram_4T (bit, bit_bar, wordline) ;
    input bit, bit_bar, wordline;
    output bit, bit_bar ;
    wire wa1, wa2 ;
    supply1 vdd ;
    suppliy0 gnd ;
    nmos na1 (bit, wa1, wordline);
    nmos n1 (wa1, gnd, wa2);
    pullup (wa1);
    nmos na2 (bit_bar, wa2, wordline);
    nmos n2 (wa2, gnd, wa1);
    pullup (wa2);
    endmodule
```

[13.2] The Verilog statements are quite simple.

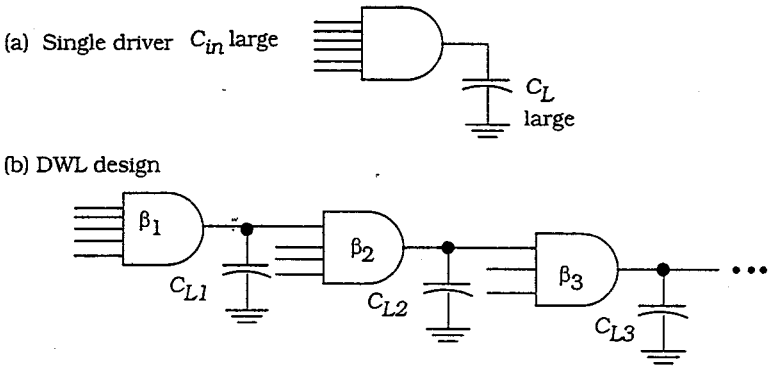
```
reg [ 31 : 0 ] mem [ 0 : 2047] ;
reg [ 7: 0 ] storage [ 0 : 16383 ] ;
reg [ 7 : 0 ] file [ 08191 ] ;
```

[13.3] Yes. This is because the complementary input will aid the cell in swtiching states. This design is actually used in many commericial SRAMs to conserve layout area



Problem [13.3]

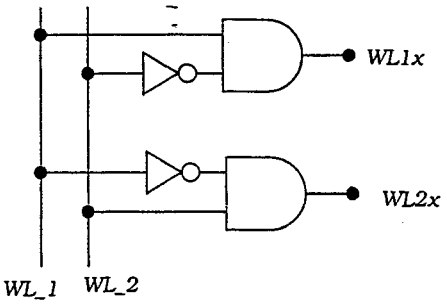
[13.4] This is an open-ended problem. The difference between the two designs is that a single gate drives a very large load capacitor and will have to be driven by a scaled chain to be fast, while a DWL architecture splits up the load into several gate/load groups and can be scaled accordingly. With a scaled design where $\beta_1 < \beta_2 < \beta_3 <$ etc. and the delays



Problem [13.4]

(including all contributions due to the sub-lines) are equalized, then the equations of Logical Effort provide the design criteria.

[13.5] A simple solution is to change the wordline signals applied to the access transistors to mutually exclusive control bits of *WL1x* and *WL2x* that are generated by basic AND logic.



Problem [13.5]

[13.6] (a) The maximum charge that can be stored on the capacitor is

$$Q_{max} = C_s V_{max} = (55\times10^{-15})(3.5) = 1.925\times10^{-13} \text{ C}$$

so the number of charges is

$$N = \frac{Q_{max}}{q} = \frac{1.925\times10^{-13}}{1.602\times10^{-19}} = 1.20\times10^{6}$$

since one electron has a charge of q.
(b) The leakage current is 75 nA. This means

$$I = 75\times10^{-9} = \frac{\Delta Q}{\Delta t} \text{ [C/s]}$$

so the rate of electrons leaking in 1 second is

$$r_N = \frac{75\times10^{-9}}{1.602\times10^{-19}} = 4.68\times10^{11} \text{ [electrons/second]}$$

(c) The time required for the # of stored charges to be reduced to 100 is approximately

$$\Delta t = \frac{\Delta N}{r_N} = \frac{1.20\times10^{6} - 100}{4.68\times10^{11}} = 2.57\mu\text{s}$$

[13.7] (a) The maximum stored charge is

$$Q_{max} = C_s V_{max} = (45\times10^{-15})(3.3 - 0.55) = 1.24\times10^{-13} \text{ C}$$

(b) The minimum final voltage after leakage and charge sharing is given as

$$V_f = 1.5 = \left(\frac{C_s}{C_s + C_{bit}}\right)V_s(t_h) = \left(\frac{45}{295}\right)V_s(t_h)$$

so the minimum stored voltage is

$$V_s(t_h) = \left(\frac{295}{45}\right)(1.5) = 9.83\text{V}$$

In other words, the V_f value is too high (the cell will not work)! This problem was included to show how difficult it is to actually store a voltage in a DRAM cell. It usually amazes the newcome how much charge sharing drops the voltage.

Suppose instead that we drop the requirement to a more reasonable value of say V_f = 0.2 V. In this case, we would have

$$V_s(t_h) = \left(\frac{295}{45}\right)(0.2) = 1.31\text{V}$$

which is possible. Using this value, we estimate the hold time using

$$t_h = \frac{C_s}{I_L}(\Delta V) = \frac{45\times10^{-15}}{75\times10^{-9}}(1.44) = 0.864\mu\text{s}$$

[13.8] The initial voltage at time $t = 0$ is $V_{max} = V_{DD} - V_{Th} = 3\text{-}0.65 = 2.35$ V. The change in the stored voltage for a given time increment Δt is

$$\Delta V_s = \frac{I_L}{C_s}(\Delta t) = -\frac{250\times10^{-12}}{55\times10^{-15}}(\Delta t) = 4545.45(\Delta t)$$

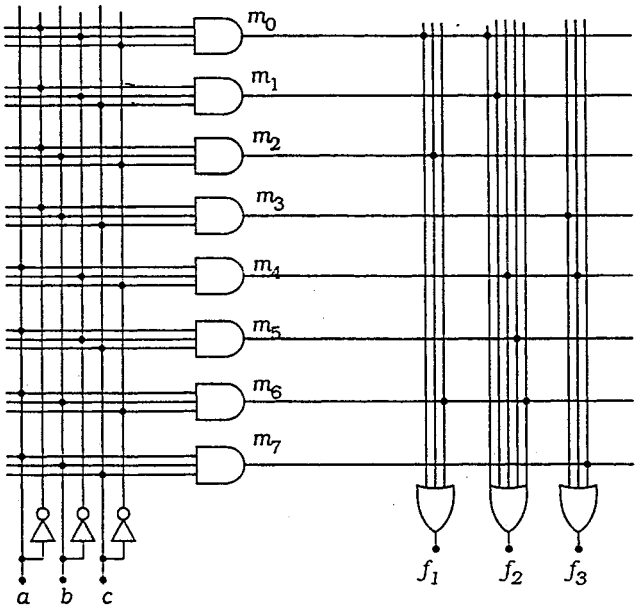
so the capacitor loses all of its stored charge after a time

$$\Delta t = \frac{2.35}{4545.45} = 0.517 \text{ ms}$$

Thus, with this high leakage current, there will be no voltage on the cell at time t = 10 ms. $V_s = V_f = 0$ V.

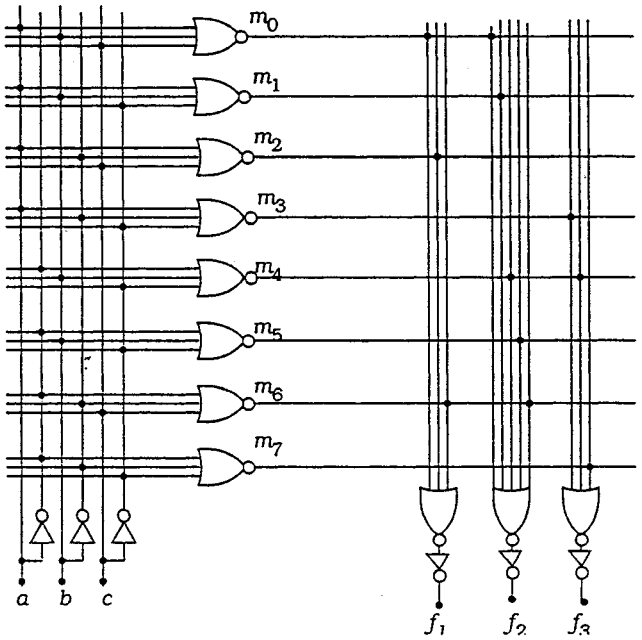
Note that even if the leakage is reduced to 0.25 pA, the charge only lasts for 517 ms. The instructor may want to have the students plot retention time for various leakage currents. This usually builds an appreciation for the problem faced by DRAM designers.

[13.9] The logic diagram is shown below.



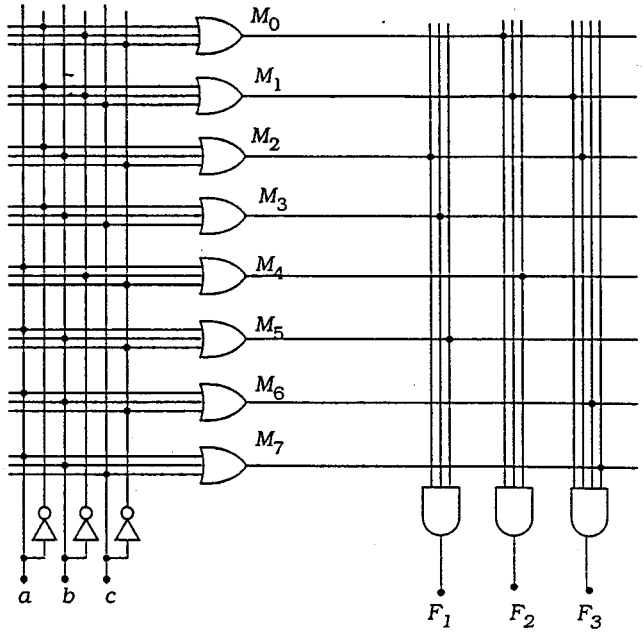
Problem [13.9] Logic

This can be translated into a CMOS NOR-NOR-NOT in a straightforward manner. The logic diagram shown illustrates the structure.



Problem [13.9] NOR-NOR

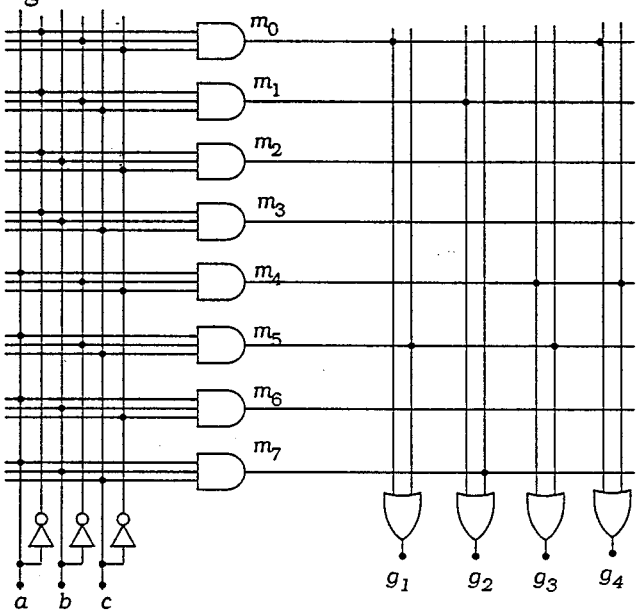
[13.10] The OR-AND array is shown below.



Problem [13.10]

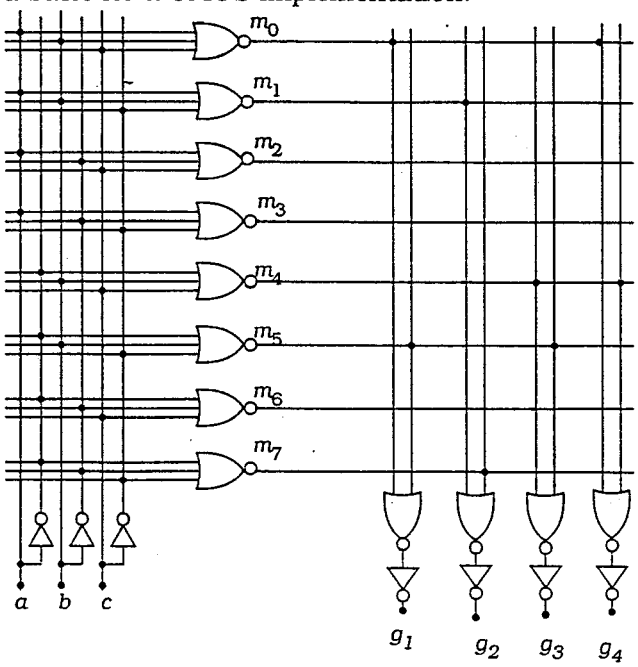
To implement this in a pseudo-nMOS basis (where NOR gates are easier), a straightforward approach is to use NOR-NOR cascades. The second NOR can be reduced to an an AND gate with assert-low inputs (via DeMorgan); the assert low inputs are restored by the input NOR gates to produce the same OR-AND sequence.

[13.11] The basic AND-OR design is shown.



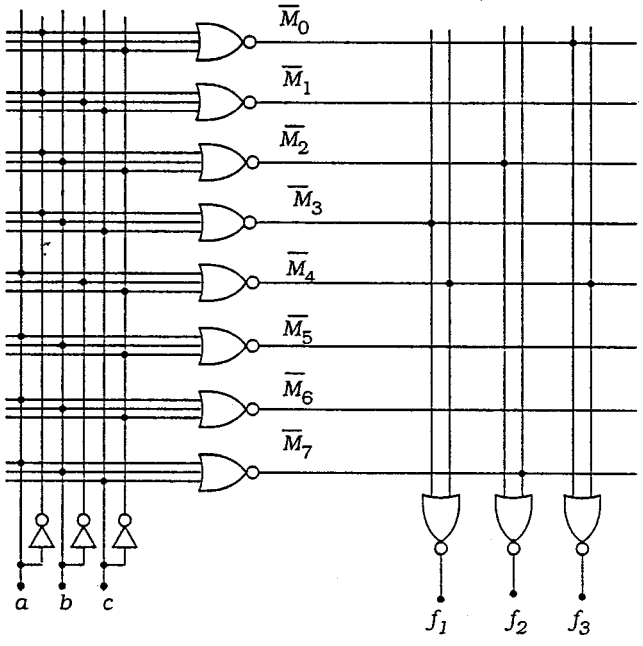
Problem [13.11] Logic

The NOR-based logic provides a basis for a CMOS implementation.



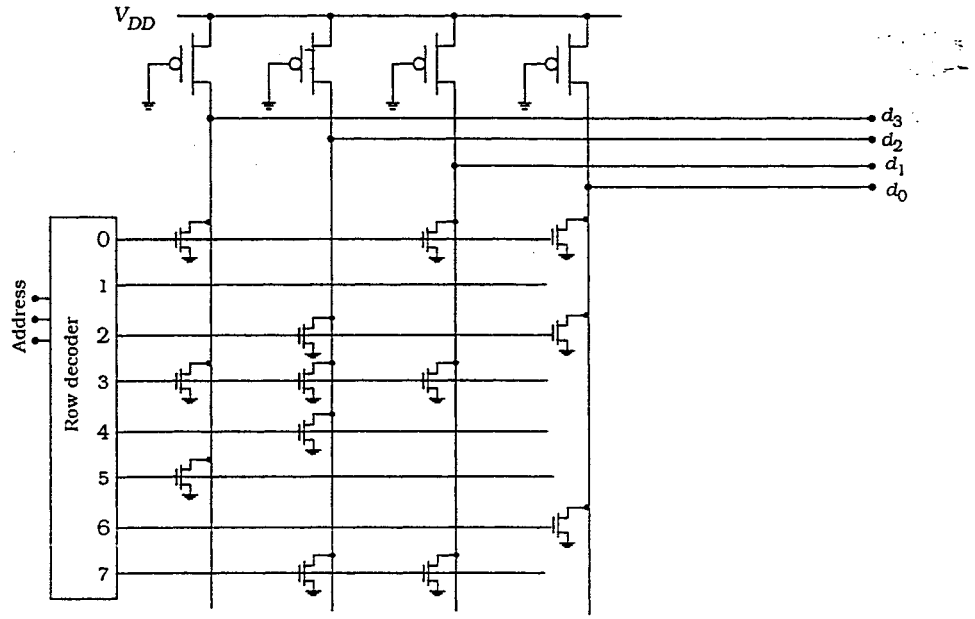
Problem [13.11]
NOR Logic

[13.12] The NOR-NOR implementation of the OR-AND PLA is shown in the logic diagram below. This can be translated to a CMOS network (using dynamic NOR gates) in a straightforward manner.



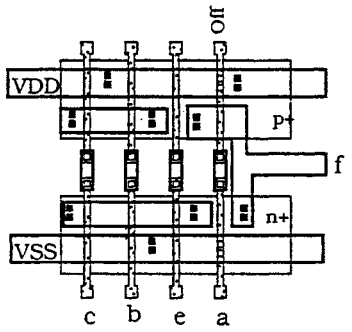
Problem [13.12]

[13.13] The circuit diagram is constructed by using the FET locations as shown below.



Problem [13-13]

[13.14] The wiring is shown below. This follows the layout strategies introduced in Part 1 of the book.



Chapter 14

[14.1] (a) The parallel-plate formula gives

$$c = \frac{\varepsilon_{ox} w}{T_{ox}} = \frac{(3.9)(8.854\times10^{-14})(0.5\times10^{-4})}{1.1\times10^{-4}} = 1.57\times10^{-13} \text{ F/cm}$$

or we can change units to

$$c = 0.157 \text{ pF/cm}$$

(b) With fringing effects,

$$c = \varepsilon_{ox}\left[1.15\left(\frac{w}{T_{ox}}\right) + 2.8\left(\frac{t}{T_{ox}}\right)^{0.222}\right]$$

$$= (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.5}{1.1}\right) + 2.8\left(\frac{0.9}{1.1}\right)^{0.222}\right]$$

$$= 1.105\times10^{-12} \text{ F/cm} = 1.105 \text{ pF/cm}$$

(c) The error incurred by neglecting fringing is

$$\% \text{ Error} = \left(\frac{1.105 - 0.157}{1.105}\right)\times 100 = 85.79\ \%$$

This large error arises from the condition $t > w$, so the fringing fields are a major contribution. It also illustrates the point that fringing capacitance is a major contribution in fine-line VLSI.

(d) For the line capacitance we have

$$C_{line} = cl = (1.105\times10^{-12})(100\times10^{-4}) = 11.05 \text{ fF}$$

The line resistance is computed as

$$R_{line} = R_s n = (0.08)\left(\frac{100}{0.5}\right) = 16\Omega$$

where the number of squares is $n = (l/w)$.

[14.2] (a) The capacitance per cm is

$$c = \varepsilon_{ox}\left[1.15\left(\frac{w}{T_{ox}}\right) + 2.8\left(\frac{t}{T_{ox}}\right)^{0.222}\right]$$

$$= (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.35}{0.9}\right) + 2.8\left(\frac{1.1}{0.9}\right)^{0.222}\right]$$

$$= 1.165\times10^{-12} \text{ F/cm}$$

(b) The line values are

$$C_{line} = cl = (1.165\times10^{-12})(48\times10^{-4}) = 5.592 \text{ fF}$$

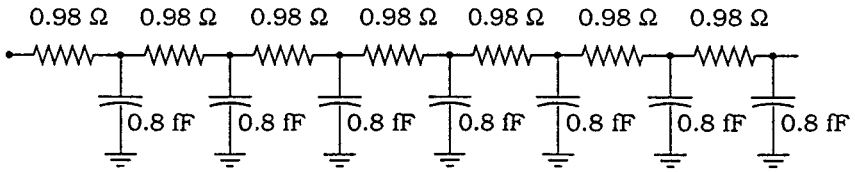
and

$$R_{line} = R_s n = (0.05)\left(\frac{48}{0.35}\right) = 6.86\Omega$$

(c) With $m = 7$, the individual rung elements have values of

$$R_7 = \frac{R_{line}}{7} = 0.98\Omega \qquad C_7 = \frac{C_{line}}{7} = 0.80\text{fF}$$

which gives the ladder shown.



Problem 14.2

The time constant is

$$\tau_m = \frac{m(m+1)}{2} R_m C_m = \frac{7(8)}{2}(0.98)(0.8\times10^{-15}) = 0.022 \text{ ps}$$

Using the simpler equation gives a larger estimate of

$$\tau = R_{line} C_{line} = (6.86)(5.592\times10^{-15}) = 0.038 \text{ ps}$$

[14.3] With CMP, the thickness of a metal line is equal to the oxide thickness next to it. This allows us to find the oxide thickness for each layer.

The answers to this problem vary with the line width w, which was omitted to allow different values to be selected. In the solutions, we will take $w = 0.35$ μm for every layer, but the instructor may wish to change the value(s) to describe a different process.

For M1, $T_{ox} = 1.1$ μm and

$$c = \varepsilon_{ox}\left[1.15\left(\frac{w}{T_{ox}}\right) + 2.8\left(\frac{t}{T_{ox}}\right)^{0.222}\right]$$

$$= (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.35}{1.1}\right) + 2.8\left(\frac{0.58}{1.1}\right)^{0.222}\right]$$

$$= 0.965 \text{ pF/cm}$$

For M2, $T_{ox} = 1.1 + .58 + 1.2 = 2.88$ μm and

$$c = (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.35}{2.88}\right) + 2.8\left(\frac{0.68}{1.88}\right)^{0.222}\right]$$

$$= 0.820 \text{ pF/cm}$$

For M3, T_{ox} = 2.88+.68+1.2 = 4.76 μm and

$$c = (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.35}{4.76}\right)+2.8\left(\frac{0.68}{4.76}\right)^{0.222}\right]$$

$$= 0.657 \text{ pF/cm}$$

For M4, T_{ox} = 4.76+ .68 + .90 = 6.34 μm and

$$c = (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.35}{6.34}\right)+2.8\left(\frac{0.68}{6.34}\right)^{0.222}\right]$$

$$= 0.611 \text{ pF/cm}$$

This shows the decrease in capacitance per unit length as metal interconnect lines are added.

[14.4] The overlap capacitance per unit area is estimated using

$$C_{ov} = \frac{\varepsilon_{ox}}{T_{ox}} \text{ F/cm}^2$$

where the oxide thickness is determined by the metal-metal oxide. For M1-M2,

$$C_{ov} = \frac{(3.9)(8.854\times10^{-14})}{(1.2\times10^{-4})} = 2.88 \text{ nF/cm}^2 = 0.0288 \text{ fF/}\mu\text{m}^2$$

For M11-M3,

$$C_{ov} = \frac{(3.9)(8.854\times10^{-14})}{(3.08\times10^{-4})} = 1.12 \text{ nF/cm}^2 = 0.0112 \text{ fF/}\mu\text{m}^2$$

[14.5] (a) The line capacitance per unit length is (10,000 Å = 1 micron)

$$c = (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.35}{1}\right)+2.8\left(\frac{0.85}{1}\right)^{0.222}\right]$$

$$= 1.072 \text{ pF/cm}$$

so

$$C_{line} = cl = (1.072\times10^{-12})(122\times10^{-4}) = 13.08 \text{ fF}$$

The line resistance is

$$R_{line} = (0.008)\left(\frac{122}{0.35}\right) = 2.79\Omega$$

(b) For m = 2,

$$R_2 = \frac{R_{line}}{2} = 1.4\Omega \qquad C_2 = \frac{C_{line}}{2} = 6.54\text{fF}$$

which gives a time constant of

$$\tau_m = \frac{m(m+1)}{2} R_m C_m = \frac{2(3)}{2}(1.4)(6.54\times10^{-15}) = 0.028 \text{ ps}$$

For $m = 6$,

$$R_6 = \frac{R_{line}}{6} = 0.465\Omega \qquad C_6 = \frac{C_{line}}{6} = 1.09\text{fF}$$

so that

$$\tau_m = \frac{m(m+1)}{2} R_m C_m = \frac{6(7)}{2}(0.465)(1.09\times10^{-15}) = 0.011 \text{ ps}$$

Since the delay has differential origins, this is more accurate than the m=2 case.

[14.6] (a) The line resistance per unit length is

$$r = \frac{R_s}{w} = \frac{0.008}{0.35} = 228.57 \ \Omega/\text{cm}$$

while the capacitance per unit length is

$$c = (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.35}{1.2}\right) + 2.8\left(\frac{0.95}{1.2}\right)^{0.222}\right]$$

$$= 1.034 \text{ pF/cm}$$

(b) We write

$$\xi = 0.05 = \sqrt{\frac{(228.57)(1.035\times10^{-12})}{4t}}\ z$$

so squaring gives

$$t = 2.37\times10^{-8} z^2$$

(c) With lengths of 100, 200, and 300 microns, we have

$$t_{100} = 2.37\times10^{-8}(100\times10^{-4})^2 = 2.37 \text{ ps}$$

$$t_{200} = 2.37\times10^{-8}(200\times10^{-4})^2 = 9.46 \text{ ps}$$

$$t_{300} = 2.37\times10^{-8}(300\times10^{-4})^2 = 21.29 \text{ ps}$$

[14.7] (a) The coupling capacitance per unit length is

$$c_c = \varepsilon_{ox}\left[0.03\left(\frac{w}{T_{ox}}\right) + 0.83\left(\frac{t}{T_{ox}}\right) - 0.07\left(\frac{t}{T_{ox}}\right)^{0.222}\right]\left(\frac{S}{T_{ox}}\right)^{-1.34}$$

$$= \varepsilon_{ox}\left[0.03\left(\frac{0.35}{1.1}\right) + 0.83\left(\frac{1}{1.1}\right) - 0.07\left(\frac{1}{1.1}\right)^{0.222}\right]\left(\frac{0.5}{1.1}\right)^{-1.34}$$

$$= 6.91\times10^{-13} \text{ F/cm}^2$$

(b) For 20 μm, the coupling capacitance is

$$C_c = 6.91\times10^{-13}(20\times10^{-4}) = 1.38 \text{ fF}$$

For 30 μm, the coupling capacitance increases to

$$C_c = 6.91\times10^{-13}(30\times10^{-4}) = 2.07 \text{ fF}$$

[14.8] (a) The line capacitance per unit length is

$$c = (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.25}{1.2}\right)+2.8\left(\frac{0.85}{1.2}\right)^{0.222}\right]$$

$$= 0.978 \text{ pF/cm}$$

(b) The coupling capacitance per unit length is

$$c_c = \varepsilon_{ox}\left[0.03\left(\frac{w}{T_{ox}}\right)+0.83\left(\frac{t}{T_{ox}}\right)-0.07\left(\frac{t}{T_{ox}}\right)^{0.222}\right]\left(\frac{S}{T_{ox}}\right)^{-1.34}$$

$$= \varepsilon_{ox}\left[0.03\left(\frac{0.25}{1.2}\right)+0.83\left(\frac{0.85}{1.2}\right)-0.07\left(\frac{0.85}{1.2}\right)^{0.222}\right]\left(\frac{0.4}{1.2}\right)^{-1.34}$$

$$= 7.967\times10^{-13} \text{ F/cm}^2$$

(c) The capacitance per unit length is $c + 2c_c$ so that the total capacitance seen into a line

$$C_{in} = (0.978+0.797)\times10^{-12}(18\times10^{-4}) = 3.194 \text{ fF}$$

[14.9] (a) The line capacitance per unit length is

$$c = (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.4}{1}\right)+2.8\left(\frac{0.84}{1}\right)^{0.222}\right]$$

$$= 1.089 \text{ pF/cm}$$

so that the line capacitance is

$$C_{line} = 1.089\times10^{-12}(50\times10^{-4}) = 5.45 \text{ fF}$$

The line resistance is

$$R_{line} = 0.005\left(\frac{50}{0.4}\right) = 0.625\Omega$$

(b) With $s = 1.5$, the new width and length are $w = 0.267$ μm and $l = 33.33$ μm while the other parameters are left the same. We thus recalulate the values as

$$c = (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.267}{1}\right)+2.8\left(\frac{0.84}{1}\right)^{0.222}\right]$$

$$= 1.036 \text{ pF/cm}$$

so that the line capacitance is

$$C_{line} = 1.036\times10^{-12}(33.33\times10^{-4}) = 3.45 \text{ fF}$$

The line resistance is invariant:

$$R_{line} = 0.005\left(\frac{33.33}{0.267}\right) = 0.625\Omega$$

[14.10] (a) $v(z,t)=V_{DD}\,\text{erfc}(0.9) \approx (0.2031)\,V_{DD}$.

(b) We have

$$c = (3.9)(8.854\times10^{-14})\left[1.15\left(\frac{0.5}{0.9}\right)+2.8\left(\frac{0.9}{0.9}\right)^{0.222}\right]$$

$$= 0.566 \text{ pF/cm}$$

and

$$r = \frac{0.04}{0.5\times10^{-5}} = 800\Omega/\text{cm}$$

$$\xi = 0.9 = \sqrt{\frac{(800)(0.566\times10^{-12})}{4t}}\ z$$

or

$$t = 1.4\times10^{-10}z^2 \text{ sec} = Bz^2$$

where z is in cm. This case must be used with care, as the large value of $\xi = 0.9$ indicates a very small voltage.

[14.11] The forward trigger voltage is

$$V^+ = \frac{3.3+\sqrt{6}(0.7)}{1+\sqrt{6}} = 1.45 \text{ V}$$

and the reverse trigger voltage is

$$V^- = \frac{\sqrt{4}(3.3-0.8)}{1+\sqrt{4}} = 1.67 \text{ V}$$

[14.12] For V^+ we rewrite the equation as

$$\sqrt{\frac{\beta_1}{\beta_3}} = \frac{V_{DD} - V^+}{V^+ - V_{Tn}}$$

so for V^+ =3.9 V we need a device ratio of

$$\frac{\beta_1}{\beta_3} = \left(\frac{5-3.9}{3.9-0.7}\right)^2 = 0.344$$

For the reverse-trigger voltage we have

$$\sqrt{\frac{\beta_4}{\beta_6}} = \frac{V^-}{V_{DD} - |V_{TP}| - V^-}$$

so we have

$$\frac{\beta_4}{\beta_6} = \left(\frac{1.2}{5-0.8-1.2}\right)^2 = 0.16$$

Chapter 15

There are no problems in Chapter 15

Chapter 16

There are no problems in Chapter 16