North South University

CSE231L

Experiment # 6

Name of Experiment: **Introduction to Multiplexers and Decoders**

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Section: 13

Group: 3

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Objectives

- We have to understand the concept of multiplexing in the context of digital logic circuits.
- We have to learn about the internal logic of digital multiplexers.
- We have to implement digital logic functions using multiplexers.
- We have to observe and analyze the operations of the 3 to 8 Line Decoder.

Equipments

- Trainer board.
- IC 7404 Hex Inverter (NOT gate)
- IC 4073 3-input AND gates.
- IC 7432 2-input OR gates.
- IC 74151 (8:1 Multiplexer).
- IC 74138 (3:8 Line Decoder).

Theory

Multiplexers have the most important attibutions of digital circuitry in communication hardware. These digital switches enable us to achieve the communication network we have today. In this experiment, we will have to construct MUX (multiplexers) with simple logic gates.

Multiplexer: A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

Decoders: A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n output lines. One input line (that is normally tied low) is routed to one of eight output lines. The output is selected by three select lines: S2, S1 and S0. Unselected output lines are normally high, so the selected output goes low when the input line is tied low. Both the multiplexer and the decoder can be used to synthesize combinational logic circuits.

In this laboratory experiment, we will realize a three input variable truth table design, first using conventional AND-OR or NAND-NAND logic. Then you will use a 74LS151 multiplexer, and finally a 74LS138 decoder and several AND gates.

Circuit Diagram

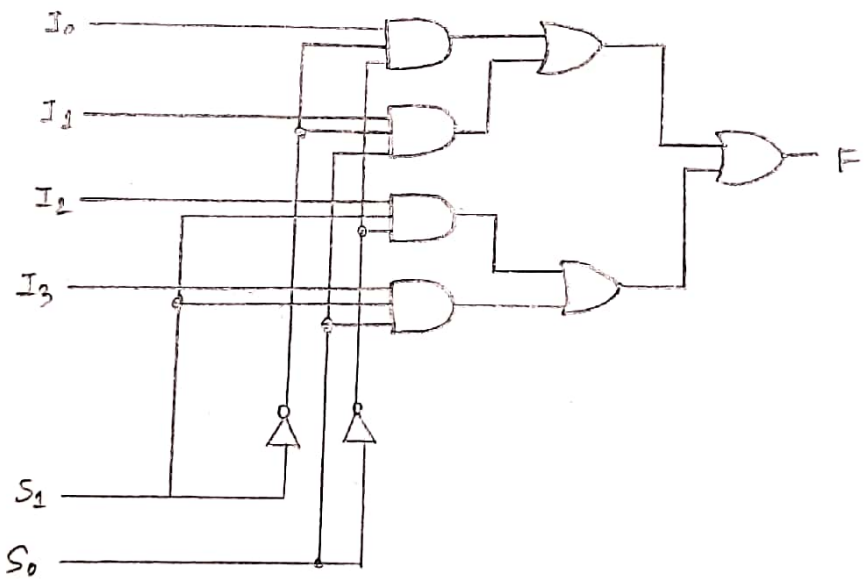


Figure D.1.1: 4:1 Multiplexer.

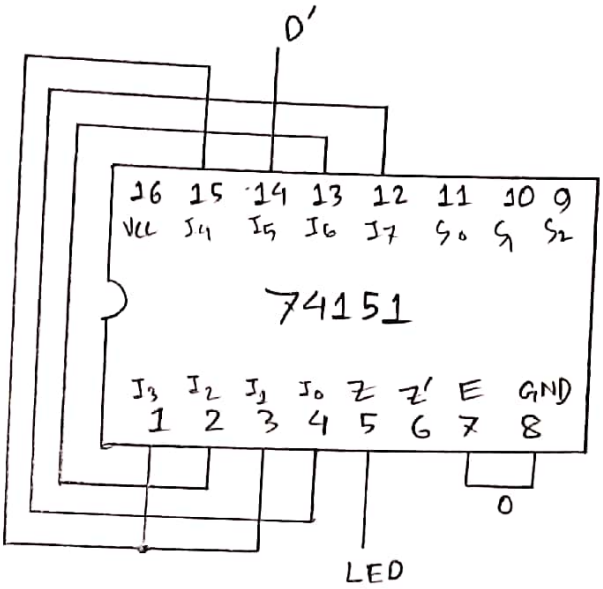


Figure F.2.1

Results

A	B	C	F(Theoretical)	Data Inputs	F(Practical)
0	0	0	1	$I_0 = \bar{C}$	1
0	0	1	0		0
0	1	0	1	$I_1 = 1$	1
0	1	1	1		1
1	0	0	0	$I_2 = 0$	0
1	0	1	0		0
1	1	0	1	$I_3 = \bar{C}$	1
1	1	1	0		0

Table F.1.1

Implementing a Boolean function using a 4:1 MUX

F.2 Experimental Data (Implementing a Boolean function using an 8:1 MUX IC):

A	B	C	D	F(Theoretical)	Data Inputs	F (Practical)
0	0	0	0	1	$I_0 = 1$	1
0	0	0	1	1		1
0	0	1	0	0	$I_1 = D$	0
0	0	1	1	1		1
0	1	0	0	0	$I_2 = 0$	0
0	1	0	1	0		0
0	1	1	0	0	$I_3 = D$	0
0	1	1	1	1		1
1	0	0	0	0	$I_4 = D$	0
1	0	0	1	1		1
1	0	1	0	1	$I_5 = D'$	1
1	0	1	1	0		0
1	1	0	0	0	$I_6 = 0$	0
1	1	0	1	0		0
1	1	1	0	1	$I_7 = 1$	1
1	1	1	1	1		1

Table F.2.1

F.3 Experimental Data (3 to 8 Line Decoder):

Enable Inputs		Select Inputs			Outputs							
G_1	G_2	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Table F.3.1

Questions

1.

If an active-LOW output (74138, one of the output will low and the rest will be high) is required for each ~~del~~ decoded number, the entire decoder can be implemented with

1. NAND gates.
2. Inverters.

If an active-HIGH output (74139, one of the output will

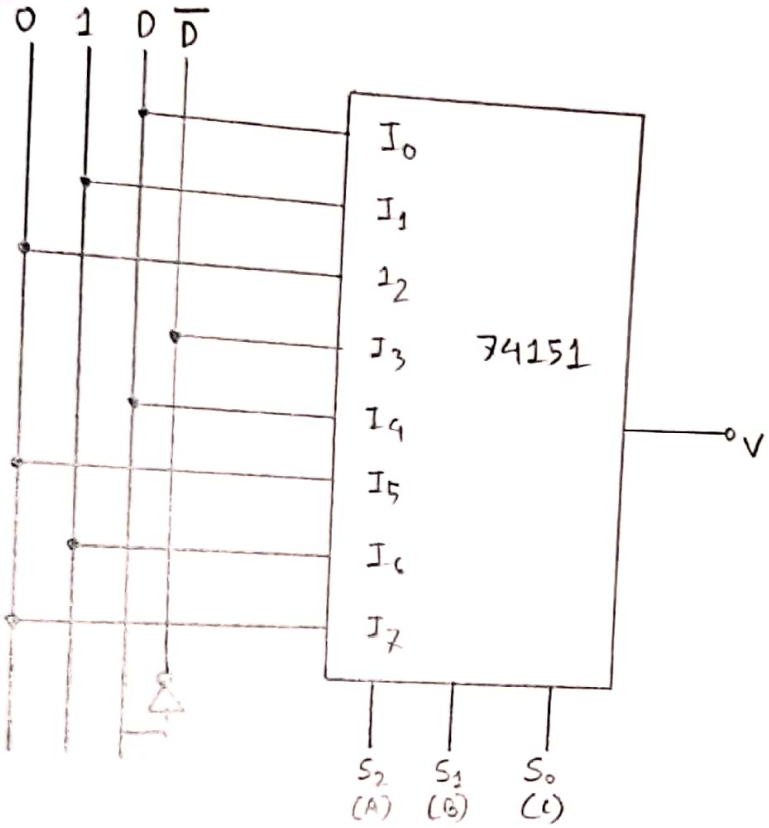
high and the rest will be low) is required for each decoded number, the entire decoder can be implemented with

1. AND gates
2. Inverters.

3|

$F(A,B,C,D) = \Sigma(1,2,3,6,9,12,13)$

A	B	C	D	F	Data Inputs
0	0	0	0	0	$I_0 = D$
0	0	0	1	1	
0	0	1	0	1	$I_1 = 1$
0	0	1	1	1	
0	1	0	0	0	$I_2 = 0$
0	1	0	1	0	
0	1	1	0	1	$I_3 = \bar{D}$
0	1	1	1	0	
1	0	0	0	0	$I_4 = D$
1	0	0	1	1	
1	0	1	0	0	$I_5 = 0$
1	0	1	1	0	
1	1	0	0	1	$I_6 = 1$
1	1	0	1	1	
1	1	1	0	0	$I_7 = 0$
1	1	1	1	0	



Discussion

Because of human error and equipment error, we didn't get our expected results. In this experiment, we got to know about Multiplexers and 3 to 8 line decoder and how they work. First we implemented the Multiplexer using IC 7407, IC 7422 and IC 7432. It was little tough for us. This hard work made easy by our lab instructor. She helped us to implement this.

We finished our experiment by implementing 3 to 8 line decoder using AND and NAND gates to different results. We drew circuit diagram, implemented it and matched the outputs with the table. This part of the experiment went smoothly without any errors.

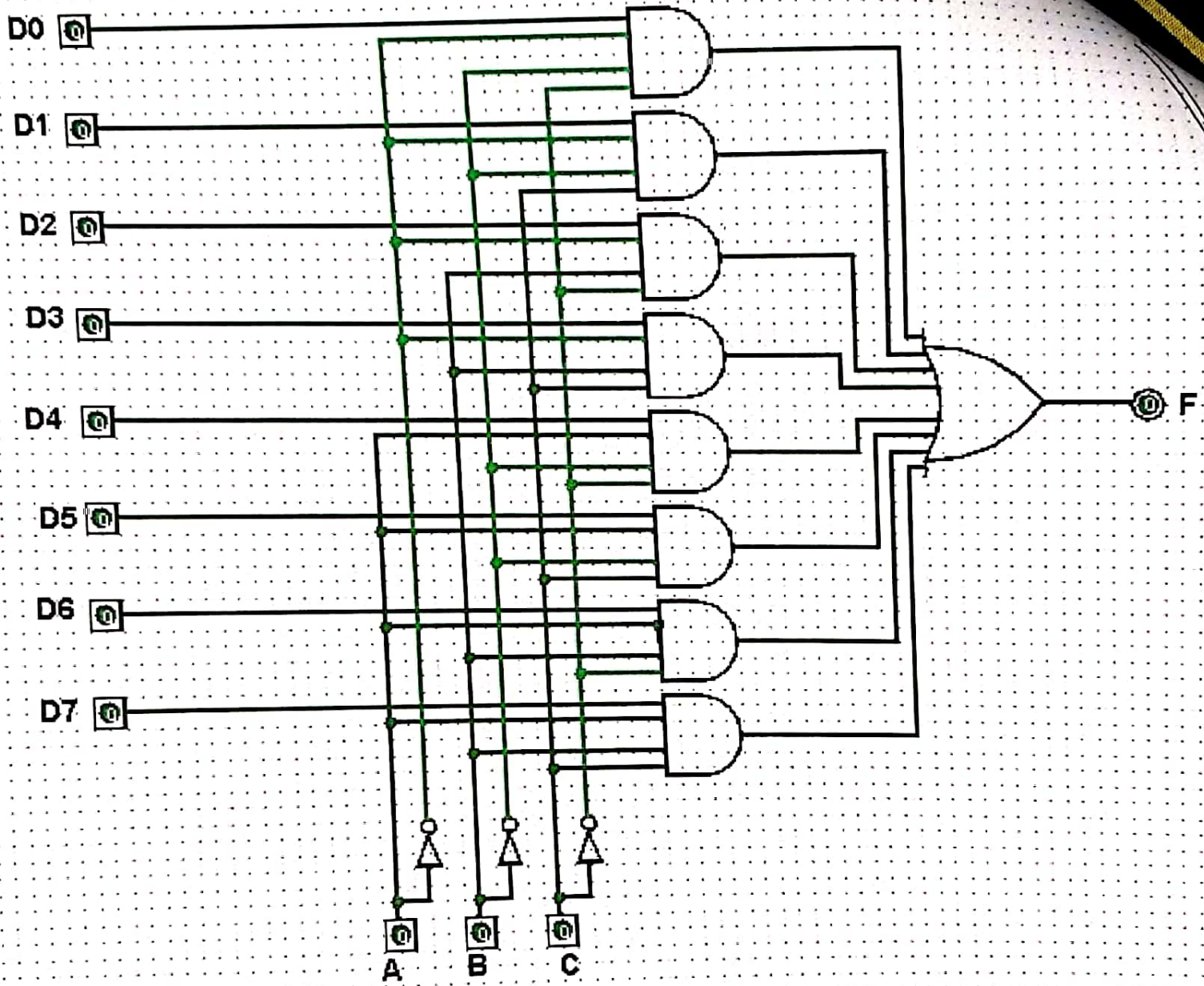


Figure: 8 : 1 Multiplexer

CSE231L/EEE211L – Lab 6 – Multiplexers and Decoders

Instructor's Signature: .....

Data Sheet: Section:	Group No.:	Date:

F.1 Experimental Data (Implementing a Boolean function using a 4:1 MUX):

A	B	C	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	1	$I_0 = \bar{C}$	1
0	0	1	0		0
0	1	0	1	$I_1 = 1$	1
0	1	1	1		1
1	0	0	0	$I_2 = 0$	0
1	0	1	0		0
1	1	0	1	$I_3 = \bar{C}$	1
1	1	1	0		0

Table F.1.1

F.2 Experimental Data (Implementing a Boolean function using an 8:1 MUX IC):

A	B	C	D	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0	1	$I_0 = 1$	1
0	0	0	1	1		1
0	0	1	0	0	$I_1 = D$	0
0	0	1	1	1		1
0	1	0	0	0	$I_2 = 0$	0
0	1	0	1	0		0
0	1	1	0	0	$I_3 = D$	0
0	1	1	1	1		1
1	0	0	0	0	$I_4 = D$	0
1	0	0	1	1		1
1	0	1	0	1	$I_5 = D'$	1
1	0	1	1	0		0
1	1	0	0	0	$I_6 = 0$	0
1	1	0	1	0		0
1	1	1	0	1	$I_7 = 1$	1
1	1	1	1	1		1

Table F.2.1

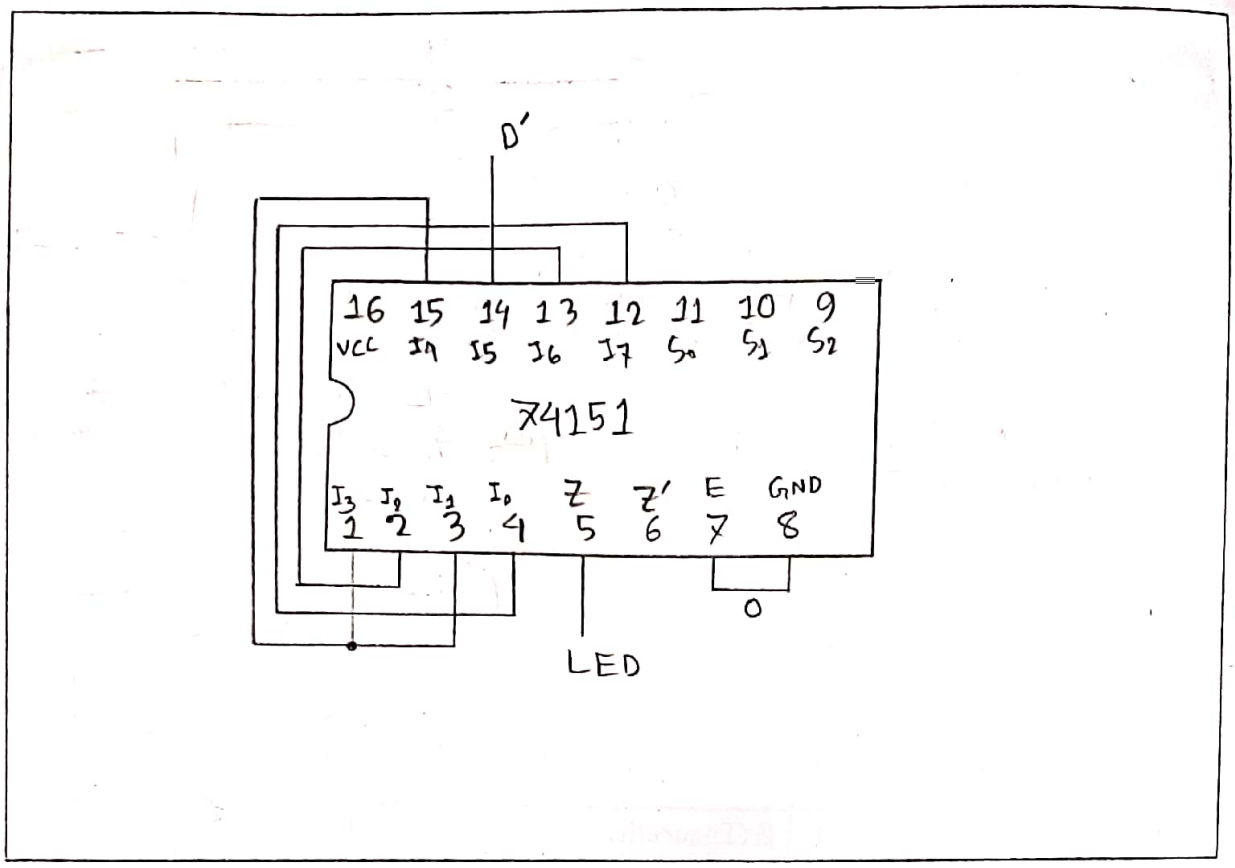


Figure F.2.1

F.3 Experimental Data (3 to 8 Line Decoder):

Enable Inputs		Select Inputs			Outputs							
G1	G2	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Table F.3.1

Correct.

13.11.19