NORTH SOUTH UNIVERSITY
Department of ECE
CSE 231: Digital Logic Design

Lab 7: Introduction to Multiplexer & Decoder.

Objectives

- Familiarize with the analysis of Multiplexer & Decoder circuits.
- Learn the implementation of Multiplexer & Decoder using gates.
- Verify the Multiplexer & Decoder with the Truth table.

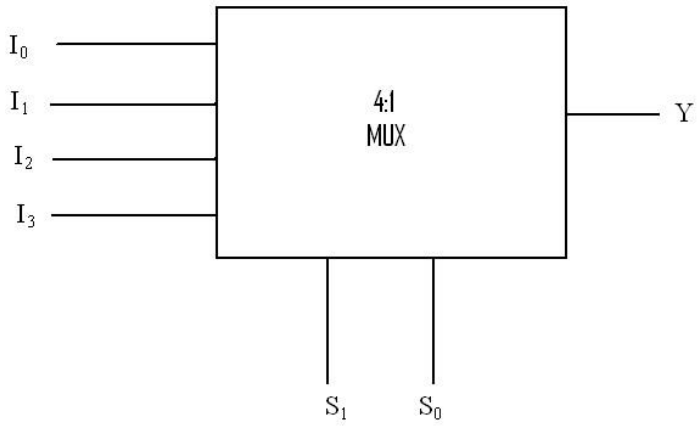
Apparatus

- Trainer Board
- IC 7404, 7432
- IC 74151, 74138
- Wires for connection

Theory

Multiplexers have the most important attributions of digital circuitry in communication hardware. These digital switches enable us to achieve the communication network we have today. In this experiment the students will have to construct MUX (multiplexers) with simple logic gates.

JOB 1: 4 to 1 MUX



Truth Table

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y= I_0S_1'S_0' + I_1S_1'S_2 + I_2S_1S_2' + I_3S_1S_2$$

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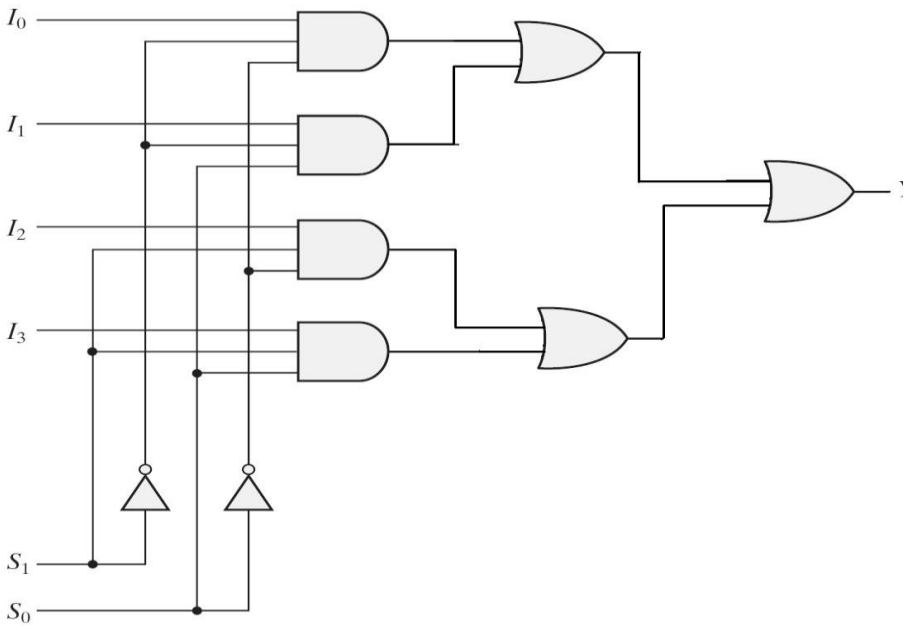
Circuit diagram:

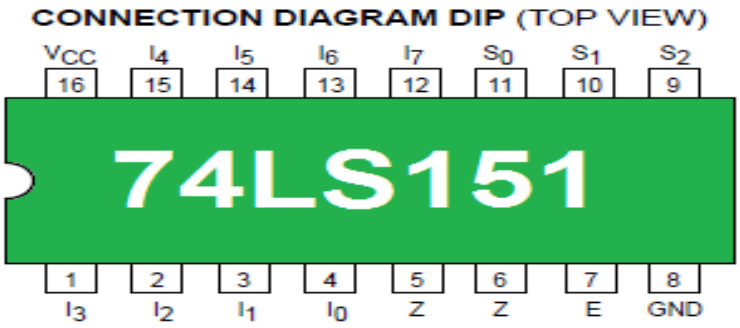


Implement the function using 4:1 MUX; F (A, B, C) = ∑ (0, 1, 5, 7) [take A as input]

Procedure:

1) Write the truth table for 4:1 MUX.
2) Write the Boolean function for the output logic.
3) Draw the logic diagram to implement the Boolean function.
4) Select the required ICs.
5) Observe and note the output logic for all combination of inputs.

JOB 2: 8 to 1 MUX



Implement the function using 8:1 MUX (IC 74151); F (A, B, C, D) = ∑ (0, 1, 3, 5, 8, 9, 14, 15) [take A as input]

Procedure:

1) Write the truth table for 8:1 MUX.
2) Write the Boolean function for the output logic.
3) Draw the logic diagram to implement the Boolean function.
4) Select the required ICs.
5) Observe and note the output logic for all combination of inputs.

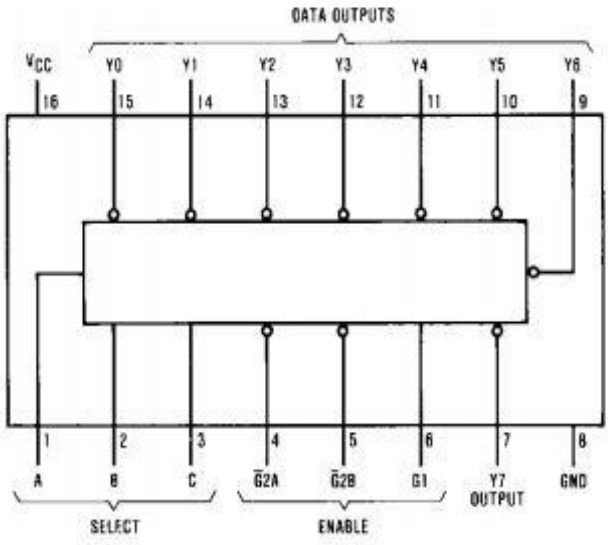
JOB 3: 3 to 8 line Decoder:

It uses all AND gates, and therefore, the outputs are active- high. **For active- low outputs, NAND gates are used.** It has 3 input lines and 8 output lines. It is also called as binary to octal decoder it takes a 3-bit binary input code and activates one of the 8(octal) outputs corresponding to that code. The truth table is as follows:

Procedure:

1. Implement a 3 to 8 line decoder by using IC 74138.
2. Verify the decoder circuit with the truth table.

Connection Diagram



Function Table

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$ (Note 1)	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1: $\overline{G2} = \overline{G2A} + \overline{G2B}$

Assignment

- Draw the logic diagram and truth table for 8:1 MUX;
  F (A, B, C, D) = Σ (0, 1, 3, 5, 8, 9, 14, 15) [take B as input]

Simulation

- Simulate the 8 to 1 MUX and 3 to 8 Decoder circuit using Logisim.