

Cairo University Computer Engineering Department

Faculty of Engineering Third year

**VLSI project**

**Home Automation System**

**Team#12 Members**

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| --- | --- | --- |
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**Design 1**

**System Schematic:**

Diagram

Description automatically generated

**Description:**

Every 6 clock cycles, the priority is completely reversed through the **reversed\_priority** signal from the counter. The counter starts from 0 to 5 and then goes back to 0, it is increased by 1 in all cycles except if there is no active input, in that case the counter remains as it is for this cycle. The priority encoder outputs a code which represent the state of the system (which is the display output mentioned in the document). The register preserves the state so that any state should take at least 1 cycle. The output decoder maps the system state to the output signals.

Score = 0.5 \* Movable Cell Area in squm + 0.3 \* (clock period in ps – worst slack in ps) + 0.2 \* total power in uw =

Timeline

Description automatically generated **Pre-Synthesis Simulation:**

**A picture containing graphical user interface

Description automatically generatedPost-Synthesis Simulation:**

**Graphical user interface

Description automatically generated with medium confidencePost-Layout Simulation:**

**Design 2**

**Algorithm:**

Initially, the priority is normal (front door, rear door, fire alarm, window, temperature). Then in every cycle, the action with the highest priority in the previous cycle becomes the action with the least priority in the current cycle.

Example:

Cycle 1: front door, rear door, fire alarm, window, temperature

Cycle 2: rear door, fire alarm, window, temperature, front door

Cycle 3: fire alarm, window, temperature, front door, rear door

and so on.

**System Schematic:**Diagram

Description automatically generated

**Description:**

Every clock cycle, the priority encoder determines the state of the system according to the counter\_value signal from the counter according to the previously discussed algorithm. The counter starts from 0 to 4 and then goes back to 0, it is increased by 1 in all cycles except if there is no active input, in that case the counter remains as it is for this cycle. The priority encoder outputs a code which represent the state of the system (which is the display output mentioned in the document). The register preserves the state so that any state should take at least 1 cycle. The output decoder maps the system state to the output signals.