

Cairo University Computer Engineering Department

Faculty of Engineering Third year

**VLSI**

**Home Automation System**

**Team#12 Members**

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| --- | --- | --- |
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Design 1

Diagram

Description automatically generated

Description:

Every 6 clock cycles, the priority is completely reversed through the reversed\_priority signal from the counter. The counter is increased by 1 in all cycles except if there is no active input, in that case the counter remains as it is for this cycle. The priority encoder outputs a code which represent the state of the system (which is the display output mentioned in the document). The register preserves the state so that any state should take at least 1 cycle. The output decoder maps the system state to the output signals.

Score = 0.5 \* Movable Cell Area in squm + 0.3 \* (clock period in ps – worst slack in ps) + 0.2 \* total power in uw =

Design 2