

Cairo University Computer Engineering Department

Faculty of Engineering Third year

**VLSI project**

**Home Automation System**

**Team#12 Members**

|  |  |  |
| --- | --- | --- |
| **Name** | **Section** | **B.N.** |
| Ahmed Ihab Yousry | 1 | 2 |
| Osama Magdy Aied | 1 | 15 |
| Mostafa Mohamed Ahmed Elgendy | 2 | 27 |
| Mostafa Wael Kamal | 2 | 29 |

**January, 2022**

**We have chosen design 2, as it handles starvation in a better way using dynamic priority and a sort of state machine.**

**Regarding the optimization parameters, design 2 utilize more area on the chip as it uses a larger design for the priority encoder and regarding the power, design 2 consumes more power due to the excessive load on the priority encoder and the frequent change of the state. Furthermore, slack value is higher as the register to output delay limits it.**

**Design 1**

**System Schematic:**

Diagram

Description automatically generated

**Description:**

Every 6 clock cycles, the priority is completely reversed through the **reversed\_priority** signal from the counter. The counter starts from 0 to 5 and then goes back to 0, it is increased by 1 in all cycles except if there is no active input, in that case the counter remains as it is for this cycle. The priority encoder outputs a code which represent the state of the system (which is the display output mentioned in the document). The register preserves the state so that any state should take at least 1 cycle. The output decoder maps the system state to the output signals.

**Schematic of the design after synthesis:**

Diagram

Description automatically generated

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

Diagram

Description automatically generated

A picture containing chart

Description automatically generated

Diagram

Description automatically generated

Diagram

Description automatically generated

Note that the values of the temperature in the simulation are 49 and 73 not 8 and 32 because our design for the temperature register is that it ranges from 41F to 104F, so each value in the simulation must be added to 41 because it is our zero reference.

Timeline

Description automatically generated **Pre-Synthesis Simulation:**

**A picture containing graphical user interface

Description automatically generatedPost-Synthesis Simulation:**

**Graphical user interface

Description automatically generated with medium confidencePost-Layout Simulation:**

**Chip Schematic:**

**Power Grid:**

**A picture containing text

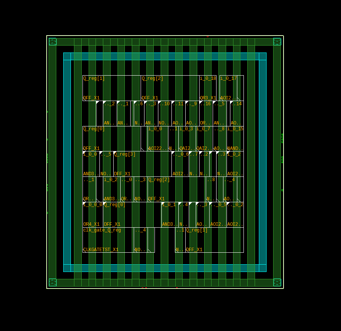
Description automatically generated**

**Routing:**

**A picture containing graphical user interface

Description automatically generated**

**Vdd Strips:**

****

**Vss Strips:**

**A picture containing graphical user interface

Description automatically generated**

**design.rpt file:**

A picture containing text

Description automatically generated

**path.rpt file:**

A screenshot of a computer

Description automatically generated with medium confidence

**power.rpt file:**

Text

Description automatically generated

Clock period used in this design = 1ns = 1000ps

Score = 0.5 \* Movable Cell Area in squm + 0.3 \* (clock period in ps – worst slack in ps) + 0.2 \* total power in uw = 167.2733166

**Design 2**

**Algorithm:**

Initially, the priority is normal (front door, rear door, fire alarm, window, temperature). Then in every cycle, the action with the highest priority in the previous cycle becomes the action with the least priority in the current cycle.

Example:

Cycle 1: front door, rear door, fire alarm, window, temperature

Cycle 2: rear door, fire alarm, window, temperature, front door

Cycle 3: fire alarm, window, temperature, front door, rear door

and so on.

**System Schematic:**Diagram

Description automatically generated

**Description:**

Every clock cycle, the priority encoder determines the state of the system according to the **counter\_value** signal from the counter according to the previously discussed algorithm. The counter starts from 0 to 4 and then goes back to 0, it is increased by 1 in all cycles except if there is no active input, in that case the counter remains as it is for this cycle. The priority encoder outputs a code which represent the state of the system (which is the display output mentioned in the document). The register preserves the state so that any state should take at least 1 cycle. The output decoder maps the system state to the output signals.

**Schematic of the design after synthesis:**

Diagram

Description automatically generated

Diagram

Description automatically generated

Diagram

Description automatically generated

A screenshot of a computer

Description automatically generated with medium confidence

Diagram

Description automatically generated

Diagram

Description automatically generated

A picture containing graphical user interface

Description automatically generatedPre-Synthesis Simulation:

**Graphical user interface

Description automatically generatedPost-Synthesis Simulation:**

**A picture containing graphical user interface

Description automatically generatedPost-Layout Simulation:**

**Chip Schematic:**

**Floor Planning:**

A picture containing text

Description automatically generated

**Power Grid with Routing:**

**Chart

Description automatically generated with medium confidence**

**Power Grid:  
A picture containing chart

Description automatically generated**

**Routing:**

**Schematic

Description automatically generated**

**design.rpt file:**

Text

Description automatically generated with low confidence

**path.rpt file:**

A screenshot of a computer

Description automatically generated with medium confidence

**time.rpt file** (it is included to show the slack of the default path group):

Text

Description automatically generated

**power.rpt file:**  
Text

Description automatically generated

Clock period used in this design = 1ns = 1000ps

Score = 0.5 \* Movable Cell Area in squm + 0.3 \* (clock period in ps – worst slack in ps) + 0.2 \* total power in uw = 319.980055