Ass_Syn_2.0

You have to synthesize your UART_RX files using Design Compiler shell and generate Technology Dependent gate level netlists in Verilog format using standard cell libraries (typical, worst, best) inside std_cells folder:-

- scmetro_tsmc_cl013g_rvt_tt_1p2v_25c.db
- scmetro_tsmc_cl013g_rvt_ff_1p32v_m40c
- scmetro_tsmc_cl013g_rvt_ss_1p08v_125c

Required: -

1. Add the following Optimization Constraints: -
    - Clock Frequency with 10 MHz
    - Clock uncertainty with 0.25 ns for setup
    - Clock uncertainty with 0.05 ns for hold
    - Clock transition with 0.1 ns
    - Input delays on all input ports except (CLK & RST) with 20 clock period
    - Output delays on all output ports with 20% clock period
    - Add Buffer driving cell for all input ports
    - Add load of 50 pf on all output ports
    - Add dont_touch attribute on CLK & RST ports
    - Set operation condition using slow and fast libraries
    - Set wireload model using slow library
2. Check the synthesis log (syn.log) is free of (Errors, Latches, Comb Loops) and modify your RTL files to fix any issues.
3. Generate the following reports: -
    1) Power report using (report_power -hierarchy) command
    2) Area report using (report_area -hierarchy) command
    3) Setup timing analysis report with worst 10 paths
    4) Hold timing analysis report with worst 10 paths
    5) Clocks report using (report_clock –attributes) command
    6) Constraints report using (report_constraint -all_violators) command

4. Generate the following Output files: -
    1) Technology Dependent Gate Level Netlist
    2) SDF File
    3) SVF File

Required: -

A) You have to deliver the following files: -
    0- Synthesis script >> syn_script.tcl
    1- Synthesis log >> syn.log
    2- Technology Dependent Gate Level Netlist >> UART_RX.v
    3- Area report >> Area.rpt
    4- Power report >> power.rpt
    5- Hold analysis report >> hold.rpt
    6- Setup analysis report >> setup.rpt
    7- Clocks report >> clocks.rpt
    8- Constraints report >> constraints.rpt
    9- Ports report >> ports.rpt
    10- SVF File >> UART_RX.svf
    11- SDF File >> UART_RX.sdf