Ass_DFT_1.0

Refer to **Ass_Syn_2.0**, after synthesizing your UART. You have to **insert DFT logic** and generate Technology Dependent gate level netlists post-dft in Verilog format

Steps: -

1. Perform RTL preparation for the **UART RX** (Top Module)
    1) Add scan ports (SI, SE, SO, test_mode, scan_clk, scan_rst)
    2) Mux all the design clocks with scan_clk
    3) Mux all the design resets with scan_ rst
2. Open dft_script.tcl and Add the following commands: -
    1) Configuring scan chain style using set_scan_configuration command
    2) Test-Ready Compile using compile -scan command
    3) Defining the DFT Signals (SI, SE, SO, test_mode, scan_clk, scan_rst) using set_dft_signal command
    4) Create Test Protocol using create_test_protocol command
    5) Preform Pre-DFT Design Rule Checking using dft_drc -verbose command
    6) Preview DFT using preview_dft -show scan_summary command
    7) Insert DFT logic using insert_dft command
    8) Optimize Post DFT Insertion using compile -scan -incremental command
    9) Preform Post-DFT Design Rule Checking using dft_drc -verbose -coverage_estimate command
3. Check the dft log (dft.log) is free of (Errors, Latches, Comb Loops) and modify your RTL files to fix any issues.

Required: -

A) You have to deliver the following files: -

0- dft script >> dft_script.tcl

1- dft log >> dft.log

2- Technology Dependent Gate Level Netlist >> UART_RX.v

3- Area report >> Area.rpt

4- Power report >> power.rpt

5- Hold analysis report >> hold.rpt

6- Setup analysis report >> setup.rpt

7- Clocks report >> clocks.rpt

8- Constraints report >> constraints.rpt

9- Ports report >> ports.rpt

10- Coverage Report >> dft_drc_post_dft.rpt