Ass_Formal 1.0

Referring to **Ass_Syn_2.0** Assignment. You have to run **Formal Verification** of the generated **gate level netlist** verses the **RTL files** of UART RX using Formality Tool

Required: -

A) You have to deliver the following files: -

0- Formality script >> fm_script.tcl

1- Formality log >> fm.log

2- Matched points report >> passing_points.rpt

3- Unmatched points report >> failing_points.rpt

4- Unverified Points report >> unverified_points.rpt

5- Aborted Points report >> aborted_points.rpt