UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Fall 1402
Computer Assignment 6 – Week 16
Accelerator RTL design

Name:
Date:

You are to design an accelerator for calculation of *cos(x)*, where *x* is between 0 and π. Calculation is to be done by Taylor series expansion of *cos(x)*. The input *x* is a 16 bit fixed point number with 8 fractional and 8 integer bits. The output is also a 16 bit fixed point number, the integer part of which is always 0. In addition to the *x* input, the circuit has an 8-bit fixed point *y* input that defines the precision of the calculation of *cos(x)*. The iteration of Taylor series calculations stops if a term being added is less than *y*. Complete the RTL design of this accelerator.

$$\cos x = \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n)!} x^{2n} = 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \cdots \quad \text{for all } x$$

Design Phase:

1. Show the schematic diagram of the datapath of this circuit.
2. Show the controller state diagram.
3. Implement the datapath (on paper) using components discussed in class. Use a lookup-table ROM for coefficients.
4. Write Controller Verilog description and show its Hoffman model.
5. Show how the controller Hoffman model connects to the datapath and outside busses.

Implementation Phase:

1. Build the *cos(x)* computation unit in Quartus II using predefined components and/or SystemVerilog modules. Use a memory hex file for initializing your ROM.
2. Enter the Verilog description of the controller of *cos(x)* in Quartus II.
3. Generate the complete design of *cos(x)*. As mentioned in 1 and 2, you are to build and test the datapath and the controller separately.
4. Synthesize the complete circuit and generate its .vo and .sdo files.
5. In a testbench, test your complete circuit.