Experiment 1 - Clock and Periodic Signal Generation

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***Abstract*— This document is the report of first experiment of logic design lab. It covers some ways for producing clock and signal generation.**

***Keywords*— Clock, Duty Cycle, Ring Oscilator, LM555, Frquency Divider, Breadboard, Osciloscope, Waweform**

I. Introduction

This experiment is designed to learn about delay times, clock frequency generation and digital systems. It also covers how to make circuits that generate periodic signals, and how to test it with an oscilloscope.

II. Clock Generation Using ICs and Analog Components

In this part, we will explain the procedure of making circuits that generate periodic clock signals using 74 Series discrete logic devices and also explain the results of tests that occur in oscilloscope.

1. *Ring Oscillator*

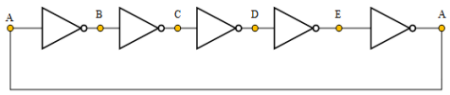

Fig. 1 Ring Oscillator

a. *Procedure*

To build a Ring Oscillator we have to put odd number of inverter gates wired to each other to build the circuit shown in Fig1. For this purpose we used 74HCT04 IC (Fig 2) that includes six inverters and we wired five of them together by connecting following pins: 2 to 3, 4 to 5, 6 to 13, 12 to 11 and 10 to 9 (Fig 3).

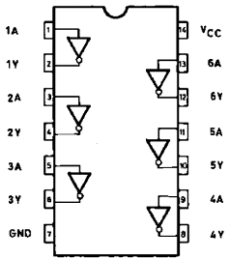

Fig. 2 74HCT04 schematic

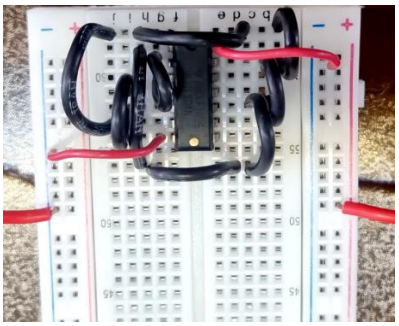

Fig. 3 Circuit on breadboard

b. *Waveform*

As it's shown in fig 4 the frequency of chain is 19.23 MHz.

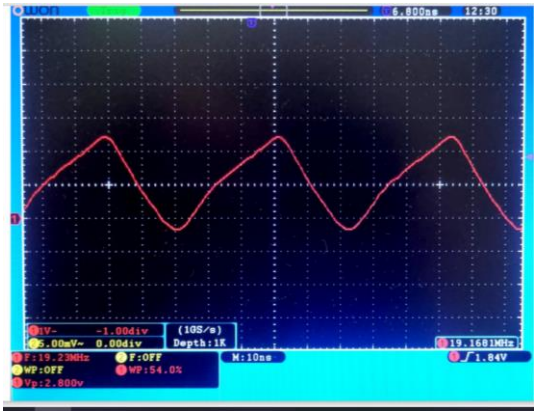

Fig. 4 Waveform of ring oscillator

c. *Calculate Delay of the Chain*

The propagation delay of chain as we know is half of duration of a cycle (that is 1/frequency). So the propagation delay is (1/2)*(1/frequency) and as it's mentioned in last part, the frequency is 19.23 MHz, so duration of a cycle of the chain is 1/19.23 ≈ 52ns and propagation delay of the chain is 1/2*1/19.23MHz ≈ 26ns.

d. *Calculate Delay of One Inverter*

As we said, in one cycle each inverter propagates 2 times so if we show number of inverters with parameter (n) and show the propagation delay of one inverter with parameter (D), the duration of a chain cycle is equal to 2*n*D. So as

we have duration of a cycle from last part (52 ns) and we know that n is equal to 5, if we put this numbers in the formula we can calculate D. So the propagation delay of one inverter (D) is equal to 52/(2*5) = 5.2 ns.

2. *LM555 Timer*

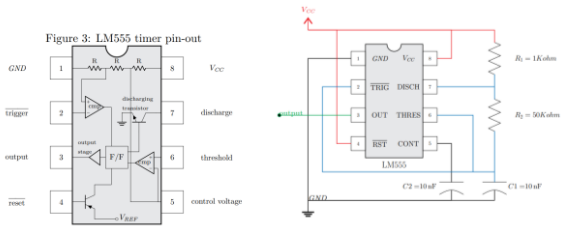

Fig. 5 LM555 in astable mode

a. Procedure

In this part we used LM555 IC (Fig 5) in astable mode for generating clock signal. We used 2 capacitors and 2 resistors. The external capacitor C1 charges through R1 + R2 and discharges through R2. In this part of experiment we used different resistors for R2 and we wanted to see its effect on duty cycle and frequency .We used a 1 kΩ resistor for R1 and we change R2 from a 1kΩ resistor to a 10 kΩ resistor and then we change it to 100 kΩ (Fig 6 to 8). We measure the frequency and duty cycle with each R2 resistors and compare them.

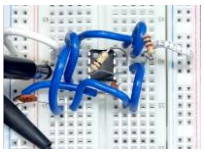

Fig. 6 Circuit on breadboard (R2 = 100 kΩ)

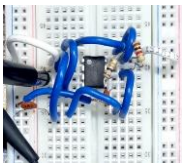

Fig. 7 Circuit on breadboard (R2 = 10 kΩ)

Fig. 8 Circuit on breadboard (R2 = 1 kΩ)

b. Waveforms (i and ii parts)

According to figure 5, the charge time (output high) is given by T1 = 0.693 ∗ (R1 + R2) ∗ C and the discharge time (output low) by T2 = 0.693 ∗ R2 ∗ C. Thus, the total time period of the square wave is T = T1 + T2 = 0.693 ∗ (R1 + 2R2) ∗ C. Consequently, the frequency of oscillation is 1 / T. The duty cycle also can be computed by (R1+R2) / (R1+2 * R2).

In this part we will calculate frequency with upper formula for each R2 resistors and compare them with our observations with oscilloscope. (R1 = 1kΩ, C = 10nF)
The frequency with each R2 resistor is:
R2 = 1kΩ (Fig 9) :

- With equations: F = 48.1KHz, Duty cycle = 66.67%
- On oscilloscope: F = 41.475KHz, Duty cycle = 64.4%

R2 = 10 k ohm (Fig 10) :

- With equations: F = 6.87KHz, Duty cycle = 52.38%
- On oscilloscope: F = 5.840KHz, Duty cycle = 51.1%

R2 = 100 k ohm (Fig 11) :

- With equations: F = 717.9 Hz, Duty cycle = 50.24%
- On oscilloscope: F = 685.4 Hz, Duty cycle = 49.1%

As you can see, the frequency and duty cycle of observed data is very close to the frequency and duty cycles that calculated with equations.

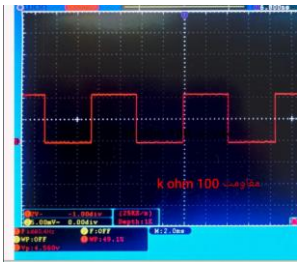

Fig. 9 Waveform (R2 = 100 kΩ)

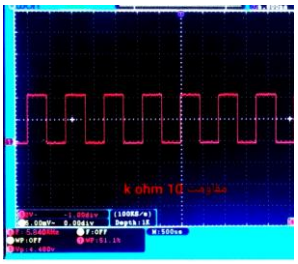

Fig. 10 Waveform (R2 = 10 kΩ)

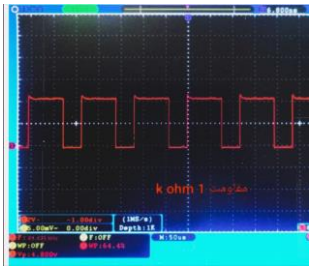

Fig. 11 Waveform (R2 = 1 kΩ)

c. Explanations

As we can see by observation, by increasing the resistance (R2), the duty cycle gets closer to 50%. Also with equations we can prove that it is a correct statement. As we know the duty cycle is equal to (R1 + R2) / (R1 + 2 * R2) so if we increase R2 resistance, the calculated duty cycle by equation gets closer to 1/2 or 50%.

3. *Schmitt Trigger Oscillator*

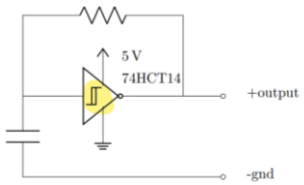

Fig. 12 Schmitt inverter oscillator circuit

a. Procedure

In this part we used a 74HCT14 IC (Fig 12) , a resistor and a capacitor to build a clock signal generator. We increase the resistance and see its effects. We used 470Ω, 1kΩ and 2.2kΩ resistors (Fig 13 to 15).

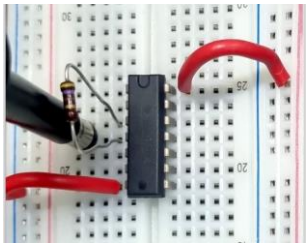

Fig. 13 Circuit on breadboard (R = 470 Ω)

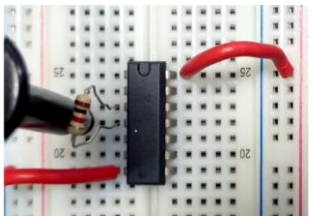

Fig. 14 Circuit on breadboard (R = 1 kΩ)

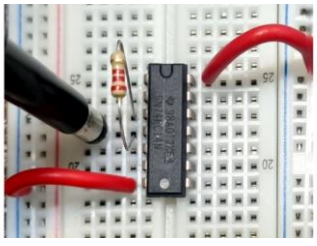

Fig. 15 Circuit on breadboard (R = 2.2 kΩ)

b. Calculate α

We have following equation for frequency : f = α / RC which α is a constant. As you can see for each resistor we calculated α by using α = f.RC equation. (C = 10nf)

R = 470Ω (Fig 16) :

- F = 56.5 KHz, α = 0.26555

R = 1 kΩ (Fig 17) :

- F = 24.92 KHz, α = 0.2492

R = 2.2 kΩ (Fig 18) :

- F = 12.1 KHz, α = 0.2662

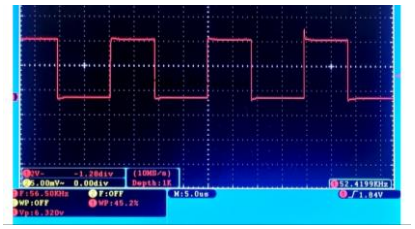

Fig. 16 Waveform (R = 470 Ω)

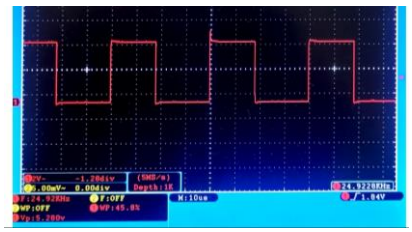

Fig. 17 Waveform (R = 1 kΩ)

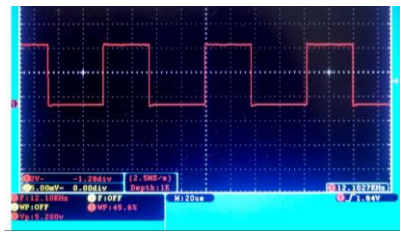

Fig. 18 Waveform (R = 2.2 kΩ)

c. Calculate average α

The average amount of α is (0.26555+0.2492+0.2662) / 3 = 0.2603

4. *Synchronous Counter as a Frequency Divider*

a. Procedure

In this part of experiment we built a Frequency Divider (divide by 200) by using counters (74HC193 IC that shown in Fig 19) and using Ring Oscillator from part one for their clocks (schematic of this frequency divider is shown in Fig 20 and schematic of ring oscillator is shown in Fig 1) . For initializing the counters we used and-gates of 74HC08 IC. For dividing by 200 we had to use two 4-bit counters and drive number 56 (256 – 200 =

56) in binary form in their parallel input (our circuit is shown in Fig 21).

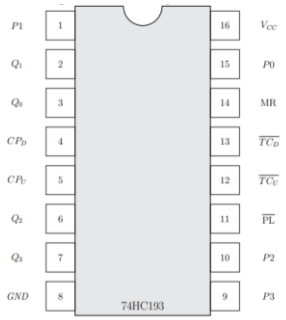

Fig. 19 Pin layout of 74193

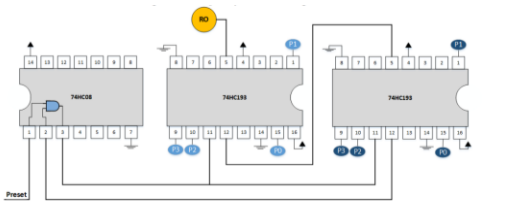

Fig. 20 Frequency divider using 74193

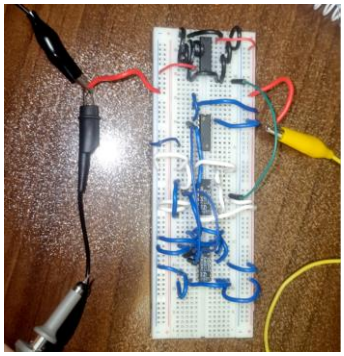

Fig. 21 frequency divider on breadboard

b. Determine the Parallel Input Values

We wanted to divide by 200 so we have to put (256 – 200 = 56) in Parallel Input using (Initial value = Maximum value – Modulus) equation. If we convert 56 to binary it would be 00111000 and because we have two 4-bit counters, we have to put 0011 (MSB) on parallel input of one of them and 1000 (LSB) on parallel input of another one. For doing this, each digit that is supposed to be one, we connected its pin to Vdd (supply 1) and each digit that is supposed to be zero, we connected its pin to Gnd (supply 0).

c. Presetting Mechanism

The counters should load the parallel input for presetting or when the counters reach 255 (the carryout becomes active). For this purpose we used an and-gate to (and) the carryout and preset together and for initializing the value of counters at first we just need to connect the preset wire in fig 20 to Vdd for a short time and then disconnect it so the Parallel load of counters gets its active value and the desired value loads into counters.

d. Waveforms

As we can see in Fig 22, Duty cycle of out signal is 99.3% and its frecuency is 103.583KHz.

e. Compare Outputs

As you can see in Fig 22, the frequency of circuit of this part is 103.583 KHz and the frequency of the Ring Oscillator as we measured at the beginning is 19.23 MHz. The goal of this circuit is deviding the frequency of the Ring Oscillator by 200. So if we calculate, we have 19.23 * 10^6 / 200 = 96.15 * 10^3 or 96.15 KHz and it's so close to our observation which is 103.58 KHz.

About duty cycle, the ring oscillators duty cycle was 54% but for this circuit the duty cycle as we can see in the waveform, is very high and it is because of that the output becomes 0 just for a short time (one clock cycle of Ring Oscillator) and for the most of the time it's 1 (because the counter didn't reach 255).

Fig. 22 Frequency divider's waveform

5. *T Flip-Flop*

a. Procedure

The purpose of using TFF is to make the duty cycle 50% because it toggles just when there is a rising edge of its clock (carryout of last part) and because of that the time between two rising edges are equal, the time that the output is 1 is as the same as the time that output is 0 so the duty cycle become 50%. Build the TFF, we used a D Flip-Flop, 74HC74 IC, and converted it to a T Flip-Flop as the pin layout shown in Fig 23, out circuit is also shown in Fig 24.

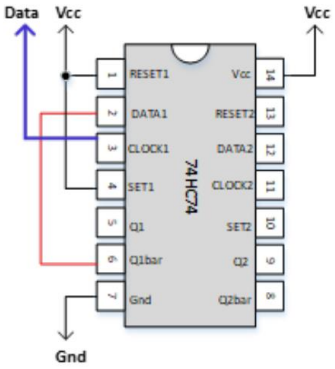

Fig. 23 D Flip-Flop connection

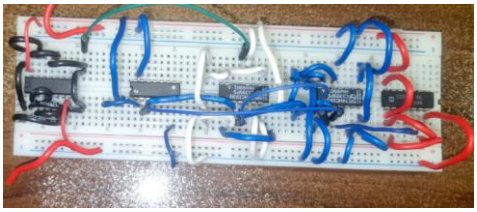

Fig. 24 Final circuit on breadboard

b. Compare Outputs

The frequency of this circuit is 52.17 KHz (Fig 25). It changes our divide by 200 circuit to a divide by 400 circuit and its because of that the TFF clock is divided by 200 so the frequency of the output would be 1/2 of the last part frequency (its input) and 1/400 of the Ring Oscillator frequency. If we calculate the frequency by the upper statement, we have 103.58 * 10^3 / 2 = 51.79 * 10^3 Hz and 19.23 * 10^6 / 400 = 48.075 * 10^3 Hz and these frequencies are very close to this circuit output frequency which is 52.17 KHz.

Fig. 25 Final circuit's waveform

III. Conclusions

There are many ways to make a circuit that generate periodic signal. In this experiment we learned some of them and observed the parameters such as duty cycle and frequency. We also learned how to make a frequency divider and make its duty cycle to 50% and we learned some theorical equations and we examine our observed data with them. The main purpose of this experiment is how to generate a periodic signal and how make a sequential circuits using clock, counter and flip flops and how to put them together.

References

[1] K. Basharkhah “Experiment 1 Digital Logic Laboratory,” under supervision of Professor Z. Navabi, University of Tehran, Spring 1403