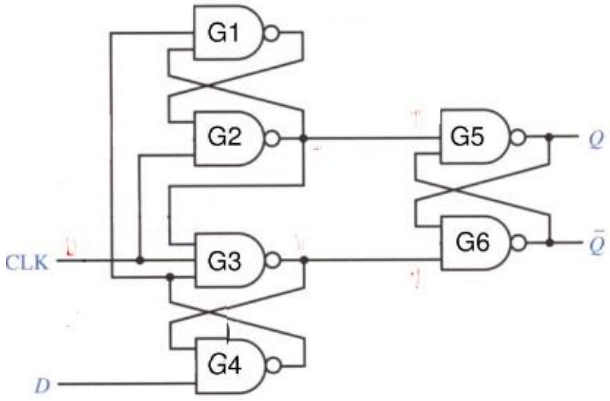
UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, ECE 894, Fall 1402
Computer Assignment 4
Latches and Flip-Flops
Week 12

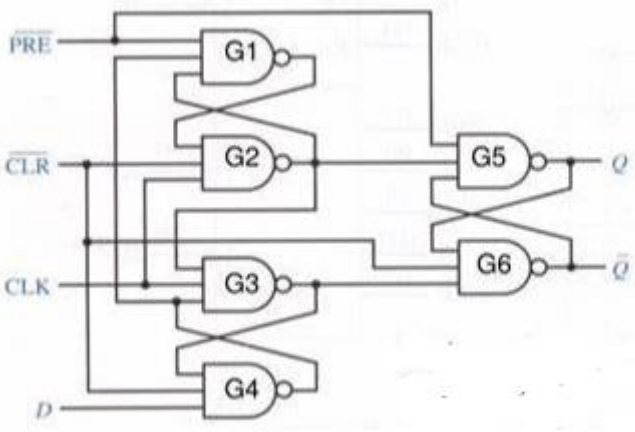
Name:
Date:

1. Generate an SR-latch with active low inputs.
   a. Show this circuit in terms of an all-NAND circuit. Describe this circuit in Verilog using NAND primitives. Write the upper gate such that it can be used as a 2-input or 3-input NAND.
   b. Annotate this circuit with gate delays that are based on switch level delays of 4 NS for the NMOS and 6 NS for the PMOS transistors.
   c. Simulate the circuit to verify its operation. Apply simultaneous active inputs (S and R) and see the loss of memory.

2. Using three of the cross coupled structures of Part 1 to build the D flip-flop circuit shown below.
   a. Write the Verilog description of the circuit.
   b. Simulate this circuit and examine it for edge triggering behavior. Show the delay values on the output after the edge of the clock. Show that changing D while the clock is active will not affect the flip-flop Q output.
   c. Setup time (t_{setup}) is defined as the time that a change on the input must be stable before the edge of the clock arrives. Estimate the setup time and examine your Verilog model to see what happens when you violate it.
   d. Hold time (t_{hold}) is defined as the time the D value must be stable (hold D at its value) after the edge of the clock selects it. Estimate the hold time and examine your Verilog model to see what happens when you violate it.



3. Using three of the cross coupled structures of Part 1 to build the D flip-flop with PRE and CLR shown below.
   e. Write the Verilog description of the circuit.
   f. Simulate this circuit and examine it for D input clocking, Preset, and Clear operations. Show the output delay after D is clocked, Presetting, and Clearing the flip-flop.
   g. Clock the flip-flop while Preset or Clear are active and see what happens to the flip-flop output.
   h. Examine the case that Preset and Clear are simultaneously active.



Deliverables:
- For all parts show the circuit, partial timing diagrams and the timings.

- For parts that you are examining the operation of the flip-flop, hand-draw the wavefoirms you are applying and the expected outputs.
- Be able to justify all timings of the simulation waveforms.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.