CorridorOS â Theory of Compute

A 2â minute tour

Photonic corridors (¸» lanes), Freeâ Form Memory (CXL) with bandwidth floors, HELIOPASS calibration, and system safety.

HELIOPASS â Photonic Environment Calibration

Stabilize BER and eye with minimal power

HELIOPASS estimates background offset from lunar, airglow, galactic, and skyglow contributions and tunes bias/¸» to hold error targets.

Photonic Corridors (¸» Lanes)

Reserve wavelength sets per workload

Corridors allocate WDM lanes with policy: shaping, preemption guards, and powerâ aware bias tuning via HELIOPASS integration.

Freeâ Form Memory (CXL)

GB/s floors as firstâ class resources

Pooled memory carved into QoS bundles with floor guarantees and latency classes; exposed to schedulers via CRDs and attested at boot.

Tactile Power â Pinâ free, Genderless

Padâ toâ pad, magnetâ aligned, or contactless

Devices receive power without exposed pins: capacitive/inductive couplers with preâ charge, or flush pads with current sharing.

Observability â Proof, Not Promises

Grafana Pack ´• Floors ´• BER ´• Energy/Bit

CorridorOS exports floors, lane utilization, BER, and energy/bit outâ ofâ theâ box. Golden dashboards ship day one â pilots see p99 drop, floors hold.

Security & Integrity â Builtâ In

Measured Boot ´• SPDM ´• PQC Ready

Attested startup, signed components, SPDM policy lanes, and PQCâ ready crypto harden the plane â production stays safe; Labs stays sandboxed.

Putting It Together

Schedule compute, light, memory â and power

CorridorOS unifies photonic corridors, calibrated by HELIOPASS, with QoS memory and safe, pinâ free power delivery â observable and schedulable from day one.