SPI Communication:

The Serial Peripheral Interface (SPI) is a bus interface connection protocol originally started by Motorola Corp. It uses four pins for communication.

- SDI (serial Data Input).
- SDO (Serial Data output).
- SCLK (Serial Clock).
- CS (Chip Select).

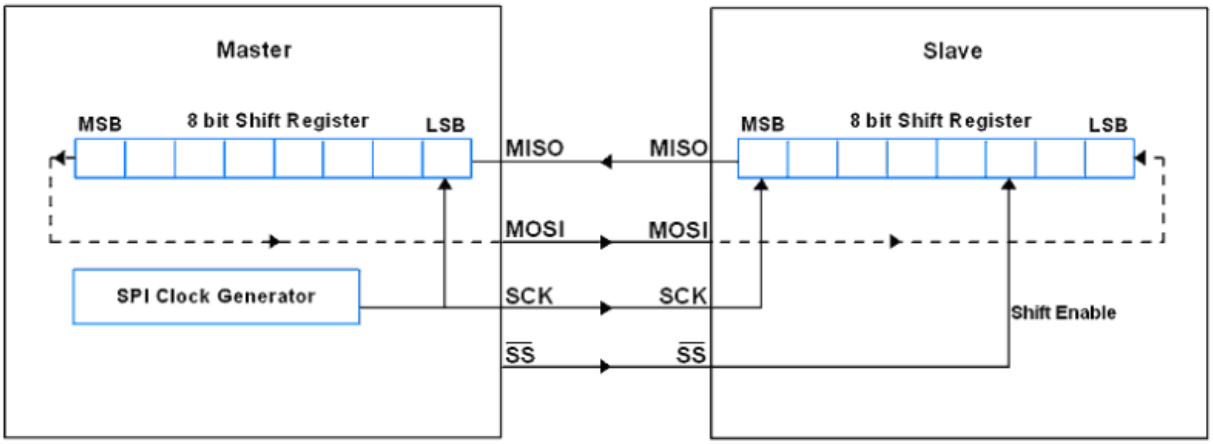
ATMega32 SPI Communication:

- MISO (Master In Slave Out)
  The Master receives data and the slave transmits data.
- MOSI (Master Out Slave In)
  The master transmits data and the slave receives data.
- SCK (Shift Clock)

  The Master generates this clock for the communication, which is used by the slave.

- SS (Slave Select)

  Master can select slaves through this pin.



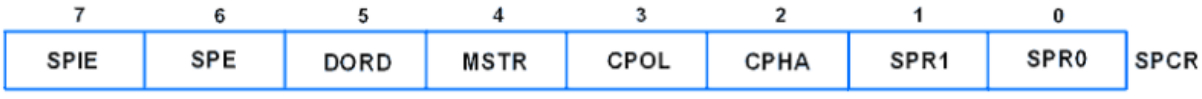
SPI Master Slave Interconnection

Pin Configurations:

SPI Pins	Pin on ATMega32	Pin Direction (Master)	Pin Direction (Slave)
MISO	B6	Input	Output
MOSI	B5	Output	Input
SCK	B7	Output	Input
SS	B4	Output	Input

AVR ATMega32 uses three registers to configure SPI communication that are SPI Control Register, SPI status Register and SPI Data Register.

SPCR: SPI Control Register:



Bit 7 – SPIE: SPI interrupt Enable bit

- 1 -> Enable SPI interrupt
- 0 -> Disable SPI interrupt

Bit6-SPE: SPI Enable bit

- 1 -> Enable SPI
- 0 -> Disable SPI

Bit5-DORD: Data order bit

- 1 -> LSB transmitted first
- 0 -> MSB transmitted first

Bit4 – MSTR: Master/Slave select bit

- 1-> Master Mode
- 0-> Slave mode

Bit3 – CPOL: Clock polarity Select bit

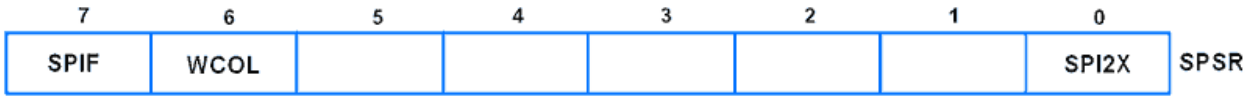
- 1 -> Clock start from logical one
- 0 -> Clock start from logical zero.

Bit2 – CPHA: Clock phase Select bit

- 1 -> Data Sample on training clock edge
- 0 -> Data sample on the leading clock edge

Bit1:0 – SPR1:SPR0 SPI clock Rate Select bits

SPSR: SPI Status Register



Bit 7 – SPIF: SPI interrupt flag bit

- This flag gets set when the serial transfer is complete.
- Also gets set when the SS pin is driven low in master mode.
- It can generate an interrupt when SPIE bit in SPCR and a global interrupt is enabled.

Bit 6 – WCOL: Write Collision Flag bit

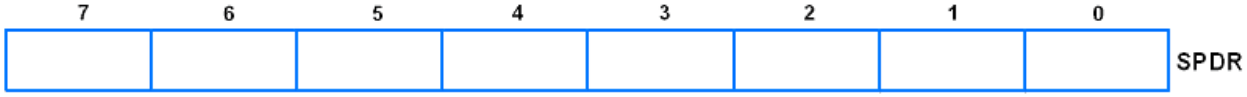
- This bit gets set when SPI data register writes occurs during previous data transfer.

Bit 5:1 – Reserved Bits

Bit 0 – SPI2X: Double SPI Speed bit

- When set, SPI speed (SCK Frequency) gets doubled.

SPDR: SPI Data Register



- SPI Data register used to transfer data between the Register file and SPI Shift Register.
- Writing to the SPDR initiates data transmission.

Programming For TC72

The overall programming interface lists below:

1. Set up the SPI to master mode
2. Select SPI clock and data sampling mode
3. Set up digital output for display
4. Send the command to TC72
5. Read temperature from TC72
6. Display the result