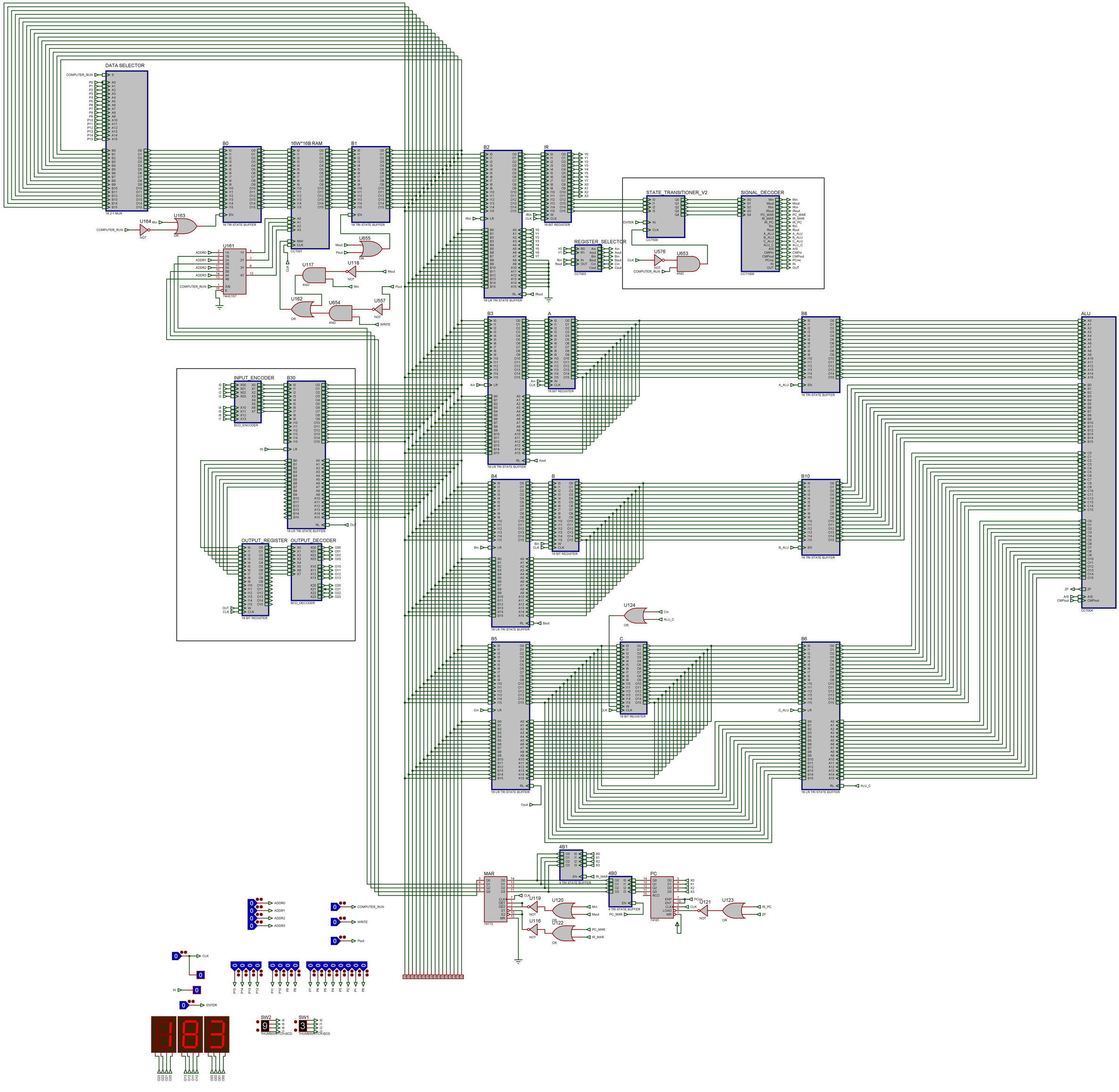
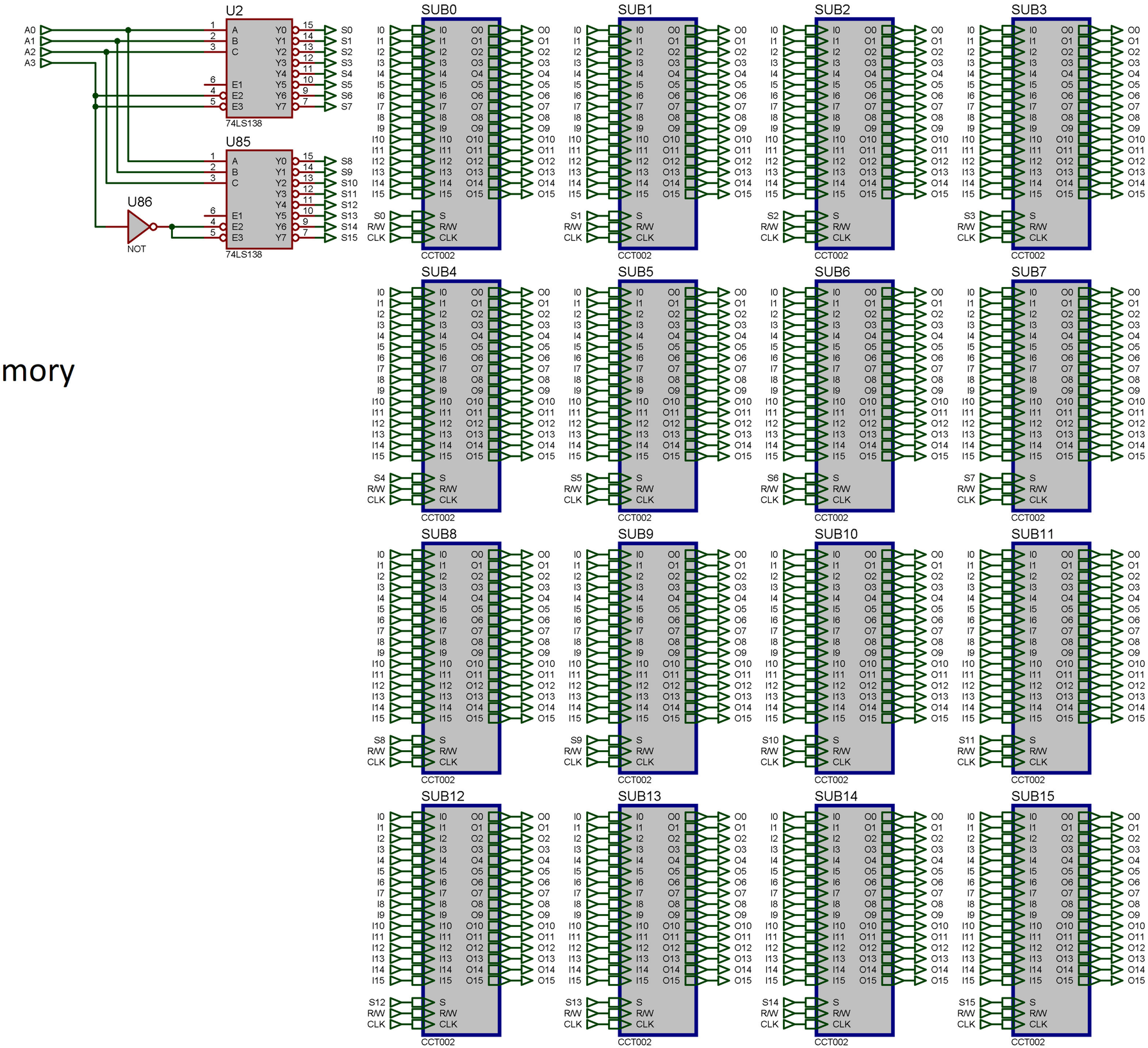
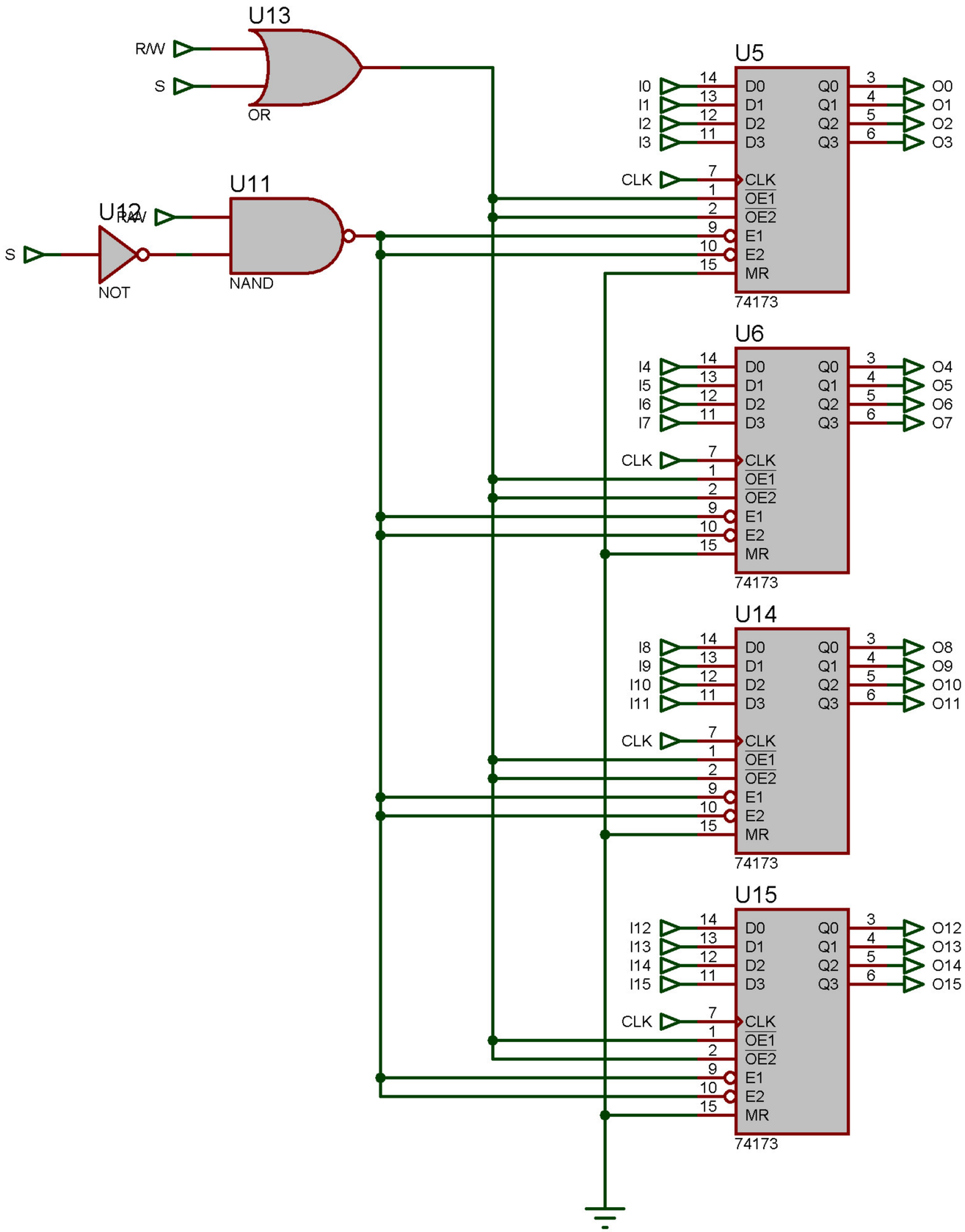

DATA SELECTOR
16 2-1 MUX
B0
16 TRI STATE BUFFER
16W*16B RAM
CCT001
B1
16 TRI STATE BUFFER
B2
16 LR TRI STATE BUFFER
IR
16 BIT REGISTER
STATE_TRANSITIONER_V2
CCT500
SIGNAL_DECODER
CCT1000
REGISTER_SELECTOR
CCT003
U161
74HC157
U163
U164
U655
U117
U118
U162
U654
U557
U576
U653
B3
16 LR TRI STATE BUFFER
A
16 BIT REGISTER
B8
16 TRI STATE BUFFER
ALU
CCT004
INPUT_ENCODER
BCD_ENCODER
B30
16 LR TRI STATE BUFFER
OUTPUT_REGISTER
16 BIT REGISTER
OUTPUT_DECODER
BCD_DECODER
B4
16 LR TRI STATE BUFFER
B
16 BIT REGISTER
B10
16 TRI STATE BUFFER
U124
B5
16 LR TRI STATE BUFFER
C
16 BIT REGISTER
B6
16 LR TRI STATE BUFFER
4B1
4 TRI STATE BUFFER
MAR
74173
4B0
4 TRI STATE BUFFER
PC
74161
U119
U120
U116
U122
U121
U123
ADDR0
ADDR1
ADDR2
ADDR3
COMPUTER_RUN
WRITE
Pout
CLK
IN
ENTER
SW2
THUMBSWITCH-BCD
SW1
THUMBSWITCH-BCD

Memory


U2
U85
U86
NOT
74LS138
A0
A1
A2
A3
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
SUB0
SUB1
SUB2
SUB3
SUB4
SUB5
SUB6
SUB7
SUB8
SUB9
SUB10
SUB11
SUB12
SUB13
SUB14
SUB15
CCT002
R/W
CLK



Register

S	R/W	EN	OE
0	0	0	1
0	1	1	0
1	0	0	0
1	1	0	0

$$EN = \overline{S}.\overline{R/W} = \overline{S + R/W}$$

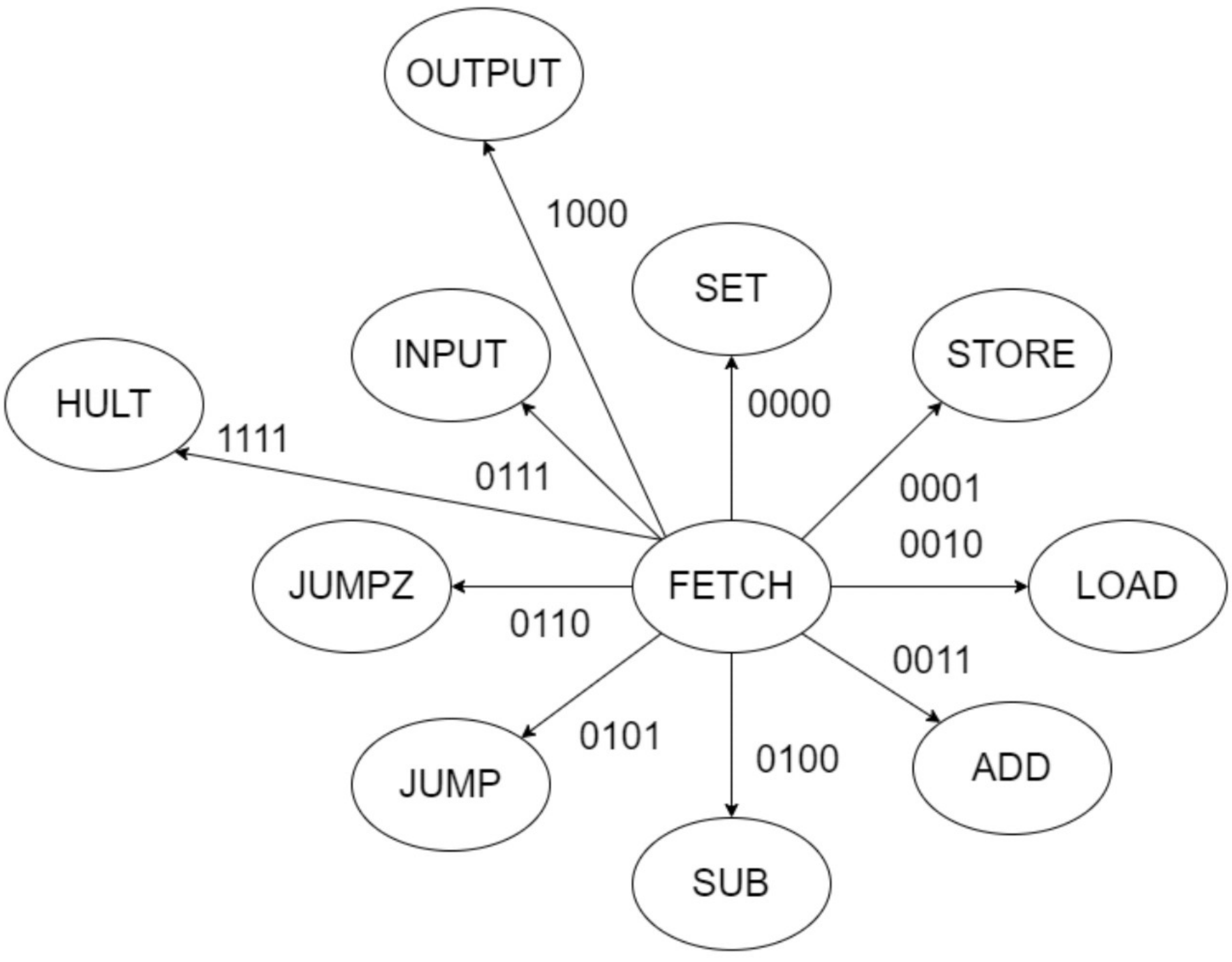
$$OE = \overline{S}.R/W$$

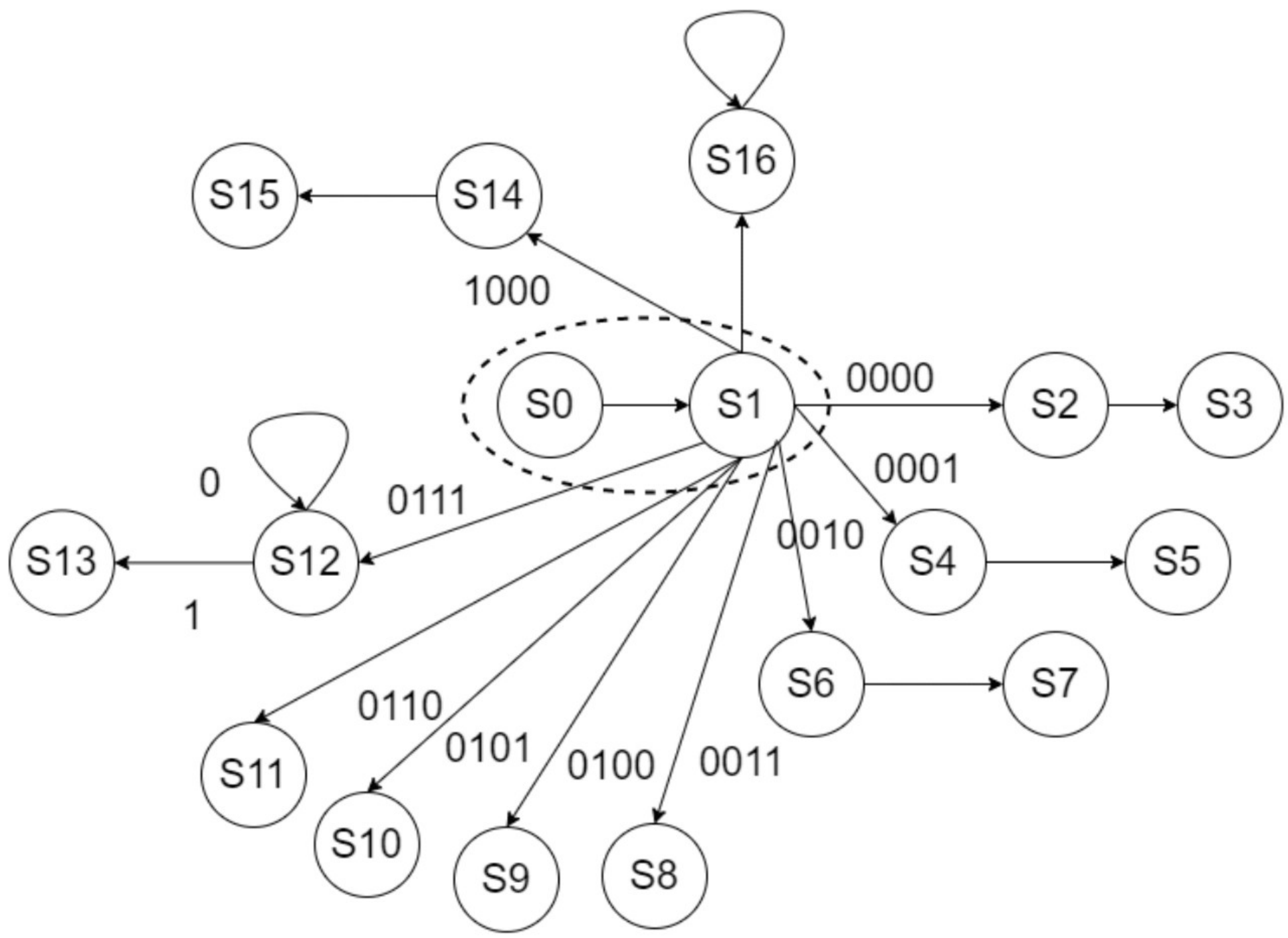
Control Unit

Microinstructions

FETCH PC_MAR Mout IRin PCinc	SET (0000) IR_MAR Min IRout
STORE (0001) IR_MAR Min Rout	LOAD (0010) IR_MAR Mout Rin
ADD (0011) A_ALU B_ALU A/S=0 ALU_C	SUB (0100) A_ALU B_ALU A/S=1 ALU_C
JUMP (0101) IR_PC	JMPZ (0110) C_ALU CMPout
INPUT (0111) IR_MAR IN Min IN	OUTPUT (1000) IR_MAR Mout OUT

State Transition Diagram




S16
S15
S14
1000
S0
S1
0000
S2
S3
0
0111
0001
S13
S12
0010
S4
S5
1
S6
S7
0110
0101
0100
0011
S11
S10
S9
S8

CS / IN / NS – TABLE

Current State					Input				NTR	Next State				
Q4	Q3	Q2	Q1	Q0	I3	I2	I1	I0		Q4*	Q3*	Q2*	Q1*	Q0*
0	0	0	0	0	X	X	X	X		0	0	0	0	1
0	0	0	0	1	0	0	0	0		0	0	0	1	0
0	0	0	0	1	0	0	0	1		0	0	1	0	0
0	0	0	0	1	0	0	1	0		0	0	1	1	0
0	0	0	0	1	0	0	1	1		0	1	0	0	0
0	0	0	0	1	0	1	0	0		0	1	0	0	1
0	0	0	0	1	0	1	0	1		0	1	0	1	0
0	0	0	0	1	0	1	1	0		0	1	0	1	1
0	0	0	0	1	0	1	1	1		0	1	1	0	0
0	0	0	0	1	1	0	0	0		0	1	1	1	0
0	0	0	0	1	1	1	1	1		1	0	0	0	0
0	0	0	1	0	X	X	X	X		0	0	0	1	1
0	0	0	1	1	X	X	X	X		0	0	0	0	0
0	0	1	0	0	X	X	X	X		0	0	1	0	1
0	0	1	0	1	X	X	X	X		0	0	0	0	0
0	0	1	1	0	X	X	X	X		0	0	1	1	1
0	0	1	1	1	X	X	X	X		0	0	0	0	0
0	1	0	0	0	X	X	X	X		0	0	0	0	0
0	1	0	0	1	X	X	X	X		0	0	0	0	0
0	1	0	1	0	X	X	X	X		0	0	0	0	0
0	1	0	1	1	X	X	X	X		0	0	0	0	0
0	1	1	0	0	X	X	X	X	0 1	0 0	1 1	1 1	0 0	0 1
0	1	1	0	1	X	X	X	X		0	0	0	0	0
0	1	1	1	0	X	X	X	X		0	1	1	1	1
0	1	1	1	1	X	X	X	X		0	0	0	0	0
1	0	0	0	0	X	X	X	X		1	0	0	0	0

CS / IN / NS – TABLE V2

Current State	Input	NTR	Next State				
CS	IN		Q4*	Q3*	Q2*	Q1*	Q0*
0	X		0	0	0	0	1
1	0		0	0	0	1	0
1	1		0	0	1	0	0
1	2		0	0	1	1	0
1	3		0	1	0	0	0
1	4		0	1	0	0	1
1	5		0	1	0	1	0
1	6		0	1	0	1	1
1	7		0	1	1	0	0
1	8		0	1	1	1	0
1	15		1	0	0	0	0
2	X		0	0	0	1	1
3	X		0	0	0	0	0
4	X		0	0	1	0	1
5	X		0	0	0	0	0
6	X		0	0	1	1	1
7	X		0	0	0	0	0
8	X		0	0	0	0	0
9	X		0	0	0	0	0
10	X		0	0	0	0	0
11	X		0	0	0	0	0
12	X	0 1	0 0	1 1	1 1	0 0	0 1
13	X		0	0	0	0	0
14	X		0	1	1	1	1
15	X		0	0	0	0	0
16	X		1	0	0	0	0

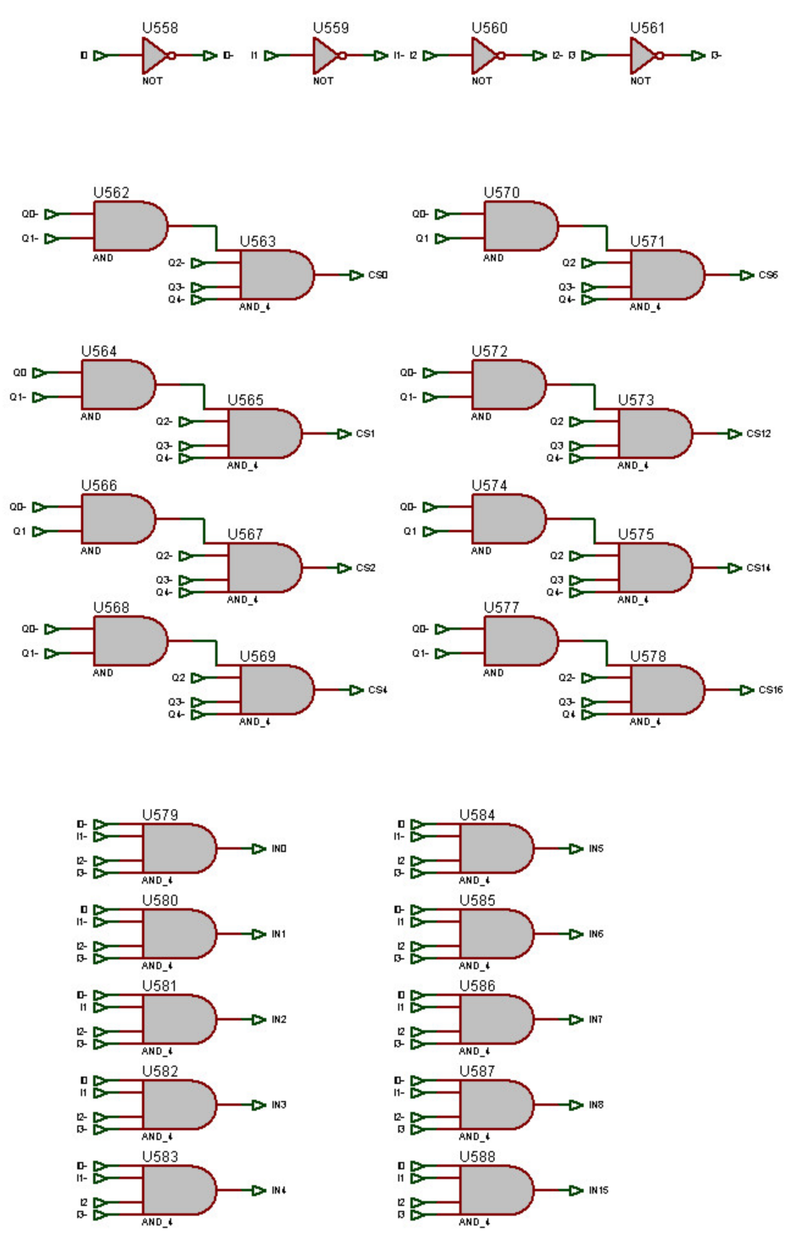
Q0* = CS0 + CS1.(IN4 + IN6) + CS2 + CS4 + CS6 + CS12.NTR + CS14

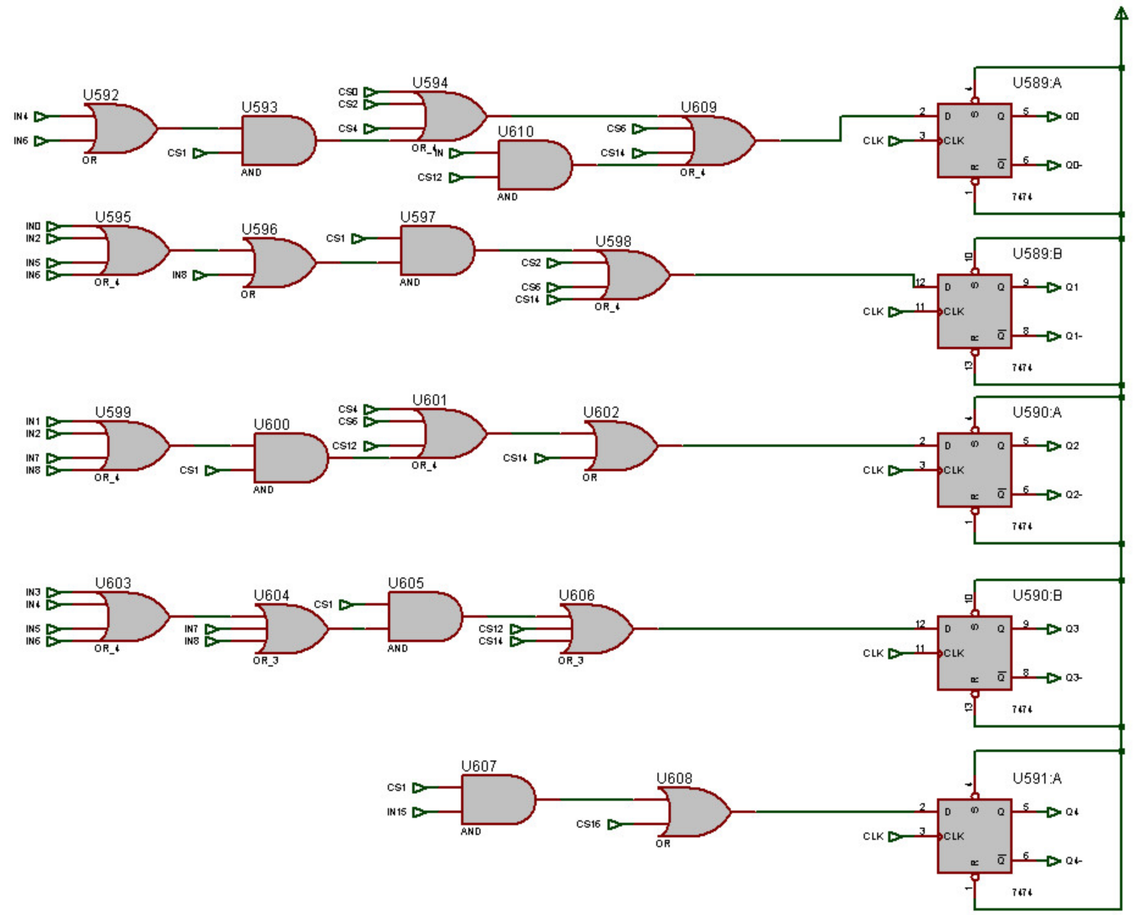
Q1* = CS1.(IN0 + IN2 + IN5 + IN6 + IN8) + CS2 + CS6 + CS14

Q2* = CS1.(IN1 + IN2 + IN7 + IN8) + CS4 + CS6 + CS12 + CS14

Q3* = CS1.(IN3 + IN4 + IN5 + IN6 + IN7 + IN8) + CS12 + CS14

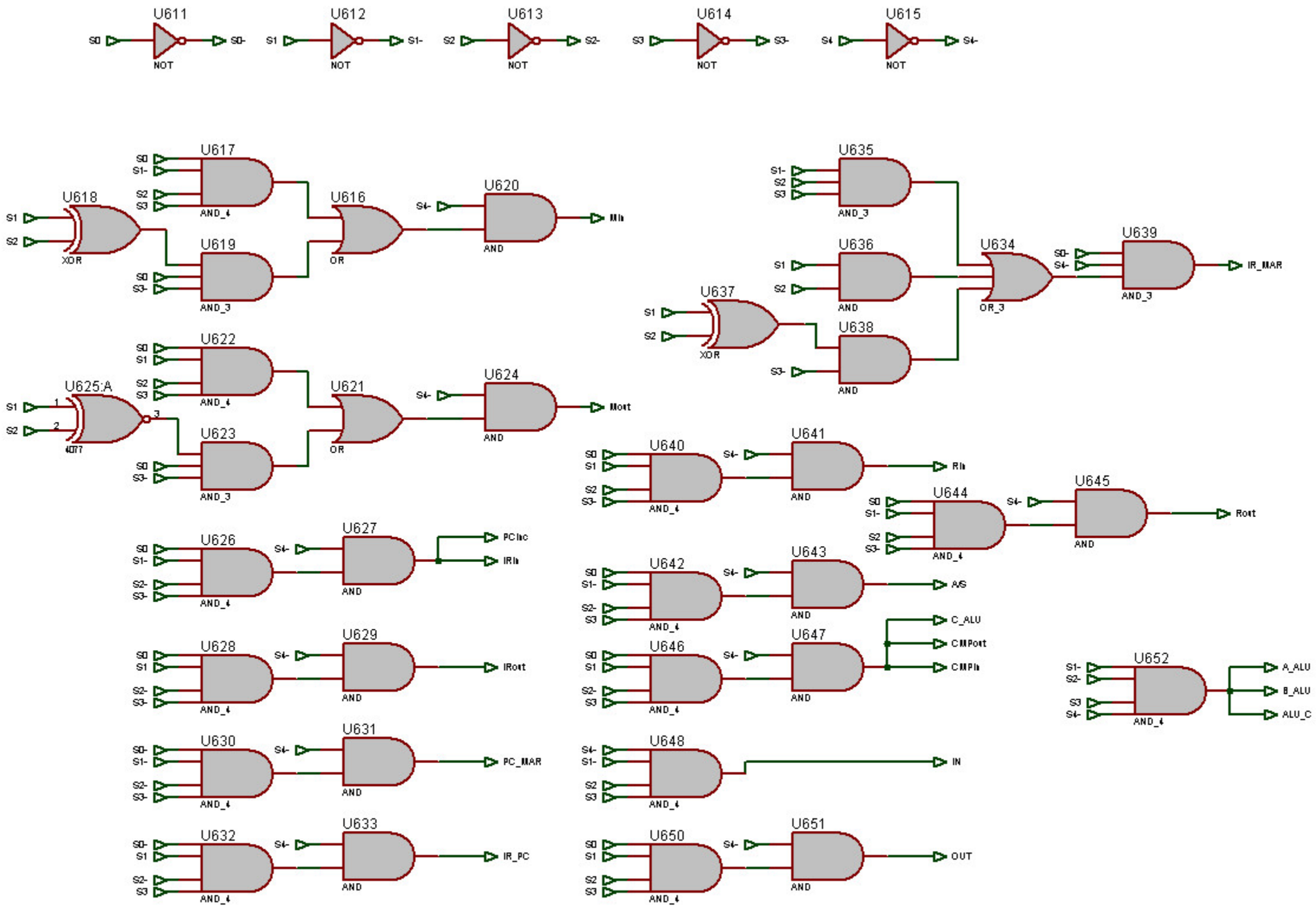
Q4* = CS1.IN15 + CS16

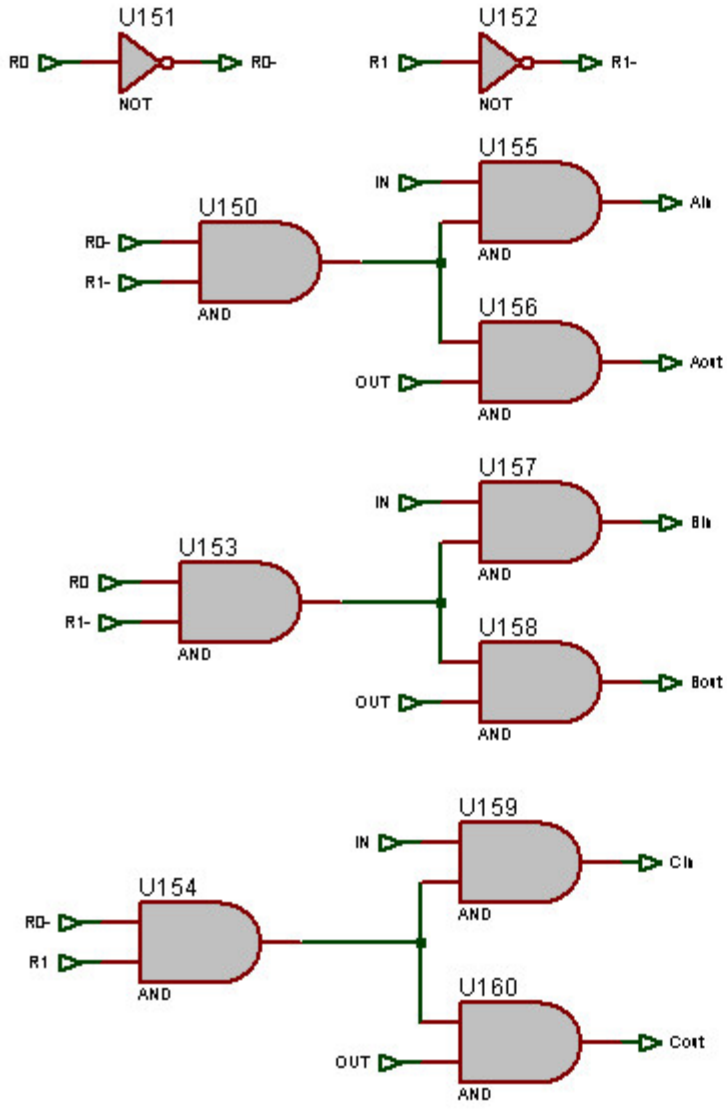

U558 NOT
U559 NOT
U560 NOT
U561 NOT
U562 AND
U563 AND_4 CS0
U570 AND
U571 AND_4 CS6
U564 AND
U565 AND_4 CS1
U572 AND
U573 AND_4 CS12
U566 AND
U567 AND_4 CS2
U574 AND
U575 AND_4 CS14
U568 AND
U569 AND_4 CS4
U577 AND
U578 AND_4 CS16
U579 AND_4 IN0
U584 AND_4 IN5
U580 AND_4 IN1
U585 AND_4 IN6
U581 AND_4 IN2
U586 AND_4 IN7
U582 AND_4 IN3
U587 AND_4 IN8
U583 AND_4 IN4
U588 AND_4 IN15


U592 OR
U593 AND
U594 OR_4
U610 AND
U609 OR_4
U589:A 7474
U595 OR_4
U596 OR
U597 AND
U598 OR_4
U589:B 7474
U599 OR_4
U600 AND
U601 OR_4
U602 OR
U590:A 7474
U603 OR_4
U604 OR_3
U605 AND
U606 OR_3
U590:B 7474
U607 AND
U608 OR
U591:A 7474

Signal Decoder Table

INPUT					OUTPUT SIGNALS																		
S4	S3	S2	S1	S0	Mi	Mo	IRi	IRo	PC_M	IR_M	IR_PC	Ri	Ro	A_AL	B_AL	C_AL	AL_C	A/S	CMPo	PCinc	IN	OUT
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	1													1		0
0	0	0	1	0	0					1												0
0	0	0	1	1	1			1														0
0	0	1	0	0	0					1												0
0	0	1	0	1	1								1									0
0	0	1	1	0	0					1												0
0	0	1	1	1	0	1						1										0
0	1	0	0	0	0									1	1		1	0				0
0	1	0	0	1	0									1	1		1	1				0
0	1	0	1	0	0						1											0
0	1	0	1	1	0											1			1			0
0	1	1	0	0	0					1											1	0
0	1	1	0	1	0																1	0
0	1	1	1	0	0					1												0
0	1	1	1	1	0	1																1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

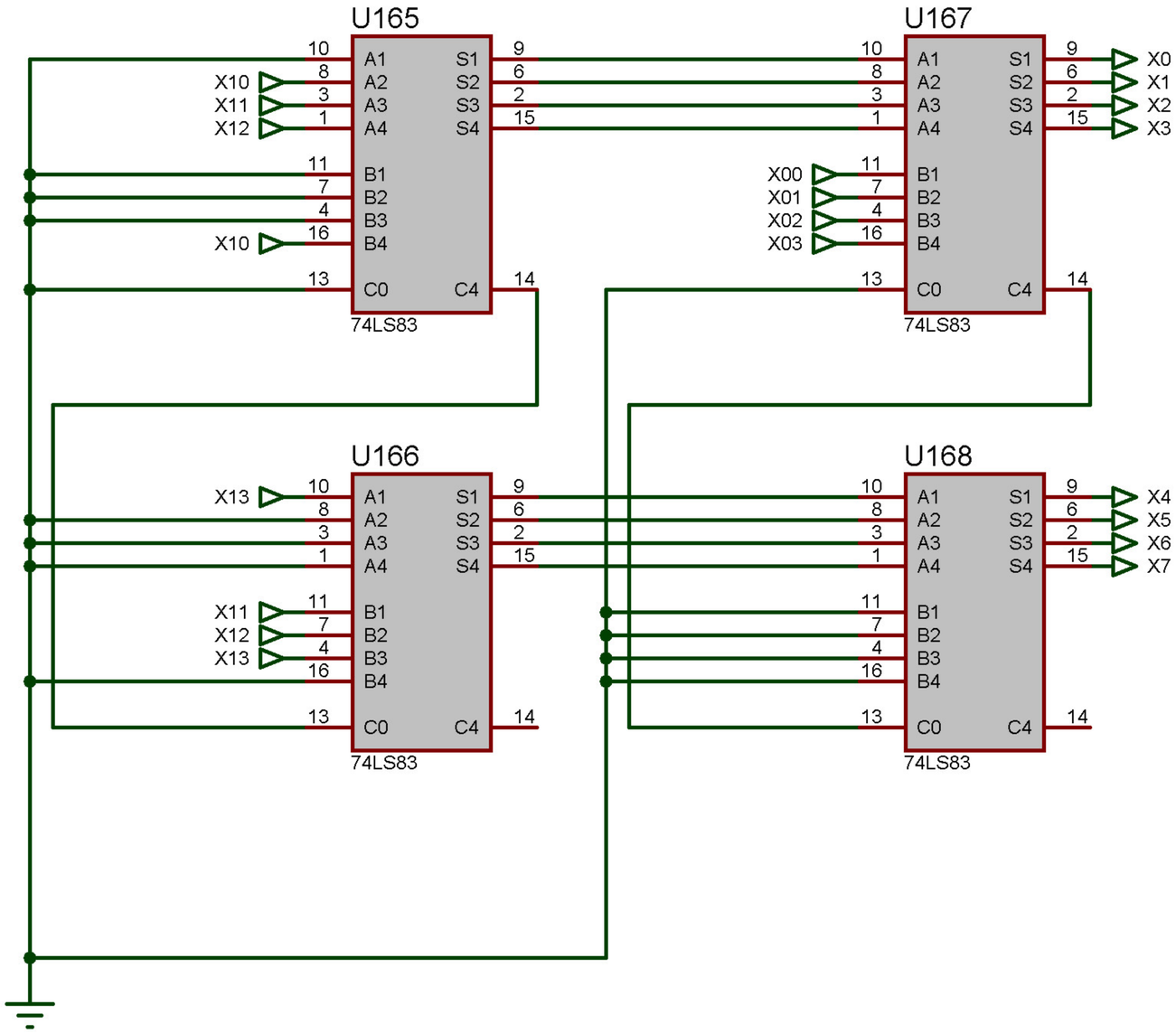

U611
S0
S0-
NOT
U612
S1
S1-
NOT
U613
S2
S2-
NOT
U614
S3
S3-
NOT
U615
S4
S4-
NOT
U617
AND_4
U618
XOR
U619
AND_3
U616
OR
U620
AND
Min
U635
AND_3
U636
AND
U637
XOR
U638
AND
U634
OR_3
U639
AND_3
IR_MAR
U622
AND_4
U625:A
4077
U623
AND_3
U621
OR
U624
AND
Mout
U640
AND_4
U641
AND
Rin
U644
AND_4
U645
AND
Rout
U626
AND_4
U627
AND
PCinc
IRin
U642
AND_4
U643
AND
A/S
U646
AND_4
U647
AND
C_ALU
CMPout
CMPin
U652
AND_4
A_ALU
B_ALU
ALU_C
U628
AND_4
U629
AND
IRout
U630
AND_4
U631
AND
PC_MAR
U648
AND_4
IN
U632
AND_4
U633
AND
IR_PC
U650
AND_4
U651
AND
OUT



Register Selector

R1	R0	A	B	C
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	0	0	0

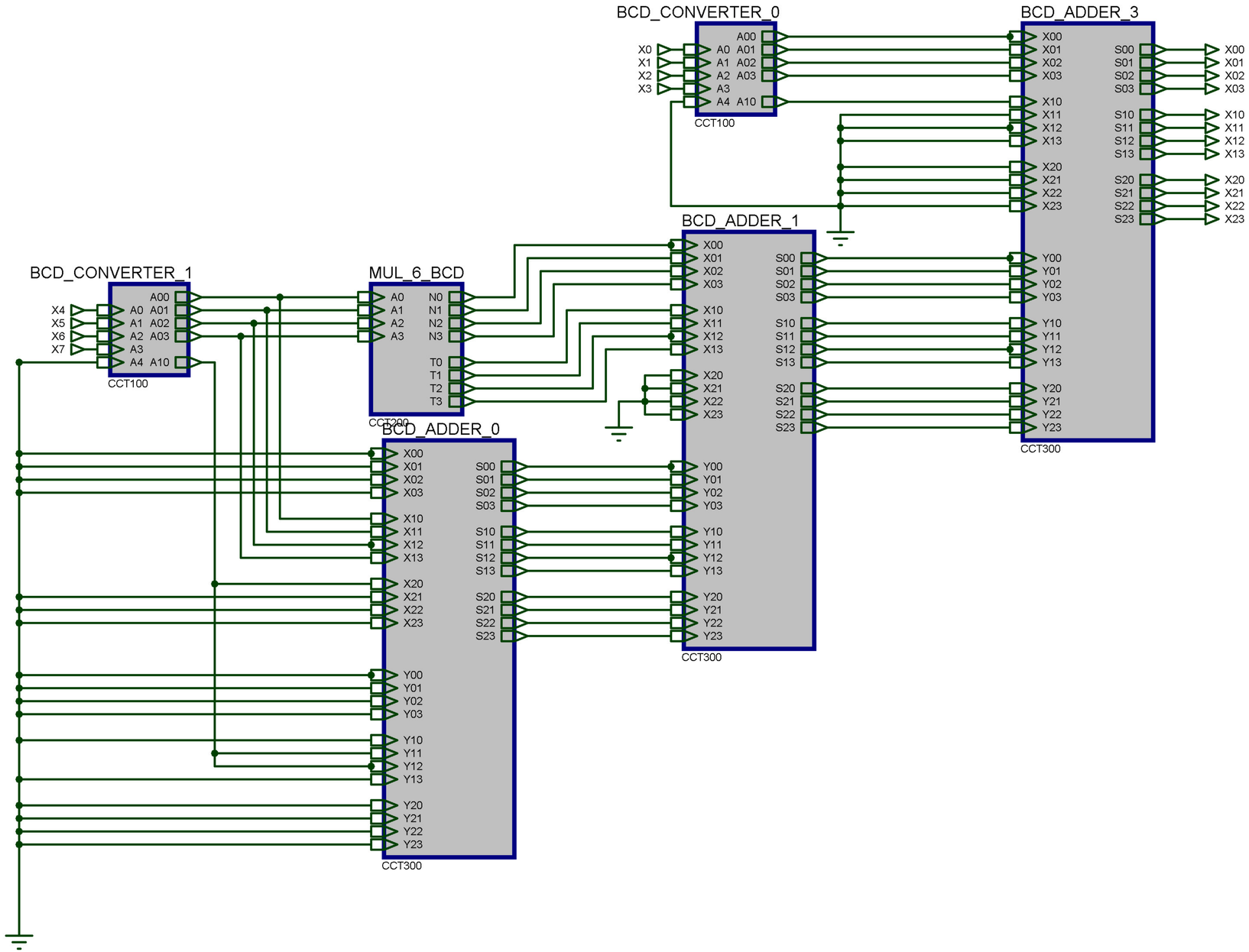
2-digit encoder



(X1X0)10 = X0*1 + X1*10
convert X0 to binary
convert X1 to binary
convert 10 to binary
do operations in binary

A3	A2	A1	A0
1	0	1	0

		A3	A2	A1	A0	0
A3	A2	A1	A0	0	0	0



8-bit BCD Decoder

$(X_{0\text{-}7})_2$ ➔ (X2 X1 X0)BCD

$(X_{0\text{-}7})_2$ ➔ $(X_{4\text{-}7}\ X_{0\text{-}3})_{16} = X_{0\text{-}3} + X_{4\text{-}7} * 16$

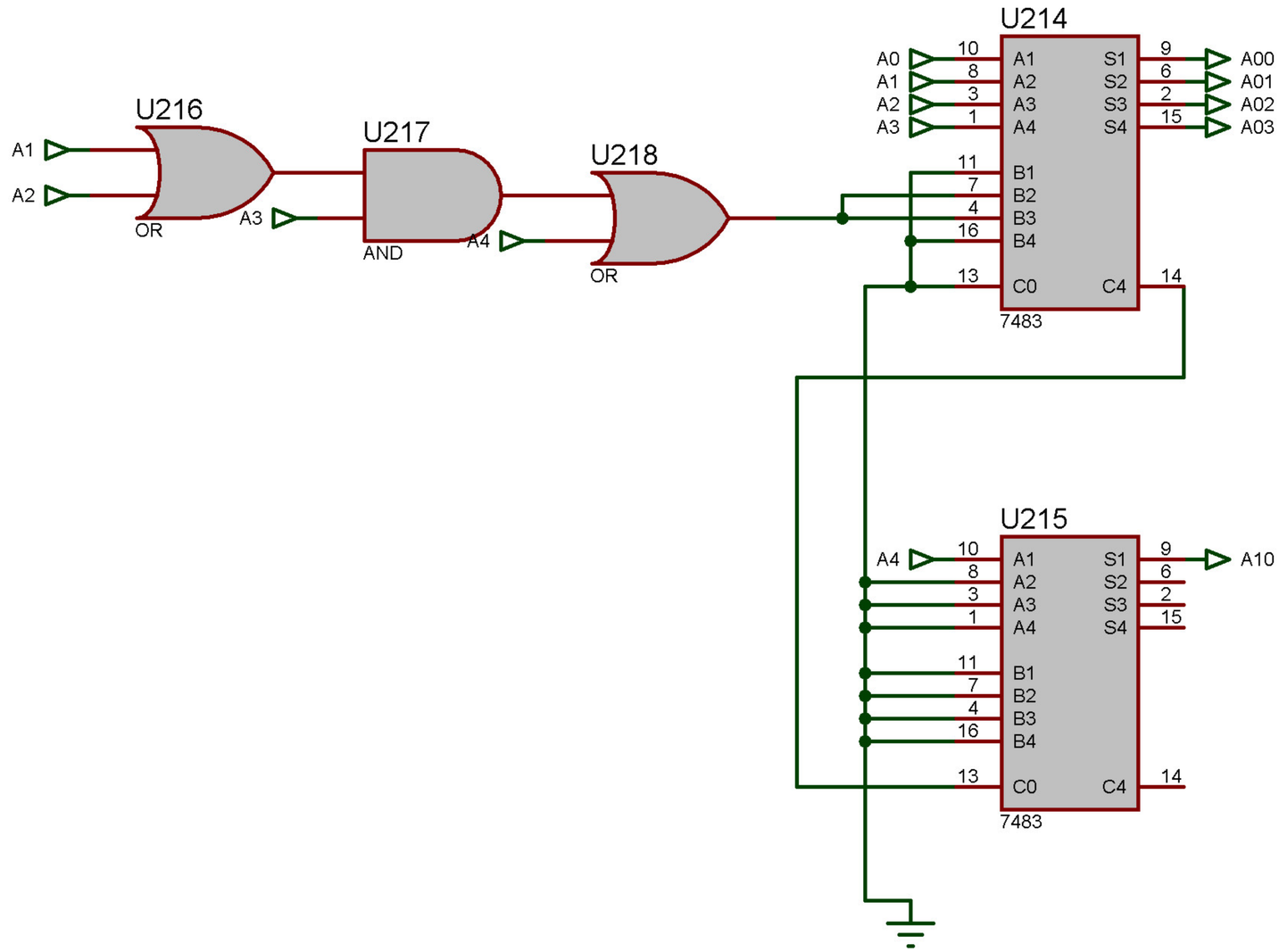
$X_{4\text{-}7}$ (BCD) * 16 (BCD)

A1 A0 * 16 = A1A0*10 + A1A0*6

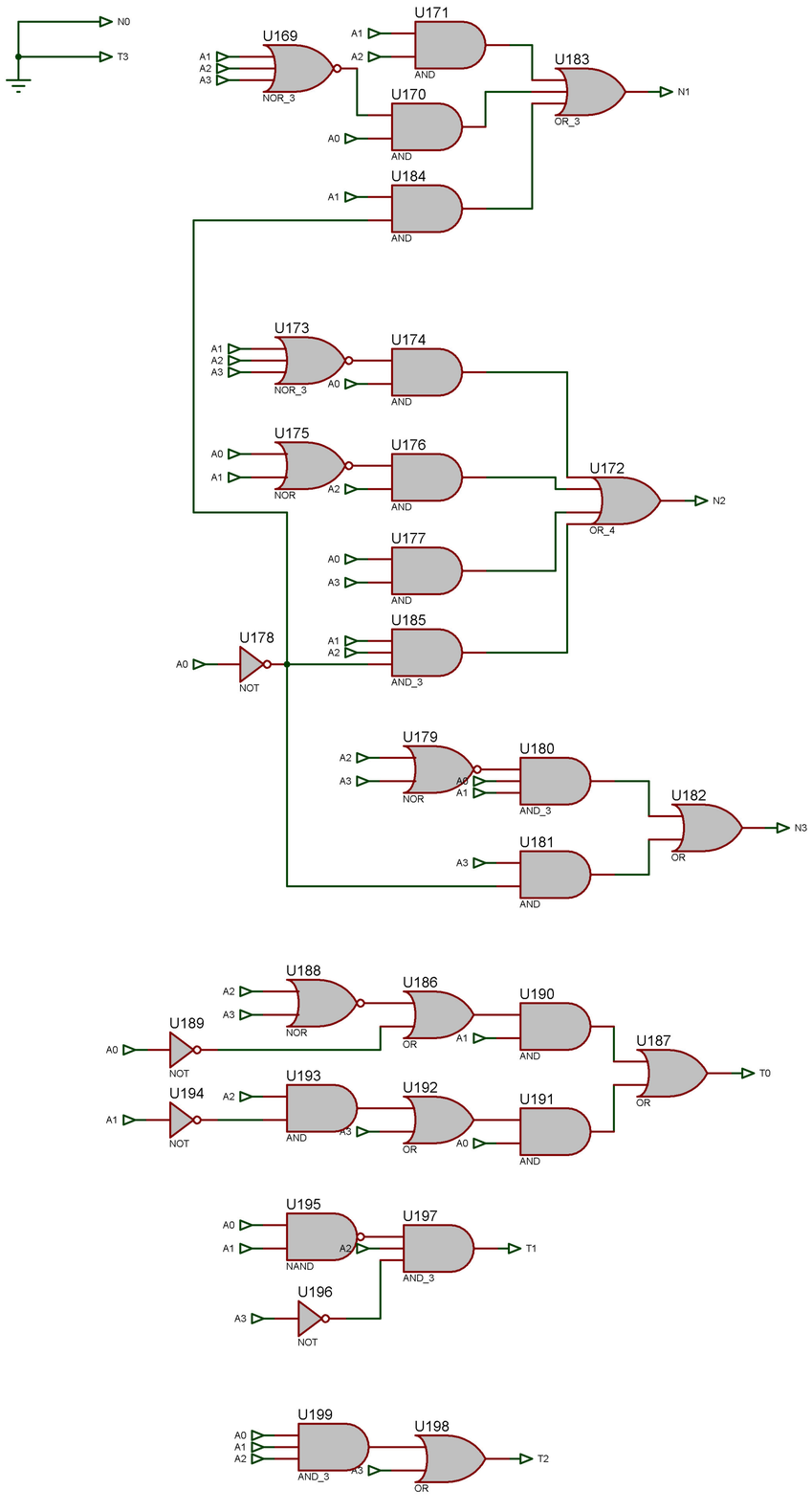
A1 A0 * 10 = (A1A0) 0

A1 A0 * 6 = (A0*6) + (A1*6) 0 = B1B0 + C1C0 0

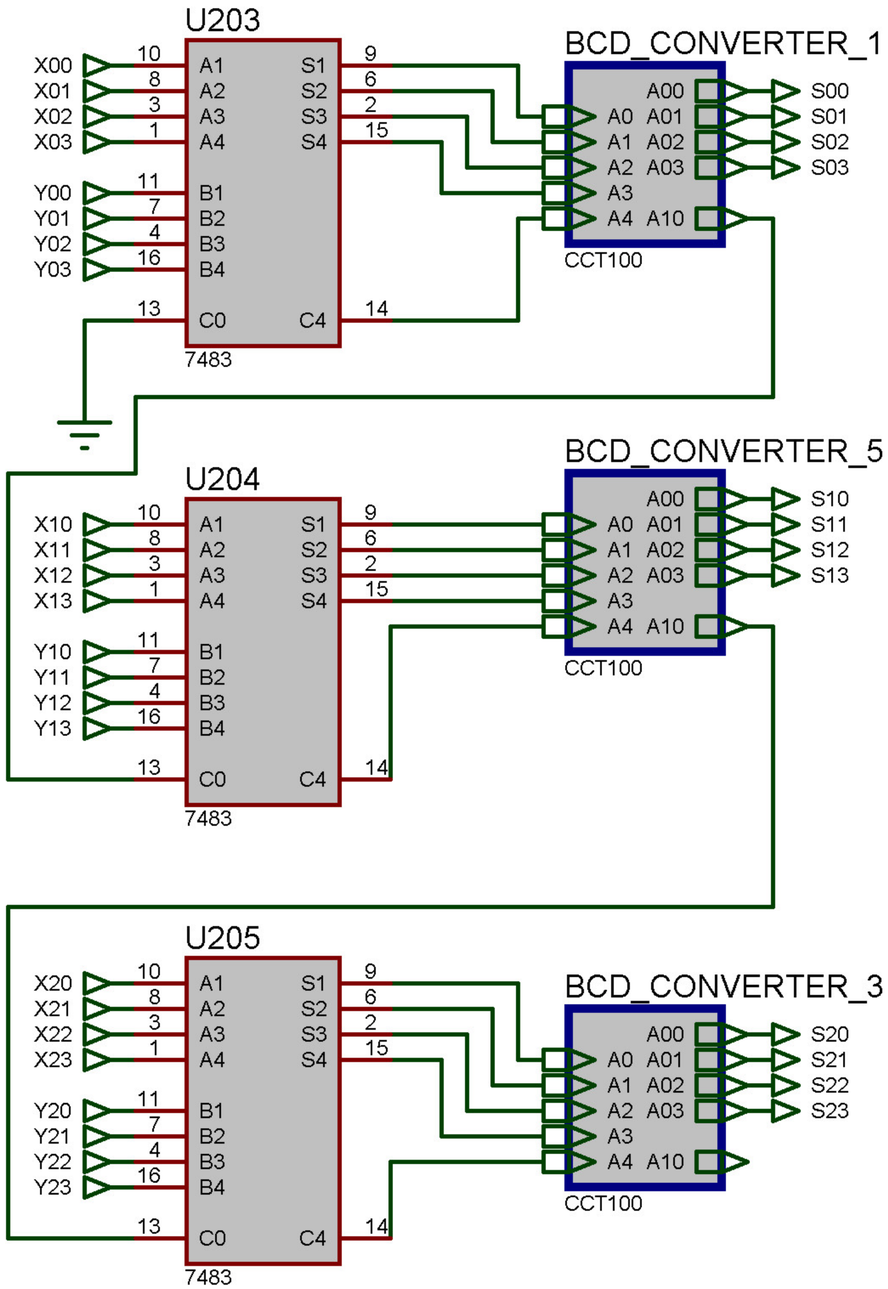
5-bit To BCD

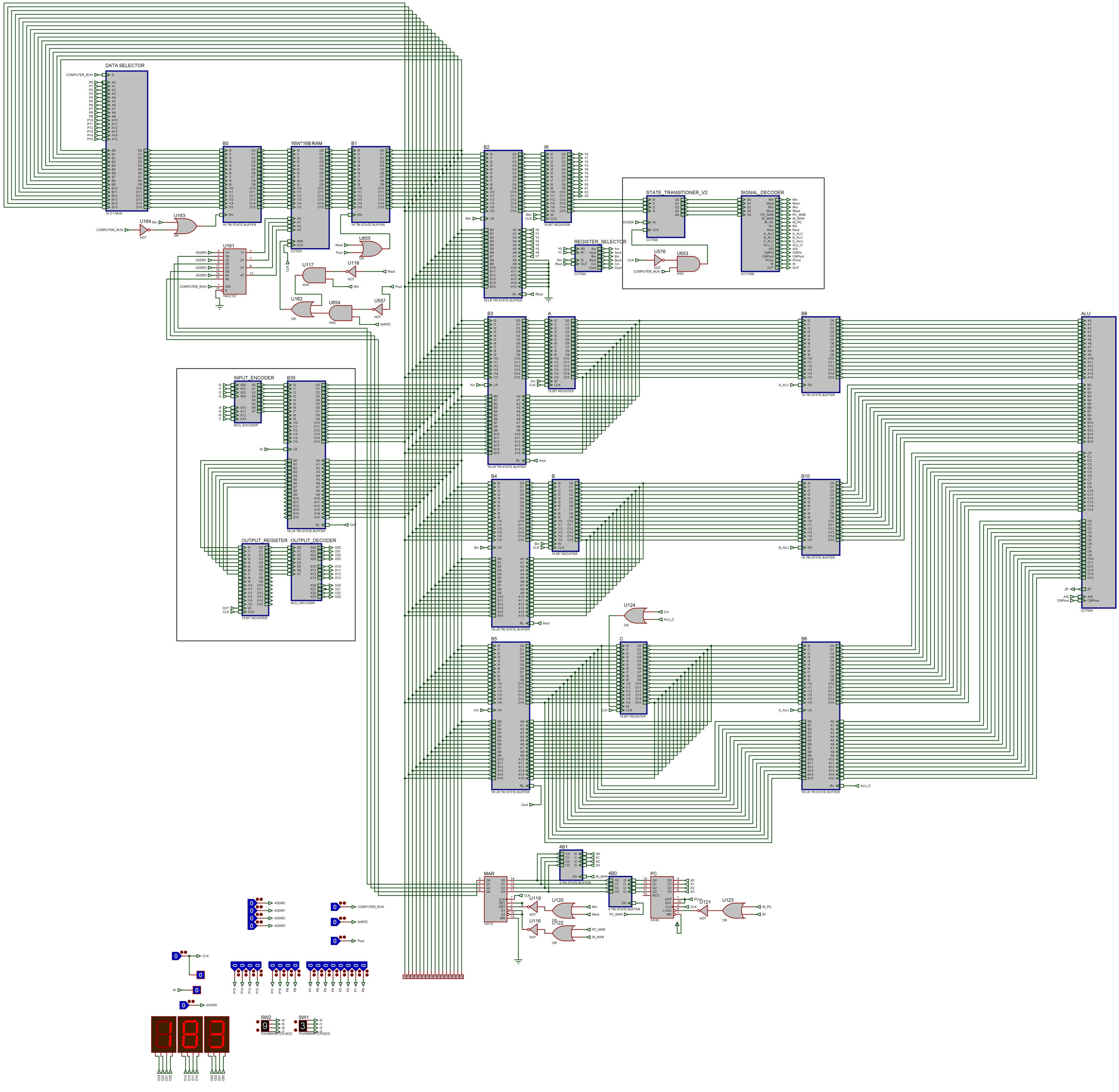

U216
A1
A2
OR
A3
U217
AND
A4
U218
OR
U214
A0
A1
A2
A3
10
8
3
1
A1
A2
A3
A4
11
7
4
16
B1
B2
B3
B4
13
C0
C4
14
S1
S2
S3
S4
9
6
2
15
A00
A01
A02
A03
7483
U215
A4
10
8
3
1
A1
A2
A3
A4
11
7
4
16
B1
B2
B3
B4
13
C0
C4
14
S1
S2
S3
S4
9
6
2
15
A10
7483

multiply by 6 BCD



BCD Adder


U203
7483
X00
X01
X02
X03
Y00
Y01
Y02
Y03
A1
A2
A3
A4
B1
B2
B3
B4
C0
C4
S1
S2
S3
S4
BCD_CONVERTER_1
CCT100
A0
A1
A2
A3
A4
A00
A01
A02
A03
A10
S00
S01
S02
S03
U204
7483
X10
X11
X12
X13
Y10
Y11
Y12
Y13
BCD_CONVERTER_5
CCT100
S10
S11
S12
S13
U205
7483
X20
X21
X22
X23
Y20
Y21
Y22
Y23
BCD_CONVERTER_3
CCT100
S20
S21
S22
S23


DATA SELECTOR
16 2-1 MUX
B0
16 TRI STATE BUFFER
16W*16B RAM
CCT001
B1
16 TRI STATE BUFFER
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U161
74HC157
U163
U164
U655
U117
U118
U162
U654
U557
U576
U653
B3
16 LR TRI STATE BUFFER
A
16 BIT REGISTER
B8
16 TRI STATE BUFFER
ALU
CCT004
INPUT_ENCODER
BCD_ENCODER
B30
16 LR TRI STATE BUFFER
OUTPUT_REGISTER
16 BIT REGISTER
OUTPUT_DECODER
BCD_DECODER
B4
16 LR TRI STATE BUFFER
B
16 BIT REGISTER
B10
16 TRI STATE BUFFER
U124
B5
16 LR TRI STATE BUFFER
C
16 BIT REGISTER
B6
16 LR TRI STATE BUFFER
4B1
4 TRI STATE BUFFER
MAR
74173
4B0
4 TRI STATE BUFFER
PC
74161
U119
U120
U116
U122
U121
U123
ADDR0
ADDR1
ADDR2
ADDR3
COMPUTER_RUN
WRITE
Pout
CLK
IN
ENTER
SW2
THUMBSWITCH-BCD
SW1
THUMBSWITCH-BCD