CS302 Project 1

5-Bit Binary Adder with 7-Segment Display Control

Project Team 33

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Abstract

This project implements a 5-bit binary adder system that performs addition on two 5-bit binary numbers.

The results are displayed using a 7-segment display, and the system supports a control bit to switch

between decimal and hexadecimal representations for the inputs and outputs.

Problem Definition

The main objective of the project is to:

• Add two 5-bit binary numbers.

• Display the operands and result on a 7-segment display.

• Integrate a control unit for toggling between decimal and hexadecimal representation.

System Architecture

The system comprises the following components:

- **5-bit Adder:** A modular circuit constructed using full adders, designed to handle 5-bit operands and produce a 6-bit output (including carry).

- **7-Segment Display:** Individual segments (A-G) designed and combined into a master circuit to display binary-to-decimal or binary-to-hexadecimal conversions.

- **Control Unit:** Enables switching between decimal and hexadecimal displays using a single control bit.

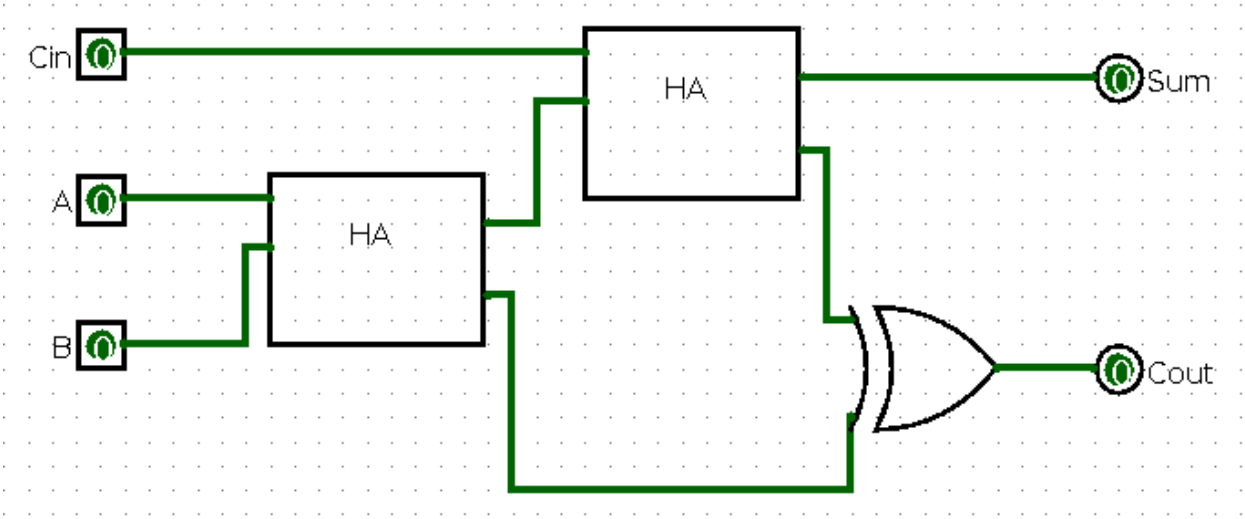
- **6x64 Decoder:** A 6x64 decoder maps the inputs to the appropriate segments of the display.

Implementation

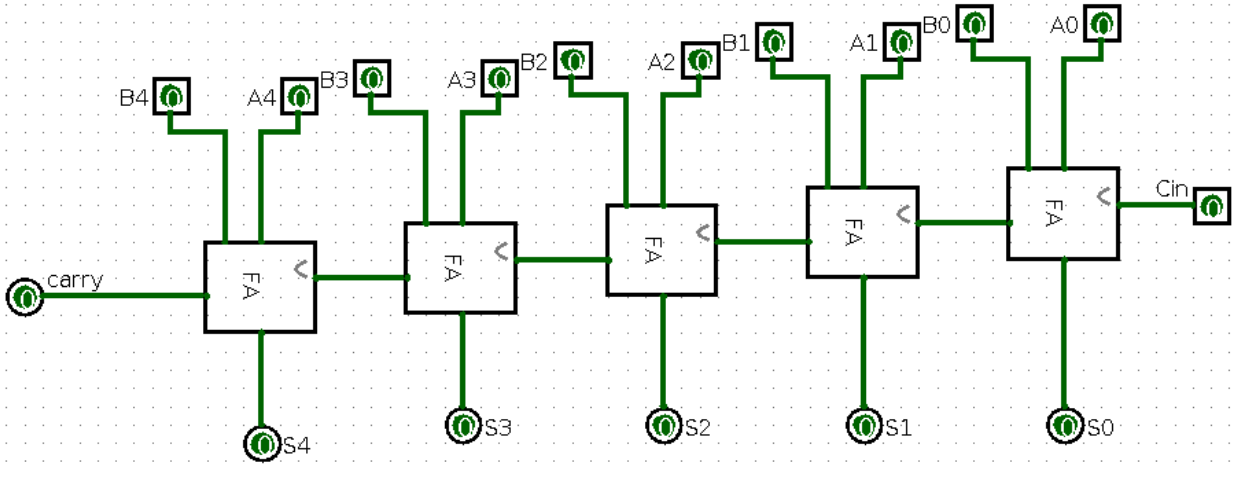
3.1 - 5 bit Adder Circuit

The 5-bit adder was implemented using:

- Half Adders (HA): Used for the least significant bit addition.
- Full Adders (FA): Used for the remaining bits to propagate carry.
- The final output is a 6-bit result, where the extra bit represents the carry-out from the addition.



Full Adder using 2 Half Adder

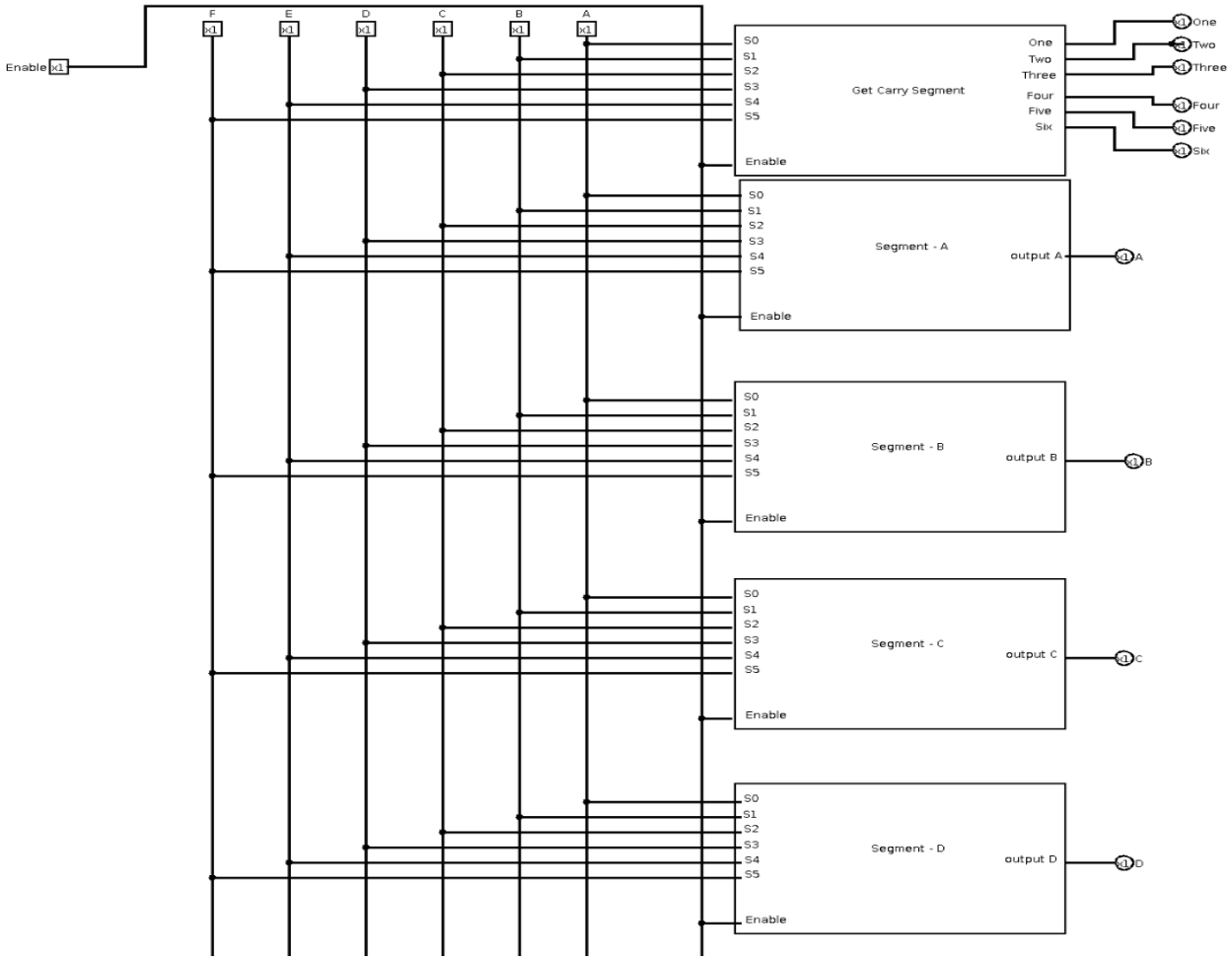


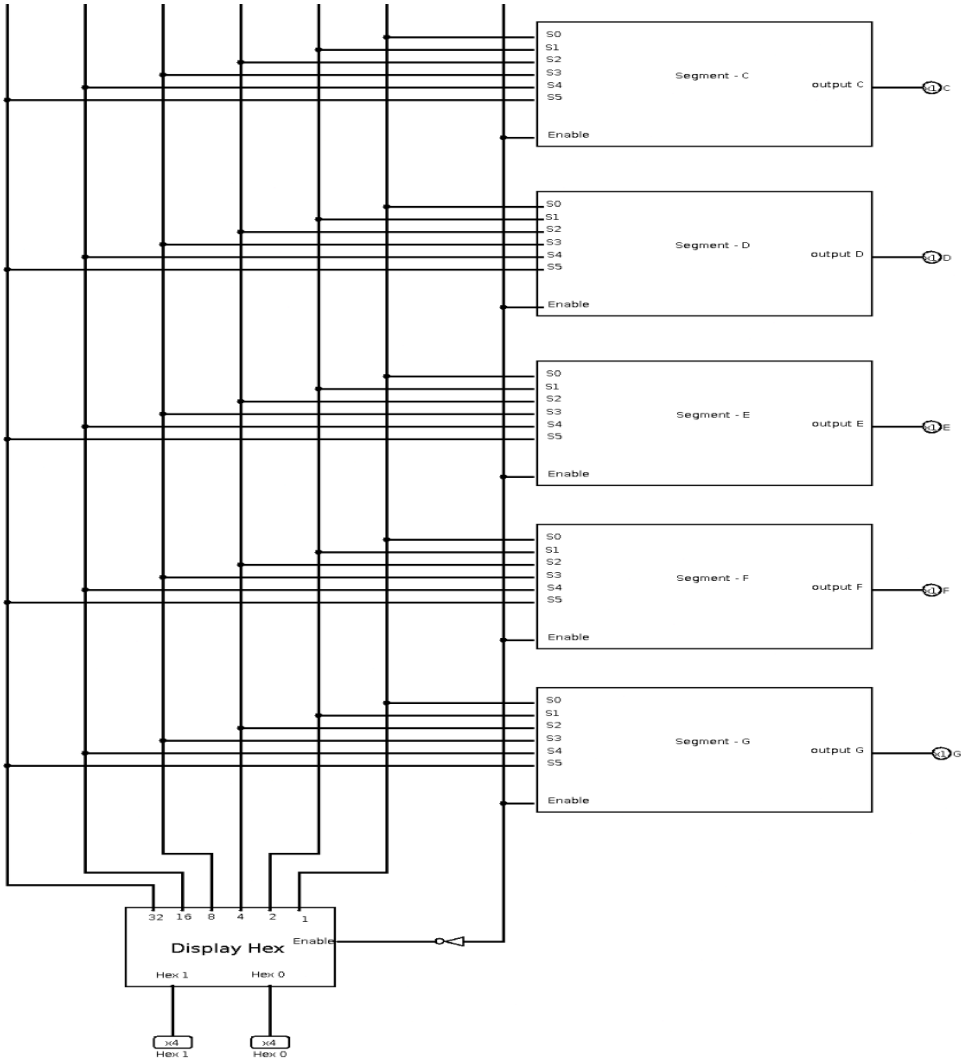
5 bit Adder using 4 Full Adder

3.2 - 7-Segment Display

The display system was designed with the following approach:

- A separate circuit for each segment (A-G).
- OR gates used to combine the output of the 6X64 decoder for each segment.
- Each segment is then combined into a master display system.





3.3 - Control Unit

The control unit uses enables to:

- Select between binary-to-decimal and binary-to-hexadecimal conversions.
- Enable or disable specific outputs on the 7-segment display.
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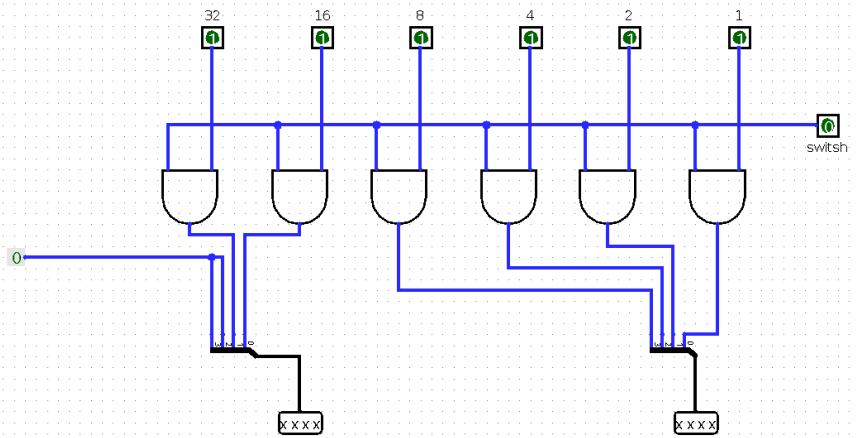


Challenges Faced

- **Keymap for 6 inputs:**
  Limited resources for keymap designs for 6-bit so decoders required using OR gates for manual mapping.

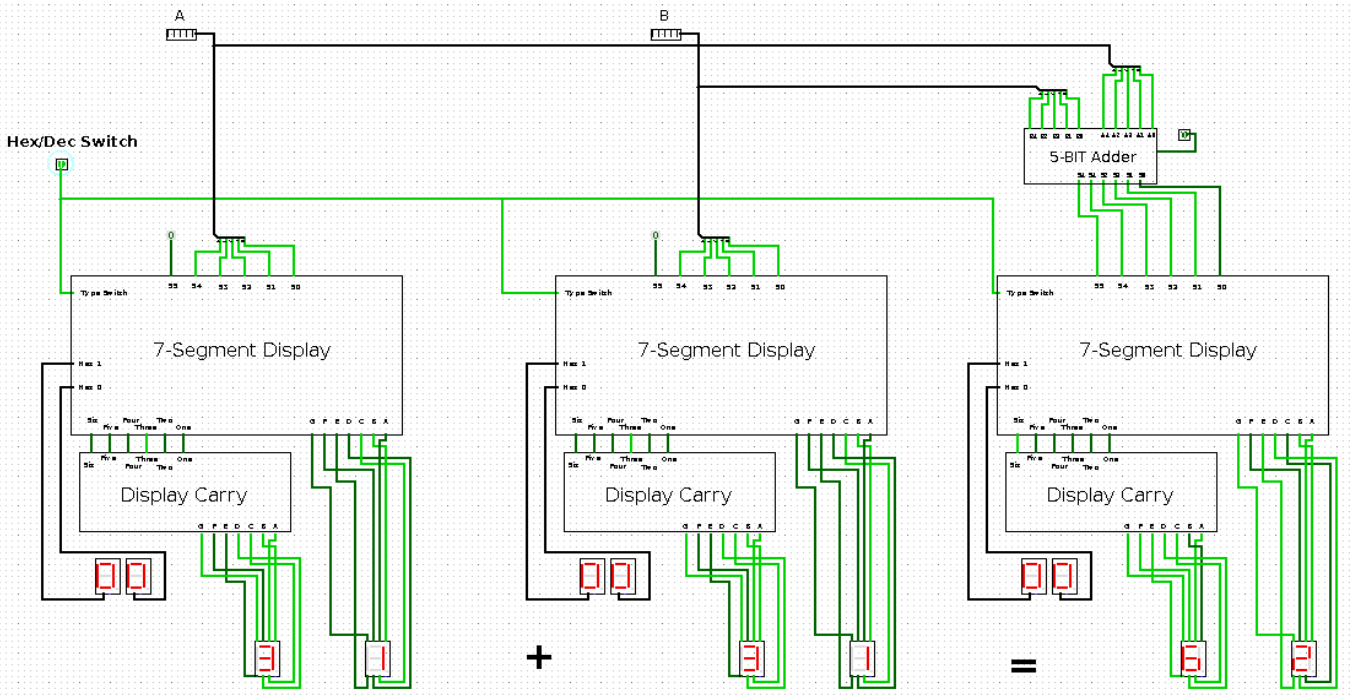
- **6X64 Decoder not exist by default in Logism:**
  The absence of a built-in 6x64 decoder in Logisim necessitated designing a custom decoder circuit. This was achieved by combining smaller decoders (e.g., 3x8 decoders) and using additional logic gates to manage outputs effectively.

- **Complexity of 7-Segment Design:**
  Mapping the outputs of the decoder to individual segments (A-G) involved extensive testing to ensure correct representation of numbers in both decimal and hexadecimal formats.

Results

The project successfully achieves the following:

- ☑ Accurate addition of 5-bit binary numbers.
- ☑ Display of inputs and results in both decimal and hexadecimal formats.
- ☑ Seamless switching using the control unit.



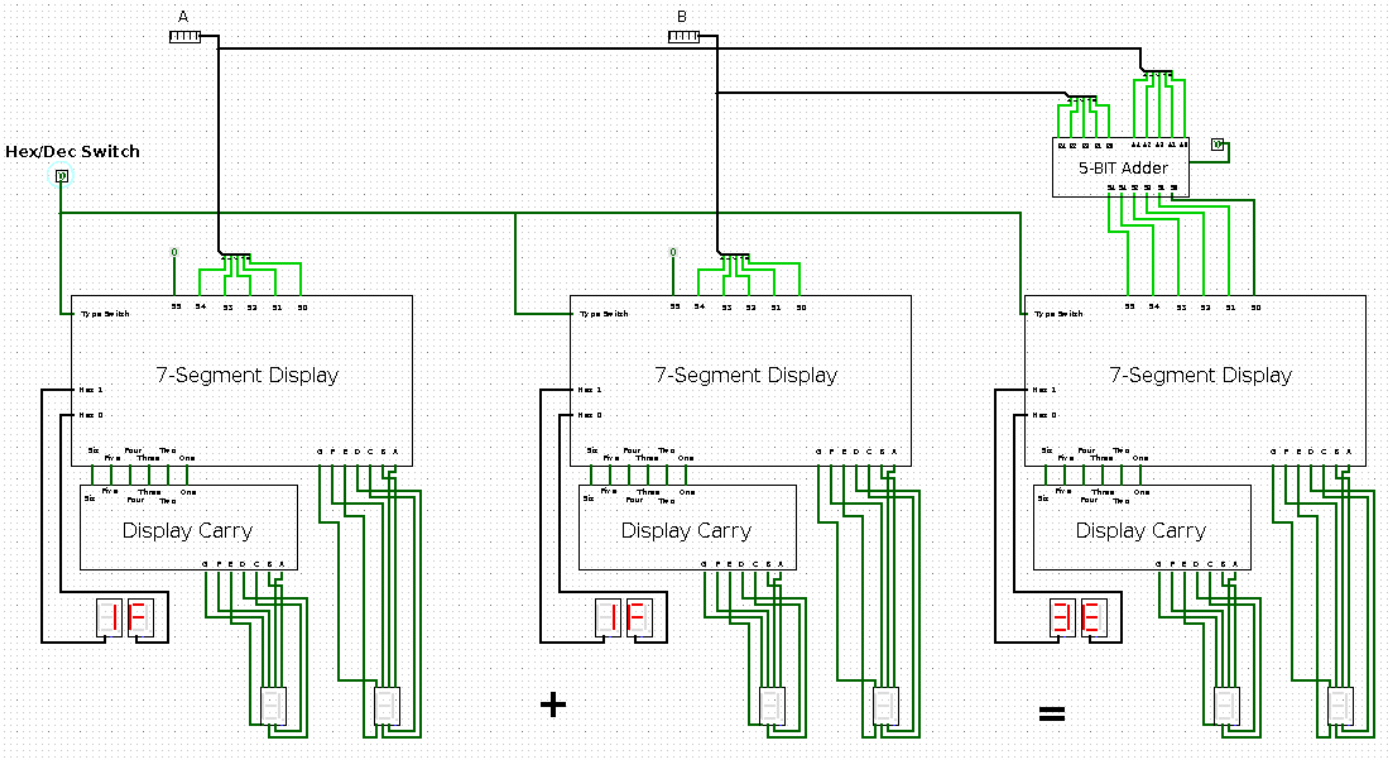


Figure 5: Overview of the main circuit in dec and hex

Conclusion

This project demonstrates the effective use of Logisim for designing and simulating digital systems.

The modular approach ensures scalability and clarity, while the added functionality of a control unit enhances usability.

and thank you for your time.
Project Team 33 ❤️.