40dB Analogue Amplifier

Moustafa Elneanaey

13001577

TABLE OF CONTENTS

I. INTRODUCTION

The purpose of this report is to present the design and implementation of a multi-stage amplifier using the **2N3904 NPN transistor**. The 2N3904 is a widely used general-purpose transistor known for its availability, reliability, and decent gain characteristics. In a common emitter configuration, a single 2N3904 transistor typically provides a voltage gain ($\mathbf{A_v}$) of approximately **38 dB**, which, while substantial, is insufficient for applications requiring higher amplification levels.

To achieve a total gain exceeding **40 dB**, a **two-stage amplifier** configuration was implemented. Each of the first two stages provides voltage gain, with careful attention to biasing and capacitor selection to maintain signal integrity and frequency response. Additionally, a **third stage** was added, configured as a **common-collector (emitter follower)**. This final stage does not contribute to voltage gain but serves a critical role as a **buffer**, lowering output impedance and improving the amplifier's ability to drive a load without distortion.

This report details the circuit design, component selection, simulation results, and frequency response analysis, highlighting the effectiveness of cascading stages to achieve the desired amplification while ensuring overall circuit stability.

II. METHODOLOGY

A. Simulation

The simulation and analysis of the amplifier circuit were carried out using **LTspice**, a widely used electronic circuit simulation software. The design consisted of three stages: two cascaded **common-emitter amplifiers** for voltage gain and a final **common-collector (emitter follower)** stage for output buffering and impedance matching. The input signal is coming from a **CMA-4544PF-W mic** with a resistance of **2.2KΩ** which is modelled in the circuit as **R9**. The load is a speaker with a typical resistance of **8Ω,** but this can be swapped for a larger resistance in case of using an **ADC**.

Capacitor values were selected for the decoupling, bypassing and isolation high enough in order to shift the roll off frequency towards the lower band without the need to increase the resistor values and more importantly due to availability at the time of conducting the experiment.

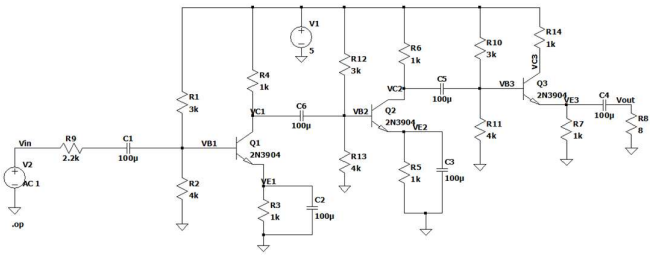
Resistor values are selected for biasing. With **potential divider bias** having a larger value (4KΩ) at the bottom than at the top (3KΩ) to allow a larger current value (IB) to flow into the transistor in comparison to if they were connected the other way around.

To ensure that all transistors (2N3904 NPN BJTs) operate in their **active (forward-biased) region**, a **DC operating point analysis** was first performed. This step allowed for checking the **base-emitter voltages (VBE)** and **collector-emitter voltages (VCE)** to confirm that each transistor was properly biased and not in saturation or cutoff. Voltages at key nodes (base, collector, emitter) were observed to ensure that for each transistor:

- VBE ≈ 0.65−0.85 V

- VCE > 0.2-0.3 V

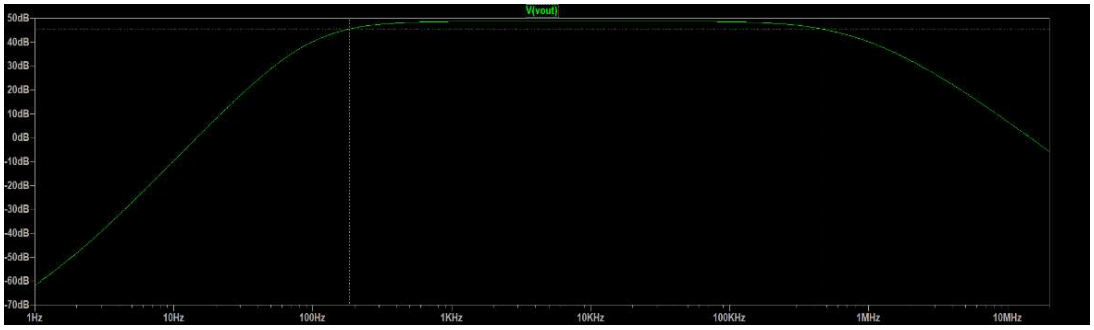
```
--- Operating Point ---

V(vb1):         2.84472         voltage
V(n001):        5               voltage
V(n002):        6.25839e-13     voltage
V(vc2):         2.83809         voltage
V(vc3):         2.83809         voltage
V(ve3):         2.16916         voltage
V(vout):        1.73533e-15     voltage
V(vc1):         2.83809         voltage
V(ve1):         2.16916         voltage
V(vin):         0               voltage
V(vb2):         2.84472         voltage
V(ve2):         2.16916         voltage
V(vb3):         2.84472         voltage
```



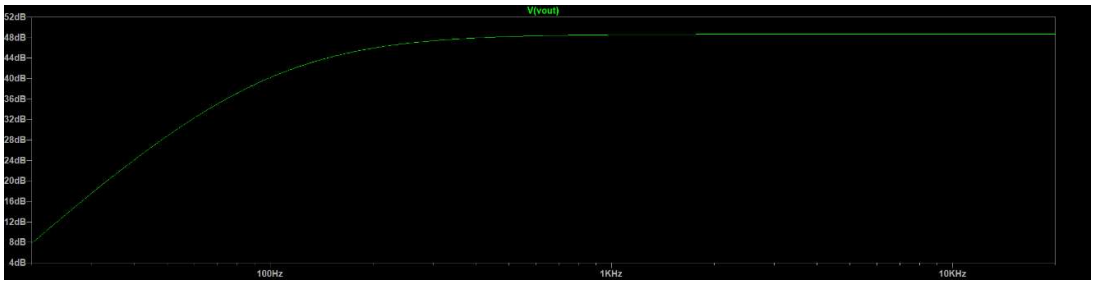
A VB ≈ 2.84V, VE ≈ 2.17V, and VC ≈ 2.84V were observed and so VBE ≈ 0.67V and VCE ≈ 0.67V, consequently all three transistors are forward biased. It is worth nothing that all three transistors have almost equal terminal voltages, but this is thanks to the capacitors (C6 and C5) isolating each transistor, (C1 and C4) decoupling DC and AC signals, and the resistor values used for biasing in the base, emitter and collector are the same for the three transistors.

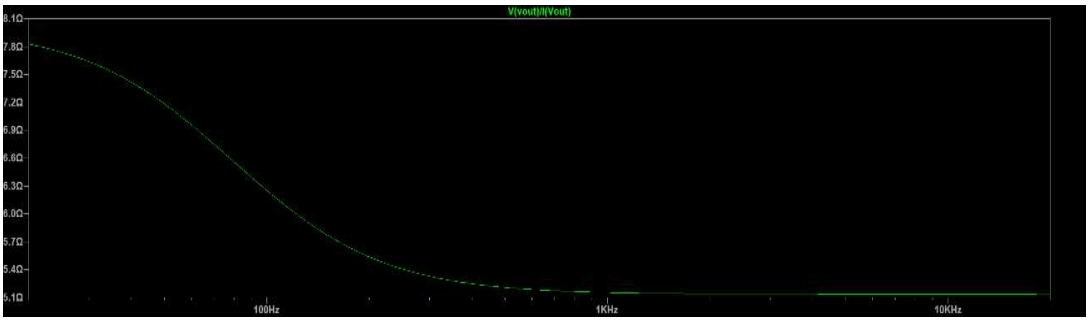
Once proper DC biasing was verified, an **AC analysis** was conducted to determine the frequency response of the amplifier. The simulation was set up using an .ac dec directive to sweep the frequency logarithmically from **1 Hz to 20 MHz.** Although the full frequency sweep was simulated, the focus of this analysis is the **audio frequency range** from **20 Hz to 20 kHz**, which is relevant for typical sound signal amplification.

In the AC simulation, a small signal (1 V AC) was applied at the input, and the gain was observed at the output using the waveform viewer. Additional AC current probes were used to calculate the input impedance and observe the frequency-dependent behavior of the circuit. Key parameters such as **gain (in dB)**, and **bandwidth** were analyzed in this range to evaluate the amplifier's performance for audio applications.

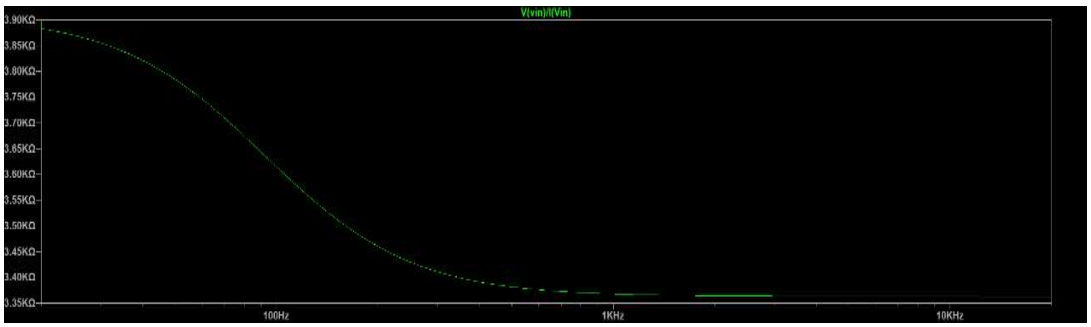


A maximum gain of **48.67 dB** was observed in the mid band with roll off starting at about **200Hz** and **440kHz** effectively giving a bandwidth of **439780Hz**.





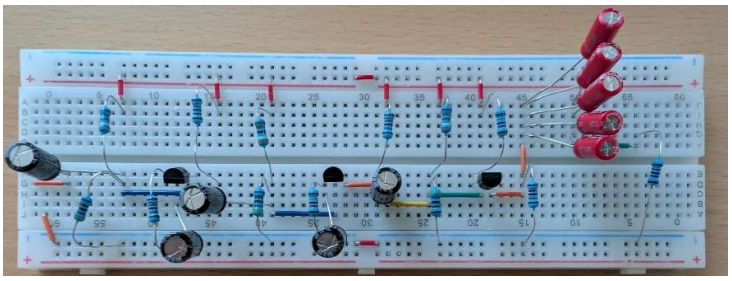
Although the amplifier's intended bandwidth was **20 Hz to 20 kHz**, the measured performance shows effective operation only from **200 Hz to 20 kHz**. While this means the amplifier **attenuates** lower frequencies below **200 Hz**, the impact on practical use is minimal for most audio applications. The human ear is less sensitive to very low frequencies, and much of the important information in music, speech, and general-purpose signals lies above 200 Hz. Additionally, sub-



200 Hz content often requires large speaker systems or specialized subwoofers to reproduce effectively, which may not be relevant for the intended use of this amplifier. Therefore, the loss of response below 200 Hz is not considered critical for the overall performance in typical use cases.

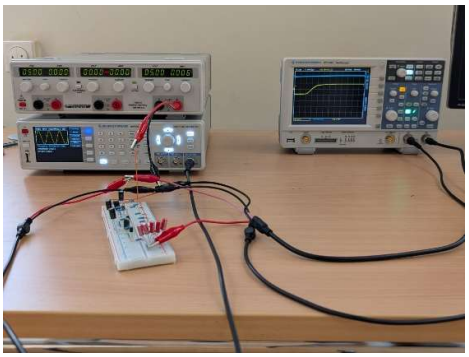
The **input resistance** as can be seen from the figure above settles at about **3.35KΩ** (considerably high) and **output resistance** around **5.1 Ω** (very low) which are good characteristics of an amplifier. It should be noted that we can add series a resistance after C1 to increase the input resistance however this will cause a dip in the gain.

B. Implementation

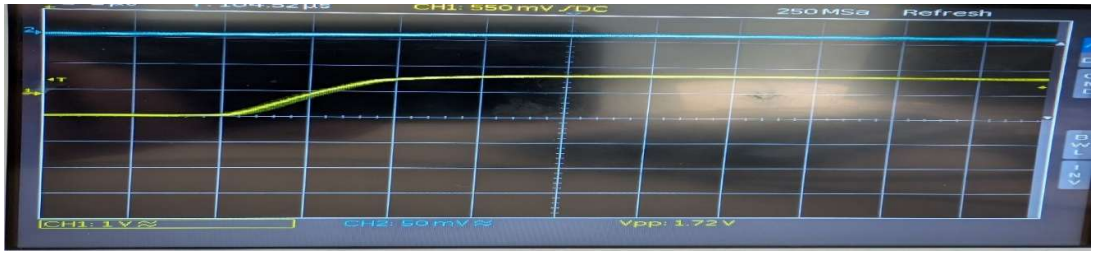


Due to limitations on the availability of the capacitors, the last capacitor (C4) was swapped with 5 parallel 1uF capacitors to give an equivalent 5uF capacitor. While this change is not expected to change the maximum gain achieved, it will certainly cause the gain of the lower frequency to suffer (as roll off will start quicker).

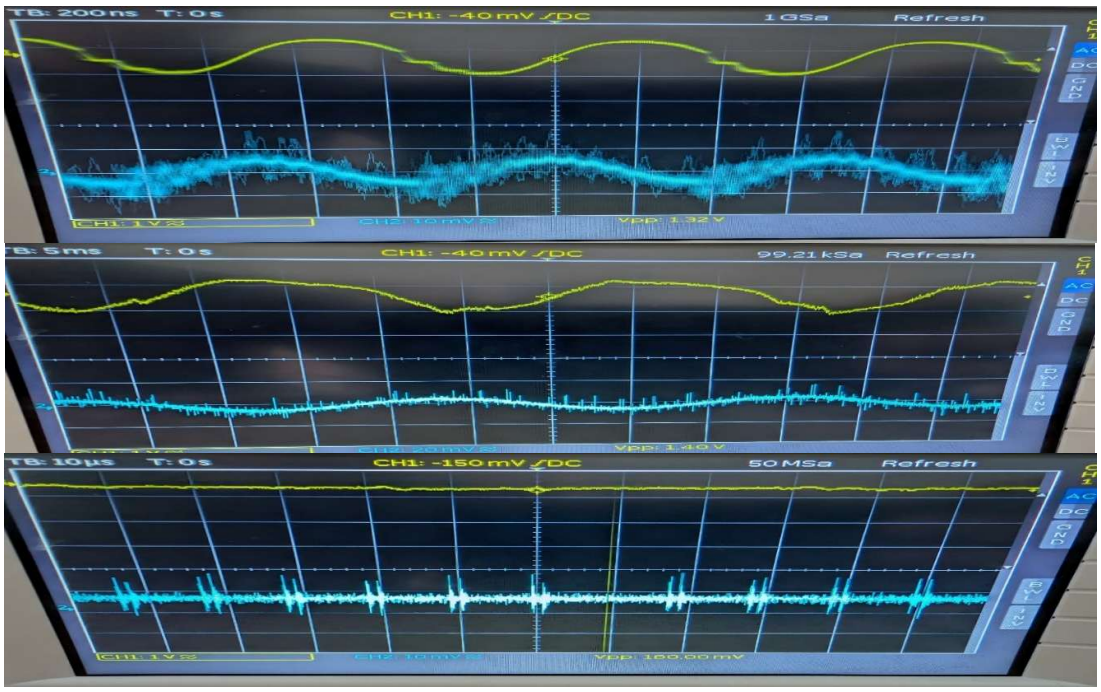
Due to the mic being faulty, the mic was replaced with a sinusoidal input from the HMF2525 signal generator with a series resistance of 2KΩ in order to model the output resistance of the mic. The output was observed on the RTC1002 oscilloscope with channel 1 and channel 2 measuring Vout and Vin respectively. Gain was observed at different input frequencies, however, with the same input voltage amplitude of 10mV. It is also worth noting that simulation was redone, although not shown here, with 5uf capacitance and 1kΩ resistance at the output terminal.



At 20 kHz, Vout was observed to be about 1.6V giving a gain of around 45.6 dB which gives a lower 3 dB gain compared to the simulation results. The same gain was observed for values between 2kHz and 1MHz.



The gain dropped at 1.4 MHz to 43.6 dB (cut off frequency) which shows how the change from 100uF to 5uf capacitance at the output node shifted the midband to the right strongly. But this change also worsened the gain drastically for at 20Hz. While the output at extremely low frequencies became attenuated, the lower cutoff frequency surprisingly improved, reaching 50Hz, and so the bandwidth increased drastically. The figures below show the voltage at 1.4MHz, 50Hz and 20Hz, respectively.



III Discussion

The results of the simulation and implementation highlight the effectiveness of the three-stage amplifier design in achieving high voltage gain, with some discrepancies between theoretical and practical performance. It is also worth noting that the output signal had a lot of abrupt changes but as seen from the input channel, the input signal itself had a lot of noise which may be one of the reasons for such an observation. The deviations and discrepancies between theoretical and practical results are attributed to several sources of error and real-world constraints:

1. Sources of Error

a. Component Tolerances

Resistors and capacitors used in the implementation have tolerances (e.g., ±5% or ±10%), which affect bias points and frequency response. In simulation, ideal components are assumed, but in reality, variations can significantly shift operating points or gain.

b. Capacitor Substitution

Due to limited availability, the 5 µF output coupling capacitor (C4) was constructed from five parallel 1 µF capacitors. This substitution introduces parasitic inductance and resistance, which can affect high-frequency response and contribute to distortion or reduced gain.

c. Faulty Microphone Replacement

The original CMA-4544PF-W microphone was replaced with a signal generator and resistor. While this substitution approximates the mic's output resistance, it does not replicate the mic's frequency response or noise characteristics, potentially leading to gain or frequency response differences.

d. Breadboard Parasitics

Since the implementation was done on a breadboard, stray capacitance and inductance could significantly affect high-frequency operation and stability. These effects are not present in simulation environments like LTspice.

e. Measurement Inaccuracies

Measurement with an oscilloscope can introduce small errors, especially in low-amplitude signals or high-frequency signals where probe compensation or bandwidth limitations come into play.

2. Possible Improvements and Fixes

a. Use Precise Components

To reduce tolerance-related variability, resistors with 1% tolerance and capacitors with tighter specifications should be used. This would make the experimental performance closer to simulation results.

b. Redesign for Better Low-Frequency Response

Simulations showed lower gain below 200 Hz. If low-frequency audio signals are important (e.g., for full-range speakers), the circuit can be optimized for lower roll-off by increasing capacitor values or adjusting emitter resistor bypassing.

c. PCB Implementation

Moving from a breadboard to a printed circuit board (PCB) can drastically improve performance by minimizing parasitic elements, improving stability, and allowing better grounding and layout optimization.

3. Future Considerations

Thermal Effects: Changes in ambient temperature may affect transistor parameters like β and VBE. Using temperature-compensating circuits or designing for thermal stability could improve robustness.

Power Supply Noise: A poorly filtered or unstable power supply could introduce noise into the amplifier. Using a regulated power supply and adding decoupling capacitors (e.g., 100 nF ceramic + 100 µF electrolytic) near each transistor stage could reduce noise.

Load Matching: The amplifier was designed to drive an 8 Ω speaker. If connected to a different load (e.g., ADC input), impedance matching should be considered for maximum signal transfer and minimal distortion.

4. Conclusion of Discussion

The three-stage amplifier achieves a high gain suitable for audio applications, and the simulation closely matches practical results, with deviations due to real-world imperfections. While some low-frequency performance was compromised due to capacitor limitations, the core design performs effectively within the mid-band audio range. With further refinements in component selection, layout, and biasing strategy, performance can be enhanced for more demanding applications.