Freescale Semiconductor
Application Note

Document Number: AN3940
Rev. 6, 11/2013

Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces

This document provides general hardware and layout considerations and guidelines for hardware engineers implementing a DDR3 memory subsystem.

The rules and recommendations inthis document serve as an initial baseline for board designers to begin their specific implementations, such as fly-by memory topology.

CAUTION

It is strongly recommended that the board designer verifies that all aspects, such as signal integrity, electrical timings, and so on, are addressed by using simulation models before board fabrication.

Contents

1 DDR3 designer checklist

Table 1. DDR3 designer checklist

No.	Task	Completed?
	Simulation	
1.	Ensure that optimal termination values, signal topology, and trace are lengths determined through simulation for each signal group in the memory implementation. The unique signal groups are as follows: • **Data group:** MDQS(8:0), $\overline{\text{MDQS}}$(8:0), MDM(8:0), MDQ(63:0), MECC(7:0) **Note:** In T4xxx processors, the MDM(8:0) signals in a x4 DRAM mode are no longer available as mask signals but configured in a secondary function as MDQS(17:9) signals. Therefore the full Data Group for T4xxx processors is: MDQS(17:0), MDQS(17:0), MDQ(63:0), MECC(7:0) • **Address/CMD group:** MBA(2:0), MA(15:0), $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MWE}}$ • **Control group:** $\overline{\text{MCS}}$(3:0), MCKE(3:0), MODT(3:0) • **Clock group:** MCK(5:0) and $\overline{\text{MCK}}$(5:0) **Note:** 28nm processors only have MCK(3:0) and $\overline{\text{MCK}}$(3:0) **Note:** These groupings assume a full, 72-bit data implementation (64-bit + 8 bits of ECC). Some products may only implement 32-bit data and may choose to have fewer $\overline{\text{MCS}}$, MCKE, and MODT signals. Some products support the optional MAPAR_OUT and $\overline{\text{MAPAR\_ERR}}$ for registered DIMMs. In such cases, treat MAPAR_OUT as part of the ADDR/CMD group and $\overline{\text{MAPAR\_ERR}}$ as an asynchronous signal. **Note:** If on-die termination is used at both the memories and the controller, no additional termination is required for the data group.	
2.	Ensure to consider the following 3 points in read timing budget simulation: • No Slew Rate Derating should be done for the FSL DDR3 controllers on reads (i.e. DDR3 Inputs (DQS/DQ) to the FSL DDR3 controllers do not need to be derated per JESD79-3E) • Timing budgets for reads can be done with customer's simulation tool by adding the setup and hold margins rather than looking at the setup or hold margins by themselves (to account for the DQS-DQ calibration) • Read timing should be taken at Vref rather than Vin levels. (i.e. ALL read timing measurements for DQ shall be taken at Vref. No read timing measurements are taken at Vih(ac), Vil(ac), Vih(dc), or Vil(dc)) Ensure the selected termination scheme meets the AC signaling parameters (voltage levels, slew rate, and overshoot/undershoot) across all memory chips in the design.	
	Termination scheme **Note:** It is assumed that the designer is using the mainstream termination approach as found in commodity PC motherboards. Specifically, it is assumed that on-die termination is used for the data groups and that external parallel resistors tied to VTT are used for the address/CMD and control groups. **Note:** Different termination techniques may also prove valid and useful, but are left to the designer to validate through simulation.	
3.	Ensure the worst-case power dissipation for the termination resistors are within the manufacturer's rating for the selected devices. See Section 2, “Selecting termination resistors.”	
4.	***Note:*** *This task is not applicable if the ODT feature is used.* If resistor packs are used, ensure that data lanes are isolated from the other DDR3 signal groups. **Note:** Because on-die termination is the preferred method for DDR3 data signals, external resistors for the data group are not required.	

Table 1. DDR3 designer checklist (continued)

No.	Task	Completed?
5.	Ensure the V_{TT} resistors are properly placed by tying the R_T terminators into the V_{TT} island at the end of the memory bus.	
6.	Ensure the differential terminator is present on the clock lines for discrete memory populations (the DIMM modules contain this terminator).	
	V_{TT} related items	
7.	Ensure the worst-case current for the V_{TT} plane is calculated based on the design termination scheme. See Section 2, "Selecting termination resistors."	
8	Ensure the V_{TT} regulator can support the steady state and transient current needs of the design.	
9.	Ensure the V_{TT} island is properly decoupled with high frequency decoupling: • Use at least one low ESL cap or two standard decoupling caps for each four-pack resistor network (or every four discrete resistors). • Use at least one 4.7-μF cap at each end of the V_{TT} island. **Note:** This recommendation is based on a top-layer V_{TT} surface island (lower inductance). If an internal split is used, more capacitors may be needed to handle the transient current demands.	
10.	Ensure the V_{TT} island is properly decoupled with bulk decoupling. At least one bulk cap (47–220 μF) capacitor should be at each end of the island.	
11.	• Ensure the V_{TT} island is placed at the end of the memory channel and as closely as possible to the last memory bank? • Ensure the V_{TT} regulator is placed in close proximity to the island.	
12.	Ensure a wide surface trace (~150 mils) is used for the V_{TT} island trace.	
13.	If a sense pin is present on the V_{TT} regulator, ensure that it attached in the middle of the island.	
	V_{REF}	
14.	Ensure that V_{REF} is routed with a wide trace (a minimum of 20–25 mils is recommended).	
15.	• Ensure that V_{REF} is isolated from noisy aggressors. • Maintain at least a 20–25 mils clearance from V_{REF} to other traces; if possible, isolate V_{REF} with adjacent ground traces.	
16.	Ensure that V_{REF} is properly decoupled by decoupling the source and each destination pin with 0.1 μf caps.	
17.	Ensure the V_{REF} source tracks variations in V_{DDQ}, temperature, and noise, as required by the JEDEC specification.	
18.	Ensure the V_{REF} source supplies the minimal current required by the system (memories + processor).	
19.	If a resistor divider network is used to generate V_{REF}, ensure that both resistors the same value and 1% tolerance.	
	Routing	
20.	The recommended routing order within the DDR3 interface is as follows: 1. Data address/command 2. Control 3. Clocks 4. Power **Note:** This order allows the clocks to be tuned easily to the other signal groups. It also assumes an open critical layer on which clocks are freely routed.	

Table 1. DDR3 designer checklist (continued)

No.	Task	Completed?
21.	Complete the following global routing items: • Do not route any DDR3 signals overs splits or voids. • Ensure that traces routed near the edge of a reference plane maintain at least 30–40 mils gap to the edge of the reference plane. • Allow no more than 1/2 of a trace width to be routed over via antipad.	
22.	When routing the data lanes, route the outer-most (that is, longest lane first), because this determines the amount of trace length to add on the inner data lanes.	
23.	Ensure the max lead-in trace length for data/address/command signals are no longer than 7 inches.	
24.	Ensure the clock pair assignments are optimized to allow break-out of all pairs on a single critical layer.	
25.	Route all signals within a given byte lane on the same critical layer with the same via count. Assuming ECC is used, the DDR3 data bus consists of nine data byte lanes. **Note:** The byte ordering below is not a requirement; byte lanes can be routed in the order that best fits the user's application. • Byte lane 0—MDQ(7:0), MDM(0), MDQS(0), $\overline{\text{MDQS}}$(0) • Byte lane 1—MDQ(15:8), MDM(1), MDQS(1), $\overline{\text{MDQS}}$(1) • Byte lane 2—MDQ(23:16), MDM(2), MDQS(2), $\overline{\text{MDQS}}$(2) • Byte lane 3—MDQ(31:24), MDM(3), MDQS(3), $\overline{\text{MDQS}}$(3) • Byte lane 4—MDQ(39:32), MDM(4), MDQS(4), $\overline{\text{MDQS}}$(4) • Byte lane 5—MDQ(47:40), MDM(5), MDQS(5), $\overline{\text{MDQS}}$(5) • Byte lane 6—MDQ(55:48), MDM(6), MDQS(6), $\overline{\text{MDQS}}$(6) • Byte lane 7—MDQ(63:56), MDM(7), MDQS(7), $\overline{\text{MDQS}}$(7) • Byte lane 8—MECC(7:0), MDM(8), MDQS(8), $\overline{\text{MDQS}}$(8) To facilitate fan-out of the DDR3 data lanes (if needed), alternate adjacent data lanes onto different critical layers (see Figure 1 and Figure 2). **Note:** Some product implementations may only implement a 32-bit wide interface. **Note:** If the device supports ECC, Freescale highly recommends that the user implements ECC on the initial hardware prototypes.	
26.	Choose one of the following options to select the impedances and spacings for the DDR3 data group. Option #1 (wider traces—lower trace impedance) • Single-ended impedance = 40 Ω. The lower impedance allows traces to be slightly closer with less cross-talk. • Utilize wider traces if stackup allows (7–8 mils) • Spacing to other data signals = 1.5x to 2.0x • Spacing to all other non-DDR signals = 4x Option #2 (smaller traces—higher trace impedance) • Single-ended impedance = 50 Ω. • Smaller trace widths (5–6 mils) can be used. • Spacing between like signals should increase to 3x (for 5 mils) or 2.5x (for 6 mils) respectively	
27.	Ensure one of the following across all DDR3 data lanes: • For MPC8572 and MPC8536 only, ensure that all the data lanes are matched to within 1.0 inch. • For all other QorIQ devices, ensure that all the data lanes are matched to within 2.0 inches.	
28.	Ensure that each data lane properly is trace-matched to within 20 mils of its respective differential data strobe (this assumes the highest frequency operation). • Ensure the trace matching for parts with operational speeds of higher than 1600MT/s is within +/-5 mils.	
29.	When adding trace lengths to any of the DDR3 signal groups, ensure that there is at least 25 mils between serpentine loops that are in parallel.	

Table 1. DDR3 designer checklist (continued)

No.	Task	Completed?
30.	**Note:** Some product implementations may support only the single-ended version of the strobe. • Match all segment lengths between differential pairs along the entire length of the pair. Trace match the MDQS/ $\overline{\text{MDQS}}$ pair to be within +/- 5 mils. • Maintain constant line impedance along the routing path by maintaining the required line width and trace separation for the given stackup. • Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices such as clock chips. • Differential impedance 75–95 Ω • Differential impedance 90-95 Ω, for parts with operational speeds of higher than 1600MT/s • Diff Gap = 4–5 mils (as DQS signals are not true differential (also known as “pseudo differential”) • Diff Gap = 5–8 mils, for parts with operational speeds of higher than 1600MT/s Choose one of the following options to select the impedances and spacings for MDQS/$\overline{\text{MDQS}}$ differential strobes. Option #1 (wider traces—lower trace impedance) • Single-ended impedance 40 Ω. The lower impedance allows traces to be slightly closer with less cross-talk. • Utilize wider traces if stackup allows (7–8 mils) • Spacing to other data signals = 2x. • If not routed on the same layer as its associated data, then 4x spacing Option #2 (smaller traces—higher trace impedance) • Single-ended impedance = 50 Ω. • Smaller trace widths (5–6 mils) can be used. • Spacing between like signals (other data) should increase to 3x (for 5 mils) or 2.5x (for 6 mils) respectively. • Do not divide the two halves of the diff pair between layers. Route MDQS/$\overline{\text{MDQS}}$ pair on the same critical layer as its associated data lane.	
31.	Ensure fly-by topology is used for address/command/control and clock groups. The routing in fly-by topology should go from chip 0 to chip *n* and can be in the order that is most convenient for the board design. The fly-by topology routing of address/command/ control and clock groups must end at the termination resistors that are after chip *n.* Choose one of the following options to select the impedances and spacings for the DDR3 address/command/control group. Option #1 (wider traces—lower trace impedance) • Single-ended impedance = 40 Ω. The lower impedance allows traces to be slightly closer with less cross-talk. • Utilize wider traces if stackup allows (7–8 mils) • Spacing to other like signals = 1.5x to 2.0x • Spacing to all other non-DDR signals = 3–4x Option #2 (smaller traces—higher trace impedance) • Single-ended impedance = 50 Ω. • Smaller trace widths (5–6 mils) can be used. • Spacing between like signals should increase to 3x (for 5 mils) or 2.5x (for 6 mils) respectively • Spacing to all other non-DDR signals = 3–4x with regards to tuning • Tune signals to +/-10 mils of the clock at each device.	

Table 1. DDR3 designer checklist (continued)

No.	Task	Completed?
32.	Ensure clocks are routed as a differential pair, with the following recommendations: • P-to-N tuning = +/-5 mils • Target single-ended impedance 40–50 Ω. The lower impedance reduces cross-talk. • Differential impedance 75–95 Ω • Differential impedance 90–95 Ω, for parts with operational speeds of higher than 1600MT/s • Diff Gap = set per stackup Choose one of the following options for the DDR3 differential clocks. Option #1 (wider traces—lower trace impedance) • Attempt to utilize wider traces if stackup allows (7–8 mils) • Spacing to other signals = 4x. Option #2 (smaller traces—higher trace impedance) • Single-ended impedance = 50 Ω. • Smaller trace widths (5–6 mils) can be used. • Spacing to other signals = 4x. **Note:** The clock signal trace length from the memory controller to any given DDR3 chip must be longer than its corresponding strobe trace length.	
33.	Ensure that all clock pairs are routed on the same critical layer (one referenced to a solid ground plane).	
34.	Ensure space from one differential pair to any other trace (this includes other differential pairs) should be at least 25 mils.	
35.	If unbuffered DIMM modules are used, are all required clock pairs per DIMM slot connected? **Note:** Single ranked DIMM requires 1 clock pair and dual ranked DIMM requires 2 clock pairs	
36.	Check the skew between the clock and corresponding strobe for each byte lane. The clock and strobe trace lengths should be measured from the memory controller pin to the DDR3 DRAM chip pin. After obtaining the MCK to DQS for each byte lane, do the following: • For all devices, max skew is less than 10 inch. • For MPC8572 and MPC8536, (max skew – min skew) is less than 5.5 inches.	
MODT-/MDIC-related items		
37.	Connect each of the MODT signals that are in the same group to the same physical memory bank: • MODT(0), $\overline{\text{MCS}}$(0), MCKE(0) • MODT(1), $\overline{\text{MCS}}$(1), MCKE(1) • MODT(2), $\overline{\text{MCS}}$(2), MCKE(2) • MODT(3), $\overline{\text{MCS}}$(3), MCKE(3)	
38.	• Ensure that MDIC0 is connected to ground via an 40-Ω precision 1% resistor. • Ensure that MDIC1 is connected to DDR power via an 40-Ω precision 1% resistor.	
Miscellaneous items		
39.	**Note:** This task only applies to Freescale products that support external power-on reset configuration pins for selecting the DDR type. Ensure the power-on reset configuration pins are properly set for the correct DDR type.	
Registered DIMM topologies **Note:** All previous tasks still apply.		
40.	Ensure the DIMM reset pin has been considered and connected to the proper reset logic. **Note:** The reset pin to the DRAM is 1.5 V LVCMOS.	

Table 1. DDR3 designer checklist (continued)

No.	Task	Completed?
41.	Although registered DIMMs require only a single clock per bank, attach all DDR3 clock pairs at the DIMM connector (analogous to unbuffered DIMMs) so the design can also support unbuffered DIMMs with minimal changes.	
42.	If the controller supports the optional MAPAR_OUT and $\overline{\text{MAPAR\_ERR}}$ signals, ensure that they are hooked up in the following way: • MAPAR_OUT (from the controller) => PAR_IN (at the RDIMM) • ERR_OUT (from the RDIMM) => $\overline{\text{MAPAR\_ERR}}$ (at the controller)	
43.	Ensure that a 4.7K pull-up to 1.5 V is present on $\overline{\text{MAPAR\_ERR}}$, which is an open-drain output from registered DIMMs.	
Discrete memory topologies **Note:** All previous tasks still apply with the exception of tasks in Registered DIMM topologies.		
44.	Construct the signal routing topologies for the groups like those found on unbuffered DIMM modules (that is, proven JEDEC topologies).	
45.	When placing components, optimize placement of the discretes to favor the data bus (analogous to DIMM topologies). **Optional:** Pin-swap within a given byte lane to optimize the data bus routes further. **Caution:** Do not swap individual data bits across different byte lanes.	
46.	Ensure one clock pair is used for each chip-select. The clock pair should follow the address/command/control signal groups in fly-by topology.	
47.	If multiple physical banks are needed, double stack (top and bottom) the banks to prevent lengthy and undesirable address/cmd topologies.	
48.	Properly decouple the DDR3 chips per manufacturer recommendations. Typically, five low ESL capacitors per device are sufficient. For further information (see *Decoupling Capacitor Calculation for a DDR Memory Channel* on Micron's website).	
49.	To support expandability into larger devices, ensure that extra NC pins (future address pins) are connected.	
50.	Ensure access/test points are available for signal integrity probing. This is especially critical if using blind and buried vias within the memory channel. If through-hole vias are used under the BGA devices, then generally these sites can be used for probing.	
51.	Ensure R_T, resistors on the address/command/control and clock groups are located after the last DRAM chip in the-fly-by topology.	
52.	Ensure the reset pin has been considered and connected to the proper reset logic. **Note:** The reset pin to the DRAM is 1.5V LVCMOS.	

Table 1. DDR3 designer checklist (continued)

No.	Task	Completed?
53.	If more than one chip-select/rank is implemented, ensure the same clock-to-strobe skews used for CS0 byte lanes are applied for other chip selects. **For example:** If the clock-to-strobe skew of byte lane 1 of CS0 is 2 inches, then clock-to-strobe skew of byte lane 1 of CS1/CS2/CS3 should also be 2 inches. If the clock-to-strobe skew of a byte lane cannot be the same among all chip-selects, then the maximum variation among all chip-selects/ranks must be less than 0.5 inches.	
54.	In fly-by topology, for a given byte lane, the clock trace length must be at least as long as the strobe trace length. In the case that the clock trace length is shorter, the following limits must be observed: • For MPC8572 and MPC8536 only, the clock trace length must be longer or equal to the strobe trace length for a given byte lane. • For all other devices, the clock trace length can be a maximum of 3.0 inches shorter than the strobe trance length for a given byte lane.	

2 Selecting termination resistors

Sink and source currents flow through the parallel R_T resistors on the address and control groups. The worst case power dissipation for these resistors is as follows:

$$\text{Power} = I^2 \times R_T = (13\ \text{mA})^2 \times (47\ \Omega) = 7.9\ \text{mW}.$$

Small resistors that provide dissipation of up to 1/16 W are ideal. See Section 4, "Calculating VTT current," for assumptions made for current calculations.

3 Avoiding V_{REF} noise problems

V_{REF} is a reference voltage that provides a DC bias of 0.75 V ($V_{DD}/2$) for the differential receivers at both the controller interface and the DDR devices. Noise or deviation in the V_{REF} voltage can lead to potential timing errors, unwanted jitter, and erratic behavior on the memory bus.

To avoid these problems, V_{REF} noise must be kept within the JEDEC specification:

- V_{REF} and the V_{TT} cannot be on the same plane because of the DRAM V_{REF} buffer sensitivity to the termination plane noise.
- Both V_{REF} and V_{TT} must share a common source supply to ensure that both are derived from the same voltage plane.
- Adhere to the layout considerations in Table 1 (see VREF) and ensure proper decoupling at each V_{REF} pin (at the controller, at each DIMM/discrete, and at the V_{REF} source).

Numerous off-the-shelf power IC solutions are available that provide both the V_{REF} and V_{TT} from a common source. Regardless of the generation technique, V_{REF} must track variations in V_{DDQ} over voltage, temperature, and noise margins as required by the JEDEC specifications.

See the applicable device hardware specifications to ensure that the V_{REF} supply current meets its requirements.

4 Calculating V_{TT} current

For a given topology, the worst-case V_{TT} current must be calculated. Calculate sink and source currents using a typical R_T parallel termination resistor and the worst-case parameters listed in this table.

Table 2. Worst-case parameters for V_{TT} current calculation

Parameter	Values	Comment
$V_{DDQ(max)}$	1.575 V	From JEDEC spec
$V_{TT(max)}$	0.798 V	From JEDEC spec
$V_{TT(min)}$	0.702 V	From JEDEC spec
RDRVR	20 Ω	Nominally, full strength is ~ 20 Ω.
RT	47 Ω	Can vary, but typically 25–47 Ω
VOL	0 V	Assumes driver reaches 0 V in the low state

The driver sources (V_{TT} plane sink) the following based on this termination scheme:

$$(V_{DD\_max} - V_{TT\_min})/(R_T + R_{DRVR}) = (1.575 - 0.702\ V) / (47 + 20) = 13\ mA$$

The driver sinks (V_{TT} plane source) the following based on this termination scheme:

$$(V_{TT\_max} - V_{OL}/(R_T + R_S + R_{DRVR}) = (0.798 - 0\ V) / (47 + 20) = 12\ mA$$

A bus with a balanced number of high and low signals places no real demand on the V_{TT} supply. However, a bus with all DDR address/command/control signals low (~ 28 signals)causes a transient current demand of approximately 350 mA on the V_{TT} rail. The V_{TT} regulator must provide a relatively tight voltage regulation of the rail per the JEDEC specification. Besides a tight tolerance, the regulator must also allow V_{TT} along with V_{REF} (if driven from a common IC), to track variations in V_{DDQ} over voltage, temperature, and noise margins.

5 Layout guidelines for DDR signal groups

5.1 DDR data group background information

The data group is listed before the command, address, and control group because it operates at twice the clock speed, and its signal integrityis of higher concern. The data groupalso constitutes the largest portion of the memory bus and comprises most of the trace matching requirements (those of the data lanes).

5.2 Routing DDR memory channel

To help ensure the DDR interface is properly optimized, Freescale recommends routing the DDR memory channel in this specific order:

1. Data
2. Address/command/control
3. Clocks

NOTE

The address/command, control, and data groups all have a relationship to the routed clock. Therefore, the effective clock lengths used in the system must satisfy multiple relationships. It is recommended that the designer perform simulation and construct systemtiming budgets to ensure that these relationships are properly satisfied.

5.3 Routing DDR data signals

The DDR interface data signals (MDQ[0:63], MDQS[0:8], MDM[0:8], and MECC[0:7]) are source-synchronous signals by which memory and the controller capture the data using the data strobe rather than the clock itself. When transferring data, both edges of the strobe are used to achieve the 2x data rate.

An associated data strobe (DQS and $\overline{DQS}$) and data mask (DM) comprise each data byte lane. This 11-bit signal lane relationship is crucial for routing (see Table 3). When length-matching, the critical item is the variance of the signal lengths within a given byte laneto its strobe. Length matching across all bytes lanes

is also important and must meet the t_{DQSS} parameter as specified by JEDEC. This is also commonly referred to as the write data delay window. Typically, this timing is considerably more relaxed than the timing of the individual byte lanes themselves.

Table 3. Byte lane to data strobe and data mask mapping

Data	Data Strobe	Data Mask	x4 Mode Data Strobe	Lane Number
MDQ[0:7]	MDQS0, $\overline{\text{MDQS0}}$	MDM0	MDQS9, $\overline{\text{MDQS9}}$	Lane 0
MDQ[8:15]	MDQS1, $\overline{\text{MDQS1}}$	MDM1	MDQS10, $\overline{\text{MDQS10}}$	Lane 1
MDQ[16:23]	MDQS2, $\overline{\text{MDQS2}}$	MDM2	MDQS11, $\overline{\text{MDQS11}}$	Lane 2
MDQ[24:31]	MDQS3, $\overline{\text{MDQS3}}$	MDM3	MDQS12, $\overline{\text{MDQS12}}$	Lane 3
MDQ[32:39]	MDQS4, $\overline{\text{MDQS4}}$	MDM4	MDQS13, $\overline{\text{MDQS13}}$	Lane 4
MDQ[40:47]	MDQS5, $\overline{\text{MDQS5}}$	MDM5	MDQS4, $\overline{\text{MDQS14}}$	Lane 5
MDQ[48:55]	MDQS6, $\overline{\text{MDQS6}}$	MDM6	MDQS5, $\overline{\text{MDQS15}}$	Lane 6
MDQ[56:63]	MDQS7, $\overline{\text{MDQS7}}$	MDM7	MDQS6, $\overline{\text{MDQS16}}$	Lane 7
MECC[0:7]	MDQS8, $\overline{\text{MDQS8}}$	MDM8	MDQS7, $\overline{\text{MDQS17}}$	Lane 8

NOTE

When routing, each row (that is, the 11-bit signal group) must be treated as a trace-matched group.

When x4 DRAM mode is available and used, the data mask signals are not available and instead the strobe signals listed under x4 Mode Data Strobe column will be the strobe for the second nibble of each byte lane.

5.4 DDR signal groups layout recommendations

This table lists the layout recommendations for DDR signal groups and the benefit of following each recommendation.

Table 4. DDR signal groups layout recommendations

Recommendation	Benefit
• Route each data lane adjacent to a solid ground reference for the entire route to provide the lowest inductance for the return currents.	Provides the optimal signal integrity of the data interface **Note:** This concern is especially critical in designs that target the top-end interface speed, because the data switches at 2x the applied clock.
• When the byte lanes are routed, route signals within a byte lane on the same critical layer as they traverse the PCB motherboard to the memories.	Helps minimize the number of vias per trace and provides uniform signal characteristics for each signal within the data group
• Alternate the byte lanes on different critical layers (see Figure 1 and Figure 2).	Facilitates ease of break-out from the controller perspective, and keeps the signals within the byte group together

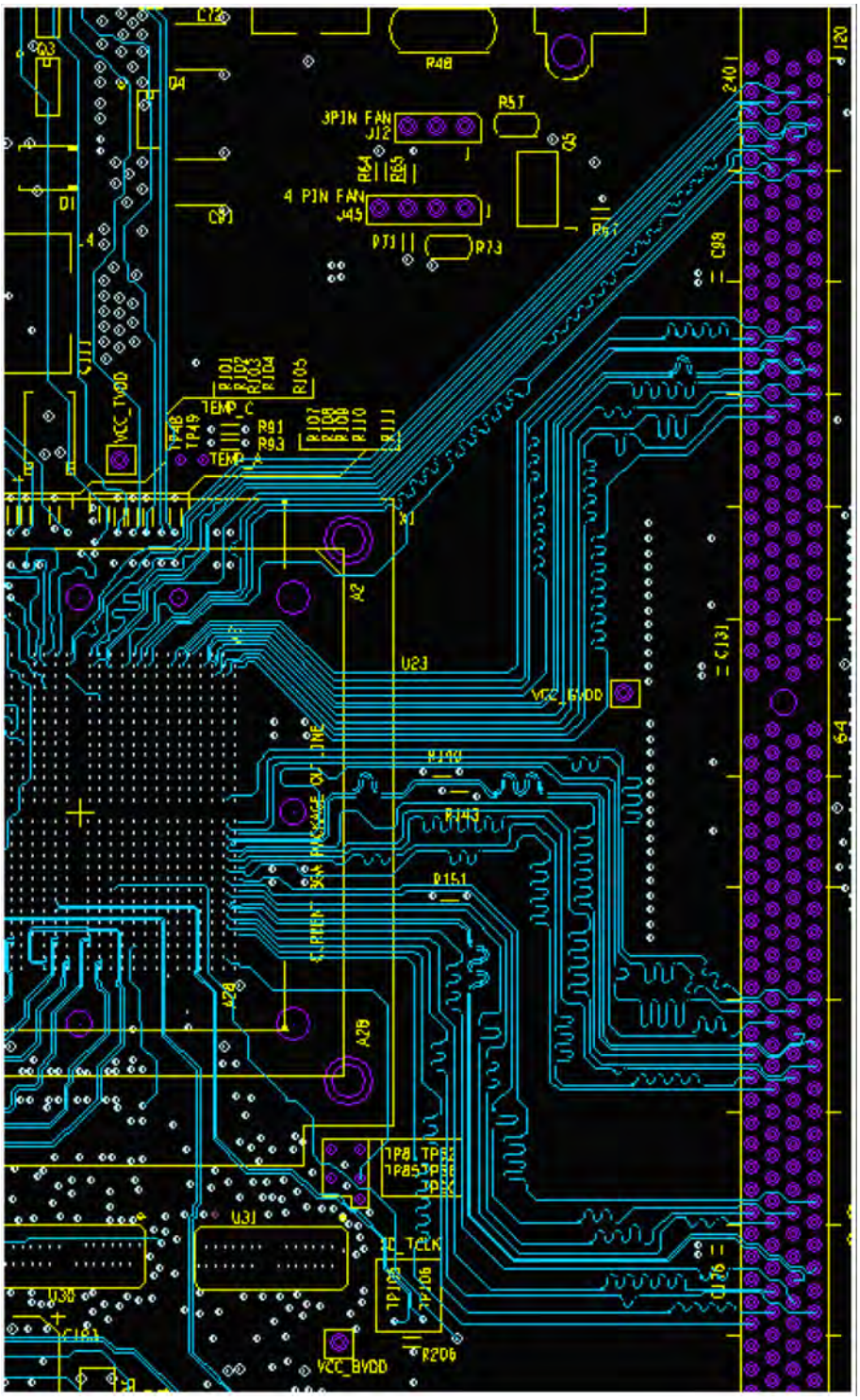

Figure 1. Alternating data byte lanes on different critical layers—Part 1

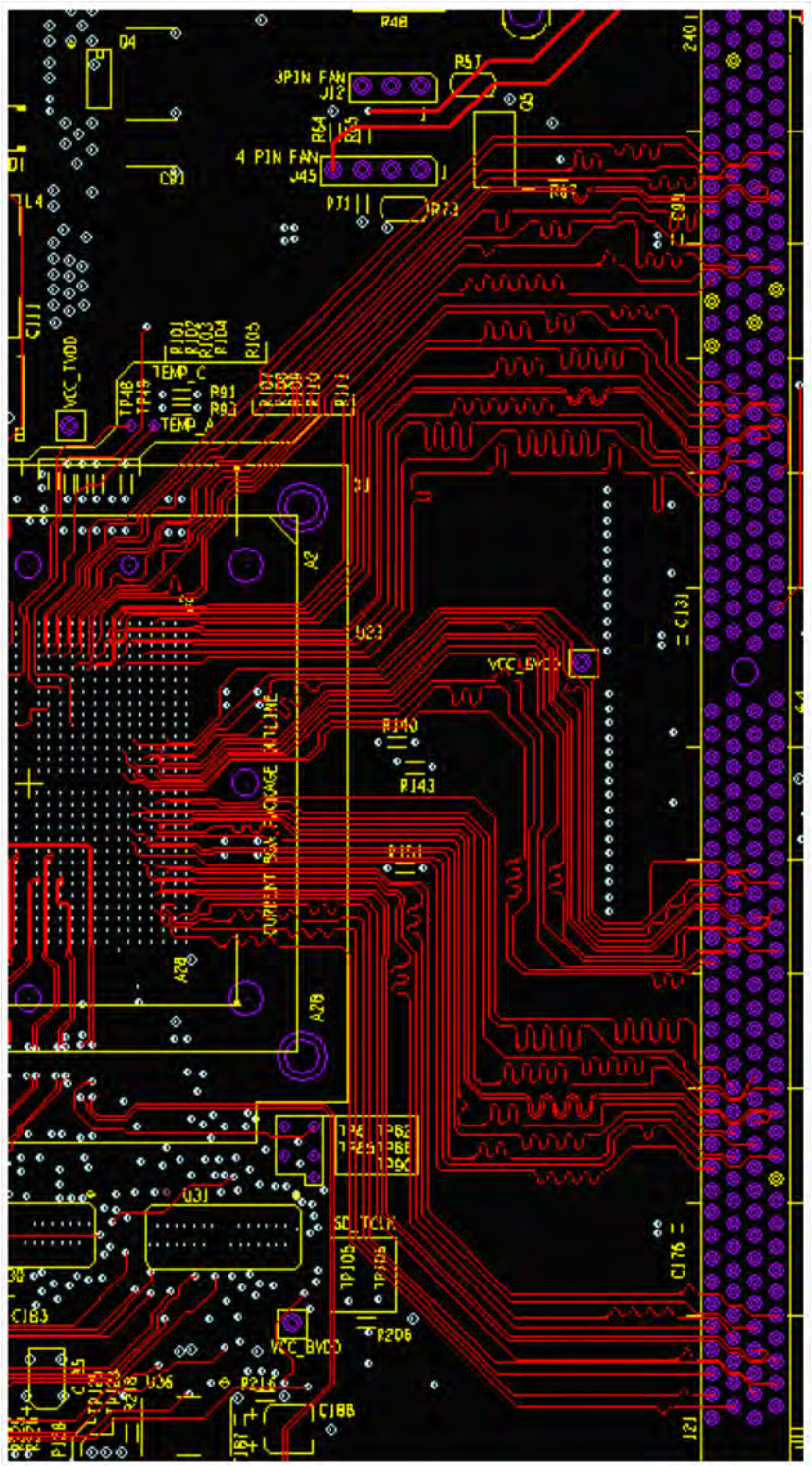

Figure 2. Alternating data byte lanes on different critical layers—Part 2

6 Using simulation models

Freescale provides IBIS models for simulation in tandem with memory vendors. The board designer can realize a key advantage in the form of extra noise margins and extra timing margins by taking the following actions:

- Optimize the clock-to-signal group relationships to maximize setup and hold times.
- Optimize termination values. During board simulation, verify that all aspects of the signal eye (see Figure 3) are satisfied, which includes at a minimum the following:
  - Sufficient signal eye opening meeting both timing and AC input voltage levels
  - Vswing max not exceeded (or alternatively, max overshoot/max undershoot)
  - Signal slew rate within specifications

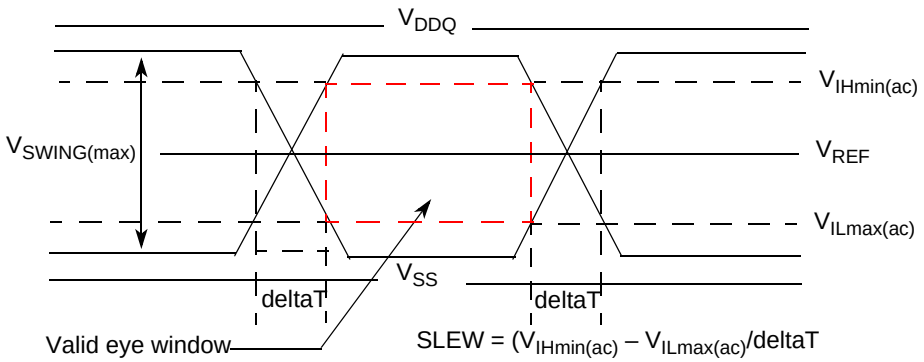

Figure 3. SSTL signal waveform eye diagram

6.1 Important read timing budget simulation considerations

Consider the following:

- Do not perform slew-rate derating for the FSL DDR3 controllers on reads (that is, DDR3 inputs (DQS/DQ) to the FSL DDR3 controllers do not need to be derated per JESD79-3E)
- Timing budgets for reads can be done with customer's simulation tool by adding the setup and hold margins rather than looking at the setup or hold margins by themselves (to account for the DQS-DQ calibration).
- Read timing should be taken at Vref rather than Vin levels (that is, read timing measurements for DQ shall be taken at Vref. No read timing measurements are taken at Vih(ac), Vil(ac), Vih(dc), or Vil(dc)).

6.2 Simulation results for QorIQ memory controller receiver during a read cycle

This figure shows the simulation results.

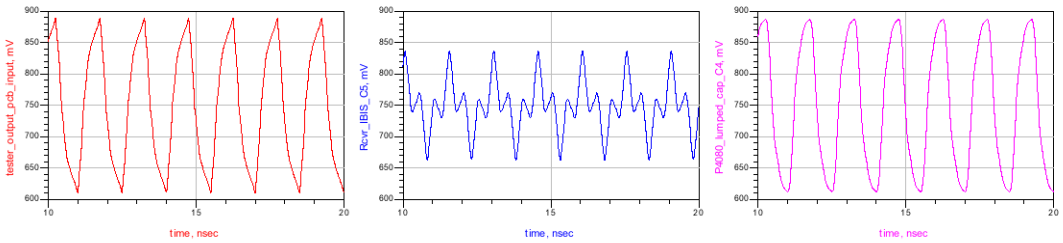

Figure 4. QorIQ memory controller receiver simulation results

From left to right:

Sent strobe (DQS) signal by DRAM during a read cycle

Same DQS signal observed at the QorIQ memory controller pin

Same DQS signal observed at the QorIQ memory controller die

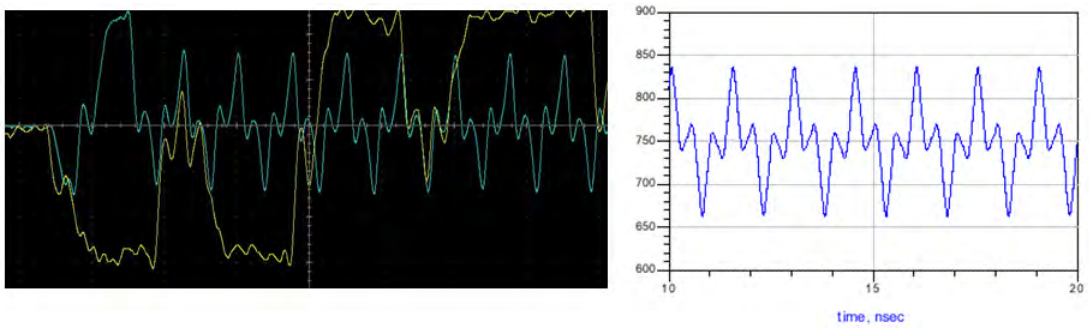

Figure 5. Measurement vs. simulation

From left to right:

Measured DQS (blue signal in scope shot) at QorIQmemory controller pin during a read cycle with ODT off

simulated DQS at QorIQ memory controller pin during a read cycle with ODT off

7 Further reading

Additional documentation that may be useful includes the following:

- The DDR chapter of the applicable device reference manual
- Micron's website: http://www.micron.com (a good example is *Design Guide for DDR3-1066 UDIMM systems: TN_41_08*)
- JEDEC's website: http://www.jedec.com (a good example is *DDR3 SDRAM Specification*)

8 Revision history

This table provides the revision history for this document.

Table 5. Document revision history

Rev. Number	Date	Substantive change(s)
6	11/2013	In Table 1, “DDR3 designer checklist”: • Changed item 2 from “Timing budgets for reads can be done with their tool by adding the setup and hold margins rather than looking at the setup or hold margins by themselves (to account for the DQS-DQ calibration) to “Timing budgets for reads can be done with customer's simulation tool by adding the setup and hold margins rather than looking at the setup or hold margins by themselves (to account for the DQS-DQ calibration)” In Section 6.2, “Simulation results for QorIQ memory controller receiver during a read cycle, • Changed belluet 2 from “Timing budgets for reads can be done with their tool by adding the setup and hold margins rather than looking at the setup or hold margins by themselves (to account for the DQS-DQ calibration) to “Timing budgets for reads can be done with customer's simulation tool by adding the setup and hold margins rather than looking at the setup or hold margins by themselves (to account for the DQS-DQ calibration)” In Table 1,“DDR3 designer checklist” item 31: • Removed bullet for “with regards to tuning“ and placed it with previous bullet • Removed the following sentence, “However, it is recommended that chip 0 be the lower data bits DQ[0:7] and chip n be the upper data bits“ Throughout: Editorial changes
5	10/2012	• Added Section 6.1, “Important read timing budget simulation considerations,” and Section 6.2, “Simulation results for QorIQ memory controller receiver during a read cycle.” • Added a column and a note for x4 DRAM mode in Table 3. In Table 1, “DDR3 designer checklist,” made the following modifications: • Modified item1. Added two notes. • Modified item2. Added information for read timing budget simulation work. • Modified item10. Changed from (100–220 μF) to (47–220 μF) • Modified item 28. Added limitation for parts with speeds of higher than 1600MT/s • Modified item 30. Added limitation for parts with speeds of higher than 1600MT/s • Modified item 32. Added limitation for parts with speeds of higher than 1600MT/s
4	01/2011	• Editorial changes throughout document In Table 1, “DDR3 designer checklist,” made the following modifications: • Modified item 31. • Modified item 32. and added the note beginning “The clock signal trace length from the memory controller...” • Modified item 40. • Modified item 46. • Modified item 51. • Modified item 53. • Added item 54.

Table 5. Document revision history (continued)

Rev. Number	Date	Substantive change(s)
3	08/2010	In Table 1, “DDR3 designer checklist,” recorded the following: • Changed item 6 from “Is the differential terminator present on the clock lines for discrete memory populations? (DIMM modules contain this terminator.) Nominal range => 100–120 Ω” to “Is the differential terminator present on the clock lines for discrete memory populations? (DIMM modules contain this terminator.)” • Removed item 7: “Recommend that an **optional** 5pF cap be placed across each clock diff pair. If DIMM modules are used, the cap should be placed as closely as possible to the DIMM connector. If discrete devices are used, the cap should be placed as closely as possible to the discrete devices.” • Added the following note to item 26: “The byte ordering stated above is not a requirement and can be done in the order that best fits the customer's application.” • Deleted line 34: “Are all clock pairs properly trace matched to within 25 mils of each other?”. • Added the following item as the last item in the table: “If more than one chip-select/rank is implemented, ensure the clock to strobe skews in each byte lane is the same across all chip-selects/ranks. The maximum clock to strobe skew difference in any byte lane, among all chip-selects/ranks, must be less than 0.5 inches.”
2	05/2010	In Table 1, “DDR3 designer checklist,” for item 28, changed “0.1 inch” to “1.0 inch.” In addition, added item 38.
1	032010	In Table 1, for item# 28, changed the second bulleted sentence as follows: For all other devices, are all the data lanes matched to within 2.0 inch?
0	01/2010	Initial public release

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: AN3940
Rev. 6
11/2013