Application Report
SLUA963A–November 2019–Revised June 2020

HEV/EV Traction Inverter Design Guide Using Isolated IGBT and SiC Gate Drivers

Audrey Dearien

ABSTRACT

This document describes how to design a HEV/EV traction inverter drive system using the advantages of TI's isolated gate drivers diagnostic and protection features.

Contents

1 Introduction

Intelligent means of vehicle monitoring and protection are necessary due to the full electrification of vehicles and the stringent safety requirements that vehicle manufacturers are held to. The electronics systems and components must remain functional throughout the vehicle's lifetime in order to maintain safe operation. The traction inverter is vital to the drive system and includes protection and monitoring auxiliary circuits to prevent system-level failure modes such as over- and under-torque, unintentional motor commutation, or motor shutdown. This design guide reviews HEV/EV architectures, the failure modes of the traction inverter system, and how the gate driver and surrounding circuits can be used to enhance the reliability of the system. Texas Instruments' UCC217xx-Q1 family of reinforced isolated gate drivers have integrated protection and monitoring features that simplify the design of high-power traction inverter systems. This family of drivers is developed under the TI Functional Safety Quality-Managed process. Such features include fast over-current protection or short-circuit protection, isolated temperature and voltage sensing, and under voltage lockout. Additionally, the advanced feature UCC5870-Q1 basic isolated gate driver includes integrated SPI-programmable diagnostic, protection and monitoring functions and is developed under the Functional Safety-Compliant TI process. For more information regarding the categories of TI's safety chips, visit TI's Functional Safety web page.

2 HEV/EV Overview

This section describes the key components of an HEV/EV automotive powertrain system.

2.1 HEV/EV Architectures

The electrification of vehicles has revolutionized the transportation industry and has resulted in technological advancements in both the automotive and semiconductor industries. Electrified vehicles including both hybrid electric (HEV) and full electric (EV) vehicles consist of various power electronics systems for regulating power from the grid, managing the battery storage element, and ultimately driving the vehicle. Electric motors are used to drive the wheels of the vehicle or to act as a generator to transfer mechanical energy into electric energy to store in the battery. HEVs use a combination of electric motors and generators, used as a low-power starter and alternator or to fully drive the vehicle, along with the internal combustion engine (ICE) typically used as the primary source of the vehicle's motion. The EV, on the other hand, utilizes electric motors as the primary source of vehicle motion as well as for regeneration.

The main HEV architectures are series, parallel and combination of series and parallel, shown in Figure 1. In the series configuration (a), the ICE is indirectly tied to the transmission through the electric motor. The power electronics three-phase drive derives power from the ICE through the generator as well as from the battery. In this architecture, the ICE is optimized for a certain range of speed allowing for minimized size and increased efficiency. This is the simplest HEV architecture with regards to mechanical complexity since there is no coupling of mechanical energy.

The parallel HEV configuration (b) utilizes a combination of the ICE and electric motor mechanically coupled. The electric drive is primarily used as a low-power starter and alternator in this architecture, and is thus lower power. The efficiency of the ICE is lower due to the larger operating range but the size of the electric motor is minimized because it does not need to provide as much power as the ICE.

The series/parallel configuration (c) combines the two previous methods to achieve better efficiency. Mechanical coupling is performed by a planetary gear and the ICE and electric drives combine the traction power. In this case, the electric motor and ICE can be designed to operate within specified output ranges to improve their efficiency.

In each case, the three phase inverter is used to drive the electric motor. The inverter design varies based on the power output requirements which depends on architecture. The proper control of the inverter directly impacts the motor's efficiency and the overall efficiency of the vehicle.

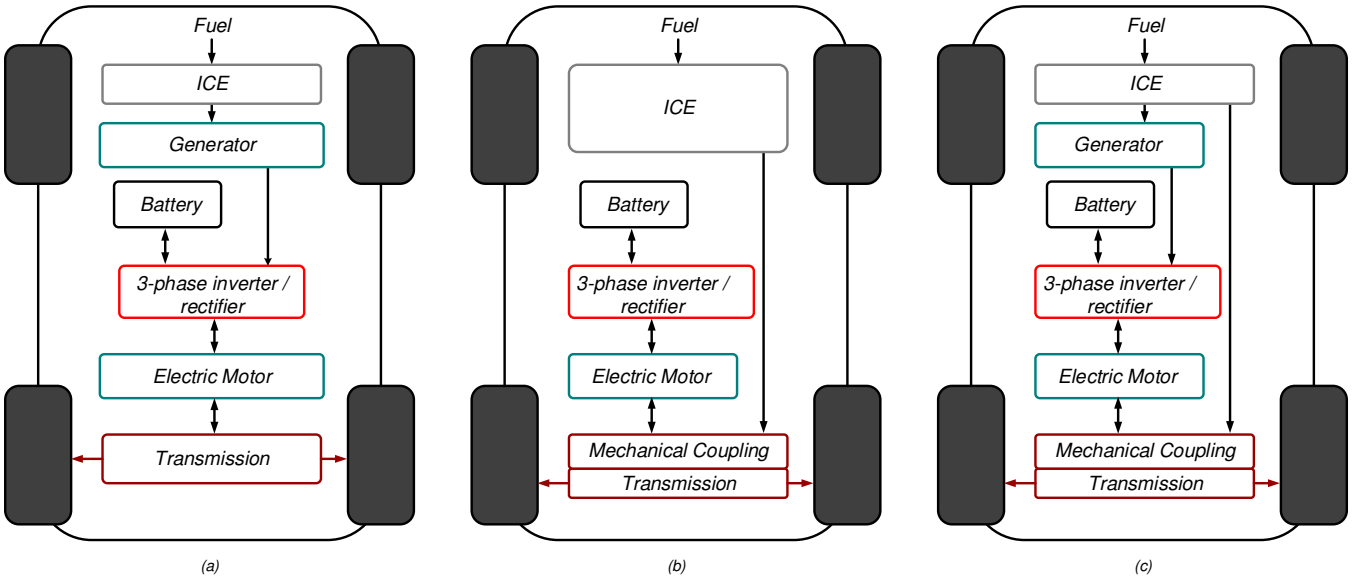

Figure 1. HEV Architectures

The pure electric vehicle, on the other hand, does not have an ICE and relies solely on the energy of the battery. Some different configurations of electric motor is shown in Figure 2. Similar to the HEV, each architecture results in different power requirements for the inverter. The electric motor may be directly tied to the wheel as shown in configurations (a) and (b) or tied to the wheel through a differential as shown in (a) and (c). Direct in-wheel drives has the benefit of simplicity and high efficiency with low maintenance, but must typically be larger in size due to low-speed requirements. The differential drive allows for high power density such that the motor can operate at a high RPM while the differential provides a fixed gear ratio. The drawback is that the mechanical gears require maintenance and has transmission loss.

High-voltage Li-ion batteries are commonly used as the energy storage unit to provide the maximum amount of capacity, minimal weight, and highest efficiency. With current technology, including various battery chemistries and power electronics efficiency, EVs still have limited range compared to HEV and plug-in HEVs. High performance EVs rely on increased power level of the traction inverter, minimization of the electronics' size, and complex controls based on sensed signals.

By increasing the efficiency and robustness of the inverter comes the increase of overall vehicle efficiency. The gate drivers makes an impact by providing the driving force behind each power switch in the inverter, as well as protection and monitoring to reduce the likelihood of failure.

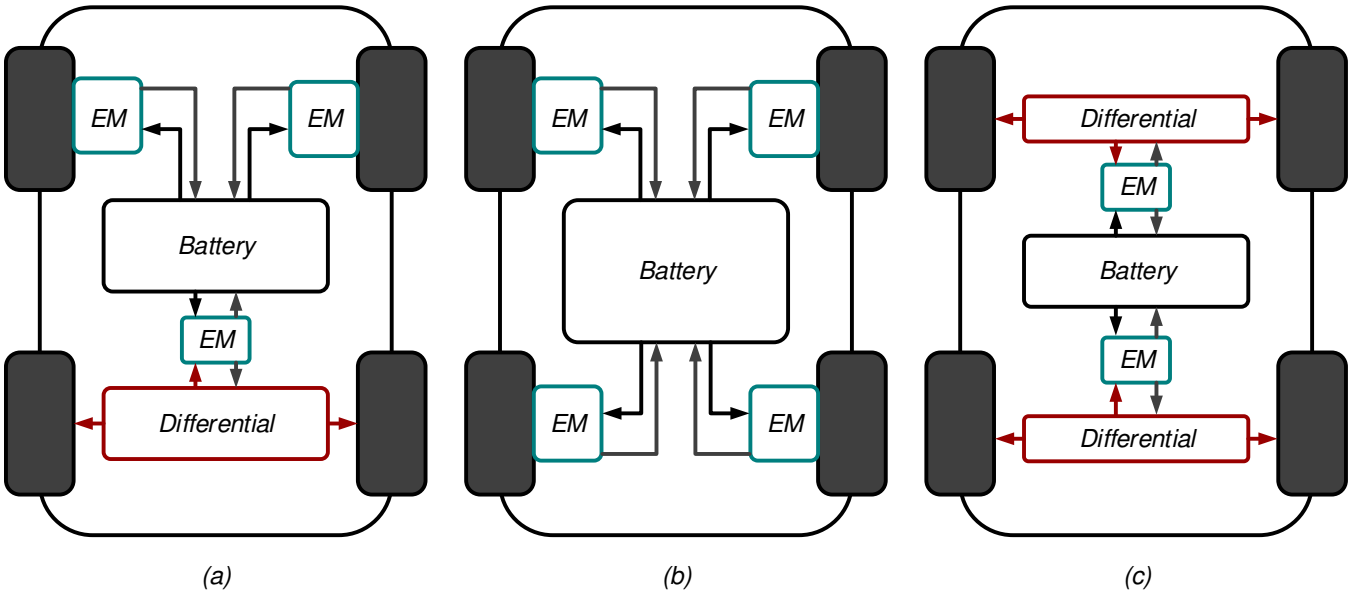

Figure 2. EV Architectures

The key blocks of an EV powertrain system are the electric motor, the traction inverter drive, the DC/DC converter, the Li-ion battery, the AC/DC grid-tied on-board charger (OBC), and controllers (MCU and PMIC), as shown in Figure 3. The traction inverter system, highlighted in red, is described in detail in the following sections. This system alone incorporates many of the protection and monitoring features utilized to achieve high safety levels.

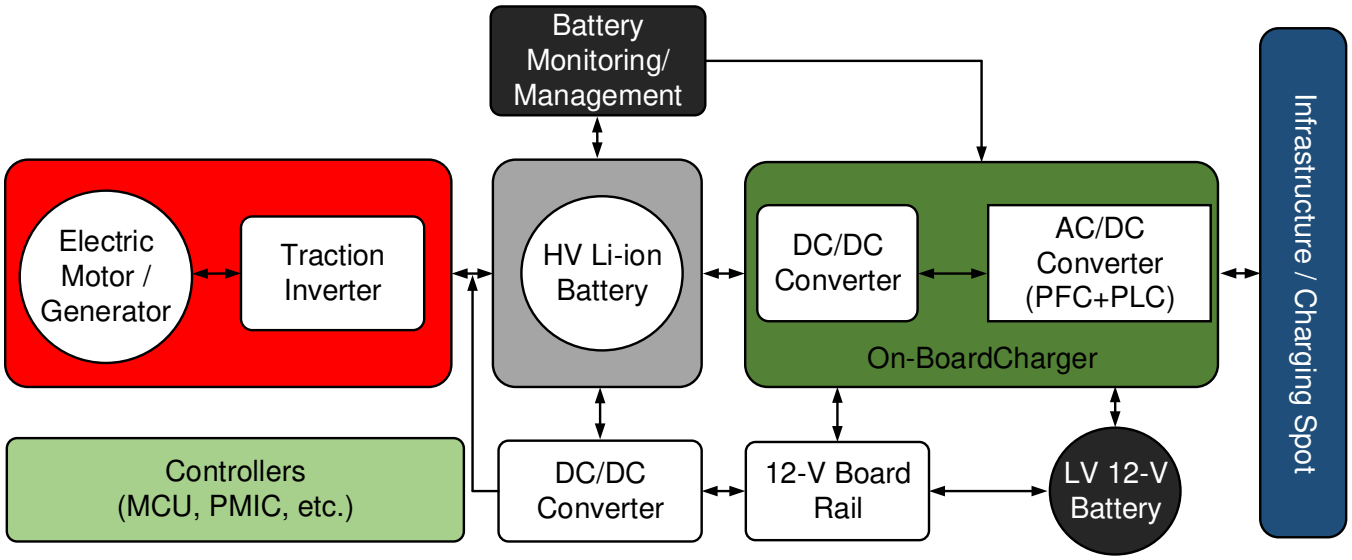

Figure 3. Blocks within an EV System

2.2 HEV/EV Traction Inverter System Architecture

Zooming in to the traction inverter system reveals multiple blocks including the power management IC (PMIC) and the microcontroller (MCU), the high-power IGBT or SiC MOSFET power modules and their temperature sensing elements, the high-voltage (HV) battery, the DC-link capacitor, sensing blocks, various protection and monitoring circuits and signal isolation, shown in Figure 4. The high-power switches are the most critical component in the inverter as they control the flow of current to the motor to generate motion. As such, the switches' are monitored and protected by sensing their temperature, voltage and current throughout their operation. The switches are controlled via the MCU and isolated gate drivers for the high side (HS) and low side (LS) of the inverter leg. The PWM signals are commonly generated using the space vector modulation (SVM) scheme. As the motor operates, the voltage, current and position signals are sensed and fed back to the controller to modify the modulation of the inverter. One such feedback method is field oriented control (FOC), which uses two phases of current and the position to generate the proper vector of modulation. A good modulation scheme, fast feedback and accurately sensed signals are required for efficient motoring.

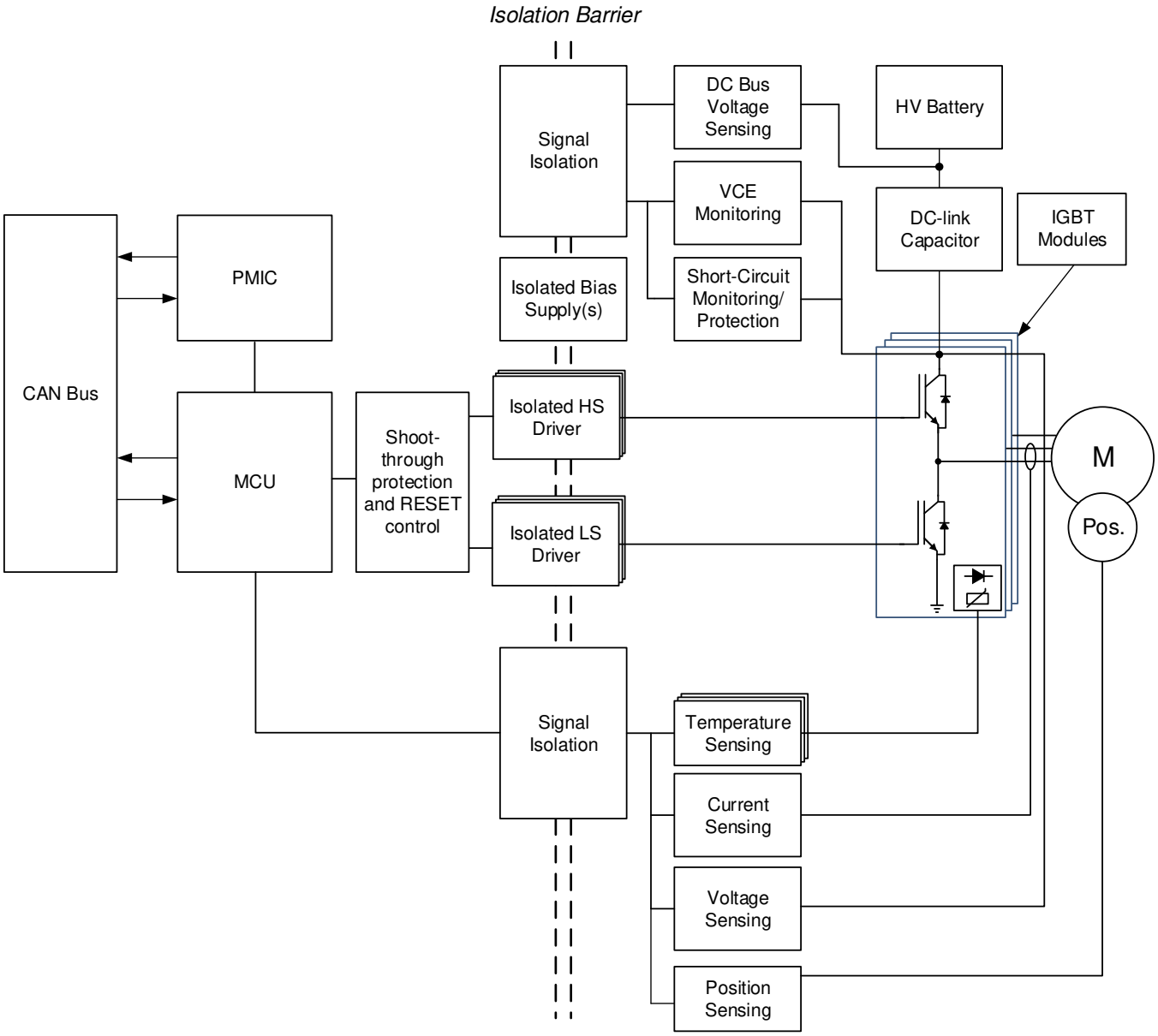

Figure 4. High-Voltage Traction Inverter Block Diagram

A closer look at the inverter, shown in Figure 5, reveals six total semiconductor power switching devices with a gate driver to amplify the PWM signal from the MCU. The three legs of the inverter convert the DC battery voltage into three phases of AC voltage and current to drive the motor. Two current measurements and a position measurement are fed back to the MCU for FOC which utilizes mathematical transformations to generate the proper signals for the six switches to control the output voltages at phases A, B and C.

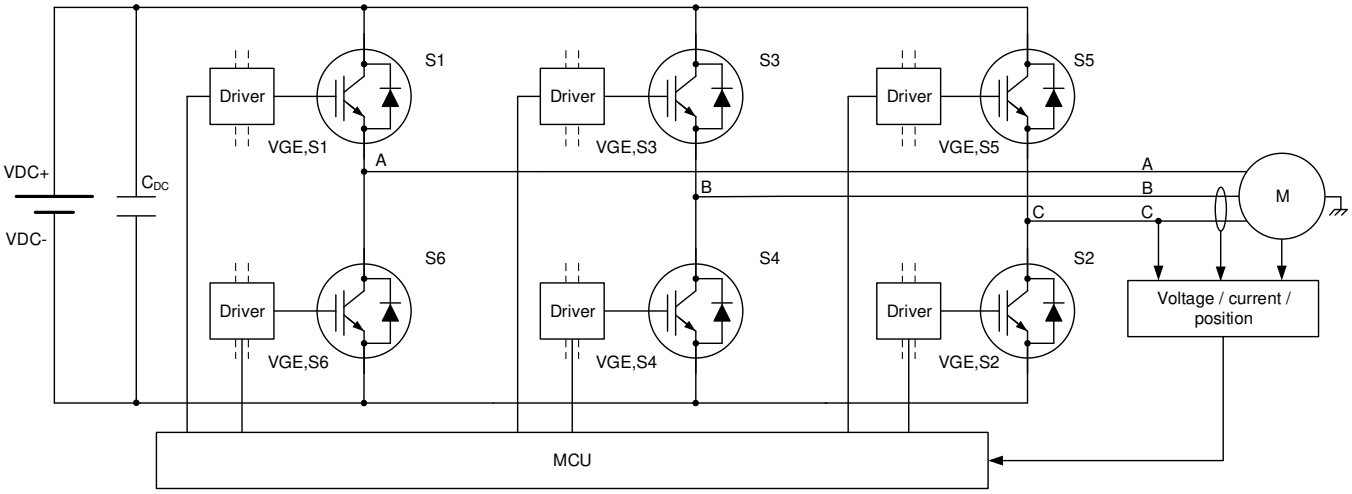

Figure 5. Three-Phase Two-Level Inverter Using IGBTs

In vector modulation, eight total states are available where two are zero vectors and the rest are active vectors used to apply the necessary voltage to the motor to generate the proper amount of torque. Table 1 shows the states where switch pairs S1 and S6, S3 and S4, and S5 and S2 are complementary to one another.

Table 1. Space Vector Modulation States

Vector	S1	S2	S3	S4	S5	S6	VAB	VBC	VCA	Vector Mode
{000}	OFF	ON	OFF	ON	OFF	ON	0	0	0	Zero
{100}	ON	ON	OFF	ON	OFF	OFF	+VDC	0	-VDC	Active
{100}	ON	ON	ON	OFF	OFF	OFF	0	+VDC	-VDC	Active
{010}	OFF	ON	ON	OFF	OFF	ON	-VDC	+VDC	0	Active
{011}	OFF	OFF	ON	OFF	ON	ON	-VDC	0	+VDC	Active
{001}	OFF	OFF	OFF	ON	ON	ON	0	-VDC	+VDC	Active
{101}	ON	OFF	OFF	ON	ON	OFF	+VDC	-VDC	0	Active
{111}	ON	OFF	ON	OFF	ON	OFF	0	0	0	Zero

There are various methods of implementing SVM. Tradeoffs between the SVM methods include reduction of switching losses, bus voltage maximum utilization, reduced harmonic content, while still achieving precise control. One such method is seven segment SVM, which is beneficial to produce a voltage waveform with low harmonics, and thus less distortion when driving the motor. The gating sequence is shown in Figure 6. A single skipped or extra gate signal as a result of an MCU control error or gate driver latched output as a result of a failure could result in inverter output distortion. Overlap of complementary switches in a phase leg could result in shoot through, and must always be avoided. As shown, the commutation of the motor is dependent on very specific gating sequences. Thus, it would be very difficult to unintentionally commutate the motor with a one-off gate driver failure.

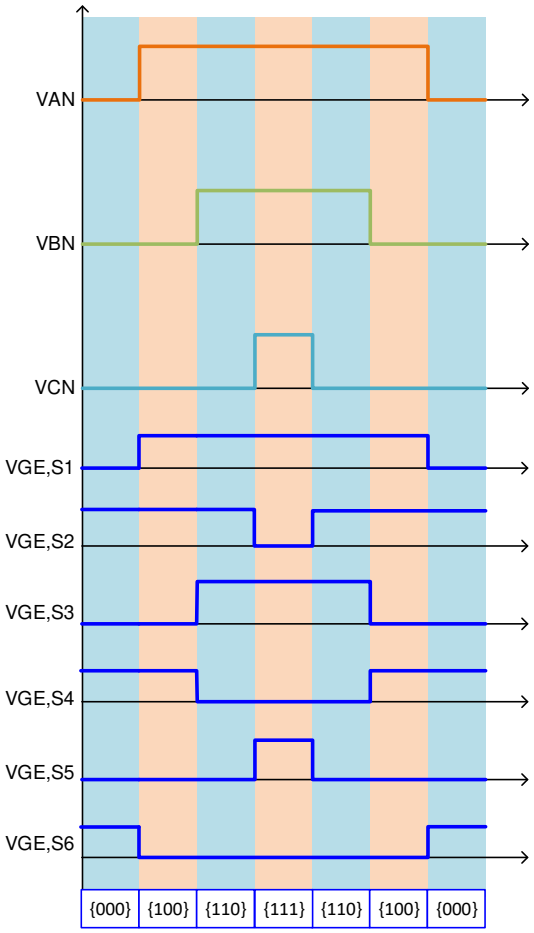

Figure 6. Seven Segment SVM

Aside from an effective gating sequence as generated by the MCU, a smart drive system includes gate drivers with protection and monitoring capabilities to protect the power switch. The following sections discuss the traction inverter system impact due to various failures within the system and how the gate drive and surrounding circuits are used to enhance the reliability of the system.

2.3 HEV/EV Traction Inverter System Performance Impact

The failure modes must all be considered throughout the traction inverter's design and implementation to ensure safe and efficient operation. Some mechanical or electronics failures that can impact the motor's performance related to the inverter system are shown in Table 2. Causes such as a motor short or open due to mechanical failure will not be discussed in this application note. Those failures that occur from the vantage point of the power electronics' will be discussed in more detail and the prevention mechanisms outlined in this section.

Table 2. Traction Inverter System Event Examples

TRACTION INVERTER SYSTEM IMPACT	MECHANICAL CAUSE	ELECTRONICS CAUSE	PREVENTION MECHANISM
Under torque	Coil short or open	IGBT short or open	IGBT protection
		Gate driver damaged	Self-test and diagnostics
		Gate driver output latched	
		Gate driver incorrect logic	
		Isolation Failure	
		MCU failure	MCU watchdog
		PMIC failure	PMIC monitor
		Sensor failure	Redundant sensing
Over torque	N/A	MCU failure	MCU watchdog
		Sensor failure	Redundant sensing
Unintended motor commutation	N/A	MCU failure	MCU watchdog
Unintended motor shutdown / no output	Coil short or open	IGBT short or open	IGBT protection
		DC bus failure	Voltage monitor
		MCU failure	MCU watchdog
		PMIC failure	PMIC monitor

The voltage applied to the three windings of the motor, as previously discussed, determine the speed and torque of the motor. Disturbances can occur due to a variety of events. The power switching devices in the inverter, referred to as the IGBTs from this point on, may become shorted or open due to a mechanical failure, over-heating, etc. The gate driver itself could be a source for failure if it is damaged due to over-temperature or mechanical reasons, has a latched output, receives an incorrect signal from the MCU, or has experienced isolation barrier failure. To cover a variety of potential failures, the gate driver and auxiliary circuits are used to monitor the power switch for short circuit, proper gate voltage and other signals to protect the IGBTs and gate drivers. Additionally, circuitry is included to perform self-tests on critical functions in the case of a latent failure which occurs after a cycle of operation. Aside from the gate driver circuits, the MCU or PMIC should also have redundant monitoring circuits to prevent controller failure or supply failure.

The following sections introduce the UCC217xx-Q1 and the UCC5870-Q1 drivers, their integrated protection and diagnostic functions, and how they simplify the design of the traction inverter system. External circuits are also described, when necessary, to assist in performing self-tests and diagnostics.

3 Design of HEV/EV Traction Inverter Drive Stage

This section will discuss how to design the HEV/EV traction inverter system using UCC217xx-Q1 and UCC5870-Q1 devices to provide the protection and diagnostics necessary for reliable operation.

3.1 Introduction to UCC217xx-Q1

The UCC21732-Q1 is a galvanic isolated single channel gate drivers designed for up to 1700V SiC MOSFETs and IGBTs with advanced protection features, best-in-class dynamic performance and robustness. UCC21732-Q1 has up to ±10-A peak source and sink current. The input side is isolated from the output side with SiO2 capacitive isolation technology, supporting up to 1.5-kVRMS working voltage, 12.8-kVPK surge immunity with longer than 40 years Isolation barrier life, as well as providing low part-to-part skew, and >150V/ns common mode noise immunity (CMTI). The UCC217xx-Q1 family of devices include the state-of-art protection features, such as fast overcurrent and short circuit detection, shunt

current sensing support, fault reporting, active miller clamp, input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness. The isolated analog to PWM sensor can be utilized for easier temperature or voltage sensing, further increasing the drivers' versatility and simplifying the system design effort, size and cost. The benefits of these circuits are given below, along with auxiliary circuitry to enhance system-level reliability.

3.2 Designing a Traction Inverter Drive System Using UCC217xx-Q1

The UCC21732-Q1 is shown in Figure 7 along with the various monitoring and protection blocks required in the inverter system. Four categories are used to describe the various blocks: Self-Test, Diagnostics, Protection and Driver Function. Self-Test blocks signify the circuits used to ensure another critical block is functioning properly. The Diagnostic blocks are used to feed back critical information to the MCU to determine monitor the power stage performance and/or behavior. The Protection blocks are used to prevent IGBT failure. Finally the Driver Function blocks include the basic gate driver function.

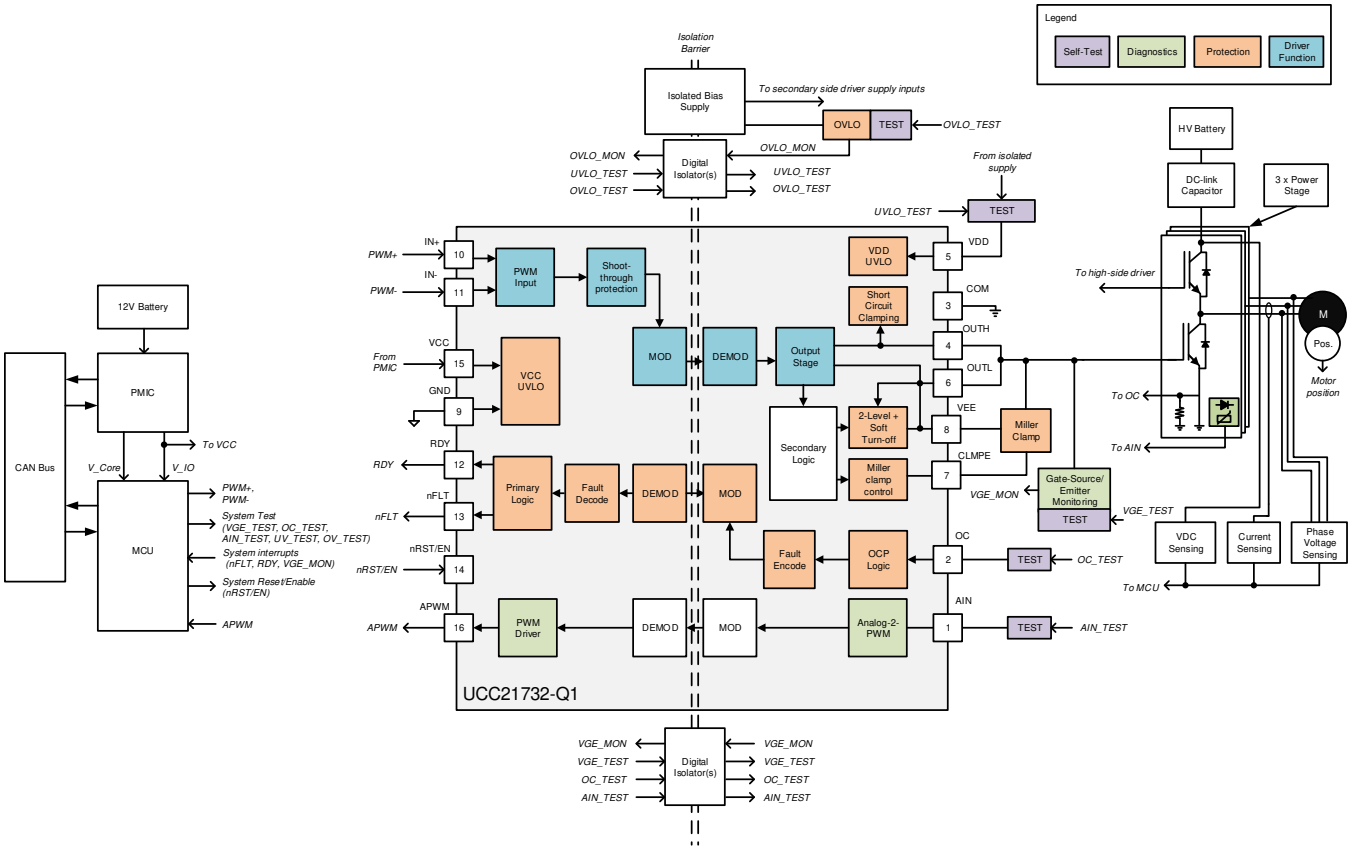

Figure 7. Block Diagram of a Traction Inverter System with UCC217xx-Q1

3.3 Description of Protection Features

This section describes the UCC217xx-Q1 integrated protection and diagnostic features and non-integrated features that are beneficial for reliable traction inverter system operation.

3.4 Protection Features of UCC217xx-Q1

The system impact of various failures are shown as given in Table 2 may be prevented using integrated and auxiliary circuits around the gate driver. Table 3 shows these system impacts and potential failures along with the integrated and auxiliary circuits of the gate driver circuitry that can be used to prevent them.

The potential failure location(s) within the system block are as shown in Figure 8, classified as (F1) PMIC failure, (F2) MCU failure, (F3) Driver failure, or (F4) Motor/Mechanical failure.

Table 3. Protection and Diagnostic Features Using UCC217xx-Q1

System impact	Associated driver and/or inverter failures	Potential failure location(s)	UCC217xx-Q1 integrated features	External circuit features
Torque disturbance	Over or under voltage of driver power supply	F1	UVLO + interrupt signal	OVLO + interrupt signal
Unintended commutation	Gate driver pulse width skew	F2 or F3	Low-delay capacitive isolation barrier and proven process	N/A
Unintended motor shutdown / Torque disturbance	Power switch short circuit	F2 or F4	DESAT/OC detection and interrupt	DESAT (UCC21750) or OC (UCC21732/10) self-test UVLO/OVLO self-test
Unintended motor shutdown / Torque disturbance	Gate shorted to ground or VDD	F2 or F3	N/A	VGE monitoring and compare to PWM with interrupt
Unintended motor shutdown	Power switch shoot-through due to false gate signal or dv/dt-induced current	F2	Anti-shoot-through logic and Miller clamp (internal or external	N/A
Torque disturbance	Power switch over-voltage	F2	Two-level turn-off and/or soft turn-off	VCE/VDS monitoring
Torque disturbance	Power switch over-temperature	F1, F2, or F4	Integrated isolated sensing with integrated bias current	N/A
Torque disturbance	Power switch gate oxide breakdown	F2 or F4	Short circuit clamping to VDD	N/A
Torque disturbance	Power switch false turn-on when input power is floating	F1 or F2	Active pulldown	N/A
Torque disturbance / Unintended motor shutdown	Power system DC bus over/under voltage	F1 or F4	Integrated isolated sensing	N/A

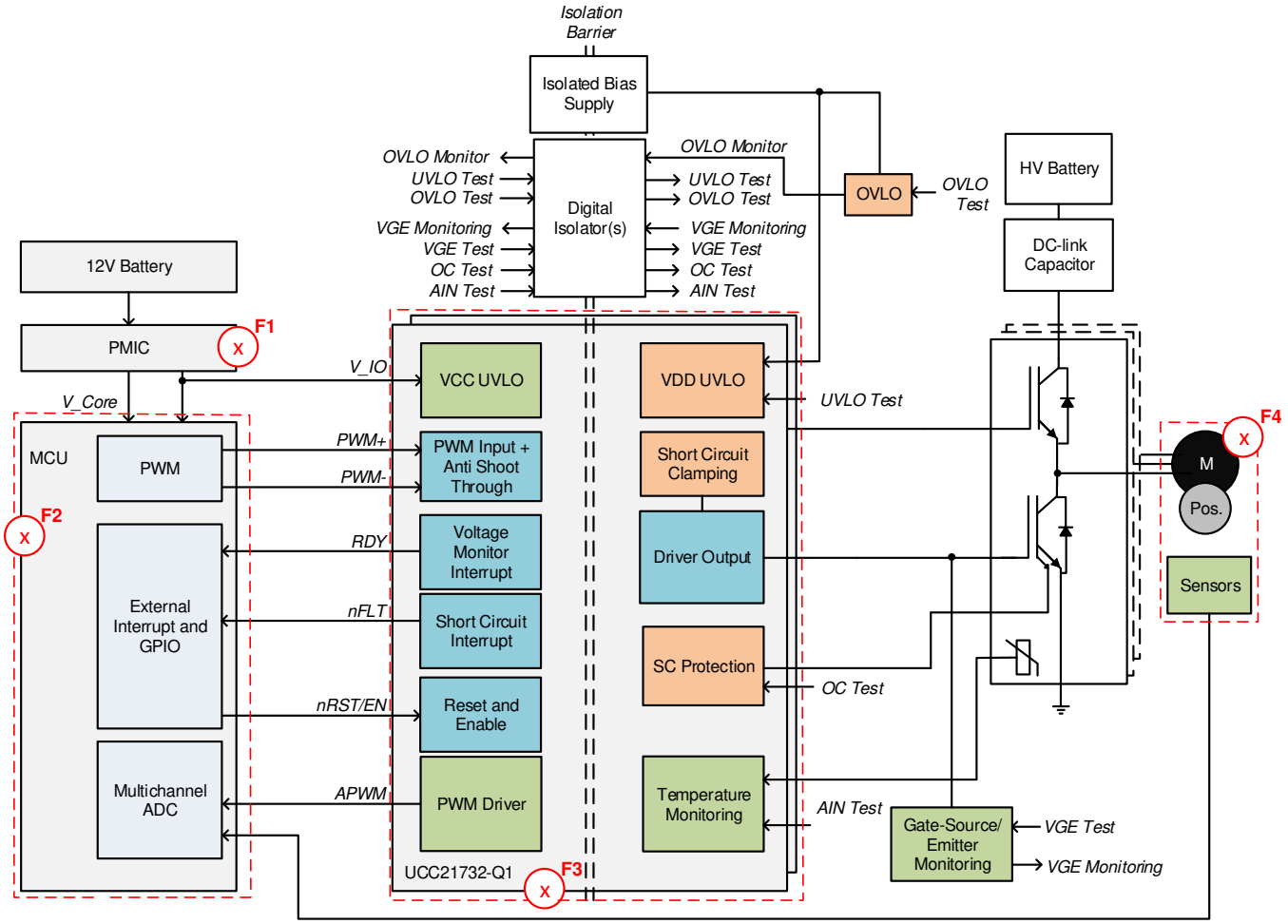

Figure 8. Possible Traction Inverter System-Level Failures and Prevention Circuits Using UCC21732-Q1

3.5 UCC217xx-Q1 Protection and Monitoring Features Descriptions

This section describes the implementation of monitoring and protection circuits using UCC217xx-Q1.

3.5.1 Primary and Secondary Side UVLO and OVLO

Under and over-voltage lockout (UVLO and OVLO) are used to protect the driver IC as well as monitor the voltage used to drive the power switch on the secondary side. UVLO is integrated into UCC217xx-Q1 for both the primary and secondary side supplies, VCC and VDD respectively. These are used to protect the system in case of bias supply failures. The output is pulled low if VCC or VDD drops below the UVLO threshold. Additionally, if there is a UVLO fault, the RDY pin will go HIGH. For VCC the threshold is 2.7 V with a 0.2 V band of hysteresis. The VDD UVLO threshold is 12 V, referenced to COM, with 0.8 V hysteresis. Aside from bias failures, the VDD-side UVLO is beneficial to protect the power switch. Based on the I-V characteristics of high-power IGBTs and SiC MOSFETs, if the device is driven at 12 V the conduction losses are smaller and early saturation of the device can be prevented. In this way, UVLO can be useful to prevent damaging the FET due to a drop in supply voltage.

Overvoltage lockout (OVLO) is also implemented to protect the power switch from being driven with too high of a voltage, outside of the device ratings, which could cause gate oxide breakdown or reduced lifetime. The driver IC should not be supplied with a voltage beyond the maximum ratings, as it may result in driver failure and uncertain driver output state. OLVO is implemented using external circuitry to protect the driver and power device from bias supply failure on the secondary side supply, VDD. VDD is divided down and compared to a fixed voltage reference generated by a Zener diode. When the divided voltage drops below the Zener voltage, the comparator output will switch and will be sent across the isolation barrier to the MCU.

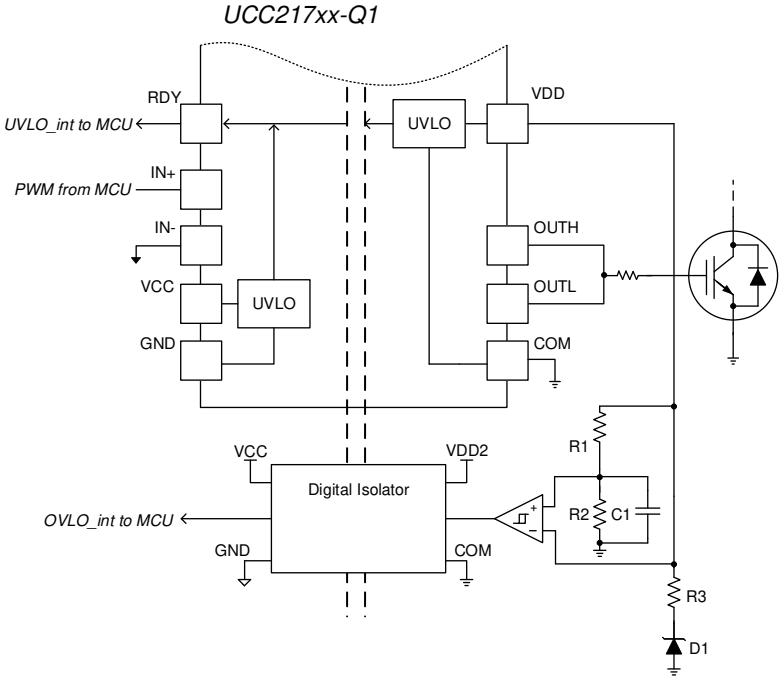

Figure 9. Integrated UVLO and External OVLO Implementation

3.5.2 Over-Current (OC) and Desaturation (DESAT) Detection

Overcurrent (OC) protection (UCC21732-Q1 and UCC21710-Q1) and desaturation (DESAT) protection (UCC21750-Q1) are used to prevent a short-circuit event from destroying the power devices. Both OC and DESAT protection are available with UCC217xx variants and are integrated internally, with a few external components based on the application. The OC and DESAT protection ST (self-test) circuits may be implemented externally and are shown below.

Integrated OC protection is shown in Figure 10. In this example, the IGBT's current is stepped down with an integrated current mirror and is output at the split emitter. The current is then measured via a shunt resistor, R_{Shunt}. The OC pin monitors the current via the voltage across R_{Shunt} and triggers the OC fault when the voltage surpasses the internal threshold of 0.7 V. At this time, the driver will initiate soft turn-off and/or 2-level turn-off to safely shut down the power device.

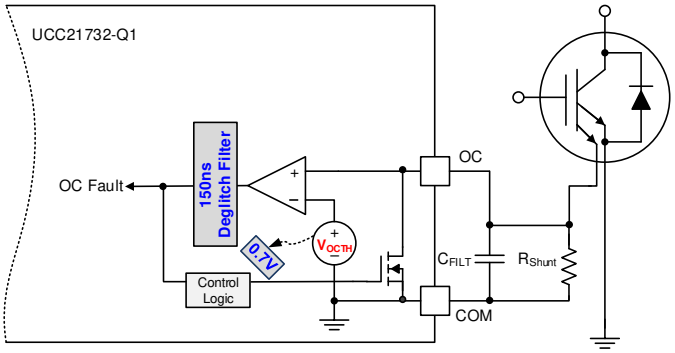

Figure 10. Overcurrent and Short Circuit Protection (UCC21732-Q1 and UCC21710-Q1)

Desaturation detection, or DESAT is a method most commonly used with IGBTs because of their well-defined knee point in the I-V curve at which the device moves from the linear to the active region as a short circuit occurs. The DESAT pin utilizes this information by monitoring the voltage across the IGBT when it is turned on. The DESAT pin is connected to the collector of the IGBT through a series resistor and HV diode, D_{HV}. D_{HV} becomes forward biased when the voltage at the IGBT increases beyond the DESAT threshold voltage of 9 V. R_{DESAT} limits the current flowing to the DESAT pin. The timing is controlled by C_{BLK}, which charges up to the threshold voltage when the driver turns on. The DESAT threshold voltage can be adjusted manually with the addition of more D_{HV} diodes in series or by adding a Zener diode in series.

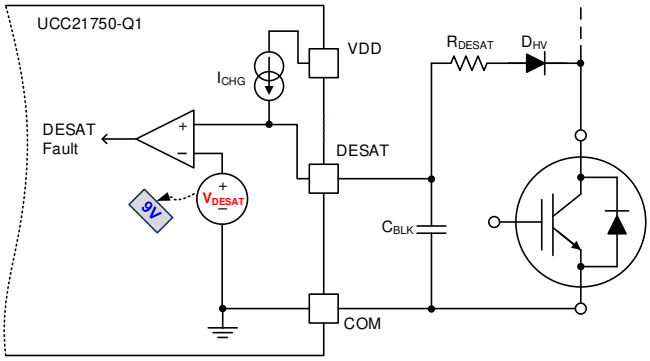

Figure 11. DESAT Protection (UCC21750)

The self-test circuit for the OC or DESAT detection is performed via external circuitry controlled by the MCU through a digital isolator, shown in Figure 12. A digital isolator is used to drive the gate of a NMOS FET to enable a fault at the DESAT/OC pin. The NMOS FET is turned on and causes the upper PMOS FET to become turned on, which allows current sourced from VDD to increase the voltage at the pin to beyond the threshold voltage. At this point, the nFLT will trigger. The input, IN+, must be high during this self-test for nFLT to trigger. If nFLT is triggered, then the short circuit detection is working properly. For more information on this circuit design and implementation, please read SiC/IGBT Isolated Gate Driver Reference Design With Thermal Diode and Sensing FET.

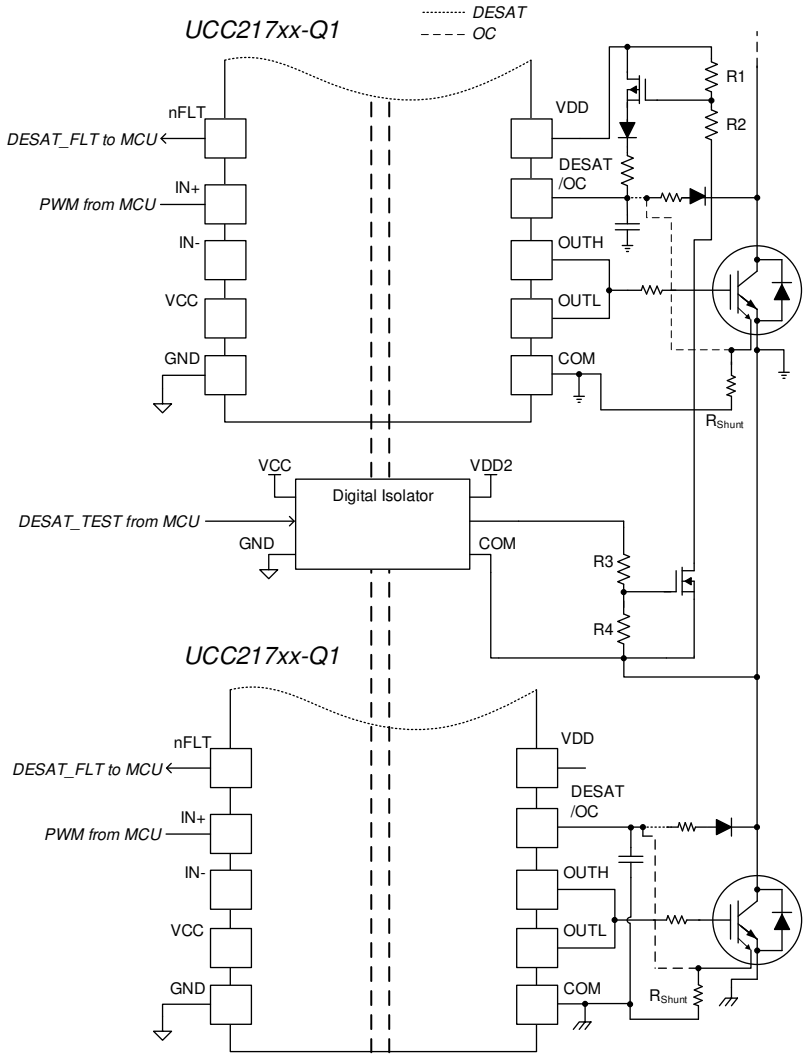

Figure 12. DESAT/OC Detection Self-Test Circuit

3.5.3 2-Level and Soft Turn-Off

As mentioned in the previous section, short circuit detection sends back a fault indication and triggers the driver to turn off the IGBT or SiC MOSFET. The driver initiates either 2-level turn-off or soft turn-off to safely shut down the IGBT or MOSFET, preventing large voltage overshoot across the device as a result of the high current transient.

2-level turn-off, shown in Figure 13, slows down the turn-off transient by pulling the gate to a mid-level voltage, 9 V, during the turn-off transition to reduce the channel current flow through the device. This significantly reduces the energy dissipation during the fault event. After the second voltage level is applied for a period of time, the driver finally pulls the gate down to VEE using a soft pull down current to transition smoothly to the off-state.

Soft turn-off, shown in Figure 14, uses a soft pull down current throughout the entire turn-off transition as opposed to applying a specified gate voltage. The 400 mA current causes the device to transition at a slower rate than it would with a hard turn-off, and thus reduces voltage overshoot while minimizing the amount of energy dissipation.

The inverter benefits not only to prevent the damage or destruction of the power switches, but also prevents high-voltages from being applied to the motor windings, which can also reduce the lifetime of the motor itself.

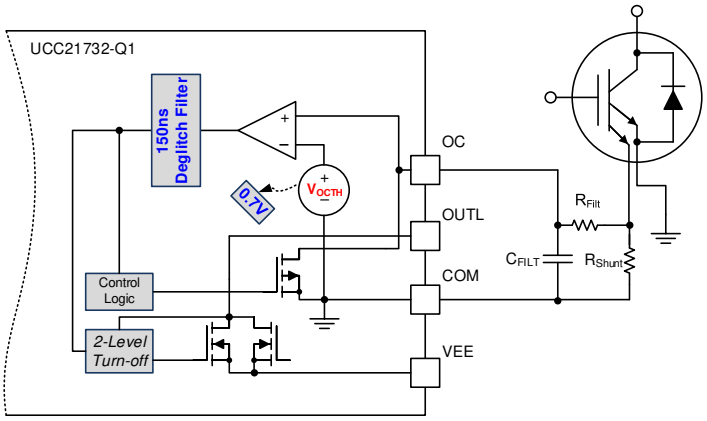

Figure 13. 2-Level Turn-Off Block (UCC21732-Q1)

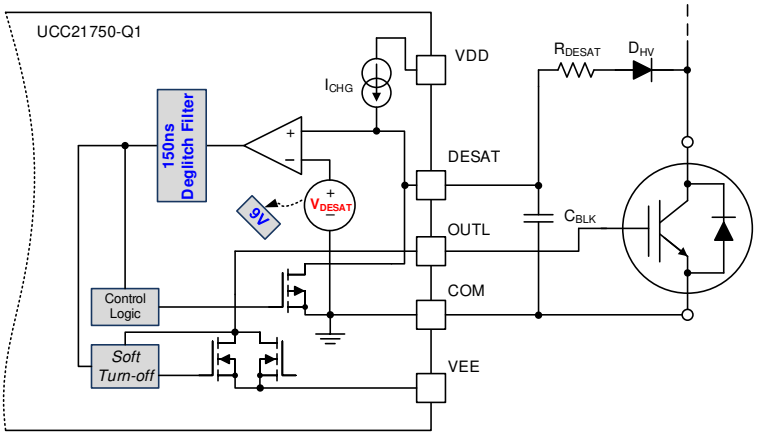

Figure 14. Soft Turn-Off Block (UCC21750-Q1, UCC21710-Q1)

3.5.4 Power Switch Gate Voltage (VGE/VGS) Monitoring

Gate voltage monitoring, as shown in , Figure 15 is used to ensure that the gate voltage is reaching the VDD level when IN+ is pulled high. This is important to ensure the device is being driven efficiently to reduce switching loss and is held on at the proper voltage level to reduce conduction loss. The gate voltage is compared to VDD, with a small voltage divider to account for the gate voltage drop due to the gate resistance, $R_{G,tot}$. The comparator's output is sent back to the MCU using a digital isolator. In case of a fault, the secondary bias supply should also be checked. This function may also be used to monitor V_{GE} when DESAT or OC detection has been detected to ensure proper turn off when the gate is pulled low by the driver.

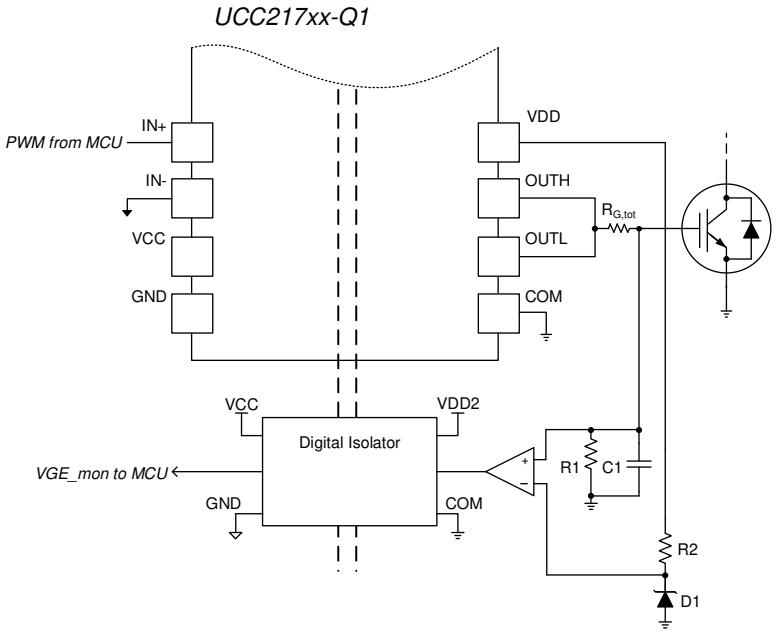

Figure 15. V_{GE} Monitoring Circuit

3.5.5 Power Switch Anti-Shoot-Through

Anti-shoot through circuitry is integrated in UCC217xx to prevent IN+ and IN- from overlapping. This allows for two single-channel drivers to be interlocked, as shown in Figure 16, where IN+ of the upper device is tied to IN- of the lower device, and vise versa. This prevents the upper and lower switches from conducting at the same time, which would result in a short circuit and device over-heating.

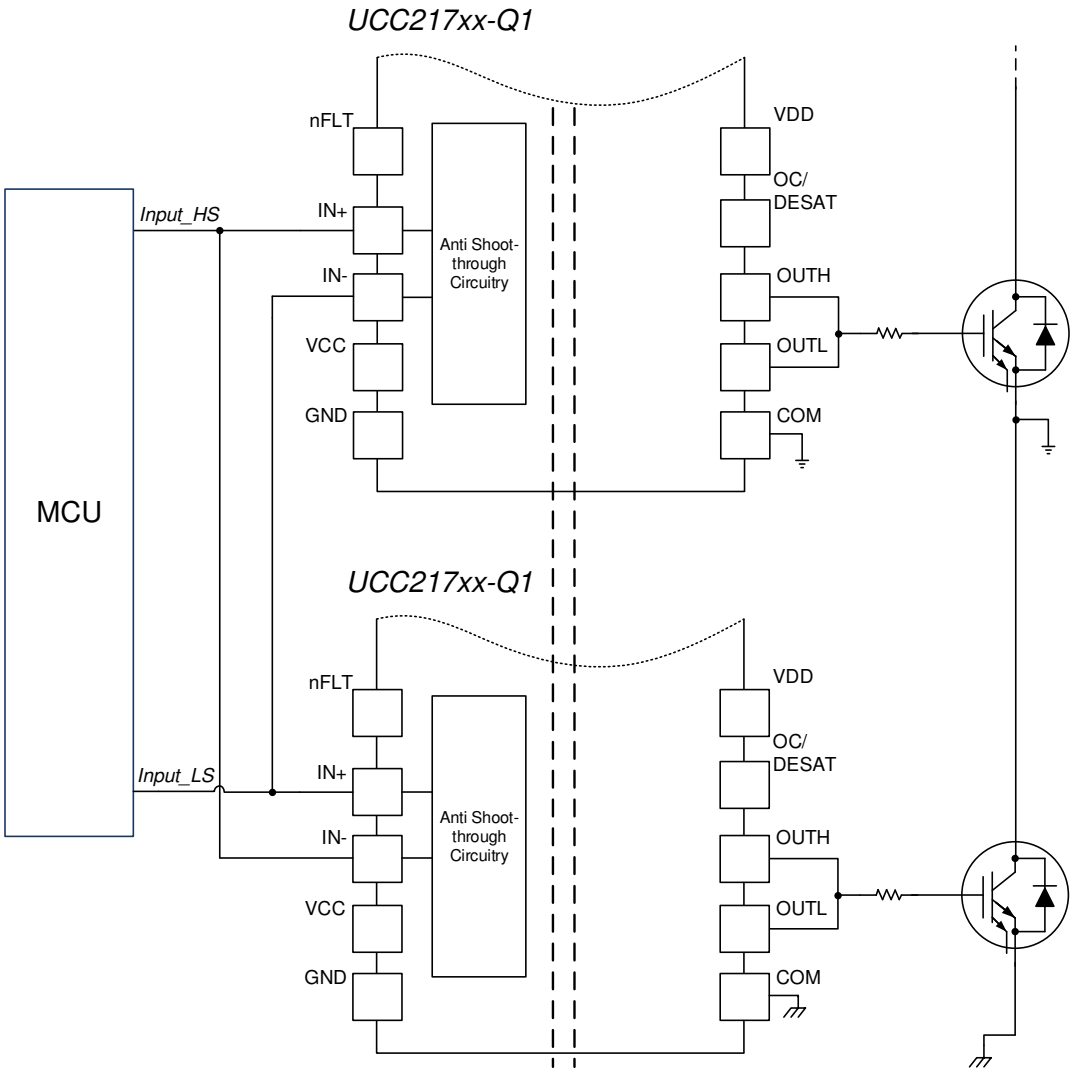

Figure 16. Integrated Anti-Shoot-Through and Interlock Circuit

3.5.6 Integrated Internal or External Miller Clamp

The Miller clamp may be either external or internal depending on the UCC217xx variant. UCC21732-Q1 is shown in Figure 17 with an external Miller clamp driven by the CLMPE pin. When OUTL goes below 2 V, the clamp is turned on to re-direct any current generated by the Miller capacitor, C_{GC}, during a high *dv/dt* transient ensuring that the device remains off during the off-state.

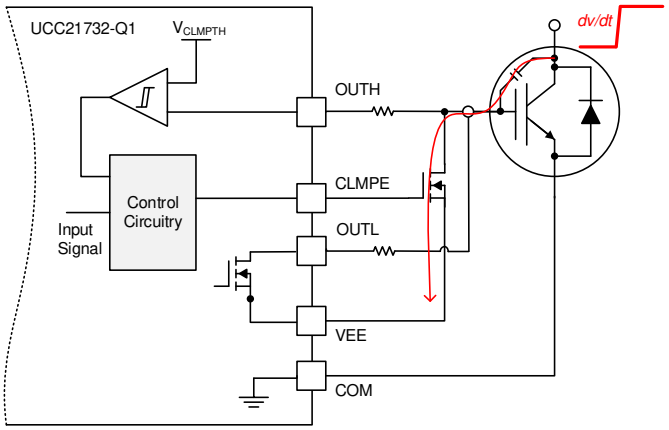

Figure 17. External Active Miller Clamp

3.5.7 Isolated Analog-to-PWM Channel

UCC217xx-Q1's integrated isolated analog-to-PWM channel can be used to monitor any voltage within the range of the AIN to COM pin including the dc bus voltage and phase current. The AIN pin also integrates a current source to bias a temperature sensor, which can be used in conjunction with the internal temperature sensor of the power switch module. Figure 18 shows the internal circuit and external connection for monitoring the IGBT module temperature. Temperature is important to determine the module's health and lifetime and monitor for misoperation.

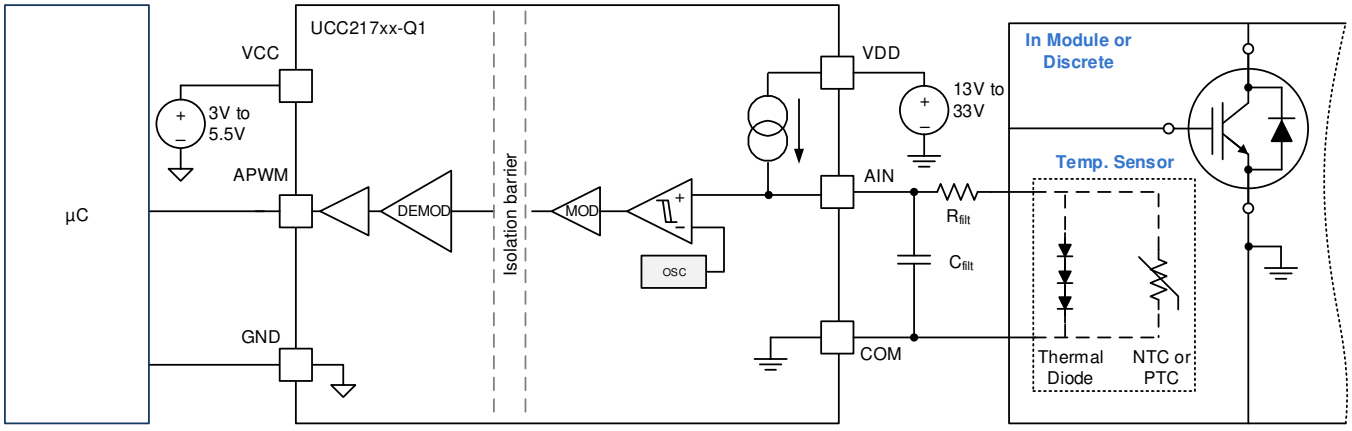

Figure 18. Isolated Analog-to-PWM Signal Block

3.5.8 Short-Circuit Clamping

During a short circuit event, the Miller capacitance, from gate to drain/collector, can source current to the OUTH/OUTL pin due to high dv/dt and may boost the OUTH/OUTL voltage. The clamping feature clamps the OUTH/OUTL pin voltage to slightly higher than VDD to prevent over-voltage at the gate and potential breakdown. The internal diodes from OUTH/OUTL to VDD perform this function as shown in Figure 19.

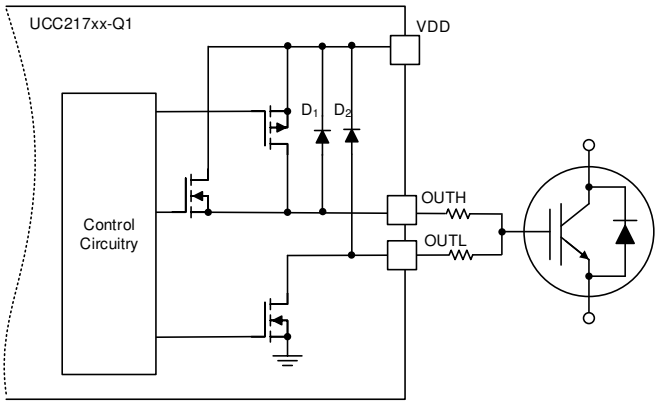

Figure 19. Short Circuit Clamping Block

3.5.9 Active Pulldown

Active pulldown ensures that OUTH/OUTL is clamped to VEE while VDD is not connected. The OUTH/OUTL pin is high-impedance when VDD is open and the pulldown feature prevents false turn on while the device supply is open. This is implemented as shown in Figure 20.

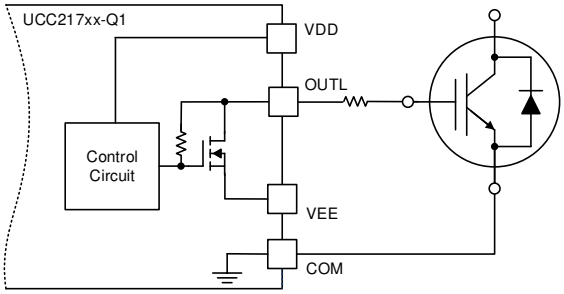

Figure 20. Active Pulldown Block

3.6 Introduction to UCC5870-Q1

The UCC5870-Q1 is a device is a TI Functional Safety-Compliant, isolated, single-channel gate driver targeted to drive high power SiC MOSFETs and IGBTs in EV/HEV applications. The input side is isolated from the output side using SiO2 capacitive isolation technology, supporting up to 1-kVRMS working voltage and longer than 40 years isolation barrier life, as well as providing low part-to-part skew, and >100V/ns common mode noise immunity (CMTI).

The UCC5870-Q1 is a platform-supporting device. The flexibility of SPI programmable blanking times, deglitches, thresholds, function enables, and fault handling allow for the UCC5870-Q1 to support a wide variety of IGBT or SiC power transistors that are used across a wide variety of applications. UCC5870-Q1 integrates all of the protection features required in most traction inverter applications. Additionally, the 15A gate drive capability eliminates the need for an external booster circuit, reducing overall solution size. The integrated Miller clamp circuit holds the gate off during transient events and can be configured to use the internal 4A pull-down, or drive an external n-channel MOSFET. All of the protections for the power transistor are integrated into the UCC5870-Q1. It supports DESAT and resistor-based over-current protection. A negative temperature coefficient power transistor temperature sensor monitor is built into the device to alert the host and prevent damage from over-temperature conditions in the switch. A zener-breakdown based clamping function is integrated to reduce the gate drive, and thereby the overshoot energy, when over-voltage spikes during turn-off occur due to inductive kick-back. Real-time gate monitoring is integrated to ensure proper connection to the power transistor and alert the host to a fault in the gate driver path.

A 10-bit ADC is built-in to the UCC5870-Q1 to provide information on power switch temperature, gate driver temperature, or any voltage that must be monitored on the secondary (high-voltage) side of the gate driver. There are six inputs (AIx) available to measure voltages with the ADC. This is convenient to acquire information on the DC-link voltage, or for measuring the VCE/VDS voltage of the power transistor during operation. The ADC features "center mode" operation to ensure low noise measurements, or can be used in a traditional "edge mode" to achieve as many measurements as possible during a PWM cycle. In addition to reading back the ADC information over SPI, a DOUT function provides a feedback signal representing one of the user-selected AIx voltages that can be monitored real-time on the primary side.

The UCC5870-Q1 integrates many safety diagnostics that enable designers to more easily implement an ASIL rated system. There are diagnostics for all of the protection features, as well as latent fault detection for circuits in the gate driver IC itself. The faults are indicated using open-drain outputs, and the specific fault is easily determined using the SPI readback. In addition to all of the safety diagnostic features, the IC integrates a primary side and secondary side "active short circuit" circuits to provide the system designer with a secondary path to control a zero-vector state for the traction inverter in the case of motor controller failure.

3.7 Designing a Traction Inverter Drive System Using UCC5870-Q1

The UCC5870-Q1 block diagram in the traction inverter system is shown in Figure 21. The legend specifies the Self-Test, Diagnostics, Protection and Driver Function blocks. In comparison to the UCC217xx-Q1 family of drivers, UCC5870-Q1 integrates many more diagnostic features such that external blocks are not longer required. Although this is beneficial to the system size and BOM reduction, it also results in the need for additional self-monitoring functions to ensure proper behavior. Thus, UCC5870-Q1 also has built-in monitoring functionality and user-commanded test features to ensure functionality of critical protection and monitoring circuits. This is done to prevent latent failures, which are those that cannot be detected by a protection mechanism.

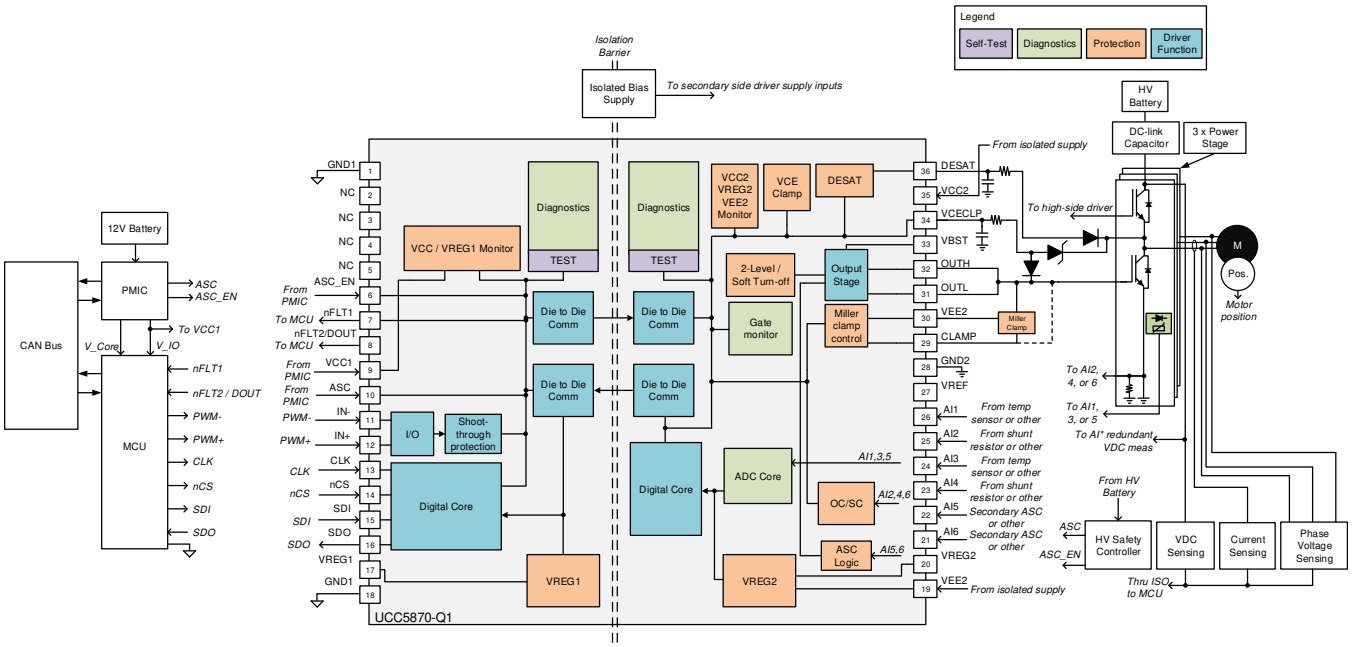

Figure 21. Block Diagram of a Traction Inverter System with UCC5870-Q1

3.8 Description of Protection Features

This section describes the UCC5870-Q1 integrated protection and diagnostic features that are beneficial for reliable traction inverter system operation.

3.9 Protection Features of UCC5870-Q1

The risk of latent and single-point failures can be reduced through gate driver integrated features as previously show in Table 3 with the UCC217xx-Q1 family. Both integrated and auxiliary circuits were outlined as ways to enable better coverage of failure modes. Table 4 shows the potential failure modes associated with the gate driver, the potential system impact and the UCC5870-Q1 integrated features. In this case, every key gate driver feature used to mitigate failure modes are integrated into the driver, versus externally implemented.

The system block visualization of the failure location(s) is shown in Figure 22 where (F1) is PMIC failure, (F2) is MCU failure, (F3) is Driver failure, and (F4) is Motor/Mechanical failure.

Table 4. Protection and Diagnostic Features Using UCC5870-Q1

System impact	Associated driver and/or inverter failures	Potential failure location(s)	UCC5870-Q1 integrated features	External circuit features
Torque disturbance	Over or under voltage of driver power supply	F1	UVLO, OVLO + interrupt signal	N/A
Unintended commutation	Gate driver pulse width skew	F2 or F3	Low-delay capacitive isolation barrier and proven process Clock and data transmission monitoring ASC control of output in case of MCU failure	N/A
Unintended motor shutdown / Torque disturbance	Power switch short circuit	F2 or F4	DESAT/OC detection and interrupt DESAT/OC self-test	N/A
Unintended motor shutdown / Torque disturbance	Gate shorted to ground or VDD	F2 or F3	VGE monitoring and compare to PWM with interrupt	N/A
Unintended motor shutdown	Power switch shoot-through due to false gate signal or dv/dt-induced current	F2	Anti-shoot-through logic and Miller clamp (internal or external)	N/A
Torque disturbance	Power switch over-voltage	F2	Two-level turn-off and/or soft turn-off VCE/VDS monitoring using ADC VCE Clamp	N/A
Torque disturbance	Power switch over-temperature	F1, F2, or F4	Integrated ADC with biasing current	N/A
Torque disturbance	Power switch gate oxide breakdown	F2 or F4	Short circuit clamping	N/A
Torque disturbance	Power switch false turn-on when input power is floating	F1 or F2	Active pulldown	N/A
Torque disturbance / Unintended motor shutdown	Power system DC bus over/under voltage	F1 or F4	Integrated ADC	N/A

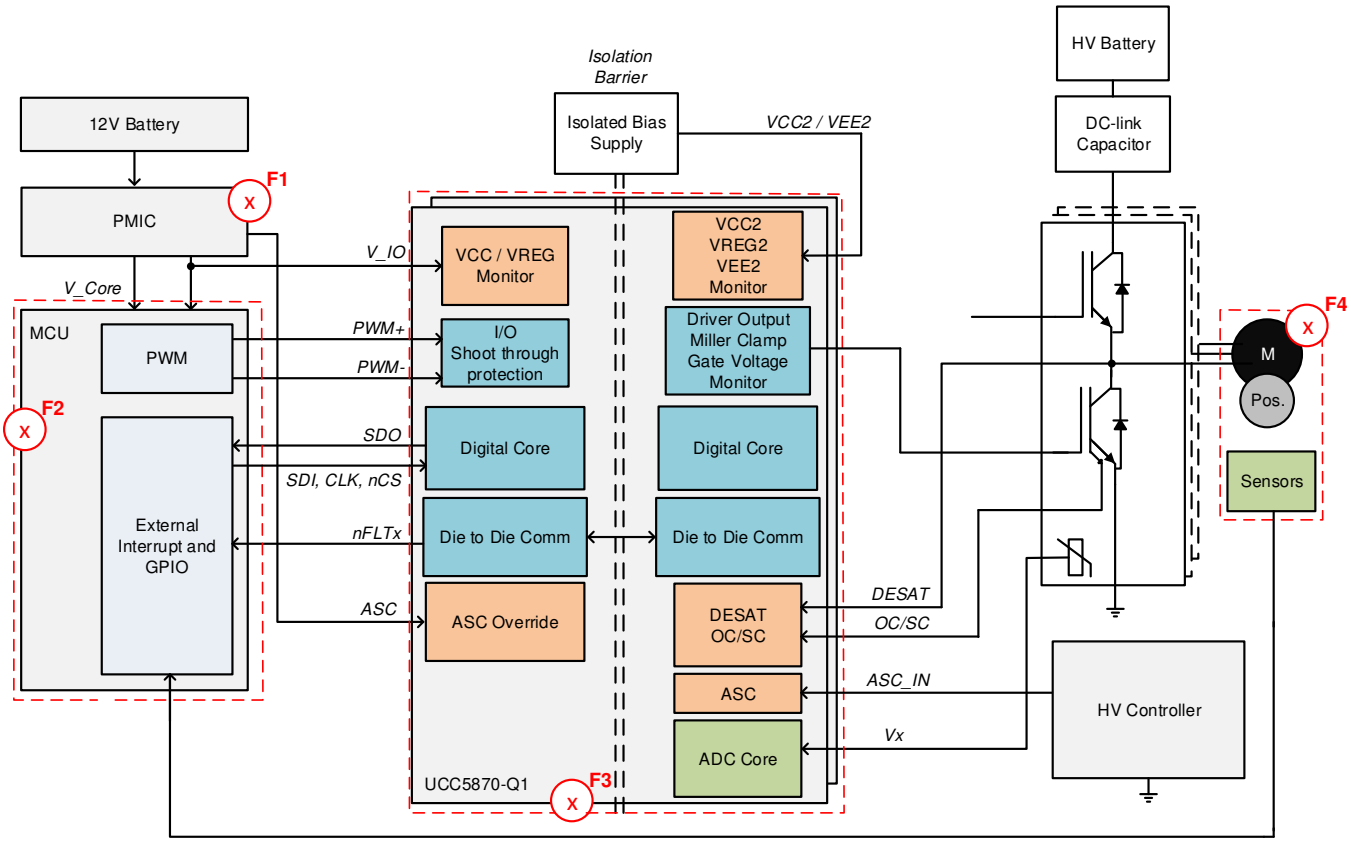

Figure 22. Possible Traction Inverter System-Level Failures and Prevention Circuits Using UCC5870-Q1

3.10 UCC5870-Q1 Protection and Monitoring Features Descriptions

This section describes the implementation of monitoring and protection circuits using UCC5870-Q1.

3.10.1 Primary and Secondary Side UVLO and OVLO

UVLO and OVLO functions are implemented for all three gate driver power supplies, VCC1, on the primary, and VCC2 and VEE2, on the secondary. The VCC1 UVLO ensures a valid supply is connected for the required logic interface. The UVLO/OVLO for VCC2 and VEE2 ensure valid supplies based on the type of transistor used (SiC MOSFET or IGBT). The UVLO function prevents overheating damage to the IGBTs/MOSFETs from being under-driven while OVLO is implemented to prevent gate oxide degredation (shortened lifetime) of the IGBT or MOSFET due to over-voltage when turned on.

The UCC5870-Q1 Analog Built-In Self-Test (ABIST) function runs diagnostics automatically on all under-voltage comparators monitoring VCC1, VCC2, and VEE2, and internal regulators during the power up process. During the test an over-voltage and under-voltage condition is simulated while the actual voltage rails remain unchanged, and the disturbance is not observable. A failure in this routine will set a fault.

3.10.2 Programmable Desaturation (DESAT) Detection and Over-Current (OC)

DESAT protection prevents the power transistor from damage in case of short circuit faults, which can be a result of incorrect control signals or a mechanical short. The DESAT input monitors the V_{CEsat} (IGBT)/V_{DSon} (MOSFET) through an external resistor and diode network, shown in Figure 23. The configuration of the DESAT pin is the same as the UCC21750-Q1. However, SPI programming enables the thresholds, blanking time, charging current, and deglitch filters to be programmable in order to best fit

the system requirement. When a fault occurs, it will be indicated in a Status Register readable by the controller and can also trigger the nFLT1 output. The turn-off of the driver output during a DESAT fault is selectable between normal, soft turn-off (STO), or two-level turnoff (2LTO) as configured via SPI. The various configurations for DESAT allow for a high level of system optimization based on switch type and power level. This only enhances the level of protection and ability to mitigate failures.

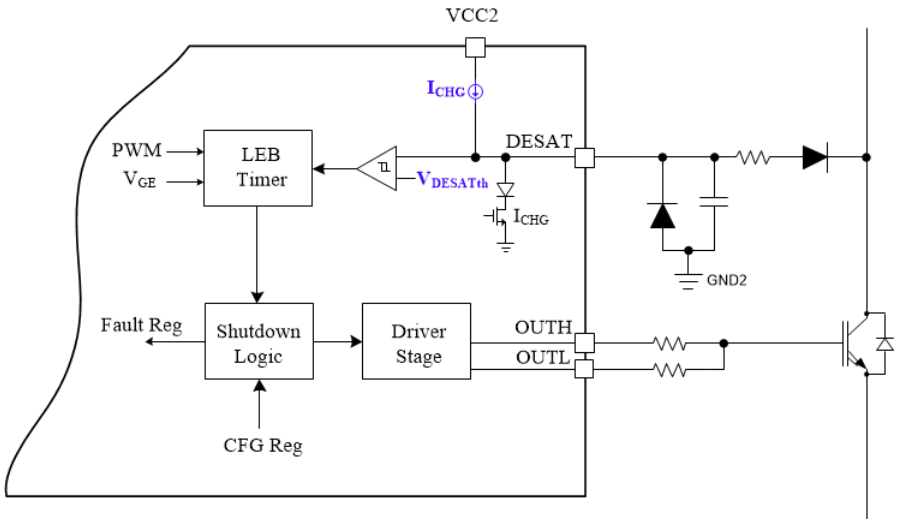

Figure 23. DESAT circuit configuration

Overcurrent and short circuit protection (OCP and SCP) is supported via three AIx inputs (AI2, AI4, AI6) for shunt resistor based OCP and SCP, shown in Figure 24. Shunt resistor-based OCP/SCP protections are intended for power transistors with integrated current sense FETs, similar to the configuration that can be used with UCC21710-Q1 or UCC21732-Q1. The mirrored power transistor currents are fed into a resistor, and the voltage is monitored at the AIx input. Once the voltage at the AIx input exceeds the threshold programmed using the Configuration Registers, the fault is indicated in the Status Register. If unmasked, nFLTx is pulled low and the driver output goes to the state defined by the Configuration Registers; this can be configured as normal turn-off, STO, or 2LTO. A blanking time is used for both OCP and SCP to prevent unwanted false protection triggering during transitions and is also selectable. The thresholds for OCP and SCP, deglitch timing, blanking time, and reporting and driver action are all programmable via SPI.

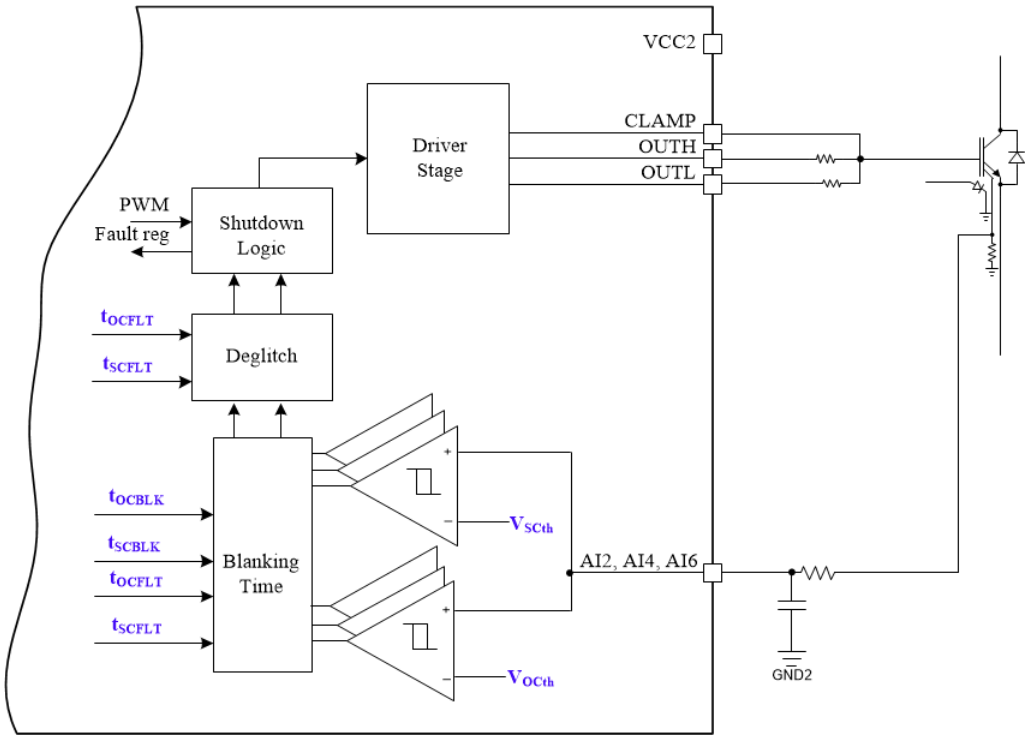

Figure 24. OC circuit configuration

3.10.3 Adjustable 2-Level or Soft Turn-Off

As mentioned in the previous sections, DESAT and OCP/SCP send back a fault indication and triggers the driver to turn off the IGBT or SiC MOSFET. The driver initiates either 2-level turn-off or soft turn-off to safely shut down the IGBT or MOSFET, preventing large voltage overshoot across the device as a result of the high current transient.

The two-level turn-off (2LTOFF) function limits the transistor current during shutoff during certain fault conditions. When 2LTOFF is triggered, the gate of the power transistor is controlled to operate the transistor in the linear region where the channel current is controlled by the voltage level on the gate terminal. The power transistor current is reduced by controlling the gate voltage to a intermediate voltage, or plateau voltage, (V2LOFF) for t2LOFF, and then ramping the gate down to turn the power transistor off. While 2LTOFF is active, OUTL sinks current to discharge the gate capacitor of the power switch to the plateau voltage. The plateau voltage level and duration are configurable. After holding the plateau voltage for the programmed time, the gate is discharged fully using the soft turn-off current or pulled low as normal with the OUTL driver. The soft turn off current can be enabled and level chosen in the Configuration Registers.

The soft turn-off (STO) function is another method of protecting the power transistors from OV damage because of parasitic loop inductance induced voltage spikes on VCE. The STO slows down the turn-off process to limit the di/dt rate, and limiting the loop inductance-induced voltage spikes. During STO, the OUTL drive strength is reduced to the threshold programmed using SPI. The STO function is enabled for SC/OC and/or DESAT faults.

The inverter benefits not only to prevent the damage or destruction of the power switches, but also prevents high-voltages from being applied to the motor windings, which can also reduce the lifetime of the motor itself.

3.10.4 Active High-Voltage Clamp

The active high voltage clamping feature protects power transistors from over-voltage damage during switching transitions, specifically turn-off, while reducing the power dissipated in the external TVS clamp diodes used to protect the power FET. The UCC5870-Q1 has a designated input pin, V_{CECLP}, that monitors the voltage during turn-off. When the VCE of the FET increases enough to turn on the external TVS diode, the RC network at the V_{CECLP} input is charged up. Once the voltage at V_{CECLP} reaches the clamp threshold ($V_{CECLPTH}$), OUTL drive strength changes from the normal pull-down strength (can be >15A) to the I_{STO} (soft turn-off) setting in order to slow down the turn-off and reduce the voltage overshoot. The high-voltage clamping remains active for a predefined time t_{VCECLP_HLD}. The OV condition is reported to a Status Register and, if unmasked, nFLT1 pulls low. The circuit implementation is shown in Figure 25.

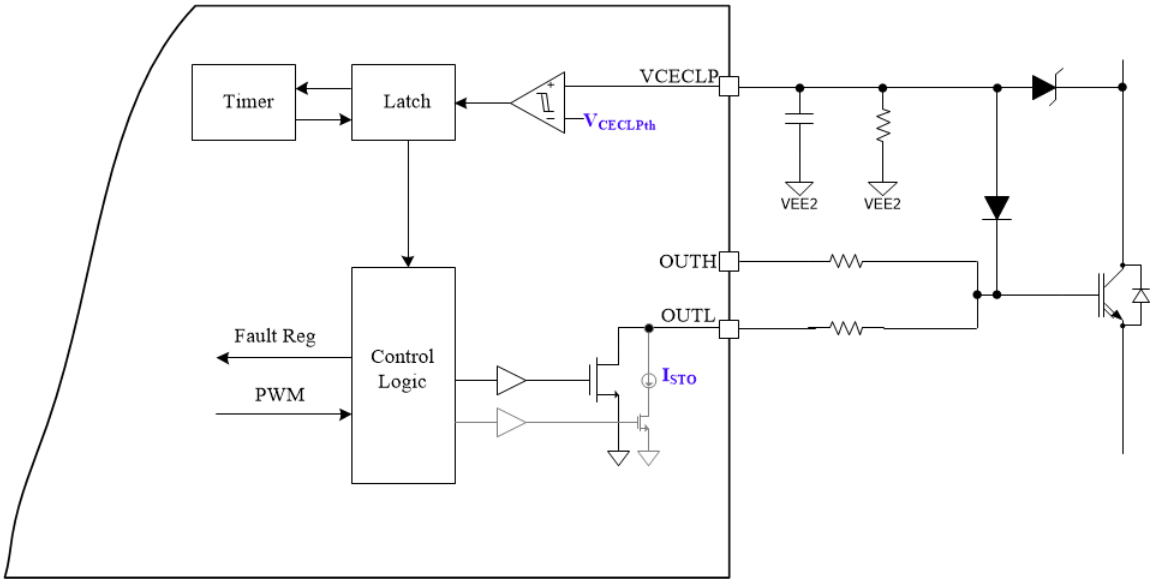

Figure 25. Integrated active high-voltage clamping configuration

3.10.5 Power Switch Gate Voltage (VGE/VGS) Monitoring

The V_{GTH} Monitor function is used to measure the gate threshold voltage of the power transistor during power up, shown in Figure 26. The gate voltage of the power transistor is monitored in order to check the integrity of the PWM signal channel, which helps to detect any communication failure due to failed isolation barrier or broken mechanical connection. The gate voltage is compared with the input PWM (IN+) signal, where the mismatch of the two signals causes a gate voltage monitor fault condition where the a Status bit is set, and the driver output is forced to the state defined by a Configuration Register. If unmasked, nFLT1 pulls low. Blanking time relative to OUTH is used to prevent false reporting of the gate voltage monitor error during driver transitions. During 2LTOFF transitions, the blanking time starts after the 2LTOFF plateau timer expires in order to prevent false gate monitor faults during the transition. Alternatively, the gate monitor fault may also be disabled during STO and 2LTOFF. The blanking time is adjustable via SPI. Additionally, the gate monitoring function may be disabled entirely.

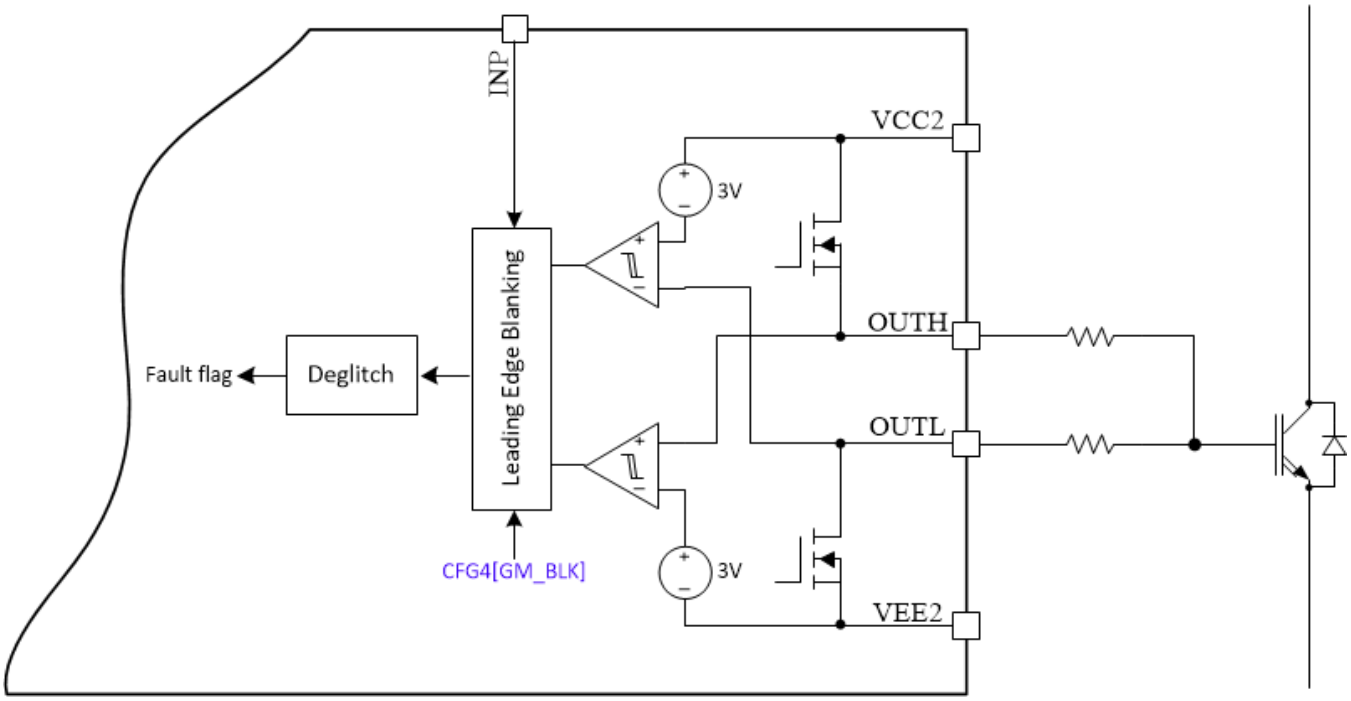

Figure 26. Gate voltage monitor

3.10.6 Gate Threshold Voltage Monitor

As a diagnostic feature, the gate threshold voltage monitor feeds back the measured threshold voltage to the MCU to judge the health of the power transistor, as described in Figure 27 and Figure 28. This is helpful in determining system lifetime and the potential for a failure later in time. The gate threshold voltage monitor measures the actual threshold voltage of the SiC MOSFET or IGBT. When enabled, the switch between DESAT and OUTH is turned on and a constant current source charges the gate capacitance of the power transistor, causing the gate voltage to ramp up gradually. Once the transistor channel starts to conduct, the gate voltage is naturally held at the threshold voltage level as the power transistor is in a diode configuration. After the blanking time, t_{dVGTHM}, the integrated ADC samples the gate voltage, and reports the measurement to the ADC Data Register.

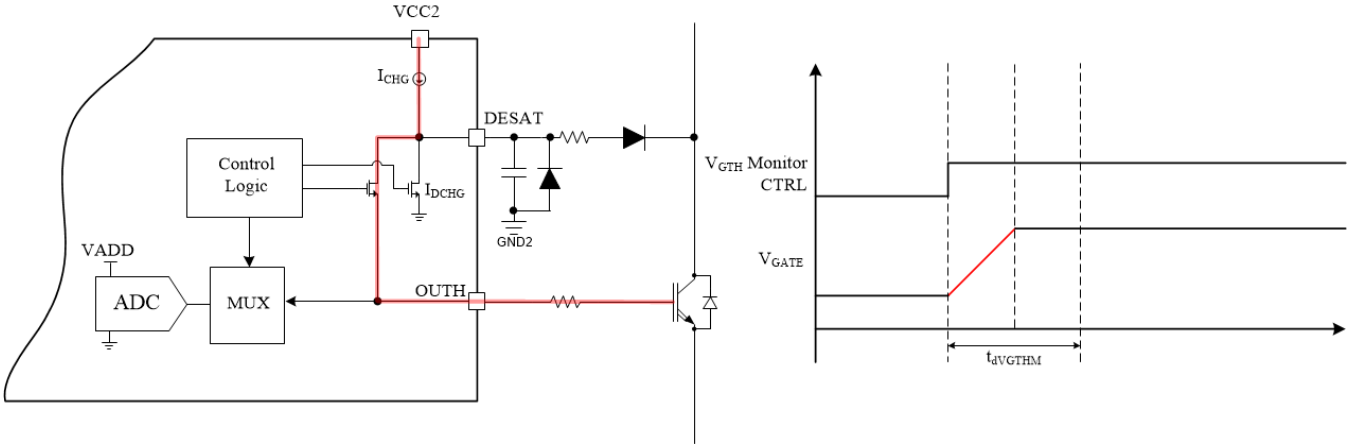

Figure 27. Gate voltage threshold monitoring while gate capacitor charges

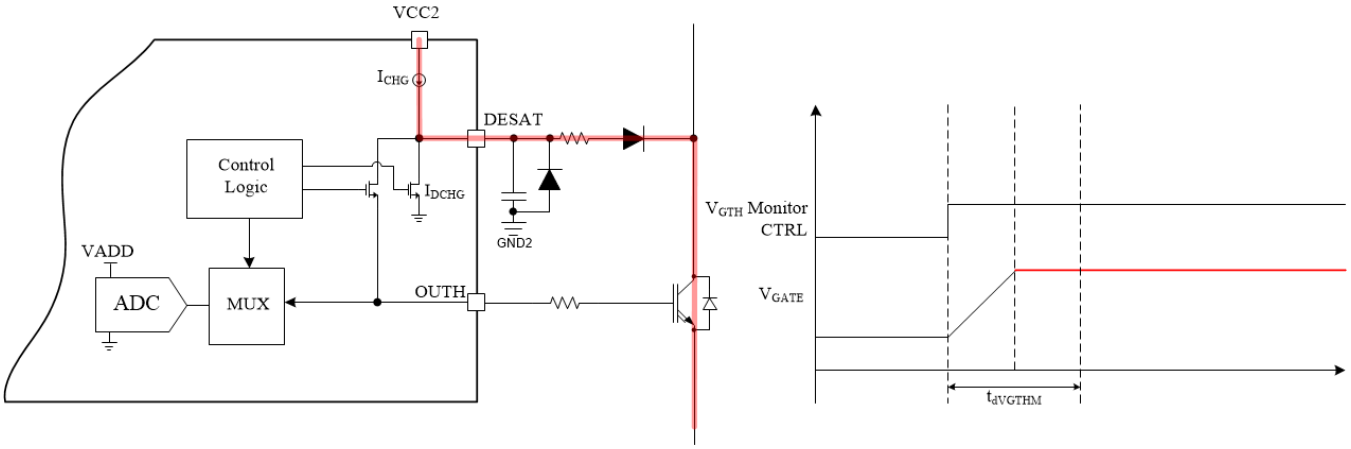

Figure 28. Gate voltage threshold monitoring while power transistor is in diode configuration

3.10.7 Power Switch Anti-Shoot-Through

The shoot through protection (STP) function provides an additional layer of protection from shoot through conditions due to incorrect PWM commands from MCU. The output of the driver uses IN+ and the complementary PWM signal provided to the IN- input to set the output state of the driver, as shown in Figure 29. Both the IN+ and IN- inputs are deglitched, which is programmable. Additionally, the output of the driver only goes high once the deglitched IN+ is high and for a programmable dead time after the deglitched IN- is low. If IN+ and IN- are both high at the same time, a shoot-through condition is detected, and is reported to a Status Register and, if unmasked, the nFLT1 output pulls low. The output of the driver is forced to the state defined by a Configuration setting. The STP function is disabled by setting the dead time to be 0 and connecting the IN- input low so the output simply follows IN+.

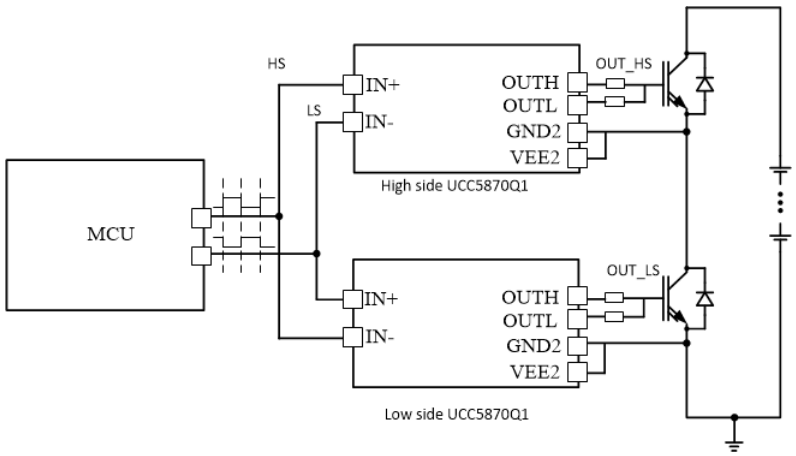

Figure 29. Shoot-through protection

3.10.8 Active Short Circuit (ASC)

The active short circuit (ASC) function allows the system to force the state of the power transistor regardless of the PWM input. The ASC interface is located on both the primary and secondary sides, depending on the architecture of the safety controller. For cases where the main MCU is not available due to fault or otherwise, a secondary control circuit drives the ASC_EN input high to force the output of the UCC5870-Q1 to the state defined by the ASC input, denoted as the HV Controller in Figure 30.

From system point of view, the implementation of ASC function is to control the inverter output to be a zero vector. The zero vector can be generated through two approaches: Main MCU or secondary control circuit. The ASC function is usually triggered when there is a system fault. If the fault is not a MCU fault, the MCU can implement diagnosis through the SPI interface and generate the appropriate zero vector based on fault type. If the fault happens in the MCU, then the secondary control circuit pulls the ASC_EN pin to be HIGH and suitable state on the ASC pin. With the ASC_EN pin pulled high, the driver output follows the state on the ASC pin. For the primary side, two dedicated inputs are available for the ASC control. The ASC control is also available on the secondary side using the AI5 and AI6 inputs. The driver is configured with the secondary ASC function using SPI. In this configuration, AI5 works as ASC_EN and AI6 is the ASC input. The primary and secondary ASC interfaces are shown in Figure 30.

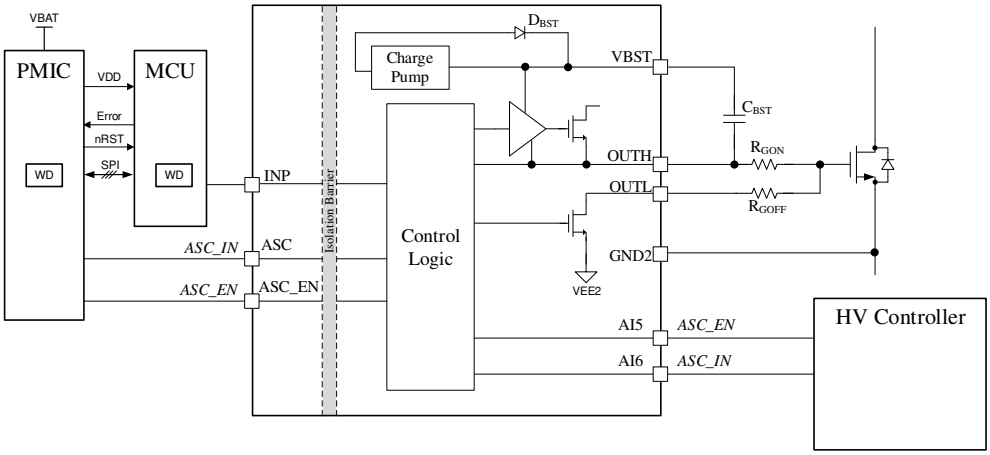

Figure 30. ASC primary and secondary side interfaces

3.10.9 Integrated Internal or External Miller Clamp

The Active Miller clamp (CLAMP) is used to prevent the power transistor from false turn-on due to Miller capacitance-induced current. The active Miller clamp adds a low impedance path between power transistor gate terminal and VEE2 to pull the gate of the external FET hard to VEE2, bypassing any external gate resistors. The Miller clamp engages when the OUTH pin falls below V_{CLPTH}, which is the threshold voltage that can be selected using SPI programming. The integrated internal Miller Clamp is shown in Figure 31. The CLAMP pin can also be configured to drive an external Miller Clamp FET if more pull-down strength is required, as shown in Figure 32. The external Miller Clamp FET also provides the ability to optimize placement of the clamp such that it is very close to the gate of the power transistor. Both options can be easily tested by configuring the output using SPI and making minor changes to the layout.

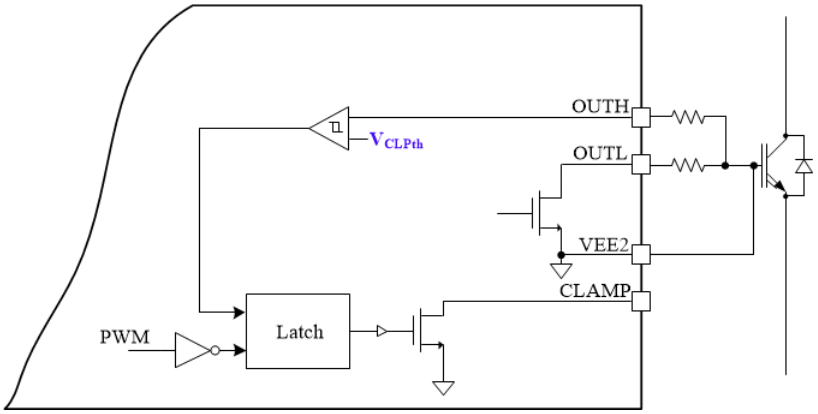

Figure 31. Integrated Internal Miller Clamp

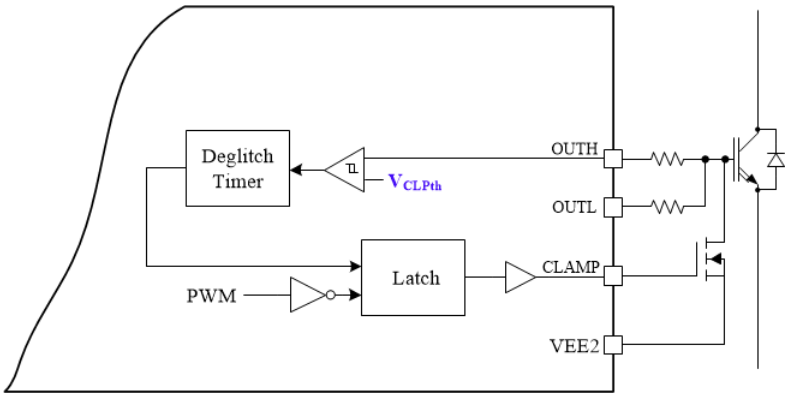

Figure 32. Integrated Driver for External Miller Clamp

3.10.10 Isolated Analog-to-Digital Converter

The isolated ADC can be used for a variety of purposes, as shown in Figure 33. Already mentioned are the OCP/SCP protection and ASC configurations. In addition to this, the temperature of the power modules can also be monitored by configuring specified AIx channels to bias external temperature sensors. This is described in the following section. Other potential uses for the ADC to enable a high level of system failure mode coverage would be DC link voltage monitoring through a resistor divider, and other DC levels. The 10-bit ADC has a full scale voltage range of 0V to 3.6V and has a total error of 1.5%. The reference voltage can be chosen as external or internal depending on accuracy requirements. The internal voltage reference has a 5% tolerance. The ADC conversions are aligned with the INP signal to ensure minimal noise coupling from the switching transients. All data is stored in the ADC data registered which can be read via SPI. There are three sampling modes available to ensure the least amount of switching noise in the measurement: Center aligned, Edge, and Hybrid modes.

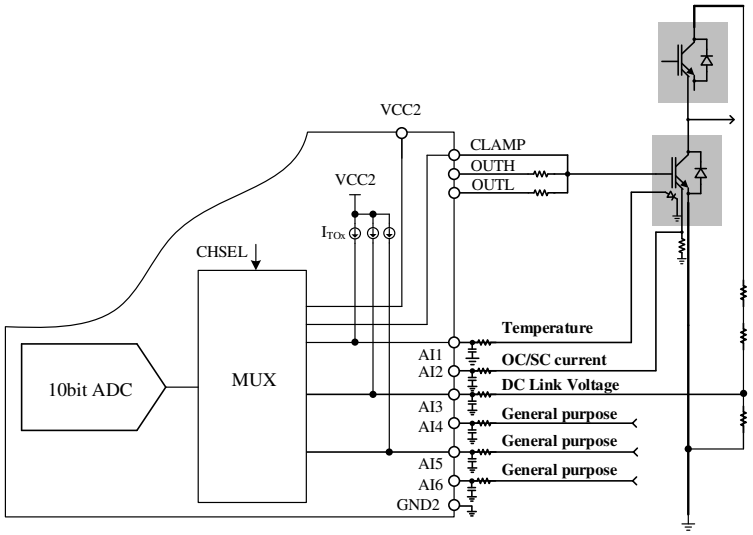

Figure 33. ADC implementation example

3.10.10.1 Temperature Monitoring of Power Transistor

UCC5870-Q1 designates three AIx inputs (AI1, AI3, AI5) to support thermal diode sensing for up to three power transistors sharing the same ground reference. An example with a single thermal diode measurement is shown in Figure 34. The temperature protection is intended for power transistors with integrated temperature sensing diodes in order to monitor the junction temperature, which can be an indication for the controller to discontinue to operate the inverter or as a mode of failure. The AIx input

provides a current that biases the integrated diode, and the voltage is monitored at the AIx input. The bias current can be enabled via SPI on one or all of the available AI pins. The temperature measurement is fed back into the ADC Data register, and a fault can also be configured for thermal shutdown (TSD) or thermal warning (TWN). The fault must exist for the deglitch time programmed before the fault is registered. The AIx pins can be enabled/disabled for temperature monitoring.

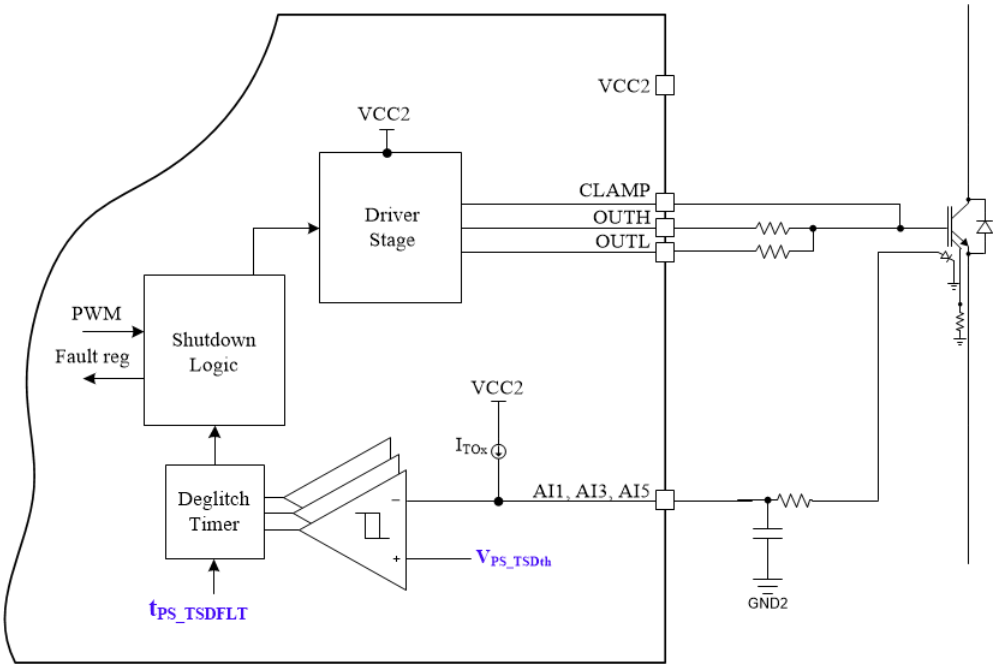

Figure 34. Power switch temperature monitoring

3.10.11 Short-Circuit Clamping

Integrated diodes protect the OUTH and CLAMP outputs during short circuit conditions. The short circuit clamping function clamps the voltages at the driver output (OUTH) and active Miller clamp (CLAMP) outputs to be slightly higher than VCC2 during power switch short circuit conditions. The clamped gate voltage limits the short circuit current and prevents the IGBT/MOSFET gate from overvoltage breakdown or degradation.

3.10.12 Active and Passive Pulldown

While VCC2 is unpowered, the gate of the external power switch his held off with a passive and active pulldown circuit. The passive pulldown continuous bleeds charge off the gate of the power transistor through a resistor. If the OUTL suddenly rises due to ramping VCC2 during power up, the active pull-down function pulls the IGBT/MOSFET gate to the low state.

3.10.13 Thermal Shutdown and Temperature Warning of Driver IC

The driver IC also has integrated thermal monitoring to prevent failure during overheating conditions. Both the primary and secondary sides of the driver utilize thermal warning and shutdown comparators to help mitigate damage due to high temperatures. When a thermal warning is detected on the primary side, the Status is set and, if unmasked, a fault is reported. If an over-temperature event is detected on the primary side, the device transitions to the RESET state where the driver output is held low. Once the device cools, the UCC5870-Q1 must be reconfigured. If a thermal warning is detected on the secondary side, the Status is set and, if unmasked, the fault is reported. When a thermal shutdown is detected on the secondary side, the driver is disabled, the Status is set and, if unmasked, the fault is reported. Once the driver cools and the fault clears, the UCC5870-Q1 must be reconfigured.

3.10.14 Clock Monitor and CRC

The UCC5870-Q1 integrates clock monitor functions to identify clock faults during operation. The Clock monitor detects internal oscillator failures such as: oscillator clock stuck high or stuck low and clock frequency out of range. The clock monitor is enabled during a power-up event after the power-on reset is released. The clocks on both the primary side and secondary side are monitored. In the event of a clock fault on the primary side, Status is set and, if unmasked, the fault output pulls low. The primary side clock monitor has no effect on the gate driver output state. In the event of a clock fault on the secondary side, the Status is set, and the driver output is forced to the state determined by the user-set Configuration, and, if unmasked, the fault output pulls low.

The clock monitor circuit also integrates a diagnostic that checks the integrity of the monitoring circuit. The diagnostic is run automatically during the start up process. Additionally, a simulated clock monitor fault can be generated by writing to the respective Control bits for the primary or secondary sides. When enabled, the diagnostics emulates clock failure that causes a clock monitor fault. During this self-test, the actual oscillator frequency is not changed.

Additionally, UCC5870-Q1 uses a cyclic redundancy check (CRC) to ensure data integrity for the configuration of the device while the driver output is active, the SPI communications (both transmitted and received), and the internal non-volatile memory that stores the trim information ensuring the performance of the device.

3.10.15 SPI and Register Data Protection

SPI input and output data integrity is monitored as well as register data content. This is to ensure proper communications and storage of data for setting driver parameters and functions.

When the UCC5870-Q1 transitions to the ACTIVE state, the contents of configuration and control registers are protected by CRC engine. The configuration CRC is enabled using the proper Configuration bit. The various registers protected by the CRC are outlined in the datasheet. The CRC fault detection is performed every t_{CRCCFG} (typically 1 ms). If the calculated CRC checksum for the configuration registers does not match the CRC checksum calculated upon entering the Active state, Status bits are set and, if unmasked, the nFLT1 output goes low. Additionally, for the secondary side CRC failure, the driver output is forced to the state pre-defined in a Configuration register. Diagnostics for the CRC check are also available. A Control Register can be commanded to induce a CRC error on the primary or secondary side.

The CRC that checks for SPI transfer are continuously updated as SPI traffic is received/sent. The CRC is updated with every 16-bits that are received. In this set of commands, the configuration is updated and compared on that command.

The SDI CRC checksum data is continuously calculated as SPI data frames are received. Once the MCU writes to the to CRC Data Transmission (TX) bits, this triggers a comparison of the data in the CRC TX bits with the internally calculated CRC. Once the comparison is complete, the CRC calculation logic is reset. When there is a mismatch between CRC TX data and CRC calculated internally, the Status bit is set and, if unmasked, the nFLT1 output pulls low and the output is set based on the pre-configured register setting.

The SDO CRC checksum is continuously calculated as data is clocked out of SDO. The resulting CRC is stored in the CRC Receive (RX) Data bits. The bits are updated whenever chip select, nCS, transitions from low to high. The CRC calculation logic is reset when the CRC RX bits are read.

After each power up, the UCC5870-Q1 performs a TRIM CRC check on the internal non-volatile memory on both the primary and secondary sides. If the calculated CRC checksum does not match the CRC checksum stored in the internal TRIM memory, Status bits are set and, if unmasked, the nFLT1 output goes low. Additionally for the secondary side CRC failure, the driver output is forced to the pre-defined state.

4 Isolated Bias Supply Architecture

Another important consideration in automotive traction inverter systems with regards to the gate drivers is the bias supply architecture. The bias supplies are used to provide isolated power used to drive each IGBT or SiC MOSFET. The reliability of the single or multiple isolated supplies is necessary to keep the inverter operational. The architectures of the gate driver bias supplies varies based on the required level of reliability. The bias supplies may be shared amongst multiple drivers (centralized), provided separately to each driver (distributed), or partially shared (semi-distributed).

Centralized bias supply architecture has the advantage of low component count, low cost, and generic control. However, the transformer for this architecture may be bulky, can suffer from common mode current, can result in complex PCB routing when shared amongst six drivers and does not inherently contain any redundancy.

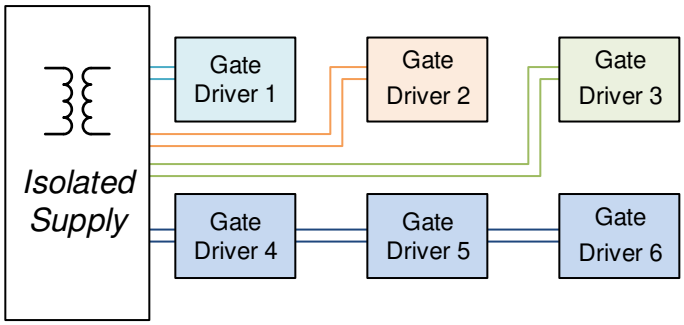

Figure 35. Centralized Bias Supply Architecture

The semi-distributed power consists of several transformers to generate the biases for various groups of drivers. For example, each high-side driver may be supplied with a separate transformer whereas all the low-side drivers may be shared. The advantage of this architecture is the simplicity of transformer construction and PCB layout, the ability to have higher power quality for each bias supply, the distribution of weight of the supplies' transformers, and the simplicity of control. The disadvantages include higher component count, higher cost, and still a lack of redundancy.

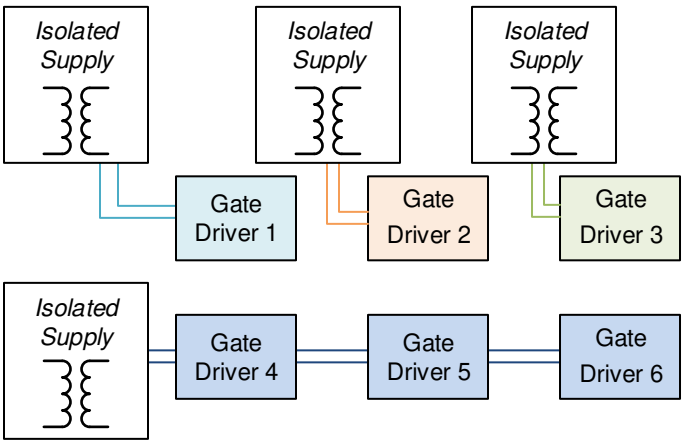

Figure 36. Semi-Distributed Bias Supply Architecture

Finally, the distributed power architecture provides a separate bias supply for each gate driver. Although it requires more components, resulting in higher cost, the advantages include a high level of redundancy, simplified layout and distribution of weight and better power quality.

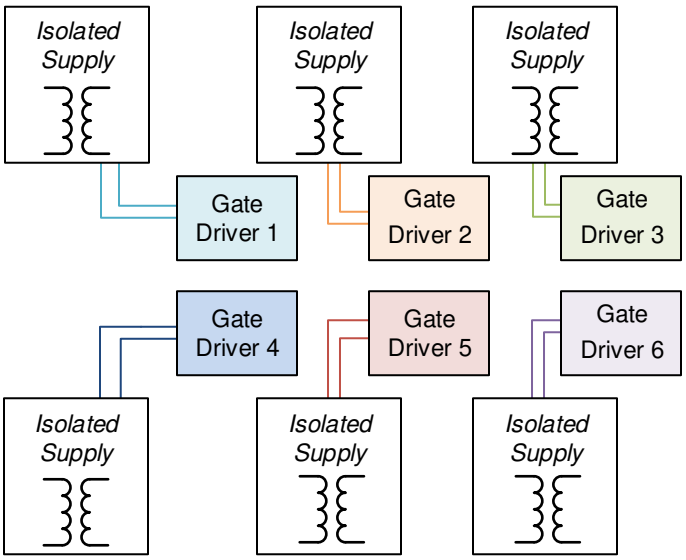

Figure 37. Distributed Bias Supply Architecture

For more information on bias supplies, please see TI's portfolio of high-voltage controllers and this reference design on bias supplies for HEV/EV traction inverters.

5 Summary

The complexity of electronics in electrified vehicles is ever-increasing with enhanced performance and safety regulations. The traction inverter contains some of the most critical components of the electric vehicle which have a direct impact on the drive of the motor. Integrated protection and monitoring features of UCC217xx-Q1 and UCC5870-Q1 drivers are shown to enable simplification of the system, as well as enhanced performance.

For more information, please see the product folders of UCC21732-Q1,UCC21750-Q1, UCC21710-Q1 and UCC5870-Q1 containing design help and technical documentation and visit the Power Management E2E Forum to get answers to your questions.

6 References

1. HEV/EV traction inverter power stage with 3 types of IGBT/SiC bias-supply solutions reference design
2. UCC217xx Family Driving and Protecting SiC and IGBT Power Modules and Transistor
3. Understanding the Short Circuit Protection for Silicon Carbide MOSFETs
4. SiC/IGBT Isolated Gate Driver Reference Design With Thermal Diode and Sensing FET
5. J. Drobnik and P. Jain, "Electric and hybrid vehicle power electronics efficiency, testing and reliability," 2013 World Electric Vehicle Symposium and Exhibition (EVS27), Barcelona, 2013, pp. 1-12.
6. Haizhong Ye, Y. Yang and A. Emadi, "Traction inverters in hybrid electric vehicles," 2012 IEEE Transportation Electrification Conference and Expo (ITEC), Dearborn, MI, 2012, pp. 1-6.
7. S. Jain and L. Kumar, "Fundamentals of Power Electronics Controlled Electric Propulsion," in *Power Electronics Handbook*, M. H. Rashid, Ed. United Kingdom: Butterworth-Heinemann, 2018, pp. 1023-1065.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2019) to A Revision	Page
• Added additional detail throughout.	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265