

What we covered in Electronics - 1 :-

- Abstract from semi-conductor physics
- Diodes
- BJT and BJT Amplifiers
- MOS Device Physics
- Single stage MOS Amplifiers
 - * Common Source Stage with resistive load
 - * CS Stage with diode connected load, source degeneration also
 - * Source follower
 - * Common Gate Stage

What we will study here :- → Operational Amplifier Basics

- Advanced Circuit Topologies
 - * Cascade structure
 - * Current mirrors
 - * Differential pair
- Speed Limitations : frequency response
- Feedback Circuits

Unit - 1 : Operational Amplifier Basics

→ Was invented to perform mathematical operations (specifically differential equations) easily.

Example Airplane in sky experiences various forces modelled in differential equation. To simulate these equation operational Amplifier was used. It solve arithmetic and various calculus operations hereafter termed as operational Amplifier.

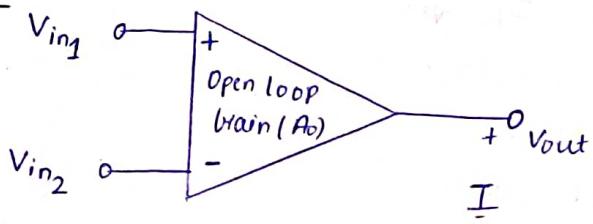
→ If we can visualize a complex transistor circuit as OP-Amp then analysis becomes easier.

Op-Amp Basics :-

$$V_{out} = (V_{in_1} - V_{in_2}) A_o$$

where A_o is open loop gain.

Let $V_{in_1} = \text{some voltage}$
 $V_{in_2} = 0$



$$V_{out} = A_o V_{in_1}$$

That's why it is called Non-inverting terminal.

Let $V_{in_1} = 0$ and $V_{in_2} = \text{some value}$
 then, $V_{out} = -V_{in_2} A_o$

(a most used op-Amp)

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Modern Integrated Op-Amp

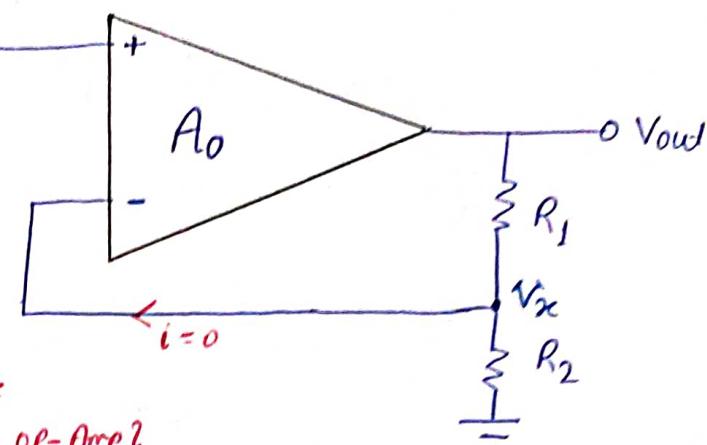
Ideal Op-Amp

Open loop gain (A_o)	∞	100,000	50-100
Input Imp.	∞	Several M Ω	Several M Ω
Output Impedance	0	< 100 Ω	Several K Ω
Speed (Bandwidth)	∞	1.5 MHz	Several kHz
Power dissipation	0	80 mW	5-10 mW
Cost	0	< \$1	$\approx 10^{-5}$

Non-Inverting Amplifier :- Signal to amplify is given at Non-Inv. terminal

As from Basic of Op-Amp: $(V_{in} - V_x) A_0 = V_{out}$

$$\text{And } V_x = \frac{R_2}{R_1 + R_2} V_{out}$$



{ we assume that current input to op-Amp terminal = 0, Because of very High Input Resistance of Op-Amp }

$$\text{So, } \left[V_{in} - \frac{R_2}{R_1 + R_2} V_{out} \right] A_0 = V_{out}$$

$$\Rightarrow A_0 V_{in} = V_{out} \left[1 + \frac{A_0 R_2}{R_1 + R_2} \right]$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \frac{R_2}{R_1 + R_2} A_0}$$

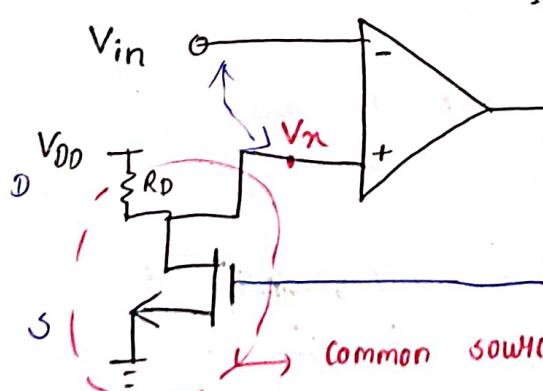
a) if Op-Amp Ideal then $A_0 = \infty$

$$A_v = 1 + \frac{R_1}{R_2}$$

b) if $\frac{R_2}{R_1 + R_2} A_0 \gg 1$ then also $A_v \approx 1 + \frac{R_1}{R_2}$

Ques: Find gain of given topology: given Ideal Op-Amp.

brain depends only $\frac{R_1}{R_2}$ ratio. Suppose temp changes \pm also $\frac{R_1}{R_2}$ maintained because R_1, R_2 both have almost same fluctuation. In this way very precise gain.



$V_{out} \rightarrow$ positive terminal is feedback with V_{out} after mos.

But in actual its negative feedback because mos inverts V_{out}

Common source stage for which input = V_{out} and output = V_x

$$V_x = -g_m R_D V_{out}$$

$$\Rightarrow V_{in} = -g_m R_D V_{out}$$

Because of Ideal-Amp + neg feedback virtual ground is there so $V_x = V_{in}$

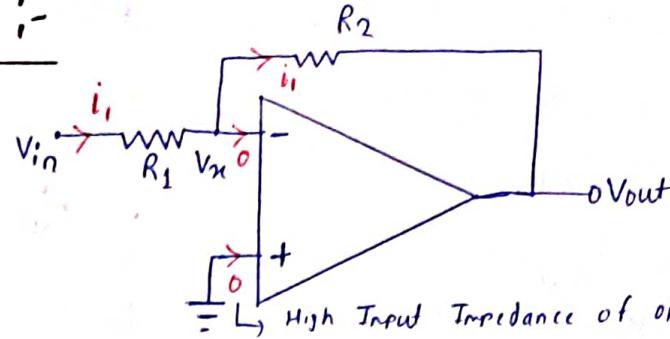
$$A_v = \frac{V_{out}}{V_{in}} = \frac{1}{-g_m R_D}$$

Inverting Amplifier :-

Basic of op-Amp:

$$(0 - V_N) \times A_0 = V_{out}$$

$$\Rightarrow V_N = \frac{-V_{out}}{A_0}$$



And, $i_1 = \frac{V_{in} - V_N}{R_1}$

And $i_1 = \frac{V_N - V_{out}}{R_2}$

$$\frac{V_{in} + V_{out}/A_0}{R_1} = \frac{\frac{-V_{out}}{A_0} - V_{out}}{R_2}$$

$$V_{out} \left[\frac{1}{A_0 R_1} + \frac{1}{A_0 R_2} + \frac{1}{R_2} \right] = -\frac{V_{in}}{R_1}$$

$$A_V \Rightarrow \frac{V_{out}}{V_{in}} = \frac{1}{(R_2 + R_1 + A_0 R_1) (-R_1)} \quad \cancel{A_0 R_1 R_2}$$

$$A_V = \frac{-1}{\frac{R_1}{R_2} + \frac{R_1 + R_2}{A_0 R_1}}$$

Again if $A_0 = \infty$

then $A_V = -\frac{R_2}{R_1}$ OH $\frac{R_1}{R_2} \gg \frac{R_1 + R_2}{A_0 R_1}$

Integrator :-

Inverting Configuration

it is :

$$A_V = \frac{-1}{\frac{1}{A_0} + \left(1 + \frac{1}{A_0} \right) R_1 C_1 s} \Rightarrow \text{pole not at origin}$$

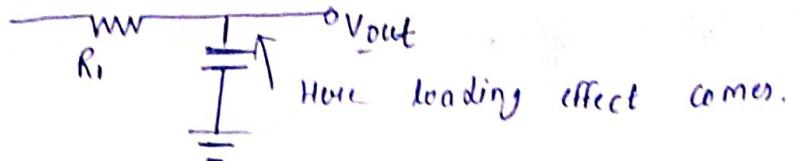
If A_0 is very high :

$$A_V = \frac{-1}{R_1 C_1 s} \text{ so it is a Integrator. Let us see time domain expressions.}$$

$$\text{So, } \frac{-dV_{out}}{dt} C_1 = \frac{V_{in}}{R_1}$$

$$V_{out} = \frac{-1}{R_1 C_1} \int V_{in} dt$$

Side note:



Hence loading effect comes.

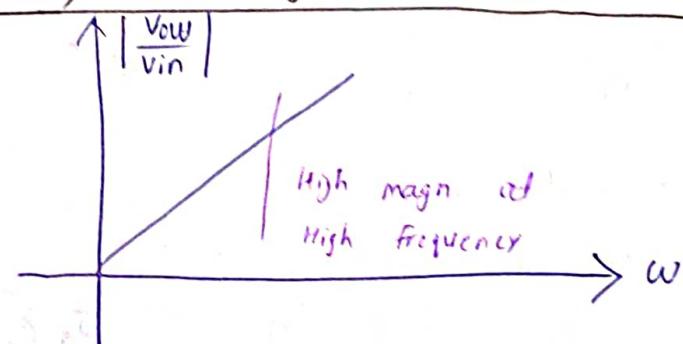
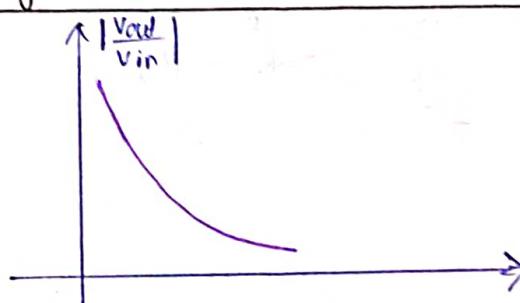
→ But this integration does not work in lab because of offset and all.

Differentiator :-

$$\frac{V_{out}}{V_{in}} = -\frac{Z_2}{Z_1} \quad (\text{Ideal OP-Amp})$$

$$= -\frac{R_1}{1/C_1 s} = -R_1 C_1 s$$

Magnitude and plot (freq. Response) of Integrator & differentiator :-

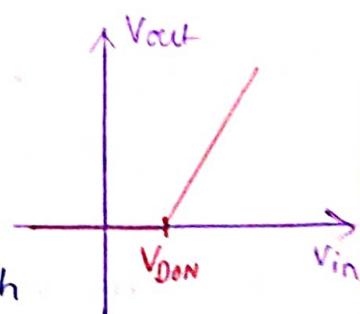
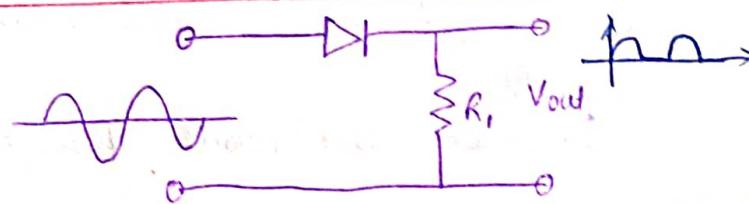


→ Generally noise have high frequency and differentiator amplifies high frequency, so we rarely use differentiator. In most practical application we use Integrator.

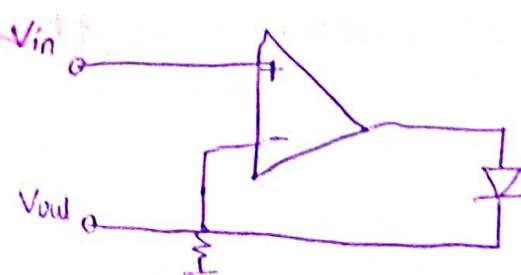
Non-linear function Using Op-Amp :-

1) Simple Rectifier & Precision Rectifier :-

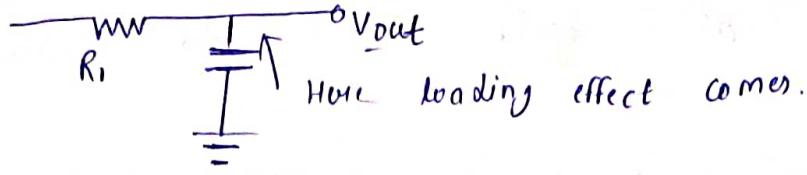
$$V_{DOL} = 700 \text{ mV}$$



But suppose we want to rectify a signal which have Amplitude below 700mV and diode will never on in this situation so To rectify those type of Signals we use precision rectifier.



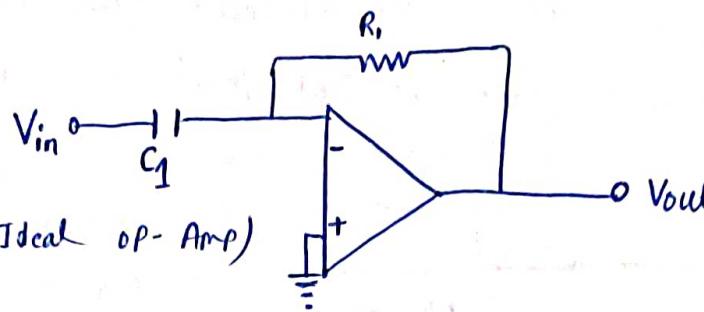
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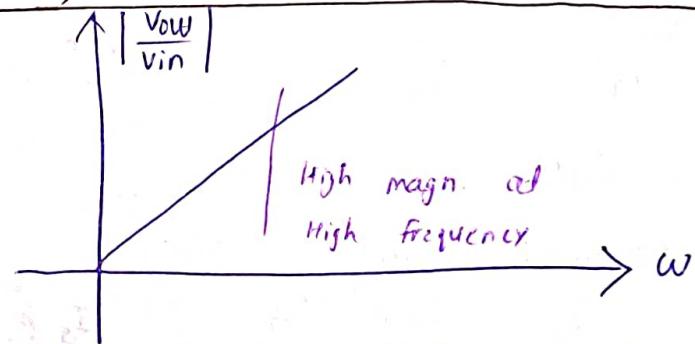
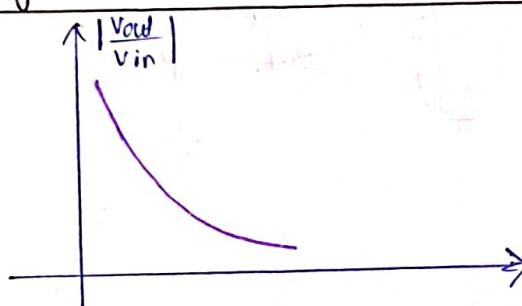
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Magnitude and Plot (freq. Response) of Integrator & Differentiator :-

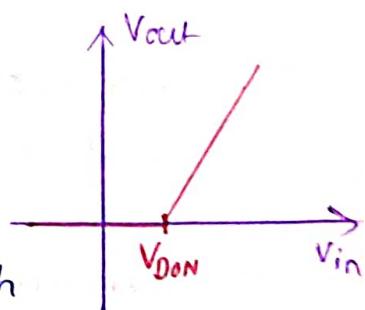
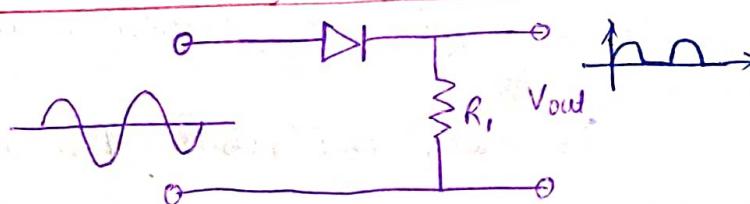


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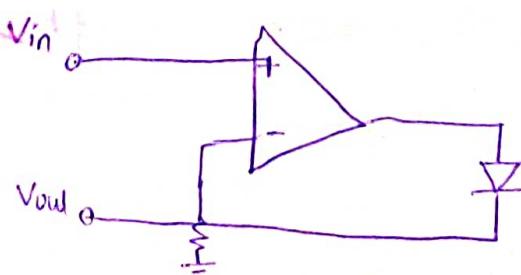
Non-linear Function Using Op-Amp :-

1) Simple Rectifier & Precision Rectifier :-

$$V_{DOL} \approx 700mV$$

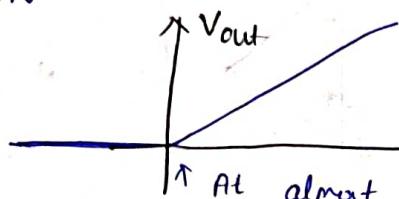


But suppose we want to rectify a signal which have Amplitude below 700mV and diode will never on in this situation so To rectify those type of Signals we use precision rectifier.



When $V_{in} > 0^+$, Because of high A_o , Diode gets ON, instantly
and $V_{out} = V_{in}$.

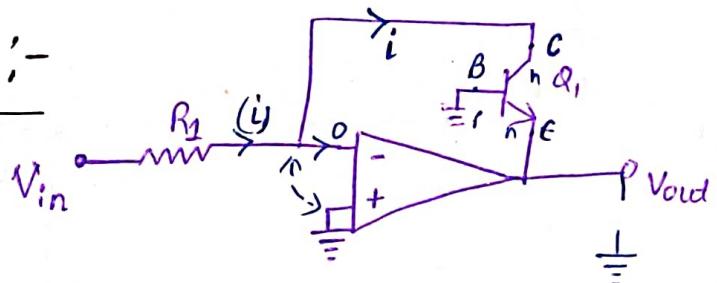
When $V_{in} < 0^-$, voltage at OP-Amp output terminal = high $8-10$
so diode gets off. so Basically Hi, High A_o provides
Diode $V_{D_{ON}}$ even if Input Signal is just 0^+ .



At almost zero input voltage (0^+), diode gets $V_{D_{ON}}$, because of High A_o .

Logarithmic Amplifier :-

$$i = \frac{V_{in} - 0}{R_1} = \frac{V_{in}}{R_1}$$



$$V_{EB} = V_{out}$$

The transistor current i given by:

$$I_{C1} = I_s e^{V_{BE}/V_T} = I_s e^{-V_{out}/V_T}$$

And I_{C1} is nothing but i so

$$\frac{V_{in}}{R_1} = I_s e^{-V_{out}/V_T}$$

$$\Rightarrow V_{out} = -V_T \ln \frac{V_{in}}{I_s R_1}$$

If $V_{in} < 0$; \ln can not take negative value.

$i = -\infty$, Not possible for BJT so output of Transistor not defined.

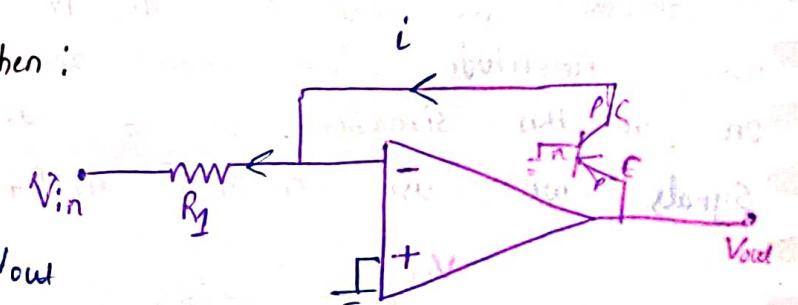
if we use pnp transistor then:

$$i = -V_{in}/R_1$$

$$i = I_s e^{+V_{EB}/V_T} \quad \because V_{EB} = V_{out}$$

$$\therefore \frac{-V_{in}}{R_1} = I_s e^{V_{out}/V_T}$$

$$V_{out} = V_T \ln \left(\frac{-V_{in}}{I_s R_1} \right)$$



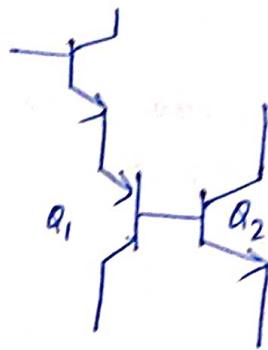
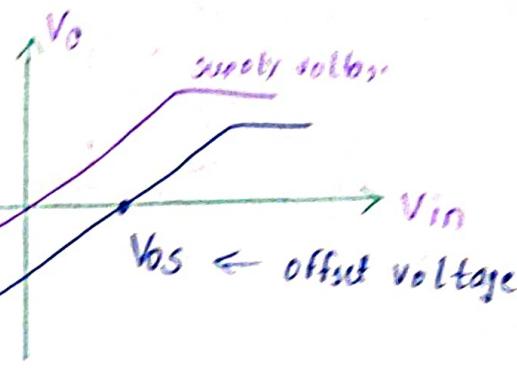
Here V_{in} cannot be positive

Op-Amp Imperfections :- (Non-Idealities)

- * Finite gain
- * DC offsets
- * Input bias currents
- * Finite speed

DC offsets :-

Op-Amp is made of Transistors.
There are various symmetrical structures in Op-Amp such as

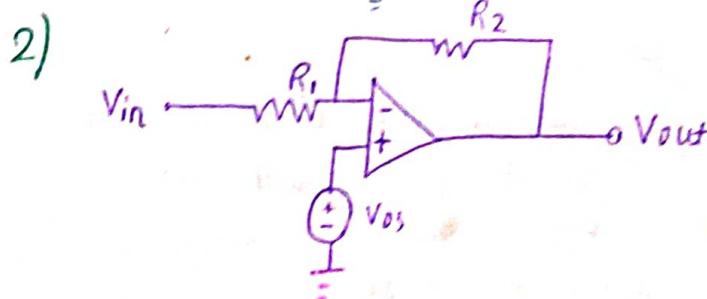
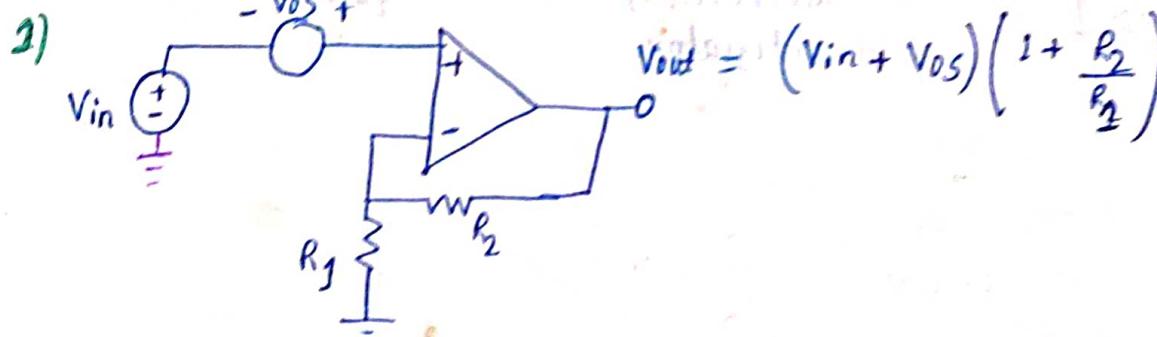


a_1, a_2 should be perfectly matched but due to some manufacturing defects it's not the case so there is offset.

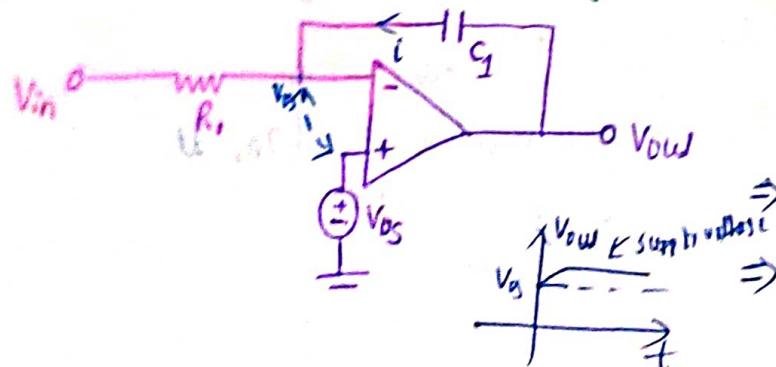
$\rightarrow V_{os}$ is random in sign.

\rightarrow It can be placed in source with either inact

Effect of Offset on Amplifier :-



3) Effect of offset on Integrator :-



Also the reason ideal integrator not worked in lab.

For a moment disable $V_{in} = 0$.

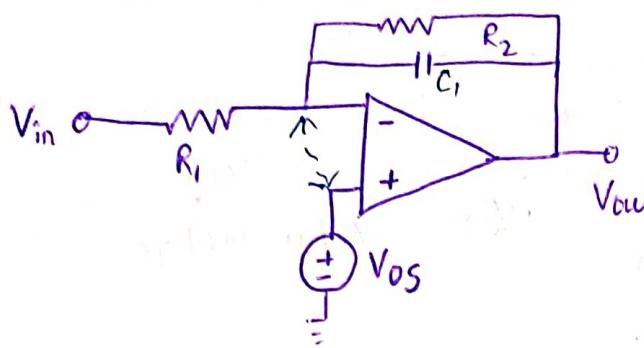
then

$$V_{out} - V_{os} = \frac{1}{C} \int i dt \xrightarrow{R_1} \frac{V_{os}}{R_1}$$

$$V_{out} = V_{os} + \frac{V_{os}}{R_1 C} t$$

$\Rightarrow V_{OS}$ is integrated by capacitor and with time output is saturated to supply voltage of Op-Amp. so V_{in} is not integrated and integrator fails.

To fix the circuit :-



\Rightarrow Assuming $A_o = \text{very high}$.

$$\frac{V_{out}}{V_{in}} \approx \frac{-R_2}{(R_2 C_1 s + 1) R_1}$$

For a moment disable V_{in} and see the effect of V_{OS} .

If $V_{in} = 0$:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) V_{OS}$$

At steady state
 $C \rightarrow \text{open}$

so current $\frac{V_{OS}}{R_1}$ prefers to flow thru R_2 rather than thru C_1 .

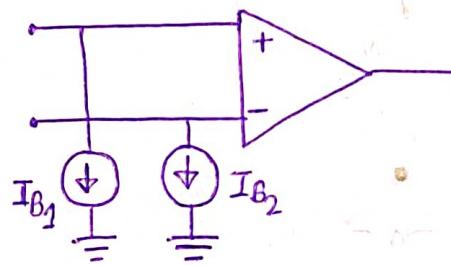
Ideal integrator Transfer function:

$$\frac{-1}{s R_1 C_1}$$

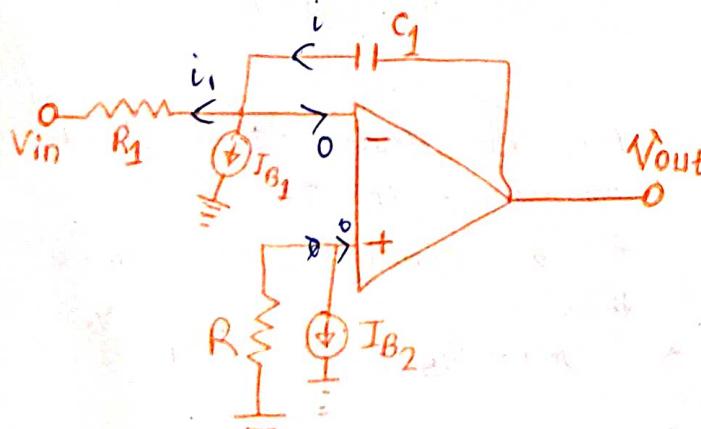
so To be a good integrator, the circuit requires that $|R_2 C_1 s| \gg 1 \Rightarrow$ for sufficiently high frequencies, its a good integrator.

#) Input Bias Currents:-

* BJT type Op-Amp have some Bias current Because in $I_B \neq 0$ in BJT.



* Input Bias Currents in Integrator:-



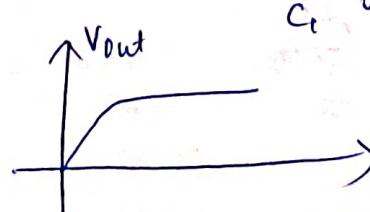
To see the effect of Bias current just disable V_{in} by $V_{in} = 0, R = 0 \rightarrow$ first take it

K.C.L at node:

$$\Rightarrow i = i_1 + I_{B1}$$

$$\Rightarrow i = I_{B1}$$

$$\Rightarrow V_{out} = \frac{1}{C_1} \int I_{B1} dt$$



Here also integrator saturates. But if we choose $R = R_1$, then both I_{B_1} effect & I_{B_2} effect cancelled, assuming $I_{B_1} \approx I_{B_2}$. But this will be not reliable solution because I_{B_1}, I_{B_2} little difference can saturate OP-Amp. so using a resistor R_2 in parallel with C_1 will be reliable solution.

Speed Limitations: What we expect frequency of OP-Amp v/s Reality:

So our model of OP-Amp $H(s) = \frac{A_0}{s + s_0}$ is

true only at low frequencies. Actually we should use first order model for this:

$$H(s) = \frac{A_0}{1 + \frac{s}{\omega_0}}$$

so in all derivation Inverting, Non-inverting Amplifier replace A_0 to see $H(s)$ effect.

Slew rate:

what we think is: The moment we give V_{in} , output

should settle at $V_{out} = \left(\frac{R_2}{R_1} + 1 \right) V_{in}$

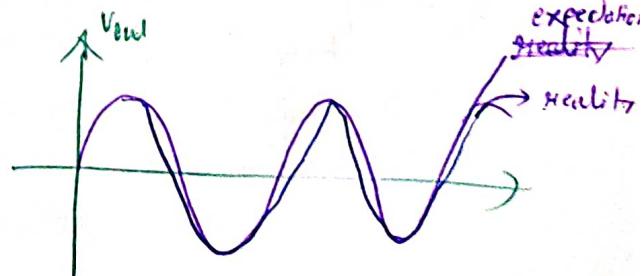
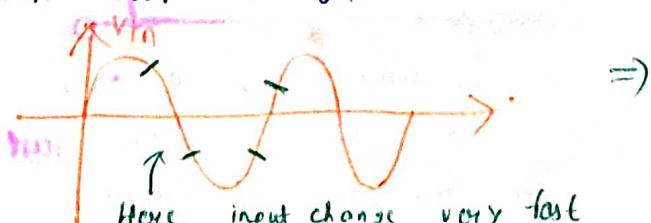
But in actual gain is model as first order equation so,

$$V_{in3} > V_{in2} > V_{in1}$$

But if V_{in} is very high then the fast change

is not possible and settling time does not improve it have some limitations. Slew rate is basically maximum allowed rate of change of OP Amp's output-voltage.

Example:



so if slew rate not that much OP-Amp will unable to reflect this fast change in output

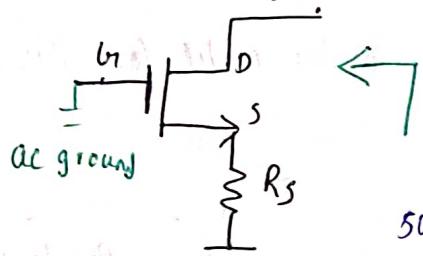
Unit : 2 Advanced Circuit Topologies

Introduction :- Mosfet works as a current source in saturation region. Due to channel length modulation it's not perfect current source and that's why there is a associated output resistance H_0 .

→ For Ideal current source Internal resistance = ∞

→ H_0 works as Internal resistance here. If somehow we increase this output resistance (works as internal resistance) then our current source will get better.

Source with Degeneration is used for this purpose.



We know in this topology
$$R_{out} = (1 + g_m H_0) R_S + H_0$$

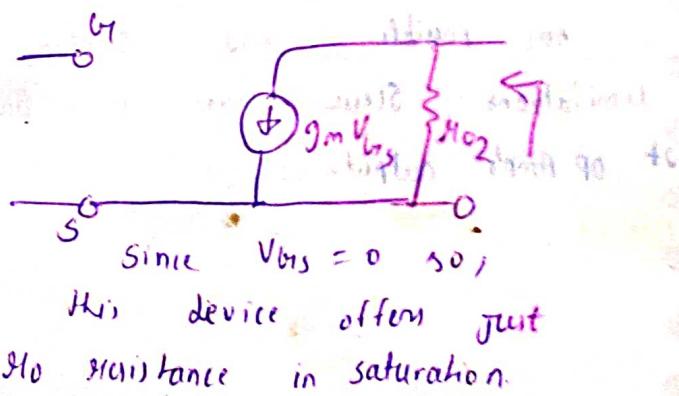
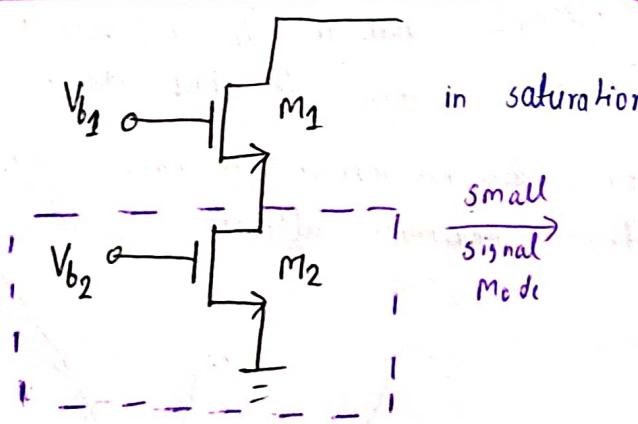
so it becomes better current source.

But as $I_D \neq$ Drop across $R_S \neq$ so

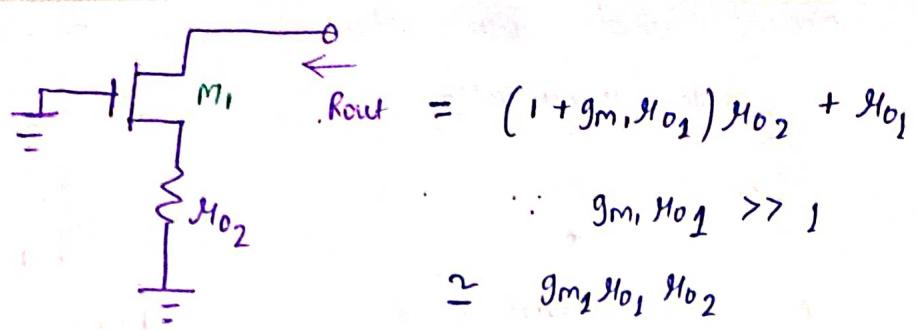
The device may be out of saturation. so we need a device in place of R_S which does not follow ohm's law. Here is the idea we introduce BJT's or MOSFET's in place of R_S . And these devices are called Cascode Current Source.

Cascode Current Source :-

MOS and Bipolar type cascodes
Current needs to be same in both device, and both are biased in saturation region.



30. The fig is:



$$R_{out} = (1 + g_m M_{O_1}) M_{O_2} + M_{O_1}$$

$\because g_m, M_{O_1} \gg 1$

$$\approx g_m M_{O_1} M_{O_2}$$

Ques. What if magically M_{O_1}, M_{O_2} doubled but I_D same.

I_D same so M_{O_1}, M_{O_2} same.

But $g_m = \sqrt{\frac{2 I_D \mu_n C_{ox} W}{L}}$

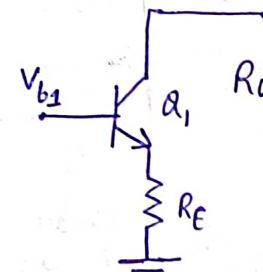
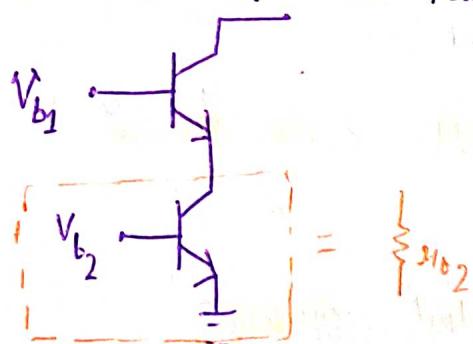
So $g_m, \text{new} = \sqrt{2} g_m$ Hence R_{out} is increased by $\sqrt{2}$ factor.

Bi-polar Cascode Current Source :-

In Source with degeneration stage (Emitter)

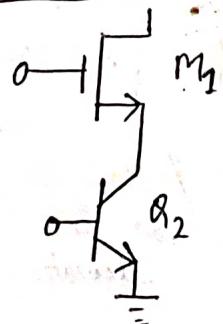
BJT also have internal i/p resistance \downarrow

In Cascode connection we Basically Use a BJT in place of R_E .

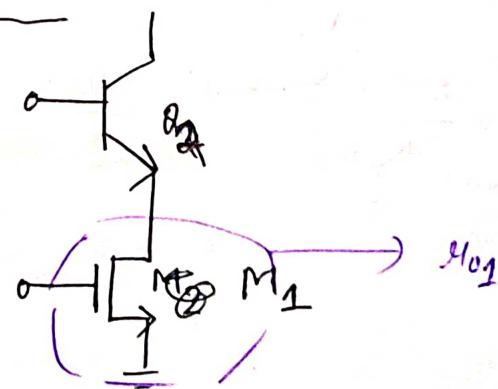


$$\text{So, } R_{out} = (1 + g_m M_{O_1}) (M_{O_2} || H_{\pi_1}) + M_{O_1}$$

Ques. Identify better current source :- Given $M_{O_1} = M_{O_2}$



same BJT



$$R_{out} = (1 + g_m M_{O_1}) M_{O_2} + M_{O_1}$$

$$R_{out} = (1 + g_m M_{O_2}) (M_{O_1} || H_{\pi_2}) + M_{O_2}$$

Since: MOS $g_m <$ BJT g_m (Generally)

And $M_{O_2} > M_{O_1} || H_{\pi_2}$ So The better current source will depend on exact values.

Till now what we studied are N-type Current sources.



Node (Higher voltage)

N-type Current Source

V_{DD} (High voltage)

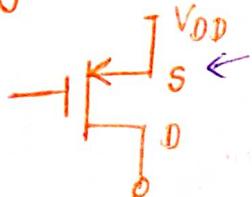


Node (Coming to node)

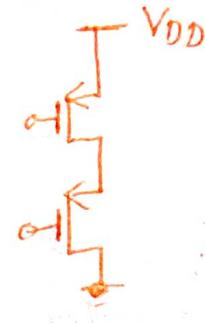
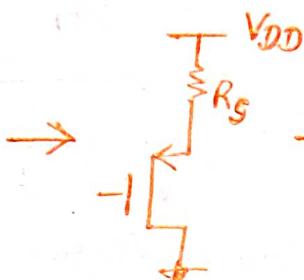
P-type Current Source

[For this we use p-type devices]

Forming of p-type Cascodes :-

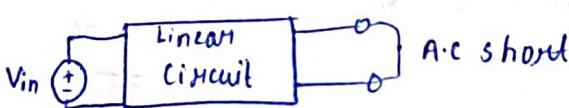
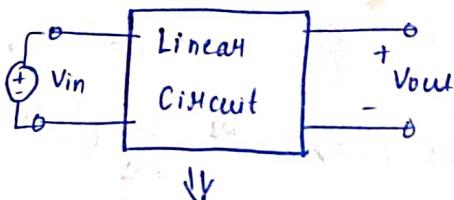


We have to degenerate source so Resistor will come here



Generalized Concept of Transconductance :-

$$b_{im} = \frac{I_{out}}{V_{in}}$$

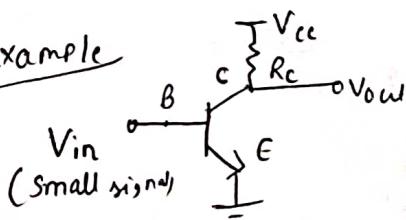


For whole circuit we use capital b_{im} . small g_m is derived for BJTs & MOS devices internal Transconductance.

Voltage Gain Calculation new style:

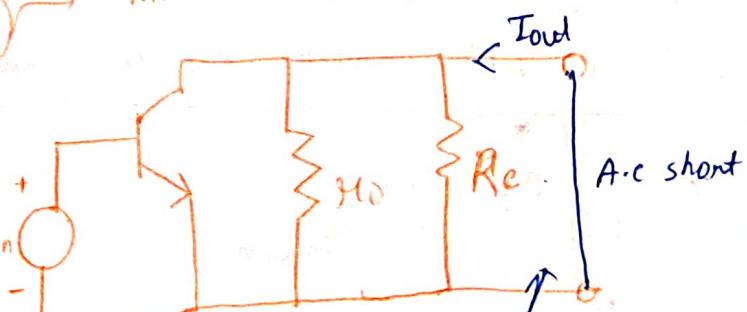
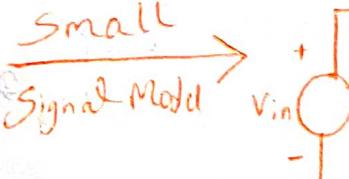
$$A_V = -b_{im} R_{out} \quad \text{Thevenin output resistance}$$

Example



Early voltage V_0

Small Signal Model



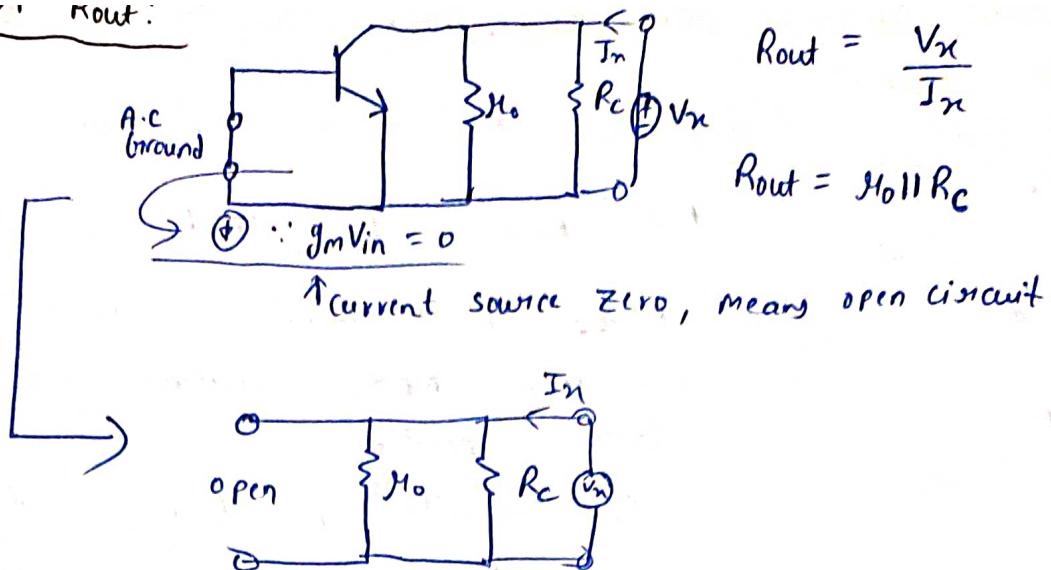
$$b_{im} = \frac{I_{out}}{V_{in}}$$

for b_{im} calculation

And H_O , R_C have no current (ac short) when ac short

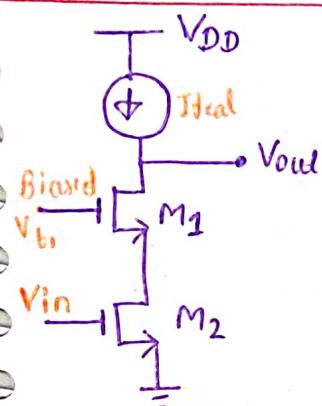
$$b_{im} = \frac{g_m V_{in}}{V_{in}} = g_m$$

Which was quite obvious also because overall circuit have no current division path in input so its b_{im} same as Transistor's g_m



∴ $A_{v\text{circuit}} = -g_m (R_c || R_o)$ → same as calculated in electronics -1.

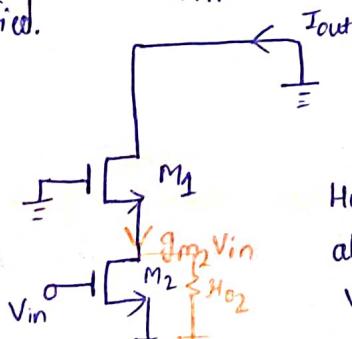
MOS Cascode Amplifier :-



(i) Calculation of b_{im} of Circuit:-

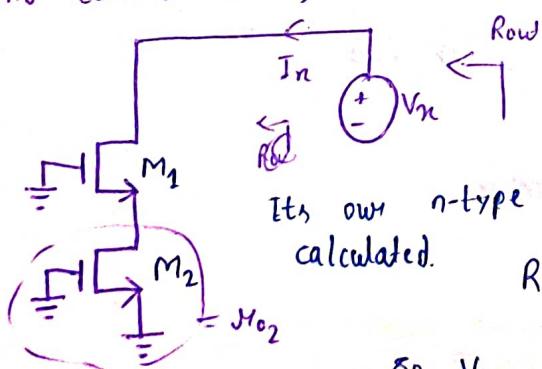
→ First we must know that Both mos are biased in saturation region.
→ For b_{im} calculation, make A.c short-circuit and find $\frac{I_{out}}{V_{in}}$. Note V_{in} is signal to amplified.

A.c short so V_t , also shorted. and Current source open circuit



Calculation of R_{out} :

Now all the independent voltage sources are shorted, and current sources are open.



It's own n-type cascode source for which R_{out} we already calculated.

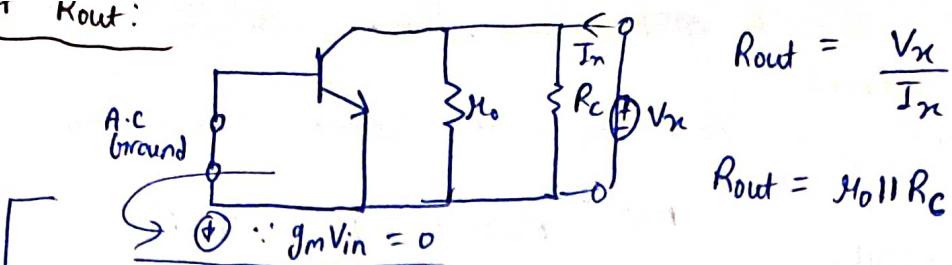
$$R_{out} = (1 + g_{m1} R_{o1}) R_{o2} + R_{o1}$$

$$\Rightarrow \frac{I_{out}}{V_{in}} \approx g_{m2} = b_{im}$$

So overall g_{m2} equals b_{im}

$$\therefore \frac{V_o}{V_{in}} = A_v = -b_{im} R_{out}$$

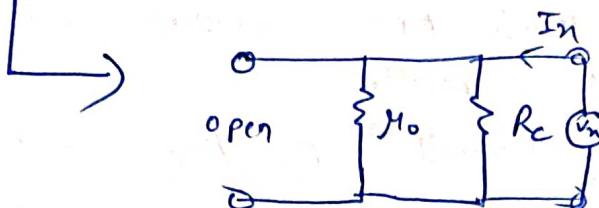
→ But that somehow, current source (Jideal) also needed to Implement



$$R_{out} = \frac{V_x}{I_n}$$

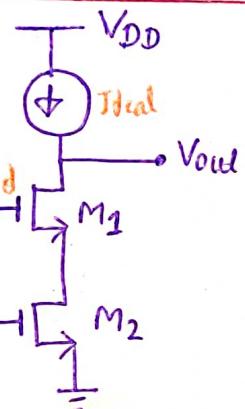
$$R_{out} = R_o \parallel R_C$$

↑ current source zero, means open circuit



∴ $A_{v, \text{circuit}} = -g_m (R_C \parallel R_o)$ → same as calculated in electronics - 1.

MOS Cascode Amplifier :-

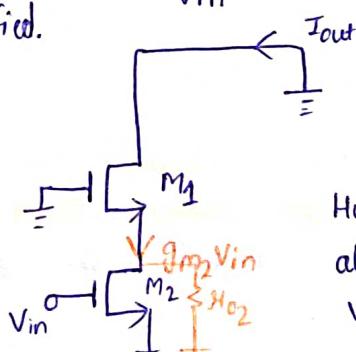


(i) Calculation of b_{im} of circuit:-

→ First we must know that Both mos are biased in saturation region.

→ For b_{im} calculation, make A.C short circuit and find $\frac{I_{out}}{V_{in}}$. Note V_{in} is signal to amplified.

A.C short so V_B also shorted. and Current source open circuit

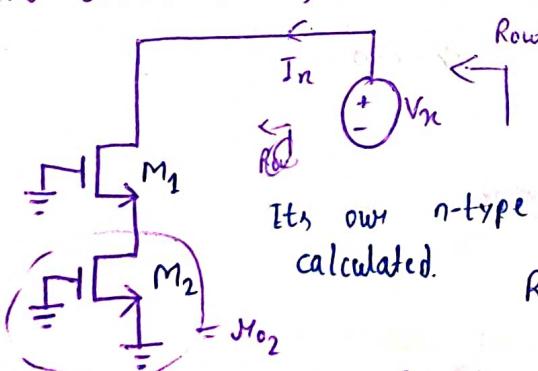


However some amount of current also goes in M_{O2} but that is very less. so,

$$g_{m2} V_{in} = I_{out}$$

$$\Rightarrow \frac{I_{out}}{V_{in}} \approx g_{m2} = b_{im}$$

so overall g_{m2} equals b_{im}



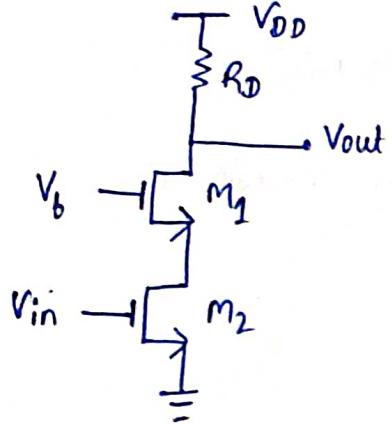
It's our n-type cascode source for which R_{out} we already calculated.

$$R_{out} = (1 + g_{m1} R_{O1}) R_{O2} + R_{O1}$$

$$\therefore \frac{V_o}{V_{in}} = A_v = -b_{im} R_{out}$$

→ But that somehow, current source (Ideal) also needed to implement

Suppose we use a resistance there, then let us see
what happens.



so bias of circuit still same.

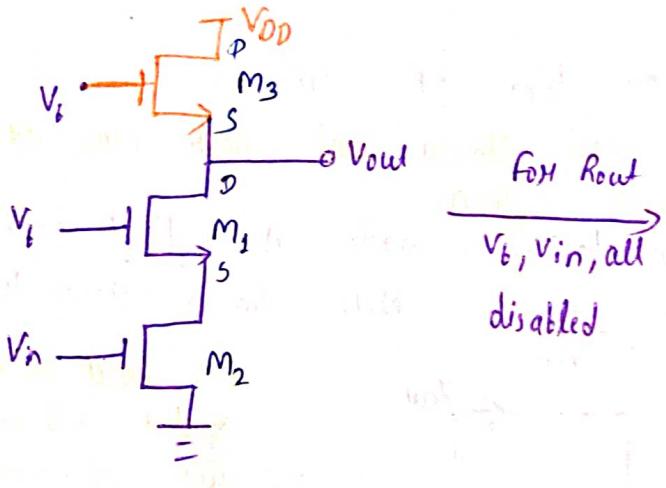
$$\text{But } R_{\text{out}} = R_{\text{cascode}} \parallel R_D$$

because while calculating R_{out} , R_D and cascode NMOS structure will come in parallel.

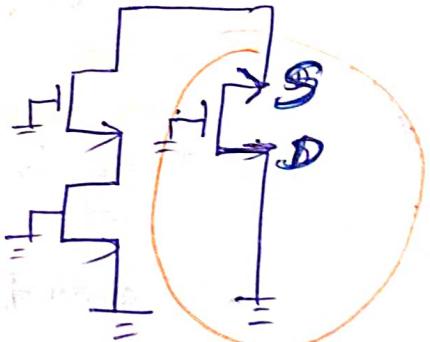
so generally R_D low, so R_{out} is even more low because of parallel.

Hence gain reduced.

Now suppose we use N-type MOS in place of R.



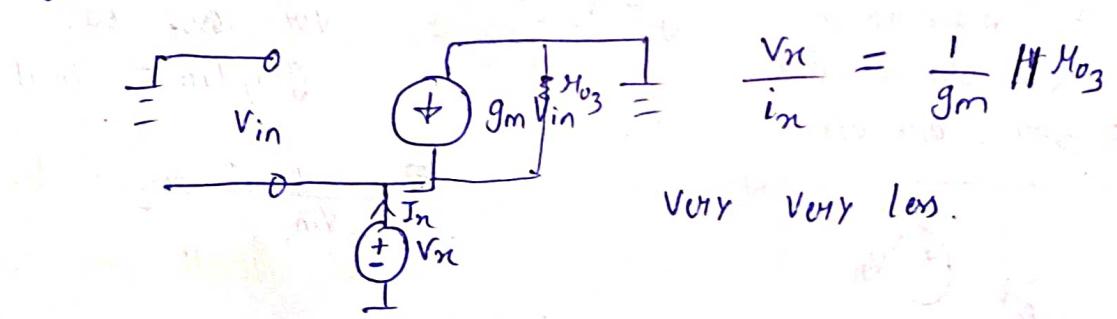
For R_{out}
 $V_b, V_{\text{in}}, \text{all}$
disabled



For this mos we want

output resistance at drain terminal.

Making small signal model for that.



Very very less.

so it will reduce gain. further.

Now situation is like

Here we want current source

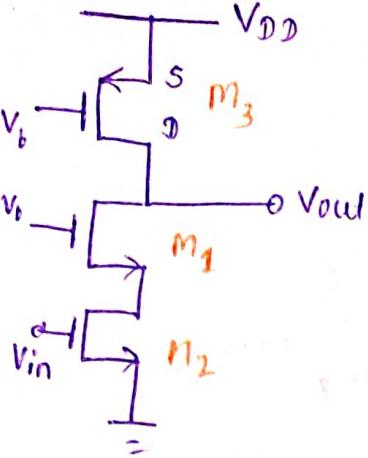
so p-type current

Node source will be bat here.

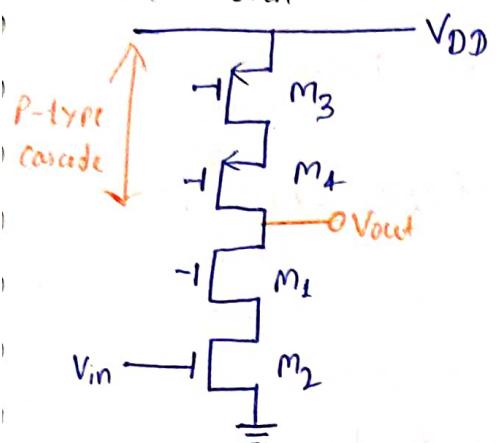
so we can use p-type MOS in saturation. And if we use cascaded p-mos then we will get even more gain.

All are biased in Saturation Region.

$$A_V = -g_{m_2} \left[\frac{1}{2} \left(1 + g_{m_1} H_{o_1} \right) H_{o_2} + H_{o_1} \right] / H_{o_3}$$



Suppose we use Cascode Amplifier with cascode load then gain will even more high.



$$A_V = -g_{m_2} \left[R_{\text{cascode}} \parallel R_{p\text{-cascode}} \right]$$

$$R_{\text{cascode}} = \left(1 + g_{m_1} H_{o_1} \right) H_{o_2} + H_{o_1}$$

$$R_{p\text{-cascode}} = \left(1 + g_{m_4} H_{o_4} \right) H_{o_3} + H_{o_4}$$

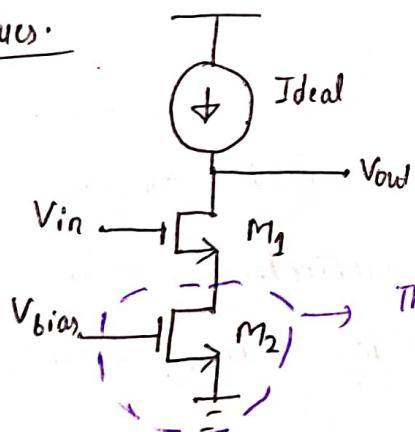
{ Here M_3 work as generation resistor }

→ BJT counterpart will also have same expression.

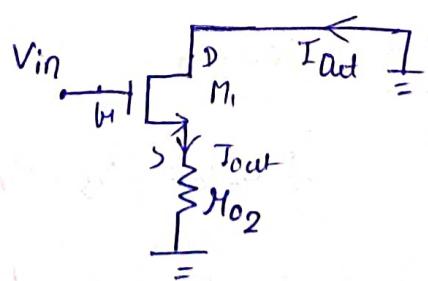
Here In MOS, $H_{o_1} \approx \infty$ but in BJT it have some finite value so take care of that.

Ques.

We have given Input signal to cascaded gate H_{o_1} . What about A_V ?



This is biased in saturation region so basically H_{o_1} will just offer H_{o_1} resistance to A.c small signal model. Fij for overall bim calculation



Assuming channel length modulation in $M_1 = 0$

$$\therefore H_{o_1} = \infty$$

Here $b_{im} = \frac{I_{out}}{V_{in}}$ and here V_{bias} voltage of Mos-1 is not V_{in} so applying K.V.L

$$V_{in} = V_{DS2} + I_{out} R_{O2}$$

$$8 g_m V_{DS2} = I_{out}$$

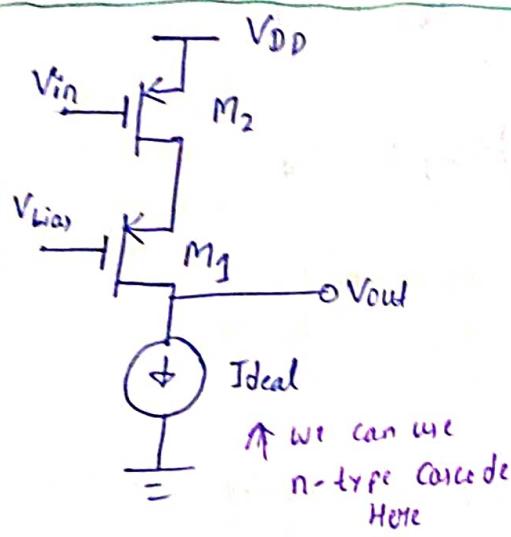
$$\Rightarrow V_{in} = \frac{I_{out}}{g_{m1}} + I_{out} R_{O2}$$

$$\Rightarrow V_{in} = I_{out} \left[\frac{1}{g_{m1}} + R_{O2} \right] \Rightarrow \frac{I_{out}}{V_{in}} = \frac{1}{\frac{1}{g_{m1}} + g_{O2}}$$

$\therefore b_{in} = \frac{1}{g_{m1}} + R_{O2} = \frac{g_{m1}}{1 + g_{m1} R_{O2}}$

* The voltage gain from gate of the cascode device to output is very low!

MOS Cascode Amplifier with p-type Input :-



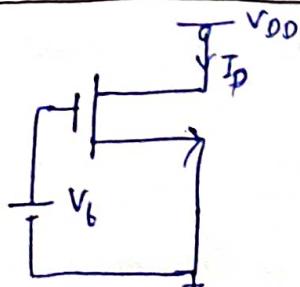
$$A_{le} = -g_{m2} R_{out}$$

$$\text{where } R_{out} = (1 + g_{m1} R_{O1}) R_{O2} + R_{O1}$$

Current Sources :-

We need current sources those are unaffected from voltage across it and also can provide same current in a vast temperature range.

Problems in MOS Current Sources :-



Mos in Saturation

Region

$$I_D = \frac{1}{2} \mu_n C_{ox} (V_b - V_{Th})^2$$

- Issues:
- (i) μ_n is temperature dependent
 - (ii) V_{Th} is temperature dependent
 - (iii) V_b is generated using resistive bias and that is also temperature dependent

Bolden Current Source: Using Bandgap circuit (Beyond His course) we make a current source that provides reference current such that it is constant in a vast range of voltage across it and temperature variation.

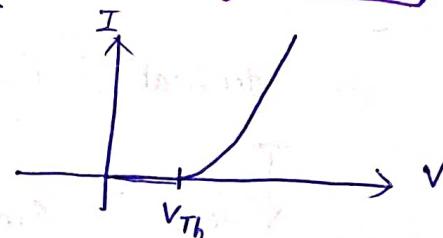
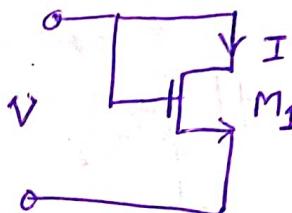
→ Suppose we need many current sources, then if we use a separate bolden current source everywhere then it will be very costly so we need a circuit which can copy current and these are called CURRENT MIRROR CIRCUIT.

Evolution of Current Mirror Circuit :-

(1) Diode connected Device:

if M_1 is on ($V > V_{Th}$), it is in saturation. And

$$I = \frac{1}{2} \mu_n C_o x \frac{W}{L} (V - V_{Th})^2$$

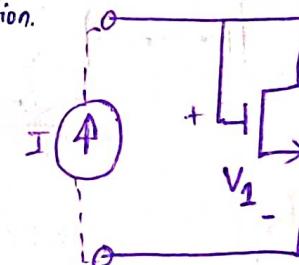
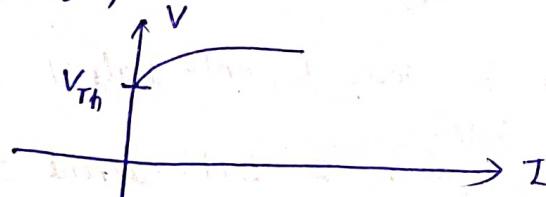


(2) Diode Connected device supplied by Current source:-

This current forcibly makes MOS in saturation.

At $I = 0$; MOS in cut off

At $I = 0^+$; MOS in saturation instantly

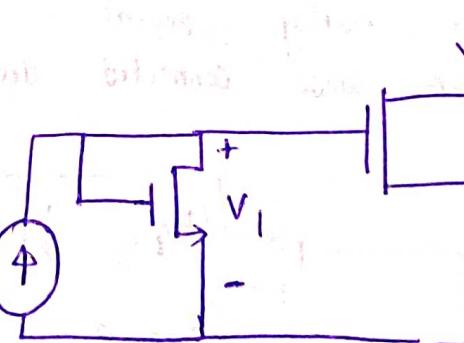


$$V = \sqrt{\frac{2I}{\mu_n C_o x \frac{W}{L}}} + V_{Th}$$

(3) Current Mirror:-

Suppose V_{Th} of Both MOS is same:

$$I_{out} = \frac{1}{2} \mu_n C_o x \left(\frac{W}{L}\right)_2 \left[V_1 - V_{Th}\right]^2 I_{in}$$



$$I_{out} = \frac{1}{2} \mu_n C_o x \left(\frac{W}{L}\right)_2 \left[\sqrt{\frac{2 I_{in}}{\mu_n C_o x \left(\frac{W}{L}\right)_1}} + V_{Th} - V_{Th} \right]^2$$

Here V_1 works as V_{DS} of MOSFET-2.

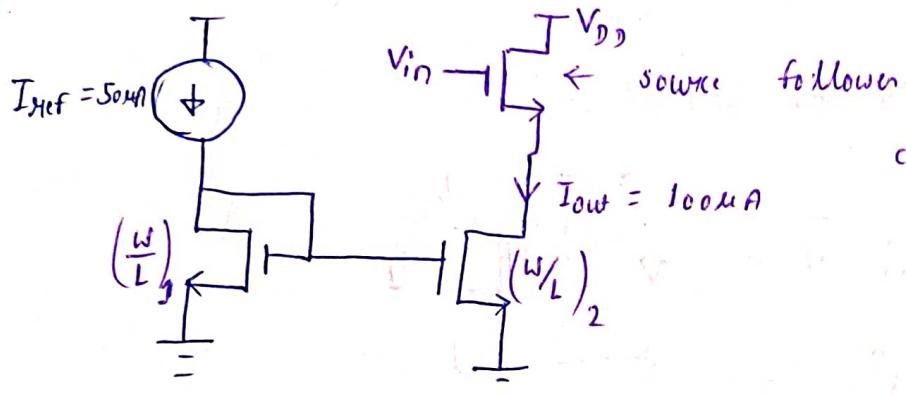
$$I_{out} = \frac{(\frac{W}{L})_2}{(\frac{W}{L})_1} I_{ref}$$

We always choose $L_1 = L_2$
and w is our design parameter.

L : Basically Technology Constant

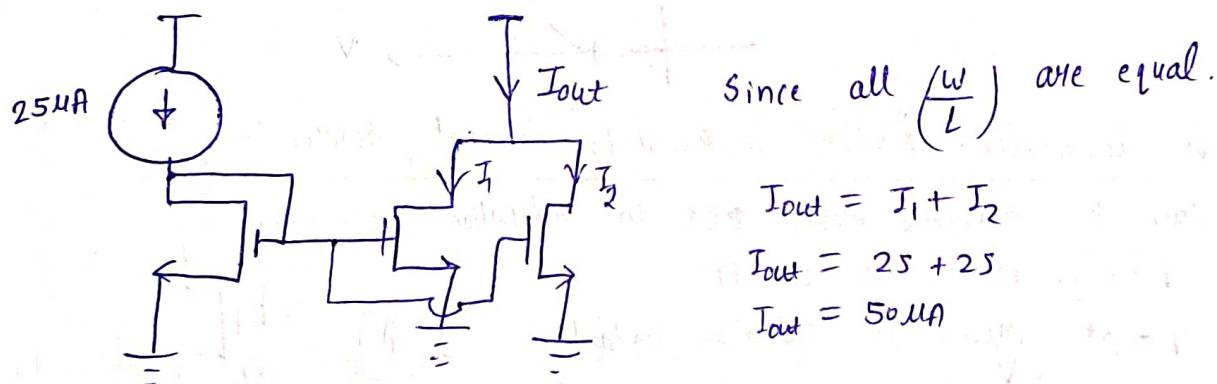
$$I_{out} = \frac{w_2}{w_1} I_{ref}$$

Ques.1 A circuit includes source follower biased at 100mA and have a reference current of 50mA.



$$\text{choose } (\frac{W}{L})_2 = 2(\frac{W}{L})_1$$

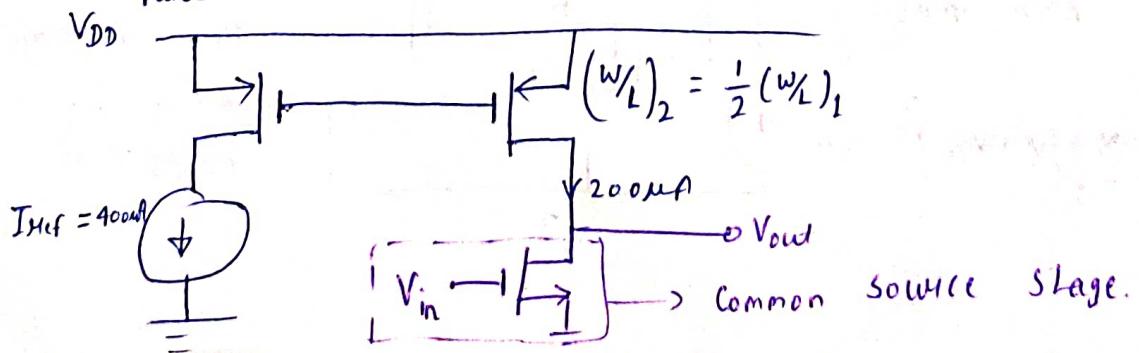
Ques.2 All MOSFETs are identical. Find I_{out} .



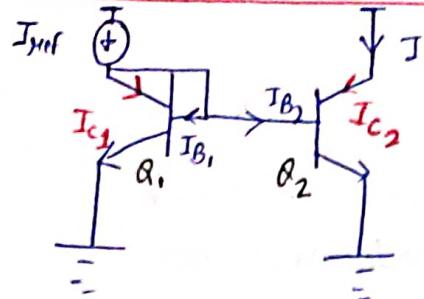
Proper Scaling :- Always choose the same L , only scale w .

Ques.3 An NMOS Common Source stage requires a load current source equal to 200mA. We have a reference current source equal to 400mA. Use p-type current mirror.

→ There is nothing special in p-type current mirror. Just use p-type diode connected device and put I_{ref} at appropriate place.



Bi-Polar Current Mirrors :-



Both BJT's are Biased
in Active mode

$$I_{C1} = I_{S1} e^{\frac{V_{BE}}{V_T}}$$

$$I_{C2} = I_{S2} e^{\frac{V_{BE}}{V_T}}$$

Both BJT's have same V_{BE} .

$$\frac{I_q}{I_{C2}} = \frac{I_{S1}}{I_{S2}}$$

In MOS current mirror, bias current = 0

But here Base requires a little current.

$\therefore I_{ref} = I_{C1} + I_{B1} + I_{B2}$

Let Both B_1, B_2 have same internal current gain.
(or) same β .

$\therefore I_{C1} = \beta I_{B1} \approx \beta I_B$ } If Both are matched
Transistor then $I_{S1} \approx I_{S2}$

$$I_{C2} = \beta I_{B2} \approx \beta I_B$$

$\therefore I_{ref} = I_{C1} + 2 I_B$

$$\Rightarrow I_{ref} - 2\beta I_B = I_{ref} = \beta I_B + 2 I_B = I_B (\beta + 2)$$

$\therefore I_{ref} = I_B (\beta + 2)$

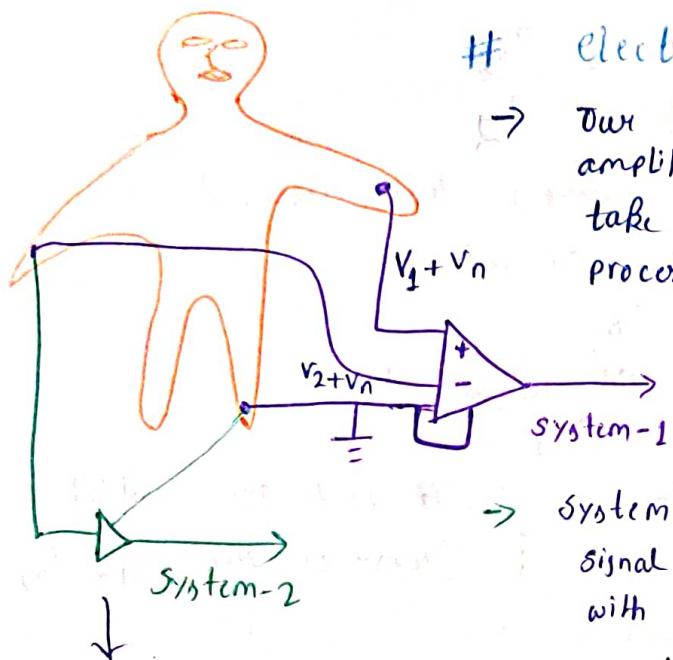
$$I_{ref} = \frac{I_{C2} (\beta + 2)}{\beta}$$
 And I_{C2} is nothing but
own I_{out} .

$\therefore I_{C2} = \frac{\beta}{\beta + 2} I_{ref}$

$$I_{out} = \frac{\beta}{\beta + 2} I_{ref}$$

Differential Amplifiers :-

Problem of Noise Coupling :- There is electricity in our house. In India it have frequency of 50 Hz. let us take a real world example to understand this.



while here noise not eliminated.

electrocardiogram (ECG) System

→ Our body have a signal very less low amplitude so for ECG we have to take that and amplify for further processing.

→ System-1 is differential Amplifier. Signal V_1 and V_2 both are coupled with noise. So we know diff. Amp.

$$V_o = A_o \times (\text{difference of signal})$$

since both signal have noise so

$$V_+ - V_- = V_1 + V_n - (V_2 + V_n)$$

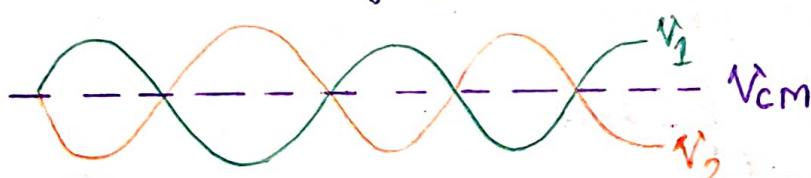
$$= V_1 - V_2 \quad \{ \text{Noise eliminated} \}$$

→ So this was the problem, we need differential Amplifiers.

Differential Signals :- (a) They vary by equal and opposite amounts.

(b) They have the same average (dc) value V_{cm} . (The common-mode level)

For example:



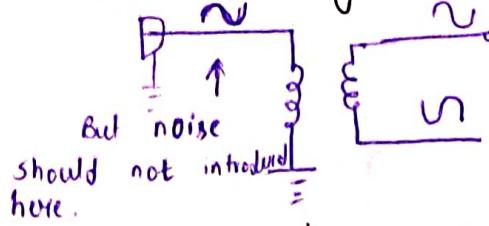
$$V_1 = V_m \sin \omega t + V_{cm}$$

$$V_2 = -V_m \sin \omega t + V_{cm}$$

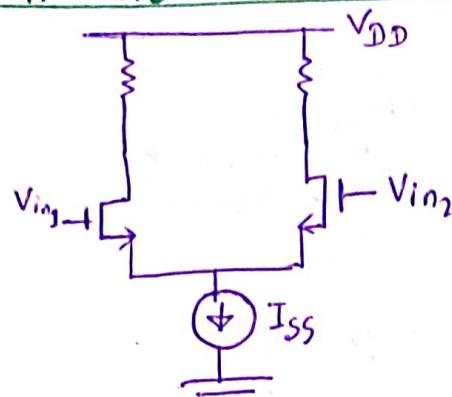
Observations:

	V_1	V_2	$V_1 - V_2$
Peak Amplitude	V_m	V_m	$2V_m$
Peak-to-peak Amplitude	$2V_m$	$2V_m$	$4V_m$

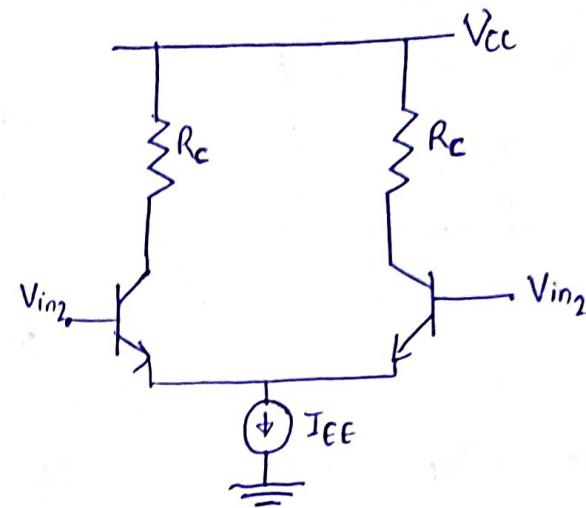
How do we generate differential signals:



The Differential Pair :-



MOS Differential Pair

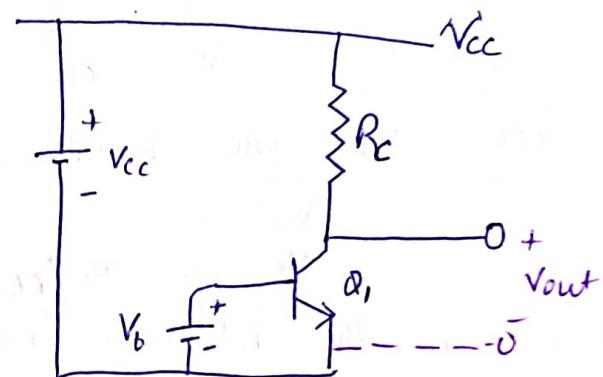


BJT differential Pair

Review of CE Stage :-

$$(i) I_c = I_s e^{V_b/V_T}$$

$$(ii) V_{cc} = I_c R_c + V_{out}$$



Intuitive Analysis of Bi-polar Differential Pair :-

(i) Case I :- Sot Base of Both BJTs, and apply a D.C signal and also bias both transistors in Active Regions.

$$\text{Since } V_{BE1} = V_{BE2}$$

$$\text{so } I_{C1} = I_{C2}$$

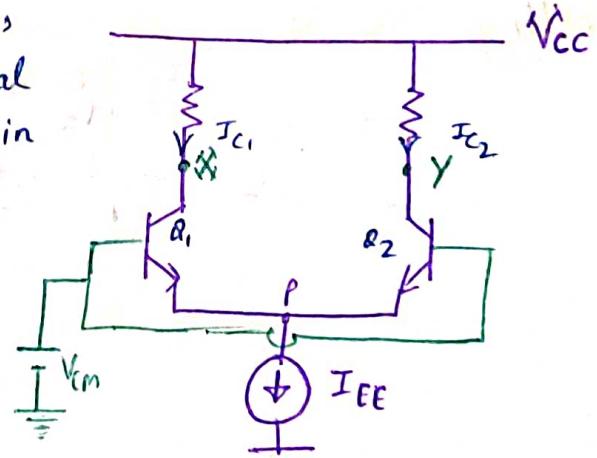
$$\text{and By K.C.L } I_{C1} + I_{C2} = I_{EE}$$

$$\text{Hence } I_{C1} = I_{C2} = \frac{I_{EE}}{2} \quad (\text{due to symmetry})$$

$$\text{voltage drop across } R_C = \frac{I_{EE}}{2} R_C$$

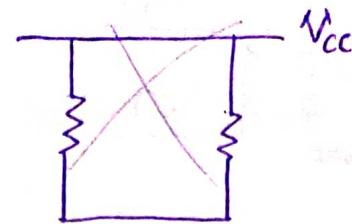
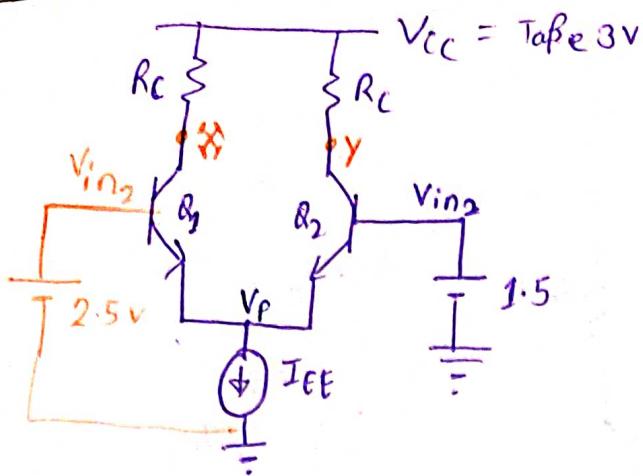
$$\therefore V_X = V_{cc} - \frac{I_{EE}}{2} R_C$$

$$V_Y = V_{cc} - \frac{I_{EE}}{2} R_C$$



Observation
If $V_{in1} - V_{in2} = 0$, then $V_X - V_Y = 0$

Case-II Biasing BJT's Base at different voltages:



Making a busers that & is
in Active Region' Committee

$$V_{BE_1} \approx 0.7 \text{ V} \quad (\text{in forward bias})$$

$$\text{Ans} \quad V_p = 2.5 - 0.7 \quad (\text{Active region}) \\ = 1.8 \text{ volt}$$

Hence $V_{BE_2} = -V_{CE}$ so it is cut-off. Hence $I_{C_2} = 0$

$$I_{C1} = I_{CE}$$

In this way $V_n = V_{CC} - R_C I_{EE}$

$$V_y = V_{CA}$$

Suppose V_{in_2} was biased at higher voltage then $I_C = 0$

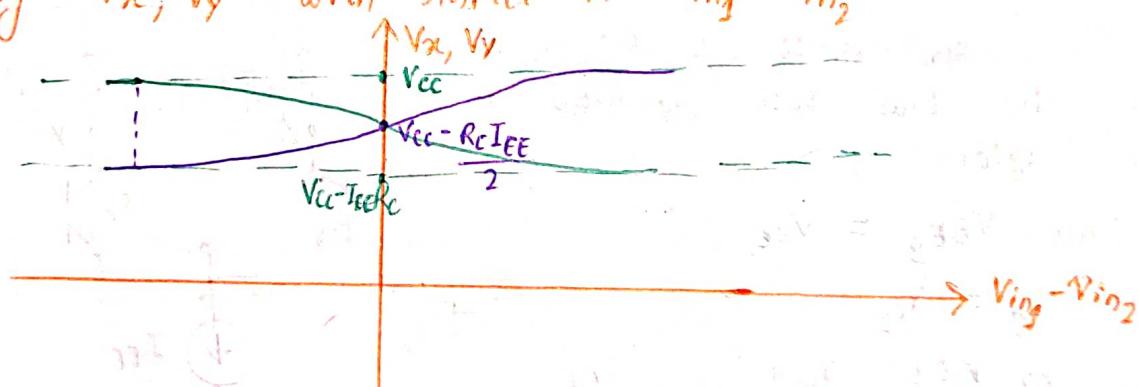
$$\text{So } V_{IN} = V_{CC}$$

$$V_Y = V_{CC} - R_C I_{EE}$$

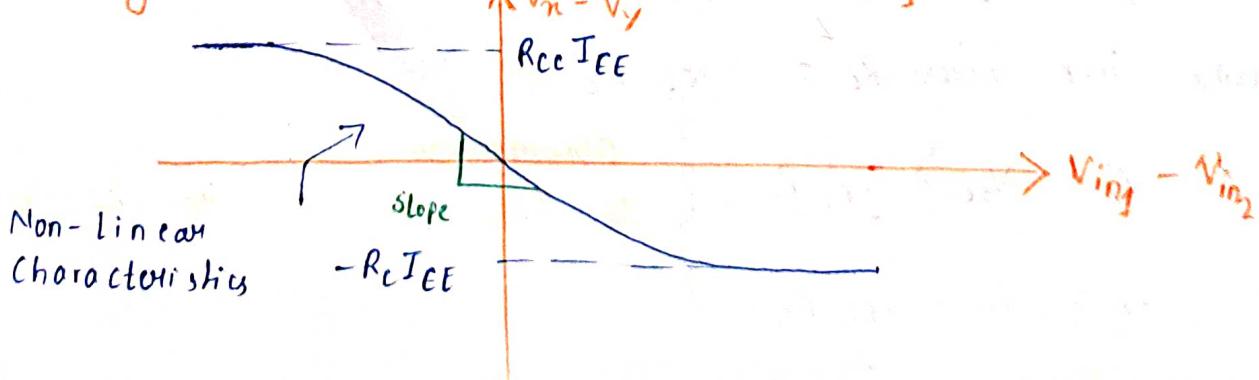
Based on the following analysis we can observe:

$$V_n - V_y = f(V_{in_1} - V_{in_2})$$

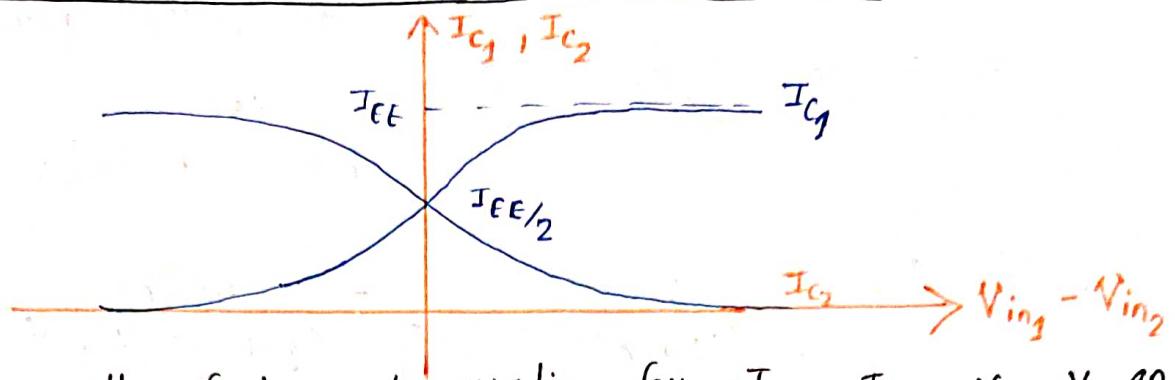
→ Plotting V_{x_1}, V_y with respect to $V_{in_1} - V_{in_2}$



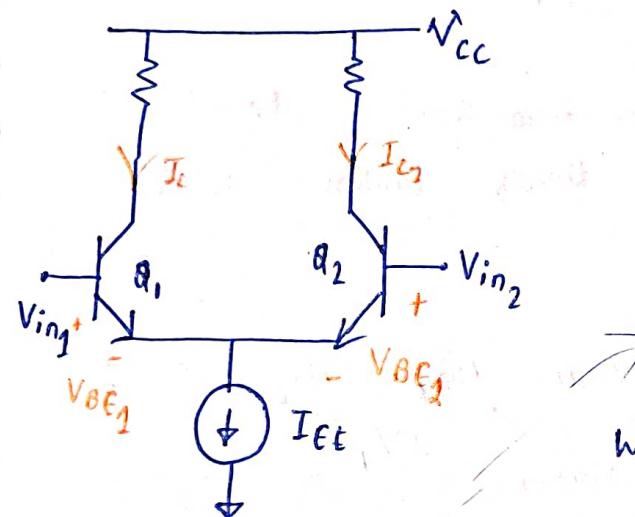
→ Plotting $V_x - V_y$ with respect to $V_{in_1} - V_{in_2}$



Plotting I_{C_1} , I_{C_2} Based on intuitive study :-



Now we will find exact equation for I_{C_1} , I_{C_2} , V_n , V_y and $V_n - V_y$ as a function of $V_{in_1} - V_{in_2}$:-
(Applicable for large, small both because these are infinit exact)



Note: → Both are matched Transistor.

→ β very high so $I_c \approx I_E$

By K.V.L

$$V_{in_1} - V_{BE_1} = V_{in_2} - V_{BE_2}$$

$$\Rightarrow V_{in_1} - V_{in_2} = V_{BE_1} - V_{BE_2}$$

We know for Transistor:

$$I_c = I_s e^{V_{BE}/V_T}$$

$$\therefore V_{BE} = V_T \ln \left(\frac{I_c}{I_s} \right)$$

That's why:

$$V_{BE_1} = V_T \ln \left(\frac{I_{C_1}}{I_s} \right)$$

$$V_{BE_2} = V_T \ln \left(\frac{I_{C_2}}{I_s} \right)$$

I_s for both Q_1, Q_2 is same

So,

$$V_{in_1} - V_{in_2} = V_T \ln \left(\frac{I_{C_1}}{I_{C_2}} \right) \Rightarrow I_{C_1} = I_{C_2} e^{\frac{V_{in_1} - V_{in_2}}{V_T}}$$

K.C.L at Node

$$I_{C_1} + I_{C_2} = I_{EE}$$

$$\Rightarrow I_{C_2} e^{\frac{V_{in_1} - V_{in_2}}{V_T}} + I_{C_2} = I_{EE}$$

$$\Rightarrow I_{C_2} = \frac{I_{EE}}{1 + e^{\frac{V_{in_1} - V_{in_2}}{V_T}}}$$

Similarly

$$I_{C_1} = \frac{I_{EE}}{1 + e^{\frac{V_{in_2} - V_{in_1}}{V_T}}}$$

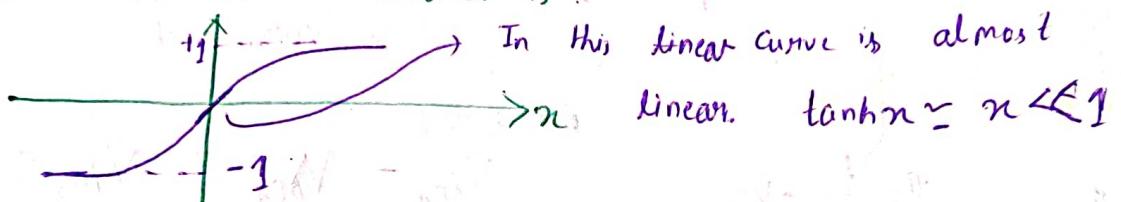
Where : $V_x = V_{CC} - I_{C_1} R_C = V_{CC} - \frac{R_C I_{EE}}{1 + e^{(V_{in_2} - V_{in_1})/V_T}}$

$V_y = V_{CC} - I_{C_2} R_C = V_{CC} - \frac{R_C I_{EE}}{1 + e^{(V_{in_1} - V_{in_2})/V_T}}$

∴ $V_x - V_y = \frac{R_C I_{EE}}{[1 + e^{(V_{in_2} - V_{in_1})/V_T}]} - \frac{R_C I_{EE}}{[1 + e^{-(V_{in_1} - V_{in_2})/V_T}]}$

 $= -R_C I_{EE} \tanh \left(\frac{V_{in_1} - V_{in_2}}{2V_T} \right)$

The tanh hyperbolic function is :



Main for Small signal :- Means $\frac{V_{in_1} - V_{in_2}}{2V_T} \ll 1$

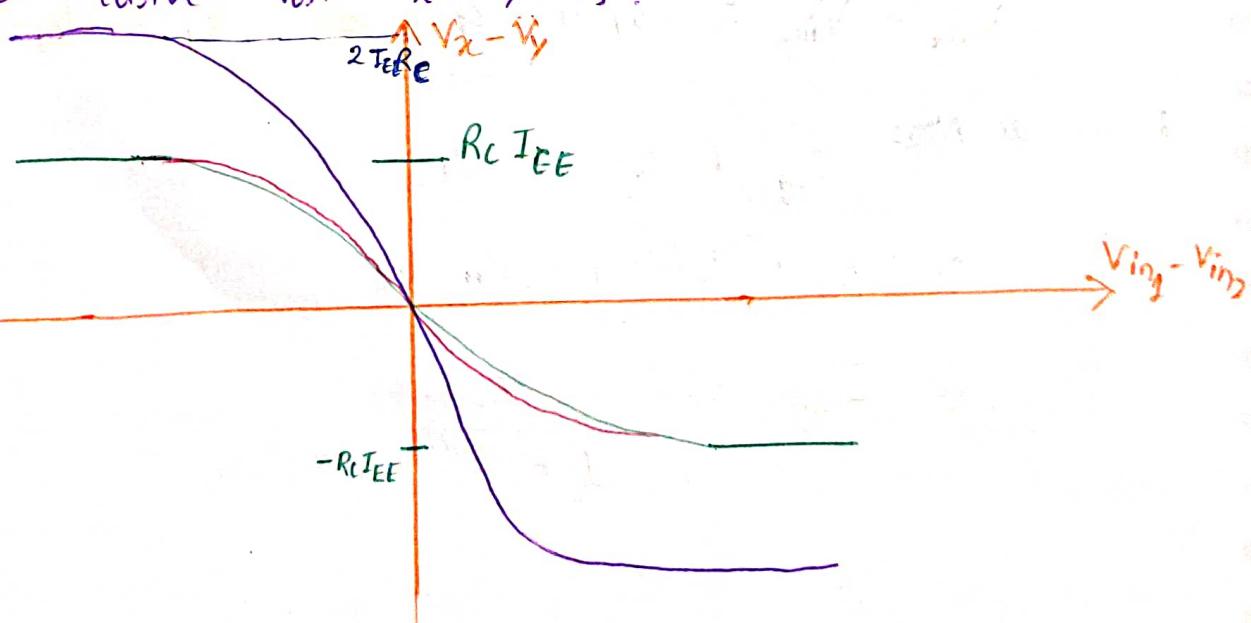
In this region curve is almost linear.

∴ $V_x - V_y = -R_C I_{EE} \left(\frac{V_{in_1} - V_{in_2}}{2V_T} \right)$

⇒ Output = $\frac{-R_C I_{EE}}{2V_T} (Input)$

This is slope for small signal.

∴ The exact curve for $V_x - V_y$ is :



Green one \rightarrow Original curve

Red one \rightarrow When Ambient temperature drops considerably.

$$V_T = \frac{KT}{q} \text{ so } V_T \downarrow$$

Slope \uparrow but peak values

still same.

Purple one \rightarrow When either R_C or I_{EE} doubled.

Summary of Differential Pair Properties :-

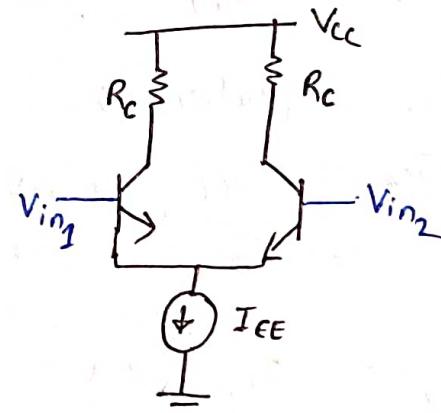
- 1) If $|V_{in_1} - V_{in_2}|$ is large, all of the tail current is "steered" to one side. Also called "Current-steering" circuits.
- 2) If $V_{in_1} = V_{in_2}$ and V_{cm} goes up and down \Rightarrow the currents and voltages do not change.
This implies
- 3) If $|V_{in_1} - V_{in_2}| \ll 2V_T$

$$\text{slope} = -\frac{R_C I_{EE}}{2V_T} \quad (\text{brain})$$

Quiz:- Can this circuit Amplify:

$$V_x - V_y = -R_C I_{EE} \tanh \frac{V_{in_1} - V_{in_2}}{2V_T}$$

Let V_{in_1}, V_{in_2} are pure differential signals and they V_{in_1} go up by ΔV then, V_{in_2} goes down by ΔV .



$$\text{So, } V_x - V_y = \left(-R_C I_{EE} \tanh \frac{2\Delta V}{2V_T} \right)$$

If ΔV is very small then

$$V_x - V_y = \left[\frac{-R_C I_{EE}}{2V_T} \times 2\Delta V \right] \rightarrow \text{This factor} > 1 \text{ then it can amplify.}$$

Recall:

For BJT:

$$g_m = \frac{\Delta I_C}{\Delta V} = \frac{I_C}{V_T}$$

At which BJT is Biased

Small Signal Behaviour Of Differential Amplifier :-

If V_{in_1} and V_{in_2} change by equal and opposite amounts and the change is small, then the tail node voltage does not change.

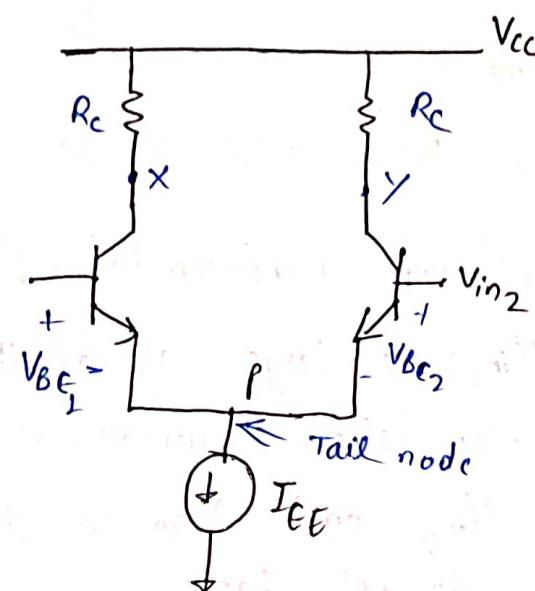
$$V_x = \beta V_{cc} - I_{C1} R_C$$

$$V_y = V_{cc} - I_{C2} R_C$$

$$\therefore V_x - V_y = -R_C (I_{C1} - I_{C2})$$

we already know,

$$V_x - V_y = -R_C I_{EE} \frac{2\Delta V}{V_T}$$



$$I_{C1} - I_{C2} = I_{EE} \cdot \frac{\Delta V}{V_T} \quad \text{--- (i)}$$

Assumed β of both Transistor is very high.

$$I_{C1} + I_{C2} = I_{EE} \quad \text{--- (ii)}$$

\therefore from equation (i) & (ii)

$$I_{C1} = \frac{I_{EE}}{2} \left(1 + \frac{\Delta V}{V_T} \right)$$

The Bias Current depends on Common mode voltage and that is same for V_{in_1}, V_{in_2} so

$$I_c = I_{EE}/2$$

Hence

$$\Delta I_{C1} = \frac{I_{EE}}{2} \cdot \frac{\Delta V}{V_T}$$

$$\therefore g_m = \frac{\Delta I_c}{\Delta V_{BE}}$$

$$\text{and } g_m = \frac{I_c}{V_T}$$

$$= \frac{I_{EE}}{2V_T}$$

$$\therefore \Delta V_{BE} = \frac{\Delta I_c}{g_m}$$

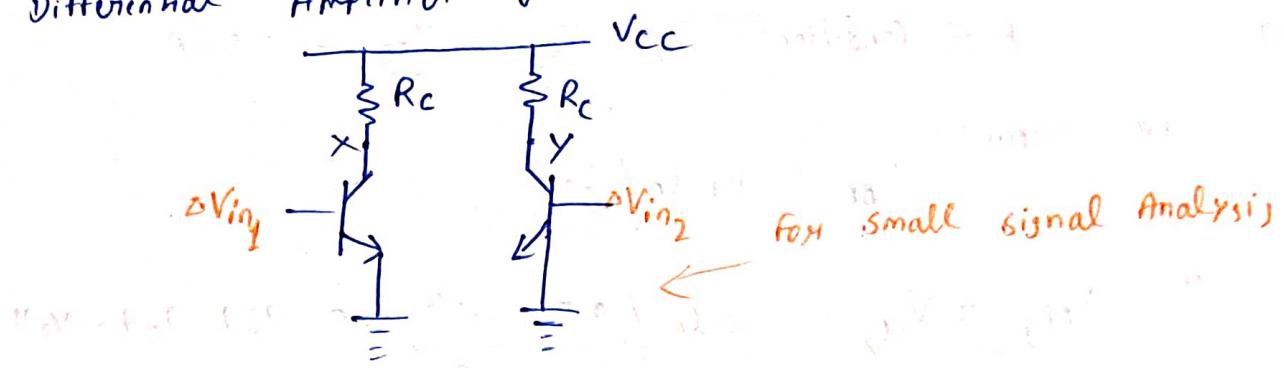
$$\Delta V_{BE} = \Delta V$$

\therefore If V_{in} goes \uparrow by ΔV then all this small change is adjusted in V_{BE} and Tail node voltage V_p is constant.

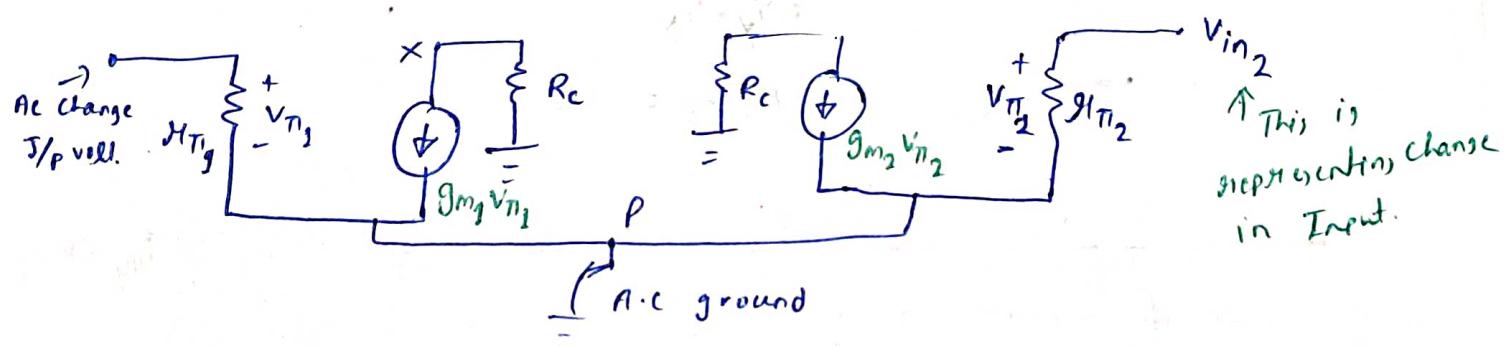
For A.C. analysis:

- All Capacitors \rightarrow shorted
- Voltage source \rightarrow shorted
- Constant voltage load \rightarrow grounded (A.C. ground)
- Current source \rightarrow open

So T_{EE} gets open for AC analysis and point P is constant voltage point so it is A.C. ground. So own Differential Amplification just converts to two Common-Emitter stages.



Model is:



We already know gain for CE stage $= -g_m R_C$

$$\text{So } V_x = -g_m R_C \Delta V_{in_1}$$

$$V_y = -g_m R_C \Delta V_{in_2}$$

$$\therefore V_x - V_y = -g_m R_C (\Delta V_{in_1} - \Delta V_{in_2})$$

\hookrightarrow Differential input voltage

$$\therefore A_v = -g_m R_C \quad \text{and} \quad g_m = \frac{\text{Bias current } (I_C)}{V_T}$$

$$A_v = \frac{-R_C I_{EE}}{2V_T} = \frac{I_{EE}/2}{V_T}$$

In this way also we are getting same gain.

Numericals on Differential pair and also some special Analysis:-

Ques. 1 $I_{EE} = 1 \text{ mA}$, $R_C = 1 \text{ k}\Omega$, $I_S = 2 \times 10^{-18} \text{ A}$

Both transistors are matched. Assume standard differential pair.

a) Determine the bias conditions of α_1 and α_2 .

b) Construct the input-output characteristics.

c) Voltage gain

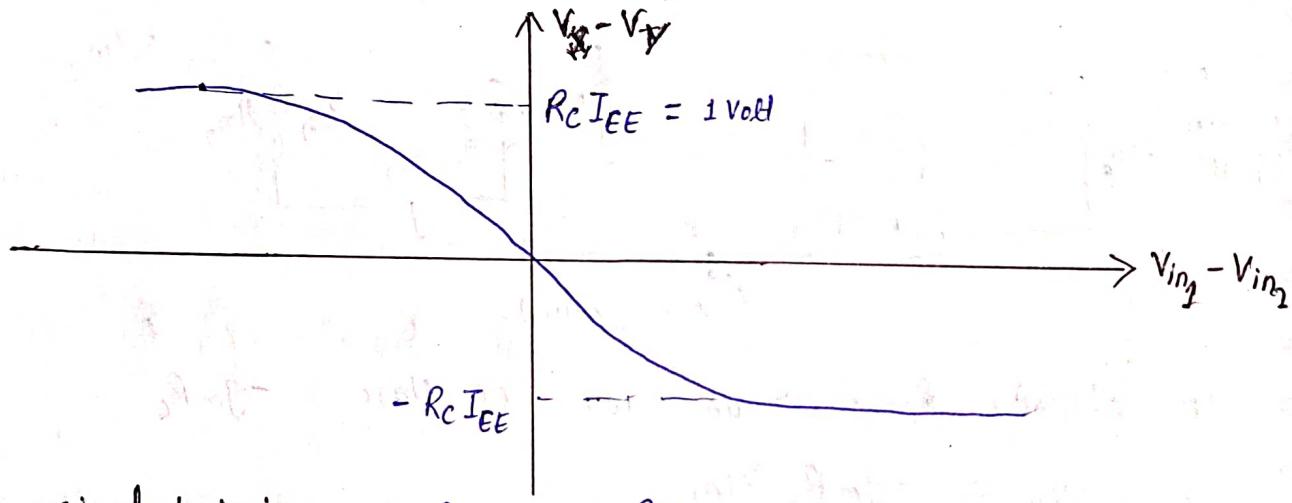
a) Bias Conditions $I_{C1} = I_{C2} = \frac{I_{EE}}{2} = 0.5 \text{ mA}$

we know,

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

$$V_{BE_1} = V_{BE_2} = 26 \ln\left(\frac{0.5 \times 10^{-3}}{2 \times 10^{-18}}\right) = 861.9645 \text{ mV}$$

b)

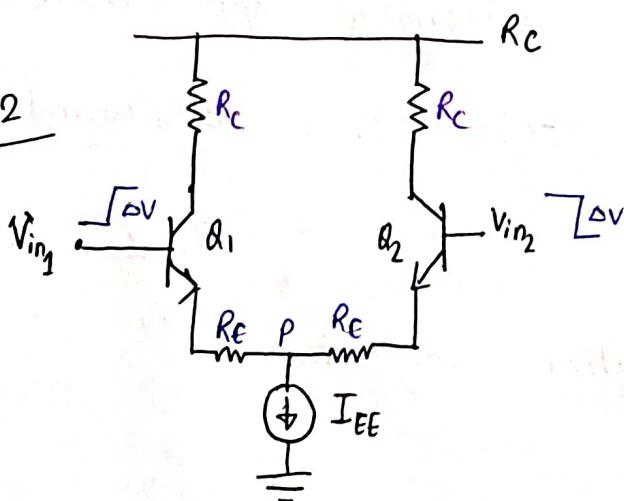


c) Small-signal gain:

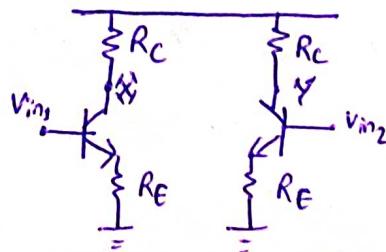
$$-g_m R_C = \frac{-R_C I_{EE}}{2V_T}$$

$$= \frac{-1 \times 1}{2 \times 26 \times 10^{-3}} = -19.23$$

Ques. 2



IF we apply a differential input then V_P does not change with time. P is ac ground. So small signal model P acts as ground.



This is a source with degeneration stage whose gain is given by

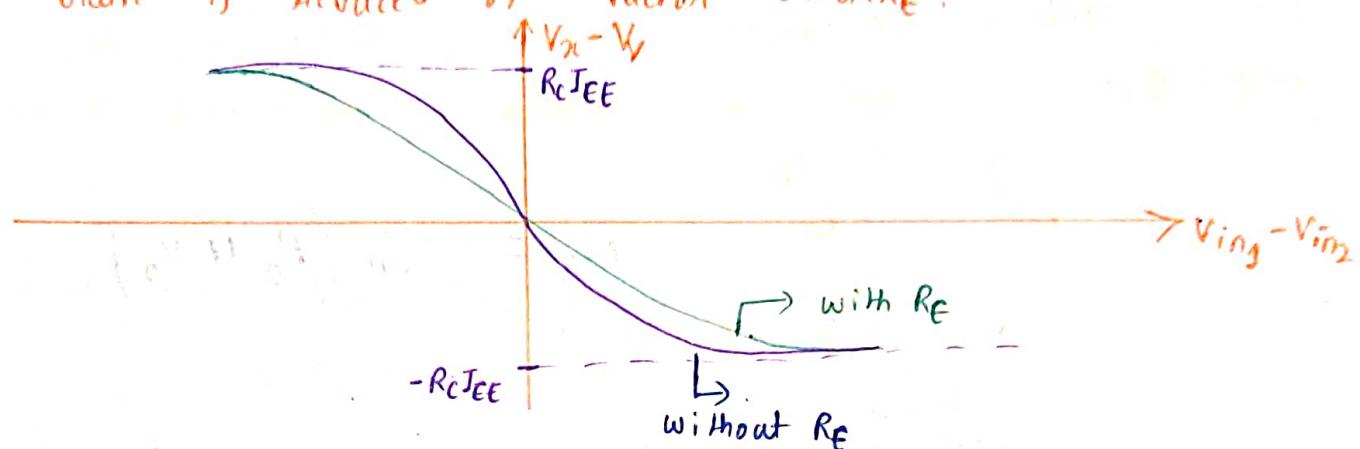
$$\frac{-R_C}{\frac{1}{g_m} + R_E}$$

$$\therefore V_{xy} = \frac{-R_C}{\frac{1}{g_m} + R_E} V_{in_1}, \quad V_y = \frac{-R_C}{\frac{1}{g_m} + R_E} V_{in_2}$$

Hence,

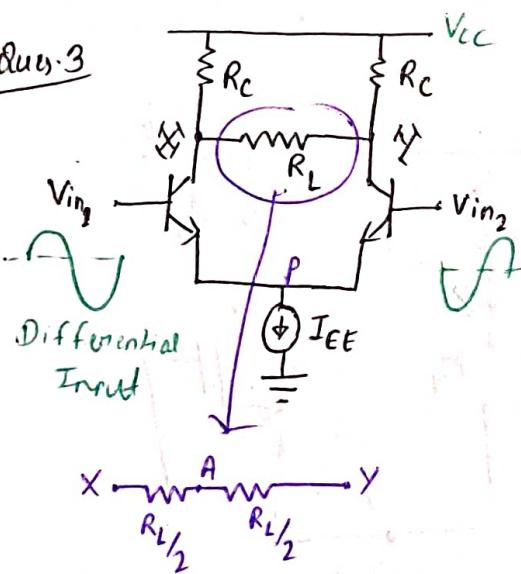
$$\therefore \text{Gain} = \frac{V_x - V_y}{V_{in_1} - V_{in_2}} = \frac{-R_C}{\frac{1}{g_m} + R_E} = \frac{-R_C g_m}{1 + g_m R_E}$$

So gain is reduced by factor $1 + g_m R_E$.

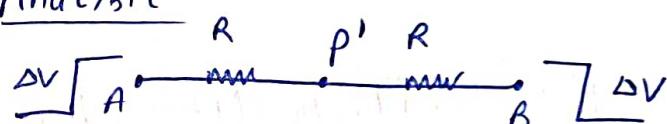


→ Emitter degeneration increases the Linearity

Ques. 3



Analysis



$$i = \frac{2\Delta V}{2R} = \frac{\Delta V}{R}$$

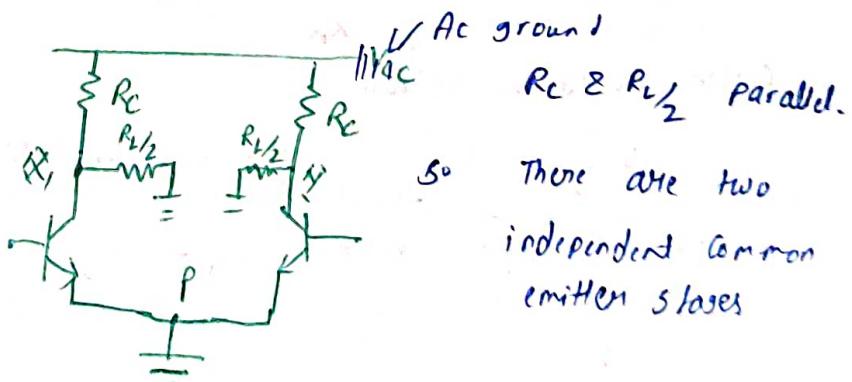
∴ drop across R = ΔV

It means node P' voltage is same (constant) if there is differential change at inputs.

∴ Here Node A and P both acts as AC ground.

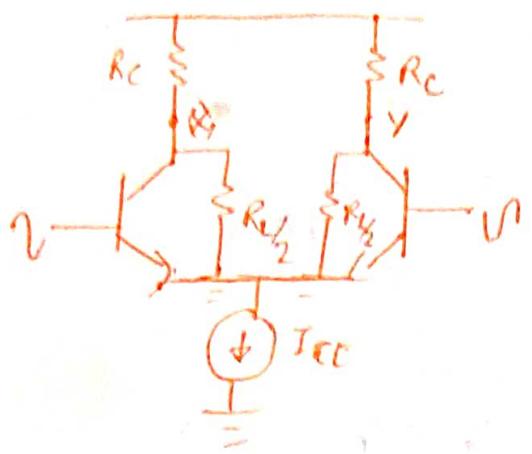
Half Circuit Equivalent is:

$$Av = -g_m \left(R_C \parallel \frac{R_L}{2} \right)$$



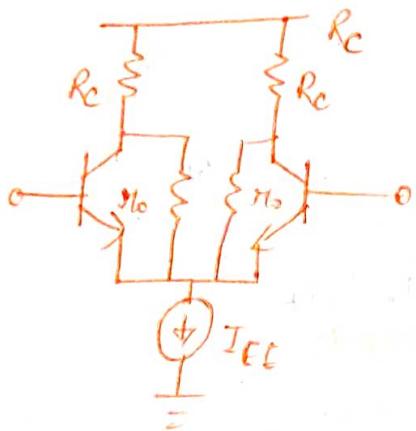
∴ There are two independent common emitter stages

so what is difference between given figure and Ques 3?



Both are same for small signal model but these D.C model/Bias conditions are different because of $R_{1/2}$.

Now if we assume early voltage of BJT $\approx \infty$ then output resistance of BJT's comes in picture and that is same way dealt in same way as $R_{1/2}$.



$$A_V = -g_m (R_C \parallel R_0)$$

MOS Differential Pair :-

→ Both MOS are matched and both are biased in saturation.

In saturation region, Drain

current is given by:

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{DS} - V_{Th})^2$$

$$V_{cm,n} = \frac{V_{DS}}{2}$$

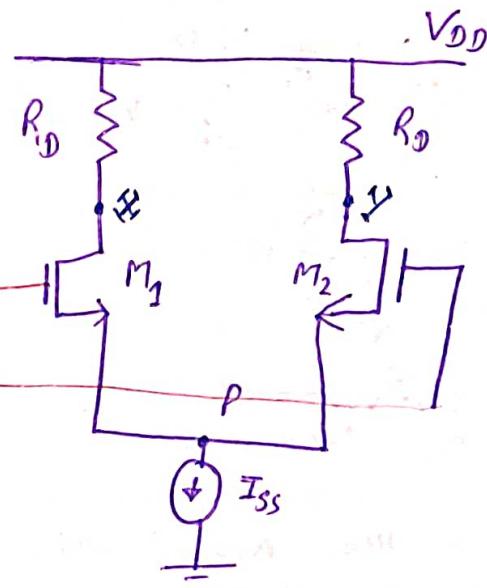
$$\Rightarrow \frac{V_{DS} - V_{Th}}{2} = \sqrt{\frac{2 I_D}{K_n}}$$

called overdrive voltage

→ When $V_{in1} = V_{in2}$, the differential pair is in equilibrium.

And in equilibrium $I_{D1} = I_D = I_{SS}/2$

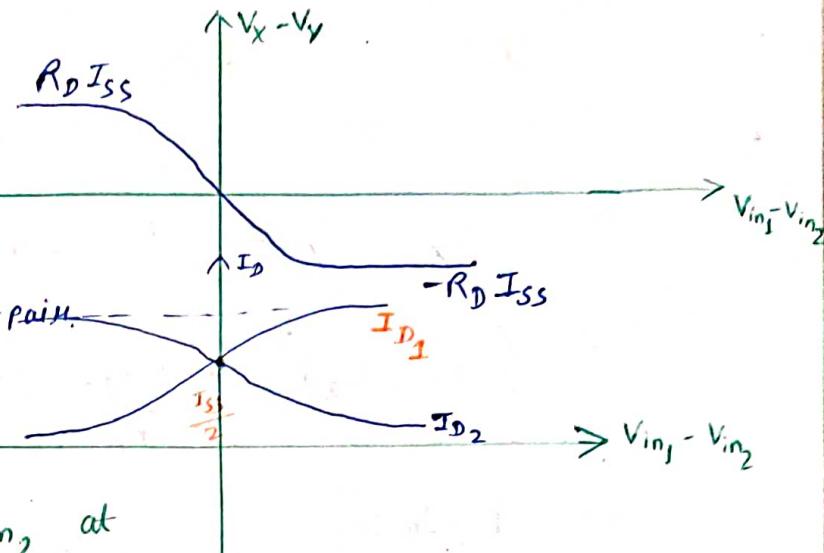
$$\therefore V_{DS} - V_{Th} = \sqrt{\frac{I_{SS}}{K_n}}$$



→ Suppose common mode voltage changes then what change in circuit? → All change is adjusted in node voltage V_p . and nothing changes in circuit because V_{BTS} is dependent on I_{SS} and K_n .

* Graph of $(V_x - V_y)$ v/s $V_{in_1} - V_{in_2}$

Since J_D follows square-law relation so this function is not going to be tangential hyperbolic as it was in BJT Diff-pair.



* Minimum value of $V_{in_1} - V_{in_2}$ at which one transistor turns off?

$$\text{From fig: } V_{in_1} - V_{BTS_1} = V_{in_2} - V_{BTS_2}$$

$$\Rightarrow V_{in_1} - V_{in_2} = V_{BTS_1} - V_{BTS_2}$$

Let M_2 Transistor turns off, so the moment I_{D2} becomes zero it goes to cut-off region and at that moment $V_{BTS_2} = V_{Th}$

Since $I_{D2} = 0$ so all of the I_{SS} goes in M_1 so $I_{D1} = I_{SS}$

In this way:

$$V_{in_1} - V_{in_2} = \sqrt{\frac{2I_{SS}}{K_n}} + V_{Th} - (V_{Th})$$

$$V_{in_1} - V_{in_2} = \sqrt{\frac{2I_{SS}}{K_n}}$$

* Large Signal Analysis :- In terms of I_{D1} and I_{D2}

$$V_{in_1} - V_{in_2} = \underbrace{\sqrt{\frac{2I_{D1}}{K_n}} + V_{Th}}_{V_{BTS_1}} - \underbrace{\left(\sqrt{\frac{2I_{D2}}{K_n}} + V_{Th} \right)}_{V_{BTS_2}}$$

since Both are matched Transistors that's why $K_{n1} = K_{n2} = K_n = \frac{m_{nL} \times W}{L}$

$$(V_{in_1} - V_{in_2})^2 = \frac{2I_{D1}}{K_n} + \frac{2I_{D2}}{K_n} - 2 \sqrt{\frac{2I_{D1} \times 2I_{D2}}{K_n^2}}$$

By KCL at Node P: $I_{D_1} + I_{D_2} = I_{SS}$

$$\Rightarrow (V_{in_1} - V_{in_2})^2 = \frac{2I_{SS}}{K_n} - \frac{4}{K_n} \sqrt{I_{D_1}(I_{SS} - I_{D_1})}$$

We know that

$$V_x = V_{DD} - I_{D_1} R_D$$

$$V_y = V_{DD} - I_{D_2} R_D$$

$$\text{So, } V_x - V_y = -R_D(I_{D_1} - I_{D_2})$$

$$\Rightarrow (V_{in_1} - V_{in_2})^2 - \frac{2I_{SS}}{K_n} = -\frac{4}{K_n} \sqrt{I_{D_1} I_{D_2}}$$

$$\Rightarrow \frac{4 \sqrt{I_{D_1} I_{D_2}}}{K_n} = \frac{2I_{SS}}{K_n} - (V_{in_1} - V_{in_2})^2$$

$$\Rightarrow 2 \sqrt{I_{D_1} I_{D_2}} = I_{SS} - \frac{K_n}{2} (V_{in_1} - V_{in_2})^2$$

$$\text{Since we know: } 4I_{D_1} I_{D_2} = I_{SS}^2 + \frac{K_n^2}{4} (V_{in_1} - V_{in_2})^4 - I_{SS} K_n (V_{in_1} - V_{in_2})^2$$

$$(I_{D_1} - I_{D_2})^2 = (I_{D_1} + I_{D_2})^2 - 4I_{D_1} I_{D_2}$$

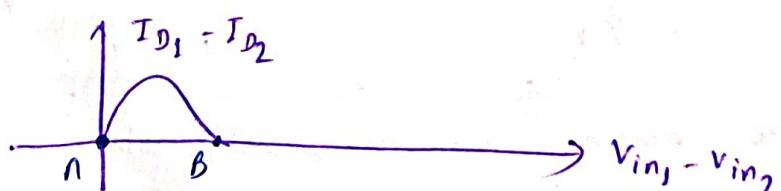
$$\Rightarrow (I_{D_1} - I_{D_2})^2 = I_{SS}^2 - \left(I_{SS}^2 + \frac{K_n^2}{4} (V_{in_1} - V_{in_2})^4 - I_{SS} K_n (V_{in_1} - V_{in_2})^2 \right)$$

$$\Rightarrow (I_{D_1} - I_{D_2})^2 = (V_{in_1} - V_{in_2})^2 \left[-\left\{ \frac{K_n}{2} (V_{in_1} - V_{in_2}) \right\}^2 + I_{SS} K_n \right]$$

$$\therefore \Rightarrow I_{D_1} - I_{D_2} = (V_{in_1} - V_{in_2}) \frac{K_n}{2} \sqrt{- (V_{in_1} - V_{in_2})^2 + \frac{4I_{SS}}{K_n}}$$

$$\Rightarrow I_{D_1} - I_{D_2} = \frac{K_n}{2} (V_{in_1} - V_{in_2}) \sqrt{\frac{4I_{SS}}{K_n} - (V_{in_1} - V_{in_2})^2}$$

If we plot this,



When $V_{in_1} = V_{in_2}$ i.e. $I_{D_1} = I_{D_2}$ so $I_{D_1} - I_{D_2} = 0$

→ But what is positive value of $V_{in_1} - V_{in_2}$ (point B) at

which $I_{D_1} - I_{D_2} = 0$? There is no such value.

Actually what happens is:

$$\text{When } V_{in_1} - V_{in_2} = \sqrt{\frac{2I_{SS}}{KnCox W/L}}, M_2 \text{ goes in}$$

zero, so cut-off region. While we derived these equations by assuming Both BJTs in saturation region MOS

so This equation of $I_{D_1} - I_{D_2}$ is valid only for Both MOS ON.

So,

$$V_x - V_y = -\frac{R_D K_n}{2} (V_{in_1} - V_{in_2}) \sqrt{\frac{4I_{SS}}{K_n} - (V_{in_1} - V_{in_2})^2}$$

\Rightarrow Form

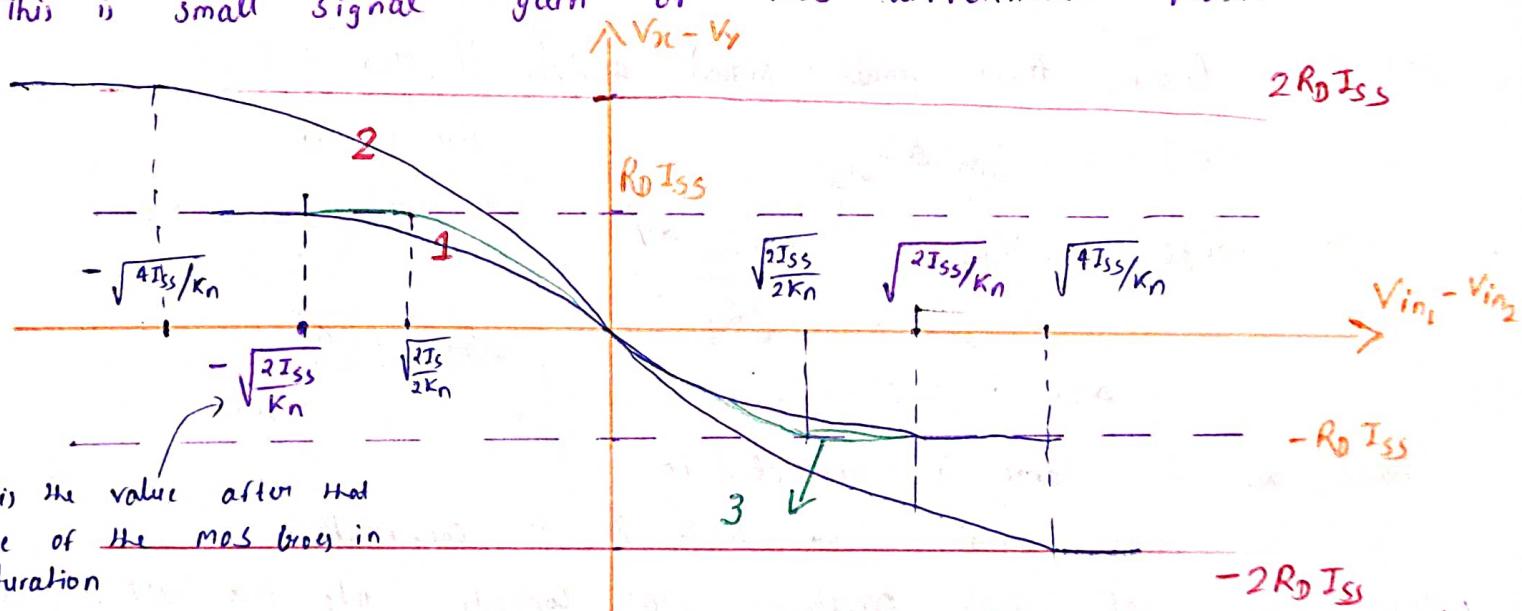
$$(V_{in_1} - V_{in_2})^2 \ll \frac{4I_{SS}}{K_n}$$

May value of $V_x - V_y$ for Transistor to be in saturation is $\frac{2I_{SS}}{K_n}$ so, R_D root is always positive.

$$\frac{V_x - V_y}{V_{in_1} - V_{in_2}} = -\frac{R_D K_n}{2} \times \sqrt{\frac{4I_{SS}}{K_n}}$$

$$= -R_D \sqrt{I_{SS} K_n}$$

This is small signal gain of MOS differential pair.



This is the value after that one of the mos goes in saturation

1 → Normal Situation

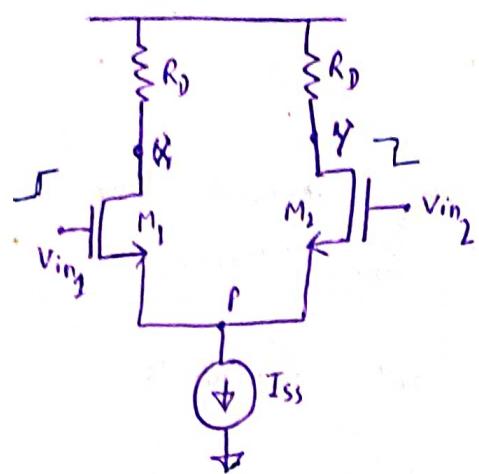
2 → This is graph when I_{SS} is doubled.

Slope for small signal increased $\sqrt{2}$ times and saturation ($V_x - V_y$)

value also increased to $2R_D I_{SS}$. And maximum allowable voltage ($V_{in_1} - V_{in_2}$) for both mos to be in saturation also increased so linearity increased.

3 → When K_n or W/L is doubled: $\rightarrow R_D I_{SS}$ same
 \rightarrow slope increased but max ($V_{in_1} - V_{in_2}$) for maintaining

Small Signal behaviour of MOS differential Pair :-



V_{in_1} and V_{in_2} are small differential voltages. For them common mode is same and as V_{in_1} goes up by ΔV , then V_{in_2} goes down by ΔV .

→ We know from earlier analysis:

$$V_x - V_y = -R_D \sqrt{K_n I_{ss}} (V_{in_1} - V_{in_2})$$

∴ $V_x - V_y = -R_D \sqrt{K_n I_{ss}} 2\Delta V$

And also $V_x - V_y = -R_D (I_{D1} - I_{D2})$

That's why

$$I_{D1} - I_{D2} = \sqrt{K_n I_{ss}} 2\Delta V$$

$$I_{D1} + I_{D2} = I_{ss}$$

So, $I_{D1} = \frac{I_{ss}}{2} + \underbrace{\sqrt{K_n I_{ss}} \Delta V}_{\text{This is change}}$

This is bias current in M_1

And we know from small signal analysis of MOS

$$\Delta I_D = g_m \Delta V_{BS}$$

So Change in V_{BS} = $\frac{\sqrt{K_n I_{ss}} \Delta V}{g_m}$

$$\Delta V_{BS} = \Delta V$$

for MOSFET

$$g_m = \sqrt{2 \mu n \epsilon_s \frac{W}{L} I_D}$$

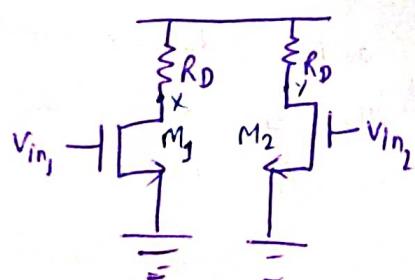
$$g_m = \sqrt{2 K_n I_D} = \sqrt{K_n I_{ss}}$$

where I_D is bias current

Hence all the change is reflected in

V_{BS} for small signal. So Node P is constant.

Hence for small signal operation, MOS converts into two half circuit Common Source stages.

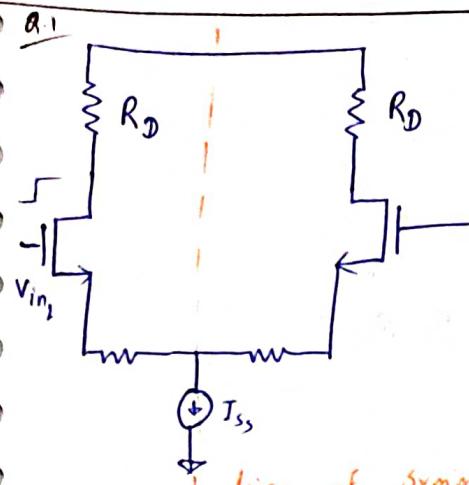


$$V_x - V_y = -g_m R_D (V_{in_1} - V_{in_2})$$

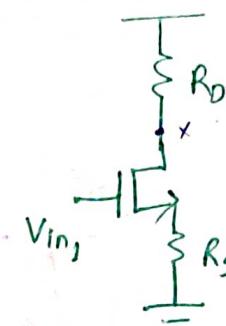
Assumed both transistors having same g_m .

$$A_v = -g_m R_D$$

Some other cases of MOS differential Pair:-



Half
Circuit



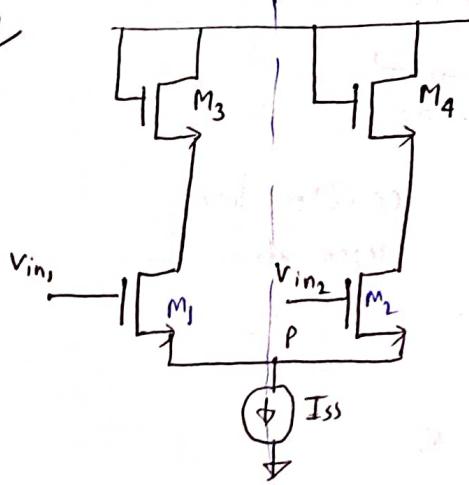
Source with degeneration stage

$$\frac{V_x}{V_{in_1}} = \frac{-R_D}{\frac{1}{g_m} + R_S}$$

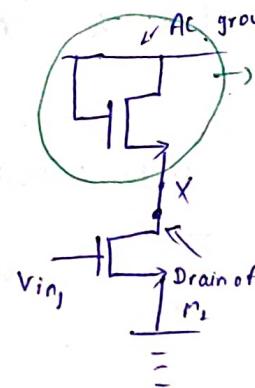
$$\frac{V_y}{V_{in_2}} = \frac{-R_D}{\frac{1}{g_m} + R_S}$$

$\therefore A_V = \frac{V_x - V_y}{V_{in_1} - V_{in_2}} = \frac{-R_D}{\frac{1}{g_m}}$

In place of R_D we have diode connected MOS.



Half
Circuit



We know CS stage gain:
 $= -g_m$ (Resistance tied b/w D & AC ground)

Output resistance of diode connected device $= \frac{1}{g_m}$ (neglected channel length modulation)

$\therefore A_V = -g_{m_1} \times \left(\frac{1}{g_{m_3}} \right)$

Assumed M_1 & M_2 have same g_m . And M_3 & M_4 have same g_m .

Q.3 Gain of standard MOS stage $= -g_m R_D$

What if (i) W doubled

$$\therefore g_m = \sqrt{\mu_n C_o x \frac{W}{L} I_D}$$

\therefore Gain $\sqrt{2}$ times

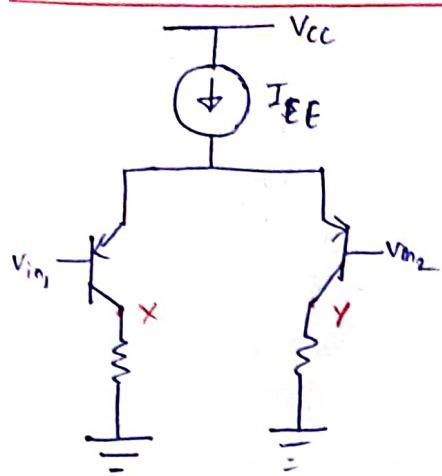
(ii) W & I_{ss} doubled

$$\text{Gain} = \sqrt{2} \times \sqrt{2} = 2 \text{ times}$$

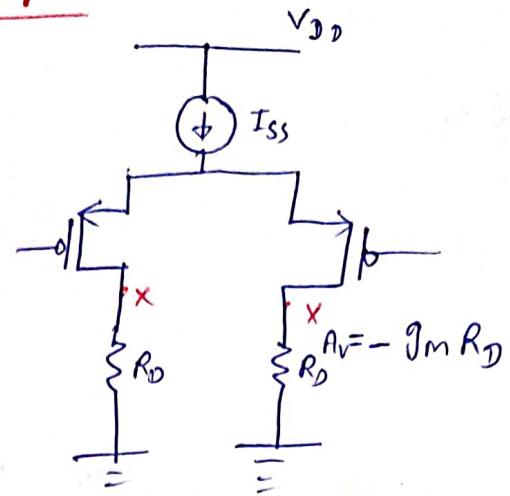
(iii) temperature rises

$$\mu_n \downarrow \Rightarrow g_m \downarrow \Rightarrow |A_V| \downarrow$$

P-type differential pair :-

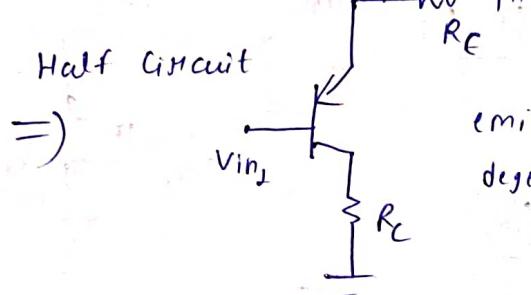
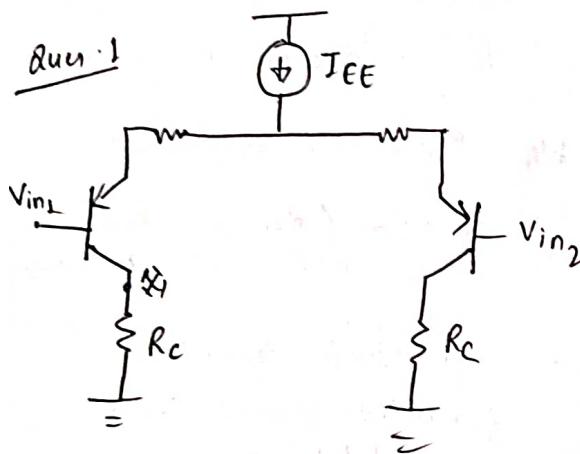


BJT differential Pair

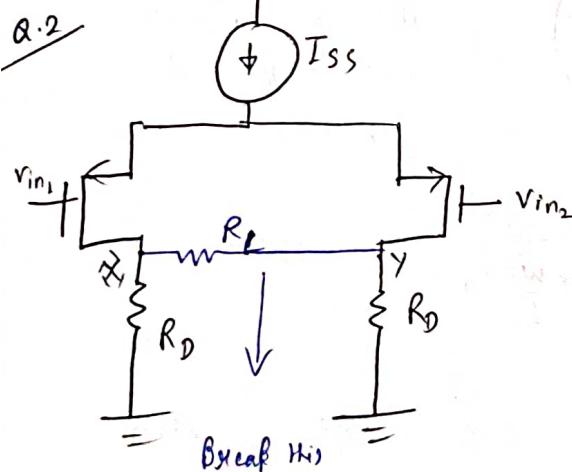


Mos differential pair.

These analysis is also similar to N-type differential pair.



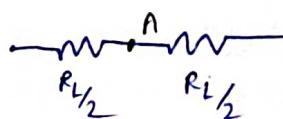
$$A_V = \frac{-R_C}{\frac{1}{g_m} + R_E}$$



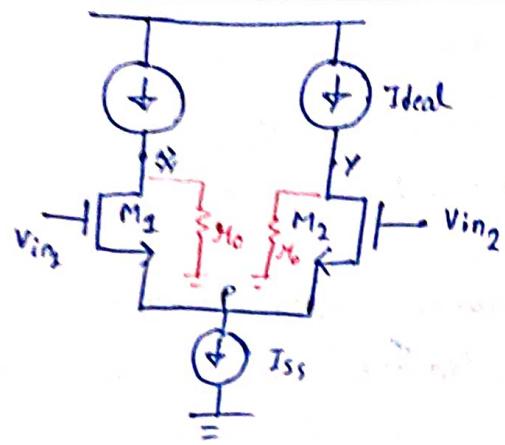
point A will act as virtual ground in A.C analysis.

$$A_V = -g_m \left(R_D \parallel R_L / 2 \right)$$

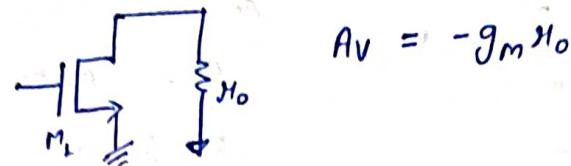
R_L and make circuit symmetric



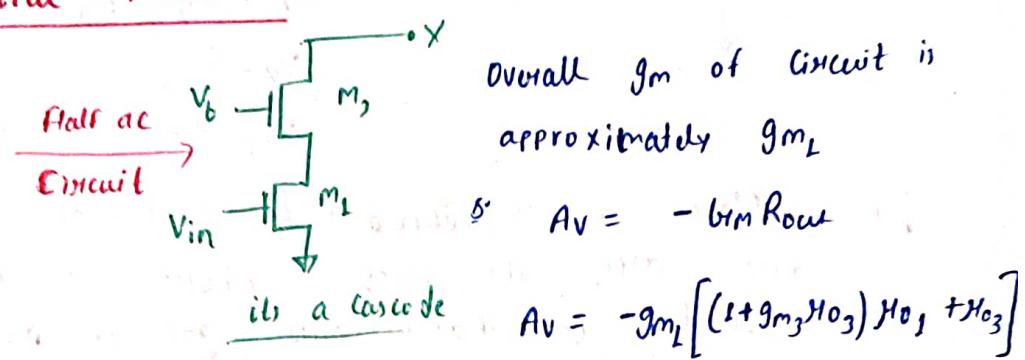
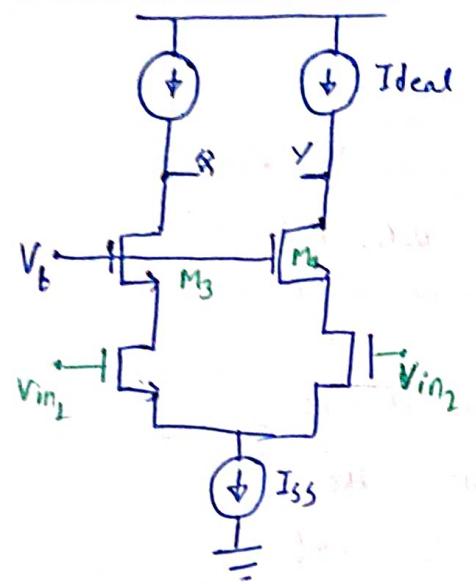
Differential Pair with Current Source Loads :-



- Bias mos properly.
- Here we have to consider channel length modulation otherwise gain will be ∞ so take practical care.
- Small signal circuit is :

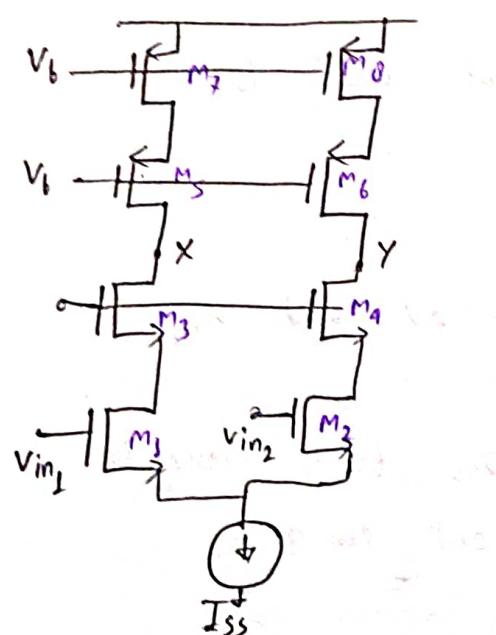


High Gain Differential Pairs :- Differential Pair with cascodes:



Now Implementing this current source also using P-type current source. Gain will be reduced because it will have some finite Trans. O/p resistance. Also called

Telescopic Cascode :



$$Av = -6gmR_{out}$$

$$6gm = \text{Approximately equal to } gm_1$$

$$R_{out} = R_{ncascade} || R_{pcascade}$$

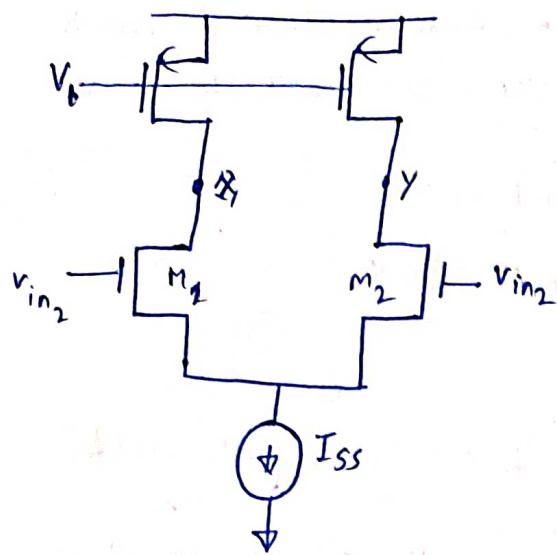
$$R_{ncascade} = [(1 + gm_3H03)H01 + H03]$$

$$R_{pcascade} = [(1 + gm_2H02)H05 + H05]$$

Here we have assumed (M_7, M_8) , (M_5, M_6) , (M_3, M_4) , (M_1, M_2) are matched. Then we will be able to take common same term while calculating $V_x - V_y$.

II Differential Pair with Active Load:

A differential pair is:



Suppose for further stage in our system we have a stage which takes differential input. did not

So we could connect only to \bar{x} and make y floating.

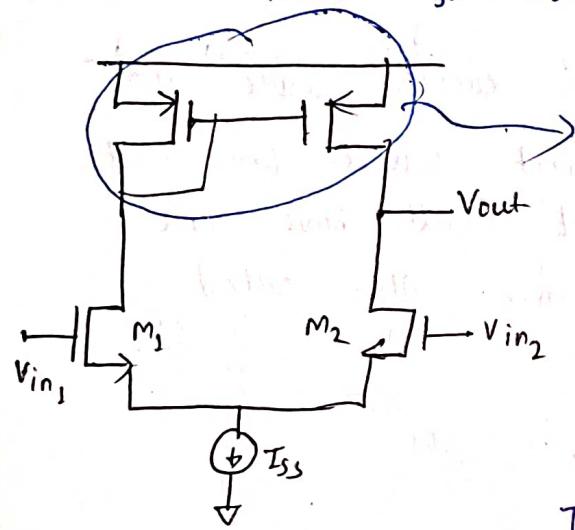
We know:

$$V_x = -g_m H_{out}$$

Let M_1, M_2 are symmetric

$$\frac{V_x - V_y}{V_{in_1} - V_{in_2}} = \frac{2V_n}{V_{in_1} - V_{in_2}}$$

The voltage is reduced to half of its original value.
So these are the cases where we need diff. pair with active load so that our gain is not compromised.



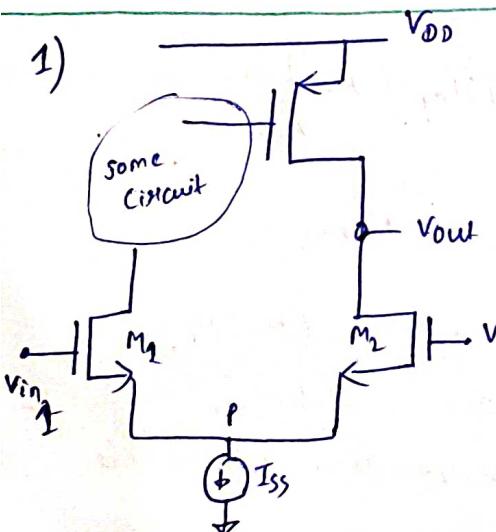
Current mirror but it is different because here the reference current is not constant, it varies according to Biasing of M_1 .

To understand this we will do

some analysis.

Intuitive Observations:

1)



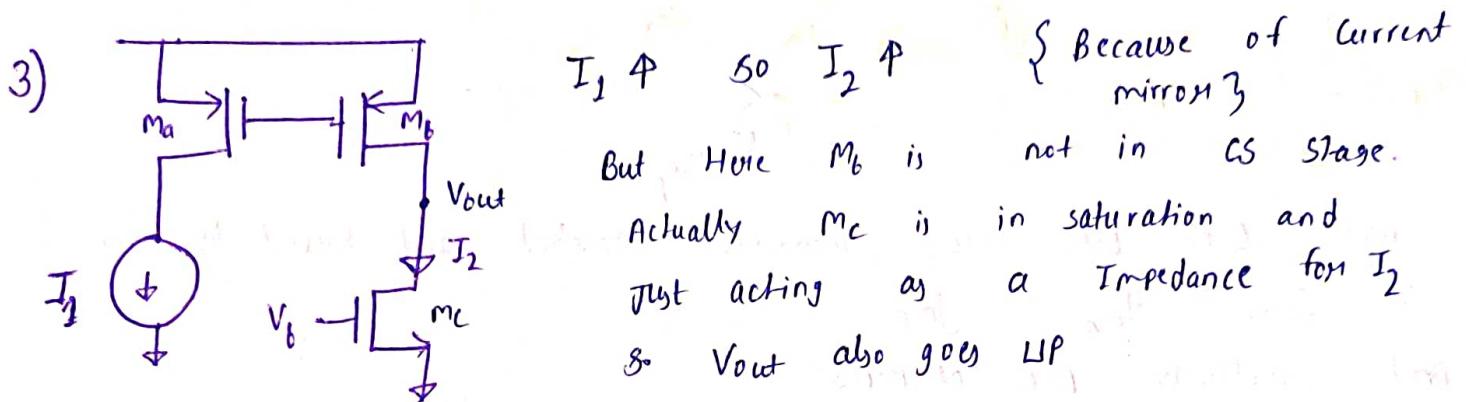
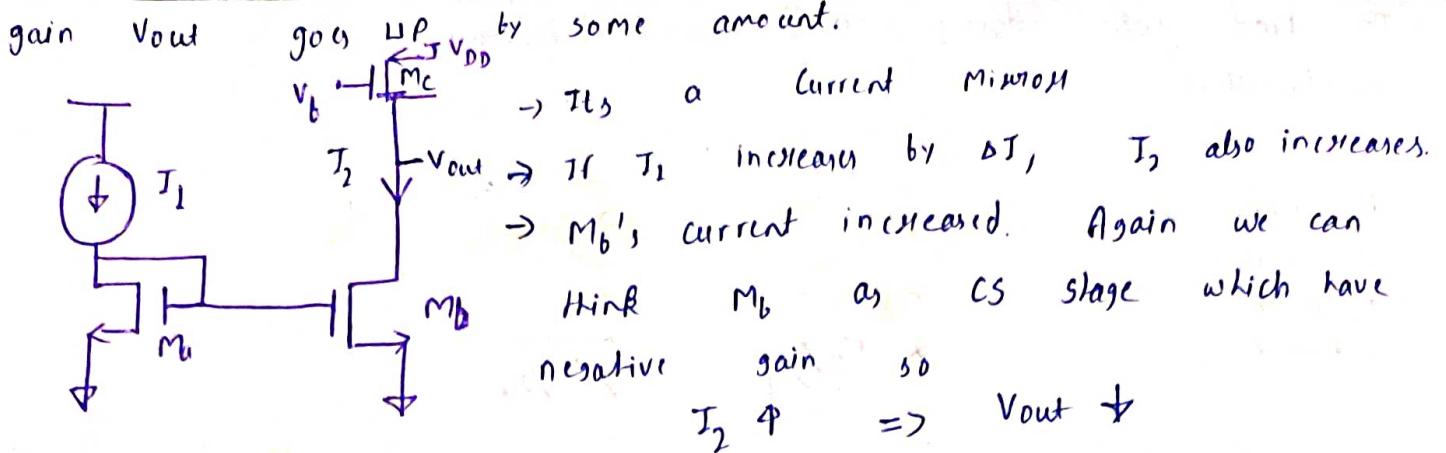
let V_{in_1} goes up by ΔV and V_{in_2} goes down by ΔV .

$\rightarrow V_{in_1}$ goes up so I_{ss} flows more to the left (from M_1) and less to M_2 .

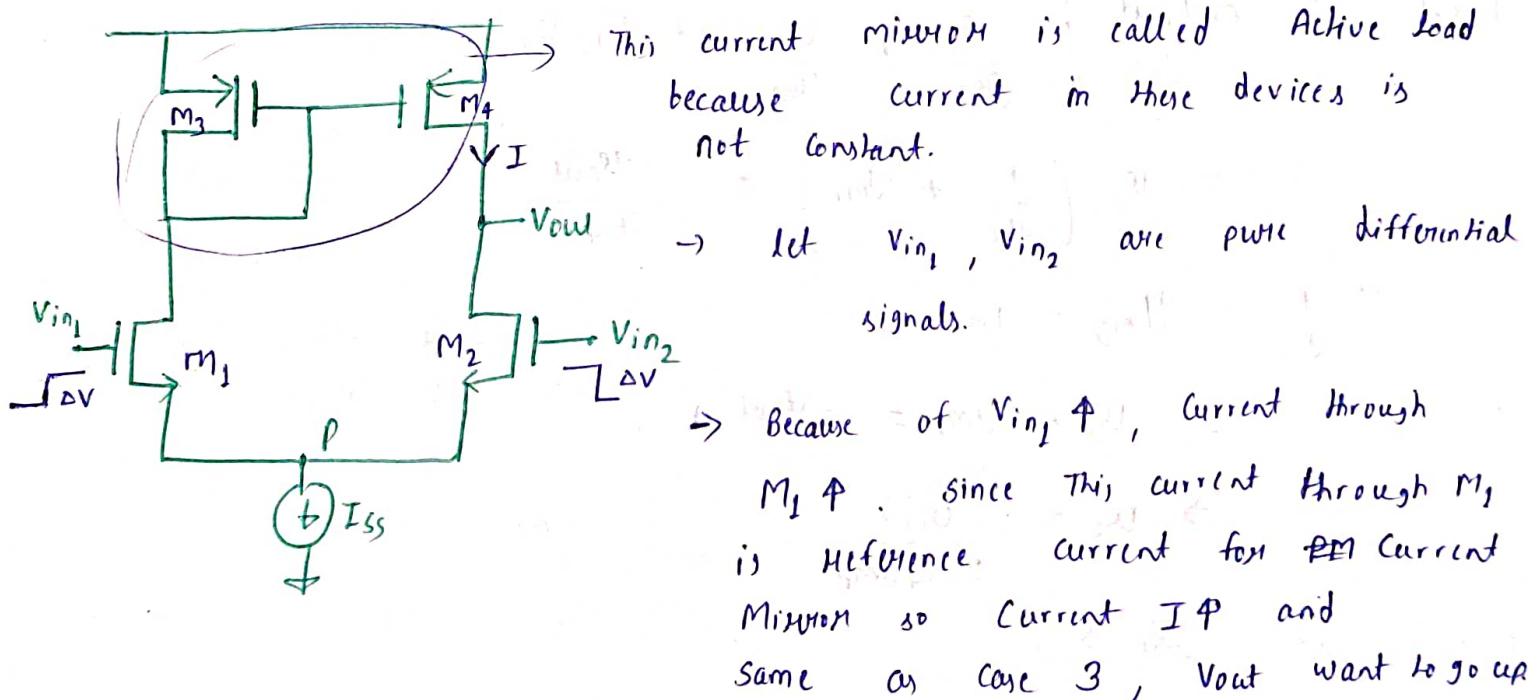
\rightarrow Now think it as common source stage for M_2 .

M_2 is biased at some current. i.e. $V_{cm in}$.

Now I_D goes down so due to negative



Now coming to our Diff-pair with Active load.

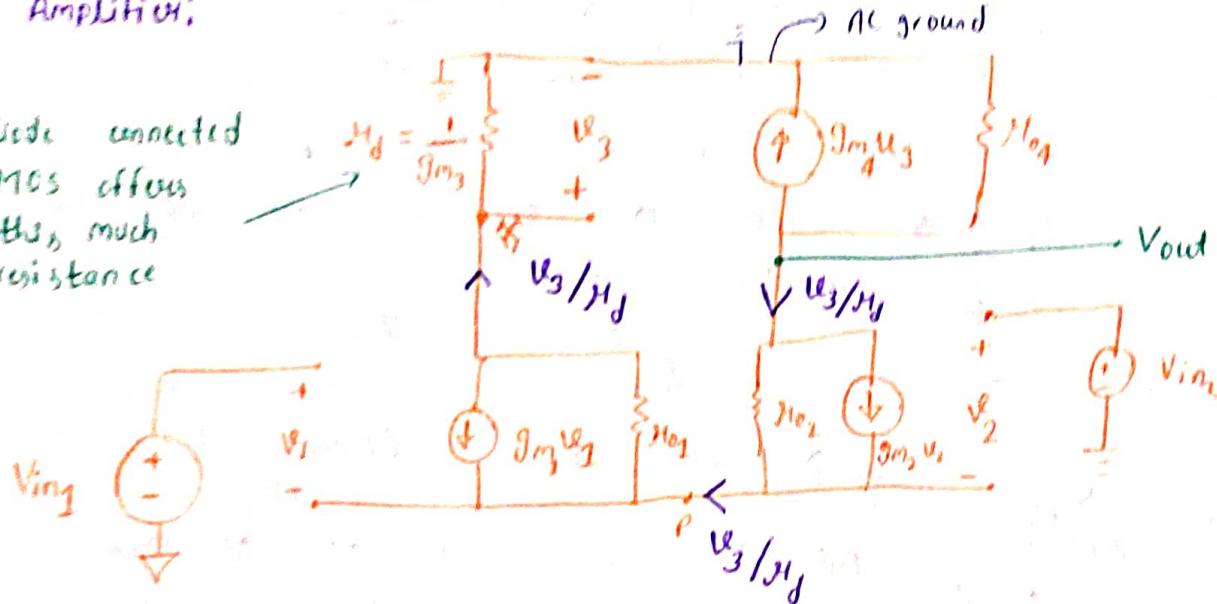


$\rightarrow V_{in_2}$ drops by ΔV , so current of M_2 wants to decrease and V_{out} acts as output common source stage for M_2 . Hence V_{out} want to go up.

so because both of V_{in_1}, V_{in_2} , output V_{out} wants to go up. M_1, M_2 are collaborating to increase V_{out} .

To find gain, doing small signal analysis of this Amplifier:

diode connected
MOS offers
this much
resistance



I will take both PMOS Transistor matched and biased by same V_B

$$\text{so } g_{m3} = g_{m4} = g_{mp}$$

And similarly for N-MOS:

$$g_{m1} = g_{m2} = g_{mn}$$

$$\text{K.C.L at output: } \frac{V_3}{H_D} + \frac{V_{out}}{H_{D4}} + g_{mp} V_3 = 0$$

$$\Rightarrow V_3 \left(\frac{1}{H_D} + g_{mp} \right) = - \frac{V_{out}}{H_{D4}}$$

$$\therefore \frac{1}{H_D} = g_{m3} = g_{mp}$$

$$\Rightarrow V_3 \times 2g_{mp} = - \frac{V_{out}}{H_{D4}}$$

$$\Rightarrow V_3 = \frac{-V_{out}}{2H_{D4}g_{mp}} \quad \dots \dots \text{(i)}$$

K.C.L at node X:

$$\frac{V_3}{H_D} + g_{m1} V_1 + \frac{V_3 - V_P}{H_{D2}} = 0$$

Subtract

And K.C.L at output (Nmos side)

$$-\frac{V_3}{H_D} + g_{m2} V_2 + \frac{V_{out} - V_P}{H_{D2}} = 0$$

$g_{m1} = g_{m2} = g_{mn}$

$$\therefore \frac{2V_3}{H_D} + g_{mn}(V_1 - V_2) + \frac{V_3}{H_{D1}} - \frac{V_{out}}{H_{D2}} - V_P \left(\frac{1}{H_{D1}} - \frac{1}{H_{D2}} \right) = 0$$

OLH both NMOS matched so $\mu_{o1} = \mu_{op}$

$$\frac{2U_3}{\partial I_D} + g_{mn}(U_1 - U_2) + \frac{\partial I_D}{\partial U_1} - \frac{\partial U_{out}}{\partial U_1} = 0$$

Now since

$$U_1 + U_p = U_{in1} \quad \text{and} \quad U_2 + U_p = U_{in2}$$

$$\therefore U_1 - U_2 = U_{in1} - U_{in2}$$

And also put U_3 's value from equation - (i) :

$$\frac{2}{\partial I_D} \left(\frac{-U_{out}}{2\mu_{o1} g_{mp} \mu_{op}} \right) + g_{mn}(U_1 - U_2) + \left(\frac{-U_{out}}{2\mu_{o1} g_{mp} \mu_{op}} \right) - \frac{U_{out}}{\partial U_1} = 0$$

$$\Rightarrow U_{out} \left(\frac{-1}{\mu_{o1}} - \frac{1}{2\mu_{o1} g_{mp}} - \frac{1}{\mu_{op}} \right) = -g_{mn}(U_{in1} - U_{in2})$$

Very big so neglect this term

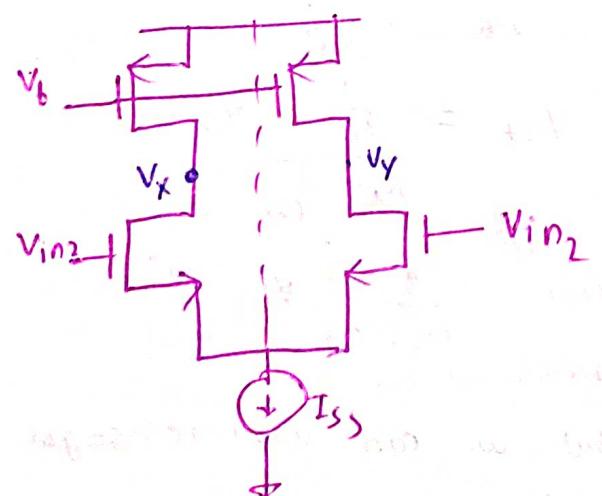
$$\Rightarrow \frac{U_{out}}{U_{in1} - U_{in2}} = \frac{g_{mn}}{\left(\frac{1}{\mu_{o1}} + \frac{1}{\mu_{op}} \right)}$$

Basically μ_{o1} is o/p resistance of N mos so μ_{o1} and $\mu_{op} = \mu_{op}$

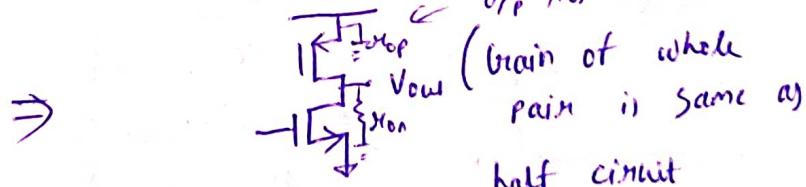
$$\Rightarrow \frac{U_{out}}{U_{in1} - U_{in2}} \approx g_{mn} \times \left(\mu_{on} || \mu_{op} \right)$$

$$\Rightarrow A_V \underset{\text{differential pair}}{\underset{\text{with active load}}{\approx}} g_{mn} (\mu_{on} || \mu_{op})$$

Even after we are using only one terminal for taking output still it is giving almost same gain as symmetrical differential pair.



Symmetrical Half circuit is o/p no. of pmos



$$A_V = \frac{V_x - V_y}{V_{in1} - V_{in2}} = -g_{mn} (\mu_{on} || \mu_{op})$$

OLN both NMOS - matched so $\mu_{o1} = \mu_{op}$

$$\frac{2U_3}{g_{M1}} + g_{mn}(U_1 - U_2) + \frac{U_3}{\mu_{o1}} - \frac{U_{out}}{\mu_{o1}} = 0$$

Now Since

$$U_1 + U_p = U_{in1} \quad \text{and} \quad U_2 + U_p = U_{in2}$$

$$\therefore U_1 - U_2 = U_{in1} - U_{in2}$$

And also put U_3 's value from equation -(i):

$$\frac{2}{g_{M1}} \left(\frac{-U_{out}}{2\mu_{o1}g_{mp}\mu_{o1}} \right) + g_{mn}(U_1 - U_2) + \left(\frac{-U_{out}}{2\mu_{o1}g_{mp}\mu_{o1}} \right) - \frac{U_{out}}{\mu_{o1}} = 0$$

$$\Rightarrow U_{out} \left(\frac{-1}{\mu_{o1}} - \frac{1}{2\mu_{o1}g_{mp}\mu_{o1}} - \frac{1}{\mu_{o1}} \right) = -g_{mn}(U_{in1} - U_{in2})$$

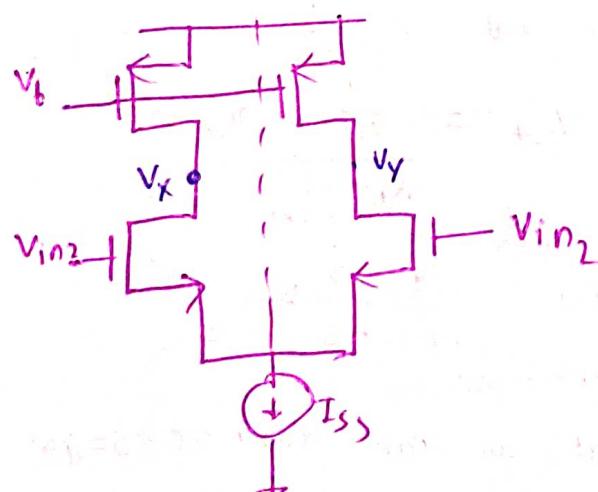
$$\Rightarrow \frac{U_{out}}{U_{in1} - U_{in2}} = \frac{g_{mn}}{\left(\frac{1}{\mu_{o1}} + \frac{1}{2\mu_{o1}g_{mp}\mu_{o1}} \right)}$$

very big so neglect this term
Basically μ_{o1} is o/p μ_{in} of all mos so g_{mn}
and $\mu_{o1} = \mu_{op}$

$$\Rightarrow \frac{U_{out}}{U_{in1} - U_{in2}} \approx g_{mn} \times (\mu_{on} || \mu_{op})$$

$$\Rightarrow A_V \underset{\text{differential pair}}{\approx} g_{mn} (\mu_{on} || \mu_{op})$$

Even after we are using only one terminal for taking output still it is giving almost same gain as symmetrical differential pair.

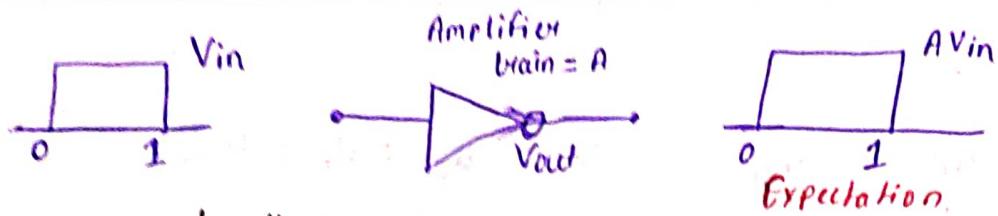


Symmetrical Half circuit is o/p nos. of pmos
 \Rightarrow

(Brain of whole pair is same as half circuit)

$$A_V = \frac{V_x - V_y}{V_{in2} - V_{in1}} = -g_{mn} (\mu_{on} || \mu_{op})$$

Unit : 3 Frequency Response

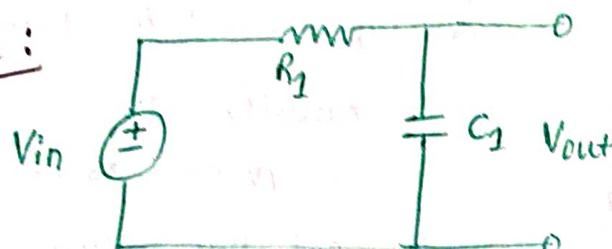


But in real there are some bandwidth limitations and that's why o/p is like



Mostly capacitor is responsible for slowness of circuit.
(parasitic capacitance in MOS).

Example :



$$V_{out} = V_1 (1 - e^{-t/\tau})$$

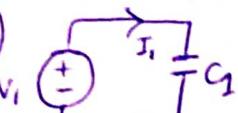
$$\tau = R_1 C_1$$

To increase the speed, we must minimize $R_1 C_1$.

Some Circuit Theory Concepts :

Time Domain

frequency Domain

1) 

$$I_1 = C \cdot \frac{dV_1}{dt}$$

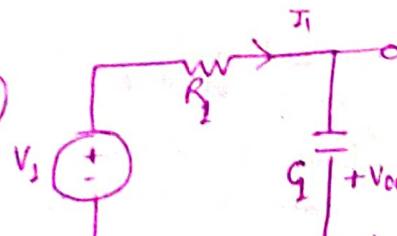
$$I_1 = (C_s) V_1$$

2) 

$$V_1 = I_1 R_1 + \frac{1}{C_1} \int I_2 dt$$

Converted to Algebraic

$$V_1 = I_1 R_1 + \frac{I_2}{s C_1}$$

3) 

$$I_1 = \frac{C dV_{out}}{dt}$$

$$R_1 C \frac{dV_{out}}{dt} + V_{out} = V_1$$

Converted to Algebraic eqn from differential eqn

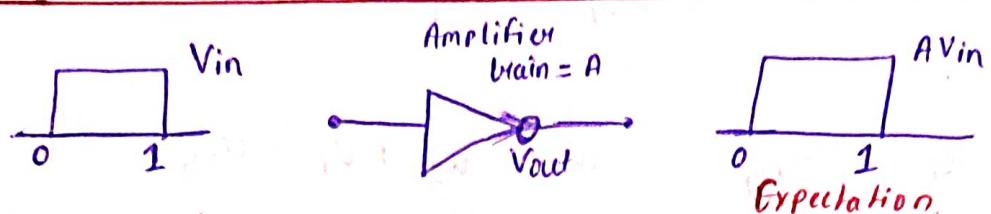
In f-domain

$$V_{out} = \frac{1}{C s} V_{in}$$

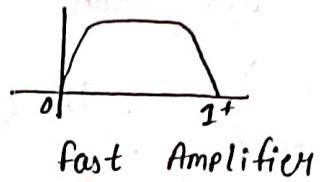
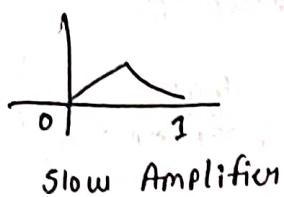
$$V_{out} = \frac{1}{s + j \omega R_1 C_1} V_{in}$$

's' is generally a complex frequency but we can assume $s = j\omega$ if the signal of interest are sinusoids.

Unit : 3 Frequency Response

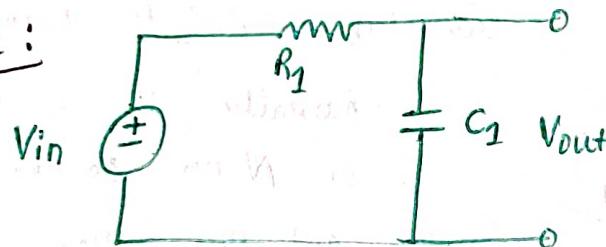


But in real there are some bandwidth limitations and that's why o/p is like



Mostly capacitor is responsible for slowness of circuit (parasitic capacitance in MOS).

Example :



$$V_{out} = V_1 (1 - e^{-t/\tau})$$

$$\tau = R_1 C_1$$

To increase the speed, we must minimize $R_1 C_1$.

Some Circuit Theory Concepts :

Time Domain

frequency Domain

1) $I_1 = C \cdot \frac{dV_1}{dt}$

$$I_1 = (C_s) V_1$$

2) $V_1 = I_1 R_1 + \frac{1}{C_1} \int I_1 dt$

$$V_1 = I_1 R_1 + \frac{I_1}{s C_1}$$

Converted to Algebraic

3) $I_1 = \frac{C dV_{out}}{dt}$

$$R_1 C \frac{dV_{out}}{dt} + V_{out} = V_1$$

In f-domain

$$V_{out} = \frac{1}{C s} V_{in}$$

Converted to Algebraic eqn from differential eqn.

$$V_{out} = \frac{1}{1 + s C R_1} V_{in}$$

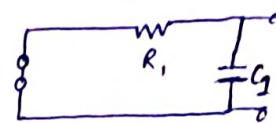
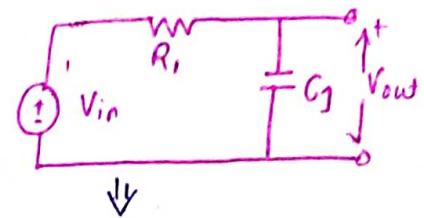
's' is generally a complex frequency but we can assume $s=j\omega$ if the signals of interest are sinusoids.

finding poles by Inspection :- We can assume that each node in the signal path contributes to

a pole. To Approximate the pole:

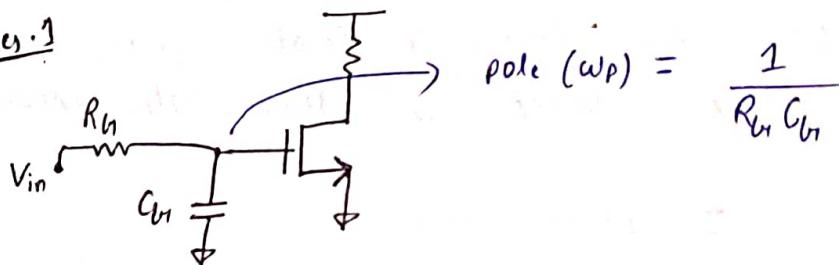
- (a) find Resistance from that pole to ac GND.
- (b) find the capacitance from that node to ac GND.
- All independent sources = 0

$$\omega_p = \frac{1}{RC}$$



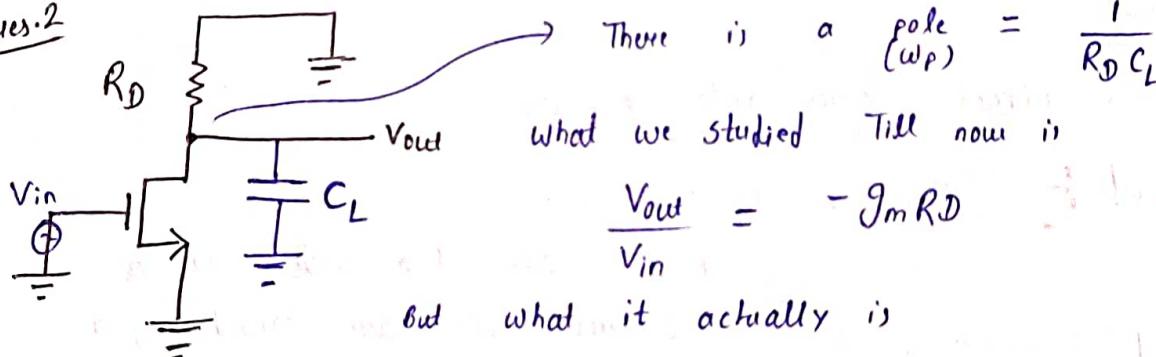
However this pole comes negative, but during Bode plot plotting we draw it at positive axis because generally in magnitude plot complex number's magnitude have form $\sqrt{\omega_p^2 + n}$ type so this square term manages that.

Ques.1



$$\text{pole } (\omega_p) = \frac{1}{R_b1 C_{b1}}$$

Ques.2



$$\text{There is a pole } (\omega_p) = \frac{1}{R_D C_L}$$

what we studied Till now is

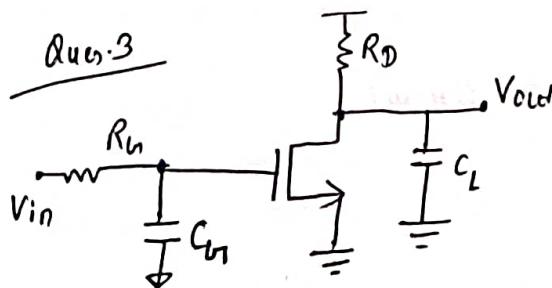
$$\frac{V_{out}}{V_{in}} = -g_m R_D$$

But what it actually is

$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_D}{1 + \frac{s}{\omega_p}} = \frac{-g_m R_D \omega_p}{s + \omega_p}$$

That's why frequency effects gain. Generally the reason in which operate gain is $-g_m R_D$. And yes there is a effect if we operate at unusual frequencies.

Ques.3



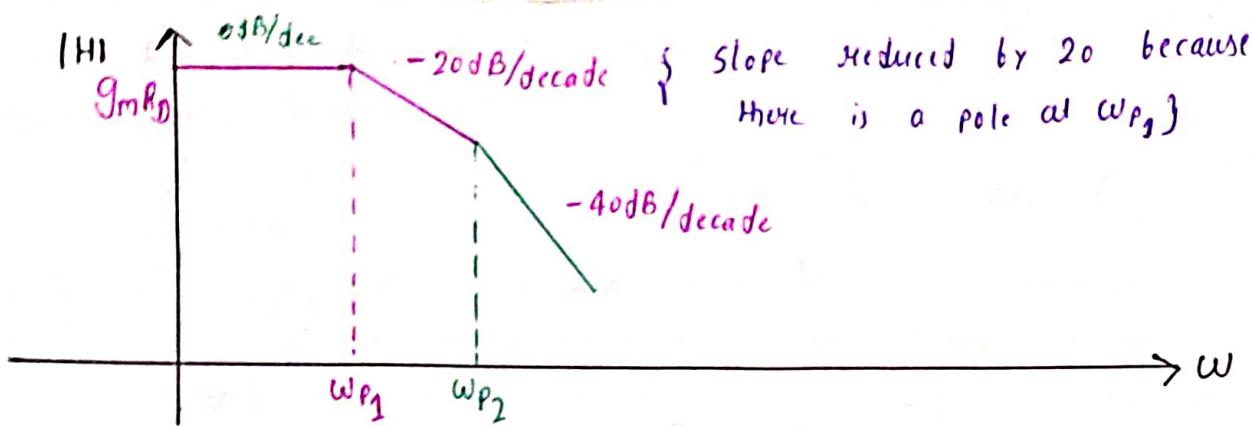
$$\omega_{p1} = \frac{1}{R_b1 C_{b1}}$$

$$\omega_{p2} = \frac{1}{R_D C_L}$$

Suppose $\omega_{p1} < \omega_{p2}$

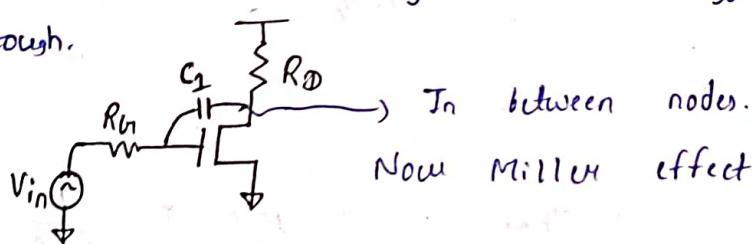
and these ω_{p1}, ω_{p2} are basically corner frequencies for our bode plot.

Plotting Magnitude frequency response:



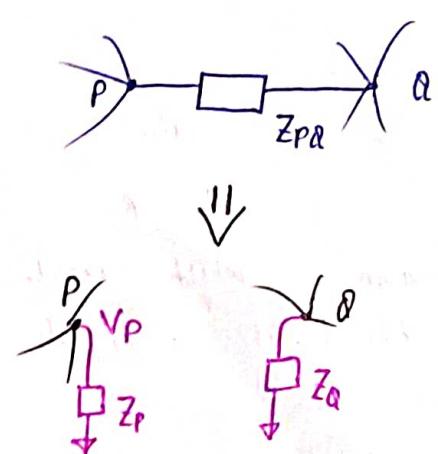
$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_D}{\left(1 + \frac{s}{\omega_{p_1}}\right) \left(1 + \frac{s}{\omega_{p_2}}\right)}$$

But a complication comes when there is a capacitor not connected to ground but in between nodes. Since BJT's or MOS devices's small signal model have dependent voltage source so here pole approximation becomes tough.



Now Miller effect comes into picture.

Miller Effect :- (Miller's Theorem)



P, Q are two nodes of a circuit. We are considering a Z_{PQ} impedance connected between them. Now we want a impedance which deminates this Z_{PQ} .

Current drawn from P is:

$$(i) \frac{V_p - V_Q}{Z_{PQ}} \text{ In first circuit.}$$

$$(ii) \frac{V_p}{Z_p} \text{ in second circuit.}$$

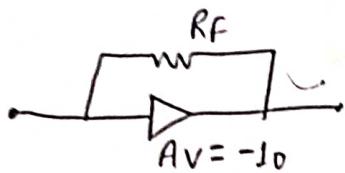
And these currents need to be equal:

$$\text{So, } \frac{V_p - V_Q}{Z_{PQ}} = \frac{V_p}{Z_p}$$

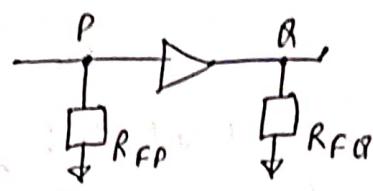
$$\Rightarrow Z_p = \frac{Z_{PA}}{1 - \frac{V_Q}{V_P}}$$

similiarly $Z_Q = \frac{Z_{PA}}{1 - \frac{V_P}{V_Q}}$

Question 1



\Rightarrow



Find R_{FP} , R_{FQ} .

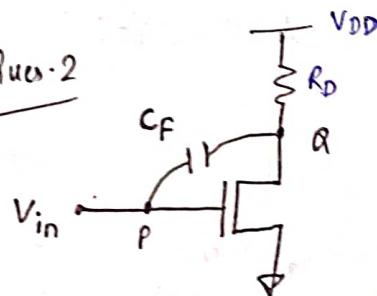
Given $AV = -10$

$$\therefore \frac{V_Q}{V_P} = -10$$

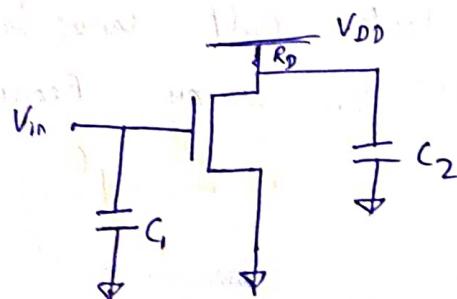
Hence $R_{FP} = \frac{R_F}{1 - (-10)} = \frac{R_F}{11}$ and $R_{FQ} = \frac{R_F}{1 + 10} = \frac{R_F}{11}$

Observation :- We can even design a negative resistance if AV is +ve and > 1 .

Ques 2



Decompose
This C_F to
broad capacitances



$$AV = -g_m R_D$$

$$\therefore \frac{1}{s C_1} = \frac{1}{s C_F} / \left(1 - (-g_m R_D) \right) = \frac{1}{s (C_F (1 + g_m R_D))}$$

$$\therefore C_1 = C_F (1 + g_m R_D)$$

$$\text{And } C_2 = C_F \left(1 + \frac{1}{g_m R_D} \right)$$

But what Assumption we made here:

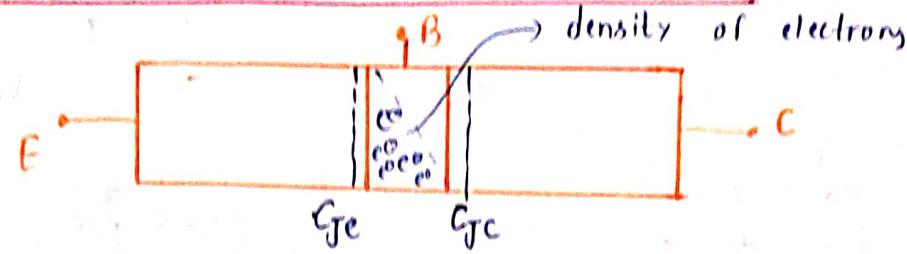
$$-g_m R_D = \frac{V_Q}{V_P}; \text{ if we neglect all the capacitances}$$

Because of this approximation
Here actual gain will be changed little bit in comparison to $-g_m R_D$.

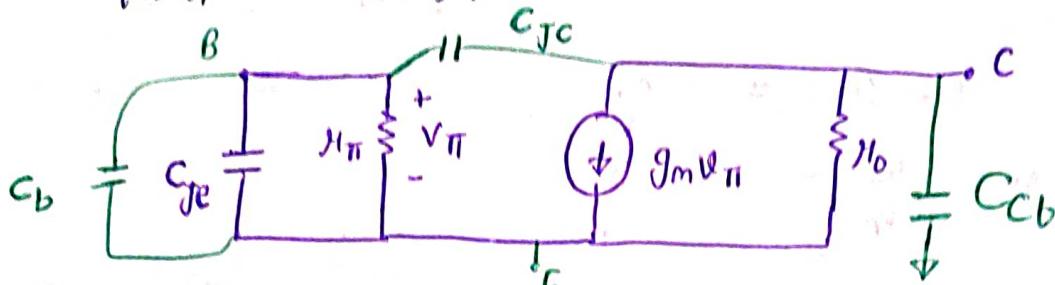
Cautions: \rightarrow Miller's Approximation has induced a new pole.

\rightarrow Miller's Approximation has eliminated the zero.

High frequency Model of BJT :-



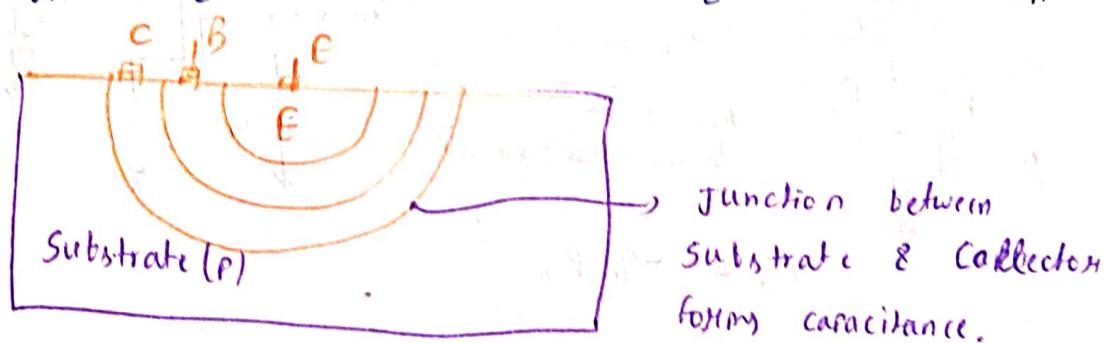
So High frequency Model is :



C_{jc} → ~~Collector~~ junction capacitance.

C_{je} → ~~Collector~~ Emitter Junction Capacitance.

C_{cb} → collection - Bulk Capacitance. It is there only if BJT is built on wafer. Because on wafer it look like:



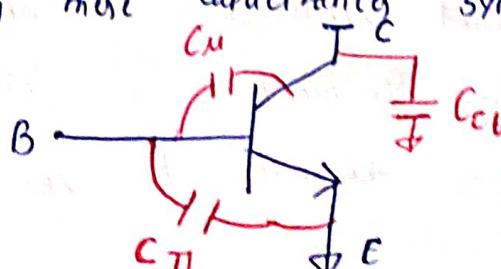
C_b : To Turn on the device we have to deliver a charge to Base & and \wedge . That is between Base & emitter.
So there is a C_b capacitance.

For Historical Reasons:

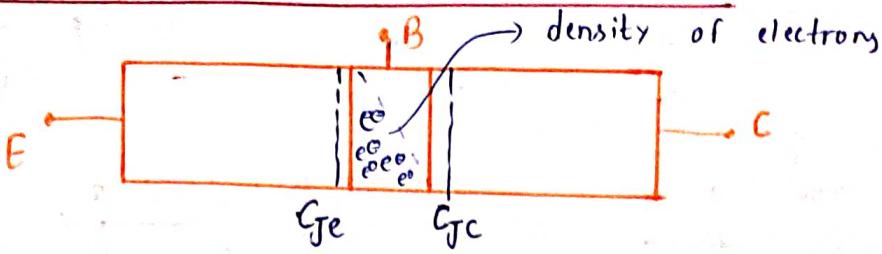
We call $C_{jc} = C_u$ and $C_{je} = C_d$

and $C_n = C_b + C_{je}$

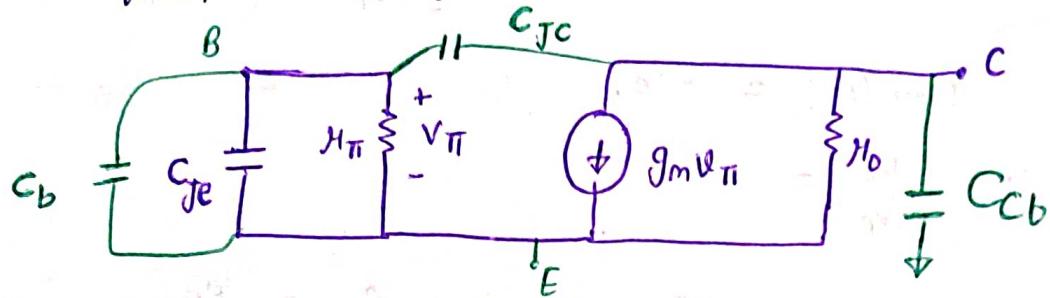
So Including these Capacitance symbol of BJT is:



High frequency Model of BJT :-



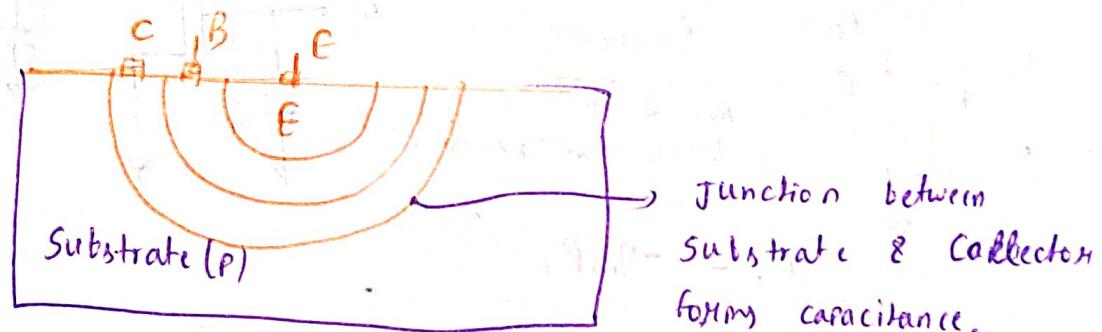
So High frequency Model is :



C_{jc} → Collector junction capacitance.

C_{je} → ~~Collector~~ Emitter Junction Capacitance.

C_{cb} → collector - Bulk Capacitance. It is there only if BJT is built on wafer. Because on wafer it look-like:



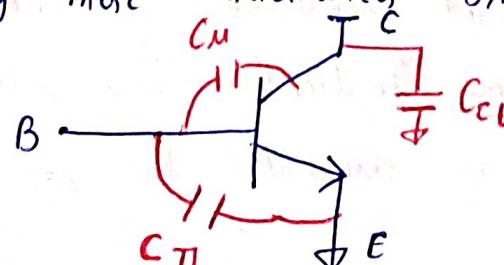
C_b : To Turn on the device we have to deliver a charge to Base & and Δ . That is between Base & emitter.
To Turn off take that charge away.
So there is a C_b capacitance.

For Historical Reasons:

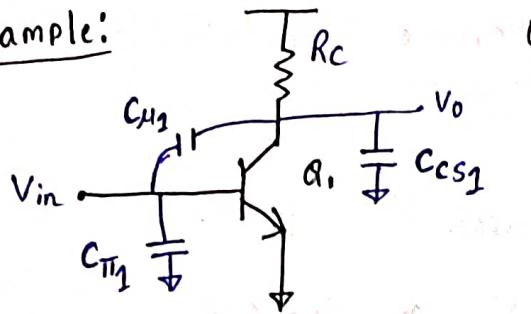
We call $C_{jc} = C_u$

and $C_{pi} = C_b + C_{je}$

So Including these Capacitance symbol of BJT is:



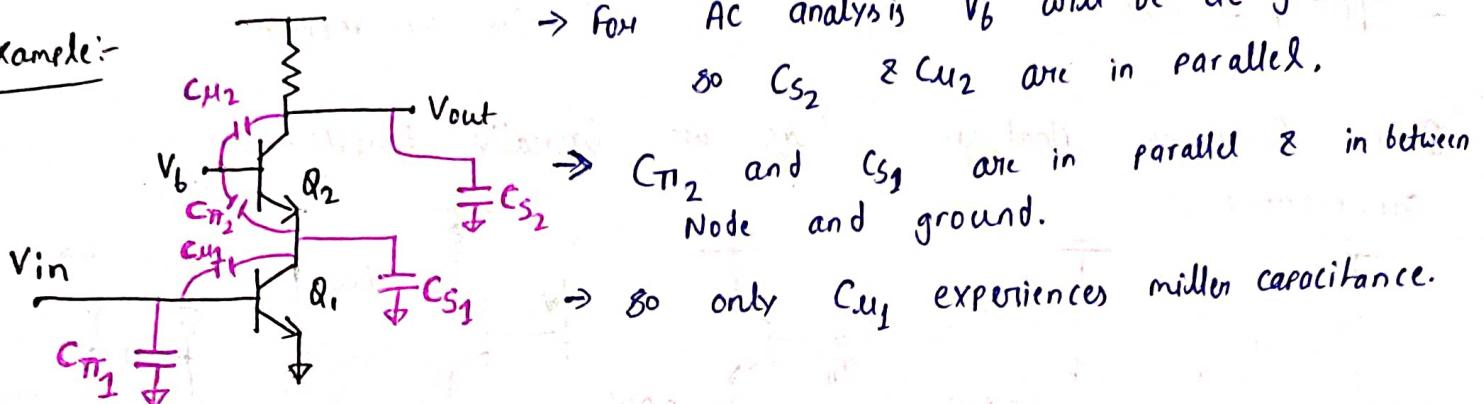
Example:



which capacitor experiences Miller multiplication.

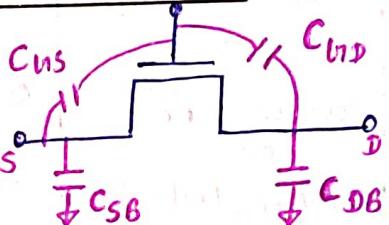
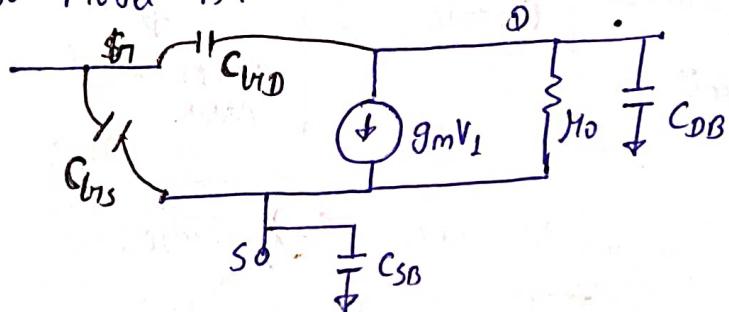
Here C_{ui2} experiences Miller multiplication, because it is connected between output & input. No node is grounded.

Example:-

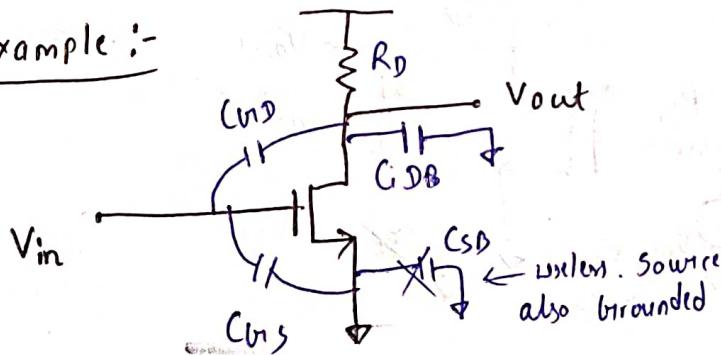


High-frequency Model of MOSFETs :-

So Model is:

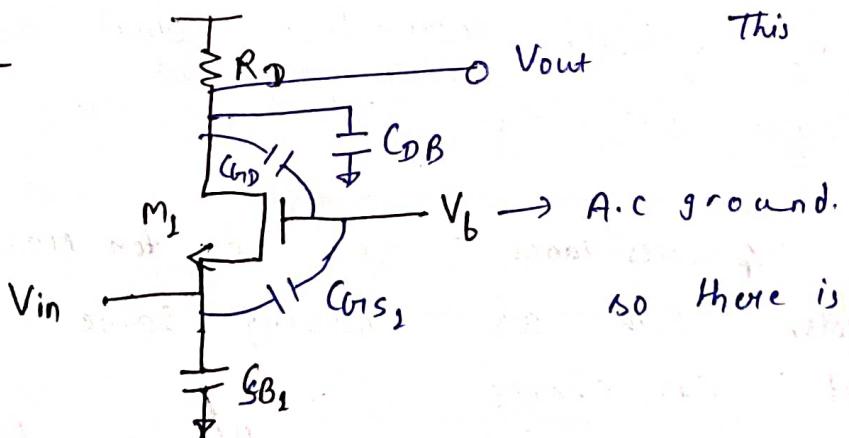


Example:-



This is Common gate stage.

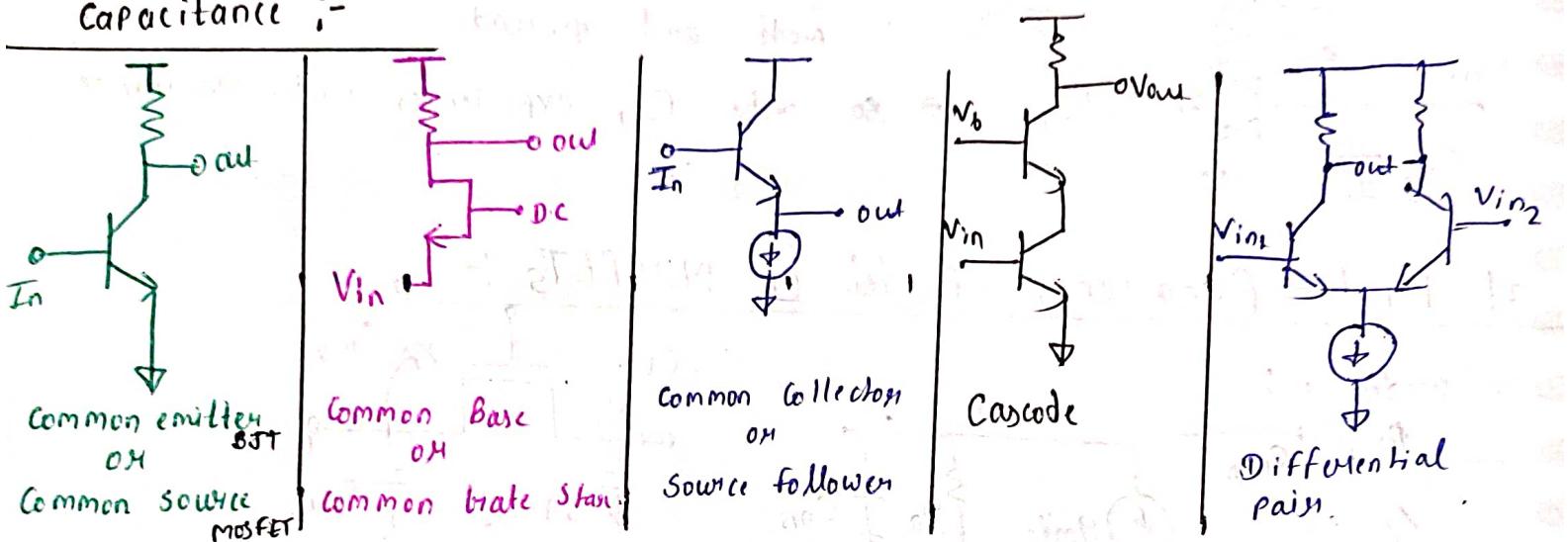
Example:-



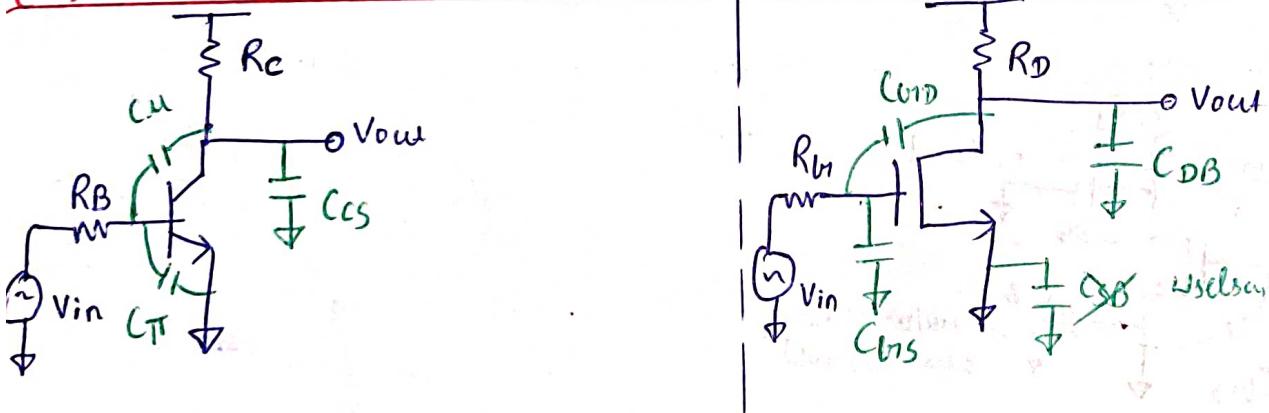
General Procedure for Frequency Response Computation :-

- Draw the circuit
- Draw all of the device capacitances.
- Remove or Merge capacitances if possible.
- Compute the Transfer function $H(s)$. } we can also find poly by inspection.
- $|H(s)| \Rightarrow$ Plot.

Our Previous Analysis where we Basically ignored Capacitance :-

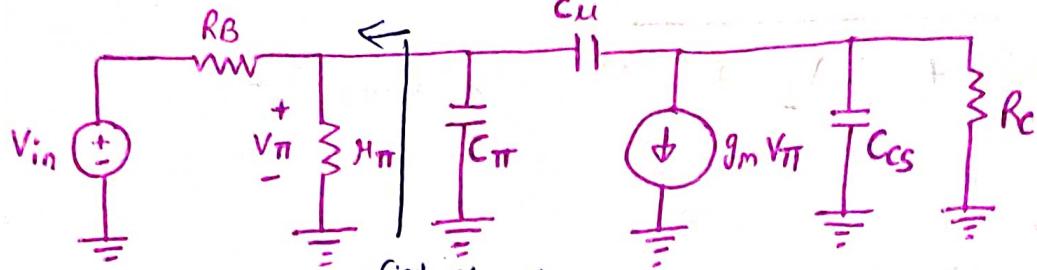


(1) Common emitter (BJT) OR Common source (CS) Stage:



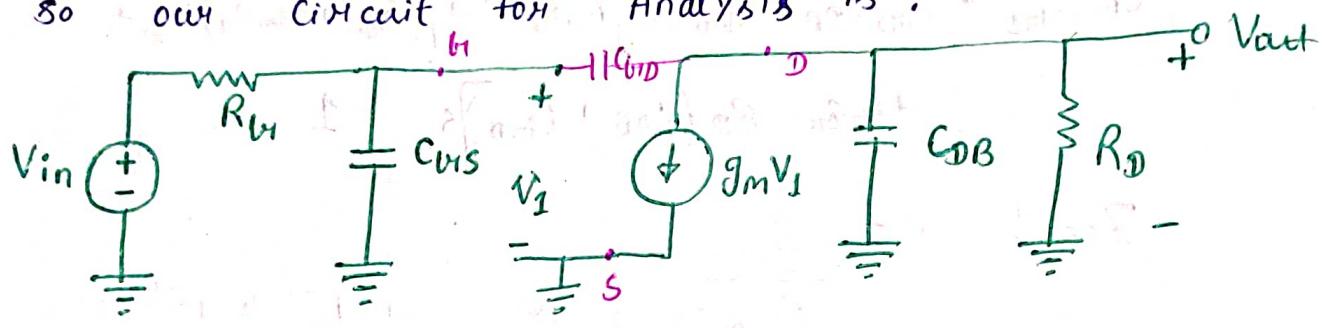
- Those R_B & R_{in} Basically represents internal resistance of source. Sometimes they also represent Resistance from previous Stage.
- BJT's internal I/p resistance = 2π but for MOSFET it is ∞ . so Basically Both are having same topology except this change.
- so we will do analysis such that our results are valid for both.

small signal model of BJT is :



Now Both circuit loops same
 \rightarrow In place of C_{π} , C_{BS} is there.
 \rightarrow C_{UB} & C_{BD} equivalent.
 \rightarrow $C_{CS} = C_{DB}$.

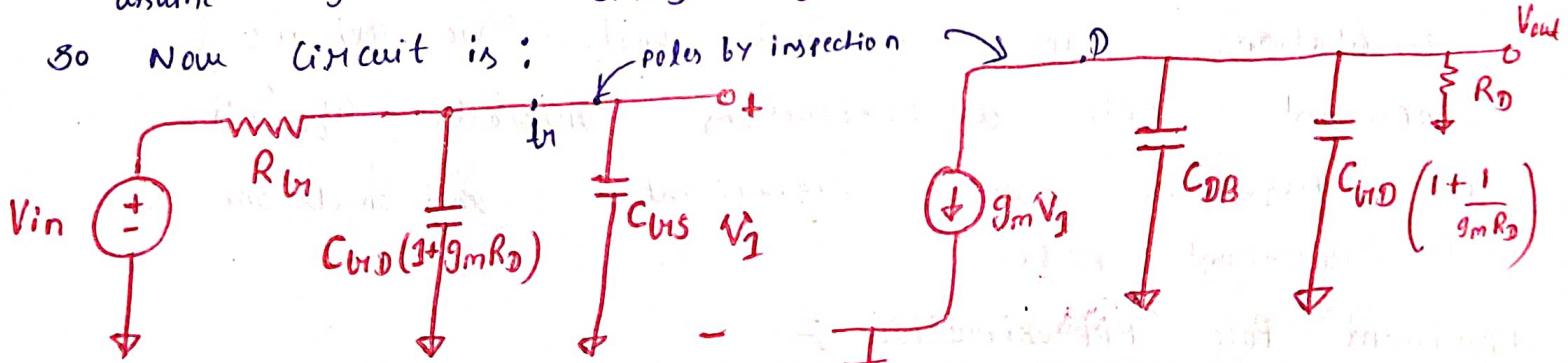
So our circuit for analysis is :



Approach I: finding the poles by inspection:

C_{UD} is between two points not ac ground so Miller effect is there. The approximation which we make here we assume gain $= -g_m R_D$ (which is low frequency gain basically)

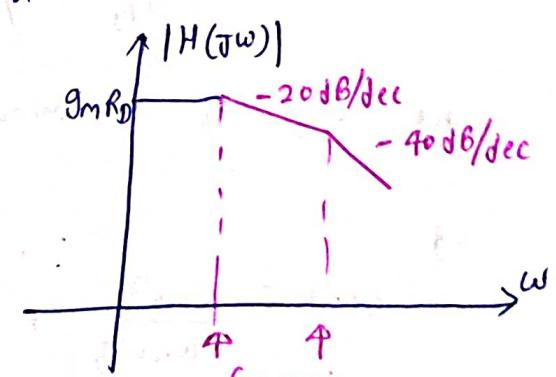
So Now circuit is :



There are two nodes basically. At node b_1 and Node D :

$$\omega_{p_{b_1}} = \frac{1}{R_{B1} [C_{BS} + C_{UD}(1+g_m R_D)]}$$

$$\omega_{p_D} = \frac{1}{R_D [C_{DB} + C_{UD}(1+\frac{1}{g_m R_D})]}$$



This approx also eliminated one zero.

Approach II: Exact Analysis :- K.C.L at output:

$$\frac{V_{out}}{R_D} + V_{out} C_{DB} s + g_m V_1 + (V_{out} - V_1) C_{BD} s = 0$$

K.C.L at Node b1:

$$\frac{V_{in} - V_1}{R_{in}} = (V_1 - V_{out}) C_{BD} s + V_1 C_{BIS} s$$

eliminate V_1 , find V_{out} in terms of V_{in} :

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{(C_{BD} s - g_m) R_D}{[C_{BIS} C_{BD} + C_{BIS} C_{DB} + C_{BD} C_{DB}] R_{in} R_D s^2 + [(C_{BD}(1+g_m R_D))' R_{in} + R_{in} C_{BIS} + R_D (C_{DB} + C_{BD})] s + 1}$$

- Zero: $\omega = \frac{g_m}{C_{BD}}$

This is of 10^{-6} to 10^{-12} order

so this ω is very very High.

And at that gain almost decayed so because of poles
so Typically Unimportant.

→ To analyse This transfer function we need to use simulations. for manual analysis we utilise Dominant pole approximations. Generally ω_{b1}, ω_p pole frequency vary significantly and small one is Dominant pole.

Dominant Pole Approximation :-

$$\text{Let } D(s) = \left(\frac{s}{\omega_{p_1}} + 1 \right) \left(\frac{s}{\omega_{p_2}} + 1 \right); \text{ where } \omega_{p_1} \text{ & } \omega_{p_2} \text{ are poles.}$$

Let ω_{p_1} is Dominant pole, then $\omega_{p_1} \ll \omega_{p_2}$

$$\Rightarrow \frac{1}{\omega_{p_1}} \gg \frac{1}{\omega_{p_2}}$$

$$D(s) = \frac{s^2}{\omega_{p_1} \omega_{p_2}} + s \left(\frac{1}{\omega_{p_1}} + \frac{1}{\omega_{p_2}} \right) + 1$$

$$D(s) \simeq \frac{s^2}{w_{p_1} w_{p_2}} + \left(\frac{1}{w_{p_1}} + \frac{1}{w_{p_2}} \right) s + 1 = 0$$

$\therefore w_{p_1}$ = Reciprocal of coefficient of s

$$w_{p_1} = \frac{1}{[C_{GD}(1+g_m R_D)R_{in} + C_{BS}R_{in} + (C_{GD} + C_{DB})R_D]}$$

When we performed pole by inspection method then also we got almost same term, just $(C_{GD} + C_{DB})R_D$ time constant was not there.

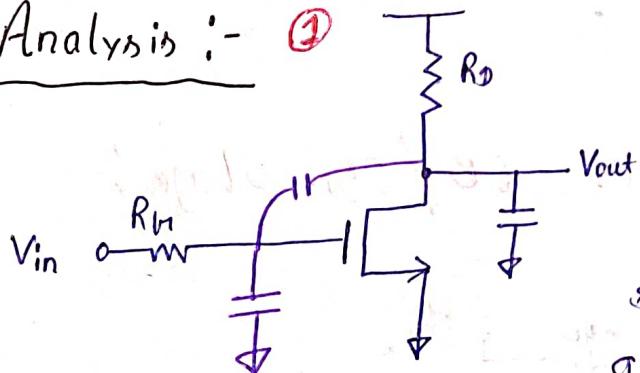
Observations :- ① if $s=0$, $\frac{V_{out}}{V_{in}} = -g_m R_D$

② if $s \rightarrow \infty$, $\frac{V_{out}}{V_{in}} \rightarrow 0$

③ We are having 3 capacitors, but a second order Transfer function, why?

Because voltage across C_{GD} + voltage across C_{BS} = voltage across C_{DB}
so There is a relation.

Analysis :- ① What happens if $w \rightarrow 2w$ maintaining I_D constant.

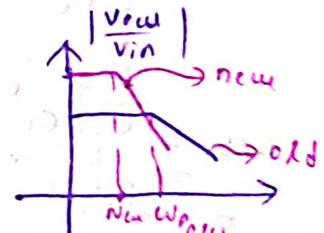


The basic concept from digital IC design is: $\propto w$

so All Transistor Caps are doubled.

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D}$$

g_m gone up $\sqrt{2} g_m$



We know dominant pole is:

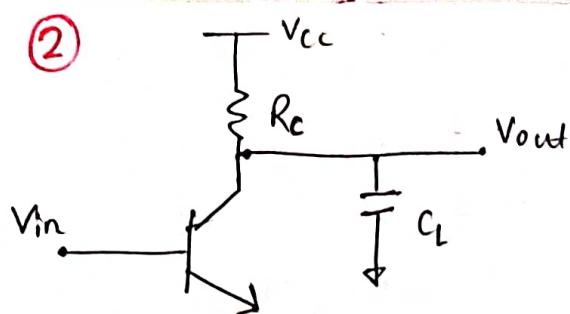
$$w_{p_1} = \frac{1}{[(\frac{1+g_m R_D}{\sqrt{2}}) \frac{C_{GD}}{2} + \frac{C_{BS}}{2}] R_{in} + (\frac{C_{GD}}{2} + \frac{C_{DB}}{2}) R_D}$$

$\rightarrow \therefore w_{p_1}$ is by at least by a factor of 2.

\rightarrow low frequency gain $-g_m R_D$ goes up by $\sqrt{2}$ factor.

\rightarrow To get High gain, there is a Tradeoff between gain & Bandwidth.

②



If $R_C \rightarrow \frac{R_C}{2}$, what happens?

I_C constant.

$$\text{Gain} = g_m R_C$$

so A_V reduced to $\frac{A_V}{2}$

$$B.W = \frac{1}{R_C C_L} \quad \text{so } B.W \text{ increased by factor of 2.}$$

so here $\text{Gain} \times B.W$ is constant.

③

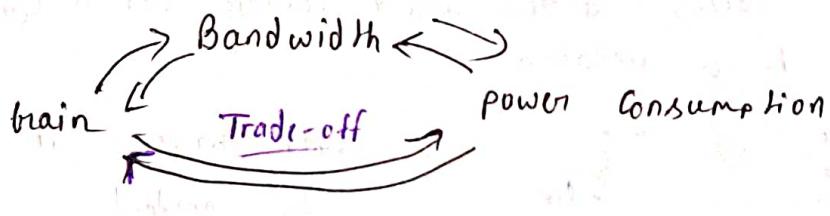
$$R_C \rightarrow \frac{R_C}{2}, \quad I_C \rightarrow 2I_C \quad \therefore g_m = \frac{I_C}{V_T} = 2 \times g_{m0}$$

Now Gain = constant

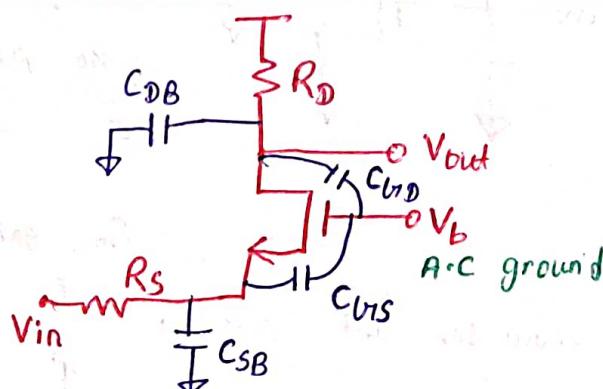
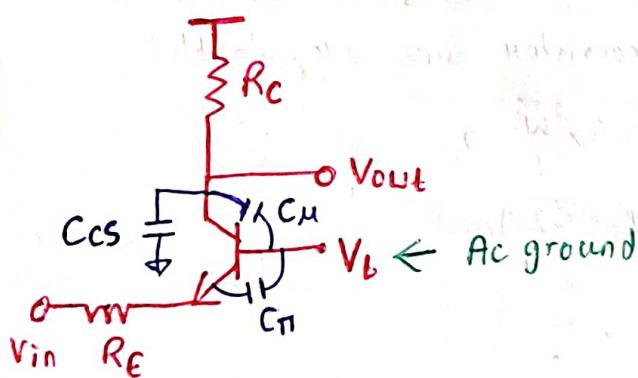
B.W = Doubled

so what is Trade-off Here. Actually I_C increased to $2I_C$ so power consumed is increased.

Conclusion:



2) Frequency Response of CB / CMOS Stage :-



CB stage \rightarrow No Miller effect.

\rightarrow Find the poly at input & output node by inspection.

At Input: Capacitor to A.C ground is C_{B1}

Resistance to A.C ground = $R_E \parallel \frac{1}{g_m}$

{ At emitter input
Resistance is not very high }

$$50 \quad \omega_{pin} = \frac{1}{C_{pi} \left(R_E \parallel \frac{1}{g_m} \right)}$$

At output: Resistance to AC ground = R_C
 Capacitance to AC ground = $C_{out} + C_{ES}$

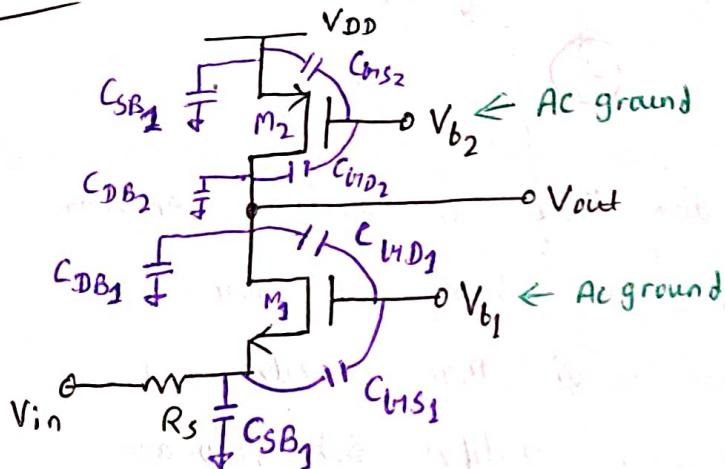
$$50 \quad \omega_{pout} = \frac{1}{R_C (C_{out} + C_{ES})}$$

This was for B.J.T Based CB stage. Now for CBF Stage.

$$\omega_{pin} = \frac{1}{\left(R_S \parallel \frac{1}{g_m} \right) (C_{BS2} + C_{BS1})}$$

$$8 \quad \omega_{pout} = \frac{1}{R_D (C_{DB1} + C_{DB2})}$$

Ques: For given amplifier find pole frequencies by Inspection:



\rightarrow So C_{BS1} & C_{BS2} are in parallel.

$\rightarrow C_{DB1}, C_{DB2}, C_{UD2}, C_{UD1}$ are in parallel.

$\rightarrow C_{BS1}$ & C_{BS2} off no use because They are in between ground and AC ground.

So there are two nodes basically where caps are present.

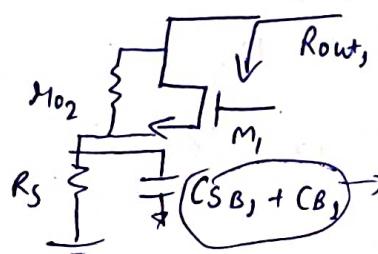
$$\omega_{pin} = \frac{1}{\left(R_S \parallel \frac{1}{g_m} \right) (C_{BS1} + C_{BS2})}$$

While seeing input impedance we made an approximation
 Here that $M_0 = 0$.

Now at output node: (i) $n=0$ then $M_0 \rightarrow 0$ so
 $\omega_{pout} \rightarrow 0$ (Not a practical case)

(ii) Here we have to consider C.C.M ($n \neq 0$)

$$R_{out1} = (1 + g_m M_0) R_S + M_0$$



Ignore this for time being. However in actual Rout is complex because of this but for

$$50 \quad W_{pin} = \frac{1}{C_{in} \left(R_E \parallel \frac{1}{g_m} \right)}$$

At output: Resistance to AC ground = R_C
Capacitance to AC ground = $C_{out} + C_{GS}$

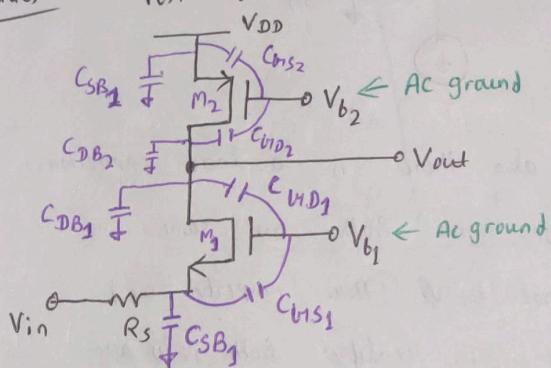
$$50 \quad W_{pout} = \frac{1}{R_C (C_{out} + C_{GS})}$$

This was for BJT Based CB stage. Now for CB stage.

$$W_{pin} = \frac{1}{\left(R_S \parallel \frac{1}{g_m} \right) (C_{BS1} + C_{GS})}$$

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Ques: For given amplifier find pole frequency by inspection:



\rightarrow C_{BS1} & C_{BS2} are in parallel.

\rightarrow C_{DB1} , C_{DB2} , C_{BD2} , C_{BD1} are in parallel.

\rightarrow C_{BS1} & C_{BS2} off no use because they are in between AC ground and AC ground.

So there are two nodes basically where caps are present.

$$W_{pin} = \frac{1}{\left(R_S \parallel \frac{1}{g_m} \right) (C_{BS1} + C_{BS2})}$$

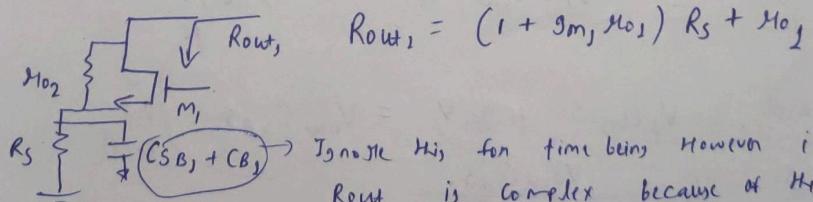
While seeing input impedance we made an approximation
Here that $M_0 = \infty$.

Now at output node: (i) $n=0$ then $M_0 \rightarrow \infty$ so

$$W_{pout} \rightarrow 0 \text{ (Not a practical case.)}$$

(ii) Here we have to consider C.C.M ($n \neq 0$)

$$R_{out1} = (1 + g_m M_0) R_S + M_0$$



Ignore this for time being. However in actual Rout is complex because of M_0 but for

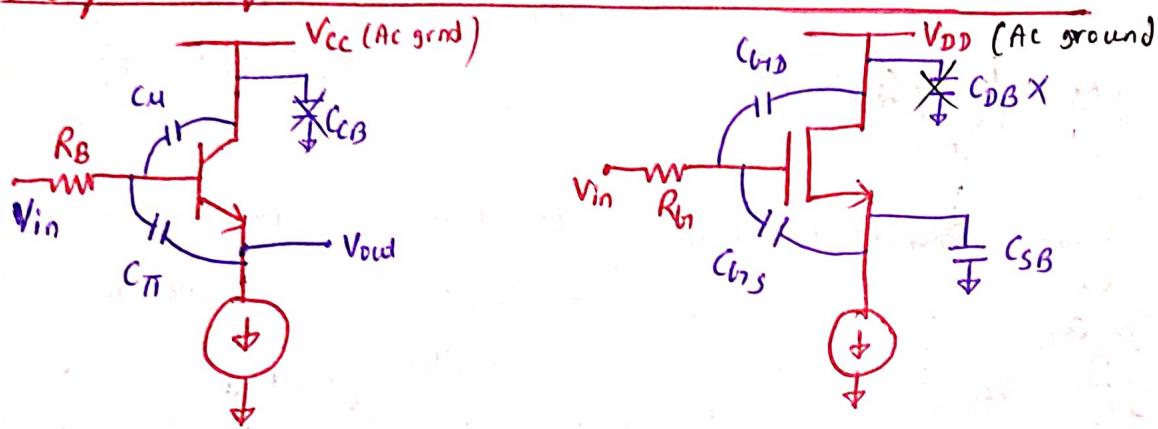
intuitive analysis, we can ignore it so

$$R_s = M_{o2} || (1 + g_m M_{o1}) R_s + M_{o1}$$

$$C = C_{DB1} + C_{DB2} + C_{GD2} + C_{GD1}$$

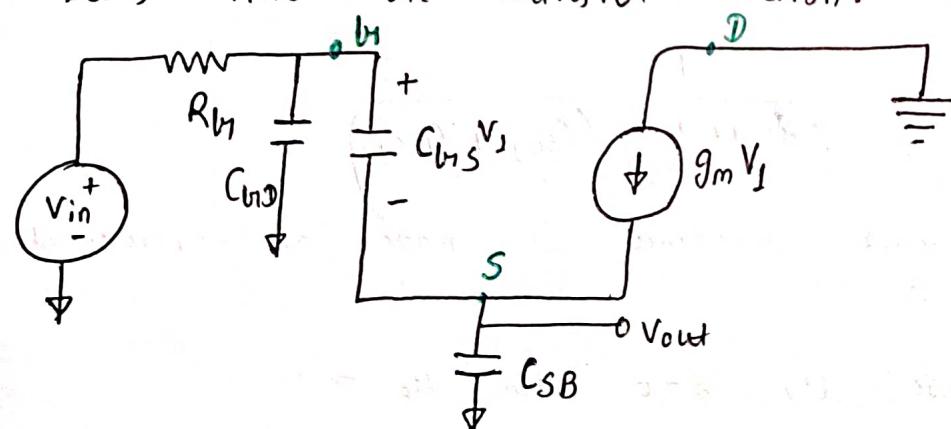
$$\text{So } \omega_{\text{poar}} = \frac{1}{R_s C}$$

3) Frequency Response of Followers :-



- Actually in BJT follower also there is a load capacitance at output terminal so Topology wise Both are same.
- Pole inspection method does not work here properly and dominant pole also because in reality both poles are very close to each other.

Let's find the Transfer function:



Apply KCL at gate:

$$\frac{V_{in} - (V_I + V_{out})}{R_D} = (V_I + V_{out}) C_{SD} s + V_I C_{SS} s$$

K.C.L at output: $V_I C_{SS} s + g_m V_I = V_{out} C_{SB} s$ put back

$$\text{So } V_I = \frac{V_{out} C_{SB} s}{s C_{SS} + g_m}$$

$$\Rightarrow \frac{V_{in}}{R_{in}} = (V_i + V_{out}) \left[\frac{1}{R_{in}} + sC_{BD} \right] + V_{out} \left[\frac{s^2 C_{BS} C_{SB}}{sC_{BS} + g_m} \right]$$

$$\Rightarrow \frac{V_{in}}{R_{in}} = V_{out} \left[\frac{1 + sR_{in}C_{BD}}{R_{in}} \right] + V_{out} \left(\frac{1 + sR_{in}C_{BD}}{R_{in}} \right) \left(\frac{sC_{SB}}{sC_{BS} + g_m} \right)$$

$$+ V_{out} \left[\frac{s^2 C_{BS} C_{SB}}{sC_{BS} + g_m} \right]$$

$$\Rightarrow \frac{V_{in}}{R_{in}} = V_{out} \left[\frac{(1 + sR_{in}C_{BD})(sC_{BS} + g_m) + (1 + sR_{in}C_{BD})(sC_{SB}) + s^2 C_{BS} C_{SB} R_{in}}{R_{in}(sC_{BS} + g_m)} \right]$$

$$\Rightarrow \frac{V_{in}}{V_{out}} = \frac{s^2 (R_{in}C_{BS}C_{BD} + R_{in}C_{BS}C_{SB} + R_{in}C_{BD}C_{SB}) + sC_{BS} + g_m R_{in}C_{BD} + C_{SB}}{sC_{BS} + g_m}$$

So Transfer function $H(s) = \frac{V_{out}(s)}{V_{in}(s)}$

$$H(s) = \frac{1 + sC_{BS}/g_m}{(C_{BS}C_{BD} + C_{BS}C_{SB} + C_{BD}C_{SB}) \frac{R_{in}}{g_m} s^2 + \left(\frac{C_{BS}}{g_m} + R_{in}C_{BD} + \frac{C_{SB}}{g_m} \right) + 1}$$

→ This is Transfer function of source follower.

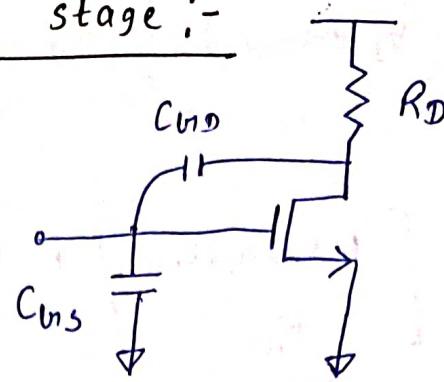
→ Just change capacitance property & put C_L in place of C_{SB} it will converted to BJT source follower Transfer function.

Input Capacitance of CS stage :-

Apply Miller effect at C_{GD} .

$\therefore \text{so}$

$$C_{in} \approx C_{BS} + (1 + g_m R_D) C_{GD}$$



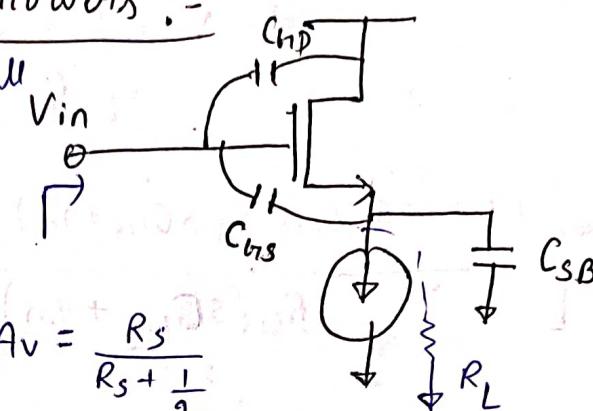
Input Capacitance of Followers :-

Here Miller effect will be applied on C_{BS} .

For that we have to assume a load resistance (R_L)

\therefore

$$C_{in} = C_{BS} + C_{BS}(1 - A_v)$$

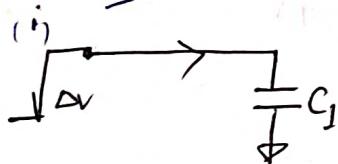


$$C_{in} = C_{BS} + \frac{C_{BS}}{1 + g_m R_L} + \left| A_v = \frac{R_s}{R_s + \frac{1}{g_m}} \right|$$

Here in place of R_s , R_L is there.

$$A_v = \frac{R_L}{R_L + \frac{1}{g_m}} = \frac{g_m R_L}{1 + R_L g_m}$$

Intuitively explain why the input Miller capacitance of source follower is less than $C_{BS} + C_{GD}$:



$$Q = C_1 \Delta V$$

(ii)



IF node - 1 voltage goes up by ΔV then node - 2 also go up by ΔV so voltage change across capacitor = 0
 $\therefore Q = 0$

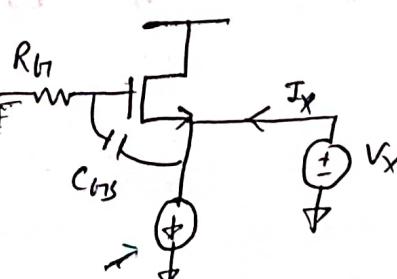
Hence C is actually Boot-strapped because it is not able to store charge.

In source follower $A_v \approx 0.8$ to 0.9

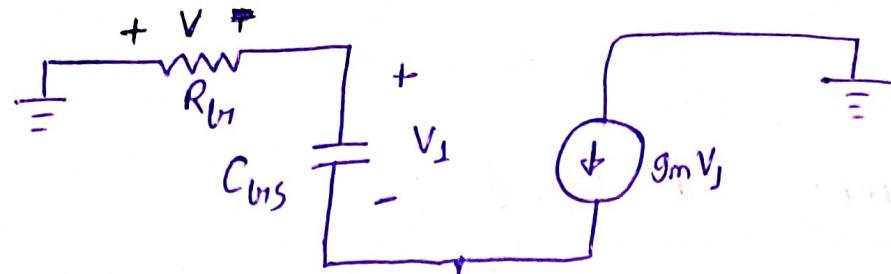
$\therefore C_{BS}(1 - A_v) \approx 0.2 C_{BS}$, That's why C_{BS} appear reduced at Input.

Output Impedance of Followers :-

For o/p Impedance calculation all V sources shorted & Current source open.



so small circuit circuit for o/p Impedance calculation is:



(we are seeing effect of only C_{BNS} here, other caps ignored)

K.C.L at source-node

is :

$$V_1 s C_{BNS} + g_m V_J + I_x = 0 \quad \text{so} \quad V_1 = \frac{-I_x}{s C_{BNS} + g_m}$$

Applying K.V.L from V_x to ground through R_{Bn} .

$$V_x + V_1 + V = 0$$

$$\Rightarrow V_x + V_1 + (V_1 s R_{Bn} C_{BNS}) = 0$$

$$\Rightarrow V_x + V_1 (1 + s R_{Bn} C_{BNS}) = 0$$

$$\Rightarrow V_x - \frac{I_x (1 + s R_{Bn} C_{BNS})}{g_m + s C_{BNS}} = 0$$

$$\Rightarrow Z_{out} = \frac{V_x}{I_x} = \frac{1 + s R_{Bn} C_{BNS}}{g_m + s C_{BNS}}$$

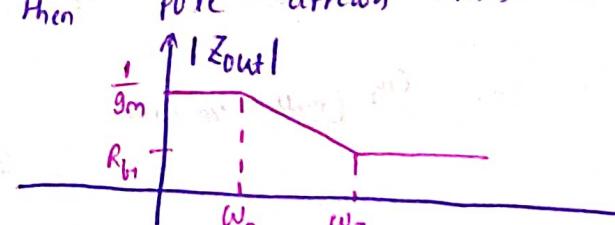
There is something special about this Z_{out} .

$$\text{Zero of } Z_{out}, \omega_Z = \frac{-1}{R_{Bn} C_{BNS}}$$

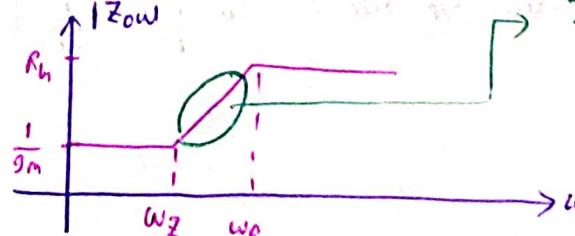
$$\omega_p = -g_m / C_{BNS}$$

Now let's plot $|Z_{out}|$:

Case-1 $g_m < \frac{1}{R_{Bn}}$ Then pole appears first in ω plane:



Case-2 $g_m > \frac{1}{R_{Bn}}$



In this region, Impedance increase with frequency increase, which is a inductive behaviour. So we can build "Active Inductor".

→ Basically we use followers to drive small o/p load, because it offers low o/p Impedance. So It acts a Buffer mostly.

4) Frequency Response of Cascodes :-

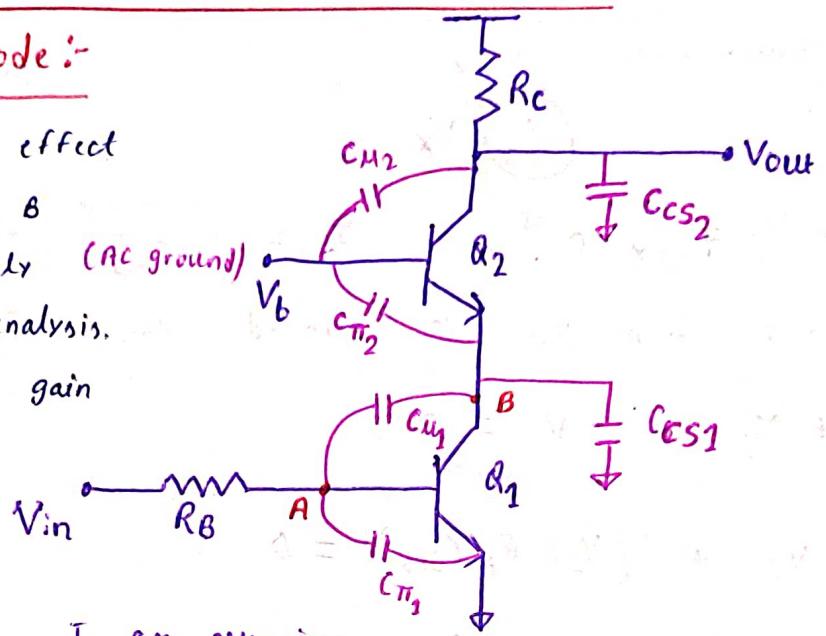
(1) Bi-Polar Cascode:-

There is a Miller effect

at C_{M1} between A & B

so we need to apply (AC ground) approximate mission analysis.

For that we want gain from A to B.



→ To find $\frac{V_B}{V_A}$, I am assuming early voltage, $= \infty$.

So $\frac{V_B}{V_A} = -g_{m1}$ (Resistance tied base collector of Q_1 to AC ground) → see ~~input~~ Resistance from collection of Q_1 on Emitter of Q_2 .

$$\frac{V_B}{V_A} = -g_{m1} \left(\frac{1}{g_{m2}} \parallel M_{O2} \right)$$

Assumed ∞

$$\frac{V_B}{V_A} = \frac{-g_{m1}}{g_{m2}}$$

Since $g_{m1} = \frac{I_{C1}}{V_T}$

$$g_{m2} = \frac{I_{C2}}{V_T}$$

There is ∞ o/p resistance means

early voltage effect eliminated, so $I_{C1} \approx I_{C2}$

$$\frac{V_B}{V_A} = -1$$

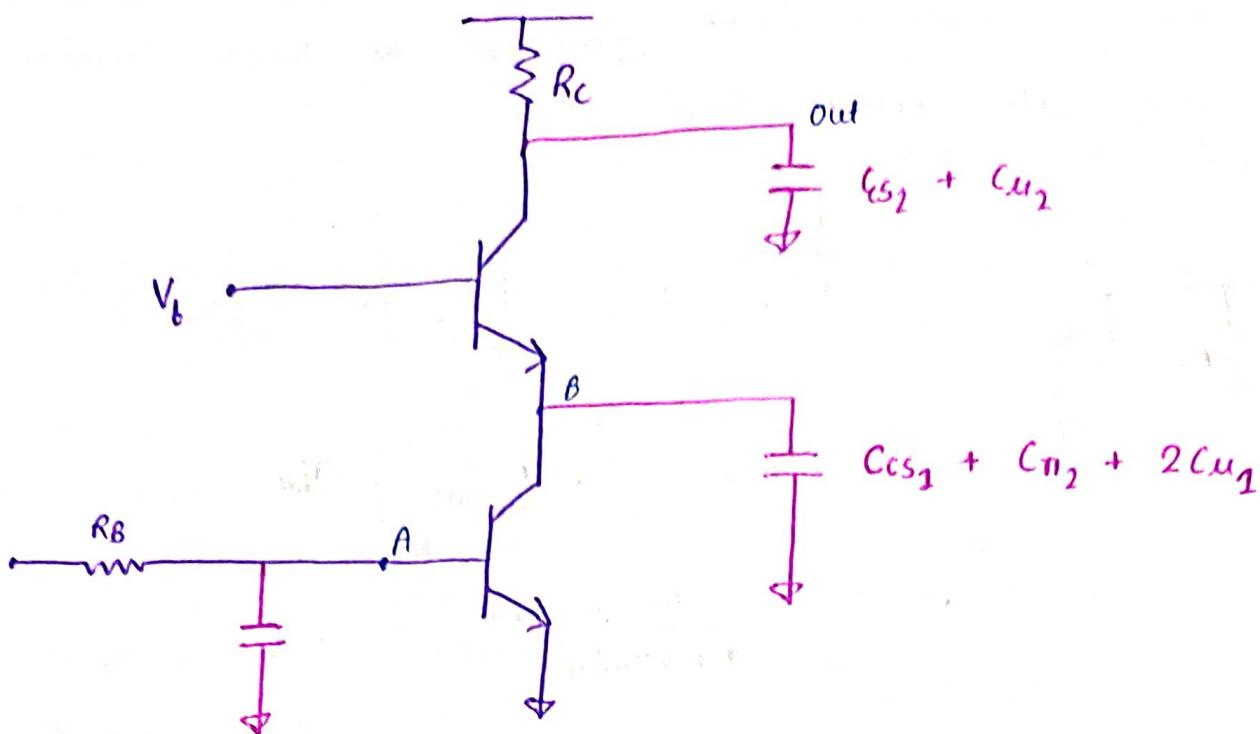
$$\text{So } C_{M1} (\text{Miller o/p side}) = C_{M1} (1 - (-1)) \\ = 2C_{M1}$$

$$C_{M2} \text{ o/p side} = C_{M1} \left[1 - \frac{1}{-1} \right]$$

→ V_b is ac ground so C_{M1} & C_{CS2} are parallel

$\times C_{\pi_2}$ & C_S1 are in parallel.

Hence simplified Cascode structure is:



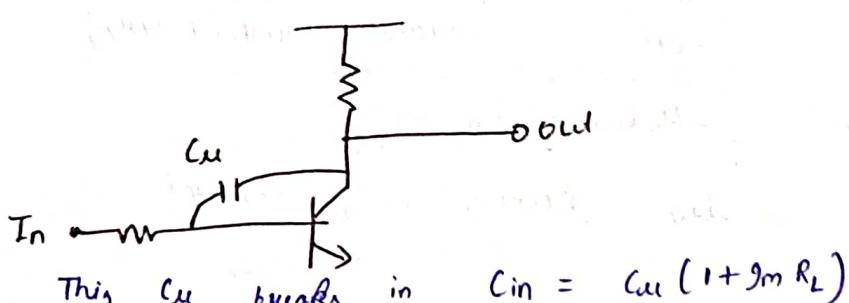
$C_{\pi_1} + 2C_{u_1}$ Now apply pole inspection method to find pole frequencies.

$$\omega_{PA} = \frac{1}{(R_B \parallel H_\pi)(C_{\pi_1} + 2C_{u_1})} ; \quad \omega_{out} = \frac{1}{R_C(C_{u_2} + C_{\pi_2})}$$

$$\omega_{PB} = \frac{1}{\frac{1}{g_m_2}(C_{s1} + C_{\pi_2} + 2C_{u_1})} \leftarrow \text{Typically very High so its of no use for us.}$$

→ In most of the cases output becomes linear for Bandwidth.

Compare this cascode with CE Amplifier



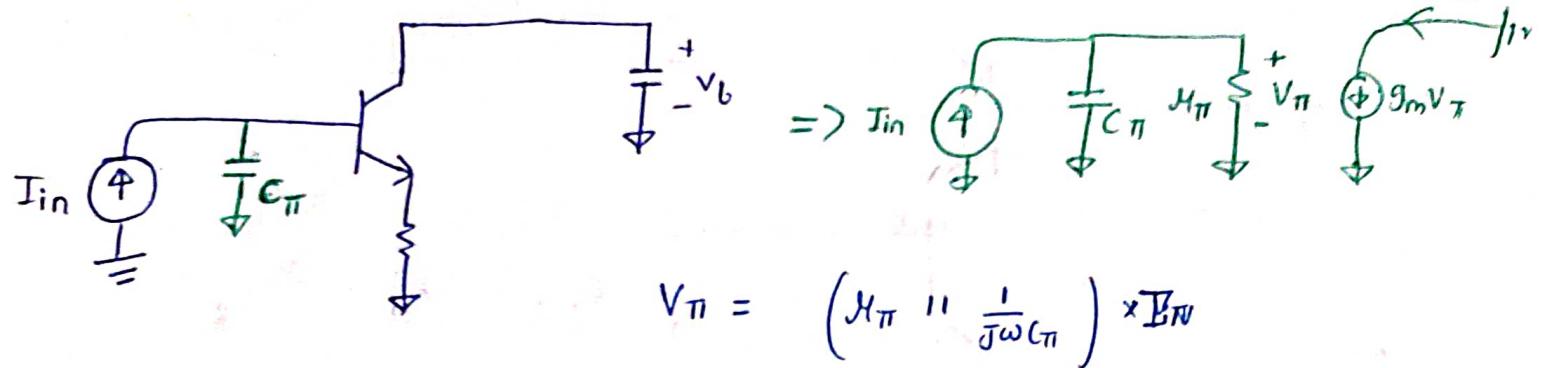
$$\text{This } C_u \text{ breaks in } C_{in} = C_u (1 + g_m R_L)$$

$$C_{in} \approx 10 C_u$$

In Cascode stage we are getting even more gain and less Miller multiplication at I/p side.

* The transit frequency f_T :- Frequency at which current gain of the device drops to 1.

Let us see its effect in CE stage.
Biasing is not shown:



$$I_{out} \Rightarrow g_m V_{pi} = \frac{H_{pi} g_m I_{in}}{1 + s H_{pi} C_{pi}}$$

$$\Rightarrow \frac{I_{out}}{I_{in}} = \frac{H_{pi} g_m}{1 + s H_{pi} C_{pi}} \quad \text{for Transit frequency magnitude of this at } \omega_T = 1$$

$$\left| \frac{I_{out}}{I_{in}} \right| = \frac{g_m H_{pi}}{\sqrt{1^2 + \omega_T^2 H_{pi}^2 C_{pi}^2}} = 1 \quad \text{for } \omega = \omega_T$$

$\therefore \beta = \frac{g_m H_{pi}}{dc}$

$$\therefore 1 + \omega_T^2 H_{pi}^2 C_{pi}^2 = \beta^2 \quad \beta_{dc} \gg 1$$

$$\therefore \omega_T = \frac{\beta}{H_{pi} C_{pi}} = \frac{g_m}{C_{pi}}$$

For MOSFET: $\omega_T = \frac{g_m}{C_{vds}}$ (It is generally several hundred MHz)

Since we know $g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D}$

a) What happens if $\frac{W}{L}$ doubled keeping I_D constant

g_m goes to $\sqrt{2} g_m$

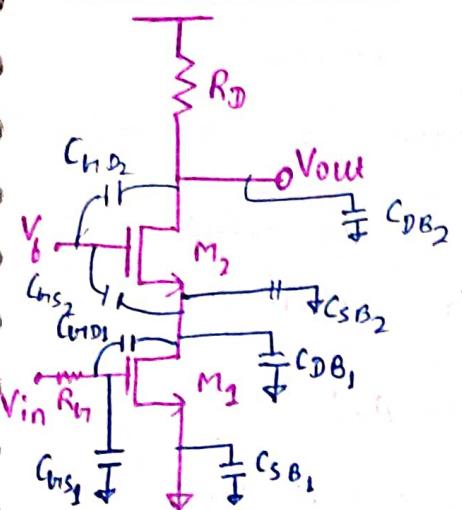
Since C_{vds} scale in proportion with W so $C_{vds} \rightarrow 2C_{vds}$

Hence Transit frequency $\omega_T \rightarrow \frac{\omega_T}{\sqrt{2}}$

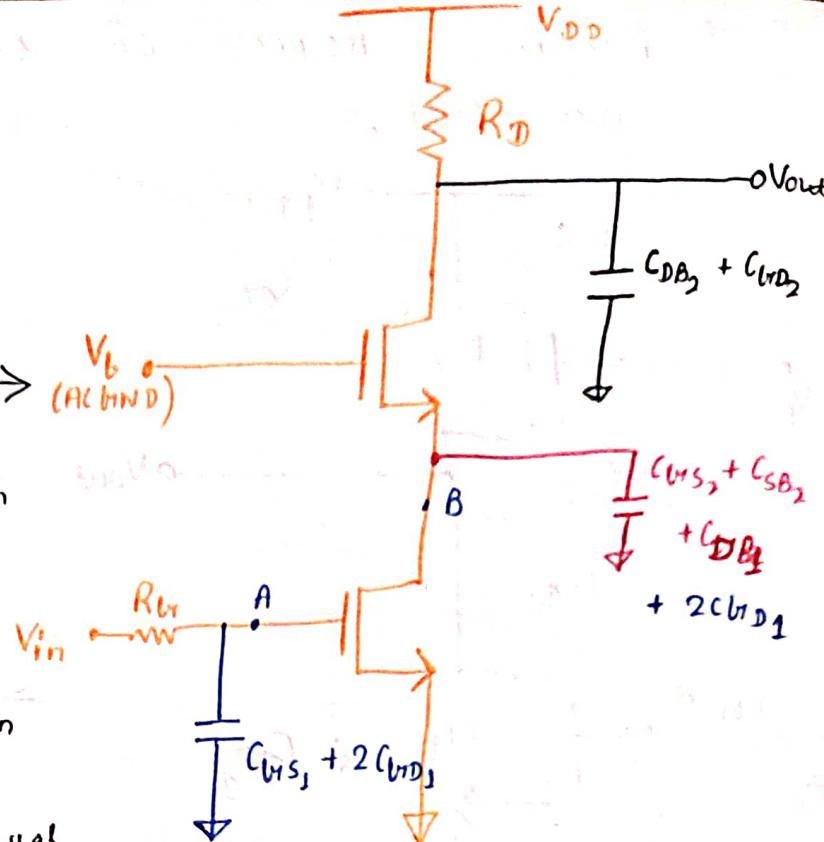
b) $\frac{W}{L}$ & I_D both doubled: $g_m \rightarrow g_m \sqrt{2} \times \sqrt{2} = 2g_m$
 $C_{vds} \rightarrow 2C_{vds}$

ω_T unaffected.

2. MOS Cascode:-



V_b acts as
A.C. BIASING
so Merging
Capacitance which
can be merged
and minimizing
useless one's.



C_{D1} experiences Miller multiplication
so we need to obtain gain from
A to B which is approximately equal
to (Nested Channel-length model.)

$$A_{AB} = -g_{m1} \times \frac{1}{g_{m2}} \\ = \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \cdot \frac{I_{D1}}{I_{D2}}}$$

We make Transistor of same sizes. And no ccm is there so
 $I_{D1} = I_{D2}$
Hence $A_{AB} = -1$

Now just use pole by inspection at nodes A, B & Vout.

$$\omega_{p1|A} = \frac{1}{R_b (C_{bs1} + 2C_{bd1})}$$

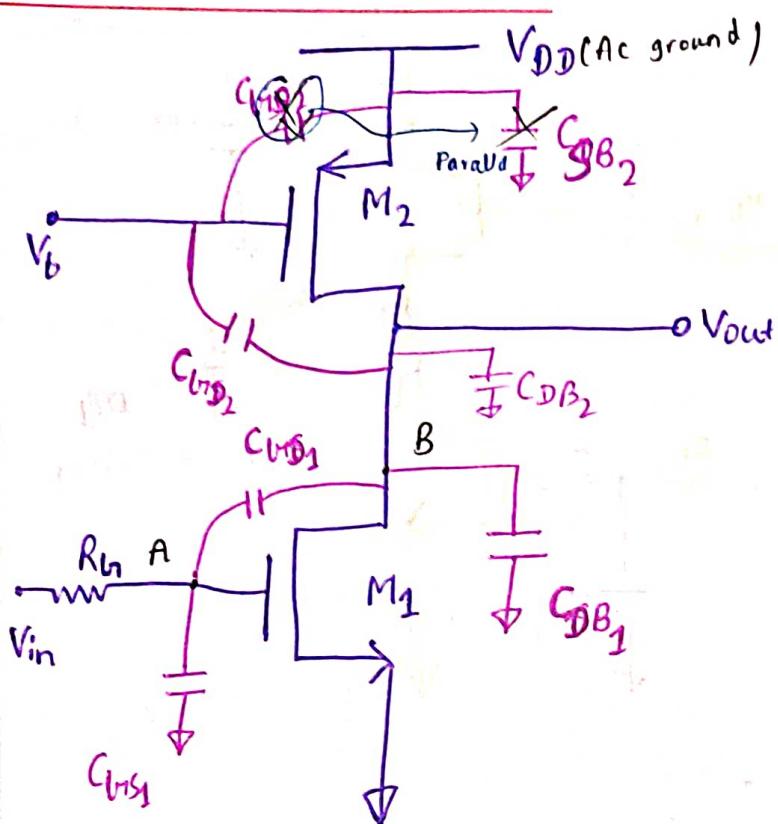
$$\omega_{p1|B} = \frac{1}{\frac{1}{g_{m2}} (C_{DB1} + C_{BS2} + C_{SB2} + 2C_{BD1})}$$

Resistance seen at terminal B (Note: M_{01}, M_{02} assumed to ∞ , otherwise they also comes in picture).

$$\omega_{pout} = \frac{1}{R_D (C_{BD2} + C_{DB2})}$$

In most cases $R_D \gg R_b \approx \frac{1}{g_{m2}}$ & C_{BD2}, C_{DB2} have a higher DC potential difference plus load is also there at out terminal so ω_{pout} is dominant frequency (i.e. Bandwidth deciding).

(5) Frequency Response of CS stage with Current Source, Load :-



C_{DB_2} is in parallel with C_{DB_1} because b is Acground

Now Apply Miller effect for C_{GD_1} so it increases in $C_{GD_1}(1 - A_v)$ in F/p side & $C_{GD_2}(1 - \frac{1}{A_v})$ at o/p side.

Since now its loaded with PMOS source, so we have to consider channel length modulation
Hence $A_v = -g_m(1/\mu_0_1 || 1/\mu_0_2)$

So Total capacitance at node-A

$$C_A = C_{BS_1} + C_{UD_1} \left(1 + g_m(1/\mu_0_1 || 1/\mu_0_2) \right)$$

$$R_A = R_b || \omega = R_b$$

$$\text{So } \omega_A = \frac{1}{R_A C_A} \quad \{ \text{By Inspection} \}$$

Total Capacitance at node-B:

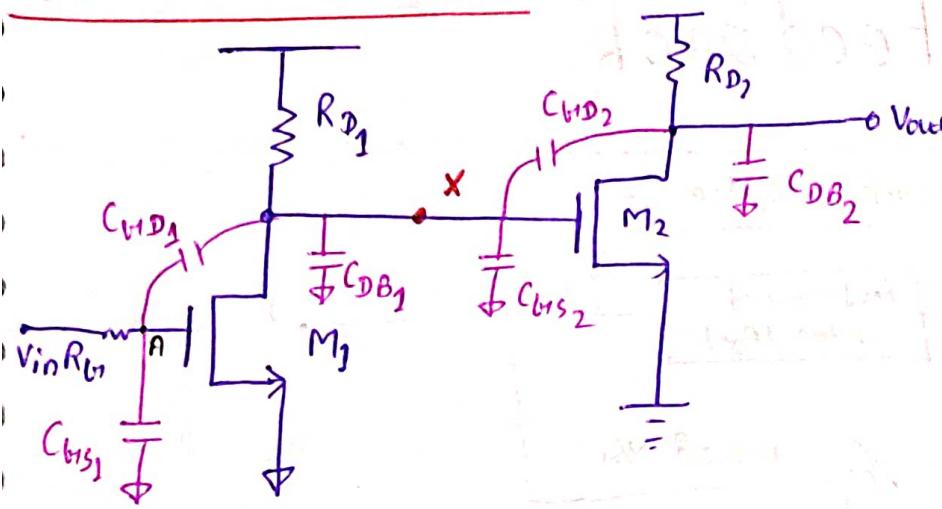
$$C_B = C_{DB_1} + C_{UD_2} + C_{UD_1} \left(1 + \frac{1}{g_m(1/\mu_0_1 || 1/\mu_0_2)} \right) + C_{DB_2}$$

R_B = Resistance looking into B

$$= (1/\mu_0_1 || 1/\mu_0_2) \text{ look at drain of PMOS.}$$

look at Drain of NMOS

(6) Cascaded Stages:



A). Gain from node-A to V_{out} is: $g_{m_1} R_{D_1}$

(Approximate, because there must be same load associated in actual.)

$\therefore C_{BD_1}$ experiences Miller effect.

However M_2 offers $1/g_{m_2} R_{D_2}$ at sat.

Breaks in $C_{BD_1} (1 + g_{m_1} R_{D_1})$ at Input side

and $C_{BD_1} (1 + g_{m_1} R_{D_1})$ at Node X.

$$\therefore W_{PA} = \frac{1}{R_{B_1} (C_{B1S_1} + C_{BD_1} (1 + g_{m_1} R_{D_1}))}$$

And

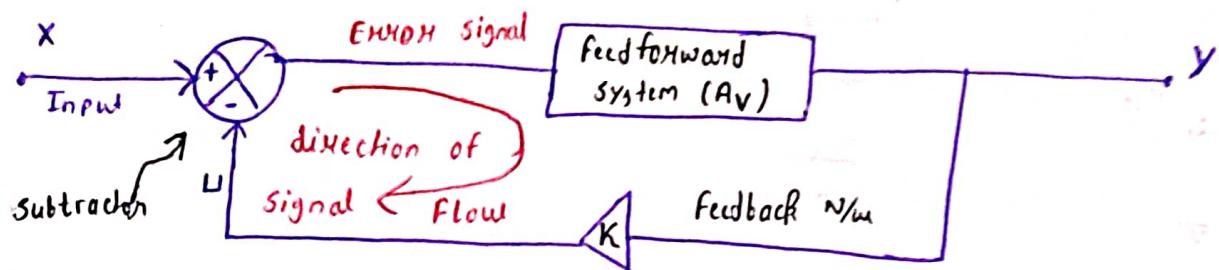
$$W_{PX} = \frac{1}{R_{D_1} || \left[C_{DB_1} + C_{B1S_2} + C_{BD_1} \left(1 + \frac{1}{g_{m_1} R_{D_1}} \right) + C_{BD_2} \left(1 + g_{m_2} R_{D_2} \right) \right]}$$

And

$$W_{Pout} = \frac{1}{R_{D_2} \left[C_{DB_2} + C_{BD_2} \left(1 + \frac{1}{g_{m_2} R_{D_2}} \right) \right]}$$

Unit 4: Feedback

Biennial Negative Feedback System :-



Transfer function of closed loop system:

$$\frac{Y}{X} = \frac{Av}{1 + KAv} \quad Av : \text{open loop gain}$$

K : feedback gain

Error signal is: $E = X - U$

$$E = X - KY$$

$$E = X - K \left[\frac{Av}{1 + KAv} \right]$$

$$E = \frac{X}{1 + KAv}$$

so for Error to minimized:

$$X \approx U$$

{ feedback signal should be a good copy of Input signal for error to be minimized }

Loop gain :- This term KAv is our loop gain.

when $KAv \gg 1$, closed loop gain $\approx \frac{1}{K}$

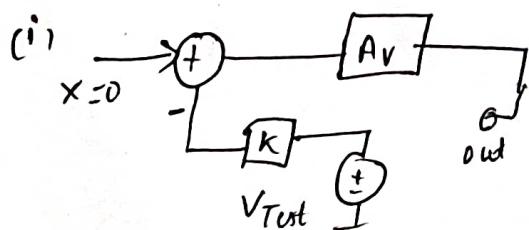
Independent of Av , which makes system more stable with respect to variations in K .

Loop gain calculations :-

Break the loop anywhere &

Set $X=0$ and measure gain

by applying test input, that is our loop gain:

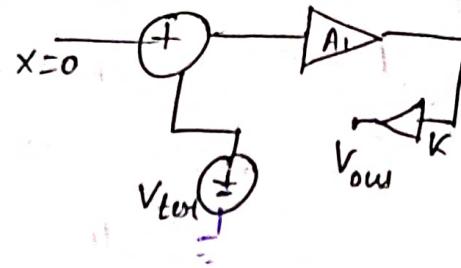


$$-V_{test} \times KAv = V_{out}$$

$$\Rightarrow \frac{-V_{test}}{V_{out}} \geq KAv$$

$$-\frac{V_{out}}{V_{in}} = KA_V$$

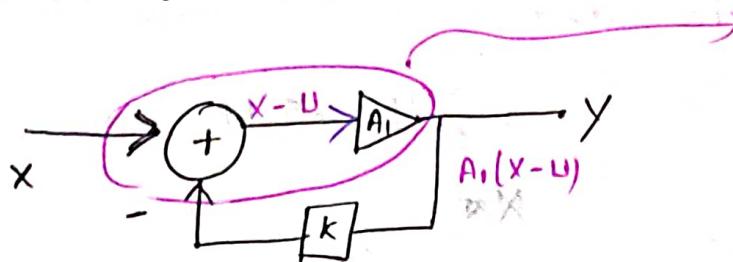
If we break loop at $X=0$ at different place then also



Here also

$$-\frac{V_{out}}{V_{in}} = KA_V = \text{loop gain.}$$

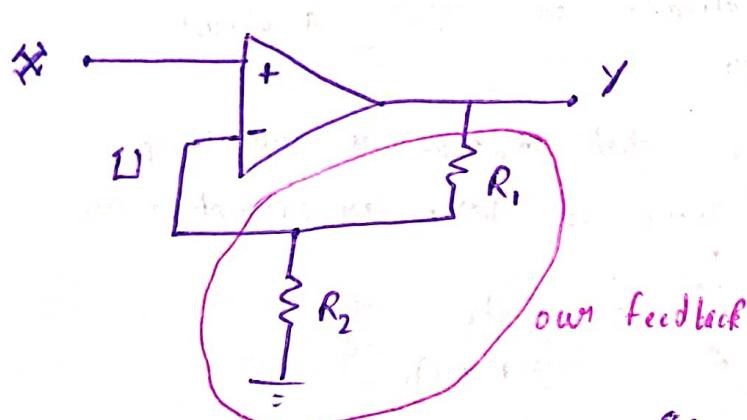
Example of feedback circuit:



We can use an op-amp to develop this part of circuit:

$$V_1 - V_2 \rightarrow A_V \rightarrow (V_1 - V_2) \times A$$

So taking a Non-Inverting Op-Amp section



U = divided by $R_1 \& R_2$ path

$$U = \frac{R_2}{R_1 + R_2} Y \rightarrow \text{our } K \text{ (feedback factor)}$$

$$\text{So, } \frac{Y}{X} = \frac{A_1}{1 + KA_1}$$

$$\text{closed loop gain} = \frac{A_1}{1 + \frac{R_2}{R_1 + R_2} A_1}$$

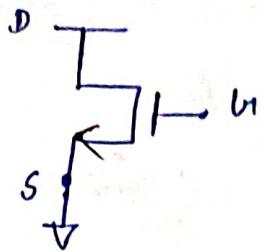
So if loop gain $\frac{R_2}{R_1 + R_2} A_1 \gg 1$

$$\text{then closed loop gain} = \frac{1}{K} = \frac{1}{\frac{R_2}{R_1 + R_2}}$$

$$= 1 + \frac{R_2}{R_1}$$

We can say This R_2/R_1 is stable in even Temperature variation because R_2, R_1 changes by same factor with T variation.

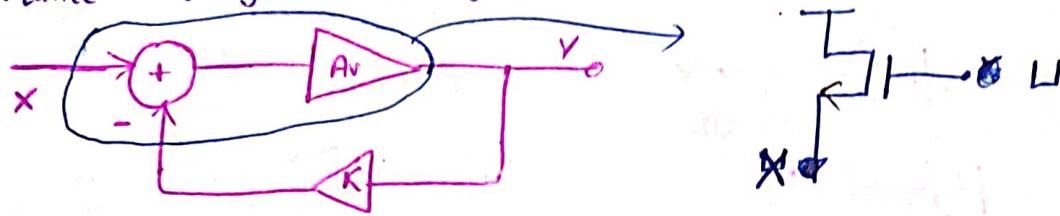
Making use of feedback using a single Transistor :-



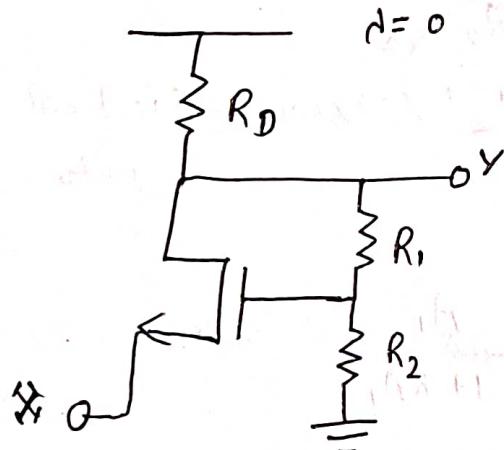
We know that for small signal operation

$$I_D = g_m V_{BIS}$$

So If apply V_I at gate & Input at X Then it will generate some part of our negative feedback. Then we will pass this I_D through any resistance & get voltage in output.



Just add a voltage divider at U & get Negative feedback system. However this would have obvious problems in practical use. But Theoretically we made a cheap Negative feedback Amplifier



$$\beta = 0$$

→ Given that $R_1 + R_2$ is very large.

→ So There is very less current there.

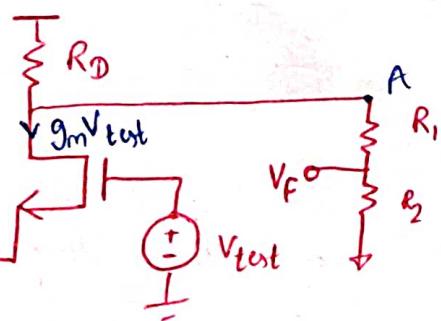
$$\frac{Y}{X} = \frac{A_1}{1 + KA_1}$$

$$A_1 = g_m R_D$$

$$\text{So } \frac{U}{Y} = K = \frac{R_2}{R_1 + R_2}$$

$$\text{So } \frac{Y}{X} = \frac{g_m R_D}{1 + \left(\frac{R_2}{R_1 + R_2} g_m R_D \right)}$$

We know this is our loop gain. Finding it using another way:



$$V_F = \left(-g_m V_{tst} R_D \right) \times \frac{R_2}{R_1 + R_2}$$

$$\frac{-V_F}{V_{tst}} = \frac{g_m R_D R_2}{R_1 + R_2} = \text{Loop gain}$$

Properties of Negative feedback :-

$$\frac{Y}{X} = \frac{A_1}{1 + KA_1} \approx \frac{1}{K} \quad \text{for } KA_1 \gg 1$$

→ Brain Desensitization: $\frac{Y}{X}$ is less sensitive to temp, supply than A_1 .

- Bandwidth Extension: greater Bandwidth for closed loop system.
- Modification of Input & Output Impedances.
- Higher linearity.

Let us take a first order system:

$$A_1 = \frac{A_0}{1 + \frac{s}{\omega_p}} \xrightarrow{\text{Brain at 0 freq}}$$

Bandwidth is determined using this pole frequency

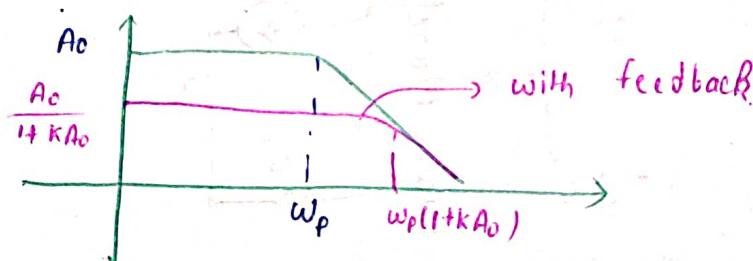
For closed loop system:

$$A_{\text{close}} = \frac{A_0}{1 + \frac{s}{\omega_p}} = \frac{A_0}{1 + \frac{s}{\omega_p} + A_0 K}$$

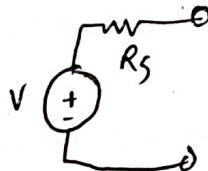
$$= \frac{A_0}{1 + \frac{s}{\omega_p(1 + KA_0)}}$$

Here feedback means

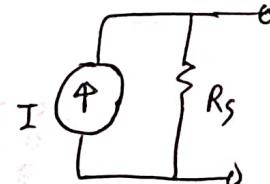
Negative feedback until and unless the feedback not said.



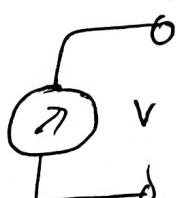
Some Basics



Ideal voltage source wants to have zero resistance $R_S = 0$



Ideal current source have $R_S = \infty$ so that all the current is available to load



Ideal voltmeter needs to be connected in parallel to points where we need to measure voltage so it should not load circuit. Hence $R_{volt} = \infty$



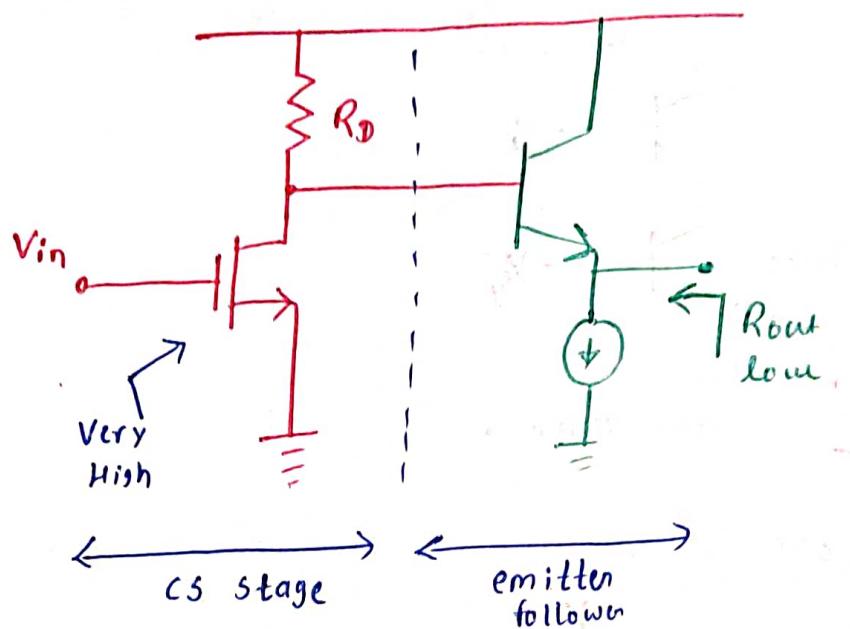
It will connect in series where we want current measurement so Ammeter Ideal internal Resistance = 0

Model of four Amplifier Topologies

Voltage Amplifier	Trans - Conductance Amplifier	Trans Impedance Amplifier	Current Amplifier
$V_{in} \rightarrow \Delta A \rightarrow V_{out}$	$V_{in} \xrightarrow{+} \frac{V_{in}}{I_{in}} \xrightarrow{-} I_{out}$ Ideal model: $\frac{V_{in}}{I_{in}} = \frac{A_{in} V_{in}}{I_{in}}$	$V_{in} \xrightarrow{+} \frac{V_{in}}{R_{in}} \xrightarrow{-} I_{out}$ Ideal model: $\frac{V_{in}}{R_{in}} = \frac{A_{in} V_{in}}{R_{in}}$	$I_{in} \rightarrow \Delta A \rightarrow I_{out}$ Ideal model: $A_{in} I_{in} = I_{out}$
$V_{in} \rightarrow \Delta A \rightarrow V_{out}$	$V_{in} \xrightarrow{+} \frac{V_{in}}{I_{in}} \xrightarrow{-} R_o I_{in}$ Ideal model: $\frac{V_{in}}{I_{in}} = \frac{A_{in} V_{in}}{I_{in}}$	$V_{in} \xrightarrow{+} \frac{V_{in}}{R_{in}} \xrightarrow{-} R_o I_{in}$ Ideal model: $\frac{V_{in}}{R_{in}} = \frac{A_{in} V_{in}}{R_{in}}$	$I_{in} \rightarrow R_{in} \rightarrow R_{out} \rightarrow I_{out}$ Actual model: $R_{in} I_{in} + R_{out} I_{out} = 0$
$V_{in} \rightarrow \Delta A \rightarrow V_{out}$	$V_{in} \xrightarrow{+} \frac{V_{in}}{I_{in}} \xrightarrow{-} R_o V_{in}$ Ideal model: $\frac{V_{in}}{I_{in}} = \frac{A_{in} V_{in}}{I_{in}}$	$V_{in} \xrightarrow{+} \frac{V_{in}}{R_{in}} \xrightarrow{-} R_o V_{in}$ Ideal model: $\frac{V_{in}}{R_{in}} = \frac{A_{in} V_{in}}{R_{in}}$	$V_{in} \xrightarrow{+} \frac{V_{in}}{R_{in}} \xrightarrow{-} R_o V_{in}$ Actual Model: $R_{in} V_{in} + R_{out} V_{in} = 0$

Examples of Amplifier Implementations :-

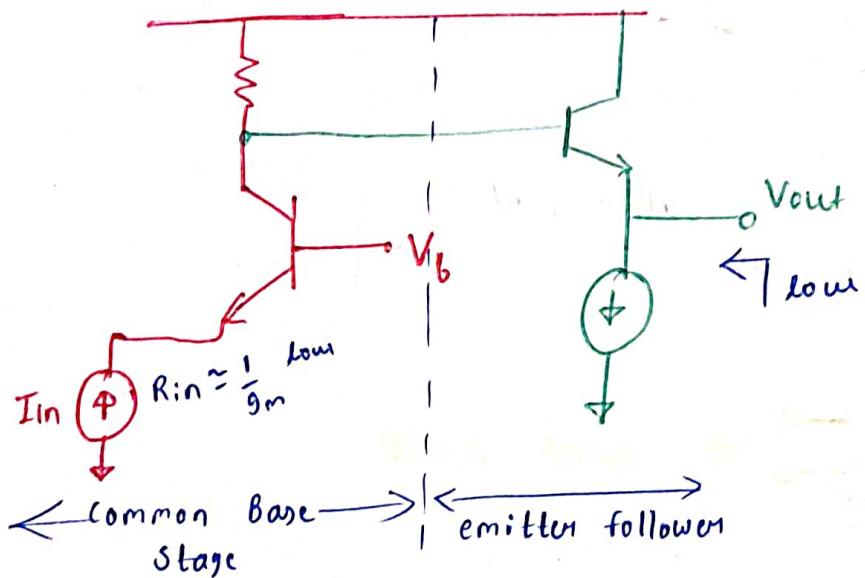
1) Voltage Amplifier :- we want a circuit such that it does not load previous stage. Mean from previous stage it picks voltage as it is without loading that so we need Input Resistance very high and output resistance very low so that all the Amplified voltage is available to load.



Used emitter follower
to make O/P Resistance
low.

2) Trans-Impedance Amplifier :-

Input = Current, want R_{in} ≈ 0
O/P = Voltage, so want R_{out} ≈ 0

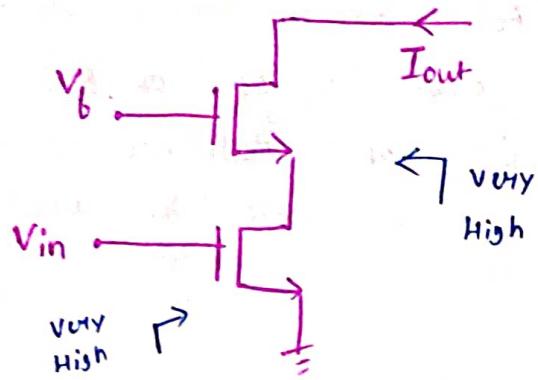


3) Trans-Conductance Amplifier :

Input : Voltage

Output : Current

We want both Input and output resistance very High.

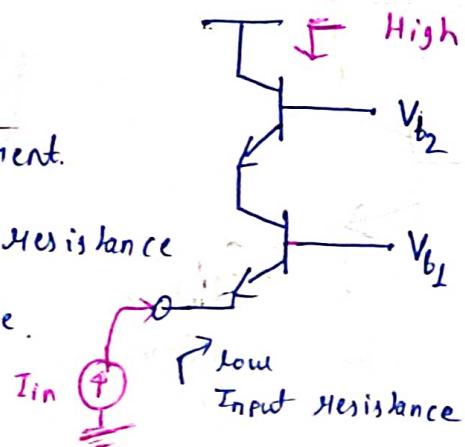


We used a Cascaded stage.

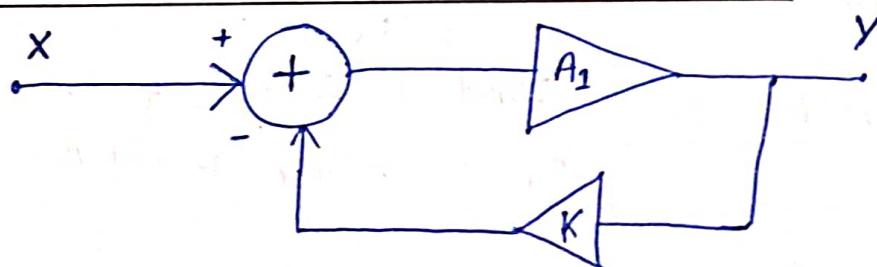
4) Current Amplifier :-

Input & Output : Both Current.

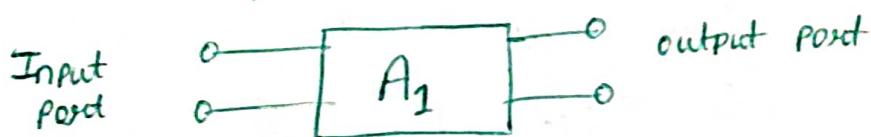
→ We want low I_{in} resistance and High output resistance.



Alternative Feedback model :-



Where Actually :

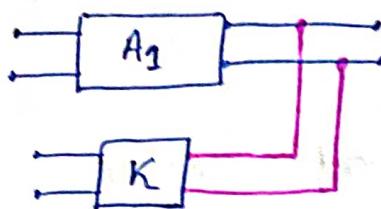


But how should we connect them, for different types of amplifiers.

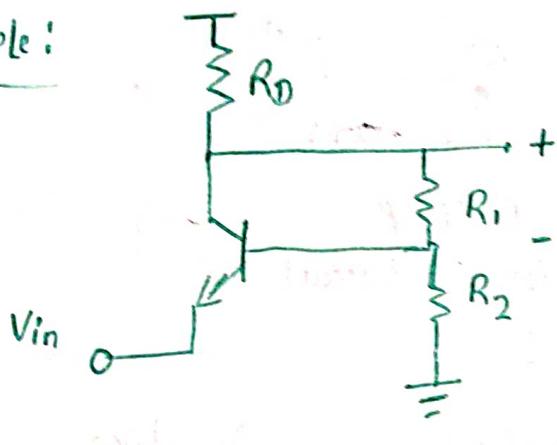
Sense Mechanisms :-

Voltage

→ To return voltage we need to place feedback network's I/P side in parallel with A_1 's output side.

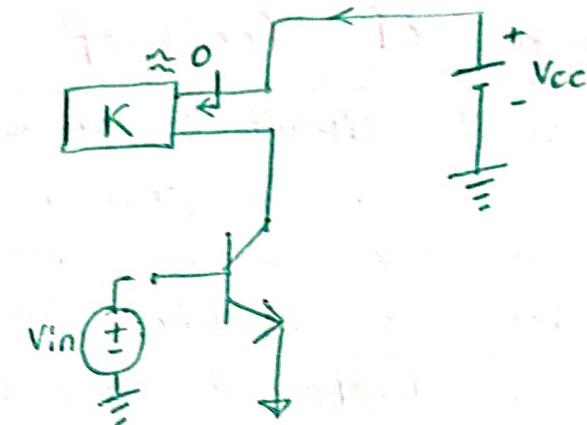
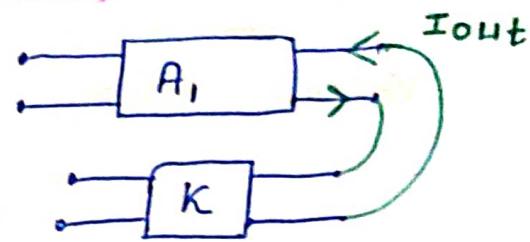


Example:



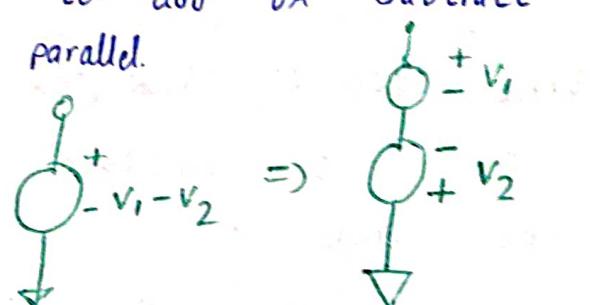
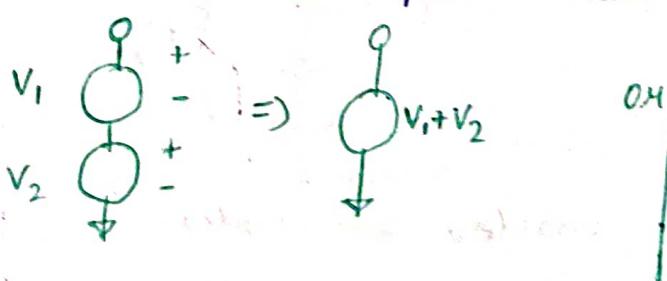
Current

→ To return current we need to place feedback network in series with output side of A_1 .

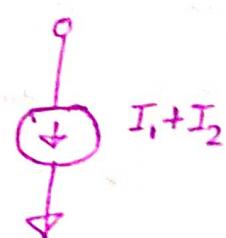
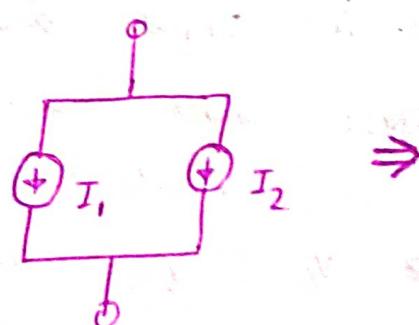


Using voltmeter also we can sense I:
 \rightarrow we measure IR
 \rightarrow we know IR, R
 \therefore we know I

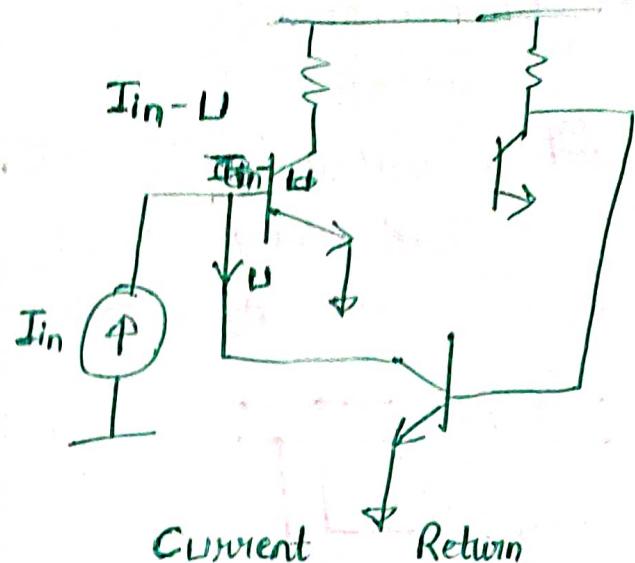
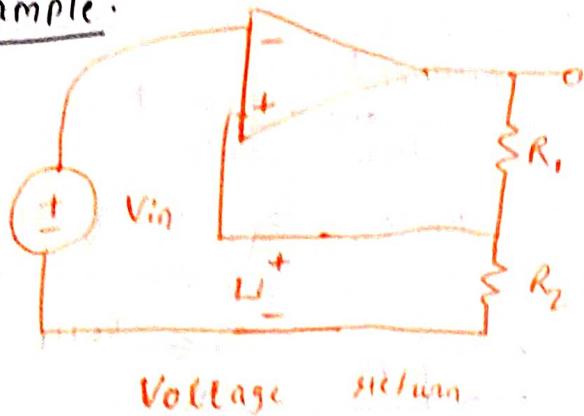
Return Mechanisms :- At return we need to subtract quantity. To subtract voltages we need to place them in series while to add or subtract currents we need to place them in parallel.



For Current:



Example:



Sign of feedback :-

In small circuit : If we get $A_1 K$ positive

then we say yes its negative feedback.

But how to identify this in large circuits ?

Break feedback at any point :

If $\frac{V_F}{V_{Test}} < 0 \Rightarrow$ feedback is negative.

Example - 1

Breaking feedback

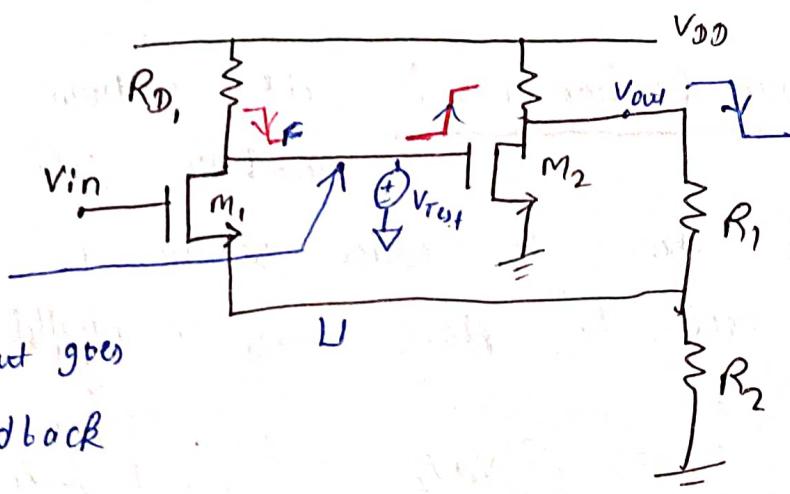
Loop Here:

→ When V_{test} goes up V_{out} goes down and so feedback also goes down.

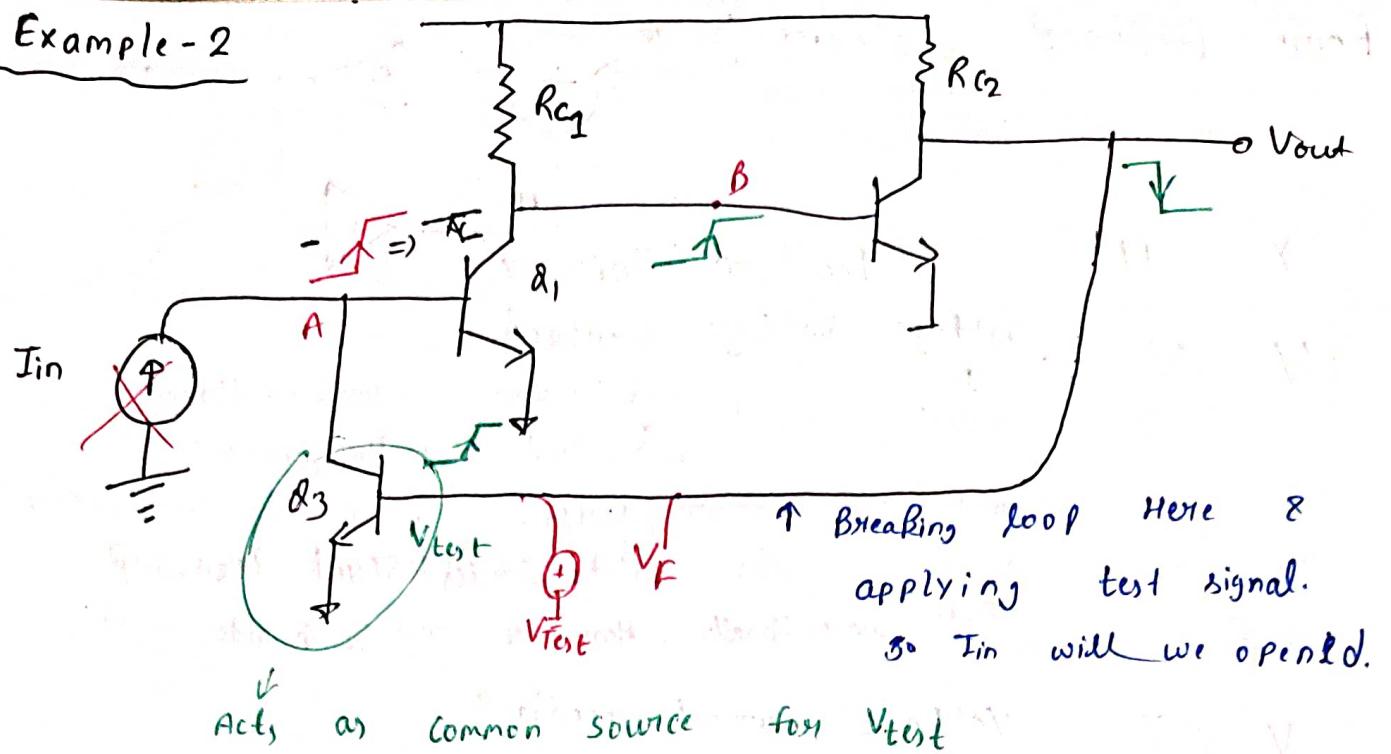
→ While doing this test V_{in} is disabled or shorted.

so now for M_1 , U is Input and it is something common gate stage which have positive gain & whose o/p is F so F also goes down.

so $V_{test} \downarrow \rightarrow F \downarrow \rightarrow V_F \downarrow$ It is negative feedback.



Example - 2

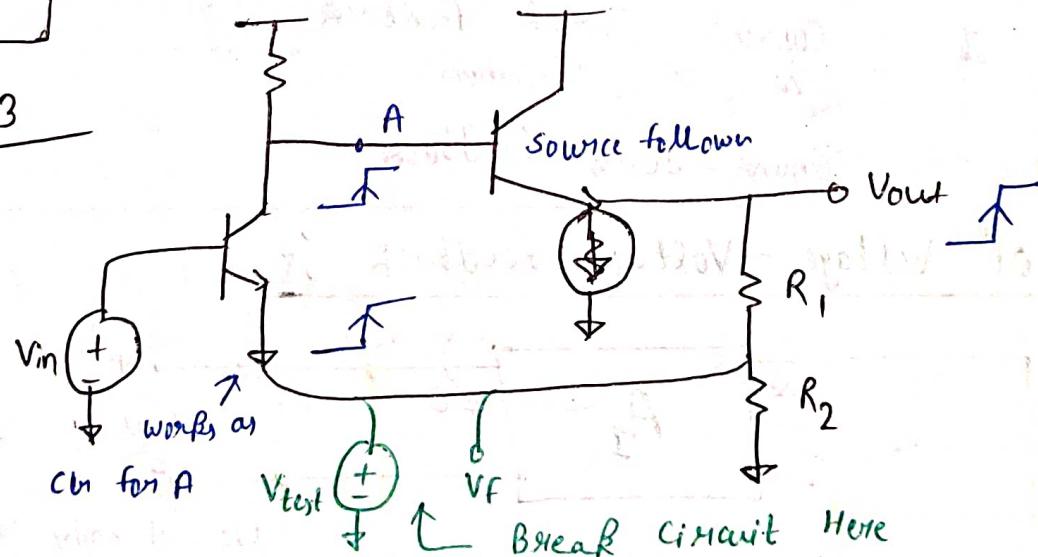


$$\text{So } A = \frac{V_A}{V_{in}} \text{ (also CS for B)}, \quad B = \frac{V_B}{V_A} \text{ goes low} \quad \text{Vout on } V_F$$

$V_{test} \uparrow \Rightarrow A \uparrow \Rightarrow B \uparrow \Rightarrow V_{out} \text{ on } V_F \uparrow \text{ So,}$

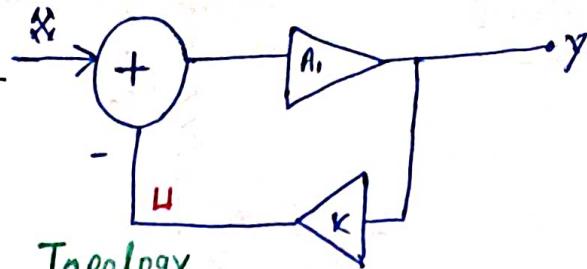
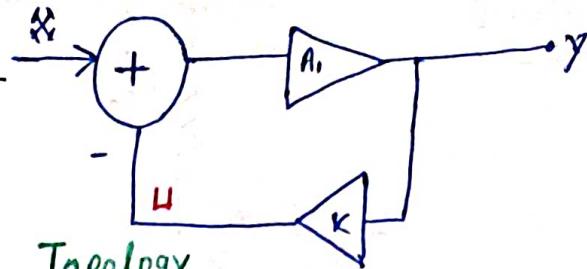
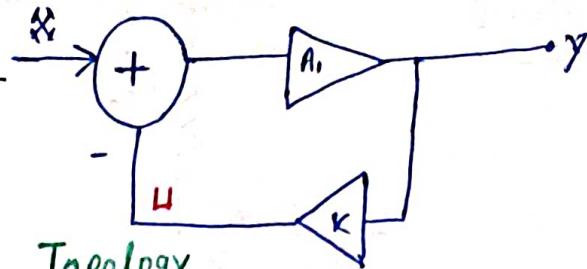
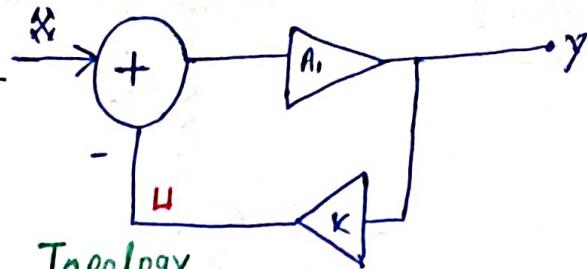
$$\frac{V_F}{V_{test}} = -ve \quad \text{Hence Negative feedback}$$

Example - 3

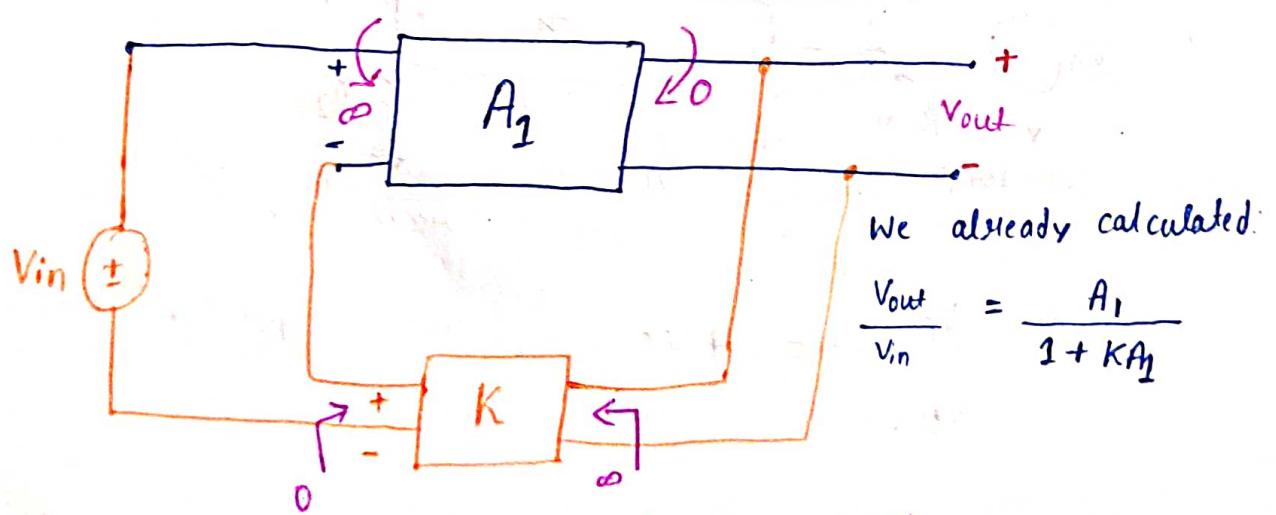


$$\text{So } \frac{V_F}{V_{test}} = +ve, \text{ Hence positive feedback.}$$

Four feedback Topologies :-

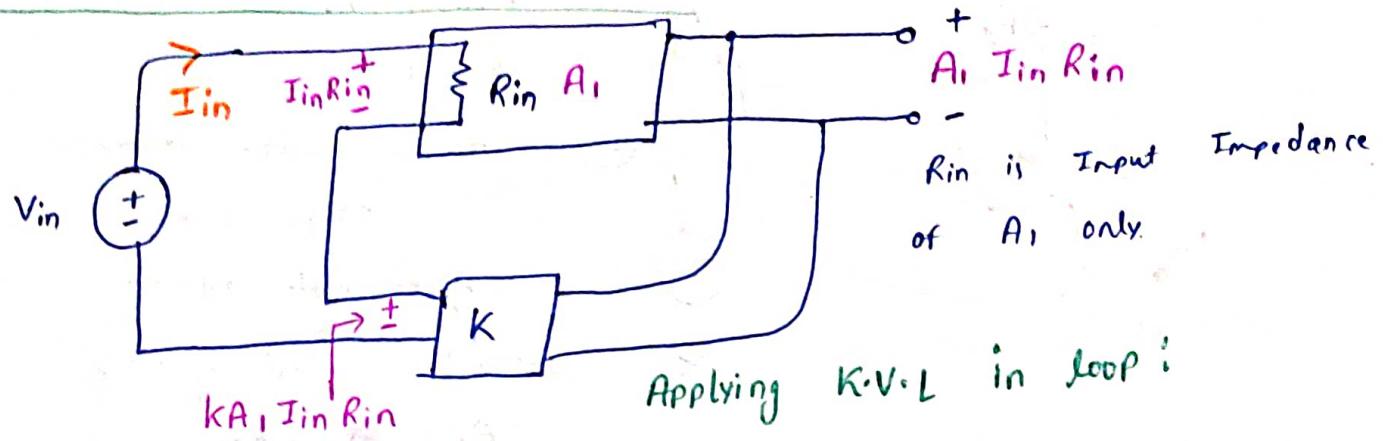
X	Y	U	Feedback Topology
V	V	V	Voltage - Voltage feedback  <p>To sense output voltage shunt connection needed</p> <p>while to return voltage series connection needed So it is also called Series-Shunt feedback.</p> <p>Note: Conventionally here we put I/p side first</p>
I	V	I	Voltage - Current feedback  <p>Sense voltage $\cancel{\rightarrow}$ (Return current)</p> <p>Shunt-shunt feedback</p>
V	I	V	Current - Voltage feedback  <p>Sense $\cancel{\rightarrow}$ Return</p> <p>Series-series feedback</p>
I	I	I	Current - Current feedback  <p>Sense $\cancel{\rightarrow}$ I/p, Return</p> <p>Shunt-series feedback</p>

Analysis of Voltage - Voltage Feedback :-



Ideally Input & output resistance are shown.

* Closed-loop Input Impedance

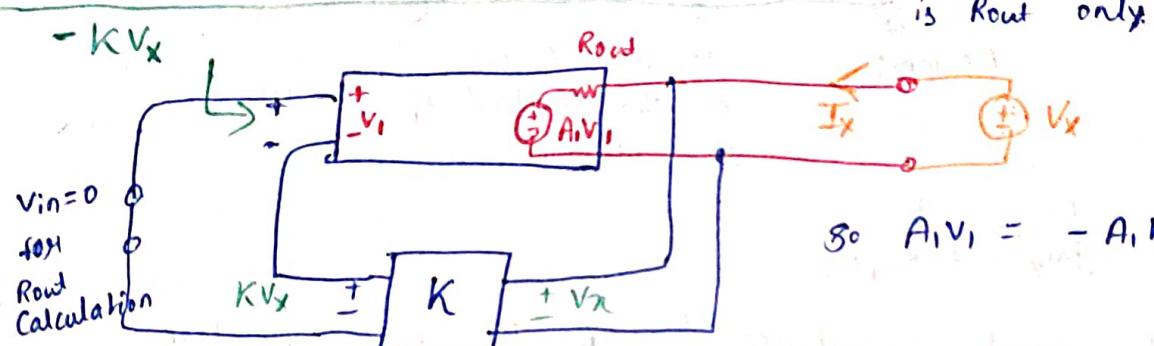


$$\Rightarrow V_{in} = I_{in} R_{in} + K A_1 I_{in} R_{in}$$

$$\Rightarrow \frac{V_{in}}{I_{in}} = R_{in} (1 + K A_1)$$

which is a advantage because in
Voltage - voltage feedback
we expect very High Input Impedance & -ve feedback Increased
this in comparison with open loop system.

* Closed-loop Output Impedance :- let o/p Impedance of A_1



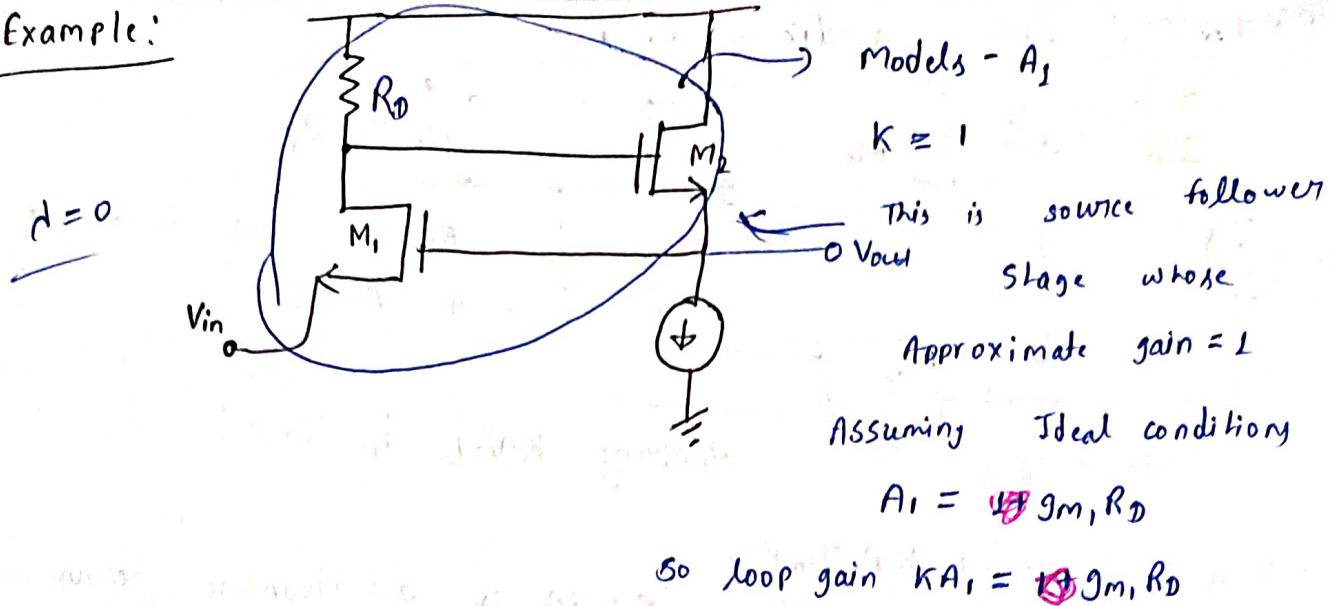
$$\text{Hence } I_x = \frac{V_x - (-A_1 K V_x)}{R_{out}}$$

$$\Rightarrow I_x = \frac{V_x (1 + K A_1)}{R_{out}}$$

$$\Rightarrow R_{out} = \frac{V_x}{I_x} = \frac{R_{out}}{1 + K A_1}$$

we expect R_{out} to less
& Negative feedback
even reduced this which
is a advantage

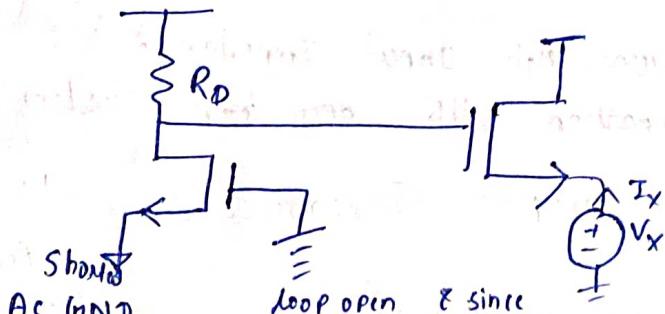
Example:



Closed loop output Impedance : first find open-loop output impedance.

Since $d = 0$

$$\frac{V_x}{I_x} = \frac{1}{g_{m2}} = R_{out}$$



loop open & since there also feedback I_p so that also AC GND

$$R_{out \text{ open}} = \frac{1}{g_{m2}} \times \frac{1}{1 + g_{m1} R_D}$$

Closed loop Input Impedance : first find open-loop Input Impedance.

That is $\frac{1}{g_{m1}}$. Because M_2 will load its preceding edge by ∞ impedance, because it's source follower. whose o/p resistance = High
 I_p resistance = High

$$\text{Closed loop Input Impedance} = \frac{1}{g_{m1}} (1 + A_1)$$

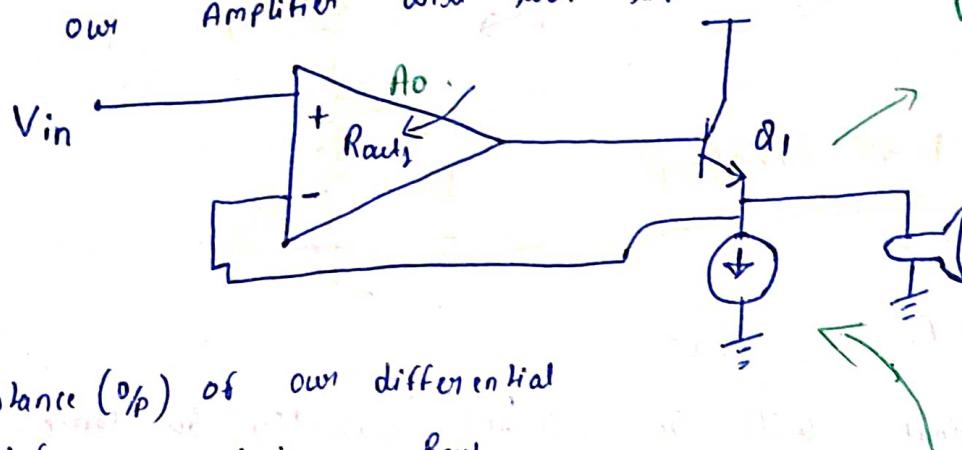
$$= \frac{1}{g_{m1}} (1 + g_{m1} R_D)$$

Application Example : Audio Amplifier :-

Since resistance of this audio device is just 8Ω & In common source stage R_D in $k\Omega$ so This will heavily load CS stage
so For this we need a amplifier such that:

- \Rightarrow Acts as buffer.
- \Rightarrow Does not load previous stage means High I/p Impedance
- \Rightarrow low O/p Impedance.

so our Amplifier will look like:



Voltage gain ≈ 1
but practically its not exactly 1

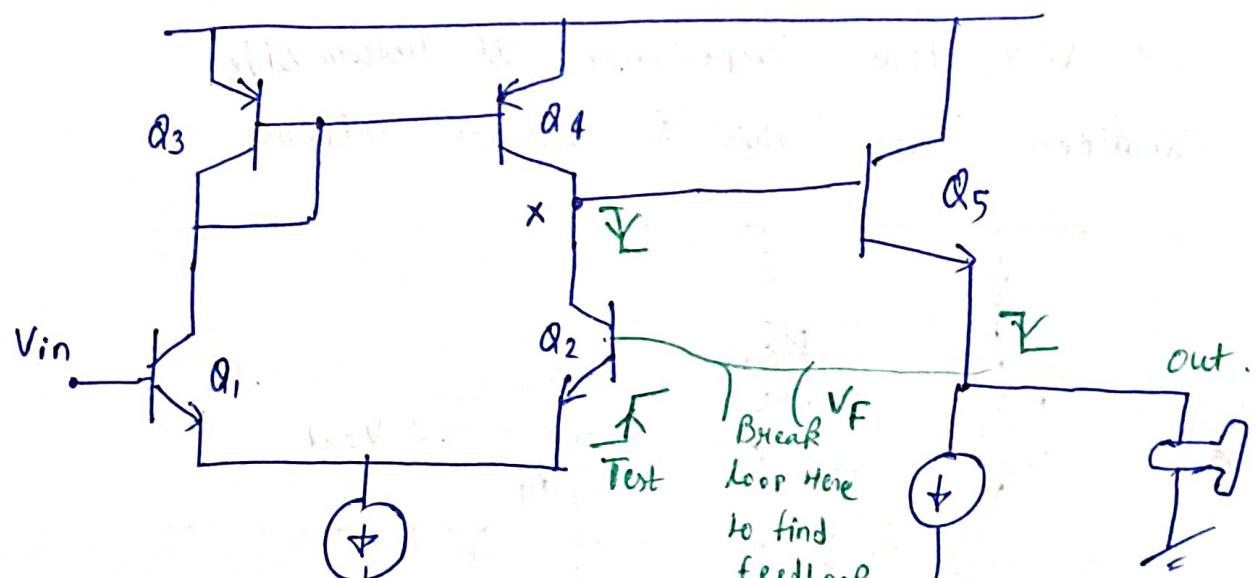
$$\text{loop gain} = 1 \times A_o = A_o$$

Resistance (Ω) of our differential amplifier only is: R_{out}

Due to Emitter follower it drops to $\frac{R_{out}}{\beta+1} + \frac{1}{g_m} = R_{out}'$

And due to negative feedback it further drops to: $\frac{R_{out}'}{1+A_o}$

\rightarrow How To Implement This Op-Amp? \rightarrow We can use a CS stage.
* we can also use Differential pair with active load.

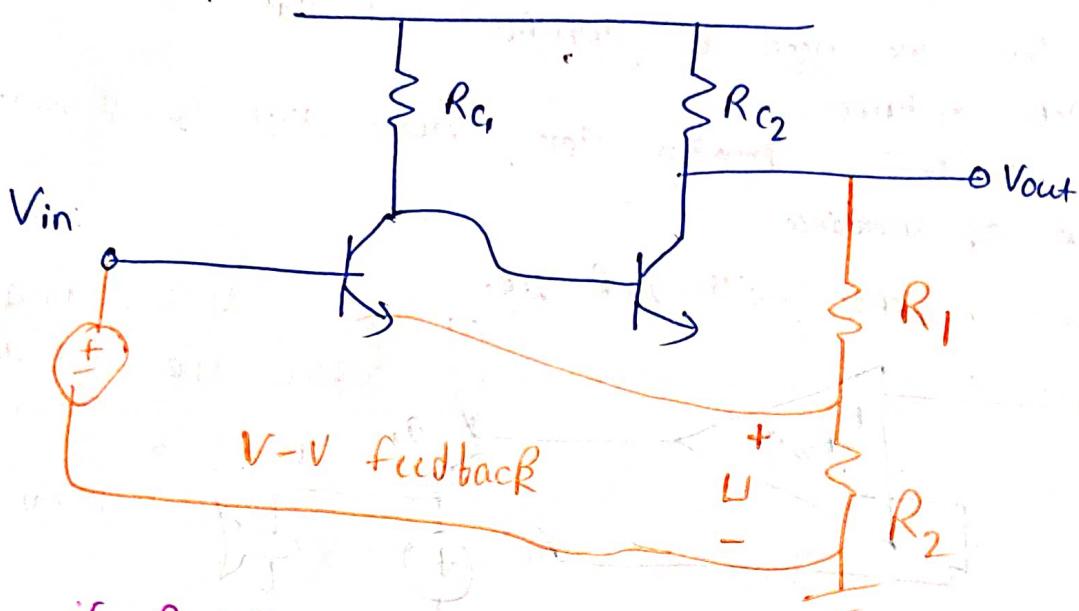


$$A_o \approx g_m n (\frac{R_{out}'}{R_{in}} || R_{op})$$

$A_o \approx g_m n (\frac{R_{out}'}{R_{in}} || R_{op})$
Disable vin while finding $(-\frac{V_f}{V_{test}})$.

Ques: Can we use a Transistor in a feedback Network :-

We studied a feedback circuit which have some serious concern:



Here:

if $R_1 + R_2$ is large:

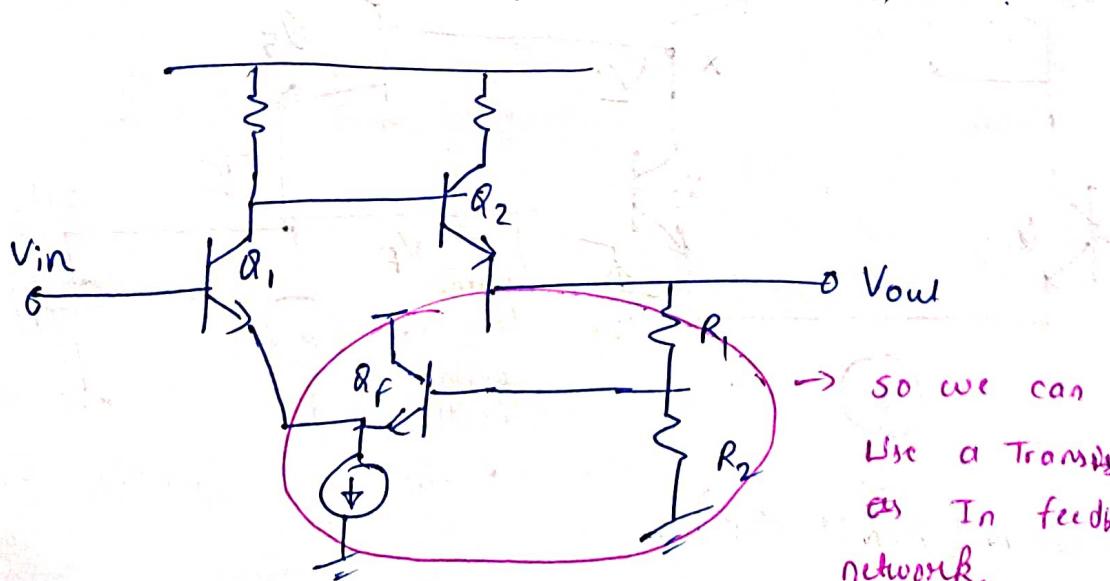
→ Then V_{out} will be sensed correctly but since same circuit ($R_1 - R_2$ divider) returning this voltage to Input. so It will be bad for return.

so we need something there which ~~is~~ have:

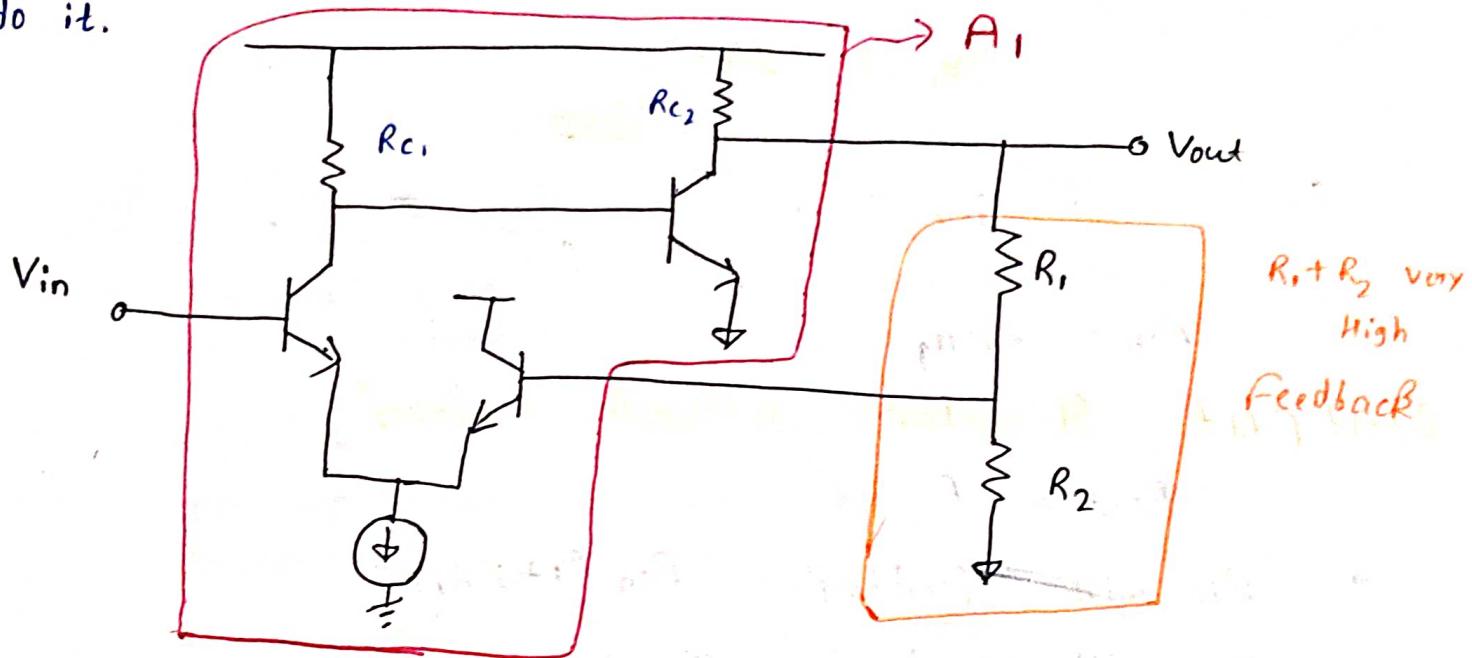
* High Resistance at sense side

* Very low Impedance at return side

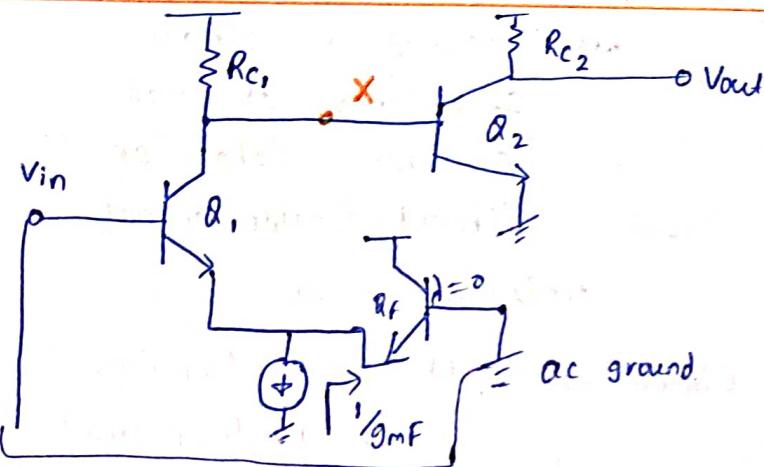
Best candidate for this is source follower.



In this Amplifier we can use α_F also as feedforward gain & remaining as feedback. Let us see how we do it.



* First find open loop parameters :-



$$\frac{V_{out}}{V_{in}} = \frac{V_x}{V_{in}} \cdot \frac{V_{out}}{V_x}$$

α_1 acts as source degenerate stage by Transistor α_F who offers $\frac{1}{g_{MF}}$ as degeneration resistance

$$so \quad \frac{V_x}{V_{in}} = \frac{-R_{C_1} || H_{\pi_2}}{\frac{1}{g_{M1}} + \frac{1}{g_{MF}}} \quad \text{This much resistance is loaded at } \alpha_2$$

For simplicity take $g_{MF} \approx g_{m1}$

$$\Rightarrow \frac{V_x}{V_{in}} = \frac{g_{m1}}{2} (-R_{C_1} || H_{\pi_2})$$

$$\text{Now, } \frac{V_{out}}{V_x} = -g_{m2} R_{C_2}$$

} However this is approximated because there is also $R_1 + R_2$ resistance in load but that is very large }

$$so \quad \text{open gain} = \frac{V_{out}}{V_{in}} = \frac{g_{m1} g_{m2}}{2} R_{C_2} (R_{C_1} || H_{\pi_2})$$

$$\text{Feedback (K)} = \frac{R_2}{R_1 + R_2} \quad \left\{ \text{Approximated because } \alpha_F \text{ is BJT so } R_1 \neq R_2 \right\}$$

Input Resistance without feedback:

$$R_{in} = \text{Source degenerated } g_m \text{ 's } I_{Dp} \text{ resistance}$$

$$= g_{mI} + (\beta + 1) \frac{1}{g_{mf}}$$

Since we taken $g_{mf} \approx g_m$, so $\frac{\beta}{g_{mf}} \approx H_{\pi_f} \approx H_{\pi}$,

$$R_{in} = 2H_{\pi_1}$$

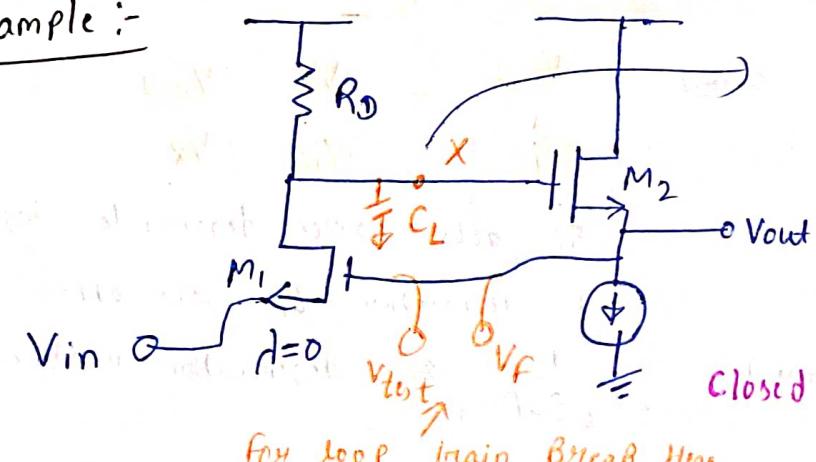
Output Resistance without feedback:

$$R_{out} = R_{C_2}$$

$$\therefore R_{in} \text{ with feedback} = R_{in} (1 + K A_1)$$

$$R_{out} \text{ with feedback} = R_{out} / (1 + K A_1)$$

Example:-



We assumed a single capacitance at load.
So this Behaves as first order circuit.
And we know.

$$\text{Closed loop BW} = (\text{Open-loop BW}) \times (1 + \text{loop gain})$$

open loop Bandwidth = pole frequency

$$= \frac{1}{R_D C_L}$$

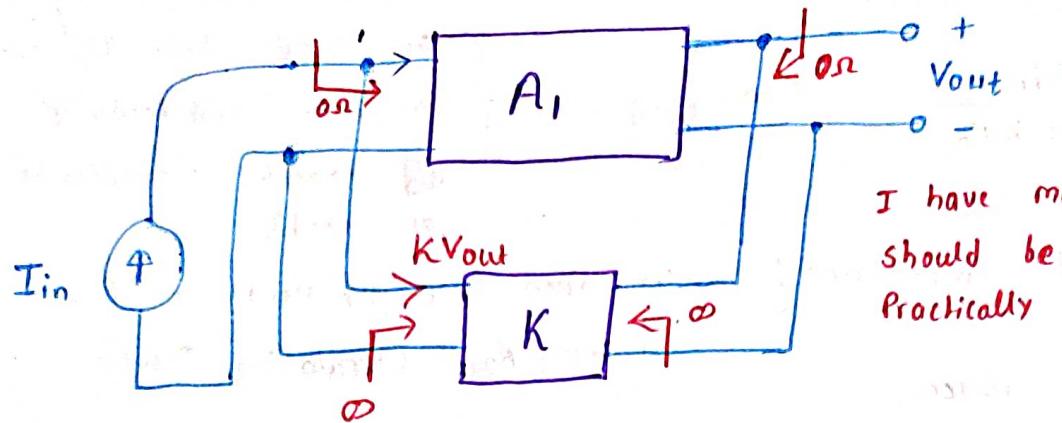
For mos source follower
bandwidth

$$\text{Loop gain} \left(\frac{-V_F}{V_{tot}} \right) = +g_m R_D \times 1$$

$$= g_m R_D$$

$$\therefore \text{Closed loop BW} = \frac{1}{R_D C_L} (1 + g_m R_D)$$

Voltage Current Feedback Topologies: (Trans Impedance Amplifier)



Here gain is of unit Ω so we will call it R_o

I have marked resistances which should be ideally seen. But practically these are not 0 & ∞

→ Here unit of A_1 is in ohm.

→ Does the unit of K always have to be $(\text{unit of } A_1)^{-1}$
We know closed loop gain = $\frac{A_1}{1+KA_1}$

From 12th level physics $\rightarrow \frac{1}{1+KA_1}$

Unit of KA_1 should also be same as unit of constant '1' \rightarrow unitless

So unit of $K = (\text{unit of } A_1)^{-1}$

Calculation of closed loop gain in this feedback topology:

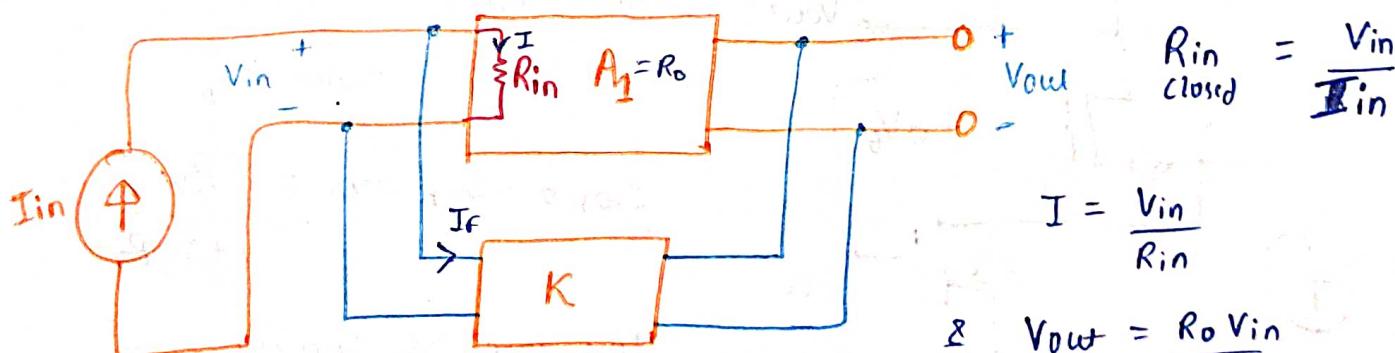
$$\text{Current going to } A_1 = I_{in} - KV_o$$

$$\text{So } R_o(I_{in} - KV_o) = V_{out}$$

$$\Rightarrow R_o I_{in} = V_{out}(1 + R_o K)$$

$$\Rightarrow \frac{V_{out}}{I_{in}} = \frac{R_o}{1 + KR_o}$$

Closed-loop Input Impedance: For this we need to assume open loop impedance ($I_{op} = R_{in}$)



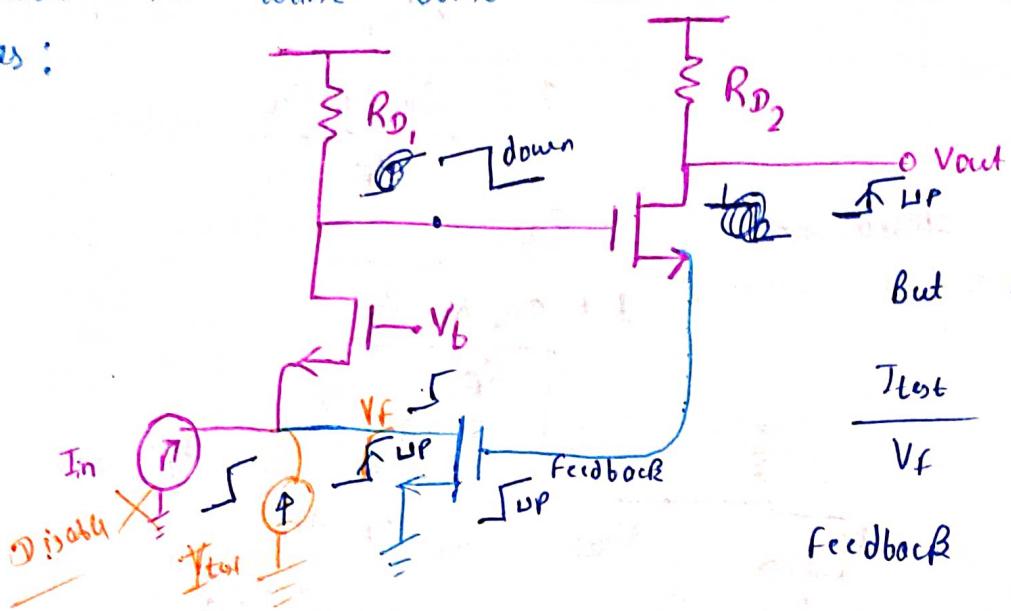
Hence

$$I = I_{in} - If$$

$$\frac{V_{in}}{R_{in}} = I_{in} - \frac{K R_o V_{in}}{R_{in}}$$

$$\text{So } If = \frac{K R_o V_{in}}{R_{in}}$$

Now if want some more brain and we make amplifier as:



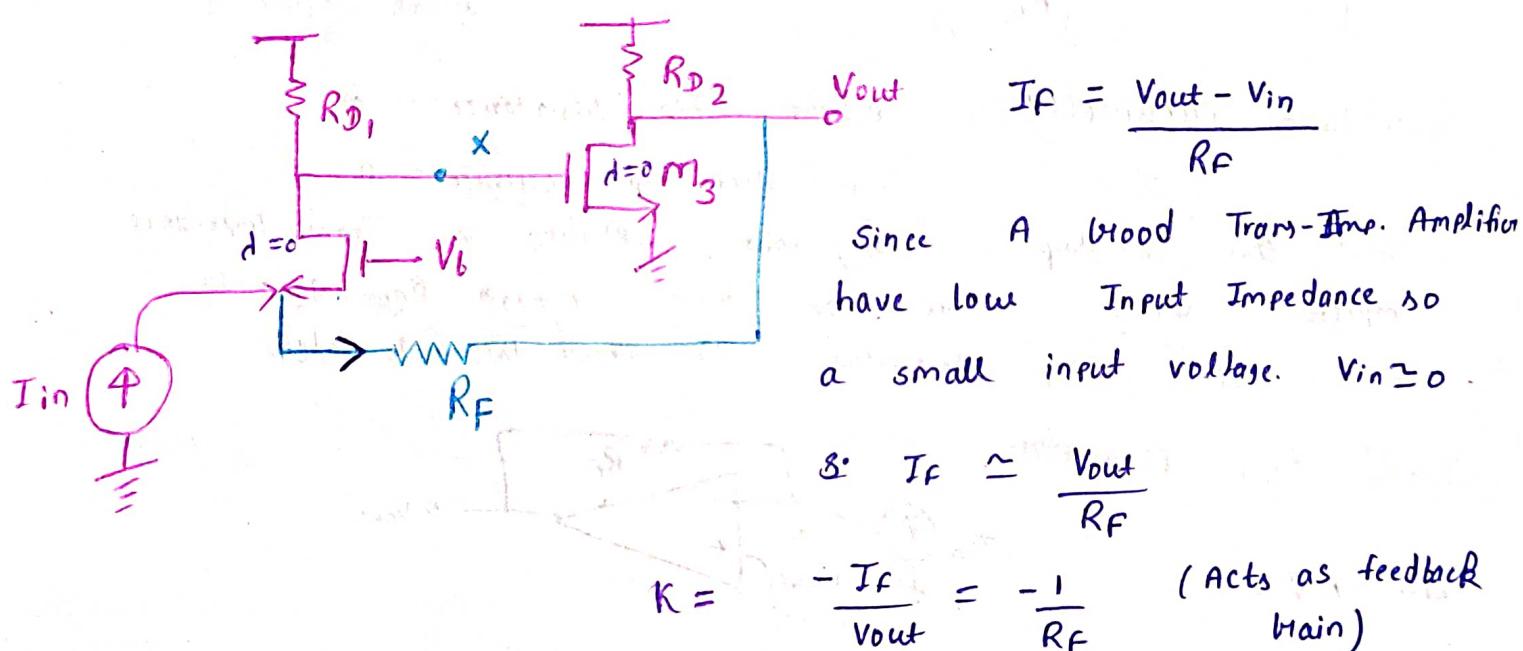
But there is a problem

$$\frac{I_{out}}{V_F} = +\infty$$

Feedback became +positive.

So we can't use this our circuit should be:

We know A transistor can convert a voltage to current so we will be using a Resistor in feedback



$$IF \approx \frac{V_{out}}{R_F}$$

$$-\frac{IF}{V_{out}} = -\frac{1}{R_F} \quad (\text{Acts as feedback gain})$$

Open loop parameters :-

$$\text{Brain} = \frac{V_{out}}{V_X} \cdot \frac{V_X}{V_{in}}$$

$$= (-g_m R_{D2}) (R_{D1})$$

$$\text{Open-loop resistance (Input)} = \frac{1}{g_m}$$

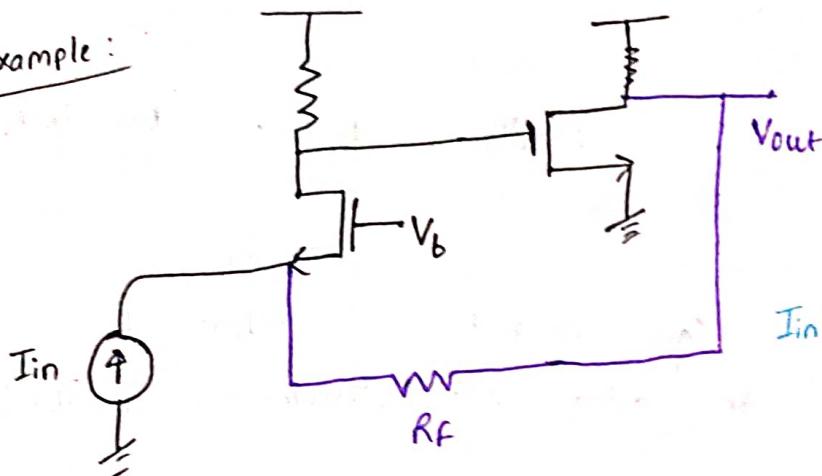
$$\text{Open-loop output resistance} = R_{D2}$$

$$\text{Closed loop parameters: } A_{VS} = \frac{-g_m R_{D1} R_{D2}}{1 + \frac{1}{R_F} (g_m R_{D1} R_{D2})}$$

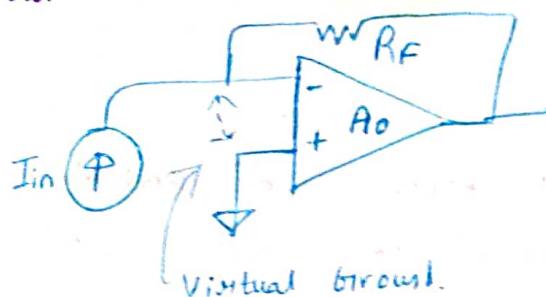
$$\text{Closed Loop Input Impedance} = \frac{1/g_m}{1 + \frac{g_m R_D R_D}{R_F}}$$

$$\text{Input Impedance closed loop} = \frac{R_D}{1 + \frac{g_m R_D R_D}{R_F}}$$

Example:



Realising this using OP-Amp:

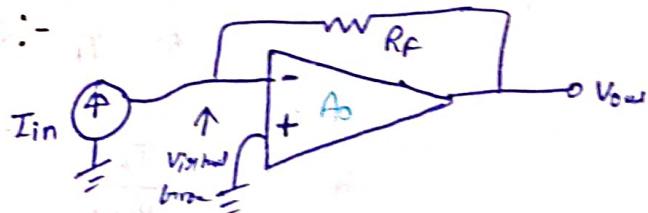


Open-loop parameters: OP-Amp I/p resistance = ∞

TIA need I/p resistance = 0

Still this OP-Amp in close loop working as Trans-Impedance amplifier why?
we don't have enough knowledge to study open-loop parameters. so defer this to later.

Closed - Loop parameter:-



Use KVL

$$I_{in} \times R_F = -V_{out}$$

Use Miller at Input side

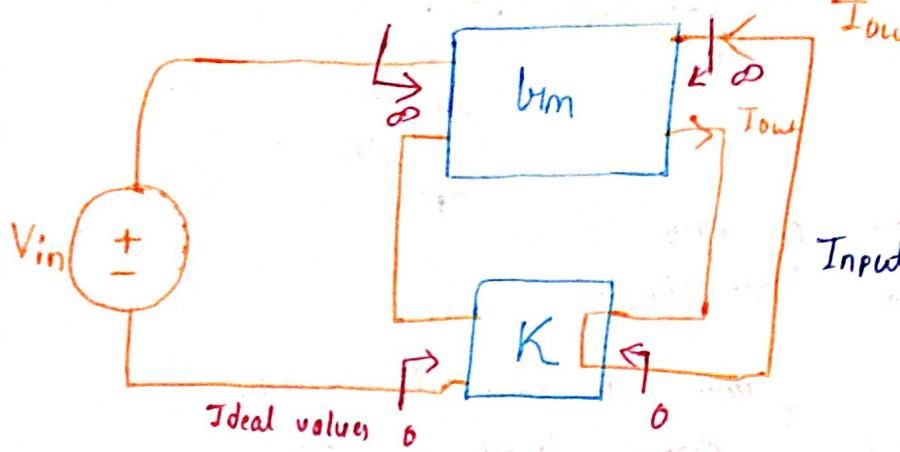
$$\Rightarrow \frac{V_{out}}{I_{in}} = \frac{-1}{R_F}$$

$$\frac{R_F}{1 + A_O}$$

$$\text{Format i)} \\ \frac{A_F}{1 - (A_V)}$$

It's connected at neg. terminal or main $-A_V$

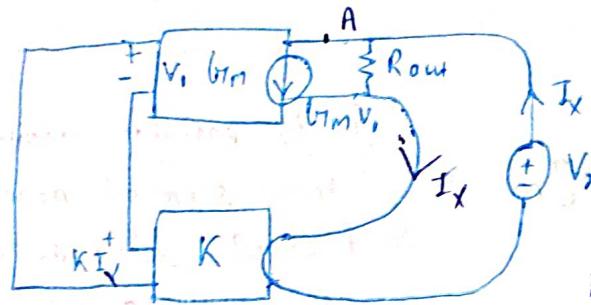
#3 Current - Voltage feedback :-



$$\frac{I_{out}}{V_{in}} = \frac{b_m}{1 + b_m K}$$

$$\text{Input Impedance} = R_{in} (1 + K b_m)$$

Closed loop o/p Impedance: Consider open loop o/p $T_{op} = R_{out}$



(Break wire), apply V_x, I_x and disable I/p source

$$V_x = -K I_x$$

K.C.L at point A

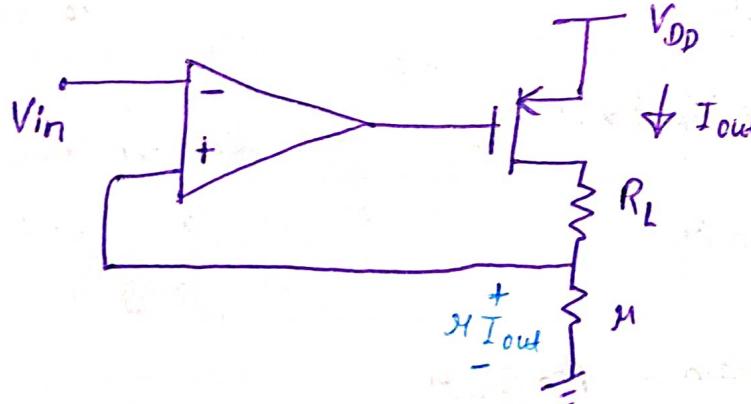
$$\Rightarrow -K I_x b_m + \frac{V_x}{R_{out}} - I_x = 0$$

$$\Rightarrow I_x (1 + K b_m) = \frac{V_x}{R_{out}}$$

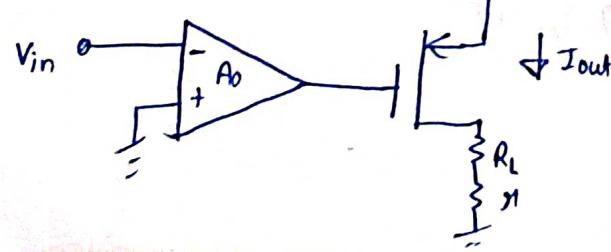
$$\Rightarrow R_{out \text{ closed}} = \frac{V_x}{I_x} = R_{out} (1 + K b_m)$$

{ Boosted by feedback which is a advantage }

Example :-



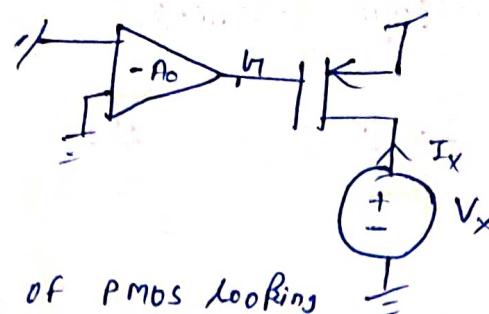
Open loop parameters:-



$$b_m = \frac{I_{out}}{V_{in}} = -A_0 g_m$$

Open loop output resistance:

$V_{in} \rightarrow$ disabled, Hence
gate of PMOS grounded.



So $R_{out} =$ O/p resistance of PMOS looking
into drain, gate shorted

$$R_{out} = M_0$$

{ Here we have to consider
channel length modulation }

loop gain

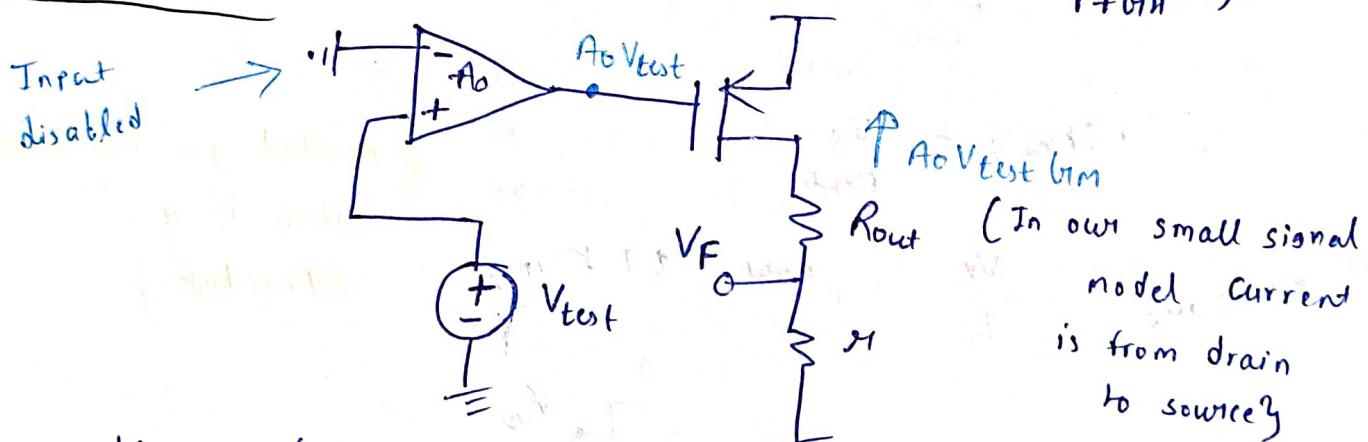
$$b_{IM} = -A_0 g_m$$

$$k = M_0$$

$$\text{So loop gain} = M_0 A_0 g_m$$

{ It's positive because
the sign of negative
feedback already considered
in formula while we
derived $\frac{b_I}{1+b_{IM}}$ }

Found loop gain by breaking
the loop:



$$V_F = (-A_0 V_{test} + b_{IM}) \times M_0$$

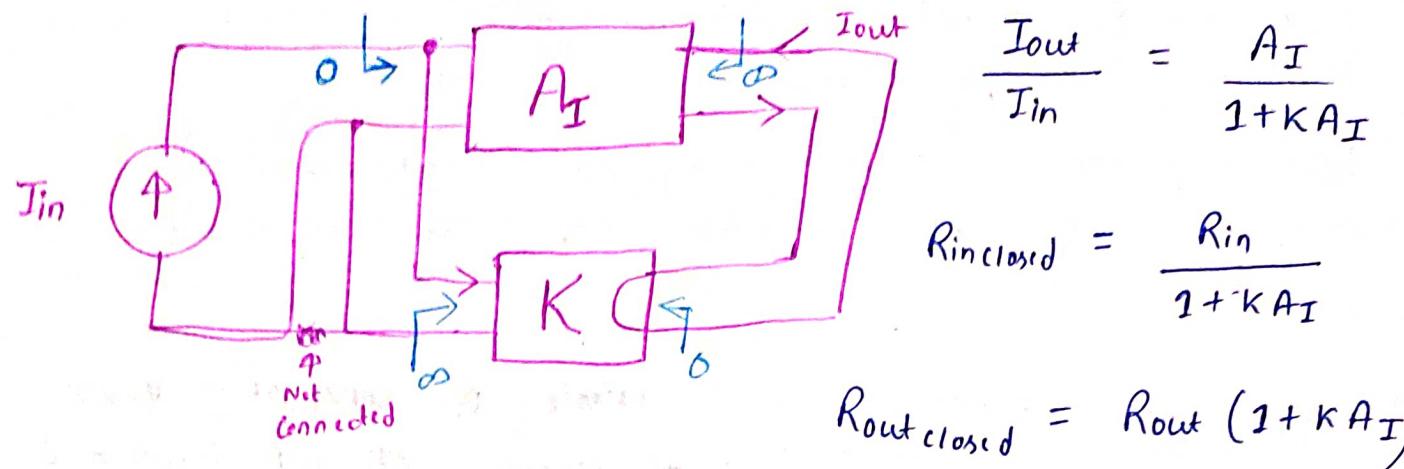
$$\frac{V_F}{V_{test}} = -A_0 g_m M_0$$

(we made approximation here
because some part of current
is also going in M_0)

$$\Rightarrow \frac{-V_F}{V_{test}} = \text{loop gain} = A_0 g_m M_0$$

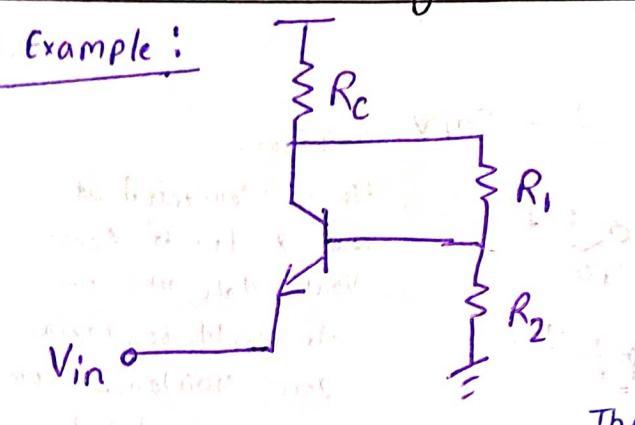
$$\text{So } R_{out \text{ closed}} = M_0 (1 + A_0 g_m M_0)$$

Current - Current Feedback :- It has very less applications.



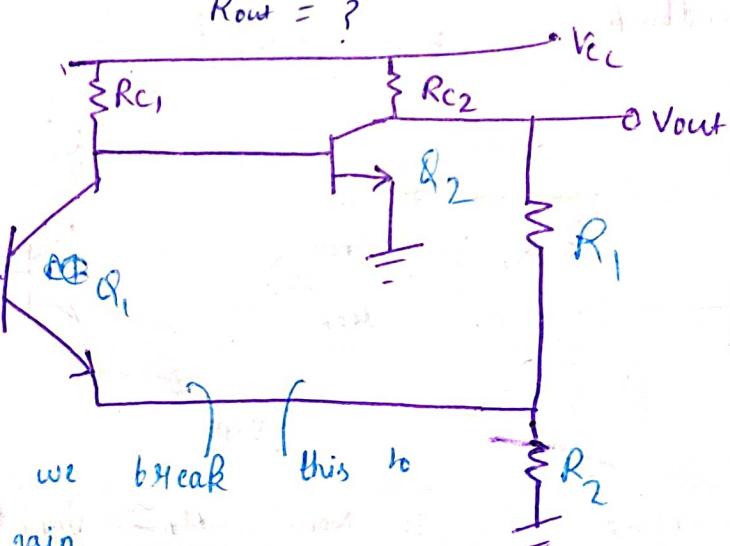
Problem of Loading in feedback Circuits :-

1) Example :-



while we calculated open loop gain. We ignored the fact that R_1 & R_2 are loading R_C . by saying R_1 & R_2 very large

2) Example :-

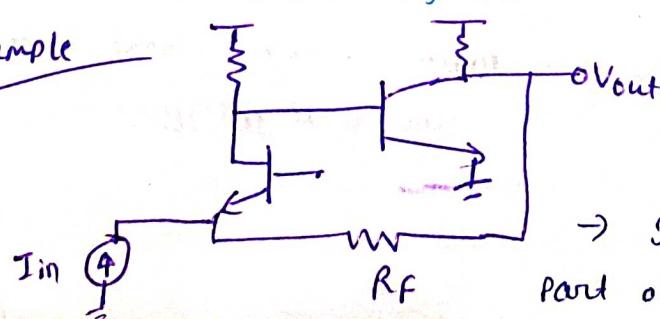


when we break this to calculate loop gain.

→ R_1 & R_2 loads R_C_2

→ There is source-degeneration at Q_1 which we are ignoring

3) Example



→ Here also same problem R_F is loading open-loop amplifier.

→ During A_v open calculation some part of I_{in} will be going in R_F .

Accurate Analysis of Feedback Circuits :-

→ Input and output impedances are not ideal. They can load when ideally they should not do it. To handle these developed some techniques. Proof of those techniques is not included here. One may develop intuitive understanding.

Opening Loop Property :-

Create a copy of feedback circuit at both input and

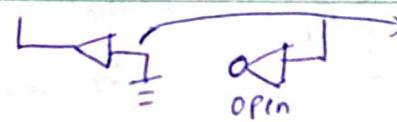
output terminals and make them open OR close as given below:

Topology

Feedback - COPY

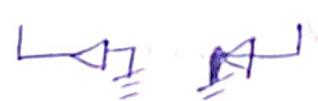
Intuition:

Voltage - Voltage feedback

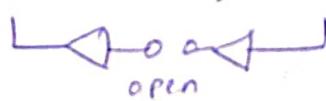


This is connected at V_{out} & try to sense V_{out} . That's why A_v would be having zero resistance there so we ground it.

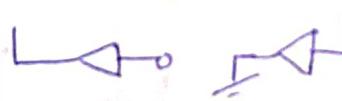
Voltage - Current feedback



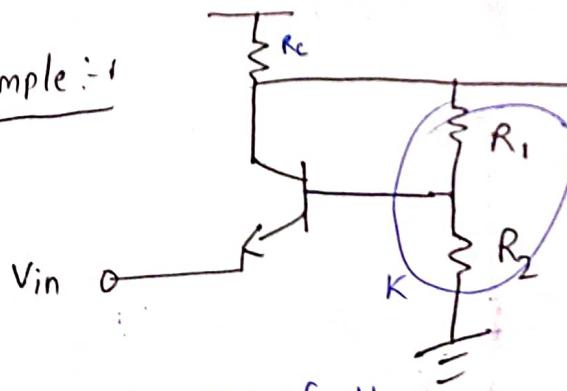
Current - Voltage feedback



Current - Current feedback

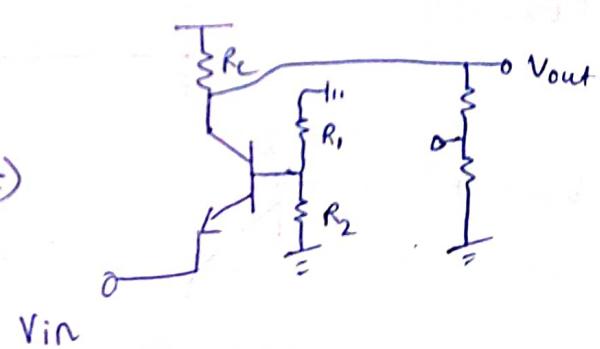


Example:-1



Vol-Vol feedback

$\text{open loop} \Rightarrow$



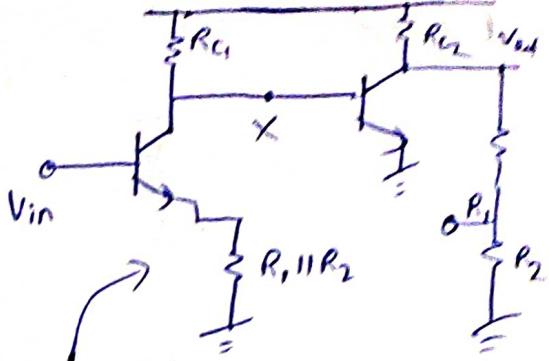
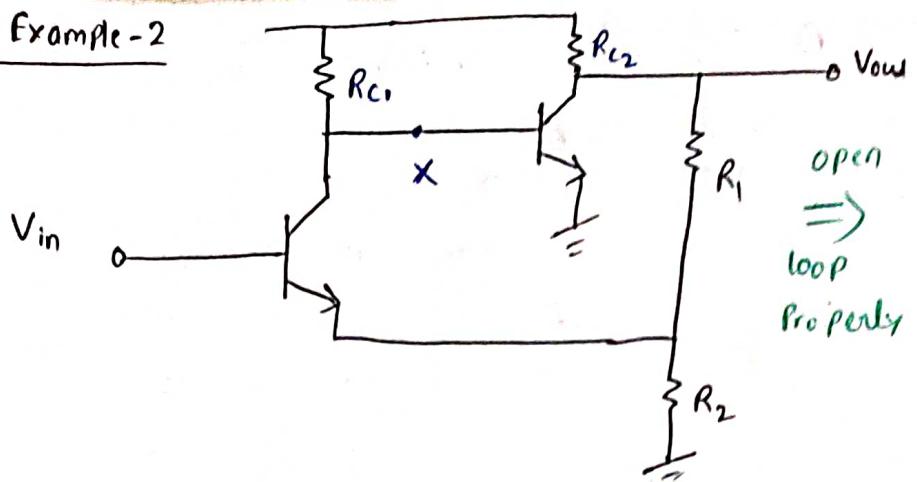
$$\text{So Now: } A_v = g_m [R_c || (R_1 + R_2)]$$

(Approx because base having some finite resistance & we ignoring that)

$$R_{in} = \frac{1}{g_m} + \frac{R_1 || R_2}{\beta + 1} \rightarrow \text{Apply small signal model, you will get it.}$$

$$R_{out} = R_c || (R_1 + R_2)$$

Example-2



Open-loop gain:-

$$A_V = \frac{V_{out}}{V_x} \cdot \frac{V_x}{V_{in}}$$

$$\frac{R_C}{\frac{1}{g_m} + R_E}$$

$$A_V = \left(-g_m \left[R_{C2} \parallel (R_1 + R_2) \right] \right) \left(\frac{-R_{C1} \parallel R_E}{\frac{1}{g_m} + (R_1 \parallel R_2)} \right)$$

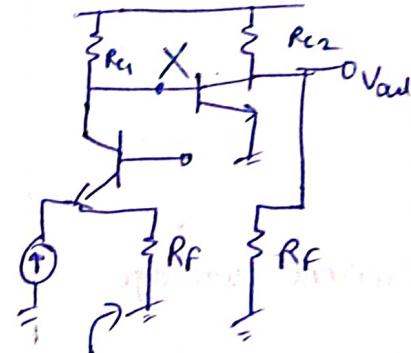
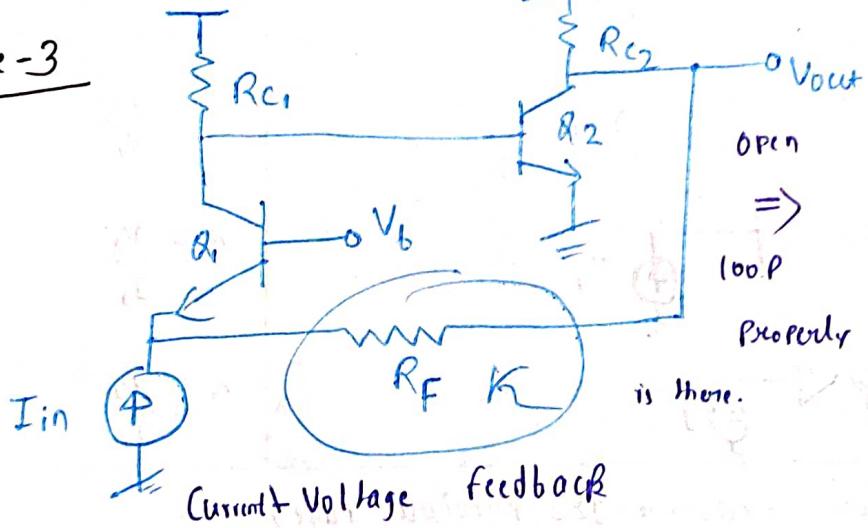
Open-loop Input Impedance :-

$$R_{in} = (B+1) R_1 \parallel R_2$$

Open-loop output Impedance :-

$$R_{C2} \parallel (R_1 + R_2)$$

Example-3



$$\text{Current available} = \frac{R_F}{R_F + \frac{1}{g_m}} I_{in}$$

Open-loop gain:-

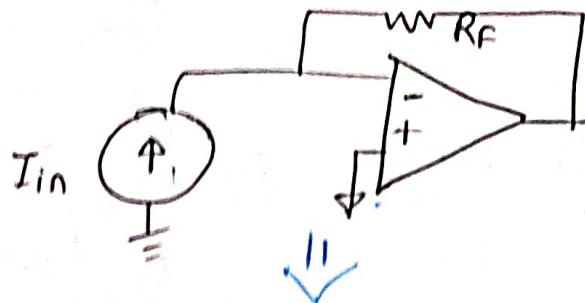
$$A = \frac{V_x}{I_{in}} \cdot \frac{V_{out}}{V_x} = \left[\frac{R_F}{\left(R_F + \frac{1}{g_m} \right)} \parallel (R_{C2} \parallel R_1) \right] (-g_m R_{C1})$$

Input Impedance (open-loop):

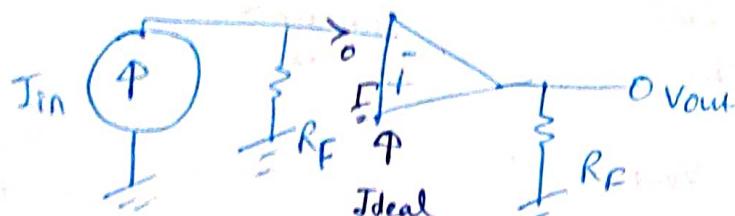
$$\frac{1}{g_m} \parallel R_F$$

Output Impedance (R_{out}) = $R_{C2} \parallel R_F$

Example:



Earlier, we were not able to study its open loop behaviour because we were unaware of accurate loop opening.



Ideal op-amp offers ∞ I/p resistance

$$\text{open loop } R_{in} = R_F \parallel \infty = R_F$$

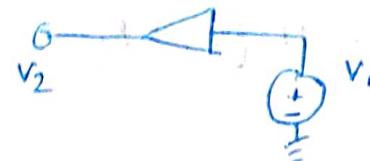
Finding Feedback Factor, K

Topology

Feedback arrangement

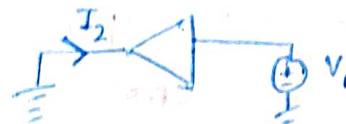
K

Voltage - Voltage fed.



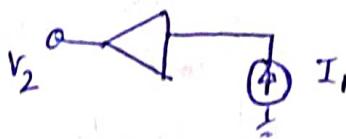
$$K = \frac{V_2}{V_1}$$

Voltage - Current



$$K = \frac{I_2}{V_1}$$

Current - voltage



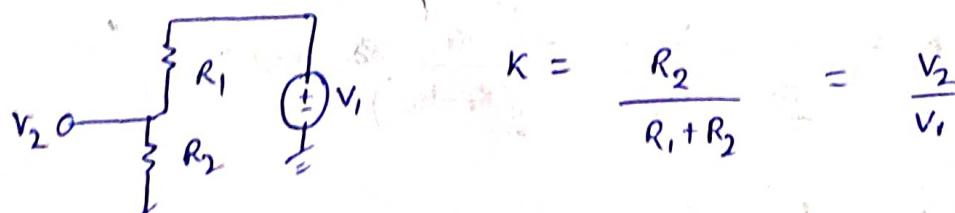
$$K = \frac{V_2}{I_1}$$

Current - Current



$$K = \frac{I_2}{I_1}$$

So Feedback factor for example-182 (previous page)

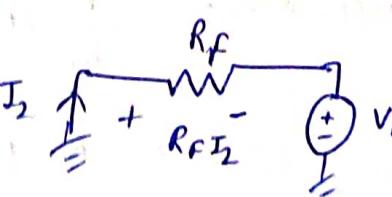


$$K = \frac{R_2}{R_1 + R_2} = \frac{V_2}{V_1}$$

Feedback factor for example -3

Using K.V.L

$$V_1 + R_F I_2 = 0$$

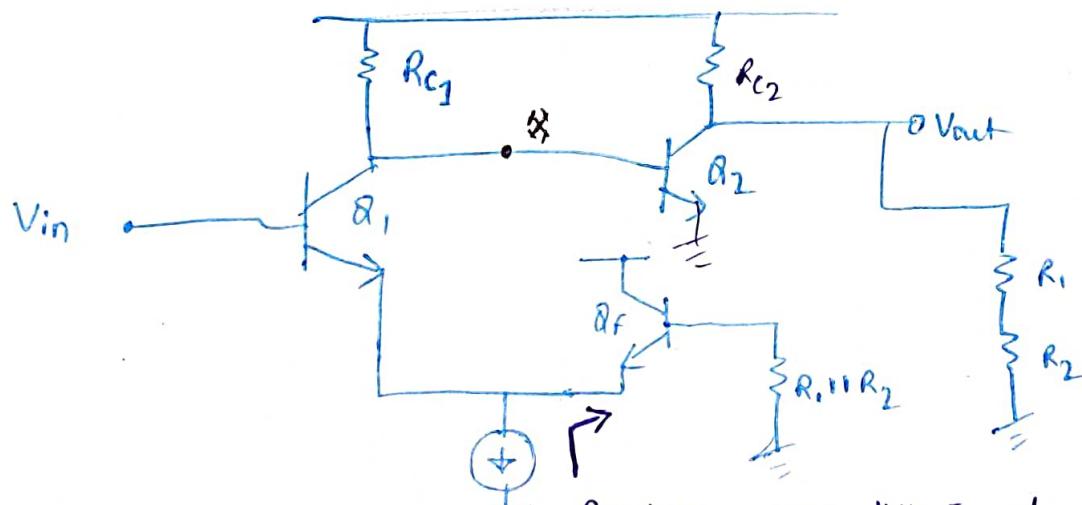
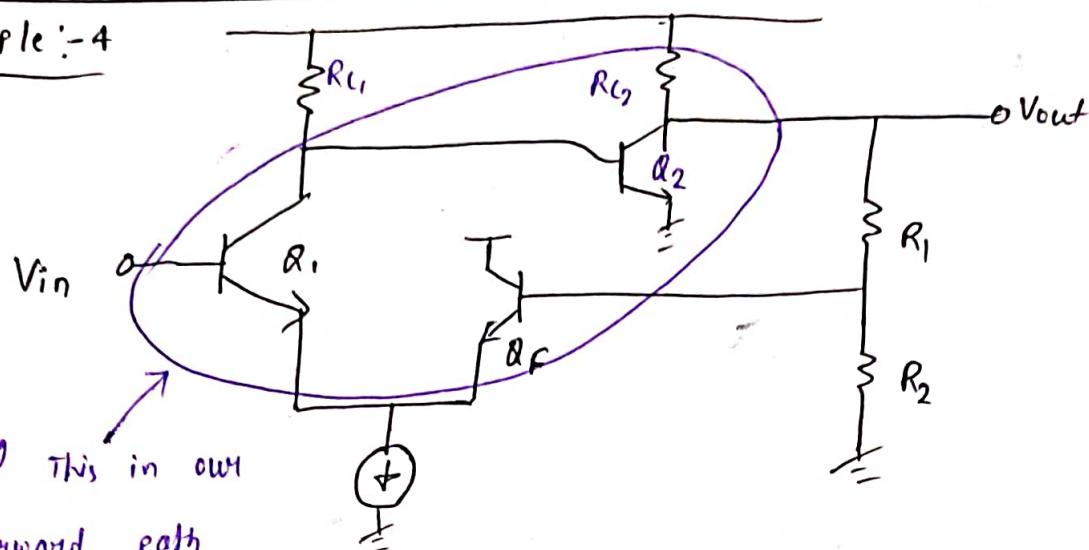


$$\Rightarrow \frac{I_2}{V_1} = -\frac{1}{R_F} = K$$

Note: For negative feedback loop gain is $+ve$. $A_1 = -ve$
 $K = -ve$

Hence, so $KA_1 = +ve$

Example:-4



$$\text{Resistance seen here} = \frac{1}{g_{mF}} + \frac{R_1 || R_2}{\beta + 1}$$

Open loop gain :-

$$\frac{V_{out}}{V_{in}} = \left(\frac{V_x}{V_{in}} \right) \left(\frac{V_{out}}{V_x} \right)$$

Emitter degenerated by β_F

$$\frac{V_x}{V_{in}} = \frac{-R_{C1} || \mu_{\pi_2}}{\frac{1}{g_{m_1}} + \frac{1}{g_{m_F}} + \frac{R_1 || R_2}{\beta + 1}}$$

$$\frac{V_{out}}{V_x} = -g_{m_2} \cdot \left[R_{C2} || (R_1 + R_2) \right]$$

Input Resistance :

$$\frac{V_{in}}{I_{in}} = \mu_{\pi_1} + (\beta + 1) R_E$$

$$R_{in} = \mu_{\pi_1} + \frac{(\beta + 1) R_1 || R_2}{\beta + 1} + \frac{\beta + 1}{g_{m_F}}$$

(open loop)

$$R_{in} = \mu_{\pi_1} + R_1 || R_2 + \mu_{\pi_F}$$

{ we taken β of all
BJT's same }

Open loop output resistance :-

$$R_{out} = R_{C_2} \parallel (R_1 + R_2)$$

and

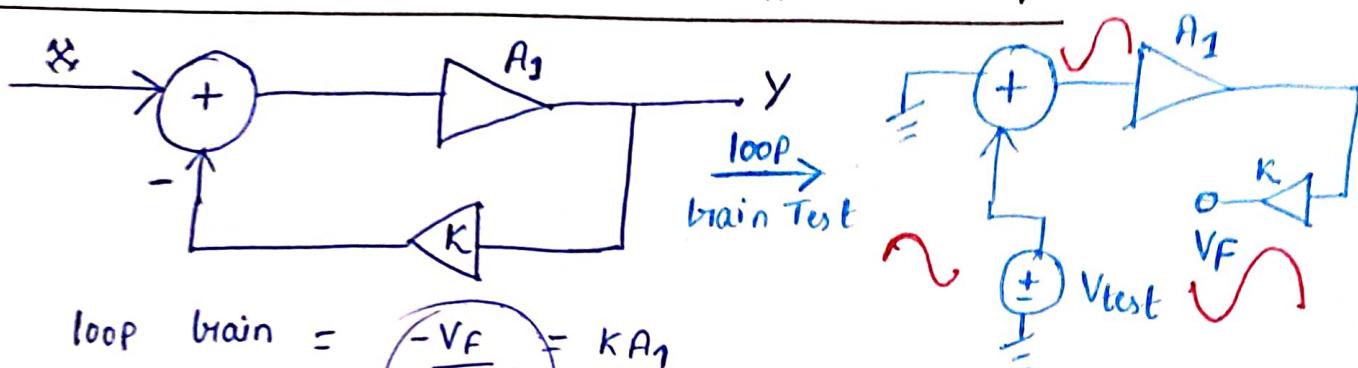
$$K = \frac{R_2}{R_1 + R_2}$$

$$\frac{R_2}{1+K} + \frac{1}{2\pi f C} \text{ and hence } G_{out} = \frac{1}{2\pi f C} \text{ and } R_{out} = \frac{1}{G_{out}}$$

Unit : 5

Stability Analysis

Instability in Negative Feedback System :-

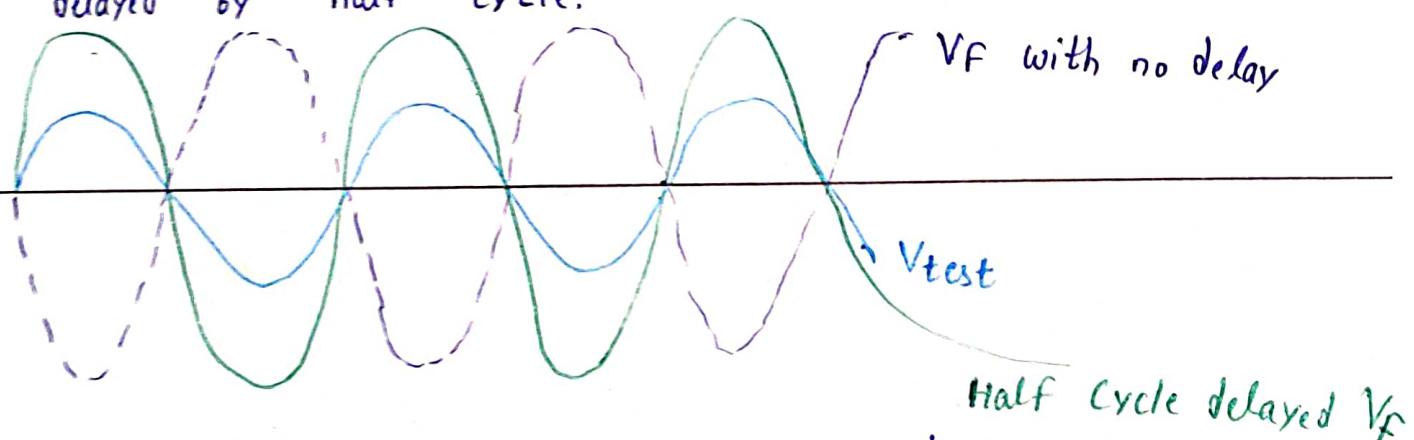


$$\text{loop brain} = \frac{-V_f}{V_{\text{test}}} = KA_1$$

This should be +ve for feedback to be negative. so V_f is actually degrading V_{test} because it's -ve of V_{test} .

How This Negative feedback can become +ve?

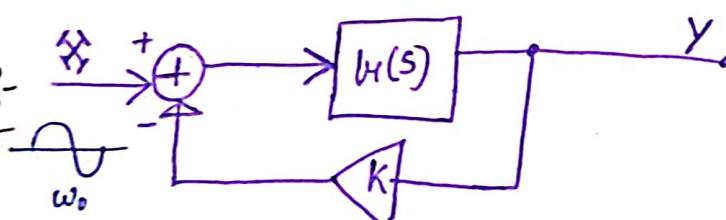
→ Actual Circuits have some delay. Let us say V_f is delayed by half cycle.



→ V_f actually enhances V_{test} and feedback becomes positive. Instability or Oscillations introduced.

Analysis for Instability :-

$$\frac{Y}{X} = \frac{b(s)}{1 + kb(s)}$$



There is something special about sinusoidal I/p. There shape does not change. Amplitude of Input multiplied by |Transfer function| & phase is shifted by \angle Trans. function.

$$\frac{Y}{X} = \frac{K H(s=j\omega_0)}{1 + K H(s)} \rightarrow \text{TF at some frequency has gain -1.}$$

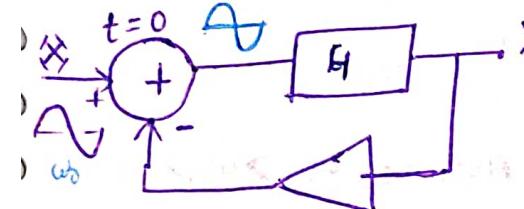
\Rightarrow Unstable loop.

\Rightarrow Good for building oscillators
Bad for building Amps.

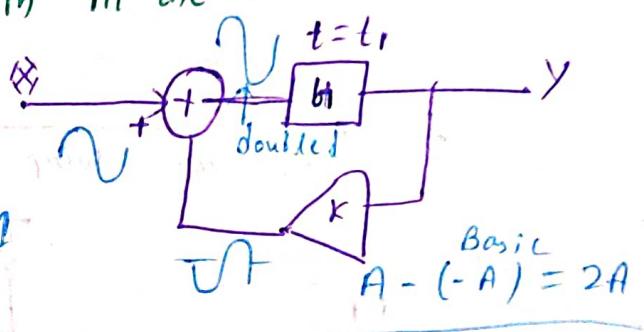
To avoid instability, we need to ensure $K H(j\omega) \neq -1$ for any

so $K H(j\omega_0) = -1$ $\left\{ \begin{array}{l} |K H(j\omega_0)| = 1, \text{ In dB its } 0 \text{ dB} \\ \angle K H(j\omega_0) = 180^\circ \end{array} \right.$

Examine the closed-loop system in the time-domain:-



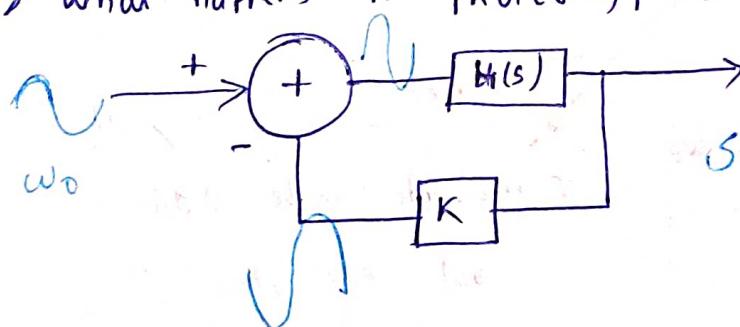
After some time
since $K H(j\omega_0) = -1$



so y keeps building & oscillates.

Important Points:-

- If the open-loop system satisfies $K H(j\omega_0) = -1$, then the closed-loop system is unstable.
- Even if $X = 0$, the system will oscillate if $K H(j\omega_0) = -1$
- What happens if $|K H(j\omega_0)| > 1$ and $\angle K H(j\omega_0) = 180^\circ$



Still system oscillation.

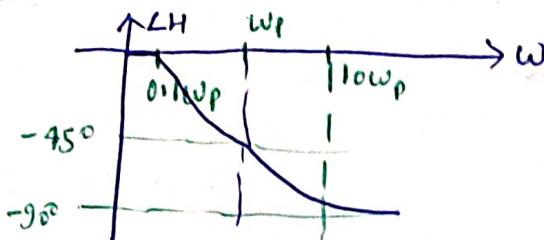
If there are no supply voltage constraint, losses etc then this amplifier may oscillate to ω . It is limited by these imperfections.

→ K usually have no phase shift so,

$$\angle K H(j\omega_0) \approx \angle H(j\omega_0)$$

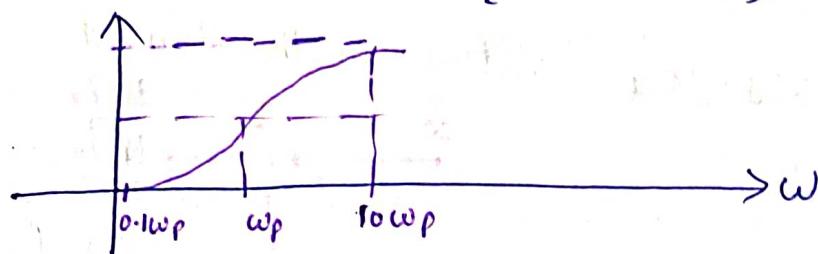
Bode's Rules for phase plot :-

→ If we have a pole at ω_p , then LH experiences a change of -45° at ω_p and -90° at $10\omega_p$.

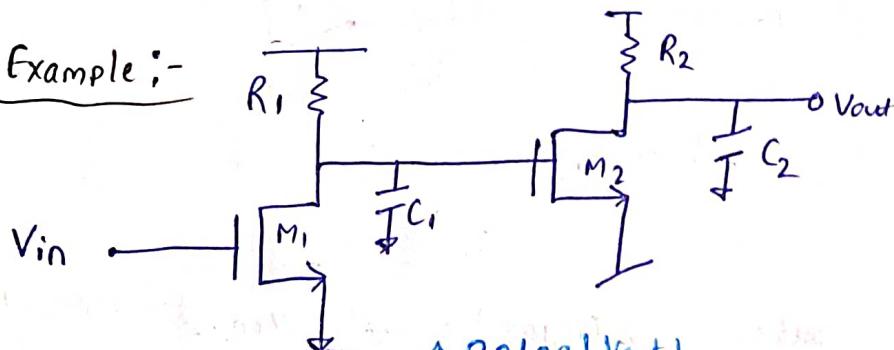


At $0.1\omega_p$, change starts coming in plot.

→ If we have a zero at ω_z , then LH experiences a change of $+45^\circ$ at ω_z and $+90^\circ$ at $10\omega_z$.



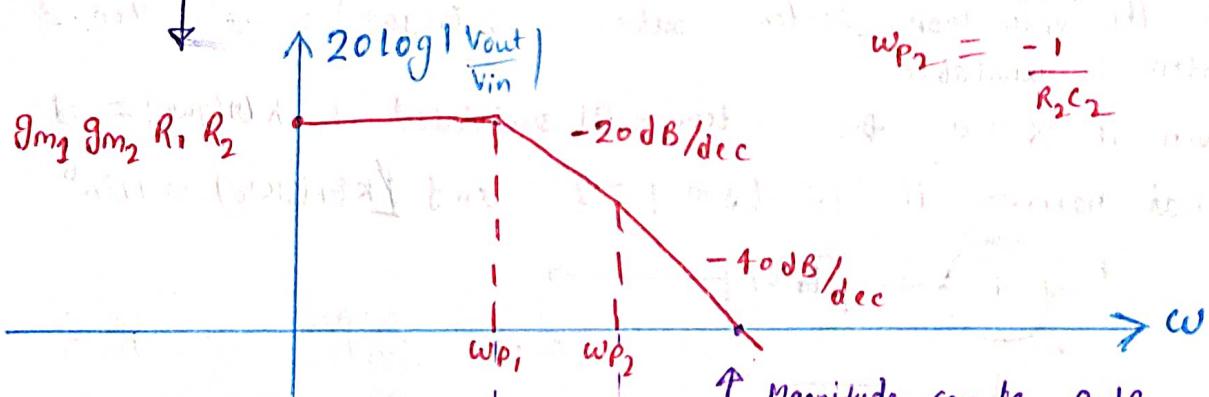
Example:-



Assume $\omega_{p_2} > \omega_p, \times 10$
8 perform Magn. & Phase analysis.

$$\omega_{p_1} = \frac{-1}{R_1 C_1}$$

$$\omega_{p_2} = \frac{-1}{R_2 C_2}$$



Phase

ω_{p_1} ω_{p_2}

-95° $-10\omega_{p_2}$ ∞ frequencies

so This circuit cannot oscillate



Stability Condition :-

- frequency at which zero dB brain occurs is brain-crossover frequency (ω_{gc}).
 - frequency at which 180° phase-shift occurs is phase crossover frequency. (ω_{pc})
-
- The figure consists of three sub-plots:
- (1) Unstable:** Shows a magnitude plot with $20\log|H(j\omega)|$ on the y-axis and frequency ω on the x-axis. A horizontal line at zero dB is labeled "brain". The plot shows a corner frequency ω_0 where the slope changes from +20dB/decade to -20dB/decade. The phase plot below it shows a corner frequency ω_{gc} where the phase crosses -180° . The two frequencies are marked as equal: $\omega_{gc} = \omega_{pc}$.
 - (2) Unstable:** Shows a magnitude plot where the brain (zero dB line) is above the plot. The phase plot shows a corner frequency ω_{pc} where the phase crosses -180° . The text indicates $\omega_{gc} > \omega_{pc}$.
 - (3) Stable:** Shows a magnitude plot where the brain (zero dB line) is below the plot. The phase plot shows a corner frequency ω_{pc} where the phase crosses -180° . The text indicates $\omega_{gc} < \omega_{pc}$.

Reason Because for Stability :

$$|\text{Brain}| > 1 \quad \text{or} \quad 0 \text{ dB}$$

and $\angle \text{Phase} = 180^\circ$ should not be together

Satisfied. Then we can guarantee Amplifier is stable at all frequencies.

In fig 1: at $\omega = \omega_0$ both condition satisfied so unstable.

In fig 2: at $\omega = \omega_{pc}$, $|\text{Brain}| > 0 \text{ dB}$ so Unstable

In fig 3 ω_{gc} occurred before ω_{pc} so both condition will never satisfy together. Hence Stable.

which implies, for all $\omega > \omega_{gc}$ $\angle \text{Phase} < -180^\circ$

start with a negative slope \Rightarrow $\angle \text{Phase} < -180^\circ$

Stability Condition :-

- frequency at which zero dB brain occurs is gain-cross-over frequency (ω_{gc}).
 - frequency at which 180° phase-shift occurs is phase or cross-over frequency (ω_{pc})
-

Reason Because for Stability :

$$| \text{Gain} | > 1 \text{ or } 0 \text{ dB}$$

and $\angle \text{Phase} = 180^\circ$ should not be together.

Satisfied. Then we can guarantee Amplifier is stable at all frequencies.

In fig 1: At $w = w_0$ both condition satisfied so unstable.

In fig 2: at $w = w_{pc}$, $|\text{Gain}| > 0 \text{ dB}$ so Unstable

In fig 3 ω_{gc} occurred before w_{pc} so both condition will never satisfy together. Hence Stable

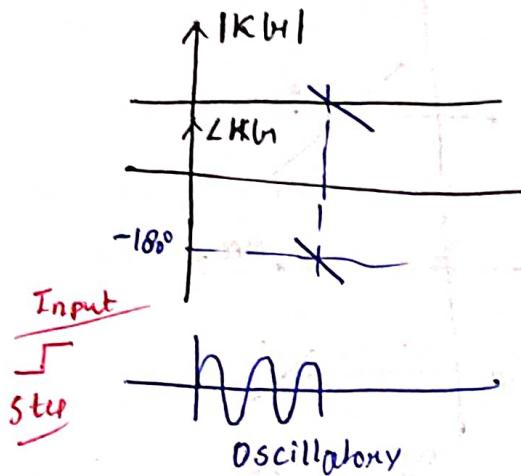
so $\omega_{gc} < w_{pc}$ to be stable.

so $\omega_{gc} < w_{pc}$ to be stable.

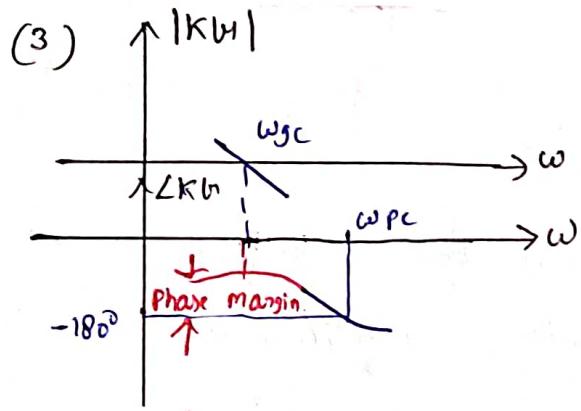
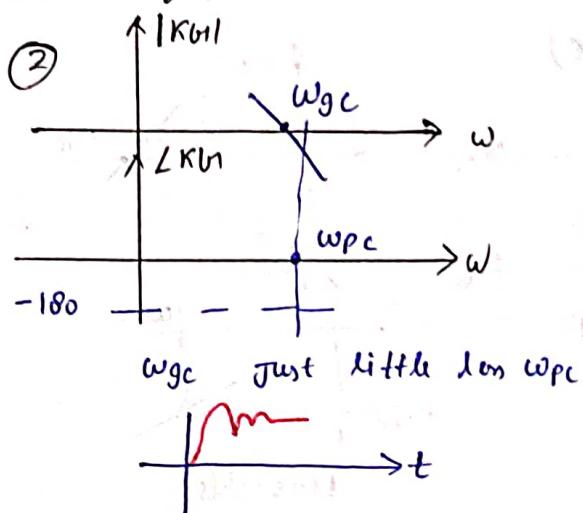
so $\omega_{gc} < w_{pc}$ to be stable.

Phase Margin :- To test stability we apply a step input & see what response it produces.

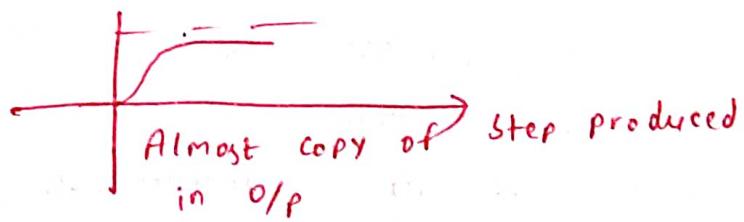
(1) ω_{gc} & ω_{pc} almost equal:



(2) ω_{gc} just little less than ω_{pc}



ω_{gc} is sufficiently lower than ω_{pc} . so now system will be more stable.

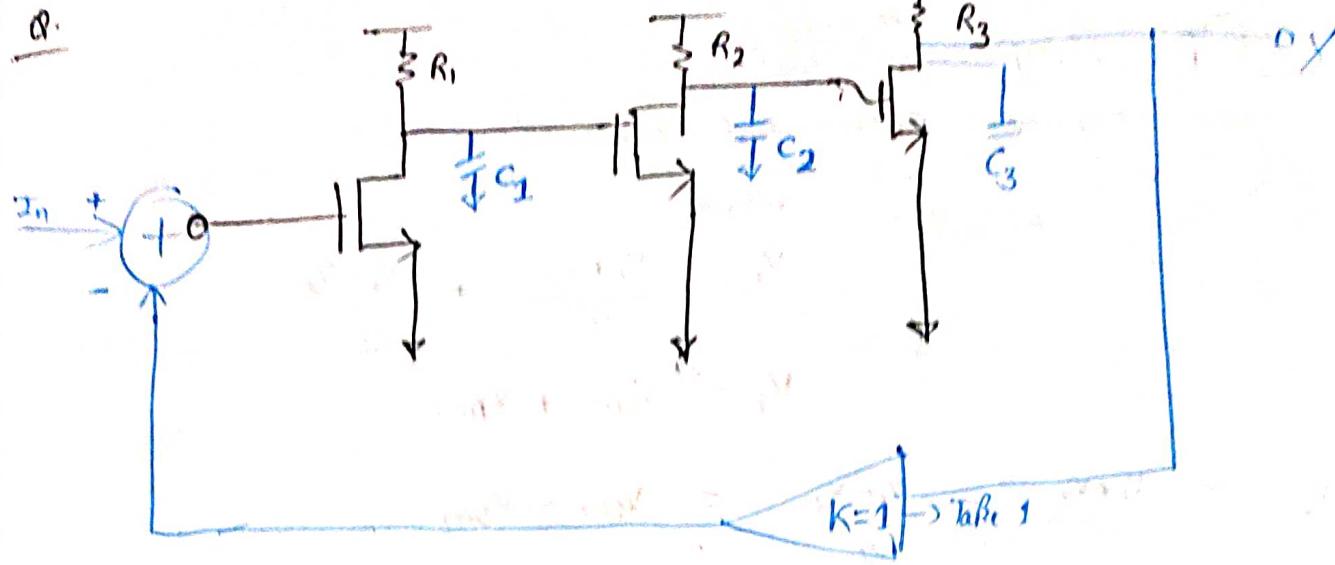


So difference between phases at ω_{gc} & ω_{pc} we define as phase margin. It should be high $\approx 60^\circ$ for well behaved response.

$$\begin{aligned} PM &= \angle K_{B1}(\omega_{gc}) - (\angle K_{B1}(\omega_{pc})) \quad \leftarrow \text{Angle at } \omega_{pc} \\ &= \angle K_{B1}(\omega_{gc}) - (-180^\circ) \\ &= \angle K_{B1}(\omega_{gc}) + 180^\circ. \quad \text{Answer} \end{aligned}$$

Frequency Compensation : \rightarrow The act of stabilizing system is called f-compensation.

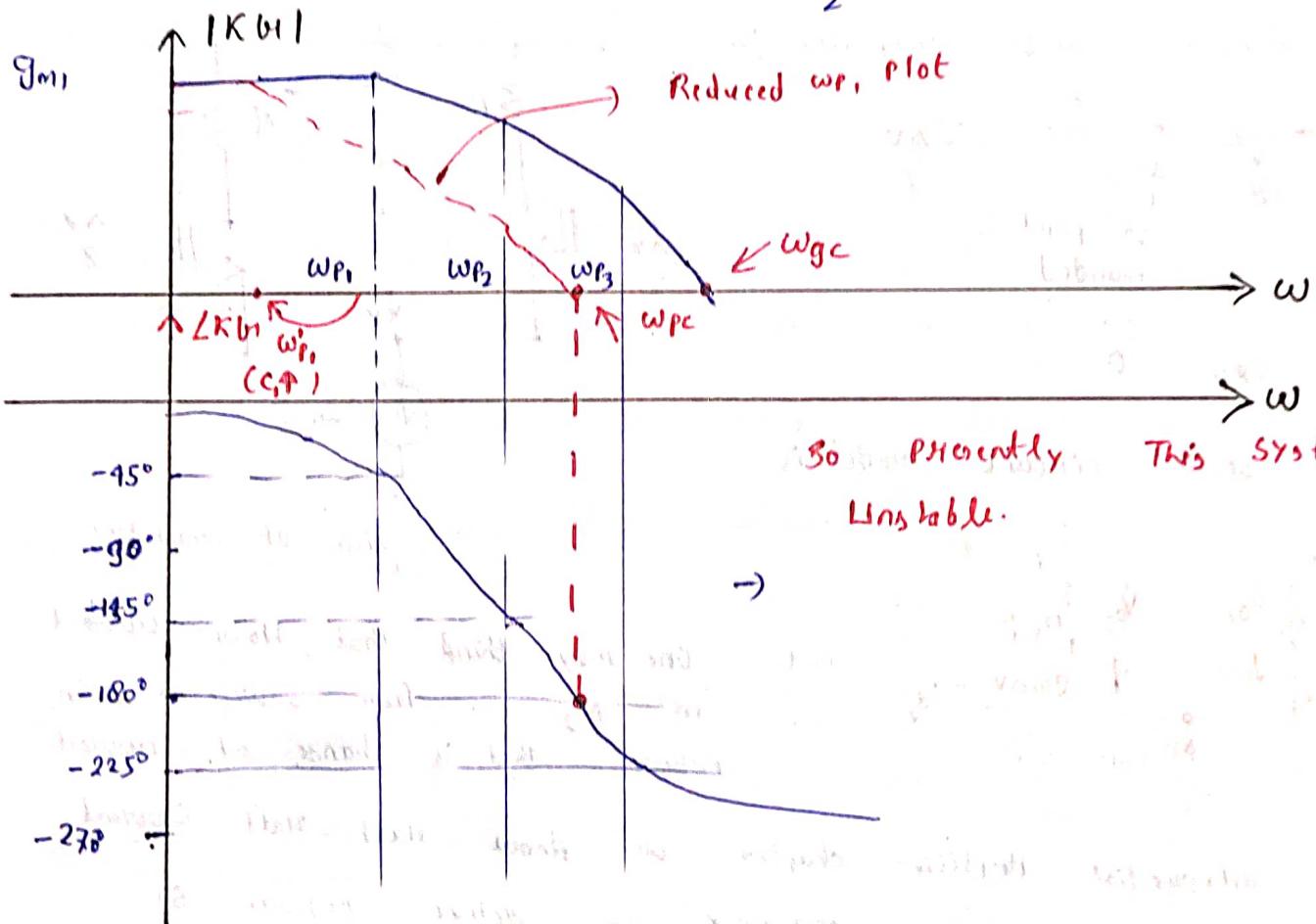
\rightarrow taking a 3-pole system to illustrate.



Open loop pole are

$$\omega_{p1} = \frac{-1}{R_1 C_1}; \quad \omega_{p2} = \frac{-1}{R_2 C_2}; \quad \omega_{p3} = \frac{-1}{R_3 C_3}$$

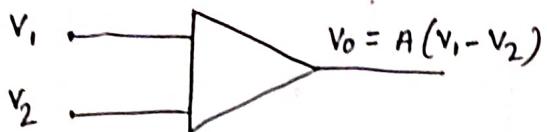
For analysis take $\omega_{p3} > 10\omega_{p2}$ & $\omega_{p2} > 10\omega_{p1}$



- If we move first (smallest) pole toward origin then w_{gc} reduced but w_{pc} very less effected. so by increasing C_1 we can stabilize it.
- Or if we reduce K , then K have no phase so it only reduces w_{gc} . And will Increase Stability.

Unit 6 : Op-Amp Design

How we express differential voltages:



Where,

$$V_1 = \frac{V_1 + V_2}{2} + \frac{V_1 - V_2}{2}$$

$$V_1 = V_{cm} + V_{dm}$$

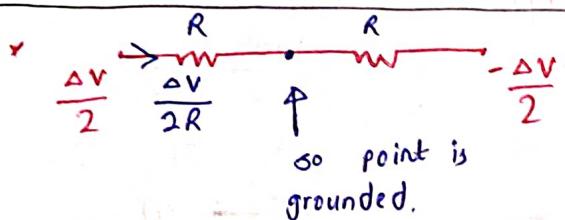
$$\text{and } V_2 = \frac{V_1 + V_2}{2} - \frac{V_1 - V_2}{2} = V_{cm} - V_{dm}$$

So, V_{cm} = Average voltage

$$\text{and } V_{dm} = \frac{1}{2} \times \text{difference voltage} = \frac{1}{2} \times \Delta V$$

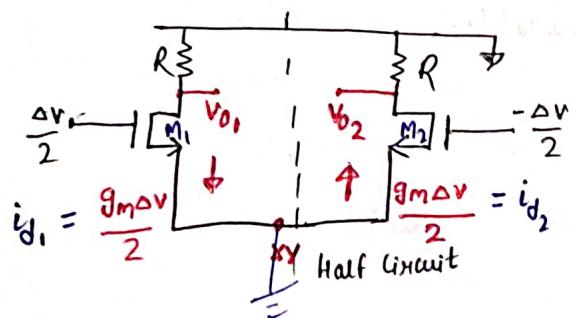
→ Now we will observe, how differential pair respond to common mode and differential mode voltages.

1) Differential mode response :-



$$\text{So } V_{xy} = 0$$

Hence small circuit model is:



Note: One may think that, how current in M_2 is from source to drain. Actually that is change of current.

In differential Amplifier chapter we know Half-Half current

of $2I_0$ is biasing MOSFET in active region. So

This is just change of current.

$$\text{and } V_{01} = -g_m R \left(\frac{\Delta V}{2} \right)$$

$$V_{02} = -g_m R \left(-\frac{\Delta V}{2} \right)$$

$$\left. \begin{aligned} \Delta V_{01} - V_{02} &= -g_m R \left(\frac{\Delta V + \Delta V}{2} \right) \\ \Delta V_{01} - V_{02} &= -g_m R \cdot \Delta V \end{aligned} \right\}$$

$$\text{Differential mode gain (A}_{\text{dm}}) = \frac{\Delta V_{\text{o1}} - \Delta V_{\text{o2}}}{\Delta V} = -g_{\text{m}} R$$

2) Response to Common mode voltage:

Now $V_{\text{in1}} = V_{\text{cm}}$, $V_{\text{in2}} = V_{\text{cm}}$ so $\Delta V_{\text{o1}} = \Delta V_{\text{o2}}$ is equally divided in both side and $\Delta V_{\text{o1}} = \Delta V_{\text{o2}}$

$$\text{so } \Delta V_{\text{o1}} - \Delta V_{\text{o2}} = 0$$

$$A_{\text{cm}} \Rightarrow 0$$

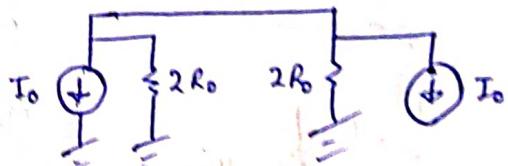
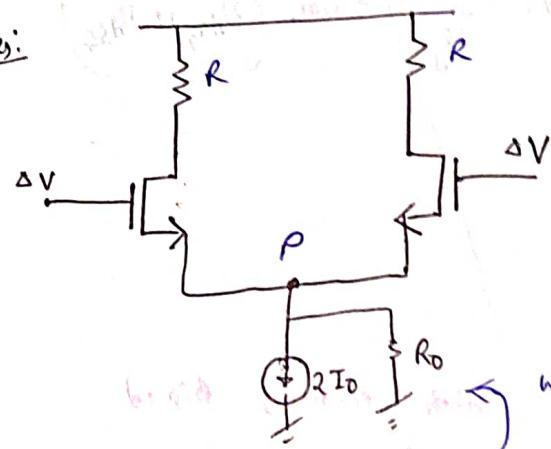
If we see change in them then $\Delta I_{\text{d1}} = \Delta I_{\text{d2}} = 0$ and $\Delta V_{\text{o1}} = \Delta V_{\text{o2}} = 0$

$$\text{CMRR} = \left| \frac{A_{\text{dm}}}{A_{\text{cm}}} \right| ; \text{ Ideally it should be } \infty \text{ OR } A_{\text{cm}} = 0$$

Common mode Rejection Ratio.

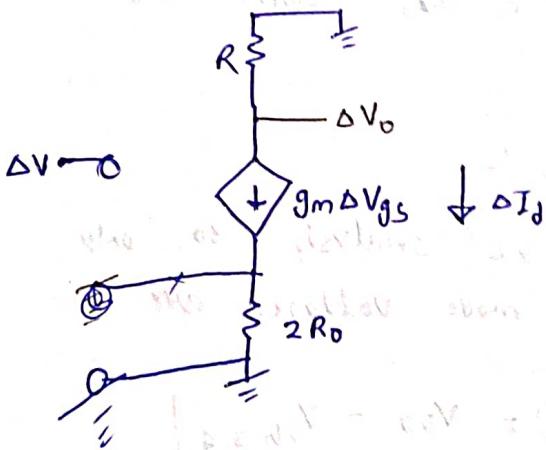
Let us take a practical

case: 1) To find A_{cm}. Break Current source as:



Now we got a symmetry

And Half circuit form A_{cm} calculation is:



$$\text{From K.V.L: } \Delta V = \Delta V_{\text{ds}} + \Delta I_d (2R_o)$$

$$\Delta V = \frac{\Delta I_d}{g_m} + \Delta I_d (2R_o)$$

$$\Delta V = \left(\frac{1 + 2g_m R_o}{g_m} \right) \Delta I_d$$

$$\Rightarrow \Delta I_d = \frac{g_m}{1 + 2g_m R_o} \Delta V$$

$$\text{and } \Delta V_o = -\Delta I_d R$$

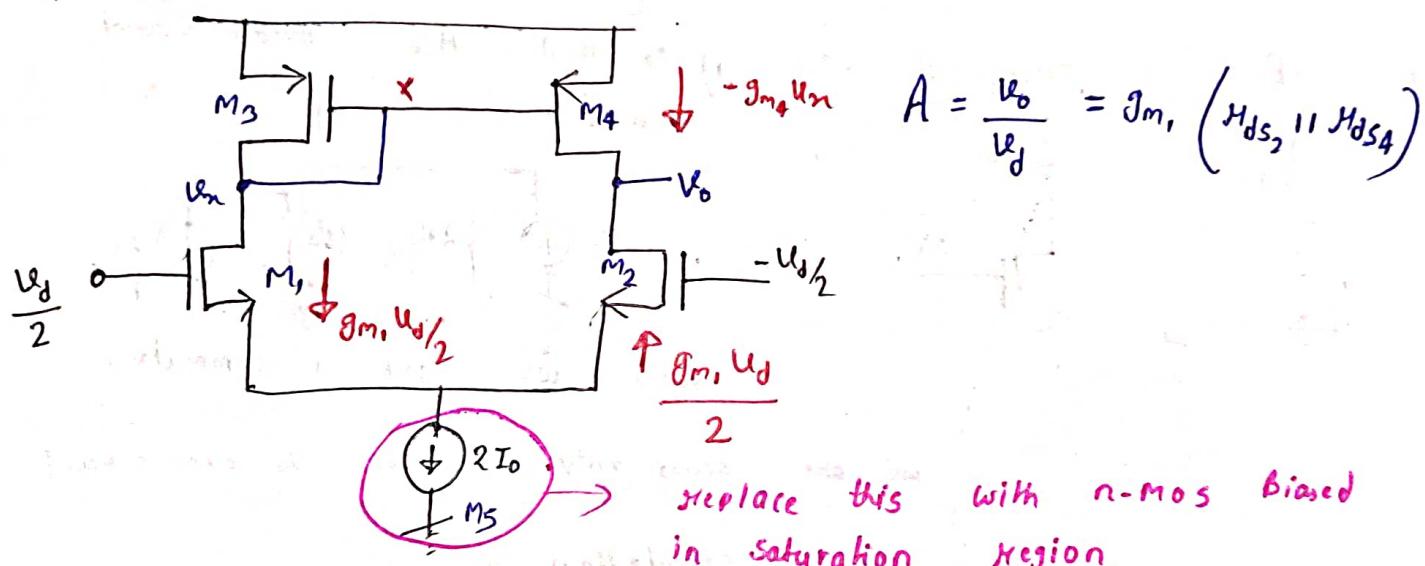
$$\Delta V_o = \left(\frac{-g_m R}{1 + 2g_m R_o} \right) \Delta V$$

$$\Rightarrow A_{CM} = \frac{\Delta V_o}{\Delta V} = \frac{-g_m R}{1 + 2g_m R_0}$$

(ii) A_{DM} calculation:- For this P point will be grounded and we have symmetrical circuit. Since P point shorted for small signal (change) analysis so no use of R_0 and $A_{DM} = -g_m R$

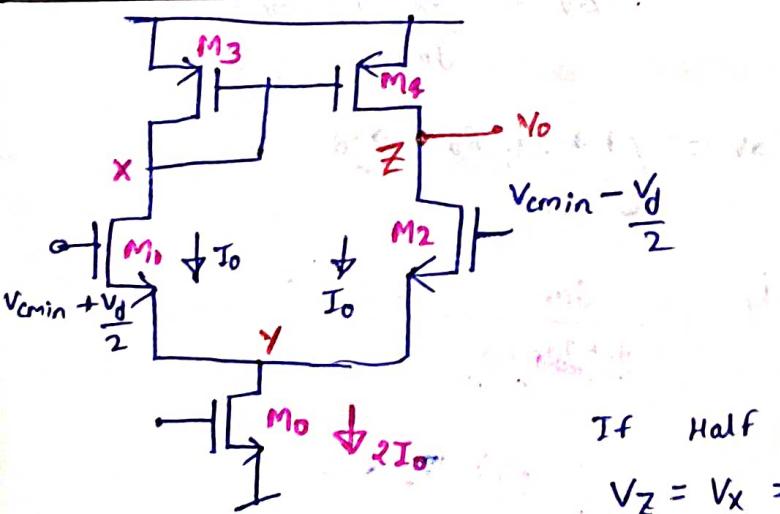
and $CMRR = \left| \frac{A_{DM}}{A_{CM}} \right| = 1 + 2g_m R_0$

One - Stage Op-amp :- We want single ended o/p with no reduction in gain. so differential pair with active load (studied earlier) works as one-stage op-amp.



choose $V_{BS} \approx \left(\frac{W}{L}\right)_5$ such that we set $2I_o$ current and H_{DS5} High.

DC analysis of one stage OP-Amp :-



since, D.C analysis so only common mode voltages are effective.

$$V_x(DC) = V_{DD} - V_{BS3,4} | I_o$$

$$V_y(DC) = V_{Cmin} - V_{BS1,2} | I_o$$

If Half circuits are matched (symmetric)
 $V_Z = V_X = V_{DD} - V_{BS}(3,4) | I_o$

Two terminologies: $V_{cm,in}$: Input common mode voltage } we want
 $V_{o,cm}$: output common mode voltage. } Accepted
 range of
 those voltages so that our circuit works fine.

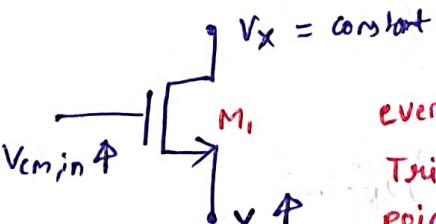
1) Decrease $V_{cm,in}$: As long as M_0 is in saturation, I_{D0} will not change so much. Hence threshold point is when it starts to go in triode region.

$$V_y = V_{cm,in} - V_{BIS,1,2} \Big|_{I_0}$$

so $\min(V_{cm,in})$ = when M_0 is at edge of triode region and at that point $V_y = V_{B_0} - V_{T_0} = V_{DSAT_0} \Big|_{2I_0}$

$$\begin{aligned} \text{so, } \min(V_{cm,in}) &= V_{y_{min}} + V_{BIS,1,2} \\ &= V_{DSAT_0} \Big|_{2I_0} + V_{BIS,1,2} \Big|_{I_0} \end{aligned} \quad \begin{matrix} \leftarrow \text{calculated at Bias} \\ \text{current } I_0. \end{matrix}$$

2) Increase $V_{cm,in}$: \rightarrow Now M_0 will remain in saturation because $V_y \uparrow$ so no problem here.

\rightarrow Drain voltage of M_1 (V_x) = $V_{DD} - V_{BIS,3,4} \Big|_{I_0}$ [since $V_{cm,in} \uparrow$ and I_{D0} constant so V_x is also constant because M_0 maintaining $2I_0$ current]
 \rightarrow  $V_x = \text{constant}$
 $V_{cm,in} \uparrow$ eventually it will go in triode and that point is $\max(V_{cm,in})$.

$$\begin{aligned} \max(V_{cm,in}) &= V_x + V_{T_1} \quad \{ \text{when bias voltage is exactly } V_{Th}, \text{ above drain} \} \\ &= V_{DD} - V_{BIS,3,4} + V_{T_1} \end{aligned}$$

so Input common mode range (ICMR) is:

$$\text{Range } V_{cm,in} = \left(V_{DSAT_0} \Big|_{2I_0} + V_{BIS,1,2} \Big|_{I_0}, V_{DD} - V_{BIS,3,4} + V_{T_1} \right)$$

3) Increase $V_{o,cm}$: \rightarrow when it is increased M_4 is at edge of triode region.

$$\max(V_{cm,out}) = V_{DD} - V_{SDSAT_4}$$

{ bias of M_4 : V_x
 Drain can go one threshold voltage above the gate because its PMOS}

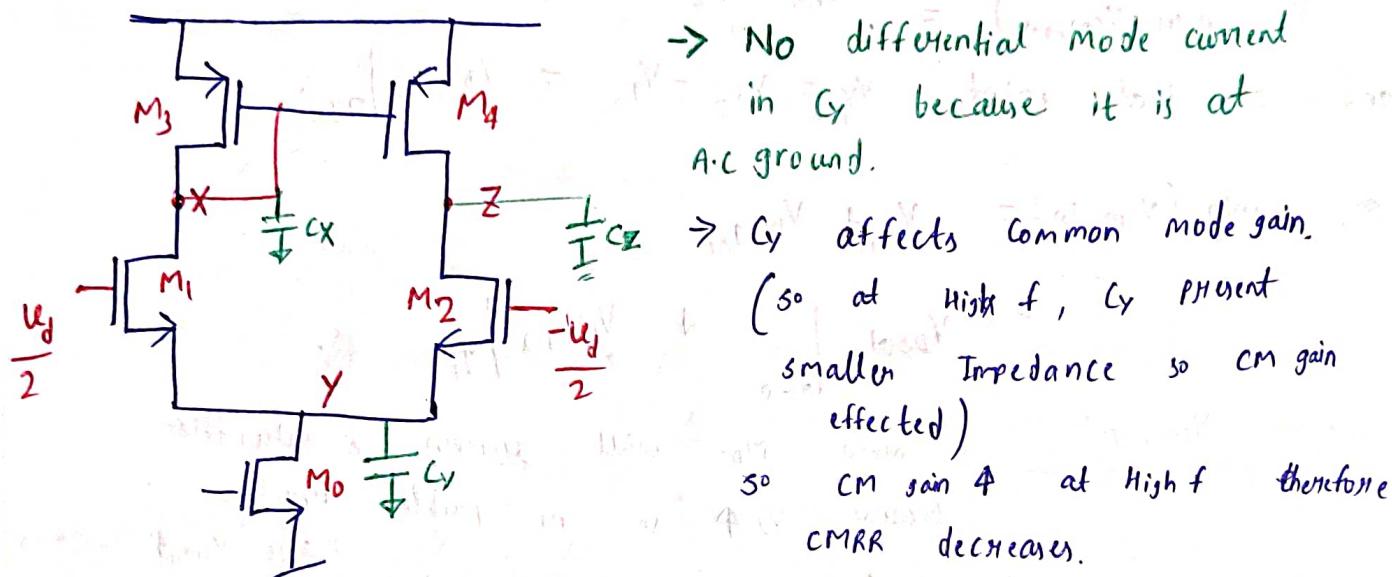
4) Decrease V_0, cm \rightarrow Gate of M_2 is held at $V_{\text{cm,in}}$
 $\Rightarrow M_2$ will go to edge of Triode.

$$\min(V_{\text{cm,out}}) = \text{drain of } M_2 \text{ going one threshold below gate.}$$

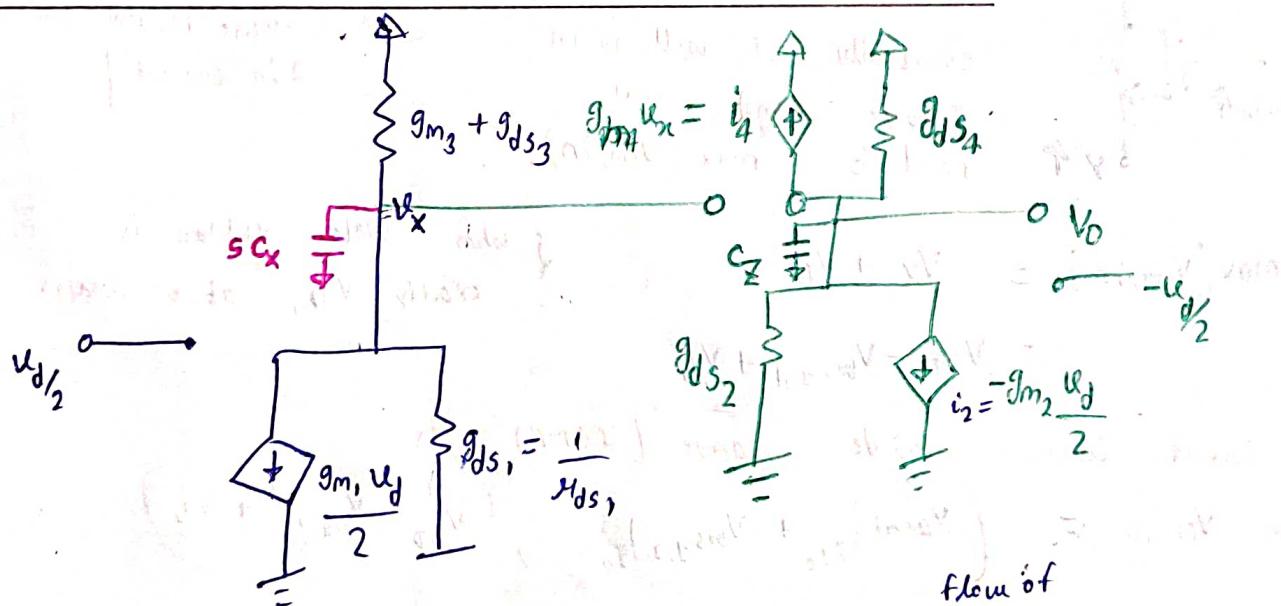
$$= V_{\text{cm,in}} - V_{T_2}$$

So output common mode range (CMRR) is:
 $(\min(V_0, \text{cm}), \max(V_0, \text{cm}))$

Frequency Response of One-Stage Op-Amp :-



small signal model considering Impedances (Admittances) :-



\rightarrow So we can see v_o is created by i_2 & i_4 current created by three admittance connected at node -Z.

$$V_o = \frac{-(i_2 + i_4)}{g_{ds_2} + g_{ds_4} + sC_Z} \quad \text{where } i_2(s) = -\frac{g_{m_2} U_d}{2}$$

$$i_4(s) = g_{m_4} U_d$$

and $V_x(s) = -g_{m_1} \frac{U_d}{2} \left(\frac{1}{g_{m_3} + g_{ds_3} + g_{ds_1} + s(C_x)} \right)$

$$\approx \frac{-g_{m_1} U_d}{g_{m_3} + sC_x} \quad \because g_{m_3} \gg g_{ds_3} = g_{ds_1}$$

so, $i_4(s) = \frac{-g_{m_1} U_d / 2}{1 + \frac{sC_x}{g_{m_3}}} \cdot \frac{g_{m_4}}{g_{m_3}} \quad \because g_{m_3} \approx g_{m_4}$

$$i_4(s) = \frac{-g_{m_1} U_d / 2}{1 + \frac{sC_x}{g_{m_3}}} \quad \text{and} \quad V_o = \frac{-(i_2 + i_4)}{g_{ds_2} + g_{ds_4} + sC_x}$$

$$\Rightarrow V_o(s) = \frac{g_{m_1} U_d}{2} \cdot \frac{1}{g_{ds_2} + g_{ds_4} + sC_Z} \left[1 + \frac{1}{1 + \frac{sC_x}{g_{m_3}}} \right] \quad \because g_{m_1} = g_{m_2}$$

$$\Rightarrow V_o(s) = \frac{g_{m_1} U_d}{2} \left[\frac{2 + \frac{sC_x}{g_{m_3}}}{\left[1 + \frac{sC_x}{g_{m_3}} \right] \left[g_{ds_2} + g_{ds_4} + sC_Z \right]} \right]$$

$$\Rightarrow \frac{V_o}{U_d} = \left(\frac{\frac{g_{m_1}}{g_{ds_2} + g_{ds_4}}}{1 + \frac{sC_x}{g_{m_3}}} \right) \left(\frac{1 + \frac{sC_x}{2g_{m_3}}}{\left[1 + \frac{sC_x}{g_{m_3}} \right] \left[1 + \frac{sC_Z}{g_{ds_2} + g_{ds_4}} \right]} \right)$$

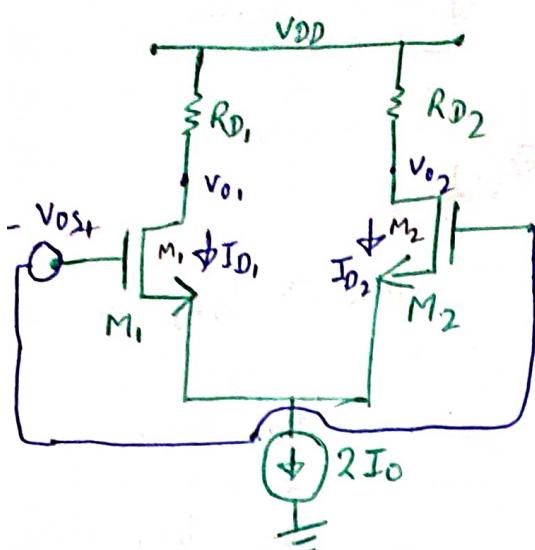
low-f gain

\Rightarrow 2 poles, 1 zero

$\omega_{p1} = \frac{1}{M_{out} R_C}$ where $M_{out} = g_{ds_2} / g_{ds_4}$ $\omega_{p1} = \frac{g_{ds_2} + g_{ds_4}}{C_Z}$ $\omega_{p2} = \frac{C_Z}{g_{m_3} / C_X} = \frac{1}{M_{out} C_X}$ $\omega_Z = \frac{2g_{m_3}}{C_X}$ \rightarrow smallest pole (dominant pole)

same logic as Razavi

Differential Amplifier offset :- When mismatches exist in Transistors we need to apply same offset voltage at input side such that $V_{OS, out} = 0$.



- * Mis-matches in: V_T , $\frac{W}{L}$ and R_D .
- * Mis-matches are small.
- * $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 ; \left(\frac{W}{L}\right)_2 = \frac{W}{L} + \Delta \frac{W}{L}$
- * $V_{T_1} = V_T ; V_{T_2} = V_T + \Delta V_T$
- * $R_{D_1} = R_D ; R_{D_2} = R_D + \Delta R_D$

and for this case $V_{OS, out} = V_{01} - V_{02} = 0$

$$V_{DD} - I_D R_{D_1} = V_{DD} - I_{D_2} R_{D_2}$$

$$\Rightarrow I_{D_1} R_{D_1} = I_{D_2} R_{D_2}$$

$$\text{and } V_{OS} = V_{BS_1} - V_{BS_2}$$

$$V_{OS} = \left[\sqrt{\frac{2 I_{D_1}}{\mu_n C_{ox} \frac{W}{L}}} + V_{T_1} \right] - \left[\sqrt{\frac{2 I_{D_2}}{\mu_n C_{ox} \left(\frac{W}{L} + \Delta \frac{W}{L} \right)}} + V_{T_1} + \Delta V_T \right]$$

$$\Rightarrow V_{OS} = \sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2 (I_D + \Delta I_D)}{\mu_n C_{ox} \left(\frac{W}{L} + \Delta \frac{W}{L} \right)}} + \Delta V_T$$

$$\Rightarrow V_{OS} = \sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}} \left[1 - \sqrt{\frac{1 + \frac{\Delta I_D}{I_D}}{1 + \frac{\Delta W/L}{W/L}}} \right] + \Delta V_T$$

$(V_{BS} - V_T)_{\text{nominal overdrive}}$

$$\frac{\Delta I_D}{I_D} \ll 1$$

$V_{D, \text{sat}}$

$$\Rightarrow V_{OS} = (V_{BS} - V_T) \left[1 - \left(1 + \frac{\Delta I_D}{2 I_D} \right) \left(1 - \frac{\Delta W/L}{2 W/L} \right) \right] + \Delta V_T$$

and $\frac{\Delta W/L}{W/L} \ll 1$

Now neglect product of 2Δ terms which is $\frac{\Delta I_D \Delta w_L}{I_D (w_L)}$

so,

$$V_{OS} = V_{BS} - V_T \left[\frac{\Delta I_D}{I_D} - \frac{\Delta w_L}{2w_L} \right] + \Delta V_T$$

For $V_{OS, out} = 0$, $I_{D1} R_{D1} = I_{D2} R_{D2}$

$$\Rightarrow I_D R_D = (I_D + \Delta I_D)(R_D + \Delta R_D)$$

$$\Rightarrow 0 = \Delta I_D R_D + \Delta R_D I_D + \Delta I_D \Delta R_D \rightarrow \text{neglect}$$

$$\Rightarrow \frac{\Delta I_D}{I_D} = -\frac{\Delta R_D}{R_D} \rightarrow \text{Because it is fundamental mismatch parameter}$$

so $V_{OS,in} = \frac{V_{BS} - V_T}{2} \left[-\frac{\Delta R_D}{R_D} - \frac{\Delta w_L}{w_L} \right] + \Delta V_T$

* -ve signs do not matter: mis-match in R_D , w_L & V_T are independent

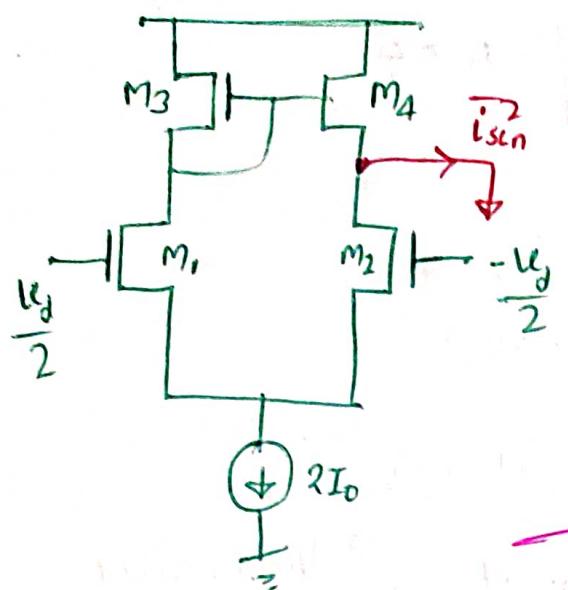
so we actually take interest in standard deviation of offset.

* Mis-match in V_T appears directly at input. and that's why it is dominant term

* Standard deviation in $V_{OS,in}$ is

$$\sigma_{OS,in}^2 = \left(\frac{V_{BS} - V_T}{2} \right)^2 \left[\frac{\sigma_{\Delta R_D}^2}{R_D^2} - \frac{\sigma_{\Delta w_L}^2}{w_L^2} \right] + \sigma_{V_T}^2$$

One - Stage Op-Amp Noise :-



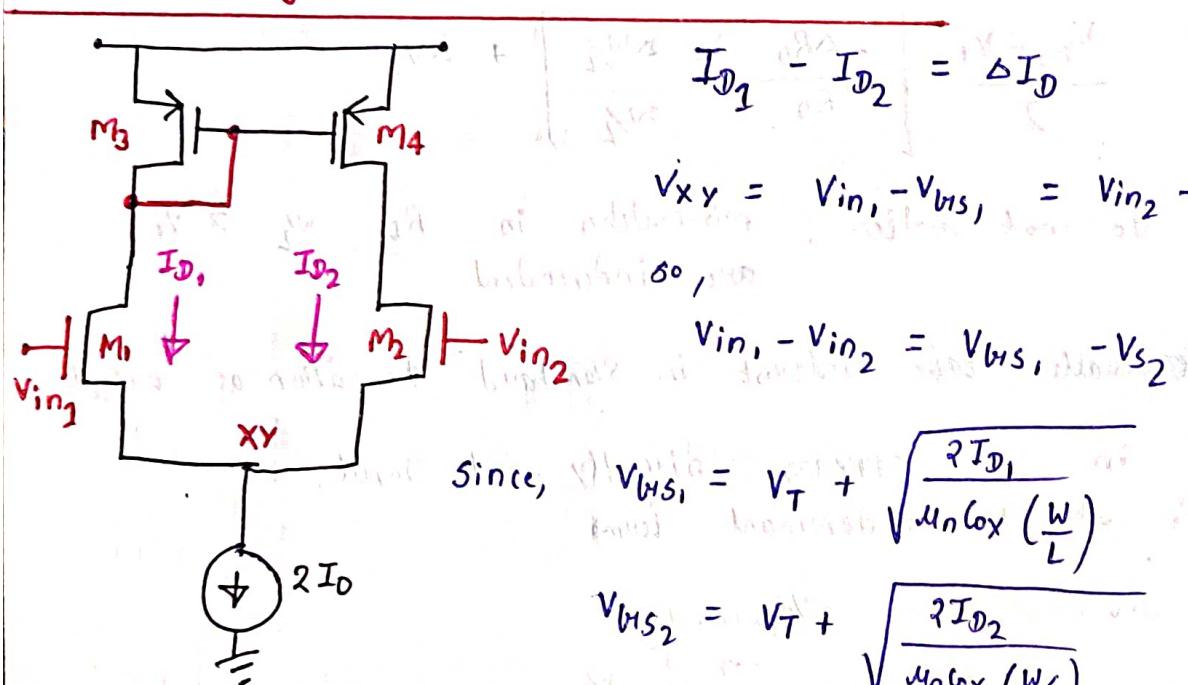
Noise: short circuit, output to ground.

and, $\frac{i_{son}^2}{b_{m2}} = \overline{e_n^2} = \text{Input-referred noise voltage of Op-Amp.}$

$$\text{and, } \overline{i_{son}^2} = \overline{i_{n1out}^2} + \overline{i_{n2out}^2} + \overline{i_{n3out}^2} + \overline{i_{n4out}^2}$$

Later

One - Stage Op-Amp Slew Rate :-



$$I_{D1} - I_{D2} = \Delta I_D$$

$$V_{XY} = V_{in1} - V_{BS1} = V_{in2} - V_{BS2}$$

$$V_{in1} - V_{in2} = V_{BS1} - V_{S2}$$

Since, $V_{BS1} = V_T + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} (\frac{W}{L})}}$

$$V_{BS2} = V_T + \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} (\frac{W}{L})}}$$

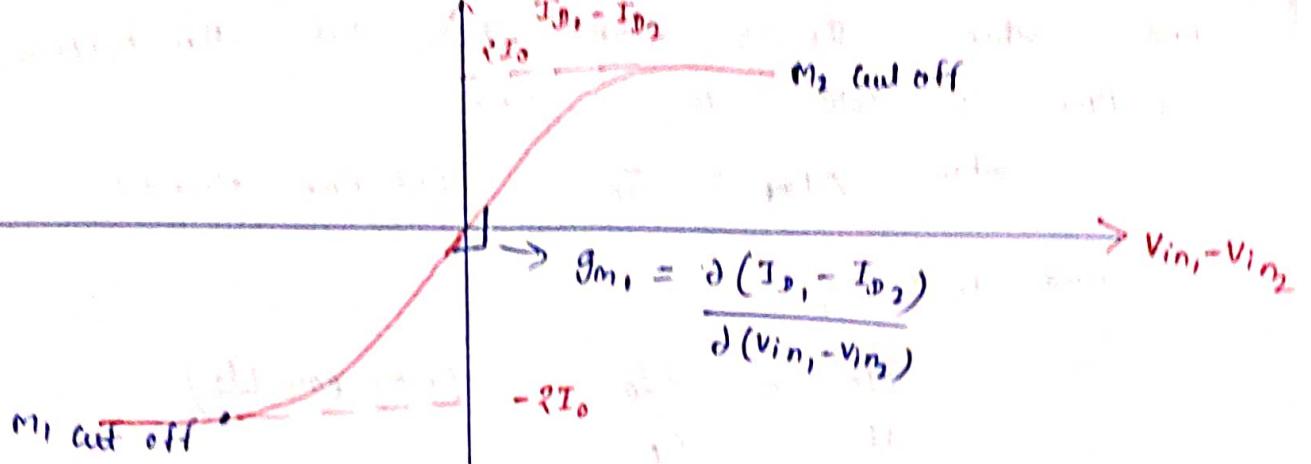
$$\text{So, } V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} (\frac{W}{L})}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} (\frac{W}{L})}}$$

$$\text{We know: } I_{D1} + I_{D2} = 2I_0$$

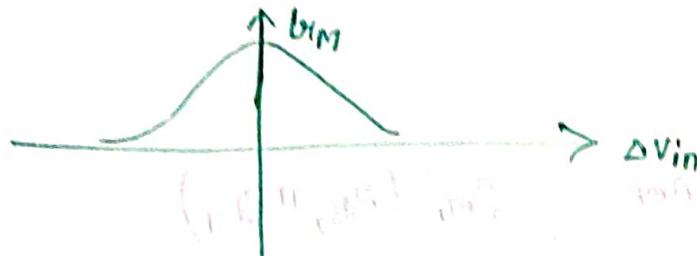
After solving we get

$$I_{D1} - I_{D2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{in1} - V_{in2}) \sqrt{\frac{8I_0}{\mu_n C_{ox} (\frac{W}{L})}} - (V_{in1} - V_{in2})^2$$

- * if $|V_{in1} - V_{in2}|$ is large one transistor goes out of saturation and all the current $2I_0$ flows from another one.

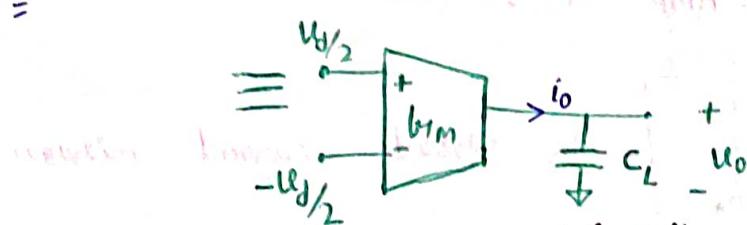
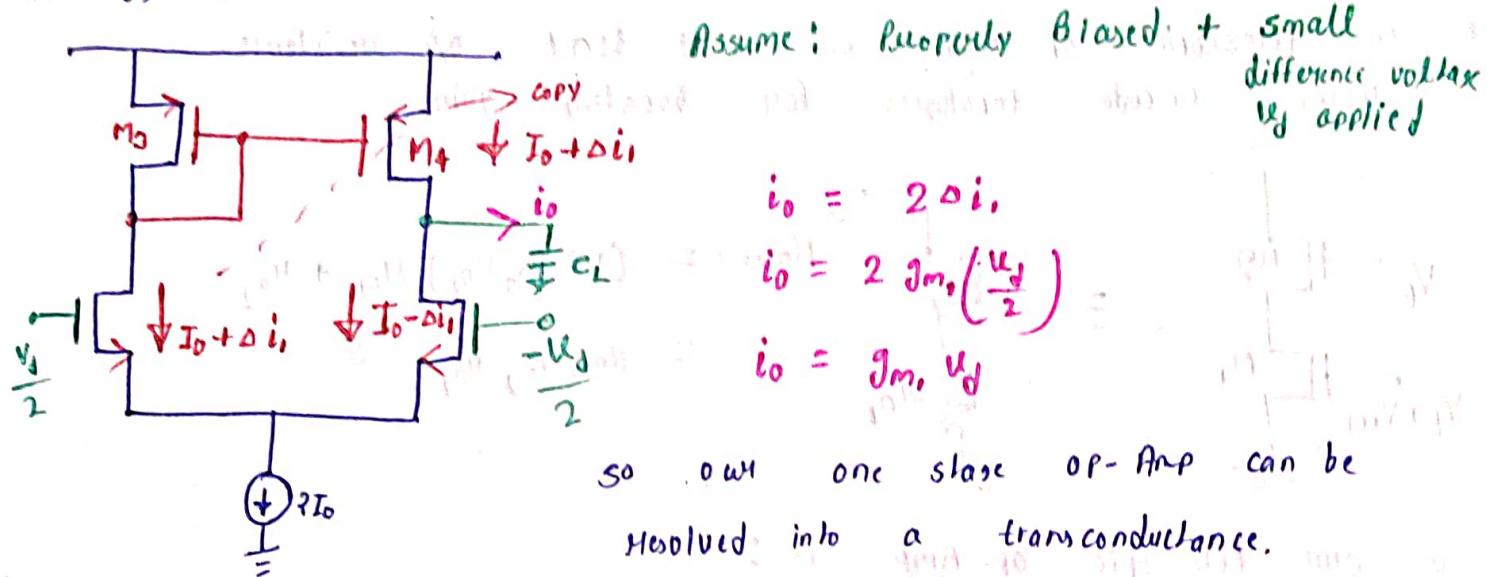


If we flat braph for Trans-Conductance:



Op-Amp: $R_{out} \approx 0$
while in our one stage op-Amp it is large.

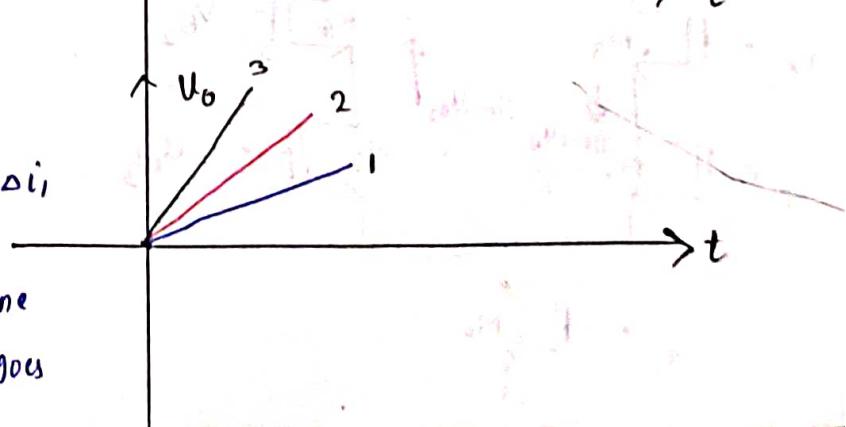
Let us drive a capacitive load using the own one stage op-Amp



Now $C_L \frac{dU_o}{dt} = i_o$

$$\frac{dU_o}{dt} = \frac{g_m U_d}{C_L}$$

As we keep Increase U_d , αi_s increases such all the current start passing through one side and other side MOS goes cut-off



And when V_d is such high that this happens
Op-Amp is said to be slewed.

when $\Delta i_{\text{eq}} = I_o$ (Op-Amp slewed)

and $i_o = 2I_o$

$$\text{so } \frac{dV_o}{dt} = \frac{2I_o}{C_L} \quad (\text{max possible})$$

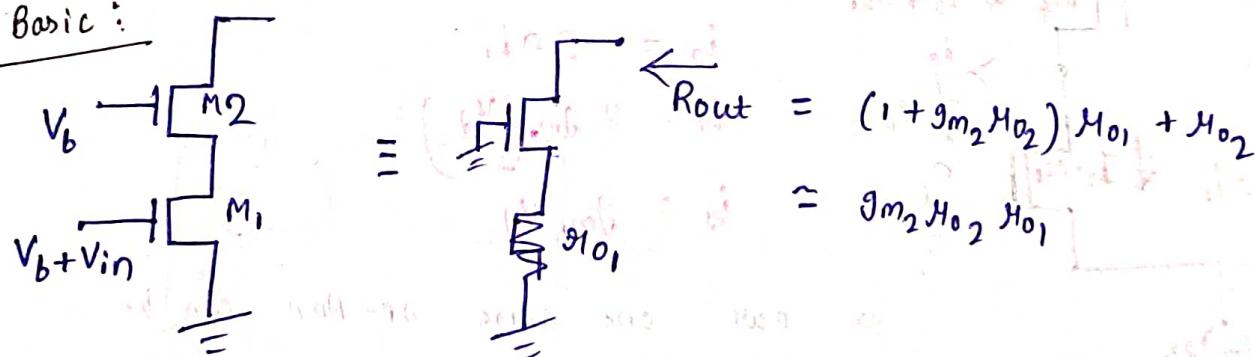
Slew rate: Max rate of charge/discharge of load capacitor

Telescopic Op-Amp :-

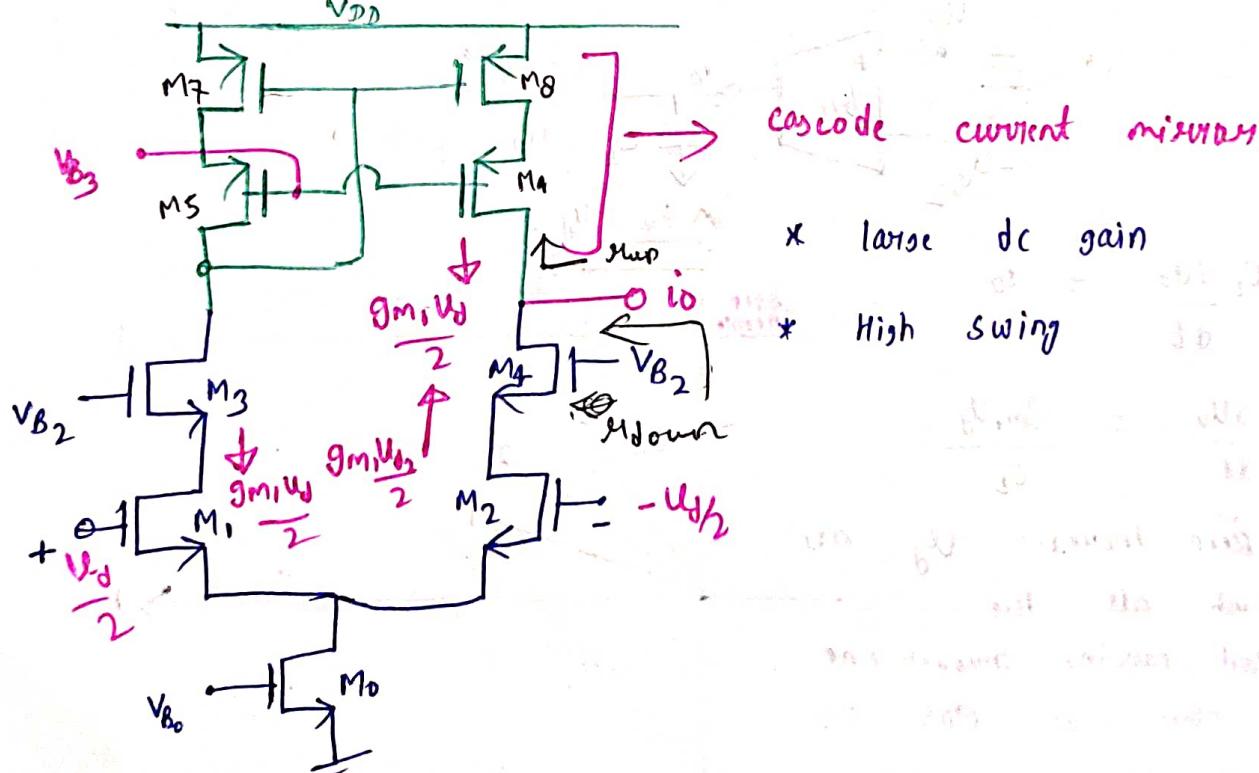
DC gain of one-stage OP-Amp = $g_m (M_{ds_2} || M_{ds_4})$

- * We want more dc gain.
- * In telescopic op-amp we will boost o/p resistance using cascode topologies for boosting gain.

Basic:



so our telescopic op-amp is :



Let us apply a differential signal and assume each MOS - Biased properly.

$$\text{so, } i_o = i_{d6} + i_{d4} = g_m u_d$$

$$\text{and } u_o = i_{\text{out}} M_{\text{out}}$$

$$u_o = g_m u_d M_{\text{out}}$$

$$A_d \Rightarrow \frac{u_o}{u_d} = g_m M_{\text{out}}$$

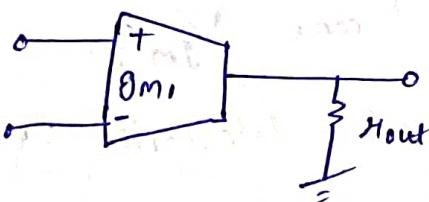
$$M_{\text{out}} = M_{\text{up}} // M_{\text{down}}$$

$$M_{\text{down}} = M_{p\text{-cascode}} // M_{n\text{cascode}}$$

$$M_{\text{out}} \approx g_{m_4} M_{ds_4} M_{ds_2} // g_{m_6} M_{ds_6} M_{ds_8}$$

$$\text{so: } A_d = g_m \left[g_{m_4} g_{m_6} M_{ds_2} M_{ds_4} M_{ds_6} M_{ds_8} \right]$$

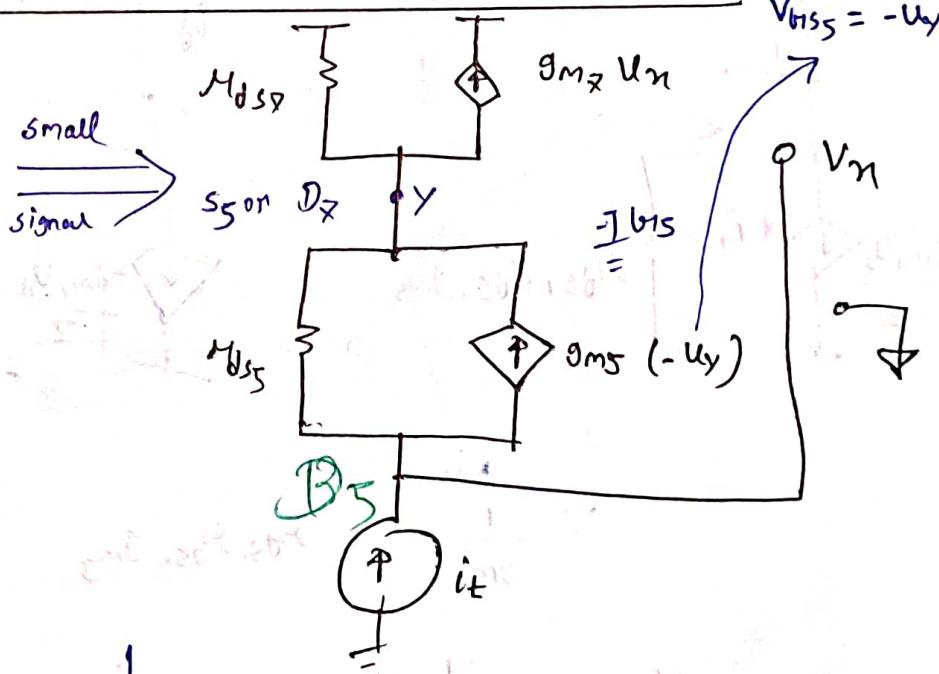
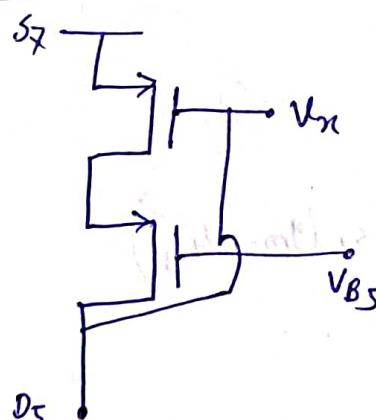
We can represent this op-Amp as operational Trans-conductance Amplifier:



Telescopic has same g_m as original one stage op-Amp.

$2 C_L \Rightarrow$ pole at output node

Calculation of I/p resistance looking at drain of M_5 :



K.C.L at D_7

$$i_t = g_{m_7} u_n + \frac{u_y}{M_{ds_7}}$$

$$i_t = g_{m_7} u_n + g_{ds_7} u_y$$

$$\Rightarrow u_y = \frac{i_t - g_{m_7} u_n}{M_{ds_7}}$$

K.C.L at D_5 :

$$i_t = \frac{u_n - u_y}{M_{ds_5}} + (-g_{m_5} u_y)$$

$$i_t = g_{ds5} u_n - (g_{m5} + g_{ds5}) u_y$$

$$i_t = g_{ds5} u_n - (g_{m5} + g_{ds5}) \left(\frac{i_t - g_{m2} u_n}{g_{ds2}} \right)$$

$$\Rightarrow g_{ds2} i_t = g_{ds5} g_{ds2} u_n + (g_{m5} + g_{ds5}) g_{m2} \cdot u_n - (g_{m5} + g_{ds5}) i_t$$

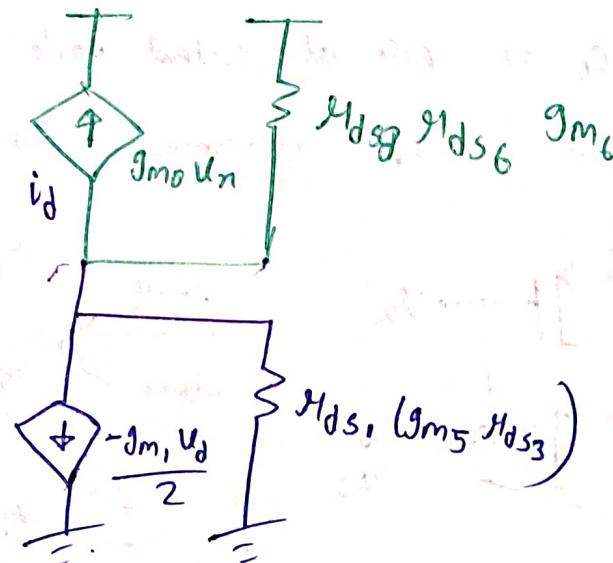
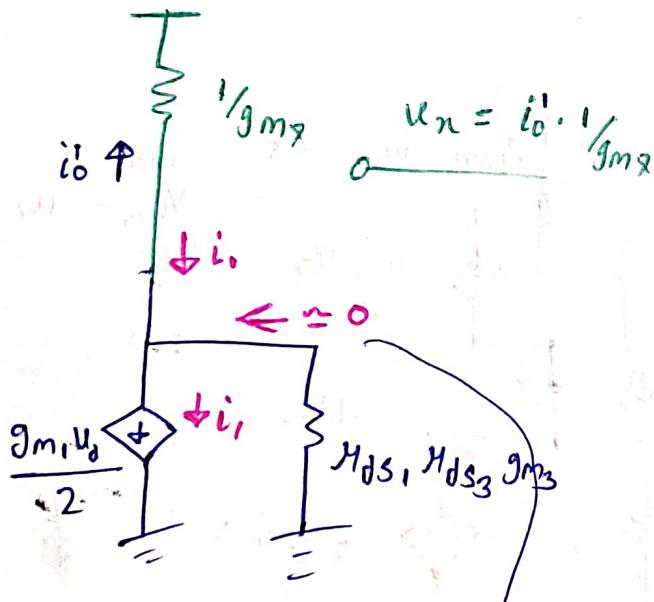
$$\Rightarrow i_t [g_{m5} + g_{ds5} + g_{ds2}] = u_n [g_{m5} g_{m2} + g_{m2} g_{ds5} + g_{ds5} g_{ds2}]$$

all $g_{m5} \gg g_{ds5}$

$$i_t g_{m5} \approx u_n \cdot g_{m5} g_{m2}$$

$$\text{Min } \Rightarrow \frac{u_n}{i_t} = \frac{1}{g_{m2}} \quad \left\{ \begin{array}{l} \text{even if for cascode it} \\ \text{came } 1/g_m \end{array} \right.$$

Hence small signal picture of telescopic cascode is:



$$\therefore \frac{1}{g_{m2}} \ll H_{ds1}, H_{ds3}, j_{m3}$$

$$\text{So } u_n = \frac{i_0'}{j_{m2}} = \frac{-i_1}{j_{m2}} = \frac{-j_{m1} u_d}{2 j_{m2}}$$

$$i_\delta = \frac{g_{m_1} u_d}{2 g_{m_2}} = \frac{-g_{m_1} u_d}{2 g_{m_2}} \cdot g_{m_2}$$

since $g_{m_2} \approx g_{m_1}$

$$i_d = \frac{-g_{m_1} u_d}{2}$$

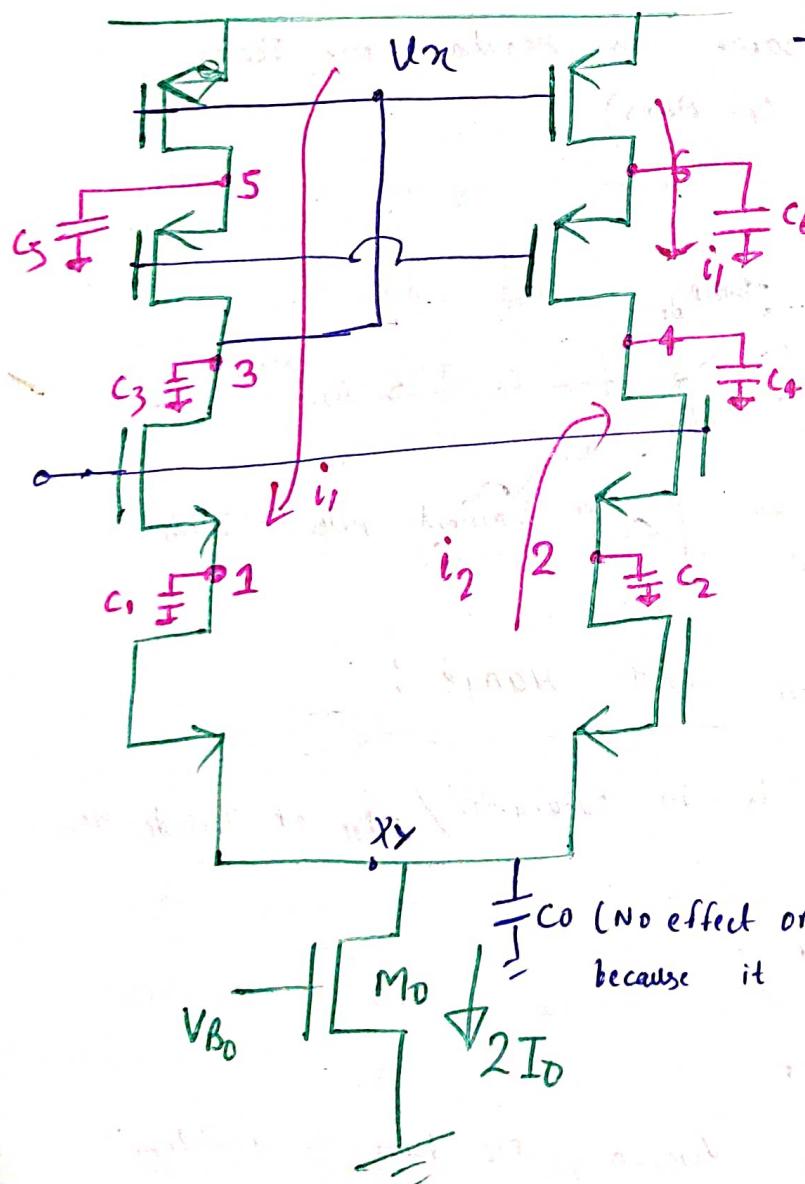
so Total o/p current (i_o) = from M_1 & M_2

$$i_o = \frac{g_{m_1} u_d}{2} + \frac{g_{m_1} u_d}{2}$$

$$i_o = g_{m_1} u_d$$

so In this way we actually get i_o & $u_o = i_o R_{out}$

Frequency Response of Telescopic Op-Amp :-



C_4 at o/p node include load and parasitic capacitance.

Telescopic Op-Amp is expected to have 6 poles in $\frac{u_o}{u_d}$.

There are zeros because i_1 & i_2 take different paths to output node.

* These paths have different phase shifts (freq-dependent)

C_0 (No effect on DM response because it is Acond)

* More than one zero possible because there are multiple caps in those paths.

$\Rightarrow C_3$ can be large because it includes C_{GS7} and C_{GS8} .
 (Mixture pole) $\approx \frac{g_m}{C_3}$

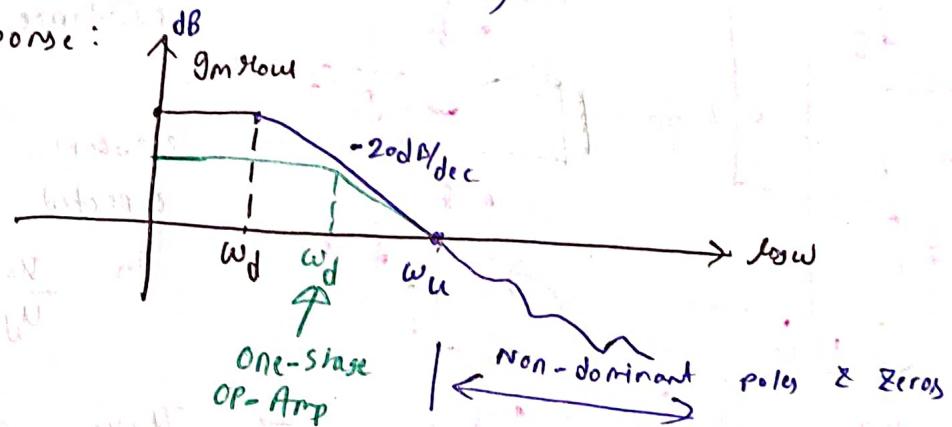
Therefore dominant pole (ω_d) = $\frac{1}{H_{out} C_A} \approx \frac{1}{H_{out} C_L}$

5. $\frac{U_o(s)}{U_d} = \underbrace{\frac{g_m H_{out}}{C_L}}_{dc gain} \times \underbrace{\frac{1}{1 + s C_A H_{out}}} \times \frac{(\) (\)}{(\) (\)}$

\Rightarrow Assuming undesired poles/zeros are much away from unity gain frequency, unity gain freq is:

$\omega_u \approx \frac{g_m}{C_L}$ (same as regular one stage OP-Amps)

\Rightarrow Magnitude Response:



Input & Output Common mode Range:

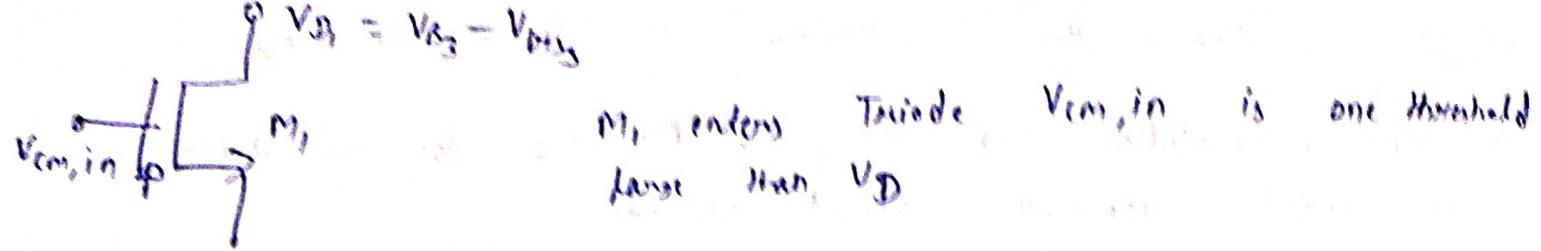
1) $V_{cm,in}(\min) =$ Until M_0 is in saturation/edge of Triode region

$$= V_{xy} + V_{BIS_1}$$

\downarrow at Triode edge

$$= V_{Osat_0} + V_{BIS_1}$$

2) $V_{cm,in}(\max) \Rightarrow$ V_{xy} follows $V_{cm,in}$, M_0 have no problem because its saturation Increasing. V_{BIS_1} & V_{BIS_2} stay constant



M_1 renders Triode, $V_{cm,in}$ is one threshold large than V_D

$$V_{cm,in}(max) = V_{D1} + V_{T1}$$

$$= V_{B3} - V_{DS3} + V_{T1}$$

3) output common mode range:

$\rightarrow V_{cm,out} \uparrow$ M_2 moves closer to Triode region as its gate have constant voltage

$$V_{cm,out}(max) = V_{B5} + V_{T6}$$

$\rightarrow V_{o,cm} \downarrow$, gate of M_2 is constant & M_2 moves closer to Triode so OCMR is smaller than that of one-stage op-amp.

$$V_{o,cm}(out) = V_{B3} - V_{T4}$$

Slew rate:- Apply $\Delta V_d / 2$ & $\frac{-\Delta V_d}{2}$ differential signal change at input.

$$\therefore \Delta I_d = \left(I_o + \frac{\Delta I_d}{2} \right) + \left(I_o - \frac{\Delta I_d}{2} \right) = \Delta I_d$$

and it charges load-cap.

$$\therefore I_C = C \cdot \frac{dV_o}{dt}$$

$$\Rightarrow \frac{dV_o}{dt} = \frac{\Delta I_d}{C} = \frac{I_m \cdot \Delta V_d}{C_L}$$

as we increase V_d current through M_1 & hence M_2 decreases eventually $2I_o$ current flows one side & other side cut-off.

$$\therefore \Delta I_{omax} = 2I_o$$

$$\text{Hence } \frac{dV_o}{dt} = \frac{2I_o}{C_L}$$

{if we increase V_d any further output will not respond to it)

so This is termed as slew rate

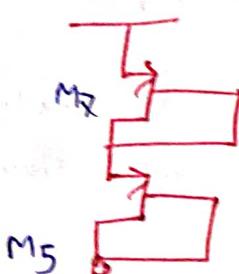
Offset: (only V_T mismatch in Telescopic Op-Amp)

- V_T mismatch of M_3, M_4, M_5, M_6 does not appear in input-referred offset voltage.
- V_T mismatch of $M_1 \& M_2$ appears directly at input.
- V_T mismatch $M_7 \& M_8$ is scaled by relative gms.

So, Input-referred offset voltage:

$$\sigma_{\text{os,in}}^2 = \sigma_{V_{T1,2}}^2 + \left(\frac{g_{m2}}{g_{m1}} \right)^2 \sigma_{V_{T7,8}}^2 \quad \left. \begin{array}{l} \text{Same as that} \\ \text{of 1-stage} \\ \text{Op-Amp} \end{array} \right\}$$

Note: If you want local-swing telescopic Op-Amp

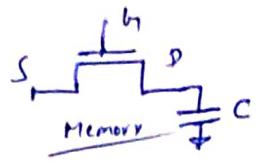


→ requires one bias voltage

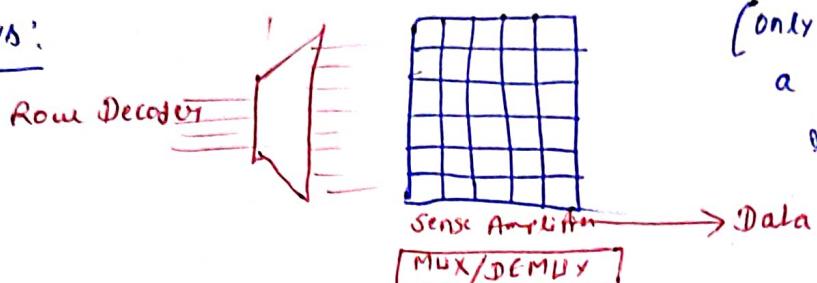
→ everything else is same

(Memory Hierarchy for DDR RAM)

DFI Specifications

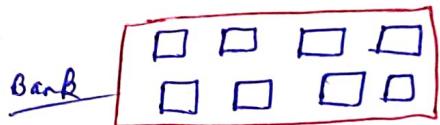


#1) Arrays:

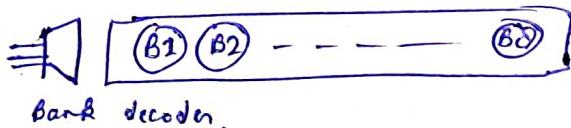


(only one cell can be active at a time using Row/Column ref value)

#2) Bank: Suppose we want θ bits at a time so we need those much arrays. Diff bits can be read at a time using Row/Column addrs.

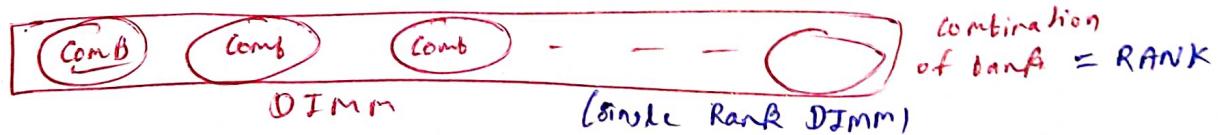


#3) Combo of Banks

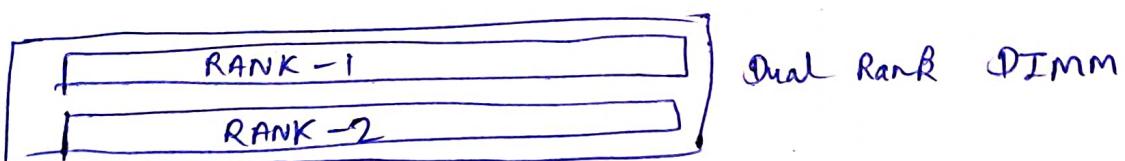


#4) Dual Inline Memory Module (DIMM) * It is plugged into RAM slot of motherboard

* Connected to memory controller via memory channel:



*



#5) Typical PC have 4 RAM slots: - we can install 4-DIMM.

DDR Phy Interface (DFI)

→ DFI is an interface protocol that defines signals, timings and programmable parameters required to transfer control information and data to and from DRAM devices and between Microcontroller(MC) & PHY.

Why DFI?

- * Mostly MC & PHY are defined separately
- * MC devices are clock ~~mos~~ based, whereas PHY usually have significant amount of Analog logic so even within same company they are designed by different engineers.
- * DFI creates a well defined interface for the two separate design teams (MC & PHY).