

MOSFET & GaN FET APPLICATION HANDBOOK

A Power Design
Engineer's Guide



nexperia

MOSFET & GaN FET Application Handbook

A Power Design Engineer's Guide

Nexperia

Manchester, United Kingdom



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Introduction

Welcome to the Nexperia MOSFET and GaN FET Application Handbook, the second edition of our successful design guide. Written by engineers for engineers, this unique collection of technical materials and application notes provides essential and up-to-date information for anybody tasked with integrating MOSFETs and GaN FETs into real-world systems. In the following pages we share expertise and learnings that Nexperia's engineering teams have built up over many years of helping customers in a variety of sectors take their applications from initial concept, through prototyping and on into final production.

The knowledge contained in this guide could not be more relevant or timely. Never before has there been such pressure on engineers to create products and systems that not only deliver high levels of performance and functionality but do so within increasingly restrictive size and power constraints. What's more, the requirement for cost-effective and efficient power conversion and electrification is only going to intensify as society looks to reduce energy costs, drive down greenhouse gas emissions and make the most of renewable resources while meeting the increased demands of a growing population and an explosion in the number of applications reliant on electricity.

From consumer products to automotive electronics, data centres to industrial automation, and communication infrastructure to medical equipment, no application area is untouched by the need for components that switch, convert and manage power and engineers who know how to deploy those components to optimal effect.

At the lower end of the power spectrum, IoT, consumer and other mobile electronic devices rely on high-efficiency configurations to support the best possible user experience in tandem with minimizing form factor and maximizing time between charge or battery replacement. Reliance on electronics for safety, comfort and infotainment combined with a shift to autonomous, connected vehicles and hybrid and fully electric powertrains makes power design a critical factor in the automotive sector. For data centres significant cost and environmental benefits can be realized by even small efficiency gains when extrapolated across millions of servers. In modern factory automation systems where output in kilowatts for motor drives is now common, effective use of power is the cornerstone of efficient and accurate motion control. And when it comes to communications infrastructure, 5G roll-out is set to generate major demand for technologies that deliver high-density, ultra-efficient, ultra-reliable power use.

What is clear is that, irrespective of the application, no longer can power be seen as an afterthought, something to be addressed only after the design and prototyping of a product or system's core functionality. What's more, with efficient and effective power management at or near the very top of the design agenda, not

only is the role of the power engineer more relevant than ever before but other engineers are having to broaden their skillset to address power and efficiency challenges. Which means gaining an understanding of discrete semiconductor technologies such as power MOSFETs, small-signal MOSFETs and GaN FETs and knowing how best to use these devices to both meet demanding product specification and performance requirements and deliver the efficiencies expected by customers and legislators.

For mains- and battery-powered applications, advances in power MOSFET structures and packaging continue to drive forward system efficiency and performance. In addition to fast and efficient switching for power supplies, many power MOSFETs are now designed with particular applications in mind. Such application-specific MOSFETs (ASFETs) may include, for example, optimised parameters to address soft-start, live insertion, short-circuit resilience, avalanche ruggedness and advanced thermal management.

Today's low-current, small-signal MOSFETs are deployed in applications that range from DC-DC conversion and load switching to level shifting in bi-directional bus systems. Among the trends for these devices are high-speed switching and advanced packaging that supports the performance, power density and miniaturization needs of high-component-density applications such as mobile battery-powered electronics and wearables.

More recent additions to the portfolio of power discretes include those fabricated from wide bandgap (WBG) materials such as gallium nitride, which have already achieved great success in RF power. Now, thanks to a combination of ultra-low $R_{DS(on)}$ at high voltages, excellent switching FOM (figure of merit), thermal stability, high-frequency operation and reducing price points they are becoming important for a growing number of high-power, high-density, ultra-high-speed switching applications – including hard-switched topologies where silicon super-junction FETs cannot be used. Offering options for automotive, telecommunications, computing and industrial market sectors, the power GaN technology covered in this Handbook targets the needs of AC-DC and DC-DC conversion, power factor correction (PFC), automotive on-board charging and electric drive applications.

It is interesting to note that the patent for the first field effect transistor was filed by Polish-American physicist Julius E. Lilienfeld in 1926 and the first super-junction FET was patented back in 1984. Although FET technology has clearly moved on significantly in the last few decades (not least in terms of switching speeds - some of the latest MOSFETs switch in the time it takes light to move just 3 m), many of the key issues that engineers must consider remain the same. Understanding the impact of switching, conduction and avalanche losses on system efficiency, for example, is critical in most designs, as are techniques for ensuring EMC compliance, optimised thermal management and reliability. A range of other factors will need to be taken into account for applications based on emerging GaN FET technology.

Furthermore, as product choice grows, so too does the challenge of narrowing down the plethora of FET options to those that are most likely to match the requirements of a given use case, comparing those devices on a ‘like-for-like’ basis and then deciding which will deliver the ‘real-world’ performance demanded by the target application. This challenge is not made any easier by a lack of consistency between suppliers regarding the conditions used for rating key parameters.

This Application Handbook provides useful guidance on all of these topics and many other issues that the design engineer is likely to encounter when working with MOSFETs and GaN FETs. By providing insight into their sometimes confusing and complex behaviour – including information necessary to solve common problems and avoid potential pitfalls – Nexperia’s belief is that the Handbook will become a ‘go-to’ reference for anybody tasked with delivering optimised power and small-signal switching, power conversion and power management.

To supplement the handbook, further product information and the most up-to-date application notes can be found at www.nexperia.com

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Chapter 1

Understanding power MOSFET data sheet parameters

Application Note: AN11158

1 Introduction

This chapter describes the content of power MOSFET data sheet parameters. The goal is to help an engineer decide what device is most suitable for a particular application.

It is important to pay attention to the conditions for which the parameters are listed, as they can vary between suppliers. These conditions can affect the values of the parameters making it difficult to choose between different suppliers.

Throughout this document, the data sheet for BUK7Y3R5-40H is used as an example. BUK7Y3R5-40H is an automotive-qualified part in a SOT669 (LFPACK56) package, with a voltage rating of 40 V.

The layout of this data sheet is representative of the general arrangement of Nexperia power MOSFET data sheets.

Nexperia Power MOSFETs are designed with particular applications in mind. For example, switching charge is minimized where switching losses dominate, whereas on-resistance is minimized where conductive losses dominate.

- General description, describing the technology used, the package and relevant qualifications, e.g. AEC-Q101
- Features and benefits, listing important features of the MOSFET and the benefit they offer.
- Applications, listing the applications for which the MOSFET is particularly suited.

The product overview is followed by these technical sections:

- Quick reference data
- Pinning information
- Ordering information
- Limiting values
- Thermal characteristics
- Electrical characteristics
- Package outline

2 Data sheet technical sections

Nexperia power MOSFET data sheets begin with an overview of the device, giving the designer the key information regarding device suitability. The overview consists of:

- General description, describing the technology used, the package and relevant qualifications, e.g. AEC-Q101

- Features and benefits, listing important features of the MOSFET and the benefit they offer.
- Applications, listing the applications for which the MOSFET is particularly suited.

The product overview is followed by these technical sections:

- Quick reference data
- Pinning information
- Ordering information
- Limiting values
- Thermal characteristics
- Electrical characteristics
- Package outline

2.1 Quick reference data

The quick reference data table contains more detailed information and the key parameters for the intended application. An example of a quick reference data table is shown in Table 1 “Quick reference data”.

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25^{\circ}\text{C}$; Figure 1 [1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25^{\circ}\text{C}$; Figure 2	-	-	115	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 20\text{ A}; T_j = 25^{\circ}\text{C}$	2	2.9	3.5	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 20\text{ A}; V_{DS} = 44\text{ V}; V_{GS} = 10\text{ V}$	-	6	15	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}$	-	16	-	nC

[1] 120 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

The general format for describing a parameter is to provide the official symbol and then the correct parameter name. Any relevant conditions and information are listed after the parameter names. The values and units of the values are entered in the remaining columns. Generally, measurement methods are as described in IEC 60747-8.

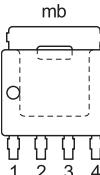
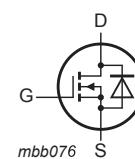
The quick reference data parameters are described in more detail in the characteristics section of the data sheet. The following list is an introduction to some of the key symbols together with a description of the parameter each represents:

- **V_{DS}** - the maximum voltage between drain and source that the device is guaranteed to block in the off state. This section of the data sheet deals with the most commonly used temperature range, as opposed to the full temperature range of the device.
- **I_D** - the maximum continuous current the device can carry with the mounting base held continuously at 25 °C with the device fully on. In the example provided in Table 1, I_D requires a V_{GS} of 10 V.
- **P_{tot}** - the maximum continuous power the device can dissipate with the mounting base held continuously at 25 °C.
- **R_{DS(on)}** (drain-source on state resistance) - the typical and maximum resistance of the device in the on-state under the conditions described. R_{DS(on)} varies greatly with both T_j and the gate-source voltage (V_{GS}). Graphs are provided in the data sheet to assist in determining R_{DS(on)} under various conditions.
- **Q_{GD}** (gate-drain charge) - an important switching parameter that relates to switching loss, along with Q_{GS} and Q_{G(tot)}. Q_{GD} is inversely proportional to R_{DS(on)}, therefore choosing an appropriate balance between R_{DS(on)} and Q_{GD} is critical for optimal circuit performance.
- **Q_r** (recovered charge) – the total amount of charge recovered from the anti-parallel diode when it is switched from its conducting state to its reverse biased state under controlled conditions. Q_r is an important factor involved in voltage spiking when interacting with external inductances and an important consideration when investigating EMC and efficiency. Generally the higher the Q_r value the larger the voltage and current spikes at switch off leading to longer damping times. Nexperia includes stored charge Q_s as well as output charge Q_{oss} in its stated value for Q_r such that Q_r = Q_s + Q_{oss}.

2.2 Pinning information

This section describes the internal connections and general layout of the device. Note that the symbol is for an enhancement mode n-channel MOSFET with the source and body tied together, and a parallel diode between the source and drain. The parallel diode is known as the body diode and is inherent in power MOSFETs. N-channel power MOSFETs have the body diode between drain and source, as shown in Table 2.

Table 2: Pinning Information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	 LFPACK56; Power-SO8 (SOT669)	 mbb076

2.3 Ordering information

The ordering section provides information on how to order the device. The package version and description are given as well as any commonly used package name.

2.3.1 Marking

Depending on the device package, the data sheet may include a marking section. This provides the marking code which is printed onto the device during manufacture, (else the device name will be printed).

2.4 Limiting values

The limiting values table provides the range of operating conditions allowed for the MOSFET. The conditions are defined in accordance with the absolute maximum rating system (IEC 60134). Operation outside of these conditions is not guaranteed, so it is recommended that these values are not exceeded. Doing so runs the risk of immediate device failure or reduced lifetime of the MOSFET. The avalanche ruggedness conditions, when given, describe the limited conditions for which the V_{DS} rating can be exceeded.

To calculate how the limiting values change with temperature, they are read together with the derating curves provided.

The limiting values table for the BUK7Y3R5-40H is given as an example of a standard limiting values table, in Table 3.

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$	-	40	V
V_{GS}	gate-source voltage		-10	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$;	-	115	W
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ }^{\circ}\text{C};$ Figure 1	[1]	-	120 A
		$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ }^{\circ}\text{C};$ Figure 2	[1]	-	93 A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ }^{\circ}\text{C}$	-	526	A
T_{stg}	storage temperature		-55	175	$^{\circ}\text{C}$
T_j	junction temperature		-55	175	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	[1]	-	120 A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ }^{\circ}\text{C}$	-	526	A
Avalanche ruggedness					
$E_{DS(ALS)}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}; V_{sup} \leq 40\text{ V};$ $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V};$ $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; unclamped; Figure 3	[2] [3]	-	45 mJ

[1] 120 A continuous current has been successfully demonstrated during application tests.

Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[3] Refer to application note AN10273 for further information.

- **V_{DS}** (drain-source voltage) - the maximum voltage the device is guaranteed to block between the drain and source terminals in the off-state for the specified temperature range. For the BUK7Y3R5-40H, the temperature range is from +25 °C to +175 °C. For operation below 25 °C, the V_{DS} rating reduces due to the positive temperature coefficient of avalanche breakdown. This is covered in

Section 2.4.1 of this document.

- **V_{GS}** (gate-source voltage) - the maximum voltage the device is specified to block between the gate and source terminals. Some Nexperia data sheets specify different values for DC and pulsed V_{GS} . In these cases the DC value is a constant gate voltage over the lifetime of the device at the maximum T_j , whilst the higher-value pulsed-rating is for a shorter, specified accumulated pulse duration at the maximum specified T_j .

Gate-oxide lifetime (refer to AN90001 (chapter 2 of this book) - Designing in MOSFETs for safe and reliable gate-drive operation) reduces with increasing temperature and/or increasing gate voltage. This means that V_{GS} lifetimes or ratings quoted for lower junction temperatures are significantly greater than if specified at higher temperatures. This can be important when comparing data sheet values from different manufacturers.

- **V_{DGR}** (drain-gate voltage) is typically the same value as the V_{DS} rating. This parameter appears in the data sheets of older devices but is not quoted for newer devices such as in the BUK7Y3R5-40H data sheet.
- **I_D** (drain current) - the maximum continuous current the device is allowed to carry under the conditions described. This value can be related to either package construction, or the maximum current that would result in the maximum T_j . As such it depends on an assumed mounting base temperature (T_{mb}), the thermal resistance (R_{th}) of the device, and its $R_{DS(on)}$ at maximum T_j . Note that some suppliers quote the "theoretical" silicon limit, while indicating the package limited value in the characteristic curves.
- **I_{DM}** (peak drain current) is the maximum drain current the device is allowed to carry for a pulse of 10 µs or less.
- **P_{tot}** (total power dissipation) is the maximum allowed continuous power dissipation for a device with a mounting base at 25 °C. The power dissipation is calculated as that which would take the device to the maximum allowed junction temperature while keeping the mounting base at 25 °C. In reality, it is difficult to keep the mounting base at this temperature while dissipating the 105 W that is the calculated power dissipation for the BUK7Y3R5-40H. In other words, P_{tot} indicates how good the thermal conductivity of the device is, and its maximum allowed junction temperature.

Note that some other semiconductor vendors quote performance when mounted on a copper PCB usually 1 inch square. In practice, this information is rather meaningless as the semiconductor vendor has no control over how the device is cooled. See AN10874 - (chapter 9 of this book) - LFPAK MOSFET thermal design guide. AN10874 describes different techniques that can be used during the design phase to ensure that the PCB layout provides optimum thermal performance.

- **T_{stg}** (storage temperature) is the temperature range in which the device can be stored without affecting its reliability. Long term storage should be in an inert atmosphere to prevent device degradation, for example, by tarnishing of the metal leads.
- **T_j** (junction temperature) is the operational temperature range of the device. Typically, T_j is the same as the storage temperature. Outside of this range, device

parameters are outside the range of the data sheet and device lifetime is reduced.

- **I_S** (source current) - the maximum continuous current of the MOSFET body diode, which is briefly discussed in Section 2.2. The same considerations apply as for I_D .
- **I_{SM}** (peak source current) - the maximum current pulse that the MOSFET body diode is guaranteed to carry. The same considerations apply as for I_{DM} .
- **$E_{DS(AL)S}$** (non-repetitive drain-source avalanche energy) - the maximum allowed single overvoltage energy pulse under the conditions specified. For this example, the conditions are the maximum continuous drain current allowed for a mounting base temperature of 25 °C. The avalanche energy allowed is the energy pulse that would raise the device temperature from 25 °C to its maximum allowed T_j , while the mounting base temperature is held at 25 °C. The avalanche energy is specified for the maximum continuous drain current. Some vendors specify the avalanche energy for a different current and higher inductive load, which can increase the apparent avalanche energy for an inferior performance. An example is given with the derating curve as described in Section 2.4.3 of this document.
- **$E_{DS(AL)R}$** (repetitive drain-source avalanche energy) - the maximum amount of energy allowed in each avalanche event when more than one avalanche event occurs. The thermal constraints imposed for repeated avalanche operation is given by curve 3 of Figure 3 in Section 2.4.3 of this document. There are also the standard thermal requirements in addition to the energy requirements for repetitive avalanche events. These requirements are assessed with the thermal characteristic curves as described in Section 2.5. Avalanche performance is covered in detail in application note AN10273 (Chapter 4 of this book) - Power MOSFET single-shot and repetitive avalanche ruggedness rating. This parameter is only listed on Nexperia data sheets where the repetitive avalanche capability has been assessed. It is not shown in Nexperia data sheets where it has not been assessed, for example non-automotive MOSFETs.

2.4.1 Derating curves

The derating curves are provided immediately after the tabulated limiting value data, and help the designer calculate how the limits change with temperature.

2.4.1.1 Continuous drain current

The following procedure serves as an example to calculate the maximum continuous drain current for the BUK7Y3R5-40H. Assume an application with a mounting base temperature T_{mb} of 75 °C.

Refer to the graph depicted in Figure 1 which depicts the continuous drain current as a function of mounting base temperature.

Figure 1 shows that for a T_{mb} of 75 °C, the maximum continuous drain current has

reduced from 120 A, listed at 25 °C, to 105 A, see Equation (1) and Equation (2) below.

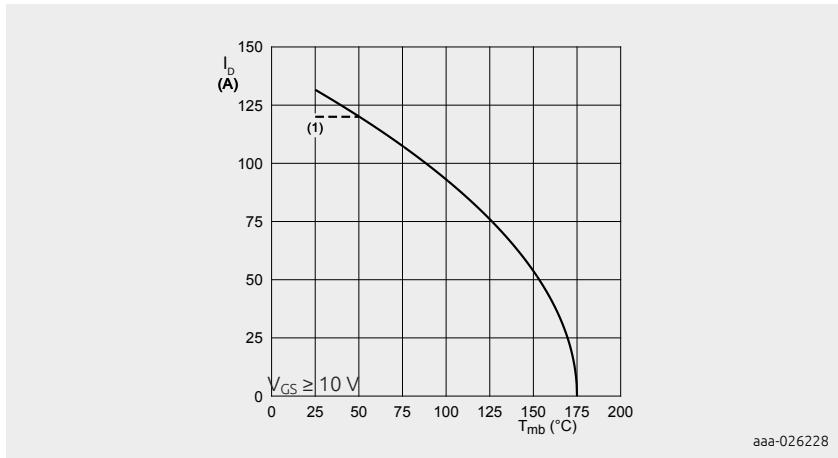
The maximum current at any T_{mb} , is the current that increases T_j to the maximum allowed temperature (175 °C). $P = I^2 \times R_{DS(on)}$ represents the power dissipation at T_j , where the $R_{DS(on)}$ used is the maximum value for the maximum T_j . Therefore, the allowed current is proportional to the square root of the allowed power dissipation.

The power dissipation allowed for a given T_{mb} is proportional to the allowed temperature increase. This means that the derating curve shown, is based on the following equations:

$$ID^2(T_{mb}) \propto \frac{T_j - T_{mb}}{T_j - 25^\circ C} \quad [1]$$

$$ID(T_{mb}) = ID(25^\circ C) \times \sqrt{\frac{T_j - T_{mb}}{T_j - 25^\circ C}} \quad [2]$$

At the maximum allowed junction temperature of 175 °C, this current has decreased to zero



(1) 120 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Figure 1 | Continuous drain current as a function of mounting base temperature

2.4.2 Power dissipation

Power dissipation varies with different temperatures. However, in this case, the power dissipation curve is normalized. The allowed power is presented as a percentage of the allowed power dissipation at 25 °C, as opposed to an absolute value.

Example:

By observing the curve in Figure 2, the allowed power dissipation for a T_{mb} of 75 °C is approximately 66 % of that allowed at 25 °C. The graphic data in Figure 2, shows the maximum continuous power dissipation (P_{tot}) at 25 °C is 105 W.

This means that the maximum power dissipation allowed at 75 °C, is 66 % of 105 W which is 70 W.

Equation (3) is the equation to calculate power dissipation:

$$\frac{P_{tot}(T_{mb}) - P_{tot}(25^{\circ}\text{C})}{T_j - 25^{\circ}\text{C}} \times [3]$$

Where $T_j = T_j(\text{max})$, usually 175 °C.

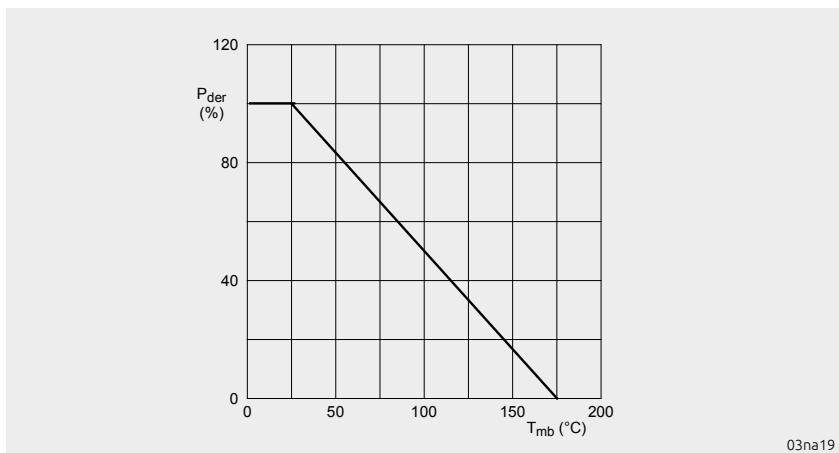


Figure 2 | Normalized total power dissipation as a function of mounting base temperature

The curves provided in Figure 1 and Figure 2 are read in conjunction with the limiting values tables. The information extracted, assists in calculating the maximum current allowed and the power dissipation with respect to temperature.

2.4.3 Avalanche ruggedness

Avalanche ruggedness is covered in detail in AN10273 (chapter 4 of this book) - Power MOSFET single-shot and repetitive avalanche ruggedness rating.

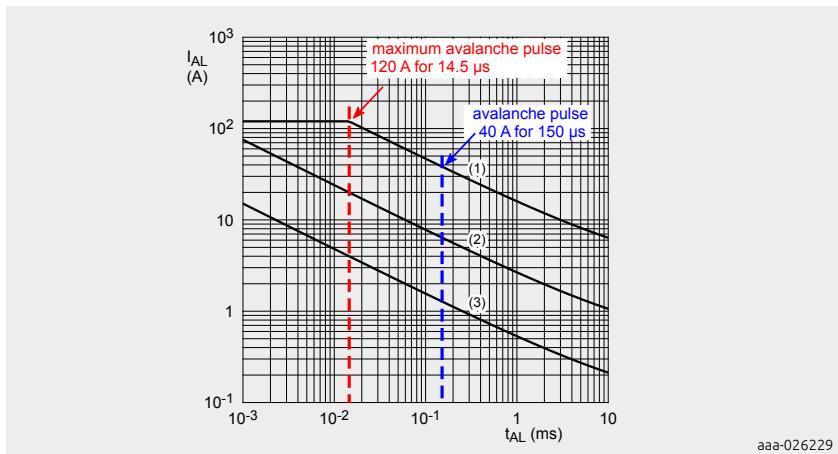


Figure 3 | Avalanche current as a function of avalanche period

A simple example for the BUK7Y3R5-40H, using the information in AN10273, is extracted from the limiting values Table 3:

With $I_D = 120$ A, $V_{sup} \leq 40$ V, $R_{GS} = 50 \Omega$, $V_{GS} = 10$ V and $T_{j(init)} = 25^\circ\text{C}$ unclamped, the maximum $E_{DS(AL)}$ is 45 mJ.

An avalanche event has a triangular pulse shape, so the average power is calculated as $(0.5 \times V_{DS} \times I_{DS})$.

AN10273 states that the assumed breakdown voltage is 130 % of the rated voltage, in the case of the BUK7Y3R5-40H this is 52 V (40 V \times 1.3).

Figure 3 shows a maximum current of 120 A at 25°C (the limiting values Table 3 confirms this value). The time for the maximum avalanche energy can be read from Figure 3 as 14.5 μs .

This means that the maximum avalanche energy allowed is:
 $0.5 \times (40 \text{ V} \times 1.3) \times 120 \text{ A} \times 14.5 \mu s = 45.24 \text{ mJ}$.

However the limit value quoted in Table 5 of the data sheet is rounded to 45 mJ. If a competitor quotes avalanche energy at 40 A, the graph shows that the avalanche time for the BUK7Y3R5-40H has increased to 150 μs . The avalanche energy is now

$0.5 \times (40 \text{ V} \times 1.3) \times 40 \text{ A} \times 150 \mu s = 156 \text{ mJ}$, which is much higher than data sheet

limiting value. Ruggedness events lie outside the Safe Operating Area (SOA).

2.4.4 Safe Operating Area (SOA)

The Safe Operating Area (SOA) curves are some of the most important on the data sheet.

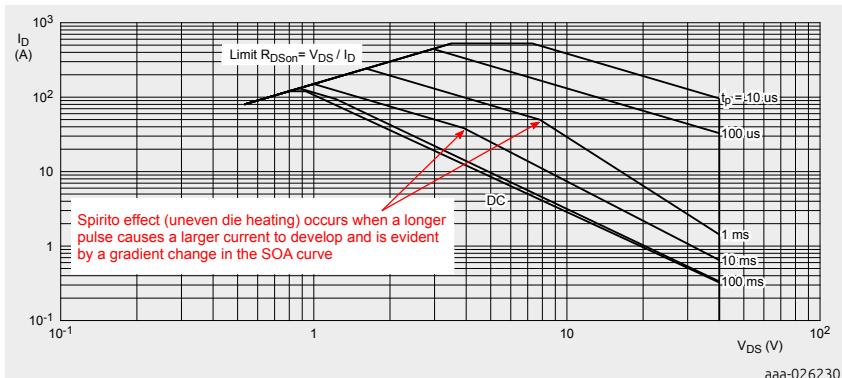


Figure 4 | Safe operating area; continuous and peak drain currents as a function of drain-source voltage

The SOA curves show the voltage allowed, the current and time envelope of operation for the MOSFET. These values are for an initial T_{mb} of 25 °C and a single current pulse. This is a complex subject which is further discussed in the appendix (Section 3.1).

2.5 Thermal characteristics

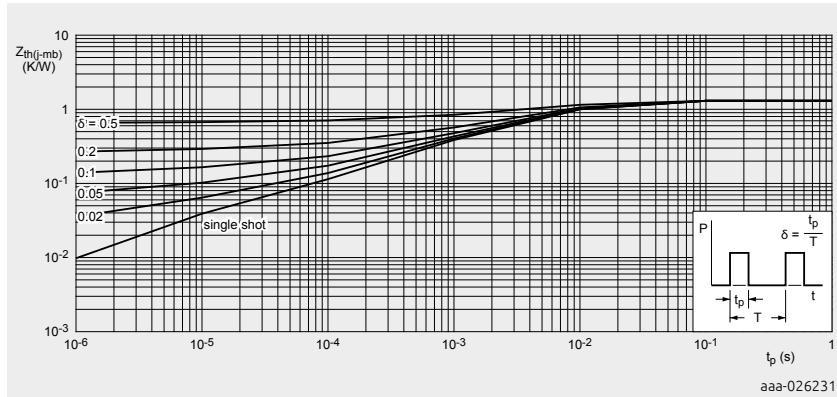
This section describes the thermal impedance as a function of pulse duration for different duty cycles. This information is required to determine the temperature that the silicon reaches under particular operating conditions, and whether it is within the guaranteed operation envelope.

The thermal characteristics are shown in Table 4. The thermal impedance changes with pulse length because the MOSFET is made from different materials. For shorter durations, the thermal capacity is more important, while for longer pulses, the thermal resistance is more important.

The thermal characteristics are used to check whether particular power loading pulses above the DC limit would take T_j above its safe maximum limit. Repetitive avalanche pulses must be considered in addition to the constraints specific to avalanche and repetitive avalanche events.

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Figure 5	-	1.18	1.3	K/W

**Figure 5 | Transient thermal impedance from junction to mounting base as a function of pulse duration.**

Thermal resistance (R_{th}) and thermal impedance (Z_{th}) are related because the thermal resistance is the steady-state measure of how the device blocks heat flow. Thermal impedance is how the device responds to transient thermal events. It involves different thermal capacities of parts of the device and the thermal resistances between these parts. Under DC conditions, Z_{th} is equal to R_{th} . Equation (4) represents the temperature rise for a particular power dissipation:

$$\Delta T_j = |Z_{th(j\text{-}mb)}| \times \text{Power} \quad [4]$$

A worked example is discussed in the appendix (Section 3.1.2).

2.6 Electrical characteristics

This section is used to determine whether the MOSFET would be suitable in a particular application. This section differs from the previous two sections that are used to determine whether the MOSFET would survive within the application. The examples in this section are taken from the data sheet for the BUK7Y3R5-40H unless otherwise stated.

2.6.1 Static characteristics

The static characteristics are the first set of parameters listed in this section and an example is shown in Table 5:

Table 5: Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C}$	40	42.7	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -40^\circ\text{C}$	-	40.1	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55^\circ\text{C}$	36	39.7	-	V
$V_{GS(\text{th})}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25^\circ\text{C};$ Figure 6; Figure	2.4	3	3.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55^\circ\text{C};$ Figure 6	-	-	4.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175^\circ\text{C};$ Figure 6	1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C}$	-	0.03	1	μA
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125^\circ\text{C}$	-	1	10	μA
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175^\circ\text{C}$	-	37	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25^\circ\text{C}$	-	2	100	nA
$R_{DS(\text{on})}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25^\circ\text{C}$	2	2.9	3.5	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 105^\circ\text{C};$ Figure 9	2.7	4.1	5.2	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 125^\circ\text{C};$ Figure 9	2.9	4.5	5.6	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175^\circ\text{C};$ Figure 9	3.4	5.4	6.7	$\text{m}\Omega$
R_G	gate resistance $f = 1 \text{ MHz}; T_j = 25^\circ\text{C}$		0.32	0.8	2	Ω

- $V_{BR(DSS)}$ (drain-source breakdown voltage) - an expansion of the parameter listed and explained in Section 2.4. This section lists the minimum voltage the device is guaranteed to block between the drain and source terminals in the off-state over the entire MOSFET temperature range. The temperature range is from -55 °C to +175 °C. The current between the drain and the source terminals of the BUK7Y3R5-40H when testing $V_{(BR)DSS}$ is 250 µA at the temperatures stated. $V_{(BR)DSS}$ is 40 V or less if the device is cooler than +25 °C and 40 V if the device is between +25 °C and +175 °C.

The effect of temperature on the off-state characteristics is twofold. The leakage current increases with temperature, turning the device on. Competing against the leakage current increase, the breakdown voltage also increases with temperature.

- $V_{GS(th)}$ (gate-source threshold voltage) is important for determining the on-state and the off-state of the MOSFET. $V_{GS(th)}$ is defined where $V_{DS} = V_{GS}$, although it is sometimes quoted for a fixed V_{DS} (e.g. 10 V). Note that the definition of the threshold voltage for a particular current where the gate and drain are shorted together, can differ from examples in textbooks. The parameter in textbooks describes a change in the physical state of the MOSFET and is independent of the MOSFET chip size. The parameter used in the data sheet is for a specified current and is dependent on the chip size, as the current flow is proportional to the chip area.

The threshold voltage in the data sheet is defined in a way that is best for routine measurement, but not how the actual device would typically be used.

Consequently, the graphs provided in Figure 6 and Figure 7.

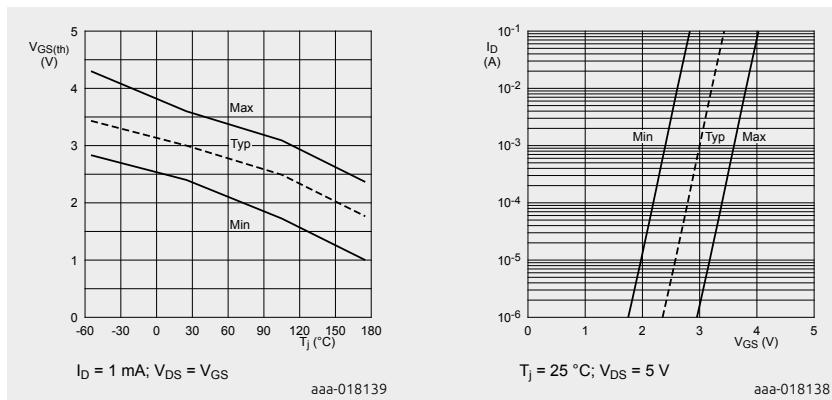


Figure 6 | Gate-source threshold voltage as a function of junction temperature

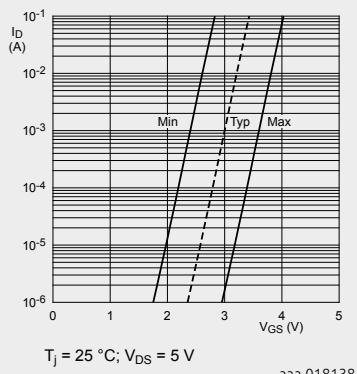


Figure 7 | Subthreshold drain current as a function of gate-source voltage

Figure 6 shows the variation in the threshold voltage for the typical and limit devices over the rated temperature range. All the MOSFETs are guaranteed to have a threshold voltage between the lines.

Consequently, for the BUK7Y3R5-40H at 65 °C, if V_{DS} and V_{GS} are both less than 2 V, all devices carry less than 1 mA. Also, all devices carry more than 1 mA if V_{DS} and V_{GS} are both greater than 4 V. At 175 °C, the lower limit has fallen to 1 V, while the upper limit has fallen to 2.4 V. The lower limit is usually more important as it determines when the device is guaranteed to be turned off, and the gate driver performance an application needs.

Figure 7 shows how the device turns on around this threshold voltage. For the BUK7Y3R5-40H, the current increases 100,000 times for an increase in gate voltage of less than 1 V. An example is given for the situation when the drain-source voltage is fixed at 5 V.

- I_{DSS} (drain leakage current) guarantees the maximum leakage current that the device passes at its maximum rated drain-source voltage(40V in this case) during the off-state. It is important to note how much higher I_{DSS} is at high temperature, which is the worst case.
- I_{GSS} (gate leakage current) guarantees the maximum leakage current through the gate of the MOSFET. The I_{GSS} is important when calculating how much current is required to keep the device turned on. Because it is a leakage current through an insulator, this current is independent of temperature, unlike I^{DSS} .
- $R_{DS(on)}$ (drain-source on-state resistance) is one of the most important parameters. The previous parameters guarantee how the device functions when it is off, how it turns off and what leakage currents could be expected. These factors are important when battery capacity is an issue in the application.

$R_{DS(on)}$ is a measure of how good a closed-switch the MOSFET is, when turned-on. It is a key factor in determining the power loss and efficiency of a circuit containing a MOSFET. The on-resistance $R_{DS(on)} \times I_D$ gives the power dissipated in the MOSFET when it is turned **fully** on. Power MOSFETs are capable of carrying tens or hundreds of amps in the on-state.

Power dissipated in the MOSFET makes the die temperature rise above that of its mounting base. Also when the MOSFET die temperature increases, its $R_{DS(on)}$ increases proportionally. Maximum recommended junction temperature is 175 °C (for all Nexperia **packaged** MOSFETs).

Using the BUK7Y3R5-40H data sheet as an example:

$R_{th(j-mb)}$ temperature rise per Watt between junction (die) and mounting base = 1.3 K/W (1.3 °C/W).

Maximum power dissipation for temperature rise of 150 K ($T_{mb} = 25$ °C, $T_j = 175$ °C) = $150 / 1.3 = 115.38$ W, note data sheet P_{tot} is rounded to 115 W.

Maximum $R_{DS(on)}$ at a die temperature (T_j) of 175 °C = 6.7 mΩ.

Therefore, at steady state with $T_{mb} = 25$ °C and $T_j = 175$ °C; $P = 115.38$ W = $I_D^2 \times$

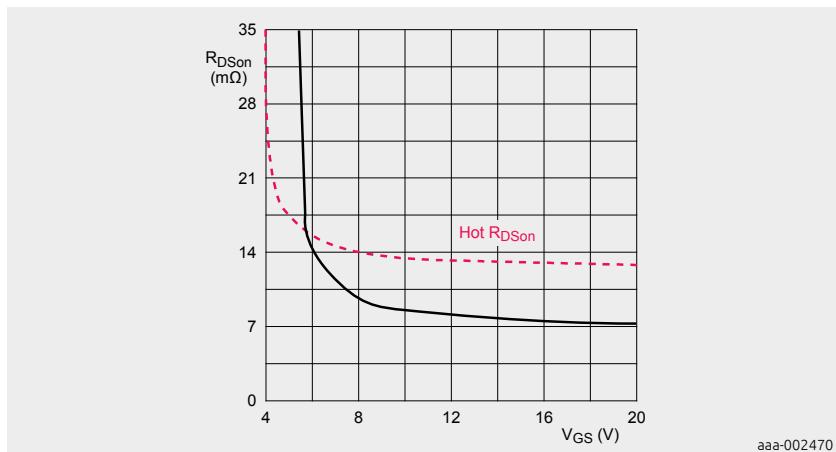
$R_{DS(on)}$ (175 °C). Therefore:

$$I_{max} = \sqrt{\frac{P_{(max)} 175 \text{ } ^\circ\text{C}}{R_{DS(on)} 175 \text{ } ^\circ\text{C}}} = \sqrt{\frac{115.38 \text{ W}}{0.0067 \Omega}}$$

= 131.23 A (rounded down to 120 A in the data sheet).

Note this value appears on the curve for I_D vs T_{mb} in Figure 1 but only 120 A is claimed in the data sheet. Practically, limitations are placed on MOSFET performance due to PCB, thermal design and operating temperature, which will all act together to raise the mounting base temperature.

Figure 8 shows the dependency of $R_{DS(on)}$ on the gate-source voltage for a standard level MOSFET (e.g. BUK7Y12-55B); the red dashed line shows the curve for a hot device and is indicative of how the dependency changes at a high temperature.



This diagram is for illustrative purposes only and not to be taken as an indication of hot $R_{DS(on)}$ performance for any device.

Figure 8 | Drain-source on-state resistance as a function of gate-source voltage at 25 °C and high temperature

If an application requires good $R_{DS(on)}$ performance for lower gate-source voltages, then MOSFETs are made with lower threshold voltages, e.g. the BUK9Y12-55B (logic level MOSFET). However, the lower threshold voltage of such a device means that it has a lower headroom for its off-state at high temperature. This lower headroom often means that a device with a higher threshold voltage is needed.

Figure 9 shows how the ratio of $R_{DS(on)}$ to $R_{DS(on)}$ at 25 °C typically varies with junction temperature for BUK7Y3R5-40H.

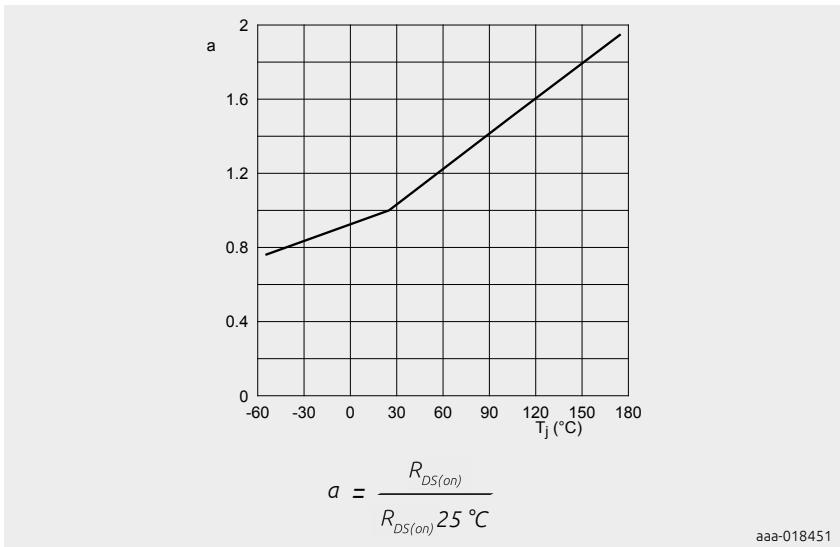


Figure 9 | Normalized drain-source on-state resistance factor as a function of junction temperature

R_G (gate resistance) is the internal series resistance presented to the gate pin. In most applications an external “gate stopper” resistance of a larger value is employed to mitigate gate oscillation and, dependent on value chosen, decrease output slew rate.

2.6.2 Dynamic characteristics

The dynamic characteristics determine the switching performance of the device. Several of these parameters are highly dependent on the measurement conditions. Consequently, understand the dynamic characteristics before comparing data sheets from suppliers with different standard conditions. Table 6 is a sample dynamic characteristics table.

Table 6: Dynamic characteristics

List of constants and limitations relating to the table i.e. voltages, currents and temperatures

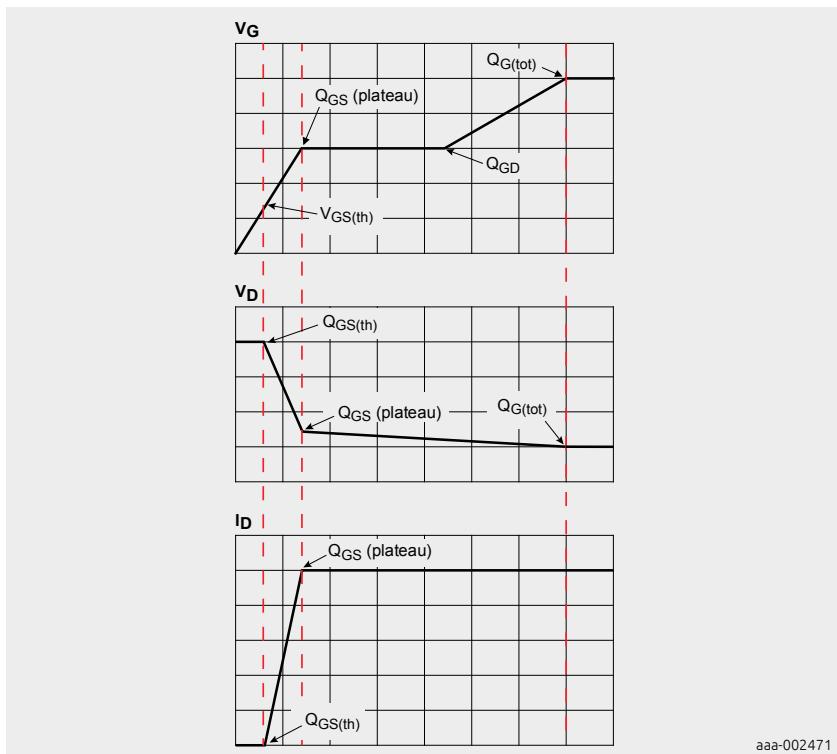
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V};$	-	31	53	nC
Q_{GS}	gate-source charge		-	10	15	nC
Q_{GD}	gate-drain charge		-	6	15	nC
C_{iss}	input capacitance		-	2294	3441	pF
C_{oss}	output capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25^\circ\text{C};$	-	682	954	pF
C_{rss}	reverse transfer capacitance		-	112	247	pF
$t_{d(on)}$	turn-on delay time		-	10	-	ns
t_r	rise time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V}; R_G(\text{ext}) = 5 \Omega$	-	8	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
t_f	fall time		-	9	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C};$	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ V}/\mu\text{s}; V_{GS} = 20 \text{ V};$	-	25	-	ns
Q_r	recovered charge		-	16	-	nC

2.6.2.1 Gate charge

$Q_{G(\text{tot})}$, Q_{GS} , and Q_{GD} are all parameters from the same gate charge curve. They describe how much gate charge the MOSFET requires to switch, for certain conditions. This is particularly important in high frequency switching applications. Much of the power loss occurs during switching, when there are significant voltage and current changes simultaneously between the drain, gate and source. In the blocking state, there are significant voltages but negligible currents. In the full-on state, there are significant currents and small voltages.

The gate charge parameters are dependent on the threshold voltage and the switching dynamics as well as the load that is being switched. There is a difference between a resistive load and an inductive load.

An example of a gate charge curve is shown in Figure 10:



aaa-002471

Figure 10 | Gate charge curve also showing drain-source currents and voltages

Due to capacitance variation with voltage and current, it is better to look at the gate charge data rather than the capacitance data when determining switching

performance. This is especially true if the gate-driver circuit for the MOSFET is limited to a particular current, and a rapid switch is required.

The gate charge curve describes what happens to a MOSFET which has a drain supply limited to a particular current and voltage. The operation of the test circuit means that during the gate charge curve, the MOSFET is provided with either a constant voltage or a constant current.

During this time, the drain-source voltage begins to fall because the increased charge on the MOSFET allows easier conduction. Consequently, although the gate-source voltage is constant, the drain-gate voltage is falling.

Eventually the capacitance stops increasing and any further increases in gate charge increase the gate-source voltage. This characteristic is sometimes referred to as the "Miller plateau" as it refers to the time during which the so-called Miller capacitance increases. The Miller plateau is also known as the gate-drain charge (Q_{GD}).

During this period, there are significant currents and voltages between the drain and source, so Q_{GD} is important when determining switching losses.

Once the end of the Miller plateau is reached, the gate-source voltage increases again, but with a larger capacitance than before Q_{GS} had been reached. The gradient of the gate charge curve is less above the Miller plateau.

The gate-charge parameters are highly dependent on the measurement conditions. Different suppliers often quote their gate-charge parameters for different conditions, demanding care when comparing gate charge parameters from different sources.

Higher currents lead to higher values of gate-source charge because the plateau voltage is also higher. Higher drain-source voltages, lead to higher values of gate-drain charge and total gate charge, as the plateau increases.

The drain-source currents and voltages during the gate charge switching period are shown in Figure 10.

If the MOSFET starts in the off state ($V_{GS} = 0$ V), an increase in charge on the gate initially leads to an increase in the gate-source voltage. In this mode, a constant voltage (V_{DS}) is supplied between the source and drain.

When the gate-source voltage reaches the threshold voltage for the limiting current at that drain-source voltage, the capacitance of the MOSFET increases and the gate-voltage stays constant. This is known as the plateau voltage and the onset charge is referred to as Q_{GS} . The higher the current is, the higher the plateau

voltage (see Figure 11). This relates to the transfer characteristic, see Figure 15. The transfer curve shows the dependency of drain current on gate voltage. The higher the voltage on the gate the higher the charge applied, ($Q = C \times V$), hence making it the easier for the MOSFET to conduct.

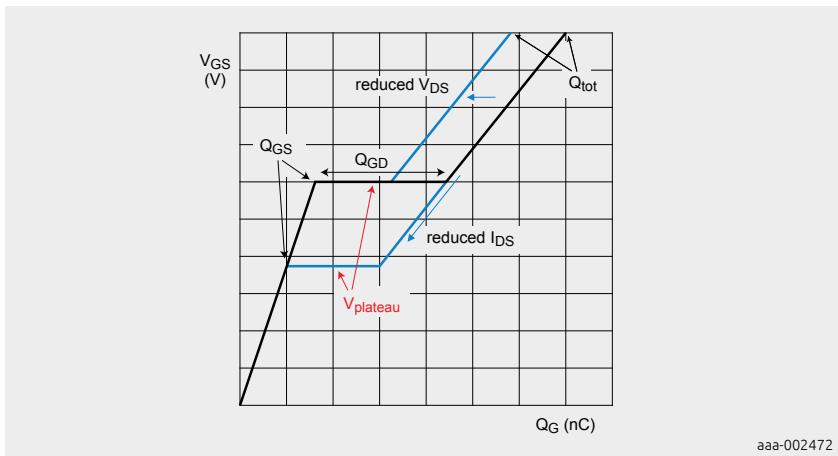


Figure 11 | Features of gate charge curve

2.6.2.2 Capacitances

Capacitance characteristics are generally less useful than the gate charge parameters, for the reasons already discussed. However, they are still listed on data sheets. The three capacitances that are normally listed are as follows:

- C_{iss} (input capacitance) is the capacitance between the gate and the other two terminals (source and drain).
- C_{oss} (output capacitance) is the capacitance between the drain and the other two terminals (gate and source).
- C_{rss} (reverse transfer capacitance) is the capacitance between the drain and the gate. See Figure 13.

Semiconductor capacitances generally depend on both voltage and the frequency of the capacitance measurement. Although it is difficult to compare capacitances measured under different conditions, many suppliers specify a measurement frequency of 1 MHz. Consequently, the capacitances vary with drain-source voltage (see Figure 12). However, the capacitances also vary with gate-source voltage, which is why the gradients in the gate-charge curve vary for different voltages (see Figure 10).

The relationship between charge, voltage and capacitance in the gate charge curve

is: $\Delta Q = \Delta C \times \Delta V$. For different gradients at different gate voltages, the capacitance changes significantly with gate-source voltage.

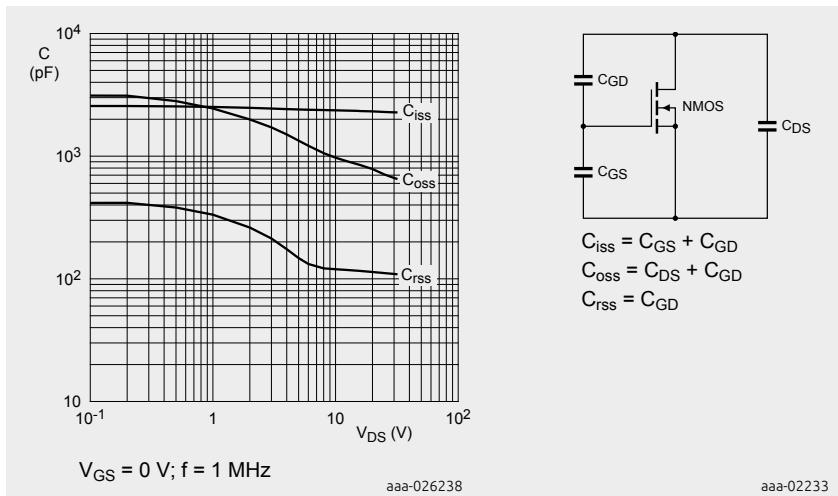


Figure 12 | Capacitances as a function of drain source voltage

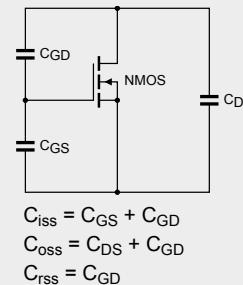


Figure 13 | MOSFET capacitance parameters

2.6.2.3 Switching times

Most manufacturers quote resistive load switching times. However, extreme care is needed when comparing data from different manufacturers, as they are highly dependent on the resistance of the gate drive circuit used for the test and in the case of logic level devices, the gate voltage applied.

In devices for fast switching applications, the gate resistance of the MOSFET is often quoted as capacitive time constants which are equally dependent on resistance and capacitance.

2.6.2.4 Diode characteristics

The diode characteristics are important if the MOSFET is being used in the so-called "third quadrant". The third quadrant is a typical arrangement where the MOSFET replaces a diode to reduce the voltage drop from the inherent diode forward voltage drop. In such a situation, there is always a small time period when the MOSFET parasitic diode is conducting before the MOSFET turns on. For such applications, the diode switching parameters are important. In addition, diode reverse recovery (Figure 14) contributes to the power losses as well as oscillation and voltage spikes, which can cause EMC concerns.

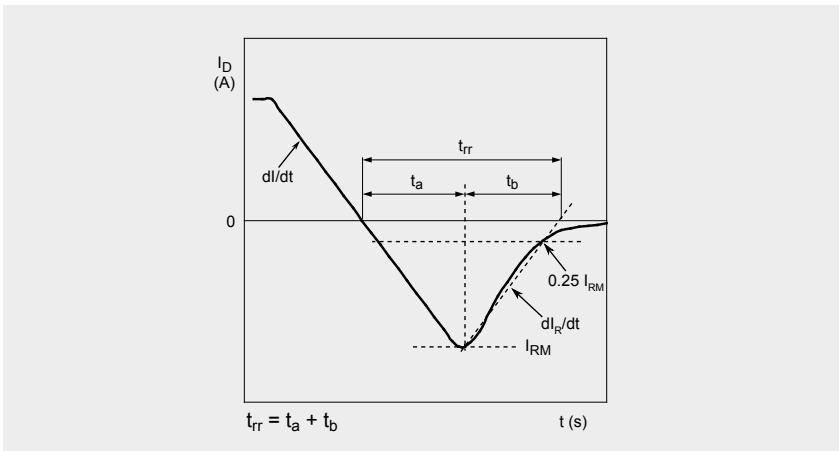


Figure 14 | Reverse recovery waveform definitions

2.6.2.5 Transfer characteristics

Figure 15 shows the transfer characteristics of the MOSFET which indicate the theoretical drain current that can be handled by the device as a result of applied gate to source voltage. The graph shows the temperature dependency of the characteristic. The convergent point indicates where the current is dependent only on gate voltage and not temperature hence the MOSFET's Zero Temperature Coefficient point I_{ZTC} . Gate charge test current and plateau voltage (refer to Figure 10) can be directly read from the transfer curve.

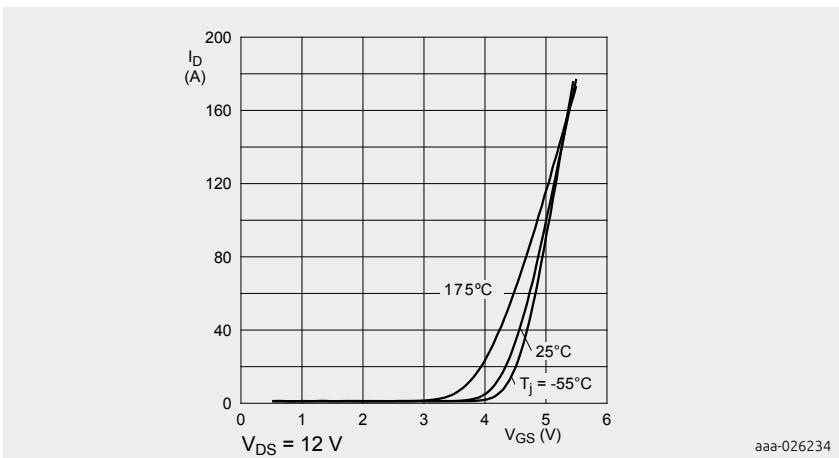


Figure 15 | Transfer characteristics; drain current as a function of gate-source voltage; typical values

3 Appendices

3.1 Safe Operating Area (SOA) curves

To highlight the key features, Figure 16 provides an idealized SOA curve for a hypothetical MOSFET. Data for a hypothetical MOSFET for a single pulse length, is shown to highlight the region where it deviates from the ideal curve.

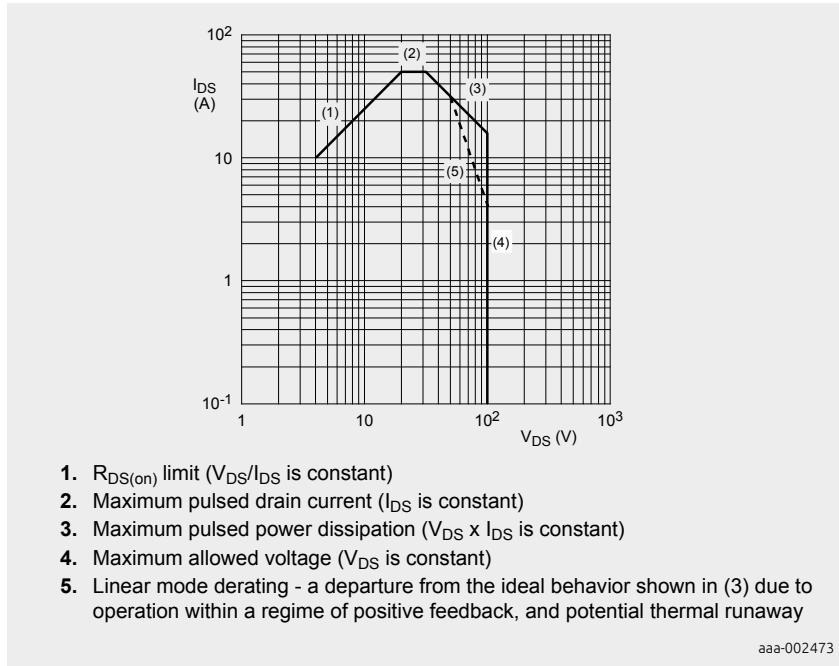


Figure 16 | Idealized SOA curve at a single time pulse for hypothetical MOSFET

The dashed line (5) is to emphasize where the curve deviates from the ideal. In reality, there is a single curve with a change of gradient where the linear mode derating becomes important.

R_{DS(on)} limit

R_{DS(on)} is region (1) of the graph and Equation [6] represents the limiting line:

$$\frac{V_{DS}}{I_{DS}} \leq R_{DS(on)(max)} (175^\circ C) \quad [6]$$

The limit is when the MOSFET is fully on and acting as a closed switch with a resistance that is no greater than the hot R_{DS(on)}.

Constant current region

The constant current region is region (2) of the graph. It is the maximum pulsed drain current, which is limited by the device manufacturer (for example, the wire-bonds within the package).

Maximum power dissipation (linear mode) limit

In this region, the MOSFET is acting as a (gate) voltage-controlled current source. This means that there are significant voltages and currents applied simultaneously, leading to significant powerdissipation. Line (3) shows the idealized curve, whereas the dotted line (5) shows where it deviates from the ideal.

The limiting factor for the SOA curve in region (5), is the heating applied during a rectangular current and voltage pulse. Even in the ideal situation, this curve depends on the transient thermal impedance of the MOSFET, which is covered in Section 2.5.

The transient thermal impedance varies with the pulse length. This is due to the different materials in the MOSFET having different thermal resistances and capacities. The differences create a thermal equivalent to an RC network from the junction (where the heat is generated) to the mounting base. Equation (7) is the calculation used to determine the ideal curve in this region.

$$P = I_D \times V_{DS} = \frac{T_{j(max)} - T_{mb}}{Z^{th(j-mb)}} = Constant \quad [7]$$

The ideal situation accurately describes the situation for sufficiently high current densities. However, it is overly optimistic for low current-densities, i.e. towards the bottom right of region (3). Low current densities and high voltages can lead to thermal runaway in the linear mode operation. Thermal runaway is discussed in the following section.

Thermal runaway in linear mode

Power MOSFETs are often considered to be immune to thermal runaway due to the temperature coefficient of resistance, which means that as temperature rises, current falls.

This is only true for MOSFETs that are fully on (i.e. in region 1), but it is not the whole story.

When a MOSFET is turned on, there are two competing effects that determine how its current behaves with increasing temperature. As the temperature rises, the threshold voltage falls. The MOSFET is effectively turned on more strongly, thereby increasing the current. In opposition, the resistance of the silicon increases with increasing temperature, thereby reducing the current. The resultant effect for a constant drain-source voltage, is shown in Figure 17. This situation occurs when the gate-source voltage of a MOSFET is being used to control the current, or when the MOSFET is switched sufficiently slowly.

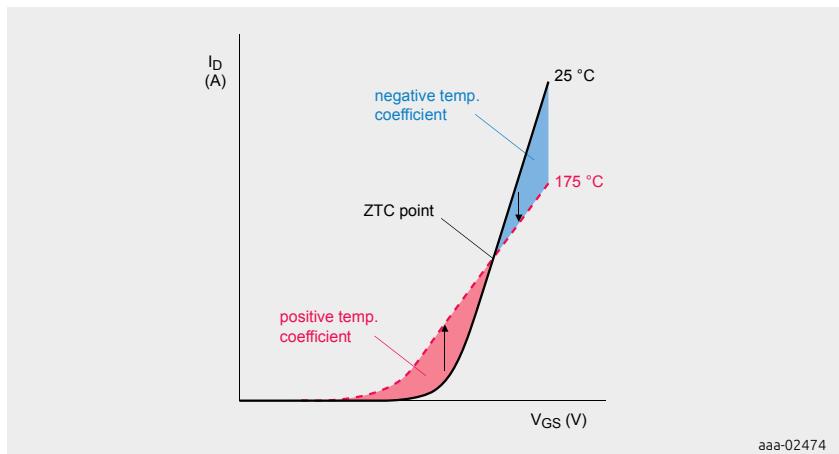


Figure 17 | Transfer characteristics for a hypothetical MOSFET, showing regions of positive and negative temperature coefficient

The resistance increase dominates at high currents, meaning that localized heating leads to lower currents. The threshold-voltage drop dominates at low currents, meaning that localized heating lowers the threshold voltage. This condition effectively turns on the device more, leading to higher currents and a risk of thermal runaway.

Consequently, for a given V_{DS} , there is a critical current below which there is a positive-feedback regime and a subsequent risk of thermal runaway. Above this critical current, there is negative feedback and thermal stability. This critical current

is known as the Zero Temperature Coefficient (ZTC) point.

This effect reduces the SOA performance for low currents and high drain-source voltages. The constant power line must be reduced as shown in region (5). For short switching events, this effect is insignificant. However, as the duration of the switching event becomes longer, for example to reduce electromagnetic interference, the effect becomes more important and potentially hazardous.

Voltage-limited region

The device is limited by its breakdown voltage V_{DS} which is shown in region (4). The quick reference data provides values for V_{DS} at temperatures of 25 °C and above. In the hypothetical MOSFET shown in Figure 16, the rating is 100 V. For the BUK7Y3R5-40H, the voltage is 40 V.

3.1.1 Safe operating area for temperatures above 25 °C

When reading from the SOA curves there are two main considerations:

1. The mounting base temperature is at 25 °C
2. The MOSFET is exposed to a rectangular power pulse

The SOA curves indicate the pulse power required to raise the MOSFET junction temperature, T_j , from 25 °C to its maximum rating of 175 °C, $T_{j(max)}$. The assumption being T_j is at the mounting base temperature $T_{mb} = 25$ °C when power dissipation begins.

Under DC conditions, where a product has been operating for some time (thermally soaked), T_j will be close to the mounting base temperature, T_{mb} .

Under high power short duration pulse conditions T_j , can be much greater than T_{mb} .

A reduction in MOSFET power handling capability results if the initial $T_{mb} > 25$ °C, so it is important to establish an accurate temperature for T_{mb} to determine T_j which is non-trivial activity.

The majority of automotive power applications thermally link the MOSFET mounting base via the PCB footprint and an electrically isolating barrier to a metallic mass (e.g. product housing) to act as a heatsink. Heatsink temperature T_{hs} is in turn thermally linked to the product's ambient temperature, T_{amb} , which may be 85 °C for in-cabin (inside the driver compartment) or 105 °C for under the hood (near and around the engine). In some automotive applications where, for example, the housing is mounted directly to the power train the customer may specify a temperature directly on the heatsink where $T_{hs} \geq 105$ °C.

Unless the offset relationship $T_{mb} > T_{amb}$ is well defined by thermal flow modelling and test verification, the designer can only estimate T_{mb} .

It is important to remember that in a product which has been operating for some time (thermally soaked) MOSFETs which have similar thermal linkages to the same heatsink will have a similar T_{mb} , whether the MOSFET is switched on or switched off.

Calculation to determine the rise in die temperature above mounting base temperature is given below, see Equation (8).

$$T_{j(rise)} = T_{j(max)} - T_{j(mb)} = P_{peak} \cdot Z_{th(t)} \quad [8]$$

Where:

P_{peak} is the peak power, as this is a rectangular pulsed waveform.

$Z_{th(t)}$ is the thermal impedance value between junction and mounting base for a pulse of t seconds duration.

Note: In DC applications, (where the MOSFET is not pulsed), use $R_{th(j-mb)}$ instead of $Z_{th(j-mb)}$. Generally, for pulses above 100 ms, Z_{th} is indistinguishable from R_{th} . Equation 8 assumes heating is uniformly spread across the whole die. A combination of higher V_{DS} with lower I_{DS} and pulse durations $\geq 100 \mu s$ can cause hot spotting (uneven heating) to occur known as the Spirito effect. Refer to TN00008 Section 5 (chapter 13 in this book) - Power and small-signal MOSFET frequently asked questions and answers.

3.1.1.1 Example calculations

Calculate the max DC I_{DS} for BUK7Y3R5-40H, with $V_{DS} = 10 \text{ V}$ at 25°C

Rewrite Equation (10) to bring out I_{DS} as the main subject (Power is substituted by $I_{DS} \times V_{DS}$). Since Equation (10) is being used for a DC situation, the $Z_{th(t)}$ parameter used in Equation (8) and Equation (9) is replaced by the R_{th} steady state condition.

$$T_{j(rise)} = I_{DS} \times V_{DS} \times Z_{th(t)} \quad T_{j(rise)} \quad [9]$$

$$\frac{T_{j(rise)}}{V_{DS} \times R_{th}} = I_{DS} \quad [10]$$

$$\frac{175 \text{ } ^\circ\text{C} - 25 \text{ } ^\circ\text{C}}{10 \text{ V} \times 1.3 \text{ K/W}} = 11.3 \text{ A} \quad [11]$$

When making these calculations always refer to the Safe Operating Area Curve for the device. The SOA curve for the BUK7Y3R5-40H is Figure 4 which can be found in Section 2.4.4. The intersection of $I_D = 11.3$ A and $V_{DS} = 10$ V occurs above the DC curve and therefore this condition exceeds device capability. The reason being heat distribution is non-uniform within the die. In other words hot spotting is present, otherwise known as the Spirito effect.

The BUK7Y3R5-40H SOA curve shows for a DC condition the Spirito effect for this device (the point at which a gradient change occurs) is evident at $V_{DS} = 0.94$ V for $I_D = 120$ A. As I_D reduces, the allowable V_{DS} increases and by $I_D = 11.3$ A the maximum permissible $V_{DS} = 4.4$ V. Thermal consideration are discussed further in Section 3.1.2.

3.1.2 Example using the SOA curve and thermal characteristics

Consider the following application during linear mode operation:

- $I_{pulse} = 20$ A
- $V_{pulse} = 30$ V
- $f = 2$ kHz
- $t_{pulse} = 100$ μ s
- $T_{amb} = 25$ °C

3.1.2.1 Calculation steps

The SOA curve (Figure 4) is initially checked to see whether any single pulse would cause a problem. Observing the SOA curve, it can be seen that the 20 A, 30 V pulse lies between the 100 μ s and 1 ms lines. This indicates that the pulse lies within acceptable limits.

The duty cycle for the pulses is now calculated using a frequency of 2 kHz for 100 μ s pulses. These values give a duty cycle of 0.2. The Z_{th} curve (Figure 5) indicates that for 100 μ s, the line with the duty cycle (δ) has a transient thermal impedance of 0.35 K/W.

The power dissipation for the square pulse is $20\text{ A} \times 30\text{ V}$, which equals 600 W. Using Equation (8), the temperature rise for the 100 μ s pulse is calculated as being $600\text{ W} \times 0.35\text{ K/W}$, which equals 210 K. With a starting temperature of 25 °C, the temperature rise results in a finishing temperature of 235 °C. As the MOSFET junction temperature must not exceed 175 °C, the MOSFET is not suitable for this application.

If the application requires a single pulse, then the curve shows that the transient thermal impedance for a 100 μ s pulse is 0.12 K/W. As a result, the temperature rise is $600\text{ W} \times 0.12\text{ K/W}$ which equals 72 K. The finishing temperature is then 97 °C for

a starting temperature of 25 °C. The device is able to withstand this, thereby confirming what the SOA curve already indicated.

3.1.2.2 Derating for higher starting temperatures

The example Safe Operating Area calculations were performed for a mounting base temperature of 25 °C. At higher mounting base temperatures, the SOA curves must be de-rated, as the allowed temperature rise in the junction is reduced. The allowed power of the pulse is reduced proportionally to the reduced temperature rise. For example, with a mounting base temperature of 25 °C, the allowed temperature rise is 150 °C. At 100 °C, the allowed temperature rise is half of that (75 °C). The allowed power is half of that allowed at 25 °C.

The allowed drain current is de-rated while the allowed drain-source voltage is maintained.

The I_D derating of the SOA curve at 100 °C is shown in Figure 18.

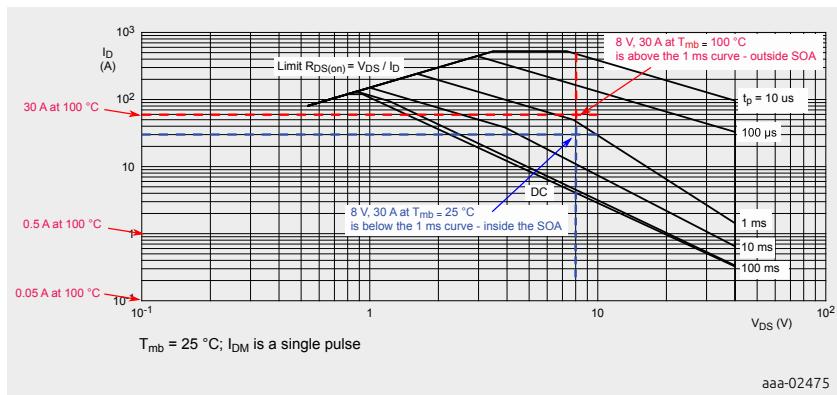


Figure 18 | SOA curve showing derating from $T_{mb} = 25$ °C to $T_{mb} = 100$ °C

Example:

Is a 1 ms pulse of 30 A and 8 V allowed at 100 °C?

See Figure 18, the intersection of the blue lines of the rectangular power pulse $I_D = 30 A * V_{DS} = 8 V$ below the 1 ms curve indicates that the device can safely handle this pulse with $T_{mb} = 25$ °C.

Power handling capability halves with $T_{mb} = 100$ °C. In Figure 18 the red text shows I_D at 100 °C is half the value at 25 °C.

The intersection of the red lines of the rectangular power pulse $I_D = 30 A * V_{DS} = 8 V$ above the 1 ms curve indicates the device cannot handle this pulse at $T_{mb} = 100$ °C.

4 References

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Chapter 2

Designing in MOSFETs for safe and reliable gate-drive operation

Application Note: AN90001

The MOSFET gate-source threshold voltage ($V_{GS(th)}$) and maximum gate-source voltage ($V_{GS(max)}$) are key parameters that are critical to the reliable operation of MOSFETs. The threshold voltage represents the voltage at which the MOSFET starts to turn on, whilst the maximum gate-source voltage is the maximum gate-source voltage that the MOSFET can withstand safely. $V_{GS(max)}$ ratings vary between suppliers and between MOSFETs, which can make it difficult to choose appropriate MOSFETs for the application. This chapter aims to provide the designer with enough knowledge to appreciate these differences and to select an appropriate MOSFET. We also present a new methodology demonstrating where higher $V_{GS(max)}$ ratings may be applied for Nexperia's automotive grade MOSFETs.

1 Introduction

The MOSFET can be considered as a voltage-controlled switch. Applying a voltage (V_{GS}) across the gate and source terminals enhances the MOSFET allowing current to flow through the MOSFET-channel between the drain and source terminals. $V_{GS(th)}$ is defined as the V_{GS} for a pre-defined drain current, commonly 1 mA. Increasing the V_{GS} further causes the MOSFET to become fully enhanced. This allows more current to flow for a given drain-source voltage. A fully enhanced MOSFET will also have achieved close to its rated on-state resistance $R_{DS(on)}$. Increasing the voltage beyond the full enhancement level will only result in a small reduction in $R_{DS(on)}$. Increasing the V_{GS} further to a level beyond the $V_{GS(max)}$ will have direct implications for the MOSFET's reliability. This could lead to destruction of the MOSFET. The design engineer can review the MOSFET data sheet to help ensure that the MOSFET's reliability is not impaired and that it operates as expected. The data sheet gives limits and guidelines, but often the design engineer needs more detail to select a MOSFET.

This chapter aims to bridge this gap. It will provide an overview of what is currently included in the data sheet concerning V_{GS} ratings and it aims to answer questions that may arise when designing in power MOSFETs.

In addition a brief introduction to the physics behind the V_{GS} ratings and the role of the gate-oxide is included. This will provide an appreciation of the reasoning behind the ratings and give confidence in the methodology employed by Nexperia to test, to qualify and to rate the MOSFET's gate-oxide capability.

An analysis of common Power MOSFET applications is also presented. This will highlight the demands imposed on the MOSFET gate-oxide by the application. Different applications have been analysed to develop a mission profile for the V_{GS} . This states what levels of V_{GS} the MOSFET will be exposed to, for how long and at what temperature. This information can then be used to select the correct MOSFET for the application, thus ensuring optimum and reliable operation.

2 Data sheet V_{GS} ratings

In Nexperia data sheets there are typically two main parameters concerning the gate-source voltages. The first being the V_{GS} threshold value or $V_{GS(th)}$. The second is the V_{GS} rating, which in this application note will be called $V_{GS\text{-max}}$.

Some MOSFET data sheets include a value for the plateau (Miller) voltage. This is the V_{GS} voltage during switching events. Its level is poorly defined as it depends on several interdependent electrical and environmental factors. It is not important for MOSFET selection or circuit design and will not be further discussed in this chapter.

2.1 V_{GS} threshold voltage - $V_{GS(th)}$

Figure 1 shows an example of data sheet $V_{GS(th)}$ values; it highlights the voltage required across the gate and source terminals to start to turn the MOSFET on. The conditions for which the $V_{GS(th)}$ is defined are specified here as the V_{GS} necessary for 1 mA of current to flow through the drain terminal. The Nexperia data sheet gives the $V_{GS(th)}$ for a range of temperatures. It also provides minimum and maximum values to account for process variation.

The $V_{GS(th)}$ is the start of MOSFET enhancement, an increase in V_{GS} is required to enhance the MOSFET further. Depending on whether a device is logic-level or standard-level, a MOSFET can be considered fully-enhanced (or fully on) when the V_{GS} is 5 V or 10 V respectively. By this point the MOSFET has achieved its rated $R_{DS(on)}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-sourced threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25^\circ\text{C};$ Figure 9; Figure 10	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55^\circ\text{C};$ Figure 9	-	-	4.5	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175^\circ\text{C};$ Figure 9	1	-	-	V

Figure 1 | V_{GS} threshold values for a Nexperia automotive grade standard level device

Symbol	Parameter	Conditions	Min	Typ	Max
$V_{GS(th)}$	gate-sourced threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25^\circ\text{C}$; Figure 9; Figure 10	1.4	1.7	2.1 V
		$I_D = 1 \text{ m}; V_{DS} = V_{GS}; T_j = -55^\circ\text{C}$; Figure 9	-	-	2.45 V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175^\circ\text{C}$; Figure 9	0.5	-	- V

Figure 2 | V_{GS} threshold values for a Nexperia automotive grade logic level device

Other differences between standard-level and logic-level devices can be observed in their threshold-voltage values (Figures 1 and 2). It is important to consider these values when selecting a MOSFET for an application. Two questions need to be answered to choose an appropriate MOSFET.

1. Can the gate-driver turn the MOSFET (fully) on?
2. Can the gate-driver turn the MOSFET (fully) off?

To answer these questions, it is necessary to take the worst case conditions in each circumstance. In order to assess question 1 we need to know what is the highest value of $V_{GS(th)}$ that the device may have. From Figures 1 and 2, we can see this occurs at the lower temperature limits. For a standard level device this can be as high as 4.5 V. If the gate-driver output is only 5 V, then a standard level device may not be suitable. This is because the MOSFET is only beginning to turn on and therefore may not operate correctly in the application. A logic level MOSFET with a maximum $V_{GS(th)}$ of ≤ 2.45 V would be more suitable.

It is important to note that $V_{GS(th)}$ has a Negative Temperature Coefficient (NTC): as the junction temperature increases, the V_{GS} for a given I_D decreases. If channel current flows because the V_{GS} is not low enough to drive the MOSFET fully OFF, I_D will increase as die temperature rises. This thermal runaway effect can ultimately cause MOSFET destruction.

Conversely, the designer must consider the upper temperature limit for turning the MOSFET off. At 175 °C a logic level device may conduct channel current at a $V_{GS} \geq 0.5$ V. The gate-driver may have a minimum output voltage of 0.6 V. This is not low enough to ensure that a logic level MOSFET is turned fully off. At $V_{GS} = 0.6$ V channel current could still flow. In this situation it is better to select a standard level device.

2.2 The maximum V_{GS} ratings - $V_{GS\text{-max}}$

$V_{GS\text{-max}}$ is the absolute maximum gate-source voltage that can be applied to the device. These values illustrated in Figures 3 and 4 conform to the International Electrotechnical Commission's IEC60134 document -“Rating systems for electronic tubes and valves and analogous semiconductor devices”. Referencing paragraph 4 of IEC60134 titled “Absolute maximum rating system” it states [1]:

“Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions. These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.”

This defines the worst case conditions and highlights the responsibility of the designer to ensure that the absolute maximum value is never exceeded. It does not explicitly place any obligations on the manufacturer in terms of long term reliability.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{GS}	gate-sourced voltage	$T_j \leq 175^\circ\text{C}$; DC	-20	20	V

Figure 3 | Maximum V_{GS} rating for a Nexperia automotive grade standard level device

Symbol	Parameter	Conditions	Min	Max	Unit
V_{GS}	gate-sourced voltage	$T_j \leq 175^\circ\text{C}$; DC	-10	10	V
		$T_j \leq 175^\circ\text{C}$; Pulsed	[1] [2]	-15	15

Notice there is an additional pulsed value limited to an accumulated duration of up to 50 hours.

Figure 4 | Maximum V_{GS} rating for a Nexperia automotive grade logic level device

3 Life Testing

For automotive MOSFETs, AEC-Q101 qualification is required. AEC-Q101 is a list of endurance tests the MOSFET must pass. Each test takes a sample of MOSFETs and places them under various electrical stresses and temperatures. The sample size is a minimum of 77 MOSFETs; each endurance test is repeated 3 times on a different sample of 77 MOSFETs to represent a different process batch. Surviving the endurance tests grants the tested product type Q101 accreditation, allowing the MOSFET to be used in automotive applications [2]. This can be found on all Nexperia automotive qualified MOSFET data sheets (Figure 5).

BUK9Y3R0-40E
N-channel 40 V 3.0 mΩ logic level MOSFET in LFPAK56
11 November 2014 Product data sheet

1. General description

Logic level N-channel MOSFET in LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

Figure 5 | Front page of a typical Nexperia automotive data sheet, showing the MOSFET is automotive by highlighting that it is Q101 compliant

To qualify the $V_{GS\text{-max}}$ ratings for Q101 the devices undergo a specified life-test procedure. The devices are placed in a chamber at the maximum rated temperature ($T_{j\text{max}}$) with gate biased at 100% of the data sheet maximum voltage rating for 1000 hours. These tests are performed by Nexperia to ensure that the data sheet ratings of $V_{GS\text{-max}}$ are within specification.

However, life-testing alone is inherently incapable of determining the actual capability of a MOSFET in terms of expected failed parts per million (ppm). In order to satisfy AEC-Q101 criteria no sample devices during the Q101 bias tests should fail. It is possible to extrapolate a failure rate from such data, but the maximum confidence it can provide is in the order of 11000 ppm (based on zero fails in a population of 240 devices under test and using a confidence interval of 95%). With this level of confidence it is not trivial to determine what to specify as the maximum voltage rating. Especially when in addition, Nexperia's own requirements target a sub 1 ppm defectivity level.

To achieve sub-ppm levels Nexperia has developed its own additional testing methodology. Using this, Nexperia can confidently rate the devices to satisfy the AEC-Q101 criteria, while also achieving sub 1 ppm defectivity rates (3). In order to understand this methodology an explanation of the role of a MOSFET's gate-oxide is required and is detailed below.

4 The Gate-oxide

The methodology to determine and qualify the maximum V_{GS} rating of a device is based upon characterisation of the gate-oxide. This is the layer of oxide that insulates the gate polysilicon from the source of the MOSFET and is critical to its operation. Figure 6 shows the location of the gate-oxide in the MOSFET.

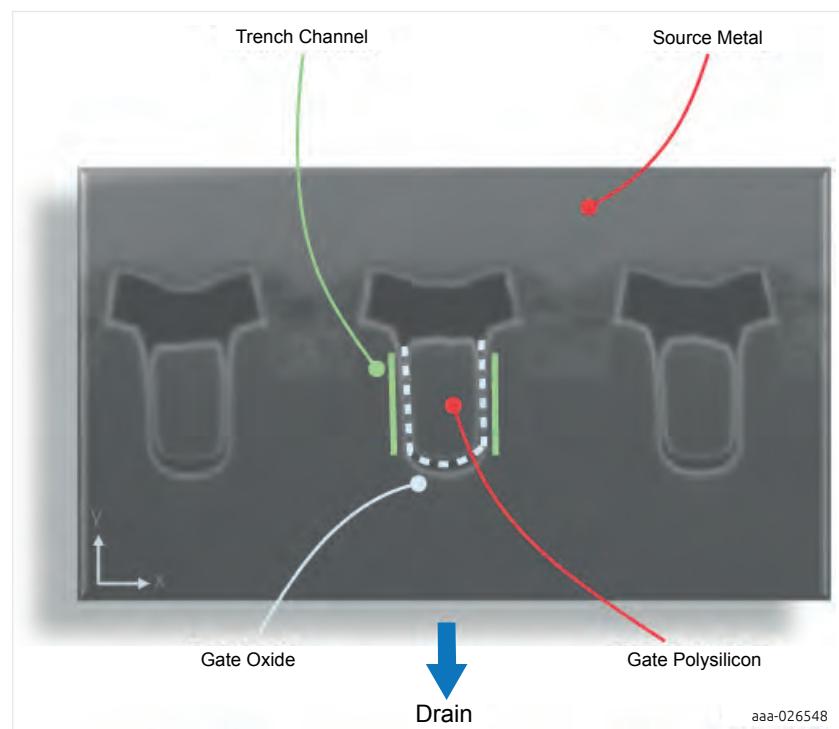


Figure 6 | Cross-section of a power MOSFET at approximately 25,000 magnification showing where the MOSFET channel forms and the location of the gate-oxide. The gate-oxide is present both sides of the trench and a channel forms next to both oxides. Current flows vertically from Drain to Source through the MOSFET channel.

When designing power MOSFETs, there are two conflicting constraints with respect to the gate-oxide thickness. Achieving a low $R_{DS(on)}$ at a low applied level of V_{GS} requires a thin gate-oxide, conversely withstanding high maximum V_{GS} requires a thick gate-oxide. In most cases, both requirements can be met and gate bias life testing can be performed at 100 % of the absolute maximum rating. However, there are some instances where this is not possible. Logic level devices are designed to provide a guaranteed $R_{DS(on)}$ at $V_{GS} = 5$ V. This implies a need for a gate-oxide that is thinner than for a standard level device. Consequently a logic-level gate-oxide is not capable of achieving the same maximum $V_{GS\text{-max}}$ rating as a standard-level gate-oxide. For Nexperia's automotive MOSFETs, this is typically 10 V logic-level and 20 V for standard-level devices at the maximum rated temperature, typically 175 °C.

However, caution should be exercised when comparing other manufacturers' data sheets. The $V_{GS\text{-max}}$ rating is not always given at the maximum rated temperature; instead it is often given for 25 °C. The rating given for a temperature of 25 °C may be higher than one given for 175 °C. This will make that MOSFET appear more capable on first review. Because MOSFET gate-oxide reliability decreases with increasing temperature, Nexperia's data sheets show the capability of the MOSFET at maximum rated junction temperature.

Exceeding the $V_{GS\text{-max}}$ rating for the gate-oxide does not mean the device will immediately fail in the application. Applying a V_{GS} to a MOSFET will develop an electric field across the internal gate-oxide (E_{ox}). The oxide electric field strength is a function of oxide thickness (T_{ox}) and V_{GS} .

$$E_{ox} = V_{GS} / T_{ox}$$

If the oxide electric field strength reaches a sufficiently high level, the gate-oxide insulation will break down and will be destroyed. However, for electric field strengths below this critical value the gate-oxide may degrade over time and ultimately fail. The rate at which this occurs depends on both the operating-temperature and the strength of the electric field within the gate-oxide. Expected oxide life-time decreases with increases in either temperature or oxide electric-field stress.

Gate-oxides need to be rated to survive for operating periods of not less than 10 years. Testing for 10 years to assess the reliability of the gate-oxide is not practical. Nexperia performs life tests under accelerated conditions to achieve quicker test results. For assessing the gate-oxide, Nexperia places a group of MOSFETs with known gate-oxide thickness under high temperatures and high oxide field strength. The MOSFETs will therefore degrade much quicker than can be expected in the application. The MOSFETs are monitored until the point of failure, which is observed as a low impedance measurement between the gate and source terminals. This is termed Time Dependant Dielectric Breakdown (TDDB).

Nexperia uses the test data from TDDB to correlate to other operating-temperatures and oxide field-strengths to determine the capability of the oxide in actual application operating conditions. This is applicable to MOSFETs with different gate-oxide thicknesses because the testing characterises oxide field-strength, not V_{GS} .

A gate-oxide production process aims to create a gate-oxide of consistent thickness throughout manufacture. However, in any real fabrication process variation will occur. This means the V_{GS} rating needs to be applicable to the MOSFET with the thinnest gate-oxide that leaves the factory. Production screens are in place that set a lower limit, which corresponds to the MOSFET with the thinnest gate-oxide. Using this value of gate-oxide thickness and the characterisation data from the accelerated TDDB tests, this MOSFET can now have its oxide rated for $V_{GS\text{-max}}$ and temperature for a given expected operating life.

For automotive MOSFET the operating requirement is outlined within AEC-Q101; 1000 hours at $V_{GS\text{-max}}$ and maximum temperature. Taking this profile into account, and knowing the thinnest oxide that can be supplied, Nexperia can confidently place $V_{GS\text{-max}}$ ratings in the data sheet.

Again, for further detail on the mechanics of gate-oxide wear out and Nexperia's methodology towards rating its gate-oxides please refer to [3].

5 Alternative operating profiles

The mission or operating-profile of a MOSFET in an actual application is rarely at the data sheet maximum temperature and at the maximum V_{GS} for 1000 hours as dictated by AEC-Q101. This combination is formulated as a compromise to allow realistic life-testing times that would protect automotive applications. The ultimate rating of a MOSFET $V_{GS\text{-max}}$ that meets AEC-Q101 may not meet the application requirements. For example the application may require 12 V V_{GS} but this exceeds the MOSFET of choice's 10 V rating, at first pass this MOSFET cannot be used in the application. However, if the operating profile of the application is outlined with greater detail it may be that the 12 V rating is required for temperatures less than 175 °C and for a cumulative lifetime duration of less than 1000 hours. Here the application criteria can be compared with the true capability of the oxide and therefore be confidently selected for the application.

This chapter assesses several common MOSFET topologies in order to provide an understanding of V_{GS} behaviour. From this it is possible to generate an estimate for what V_{GS} will be applied to the MOSFET and for how long; a V_{GS} profile. Using the V_{GS} profile along with operating-voltage profiles and temperature profiles a full mission profile can be created. An example is shown in Table 1. The mission profile can be used to assess the MOSFET's suitability for the application against the TDDB

data.

The first set of analyses presented considers steady state stress on the gate-oxide due to a constant gate-source bias from either an external gate-driver or as a result of the steady state voltages that appear on the gate and source terminals of a MOSFET. Further analysis attempts to estimate the contribution to gate stress from transient gate- source voltages. This could result from capacitive coupling through the Miller capacitance or conduction through the MOSFET body diode. Both require detailed analysis of the application to verify compatibility with the MOSFET features.

Table 1. Example MOSFET mission profile, showing the time spent in hours at a particular V_{GS} and MOSFET junction temperature

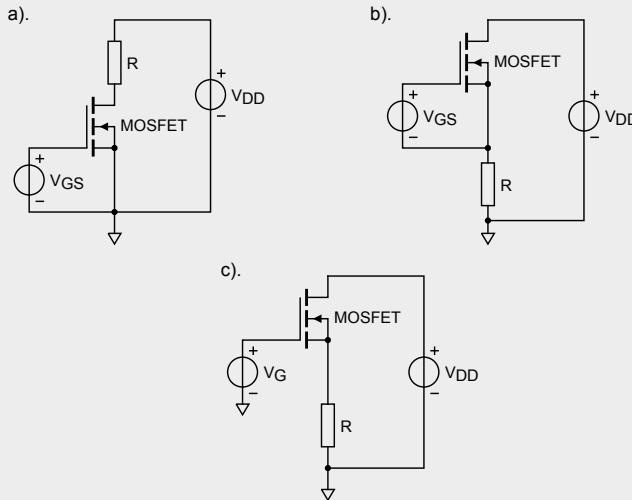
$V_{GS} =$	Time (hours)				
	$T_j = -40^\circ\text{C}$	$T_j = 25^\circ\text{C}$	$T_j = 80^\circ\text{C}$	$T_j = 105^\circ\text{C}$	$T_j = 125^\circ\text{C}$
-5 V	1	5	10	1	0
2 V	10	50	100	10	2
5 V	1000	2500	5000	50	10
10 V	100	200	300	100	5
20 V	2	10	5	2	1

5.1 Application assessments

This section assesses several common topologies featuring MOSFETs and focuses on the V_{GS} behaviour. This information will help to produce the mission profile as shown in Table 1.

5.1.1 Single MOSFETs

Starting with the three application topologies shown in Figure 7. Figure 7a and 7b can be considered similar in behaviour as they are both driven gate to source. However, Figure 7c shows the MOSFET being driven gate to ground. It is possible to drive the MOSFET in this manner by ensuring the gate voltage is higher than whatever voltage is currently at the source terminal. However, it is highly recommended not to do so as will become apparent throughout the discussion.



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Figure 7 | a) Low side MOSFET b) High side MOSFET driven Gate to Source c) High side MOSFET driven gate to ground

In Figure 7c, when a V_G is applied, first assumptions may be that the voltage across the load resistor will be close to V_{DD} due to the low on-state resistance of a MOSFET compared to the load. However, the V_{GS} of the MOSFET is $V_{GS} = V_G - V_S$, where V_S is the voltage developed across the load in this example. This means that as V_G rises so, will V_S thus reducing the overall V_{GS} across the MOSFET. The result is a MOSFET that is not fully enhanced and therefore taking a significant portion of the V_{DD} across its drain and source terminals. The MOSFET is now dissipating a considerable amount of power and operating in linear mode, which may have thermal runaway implications. In addition, the load may not behave as expected due to it no longer having the full V_{DD} across it.

In Figure 7a the MOSFET source and gate-driver supply are both grounded and therefore provides a true V_{GS} supply. Likewise in Figure 7b, now the gate-drive is able to float above the source voltage and apply the full drive to the gate-source terminals of the MOSFET. Both the circuits in Figure 7a and 7b the MOSFETs are easily turned fully on and can achieve the low $R_{DS(on)}$. This allows the full V_{DD} to be applied across the load and ensures correct operation of the application.

5.1.2 Half, Full and Three-Phase Bridges

Other application examples include half bridges and by extension full bridges and three phase bridges which can be found in DC-to-DC convertors and motor drives. Here, in any individual leg two MOSFETs are placed in series. When the MOSFETs are off the resistance across the drain-source terminals is not infinite and leakage paths exist. For simplification, these can be treated as resistances across the drain-source terminals. Referencing Figure 8 it can be seen that the V_{GS} on the high side (HS) MOSFET can be $-V_{DD}/2$. The time the MOSFET V_{GS} is at $V_{DD}/2$ V may be significant due to this occurring whenever the application is off and connected to the supply voltage. This will need considering in the mission profile and the MOSFET will need to be specified to meet this requirement.

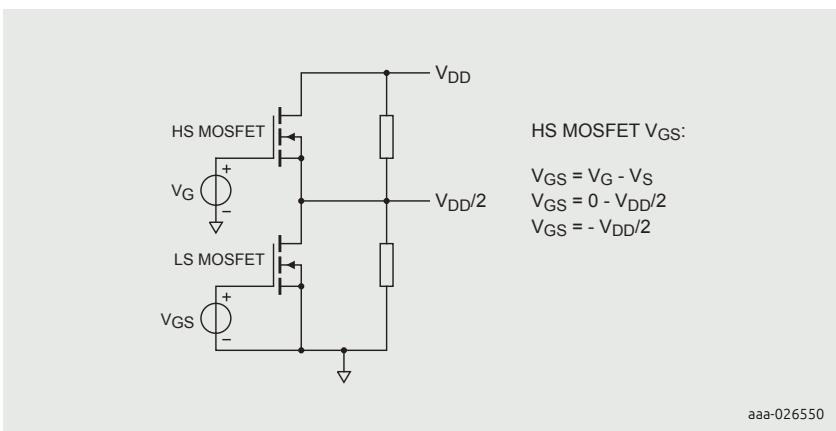


Figure 8 | Half bridge MOSFET configuration showing leakage paths and potential issues if driving High Side MOSFET with respect to ground

When the MOSFETs are driven with respect to ground the required gate-drive needs to be at least the required V_{GS} for the MOSFET summed with the maximum voltage at the MOSFET's source terminal. For example, an automotive application typically uses a lead acid battery. Potentially the application could see 18 V from the battery and therefore the same voltage may appear on the source terminal of the high side MOSFET. This means to drive a typical SL MOSFET a gate voltage of 28 V (18 V + 10 V) with respect to ground is required to ensure the MOSFET is fully enhanced. Now the gate-drive is fixed at 28 V. However, the battery voltage may be as low as 6 V. This means the V_{GS} will be 22 V (28 V - 6 V). For a SL MOSFET this is outside its safe operating limits and has the potential to reduce its reliability in the application.

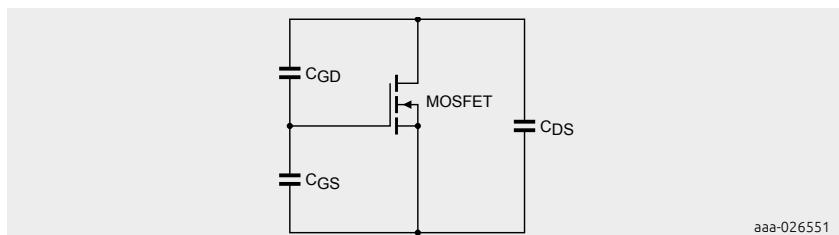
Within half bridges the extremes of the V_{GS} have been considered but the source voltage of the high side MOSFET does not depend solely upon the battery-voltage:

load conditions which are variable with temperature and supply-voltage result in not knowing accurately what the source-voltage will be during considerable periods of operation of the application. This makes it very difficult to assess the V_{GS} requirement of the MOSFET when driving them with respect to ground. It is preferred and advisable to have the gate- driver referenced to the source of the MOSFET and not ground. Now, when the source voltage changes the gate-drive will be referencing this and the V_{GS} will be controlled. However, even when driving the MOSFET with respect to source there are still times when the V_{GS} is not fully dictated by the gate-driver. An assessment of transient analysis is required next.

All the applications discussed and their V_{GS} behaviour have been assessed under steady-state conditions, the next few paragraphs take into consideration the dynamic behaviour whilst the MOSFET is switching or commutating currents. In the example figures already shown the gate-drivers have been idealised as perfect voltage sources. However, all gate-drivers will have output impedances and drive current limitations adding to the complexity of transient behaviour for the application. In addition to this the PCB layout will be a factor, with track impedances contributing to the application behaviour. It is beyond the scope of this application note to discuss best layout practices beyond noting that gate-drivers should be placed as close as possible to the MOSFET it is driving. Some of these issues have been addressed in application note AN11599 (chapter 3 of this book) - Using power MOSFETs in parallel.

The transient operation of the half bridge is now reviewed, here solely the case where the MOSFET is driven gate to source is considered. The load is inductive, representing half bridges (DC to DC convertors for example) and three-phase bridges (Brushless DC motors for example). The full operation of these applications is not considered but in each, during the switching of the MOSFETs, the considerations to the gate-drive are similar.

Before describing the application behaviour, it is important to note that all MOSFETs have parasitic capacitances that couple each of the terminals, gate, drain and source (Figure 9). They are C_{GS} , C_{GD} and C_{DS} and exist as part of the MOSFET structure, playing a critical role in the transient behaviour of MOSFETs and therefore the application.



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Figure 9 | Internal parasitic MOSFET capacitances

In half-bridges during an example transient event, one MOSFET is turned off and the second is turned on, this causes the switch node voltage to rise and fall. The switch node is where the source of the high side and the drain of the low side MOSFETs are connected. The dV/dt on the switch node can couple through the C_{GD} of a MOSFET and charge or discharge that MOSFET's C_{GS} , appearing as V_{GS} . Whether the V_{GS} is positive or negative depends on the sign of the dV/dt . It is the function of the driver to compensate for this change in V_{GS} by charging/discharging the V_{GS} to the set level. How effective the gate-driver is at this depends on a couple of factors, the rate of the dV/dt and how well the driver is coupled to the gate and source (how much impedance is between them). Again, being aware that the total impedance is a sum combination of package, resistance and inductances, trace parasitics and intentionally placed components (which have even more parasitics). This behaviour is shown in Figure 9. The consequences of this gate-bounce are biasing of the gate for a cumulative time which needs to be considered in any mission profile and worse, potentially causing cross conduction where both MOSFETs are on simultaneously.

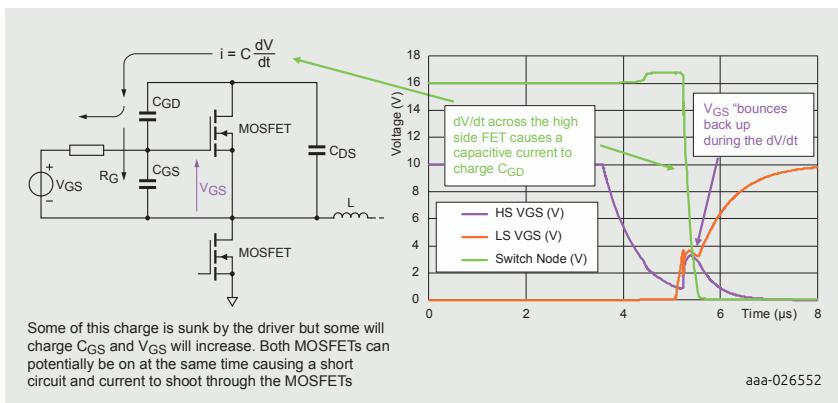


Figure 10 | Dynamic behaviour of a MOSFET half bridge

5.1.3 High side MOSFETs with Inductive loads

Other applications where V_{GS} behaviour may not be as first expected, are when driving inductive-loads. Take again the examples in Figure 7 but now replace the resistive-load with an inductive one. The difference in driving methodology, that is with respect to ground or to the source, could result in either the MOSFET operating in linear mode or entering avalanche respectively. Consider now the situation where the gate-drive is referenced to ground. Also assume there is sufficient drive on the gate to compensate for an increase in source voltage, thus allowing the MOSFET to be fully enhanced.

When the MOSFET is turned on current will increase through the inductor, and

energy will be stored in its magnetic field. Then the gate-driver is turned off, the inductor starts to demagnetise and produces a back-EMF in order to maintain current flow. As one end of the inductor is grounded this back-EMF appears as a negative voltage on the source. The voltage will continue to decrease until the V_{GS} is great enough such that the MOSFET is partially turned on, maintaining the inductive current flow. Here the MOSFET is in linear mode, the V_{GS} is somewhere between off and fully on and the V_{DS} is significant; remembering that the source is now negative. See Figure 11 for an illustration.

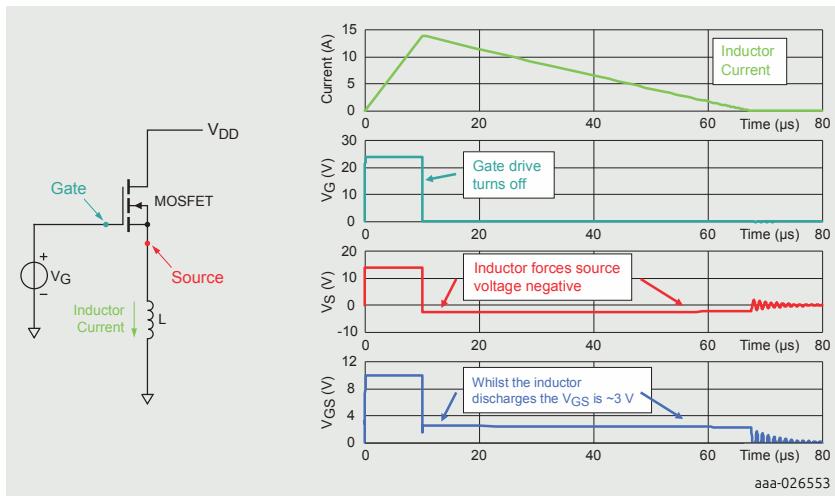


Figure 11 | Circuit and waveforms showing the V_{GS} behaviour whilst driving an inductive load and the gate of the MOSFET is driven gate to ground

Taking the previous example of driving an inductive load but with the gate being driven with respect to the source, the behaviour is similar until the MOSFET is turned off. Again the V_s will go negative until current flow is maintained, however the source is tied firmly to the gate by the driver which is operating at 0 V. No matter how negative the source goes (within operational limits) the MOSFET will stay off. Instead, the V_s will continue to decrease and therefore the V_{DS} will continue to rise. Ultimately the V_{DS} will reach the breakdown voltage of the MOSFET's internal body diode and avalanche (Figure 12). As with linear mode the power dissipation is considerable due to there being voltage and current present in the MOSFET, but avalanche is a preferable method of absorbing the inductive energy. Compared to linear mode, avalanche operation is better at sharing this power dissipation across the silicon die. Further information avalanche can be found in a MOSFET's data sheet and in more detail in application note AN10273 (chapter 4 of this book) - Power MOSFET single-shot and repetitive avalanche ruggedness rating.

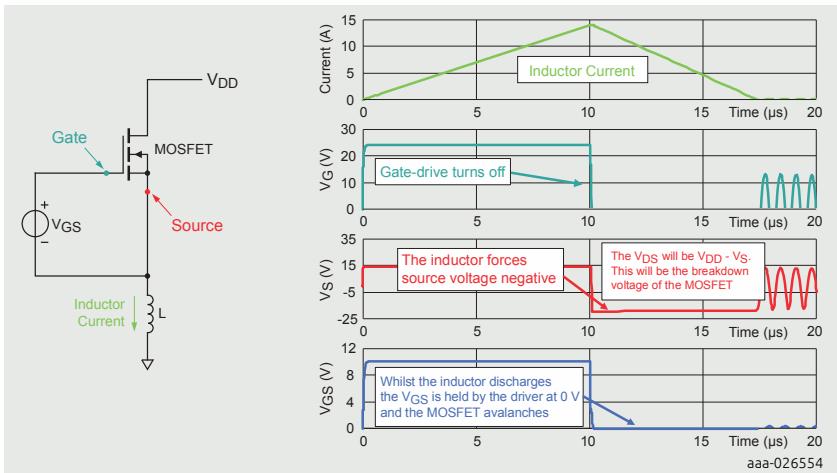


Figure 12 | Circuit and waveforms showing the V_{GS} behaviour whilst driving an inductive load and the gate of the MOSFET is driven Gate to Source

5.1.4 Motor Loads

One final application to be considered is driving motors with a single high side FET. Again the designer is recommended to drive the MOSFET with respect to ground to ensure full control of the MOSFET and application behaviour. Driving with respect to ground and the source voltage will be near V_{DD} due to motor back EMF; all the previous considerations to driving respect to ground apply.

6 Application assessment summary

This chapter has summarised some common application behaviours and their impact on the MOSFET's V_{GS} . The application note has shown that driving a MOSFET with respect to ground causes numerous issues and difficulties. These include operating in linear mode and not knowing what the V_{GS} may be at any point in time. This makes it difficult to formulate a mission profile to select the correct MOSFET. However, driving the gate with respect to source does not remove all of the issues; there are transient events that can induce positive or negative voltages on the V_{GS} that are not fully controlled by the gate-driver. We are still short, however, from producing the mission profile to ensure the correct selection of a MOSFET. The correct MOSFET should not be over-specified and should still operate reliably in the application for its intended life. We now need to create a mission profile.

7 Creating a mission profile

An example mission profile is shown in Table 1, it is a distribution of V_{GS} voltages at a range of temperatures and for how long. However, before generating a profile, several pieces of information need to be gathered. These include but are not limited to:

- How long the application is in operation
 - On and Off times
 - Possible fault conditions
- The distribution of operating temperatures
- The distribution of supply voltages

Along with an understanding of the application as outlined in the previous sections, this information can be used to create a mission profile. The mission profile can be assessed against the TDDB data for a given MOSFET, thus determining the MOSFET's suitability for the application.

7.1 Example – Full H-bridge motor drive

An example automotive application is brushed Direct Current (DC) motors such as windscreen wiper motors or seat control motors. For this worked example the MOSFETs are driven with respect to their source terminals and not to ground.

The first part of the exercise is to gather information on how long the application will be operating for. This information can then be translated into how long the MOSFETs are on for and therefore how long they will have a V_{GS} applied. In this instance it is common for the Original Equipment Manufacturer (OEM) to stipulate the usage profile of the system and it may look like (Table 2).

Table 2: Number of motor operations and the total time spent in operation

Operations	Total operation time at 0.5 s per actuation (hours)
180,000	5

Other times when there may be a voltage present at the gate of the MOSFET is when the engine is off but the electronics are on. In the case of the motor, the two high side MOSFETs may be switched on to brake the motor. This time will add cumulatively to the mission profile (Table 3).

Table 3: Battery voltage whilst the engine is off and the time spent at this voltage whilst the electronic systems are connected to the battery

V _{GS} (V)	Time (hours)
12.5	6,000

Table 3 provides the first piece of information required to build our V_{GS} profile. We need to convert the information in Table 2 into the same. To do so, we need to know the V_{GS} the MOSFET will be driven at. The V_{GS} may be set at 10 V by a power supply or alternatively the MOSFET may be driven directly by the battery voltage. The battery voltage will have its own distribution (Table 4). Using Table 2 and Table 4 we get Table 5.

Table 4: Battery voltage distribution of the life time of the application

Battery voltage	Distribution
14.5	77%
16	15%
17	5%
18	3%

Table 5: V_{GS} profile based on battery voltage distribution and application operation time, including the V_{GS} applied to the MOSFET whilst the engine is off

V _{GS} (V)	Time (hours)
12.5	6000
14.5	19.25
16.0	3.75
17.0	1.25
18.0	0.75
20.0	0.00825

Table 5 is now a V_{GS} profile, it shows the time spent at each V_{GS} value. However, it is missing the temperature profile to make it into a full mission profile to be assessed against the TDDB data. To generate a temperature profile the OEM and the application designer need to work together. Remember that the MOSFET may be operating a little hotter than its ambient (due to self-heating) so engineering margin may need to be added. An example is shown in Table 6.

Table 6: Ambient and junction temperature distribution of the expected life time of the application

The junction temperature is arbitrarily increased by 50 °C, this can be changed based on engineering judgment or calculation when better informed of the systems operational parameters.

T_{amb} (°C)	T_j (°C)	Distribution
-40	10	6%
23	73	20%
40	90	65%
75	125	8%
80	130	1%

Table 5 contains the V_{GS} values, and Table 6 has the temperature distribution. These two together contain the information to make Table 7, the full V_{GS} profile. For example, for 6% of the time the MOSFET junction temperature is at 10 °C. By multiplying the hours at each V_{GS} (from Table 5) by 6% the $T_j = 10$ °C column in Table 7 is populated. It may be the case that the higher V_{GS} voltages only occur at the lower temperatures. The profile in Table 7 will need to be updated to reflect this but can only be done so by the application designer working with the OEM.

Table 7. Full mission profile showing the time in hours for a given V_{GS} voltage and MOSFET junction temperature

V_{GS} (V)	Time at V_{GS} and Temperature (hours)				
	$T_j = 10^\circ\text{C}$	$T_j = ^\circ\text{C}$	$T_j = 90^\circ\text{C}$	$T_j = 125^\circ\text{C}$	$T_j = 130^\circ\text{C}$
12.5	360	1200	3900	480	60
14.5	1.155	3.85	12.5125	1.54	0.1925
16	0.225	0.75	2.4375	0.3	0.0375
17	0.075	0.25	0.8125	0.1	0.0125
18	0.045	0.15	0.4875	0.06	0.0075

The profile in Table 7 shows that for a time the MOSFET will see a V_{GS} of 18 V at elevated temperatures. Using solely the datasheet ratings a logic-level MOSFET's $V_{GS\text{-max}}$ rating of 15 V would seem to exclude it from use in this application. However, working with Nexperia to compare the profile to the logic level MOSFETs TDB data it can be shown that the MOSFET is more than capable of operating reliably in the application. This is because the time spent at these conditions is short.

Once the design engineer has generated a V_{GS} mission profile they are encouraged to contact their local Nexperia representative to receive support. Working with Nexperia, the profile can be assessed against the TDB data and a suitable MOSFET can then be suggested.

8 Summary

The gate-source lifetime and the gate-source turn-on voltage are highly dependent on temperature so one needs to be careful in comparing datasheets from different suppliers where the stated temperature conditions for the gate-source voltages are different.

For devices that do not see the maximum gate-voltage at maximum temperature throughout their intended life, Nexperia has a methodology to provide a better assessment of the required gate-oxide rating for such an application. This would often allow better performance in other parameters without compromising reliability in the application.

This does require the so-called mission profile of the MOSFET in the application, as described in this chapter.



9 References

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3. A methodology for projecting SiO₂ thick gate oxide reliability on trench power MOSFETs and its application on MOSFETs V_{GS} rating. Efthymiou, E, Rutter, P and Whiteley, P. 2015, Microelectronics Reliability.

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Chapter 3

Using power MOSFETs in parallel

Application Note: AN11599

Increasing the capability of a MOSFET switch element by using several individual MOSFETs connected in parallel can be useful. However, when designing switch elements careful consideration of the circuit requirements and the MOSFET characteristics and behavior must be applied. This chapter explores some of the problems that can be experienced when several MOSFETs are operated in a paralleled group. It also suggests ways to avoid the problems and minimize their effects.

1 Introduction

One much publicized benefit of power MOSFETs (compared to other semiconductor devices) is that it is easy to parallel them to create a group with increased capability. Although this feature is superficially true, there are several potential problems that can catch out the unwary circuit designer.

A MOSFET consists of a group of paralleled ‘cells’ fabricated on the surface of a silicon die. All the cells are created at the same time under the same conditions. When the MOSFET is fully enhanced and conducts channel current, the temperatures of all the cells are very similar. As the cells are structurally and thermally closely matched, they share current and power well and the parameters of the MOSFET can be well-defined.

There is a range of values for the parameters of the MOSFET dies on a wafer. There is a wider range for MOSFET dies on different wafers in the same production batch. The range is even wider for all batches even though the MOSFETs are the same type. MOSFETs with parameter values outside the data sheet limits are rejected.

The MOSFETs in a paralleled group should all be the same type, but their parameters could be anywhere within the data sheet range. Their die temperatures are unlikely to be the same. Consequently their power sharing is not perfect.

This chapter contains guidelines on how to design a group of MOSFETs to get the best performance from them. The design must accommodate MOSFET variations within the data sheet limits. It must also allow for MOSFET parameter variations over the range of electrical and environmental conditions. If all the MOSFETs in the group work within their safe maximum limits, the paralleled group of MOSFETs operates reliably.

It is technically and commercially undesirable to have to select MOSFETs and it should be unnecessary. The circuit should be designed to accommodate any MOSFET within the worst case $R_{DS(on)}$ range.

The key data sheet limit which must not be exceeded is the maximum junction temperature $T_{J(max)}$ of 175 °C.

2 Static (DC) operation

This situation is the simplest condition where current flows through a group of paralleled MOSFETs that are fully enhanced (switched ON). A proportion of the total current flows through each MOSFET in the group. At the initial point of turn on, the die temperatures of all the MOSFETs in the group are the same. The drain current I_D flowing in each MOSFET is inversely proportional to its $R_{DS(on)}$ (the drain-source voltage V_{DS} across all the MOSFETs is the same).

The MOSFET with the lowest $R_{DS(on)}$ takes the highest proportion of the current and dissipates the most power (power dissipation $P = V_{DS} \times I_D$).

All the MOSFETs heat up, but the MOSFET with the lowest $R_{DS(on)}$ heats up most (assuming the $R_{th(j-a)}$ of all the MOSFETs is the same).

MOSFET $R_{DS(on)}$ has a positive temperature coefficient. $R_{DS(on)}$ increases as T_j increases. The die temperatures and $R_{DS(on)}$ values of all MOSFETs in the group rise, but the die temperature of the lowest $R_{DS(on)}$ MOSFET increases disproportionately. The effect of this behavior is to redistribute the current towards the other higher $R_{DS(on)}$ MOSFETs in the group.

Stable thermal equilibrium is reached after a period of operation. The lowest $R_{DS(on)}$ MOSFET is the hottest, but carries a lower proportion of the current than it did initially.

The Positive Temperature Coefficient (PTC) of $R_{DS(on)}$ is a stabilizing influence that promotes power sharing between the MOSFETs in the group. However, as stated earlier the most important criterion is that the maximum junction temperature of any MOSFET in the group must not exceed 175 °C.

The cooling of each MOSFET in the group depends on its thermal resistance from junction to ambient. Die temperature influences the heat flow from adjacent MOSFETs. Rather than considering the thermal resistance paths between the MOSFET dies, the main influence is the temperature of the common heatsink. All the MOSFET mounting bases are bonded electrically and thermally to this heatsink.

The lowest $R_{DS(on)}$ MOSFET could be located anywhere in the group. The thermal resistance from mounting base to ambient of all the MOSFETs in the group should be as similar as possible and as low as possible. Cooling is optimised and independent of location.

This thermal resistance solely depends on the thermal characteristics and design of the assembly [Printed-Circuit Board (PCB) or heatsink] to which the MOSFET is thermally bonded.

Sometimes a value for $R_{th(j-a)}$ is given in data sheets but this parameter is of very limited value. It cannot be treated as a well-defined parameter because it also depends on other external factors such as PCB construction, PCB orientation and air flow. The only guaranteed thermal parameter is the thermal resistance from the MOSFET junction to mounting base $R_{th(j-mb)}$.

2.1 Worked examples for static operation

The worked examples that follow are based on the BUK764R0-40E.

Table 1: Thermal characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.82 K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a PCB	-	50	- K/W

A typical group of MOSFETs has a range of $R_{DS(on)}$ values. The distribution has a peak at around the typical data sheet $R_{DS(on)}$ value; none should have an $R_{DS(on)}$ higher than the data sheet maximum. The $R_{DS(on)}$ of about half of the samples is less than the typical value.

Minimum $R_{DS(on)}$ is not given in the data sheet, but a good estimate is

$$R_{DS(on)(min)} \approx R_{DS(on)(max)} - 2(R_{DS(on)(max)} - R_{DS(on)(typ)}) \quad [1]$$

The $R_{DS(on)}$ value range means that a group of typical MOSFETs is very unlikely to share power equally when they are operated in parallel.

The worst case would be when one of the MOSFETs has the minimum $R_{DS(on)}$ and all the others have the maximum $R_{DS(on)}$.

Modeling of the electro-thermal system is complex because its electrical and thermal characteristics are mutually dependent. However, an electro-thermally convergent Excel model can be used to estimate the performance characteristics of a paralleled group. As an example, in a worst case situation three BUK764R0-40E MOSFETs are connected in parallel; two have maximum $R_{DS(on)}$ of 4 mΩ. The other has a lower than typical $R_{DS(on)}$ of 2.6 mΩ.

The MOSFET with the lowest $R_{DS(on)}$ value takes the highest proportion of the current. It therefore has the highest power dissipation.

The target is to keep the junction temperature of the hottest MOSFET below 175 °C under worst case operating conditions.

These estimations are simplified illustrations. The thermal representation of the MOSFET group is less complex than a real application. In a real application, there are other factors such as neighboring components and orientation that would influence cooling. However, they show the approximate behavior of the group with two different $R_{th(j-a)}$ values.

The first scenario shows the system with the thermal resistance from junction to ambient for each MOSFET ($R_{th(j-a)} = 20 \text{ K/W}$; $T_{amb} = 125 \text{ }^{\circ}\text{C}$).

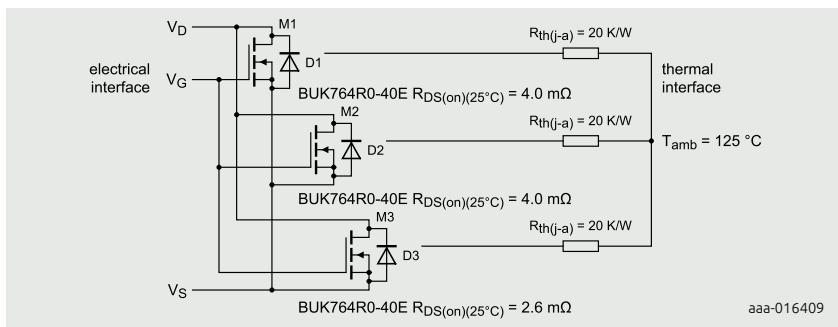


Figure 1 | Electrical and thermal schematic diagram of the three paralleled BUK764R0-40E MOSFETs

Table 2 shows the maximum safe limits of V_{DS} , I_D , P and T_j for all the MOSFETs at thermal equilibrium. At this point, the junction temperature of the hottest MOSFET is almost 175 °C.

MOSFET	V_{DS} [V]	$R_{th(j-a)}$ [K/W]	$R_{DS(on)}$ (25 °C) [mΩ]	Initial $R_{DS(on)}$ (125 °C) [mΩ]	Initial current I_D [A]	
M1	0.11	20	2.6	4.16	42.31	
M2	0.11	20	4	6.4	27.50	
M3	0.11	20	4	6.4	27.50	
Initial power P [W]	Initial power share [%]	Final $R_{DS(on)}$ [mΩ]	Final current I_D [A]	Final power P [W]	Final T_j [°C]	Final power share [%]
4.65	43.5	4.92	22.36	2.46	174	42.3
3.03	28.3	7.21	15.26	1.68	159	28.9
3.03	28.3	7.21	15.26	1.68	159	28.9

Total initial power $P(M1 + M2 + M3) = 10.70 \text{ W}$

Total final power $P(M1 + M2 + M3) = 5.82 \text{ W}$

The second scenario relates to the same electrical system, but with ideal thermal characteristics. The thermal resistance $R_{\text{th(j-a)}}$ of each MOSFET is 0.82 K/W. This situation corresponds to the ideal but unrealistic situation where each MOSFET is perfectly thermally bonded to an infinite heatsink (a heatsink with zero thermal resistance).

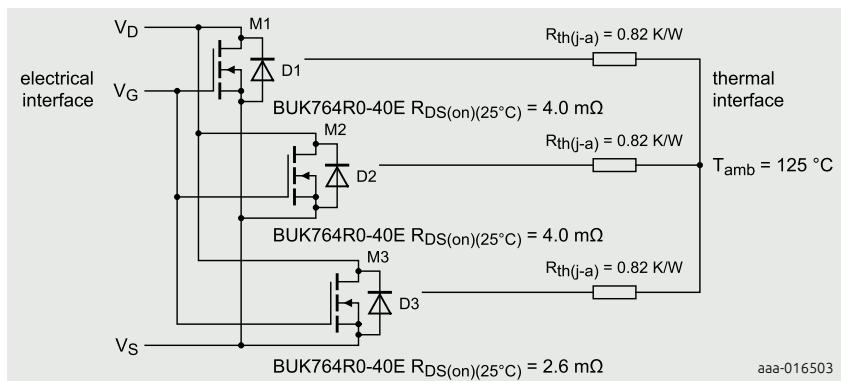


Figure 2 | Electrical and thermal schematic diagram of the three paralleled BUK764R0-40E MOSFETs with ideal thermal conditions

Table 3 shows the values of V_{DS} , I_{D} , P and T_j for all the MOSFETs at thermal equilibrium. At this point, the junction temperature of the hottest MOSFET is almost 175 °C.

Table 3: MOSFET maximum conditions for $R_{\text{th(j-a)}} = 0.82 \text{ K/W}$ and $T_{\text{amb}} = 125 \text{ °C}$

MOSFET	V_{DS} [V]	$R_{\text{th(j-a)}}$ [K/W]	$R_{\text{DS(on)}}$ (25 °C) [mΩ]	Initial $R_{\text{DS(on)}}$ (25 °C) [mΩ]	Initial current I_{D} [A]
M1	0.55	0.82	2.6	4.16	211.54
M2	0.55	0.82	4	6.4	137.50
M3	0.55	0.82	4	6.4	137.50

Table 3: continued...

Initial power P [W]	Initial power share [%]	Final R _{DS(on)} [mΩ]	Final current I _D [A]	Final power P [W]	Final T _J [°C]	Final power share [%]
116.35	43.5	4.92	111.79	61.48	174	42.3
75.63	28.3	7.21	76.28	41.96	159	28.9
75.63	28.3	7.21	76.28	41.96	159	28.9

Total initial power P(M1 + M2 + M3) = 267.60 W

Total final power P(M1 + M2 + M3) = 145.39 W

Note: This scenario is ideal and unrealistic. It is included to illustrate the benefit of reducing R_{th(j-a)} to maximize the usage of the MOSFET capabilities.

In practice, R_{th(j-a)} is always greater than R_{th(j-mb)}. The thermal bonding between the MOSFET mounting base and the heatsink is never perfect and an infinite heatsink does not exist in the real world.

In this case, the drain current (I_D) of the MOSFETs becomes the limiting factor (the data sheet maximum I_D is 75 A).

To optimize MOSFET utilization, the MOSFETs must be able to dissipate as much power as possible. At the same time, the junction temperature of the hottest MOSFET must remain below the maximum safe temperature of 175 °C.

The following conclusions can be drawn from Table 2 and Table 3:

1. It is beneficial to reduce R_{th(j-a)} as much as possible to optimize the MOSFET die cooling.
2. It is beneficial to reduce the maximum ambient temperature to increase the available thermal 'headroom'.
3. As a result of Table 2 and Table 3, it is clear that junction temperature difference between the MOSFETs depends only on their R_{DS(on)} values (assuming the R_{th(j-a)} for each MOSFET is the same).
4. When the paralleled (fully enhanced) MOSFETs heat up during use, their power distribution changes such that the cooler MOSFETs take a greater proportion of the power. This effect is due to the PTC of R_{DS(on)} and it acts to promote thermal stability.

3 MOSFET mounting for good thermal performance and power sharing

To get the most from the MOSFET group, the individual MOSFET should be mounted in a way that causes their mounting base temperatures to be as similar as possible and also as low as possible.

To realize this goal, the thermal resistance between each MOSFET (mounting base) and the mounting bases of all the other MOSFETs in the group should be matched and minimized. They should be mounted symmetrically and as close together as possible on a thermally conductive surface.

Heat flow can be considered to be analogous to electric current flow; so the thermal bonding points of the MOSFETs (usually the drain tabs) should be on a thermal 'ring main'. The low thermal resistance path allows heat to flow easily between the MOSFETs. When heat flows easily between all the MOSFETs in the group, their mounting base temperatures track together closely.

Note: This arrangement does not promote equal current sharing, but promotes better die temperature matching. The temperatures of all the MOSFETs in the group can rise more before the temperature of the hottest MOSFET reaches 175 °C. Hence the power dissipation capability of the group is maximized.

There are practical limits to the physical extent of the thermal ring main; ideally each MOSFET should be next to all its neighbors. This condition limits the group to two or three MOSFETs.

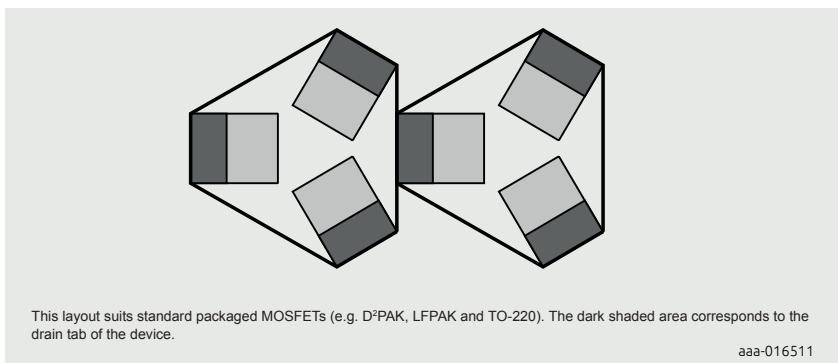


Figure 3 | A layout for six paralleled MOSFETs to promote good power sharing

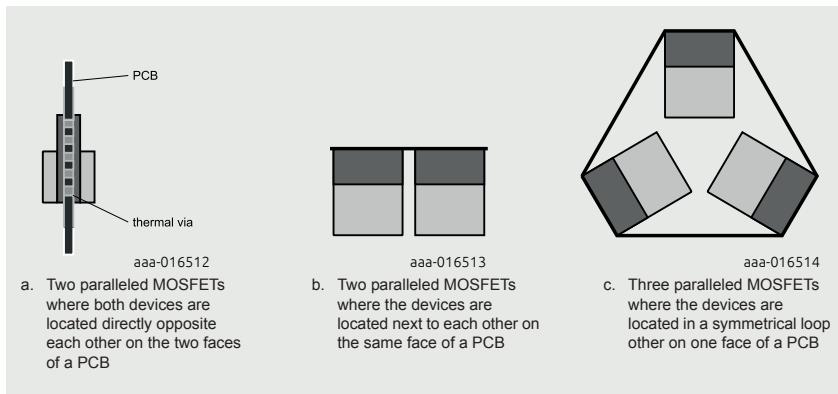


Figure 4 | Good layout arrangements for two paralleled MOSFETs and three paralleled MOSFETs

A good way to parallel a pair of MOSFETs is to locate them on opposite faces of a PCB forming a PCB ‘sandwich’ as in Figure 4a. Thermal vias between the copper ‘land’ areas on the PCB reduce the electrical and thermal resistances between their mounting bases.

To parallel a pair of MOSFETs on the same face of a PCB, they can be mounted next to each other as in Figure 4b.

A good way to parallel three MOSFETs is in a ring as in Figure 4c. This arrangement allows all the MOSFET sources in the group to be connected to a ‘star’ point. The electrical and thermal paths between the MOSFET drains match due to their symmetrical connections to the drain loop.

Minimizing and matching the electrical impedances in the source paths is more important than matching the electrical impedance in the drain paths. This difference is because their gate drives are related to the sources. Good impedance matching in both drain and source is more important in high frequency switching circuits.

If similar electrical and thermal matching can be achieved, larger paralleled groups could be considered. Groups of more than four or five become unwieldy so grouped sub groups should be used.

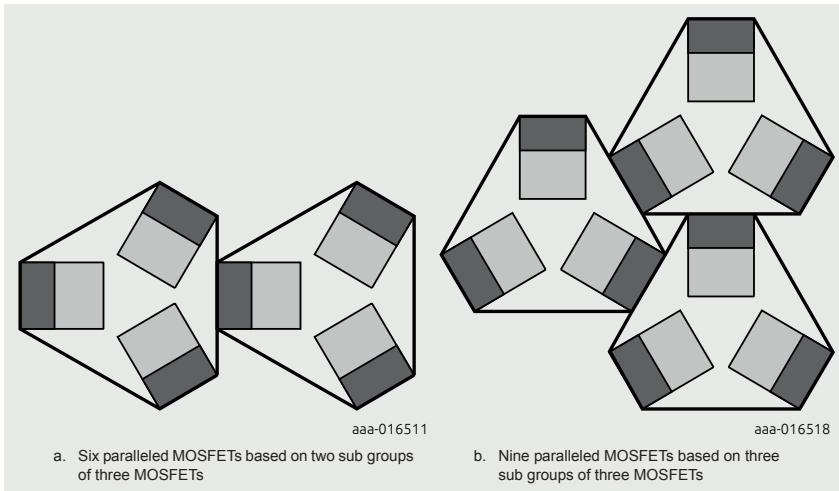


Figure 5 | Layouts using sub groups of three MOSFETs

In this group of 9 (3 groups of 3), there is a natural drain star point at the center of the group. There are separate source star points at the centers of each sub group. The source star points can be connected on a layer of a multi-layer PCB.

There is a compromise between optimizing layout for power sharing and maximizing PCB usage.

Electrically and thermally optimised layouts always use more PCB area than the minimum possible, but utilization of MOSFET capability should be better. Areas of PCB that are unoccupied by MOSFETs or gate drive components are useful for thermal interfaces with heat sink or cooling air.

4 Power sharing in dynamic operation [pulse and Pulse Width Modulation (PWM) circuits]

Many MOSFET circuits are designed to operate in systems where they are switched repetitively (such as DC-to-DC converters). Paralleled MOSFETs can be used as the switching elements in the system, but in addition to the guidelines set out for optimal steady state power sharing. Some additional points must be considered so that the MOSFETs share current during the switching transitions.

Good circuit and layout design is important. It influences the proportion of current carried by each MOSFET in the group during and after the switching event.

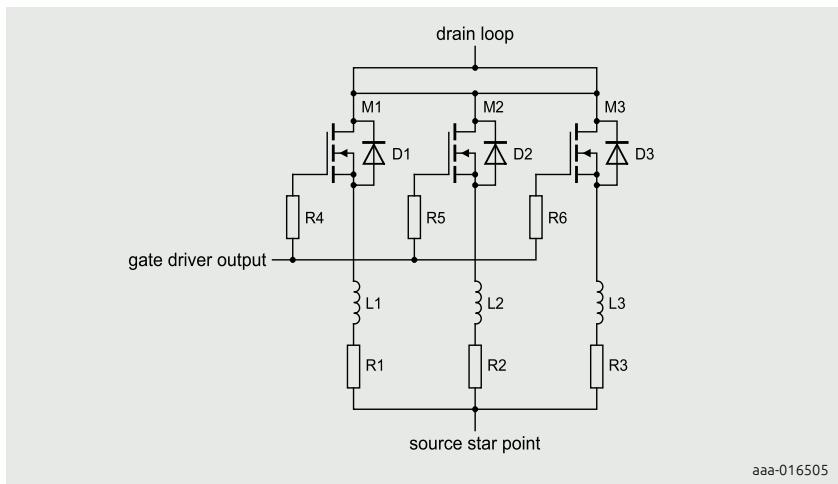


Figure 6 | Schematic diagram showing the stray source inductances and source resistances

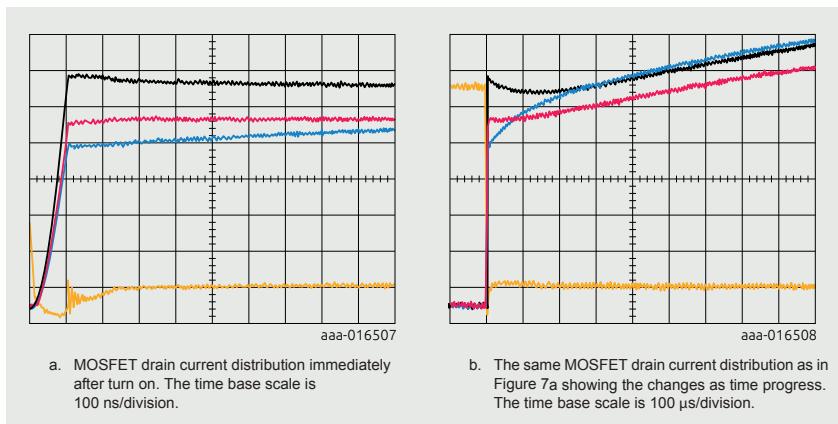


Figure 7 | Oscilloscope plots showing the MOSFET drain currents (black, red and blue) and drain source voltage (yellow) after turn on

Figure 7a and Figure 7b show how the current distribution in three paralleled MOSFETs initially depends on the source inductances in the MOSFET current paths, namely L_1 , L_2 and L_3 . As time progresses the resistances in the MOSFET current paths, namely $R_{DS(on)} + R_1$, $R_{DS(on)} + R_2$ and $R_{DS(on)} + R_3$ determine the current distribution.

The same principles hold about impedance matching of the current paths to the MOSFETs in the group. In this case, it is more important for the rates of change of

current in the MOSFETs to match. The source inductances are the key impedance as they affect the gate-source voltages (gate drives) of the MOSFETs in the group.

This effect dominates more in high frequency and short duty cycle applications (e.g. switched-mode power supplies). It may be insignificant in lower frequency applications such as motor drives.

5 Partially enhanced (linear mode) power sharing

If a group of MOSFETs must operate in linear (partially enhanced) mode, great caution is needed. MOSFETs simply paralleled together as they are for fully enhanced conduction are very unlikely to share power or current well.

This behavior is due to the Negative Temperature Coefficient (NTC) of gate threshold voltage $V_{GS(th)}$. As the group of MOSFETs starts to enhance, the MOSFET with the lowest $V_{GS(th)}$ starts to conduct channel current first. It dissipates more power than the others and heat up more. Its $V_{GS(th)}$ decreases even further which causes it to enhance further.

This unbalanced heating causes the hottest MOSFETs to take a greater proportion of the power (and get even hotter). This process is unsustainable and can result in MOSFET failure if the power is not limited. Great care is needed when designing paralleled power MOSFET circuits that operate in the partially enhanced (linear mode) condition.

If all the MOSFETs in the group operate within their Safe Operating Area (SOA), they work reliably. The SOA must be adjusted for the worst case mounting base temperature that occurs in the application. Remember that the data sheet SOA graph applies only if the MOSFET mounting base temperature is 25 °C or less.

Adding external source resistors (R1 to R4 in the schematic; see Figure 8) provides the negative feedback needed for stable operation. The gate-source voltage applied to $V_{GS}(M1) = V_G - I_D(M1) \times R_1$.

If the MOSFETs must also operate in fully enhanced mode (e.g. in 'Hot Swap' or 'Soft Start' applications), the inclusion of these resistors is an efficiency disadvantage.

As the MOSFET channel current increases, its gate drive voltage reduces.

As the MOSFETs are operating in partial enhancement (where MOSFET $R_{DS(on)}$ is not important), there is no adverse effect caused by including these resistors. If the MOSFETs must operate in both modes (as with active clamping after fully enhanced conduction), the inclusion of source resistors does have a negative impact.

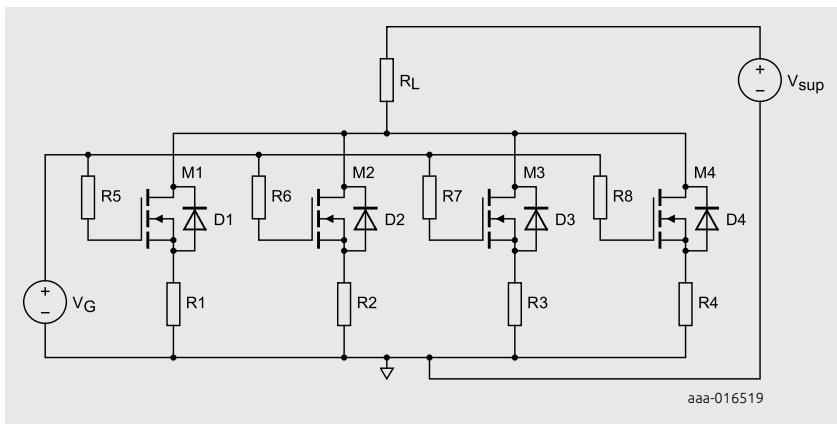


Figure 8 | Schematic diagram of a group of four paralleled MOSFETs intended to operate in linear mode

MOSFETs developed specifically for linear mode operation are available from Nexperia. They can simplify the design of paralleled groups of MOSFETs intended for linear mode operation.

6 Gate drive considerations

It is preferable to fit low value gate resistors between the gate driver and the gate of each MOSFET in the group.

Their main function is to decouple the MOSFET gates from each other so they all receive similar gate drive signals. Without these resistors, at turn on the Miller plateau of the MOSFET with the lowest threshold voltage would act to clamp the gate-source voltages of the other MOSFETs in the group. This clamping effect tends to inhibit and delay the turning on of the other MOSFETs in the group. At turn off a similar process occurs.

Without these resistors, the MOSFET with the lowest threshold voltage would switch on first and switch off last. The consequences of this effect may be insignificant in low frequency high duty cycle applications. In higher frequency PWM applications, it could cause a significant power imbalance between the MOSFETs. Positive feedback also occurs in this case which increases the imbalance and could ultimately cause MOSFET failure.

Gate resistors also help to damp out oscillatory transients on V_{GS} . They also swamp any effects caused by variations in the internal gate resistance $R_{G(int)}$ of the MOSFETs.

6.1 Should individual gate drivers be used for each MOSFET in the group?

Using individual gate drivers for each MOSFET in the group is usually unnecessary. They may be necessary in applications where fast switching of a large group of large die MOSFETs is needed. Here the MOSFETs should be arranged in smaller sub groups, each sub group driven by an individual gate driver. Care should be taken to balance the circuit so the propagation delays of all the gate drivers are similar. This matching ensures that the switching of all the MOSFETs in the group is synchronized. Usually it is sufficient to drive the gate of each MOSFET in the group from the same gate driver. However, it is important to have a gate resistor between the gate driver output and the gate of each MOSFET as mentioned earlier.

7 MOSFET packaging considerations for paralleled groups

Conventionally packaged surface-mounted MOSFETs (DPAK and D²PAK) are the most widely available types so they are considered first for paralleled groups. However, KGD and LFPAK (power SO8) MOSFETs could offer better solutions.

7.1 Bare die (KGD) MOSFETs

These MOSFETs offer the densest and most flexible options for paralleled groups; they are designed to suit a specific application. The die aspect ratio and gate pad location can be designed specifically to suit the application. More source wire bonds can be fitted to the die than can be fitted in a conventionally packaged MOSFET, so overall $R_{DS(on)}$ can be reduced. Maximum drain current can be increased to achieve better performance from a paralleled group of MOSFETs. Special manufacturing facilities are required for KGD assembly.

7.2 LFPAK MOSFETs

The power SO8 (LFPAK) MOSFETs offer the opportunity to manufacture the paralleled MOSFET circuit conventionally. Higher component density and power capability are possible (approaching that of KGDs). The connections to the source and gate are made using copper clips which give better electrical and thermal performance than aluminum wire bonds in conventional packages.

8 Inductive energy dissipation in paralleled MOSFETs

8.1 Avalanche - low side MOSFET group driving a high side inductive load

If the group of paralleled MOSFETs is driving an inductive load, energy stored in this load must be safely dissipated when the current is switched off. A good way to manage this energy is to connect a ‘freewheel diode’ across the load; see Figure 9. Current flowing in the MOSFET channel diverts into the diode when the MOSFETs switch off and the energy is dissipated in the circuit resistances. However, it is not always possible and energy must then be dissipated safely in the MOSFETs.

If the battery polarity (V_{sup}) is reversed, the low impedance path through the freewheel diode and the body diode can carry large damaging currents. Freewheel diodes are often not used for this reason.

When the group of MOSFETs is switched off, the back e.m.f. from the inductive load may be high enough to cause the drain-source voltage across the group of MOSFETs to exceed the drain-source breakdown voltage $V_{(\text{BR})\text{DSS}}$ of one of the MOSFETs. It likely that MOSFETs in the group have a range of $V_{(\text{BR})\text{DSS}}$ values (even though they are the same type). The current then flows through the body diode of the MOSFET with the lowest $V_{(\text{BR})\text{DSS}}$ in reverse (avalanche) conduction. This condition causes high-power dissipation and temperature rise in the MOSFET die ($P = I_D \times V_{(\text{BR})\text{DSS}}$). If the maximum 175 °C junction temperature is exceeded, the thermal stress on the die could degrade or destroy the MOSFET.

In the worst case, all the current which was flowing through the group of MOSFETs could be diverted into the body diode of one MOSFET in the group. If this scenario is possible, it is vital that a single MOSFET in the group can safely handle the total avalanche current under worst case thermal conditions. $V_{(\text{BR})\text{DSS}}$ has a positive temperature coefficient which tends to redistribute the current towards other MOSFETs with higher $V_{(\text{BR})\text{DSS}}$ values.

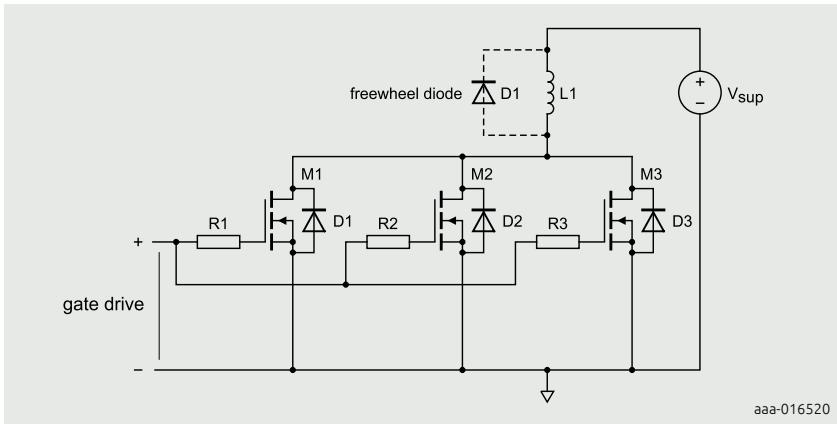


Figure 9 | Low side MOSFET group driving a high side inductive load

8.2 Active clamping - high side MOSFET group driving a low side inductive load

This configuration (see Figure 10) is often used in automotive applications. This topology is useful because the vehicle chassis can be used as the negative supply return path to the battery.

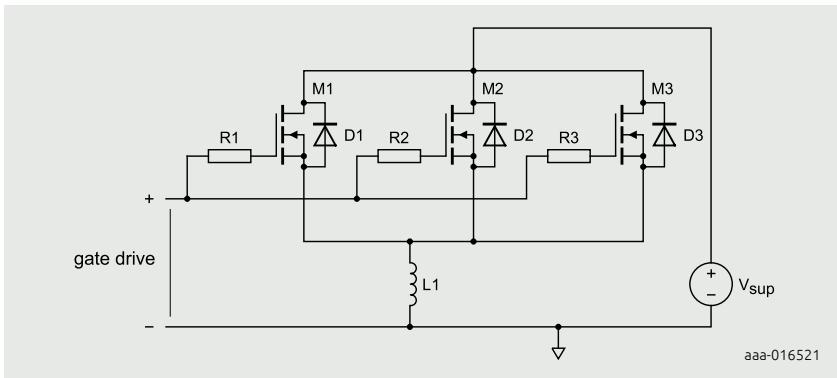


Figure 10 | High side MOSFET group driving a low side inductive load

In this circuit, the difference between the threshold voltages rather than $V_{(BR)DSS}$ spread determines where the load current flows. The MOSFET with the lowest threshold voltage conducts the greatest proportion of the current. The

drain-source voltage across the MOSFET group is $V_{\text{sup}} + V_{GS}$ and the power dissipation of the group is $(V_{\text{sup}} + V_{GS}) \times I_D$. As with the avalanche case, all the current (and hence all the power dissipation) could be diverted into a single MOSFET in the group.

This situation is worse than the avalanche case because MOSFET threshold voltage has a negative temperature coefficient. This characteristic tends to direct the current flow initially to the hottest MOSFET. This MOSFET then gets even hotter so that it retains the current.

9 Summary

1. It is better to use a single large MOSFET rather than a group of smaller MOSFETs.
2. The power capability of a group of n MOSFETs never achieves n times the power capability of a single MOSFET.
3. If it is necessary to use paralleled MOSFETs, use the lowest number possible as the basic group size (3 maximum).
4. If a larger number is needed, use a group of basic groups i.e. $4 = 2$ groups of 2; $6 = 2$ groups of 3.
5. The circuit layout is a very important factor determining how well a group of paralleled MOSFETs share power dissipation, particularly in higher frequency repetitive switching circuits.
6. Consider LFPAKs (for repetitive switching applications) because of their small size, good thermal performance and low package impedances.
7. Special care is needed when designing groups of MOSFETs that could operate in avalanche or active clamping mode.

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Chapter 4

Power MOSFET single-shot and repetitive avalanche ruggedness rating

Application Note: AN10273

1 Introduction

Power MOSFETs are normally measured based on single-shot Unclamped Inductive Switching (UIS) avalanche energy. This chapter describes in detail, the avalanche ruggedness performance, fundamentals of UIS operation and appropriate quantification method for the safe operating condition.

Electronic applications have progressed significantly in recent years and have inevitably increased the demand for an intrinsically rugged power MOSFET. Device ruggedness defines the capacity of a device to sustain an avalanche current during an unclamped inductive load switching event. The avalanche ruggedness performance of a power MOSFET is normally measured as a single- shot Unclamped Inductive Switching (UIS) avalanche energy or $E_{DS(AIS)}$. It provides an easy and quick method of quantifying the robustness of a MOSFET in avalanche mode. However, it does not necessarily reflect the true device avalanche capability (see Ref. 1, Ref. 2 and Ref. 3) in an application.

This chapter explains the fundamentals of UIS operation. It reviews the appropriate method of quantifying the safe operating condition for a power MOSFET, subjected to UIS operating condition. The chapter also covers the discussions on repetitive avalanche ruggedness capability and how this operation can be quantified to operate safely.

2 Single-shot and repetitive avalanche definitions

Single-shot avalanche events are avalanche events that occur due to a fault condition in the application such as electrical overstress. The application does not have an avalanche designed into its operation.

However, repetitive avalanche refers to the applications where avalanche is an intended operation mode of the MOSFET. Here, avalanche is a designed function and has a limited number of operations to ensure reliability of the MOSFET over its life. The number of allowed events is a function of the avalanche energy and can be determined from the data sheet charts found on repetitive avalanche specific parts – ending in suffix R e.g. BUK9K51-60R.

Any customer wishing to operate outside the current avalanche ratings may be considered on an application basis. Contact your local sales team for more information.

3 Understanding power MOSFET single-shot avalanche events

The researchers and the industry have established single-shot avalanche capability of a device (see Ref. 1, Ref. 2 and Ref. 3). The test is carried out on a simple unclamped inductive load switching circuit, as shown in Figure 1.

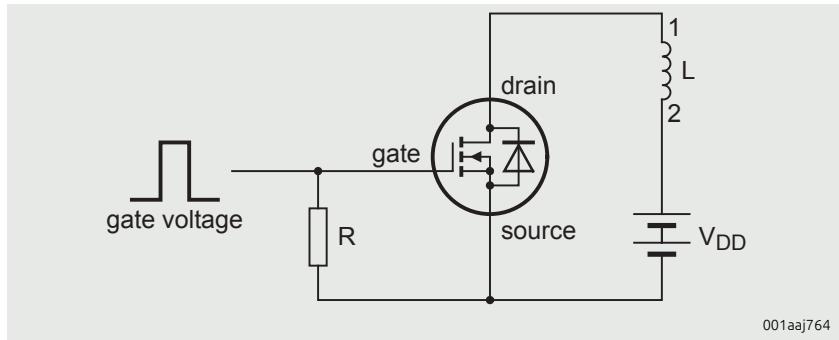


Figure 1 | Unclamped inductive load test circuit for MOSFET ruggedness evaluation

3.1 Single-shot UIS operation

A voltage pulse is applied to the gate to turn on the MOSFET, as shown in Figure 2. It allows the load current to ramp up according to the inductor value (L) and the drain supply voltage (V_{DD}). The phenomenon is shown in Figure 3 and Figure 4. At the end of the gate pulse, the MOSFET is turned off. The current in the inductor continues to flow, causing the voltage across the MOSFET to rise sharply. This overvoltage is clamped at breakdown voltage (V_{BR}) until the load current reaches zero, as illustrated in Figure 3. Typically, V_{BR} is:

$$V_{BR} \approx 1.3 \times V_{(BR)DSS} \quad [1]$$

The peak load current passing through the MOSFET before turn off is the non-repetitive drain-source avalanche current ($I_{DS(AL)S}$) of the UIS event. $I_{DS(AL)S}$ is illustrated in Figure 4. The following expression is used to determine the rate at which the avalanche current decays, which is dependent on the inductor value:

$$\frac{dI_{DS(AL)S}}{dt_{AL}} = -\frac{V_{BR} - V_{DD}}{L} \quad [2]$$

The peak drain-source avalanche power ($P_{DS(AL)M}$) dissipated in the MOSFET is

shown in Figure 5. It is a product of the breakdown voltage (V_{BR}) and the non-repetitive drain-source avalanche current ($I_{DS(AL)S}$); see Figure 3 and Figure 4. The avalanche energy dissipated is the area under the P_{AV} waveform and is estimated from the following expression:

$$E_{DS(AL)S} = \frac{P_{DS(AL)M} \times t_{AL}}{2} \quad [3]$$

or

$$E_{DS(AL)S} = \frac{1}{2} \cdot \frac{V_{BR}}{V_{BR} - V_{DD}} \cdot L I^2_{DS(AL)S} \quad [4]$$

Another crucial parameter involved in a MOSFET avalanche event is the junction temperature. After the avalanche event (τ) has begun, the following expression is used to determine the transient junction temperature variation during device avalanche at a given time:

$$\Delta T_j(\tau) = \int_0^\tau P_{AV}(t) \frac{dZ_{th}(\tau-t)}{dt} dt \quad [5]$$

where Z_{th} is the power MOSFET transient thermal impedance. Alternatively, the following expression approximates the maximum ΔT_j :

$$\Delta T_{j(max)} \approx \frac{2}{3} P_{DS(AL)M} Z^{th}(t_{AL})/2 \quad [6]$$

Assuming that $T_{j(max)}$ occurs at $t_{AL}/2$, $Z^{th}(t_{AL})/2$ is the transient thermal impedance measured at half the avalanche period t_{AL} . Note, the Z_{th} value used for the avalanche calculation is more conservative than the one published in data sheets due to the nature of avalanche.

Therefore, the maximum junction temperature resulting from the avalanche event is:

$$T_{j(max)} \approx \Delta T_{j(max)} + T_j \quad [7]$$

where T_j refers to the junction temperature prior to turn off.

3.1.1 Single-shot UIS waveforms

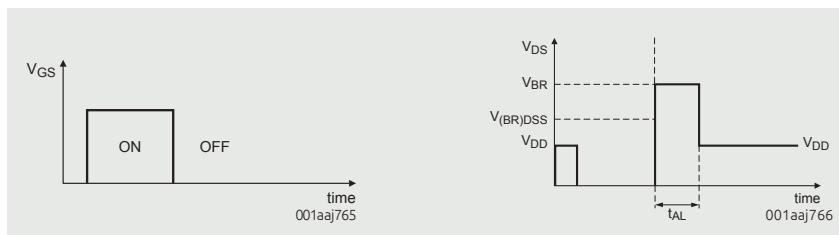


Figure 2 | Gate-source voltage, V_{GS}

Figure 3 | Drain-source voltage, V_{DS}

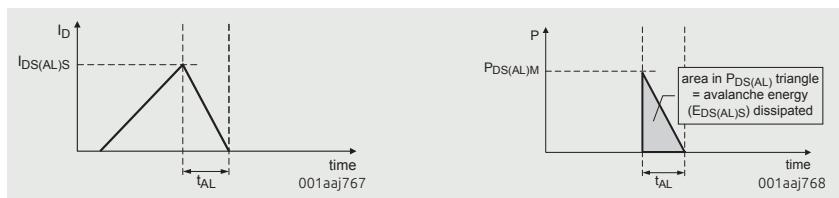
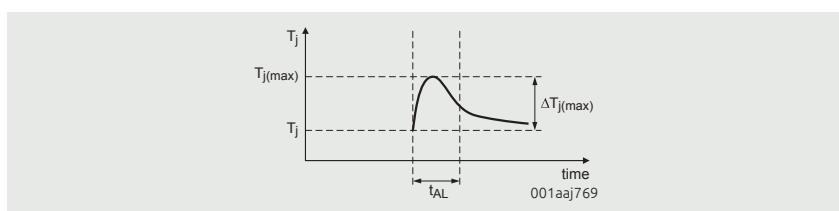


Figure 4 | Drain current, I_D

Figure 5 | Peak drain-source avalanche power, $P_{DS(Al)m}$



3.2 Single-shot avalanche ruggedness rating

The failure mechanism for a single-shot avalanche event in a power MOSFET is due to the junction temperature exceeding the maximum temperature rating. In such a case, catastrophic damage occurs to the MOSFET. If the transient temperature resulting from an avalanche event, as shown in Figure 6, rises beyond a recommended rated value, the device risks being degraded. The recommended rated value is de-rated from the maximum temperature for optimum reliability.

Blackburn (see Ref. 2) has discussed a general guideline in detail, on the

appropriate method of quantifying the single-shot avalanche capability of a device. It takes the avalanche current and initial junction temperature into consideration. The maximum allowed avalanche current as a function of avalanche time defines the safe operation for a device single-shot UIS event. The maximum allowed avalanche current is set so that a safe maximum junction temperature, $T_{j(\max)}$ of 175 °C, is never exceeded. Using Equation 7, Figure 7 is plotted.

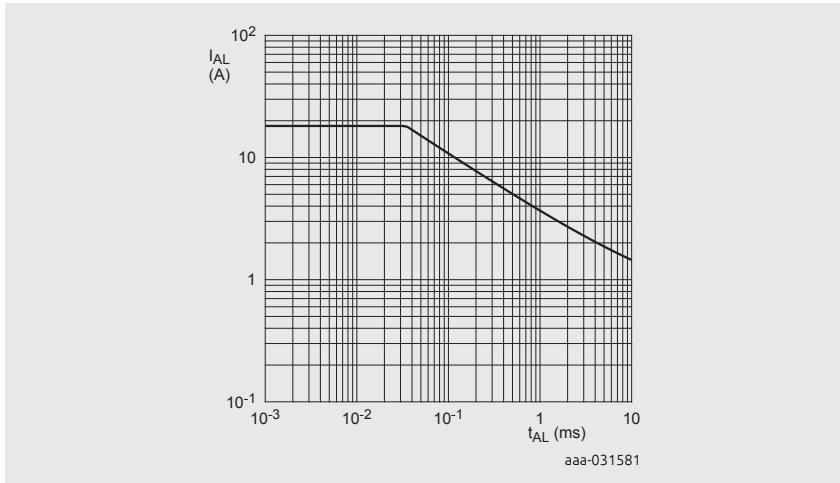


Figure 7 | BUK9K51-60R avalanche rating; avalanche current as a function of avalanche time

Figure 7 shows the SOA curve of a device single-shot avalanche capability. The 25 °C junction temperature curve shows the maximum allowable I_{AL} for a given t_{AL} at an initial T_j of 25 °C. This maximum I_{AL} results to a maximum allowable junction temperature $T_{j(\max)}$ of 175 °C, which means a $\Delta T_{j(\max)}$ of 150 °C. The area under the SOA curve is the Safe Operating Area (SOA).

The maximum junction temperature resulting in catastrophic device avalanche failure is approximately 380 °C, which is in excess of the rated $T_{j(\max)}$ of 175 °C. However, operating beyond the rated $T_{j(\max)}$ may induce long-term detrimental effects to the power MOSFET and is not recommended.

4 Understanding power MOSFET repetitive avalanche events

Repetitive avalanche refers to an operation involving repeated single-shot avalanche events, as discussed earlier. Until recently, most manufacturers have avoided the issues pertaining to the power MOSFET repetitive avalanche capability.

It is primarily due to the complexity in such operations and the difficulties in identifying the underlying physical degradation process in the device.

Due to the traumatic nature of the avalanche event, a repetitive avalanche operation can be hazardous for a MOSFET. It is hazardous even when the individual avalanche events are below the single-shot UIS rating. This type of operation involves additional parameters such as frequency, duty cycle, and thermal resistances $R_{th(j-a)}$ and $R_{th(j-mb)}$ of the system during the avalanche event. However, it is possible to de-rate the single-shot rating to define a repetitive avalanche SOA.

4.1 Repetitive UIS operation

The repetitive UIS test circuit is shown in Figure 1. The gate is fed with a train of voltage pulses at a frequency (f) and for a duty cycle as shown in Figure 8. The resulting breakdown voltage (V_{BR}) and drain current (I_D) passing through the load are the same as for a single-shot UIS. However, the peak I_D is now denoted as repetitive drain-source avalanche current ($I_{DS(AL)R}$), as shown in Figure 9.

The repetitive drain-source avalanche power ($P_{DS(AL)R}$) resulting from the repetitive UIS operation is shown in Figure 10. For finding the value of $P_{DS(AL)R}$, it is necessary to first calculate $E_{DS(AL)S}$ for a single avalanche event using Equation 3. This resultant value of $E_{DS(AL)S}$ is substituted in the following expression, to calculate the value of $P_{DS(AL)R}$:

$$P_{DS(AL)R} = E_{DS(AL)S} \times f \quad [8]$$

4.1.1 Repetitive UIS waveforms

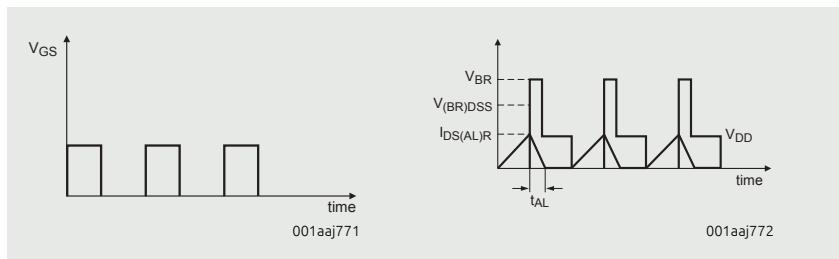


Figure 8 | Gate pulse, V_{GS}

Figure 9 | Drain-source voltage, V_{DS} and repetitive drain-source avalanche current, $I_{DS(AL)R}$

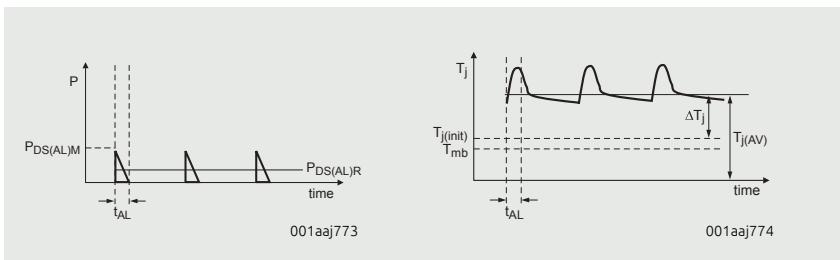


Figure 10 | Repetitive drain-source avalanche power, $P_{DS(AL)R}$

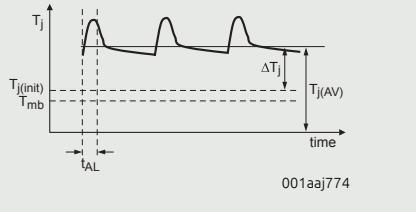


Figure 11 | Transient junction temperature components of MOSFET during repetitive avalanche

4.2 Temperature components

The temperature rise from the repetitive avalanche mode in the power MOSFET is shown in Figure 11.

The temperature ($T_{J(init)}$) comprises the mounting base temperature (T_{mb}) and the temperature rise resulting from any on-state temperature difference (ΔT_{on}).

$$T_{J(init)} = T_{mb} + \Delta T_{on} \quad [9]$$

In addition, there is a steady-state average junction temperature variation (ΔT_j) resulting from the average repetitive avalanche power loss.

$$\Delta T_j = P_{DS(AL)R} \times R_{th(j-a)} \quad [10]$$

where $R_{th(j-a)}$ is the thermal resistance from junction to ambient of the device in the application. The summation of Equation 9 and Equation 10 gives the average junction temperature, $T_{J(AV)}$ of a power MOSFET in repetitive UIS operation.

$$T_{J(AV)} = T_{J(init)} + \Delta T_j \quad [11]$$

5 Repetitive avalanche ruggedness rating

Our investigations show that there is more than one failure or wear-out mechanism involved in repetitive avalanche. Temperature is not the only limiting factor to a repetitive avalanche operation. However, by limiting temperature and the repetitive drain-source avalanche current ($I_{DS(AL)R}$), an operating environment is defined such that the avalanche conditions do not activate device degradation. It allows the power MOSFET to operate under repetitive UIS conditions safely.

Figure 12 shows the repetitive avalanche SOA curve of BUK9K51-60R, where for each avalanche event the T_j rise is limited to 30 K.

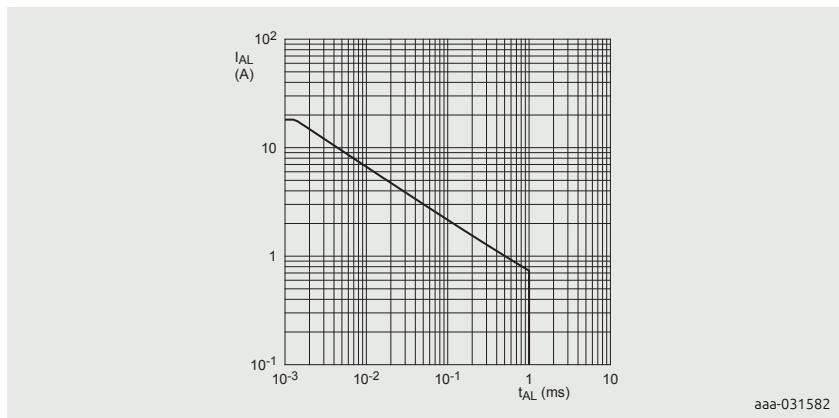


Figure 12 | Repetitive avalanche rating; avalanche current

The three conditions which must be satisfied for safe operation of a power MOSFET under repetitive avalanche mode are:

1. $I_{(AL)}$ should not exceed the repetitive avalanche SOA curve
2. T_j should not exceed 175 °C
3. The number of cycles should not exceed the avalanche cycle limit chart

The number of allowable cycles can be determined through a second chart in the avalanche MOSFET's data sheet, (see Figure 13).

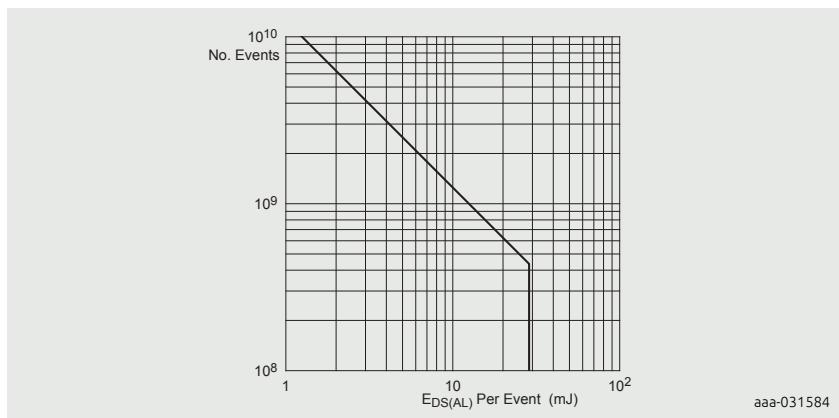


Figure 13 | Repetitive avalanche rating; maximum number of avalanche events as a function of avalanche energy

6 Conclusion

Power MOSFETs can sustain single-shot and repetitive avalanche events. Simple design rules and SOA regions are provided.

7 Examples

The following examples examine cases of avalanche operation acceptance:

7.1 Single-shot avalanche case

- Device: BUK9K51-60R; see Figure 7
- $L = 30 \mu\text{H}$
- $I_{AL} = 18 \text{ A}$
- $R_{th(j-a)} = 5 \text{ K/W}$
- $V_{(BR)DSS} = 60 \text{ V}$
- $V_{DD} = 0 \text{ V}$

7.1.1 Calculation steps

1. Using the above information, t_{AL} can be determined using Equation 2, which in this case is 7 μs . Transferring the I_{AL} and t_{AL} conditions onto Figure 12, the operating point is under the SOA curve. It suggests that the operating condition may be feasible.

7.2 Repetitive avalanche case

- Device: BUK9K51-60R; see Figure 12 and Figure 13
- $L = 30 \mu\text{H}$
- $I_{(AL)} = 10 \text{ A}$
- $f = 3 \text{ kHz}$
- $R_{th(j-a)} = 5 \text{ K/W}$
- $T_0 = 100^\circ\text{C}$
- $V_{(BR)DSS} = 60 \text{ V}$
- $V_{DD} = 0 \text{ V}$

7.2.1. Calculation steps

1. From the above information, t_{AL} can be determined using Equation 2, which in this case is approximately 4 μs . Transferring the I_{AL} and t_{AL} conditions onto

Figure 12, the operating point is under the boundary of the 'Rep. Ava' SOA curve. It suggests that the operating condition is acceptable. Therefore, condition 1 is satisfied.

2. Calculate the non-repetitive drain-source avalanche energy ($E_{DS(AL)S}$) using Equation 3 $E_{DS(AL)S} = 1.56 \text{ mJ}$).
3. Calculate the repetitive drain-source avalanche power ($P_{DS(AL)R}$) using Equation 8 ($P_{DS(AL)R} = 4.68 \text{ W}$).
4. Calculate the average ΔT_j rise from repetitive avalanche (ΔT_j) using Equation 10 ($\Delta T_j = 123.4 \text{ }^{\circ}\text{C}$).
5. Determine the average junction maximum temperature in repetitive avalanche operation ($T_{j(AV)}$) using Equation 11 ($T_{j(AV)} = 153 \text{ }^{\circ}\text{C}$). Therefore, condition 2 is satisfied.
6. Finally based on the energy we can determine the limit number of operations at these conditions from Figure 13, (No. events = $8e^9$)

Based on the above calculations, the operating conditions meet the repetitive avalanche requirements with a limited number of repetitive events of $8e^9$.



LFPAK33 Automotive MOSFETs in powertrain applications



Single shot avalanche ruggedness of MOSFETs



Electrification of the powertrain introduction



LFPAK56D taking the heat out of engine management systems



Talking 48 volts and robust MOSFETs at EEHE Conference



Trench 9 LFPAK33 MOSFETs drive powertrain systems up to 300 W

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Chapter 5

Using RC Thermal Models

Application Note: AN11261

1 Introduction

Analysis of the thermal performance of power semiconductors is necessary to efficiently and safely design any system utilizing such devices. This chapter presents a quick and inexpensive way to infer the thermal performance of power MOSFETs using a thermal electrical analogy.

The thermal behaviour of power semiconductor devices can be predicted using RC thermal models. The model types presented in this chapter are known as Foster and Cauer models, consisting in networks of resistors and capacitors. Foster and Cauer models are equivalent representations of the thermal performance of a MOSFET and they can be used within a SPICE environment. This chapter provides some basic theory behind the principle, and how to implement Foster and Cauer RC thermal models. For convenience, Foster and Cauer RC thermal models are referred to as RC models in the rest of this application note. Several methods of using RC thermal models, including worked examples, will be described.

2 Thermal impedance

RC models are derived from the thermal impedance (Z_{th}) of a device (see Figure 1). This figure represents the thermal behavior of a device under transient power pulses. The Z_{th} can be generated by measuring the power losses as a result of applying a step function of varying time periods.

A device subjected to a power pulse of duration $> \sim 1$ second, i.e. steady-state, has reached thermal equilibrium and the Z_{th} plateaus becomes the R_{th} . The Z_{th} illustrates the fact that materials have thermal inertia. Thermal inertia means that temperature does not change instantaneously. As a result, the device can handle greater power for shorter duration pulses.

The Z_{th} curves for repetitive pulses with different duty cycles, are also shown in Figure 1. These curves represent the additional RMS temperature rise due to the dissipation of RMS power.

To assist this discussion, the thermal resistance junction to mounting base $R_{th(j\text{-mb})}$ from the BUK7S1R0-40H data sheet, has been included in Table 1. The Z_{th} in Figure 1 also belongs to the BUK7S1R0-40H data sheet.

Table 1: Steady state thermal impedance of BUK7S1R0-40H

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-mb})}$	thermal resistance from junction to mounting base	-	0.35	0.4	0.4	K/W

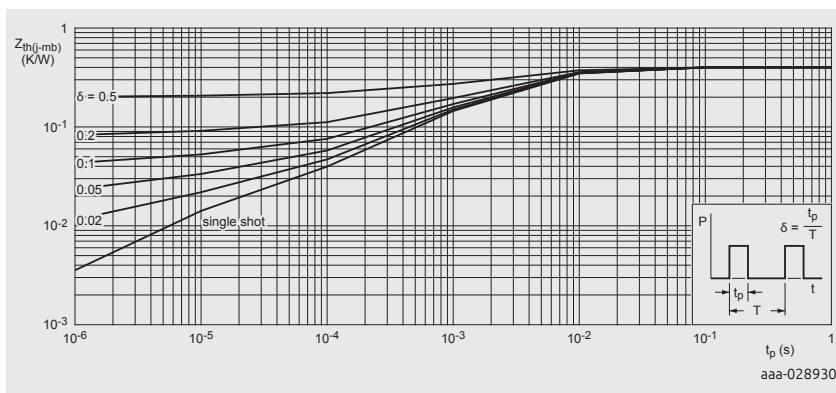


Figure 1 | Transient thermal impedance from junction to mounting base as a function of pulse duration for the BUK7S1R0-40H

3 Calculating junction temperature rise

To calculate the temperature rise within the junction of a power MOSFET, the power and duration of the pulse delivered to the device must be known. If the power pulse is a square, then the thermal impedance can be read from the Z_{th} chart. The product of this value with the power gives the temperature rise within the junction.

If constant power is applied to the device, the steady state thermal impedance can be used i.e. R_{th} . Again the temperature rise is the product of the power and the R_{th} .

For a transient pulse e.g. sinusoidal or pulsed, the temperature rise within the MOSFET junction becomes more difficult to calculate.

The mathematically correct way to calculate T_j is to apply the convolution integral. The calculation expresses both the power pulse and the Z_{th} curve as functions of time, and use the convolution integral to produce a temperature profile (see Ref. 2).

$$T_{j(rise)} \int_0^{\tau} P(t) \cdot \frac{d}{dt} Z_{th}(\tau - t) dt \quad [1]$$

However, this is difficult as the $Z_{th}(\tau-t)$ is not defined mathematically. An alternative way is to approximate the waveforms into a series of rectangular pulse and apply superposition (see Ref. 1).

While relatively simple, applying superposition has its disadvantages. The more complex the waveform, the more superpositions that must be imposed to model

the waveform accurately.

To represent Z_{th} as a function of time, we can draw upon the thermal electrical analogy and represent it as a series of RC charging equations or as an RC ladder. Z_{th} can then be represented in a SPICE environment for ease of calculation of the junction temperature.

4 Association between Thermal and Electrical parameters

The thermal electrical analogy is summarized in Table 2. If the thermal resistance and capacitance of a semiconductor device is known, electrical resistances and capacitances can represent them respectively. Using current as power, and voltage as the temperature difference, any thermal network can be handled as an electrical network.

Table 2: Fundamental parameters

Type	Resistance	Potential	Energy	Capacitance
Electrical ($R = V/I$)	$R = \text{resistance}$ (Ohms)	$V = PD$ (Volts)	$I = \text{current}$ (Amps)	$C = \text{capacitance}$ (Farads)
Thermal ($R_{th} = K/W$)	$R_{th} = \text{thermal}$ resistance (K/W)	$K = \text{temperature}$ difference (Kelvin)	$W = \text{dissipated}$ power (Watts)	$C_{th} = \text{thermal}$ capacitance (thermal mass)

5 Foster and Cauer RC thermal models

Foster models are derived by semi-empirically fitting a curve to the Z_{th} , the result of which is a one-dimensional RC network Figure 2. The R and C values in a Foster model do not correspond to geometrical locations on the physical device. Therefore, these values cannot be calculated from device material constants as can be in other modeling techniques. Finally, a Foster RC model cannot be divided or interconnected through, i.e. have the RC network of a heat sink connected.

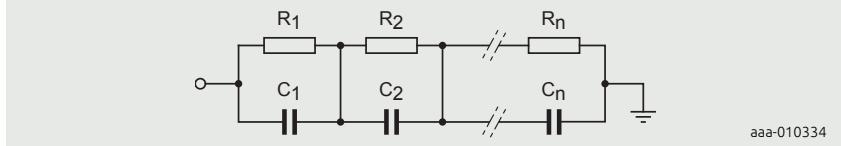


Figure 2 | Foster RC thermal models

Foster RC models have the benefit of ease of expression of the thermal impedance Z_{th} as described at the end of Section 2. For example, by measuring the heating or cooling curve and generating a Z_{th} curve, Equation 2 can be applied to generate a fitted curve Figure 3:

$$Z_{th(t)} = \sum_{i=1}^n R_i \cdot [1 - \exp(-\frac{t}{\tau_i})] \quad [2]$$

Where: $\tau_i = R_i \cdot C_i$ [3]

The model parameters R_i and C_i are the thermal resistances and capacitances that build up the thermal model depicted in Figure 2. The parameters in the analytical expression can be optimised until the time response matches the transient system response by applying a least square fit algorithm.

The individual expression, “i”, also draws parallels with the electrical capacitor charging equation. Figure 3 shows how the individual R_i and C_i combinations, sum to make the Z_{th} curve.

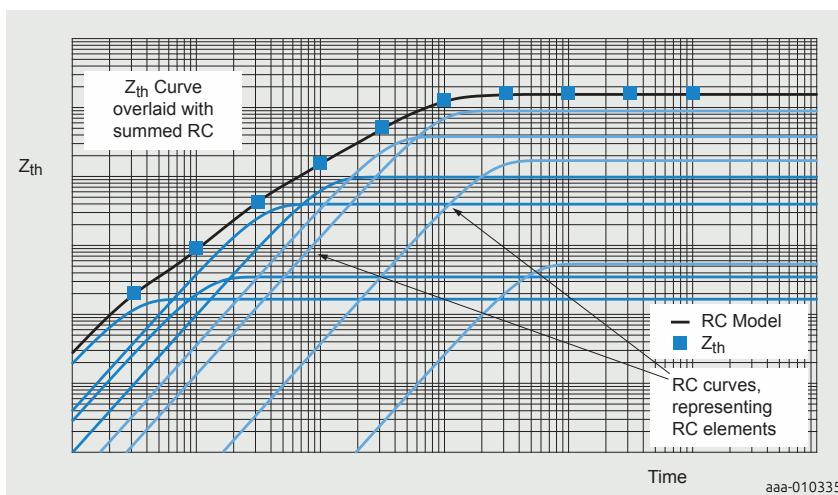


Figure 3 | Foster RC thermal models

Foster models have no physical meaning since the node-to-node heat capacitances have no physical reality. However, a Foster model can be converted into its Cauer counter-part by means of a mathematical transformation (see Ref. 4).

An n-stage Cauer model can be derived from an n-stage Foster model and they will be equivalent representations of the device thermal performance.

As seen for the Foster model, the Cauer Model also consists of an RC network but the thermal capacitances are all connected to the thermal ground, i.e. ambient

temperature as represented in Figure 4. The nodes in the Cauer Model can have physical meaning and allow access to the temperature of the internal layers of the semiconductor structure.

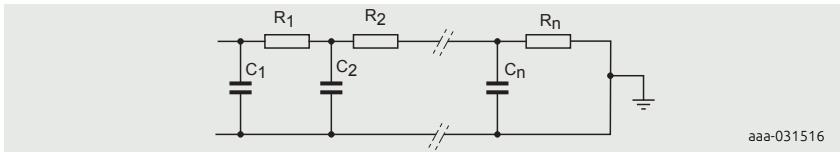


Figure 4 | Cauer RC thermal models

Nexperia provides Foster and Cauer RC models for most of their Automotive Power MOSFET products on the Product Information Pages. The models can be found under the Support tab, demonstrated below with BUK7S1R0-40H, see Figure 5.

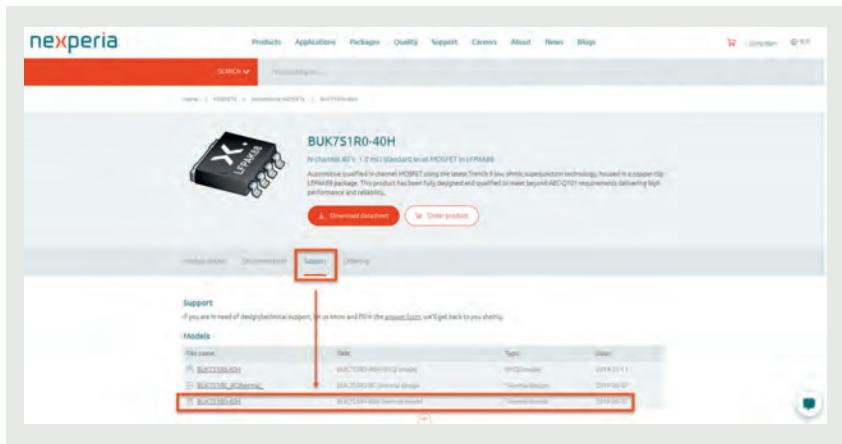


Figure 5 | Nexperia RC thermal model documentation

Foster and Cauer RC thermal models allow application engineers to perform fast calculations of the transient response of a package to complex power profiles. In the following sections several examples of using RC thermal models will be presented. Foster models and Cauer models are equivalent representations of the device thermal behaviour but in the described examples Cauer models will be used as more representative of the physical structure of the device.

As shown in Figure 8, a schematic file is available on Nexperia website for BUK7S1R0-40H Cauer model. Other products may not have this schematic file available and may be provided with a netlist file for the Cauer network as shown in Figure 6:

*Part: BUK7S1R0-40H

```
.subckt cauer 1 6 7
R1    1    2    0.00272144
R2    2    3    0.0220255
R3    3    4    0.00713124
R4    4    5    0.185679
R5    5    6    0.182443
C1    1    7    9.29451e-05
C2    2    7    0.000514739
C3    3    7    0.00195047
C4    4    7    0.00305028
C5    5    7    0.0279554
.end cauer
```

Figure 6 | BUK7S1R0-40H Cauer model netlist

The netlist describes the same Cauer network as in Figure 8, and can be used to build the same schematic. Pin 1 in the netlist can be identified as the junction temperature pin T_j in the schematic. Similarly pins 6, 7 as the T_{amb} pins in the schematic.

In order to simulate only the MOSFET pins 6 and 7 will both be tied to the ambient voltage source, as shown in Figure. 8.

However, one of the advantages of using Cauer models is to allow to add external networks to the MOSFET model, for example to model PCBs, heatsinks etc. In order to do so pin 7 will be tied to ambient and pin 6 to the first pin of the external Cauer network. For correct results, it is fundamental to make sure that the end pin of the external Cauer network is tied to the ambient source.

6 Thermal simulation examples

6.1 Example 1

RC thermal models are generated from the Z_{th} curve. This example shows how to work back from an RC model and plot a Z_{th} curve within a SPICE simulator. It allows for greater ease when trying to read values of the Z_{th} curve from the data sheet. This and subsequent examples use the RC thermal model of BUK7S1R0-40H. T_{mb} represents the mounting base temperature. It is treated as an isothermal and for

this example it is set as 0 °C.

A single shot pulse of 1 W power is dissipated in the MOSFET. Referring to Figure 7; for a single shot pulse, the time period between pulses is infinite and therefore the duty cycle $\delta = 0$. Then the junction temperature T_j represents the transient thermal impedance Z_{th} .

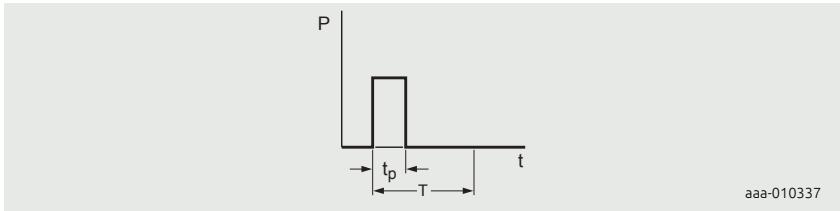


Figure 7 | Single-shot pulse

$$T_j = T_{mb} + \Delta T = 0 \text{ } ^\circ\text{C} + \Delta T = \Delta T$$

[4]

$$\Delta T = P \cdot Z_{th} = 1 \text{ W} \cdot Z_{th}$$

[5]

Equation 5 demonstrates that with $P = 1 \text{ W}$, the magnitude of Z_{th} equates to ΔT . The following steps are used to set up and run simulations:

1. set up the RC thermal model of BUK7S1R0-40H in SPICE as shown in Figure 8
2. set the value of voltage source V_{mb} to 0, which is the value of T_{mb}
3. set the value of the current source I_1 to 1
4. create a simulation profile and set the run time to 1 s
5. run the simulation
6. Plot the voltage at nod

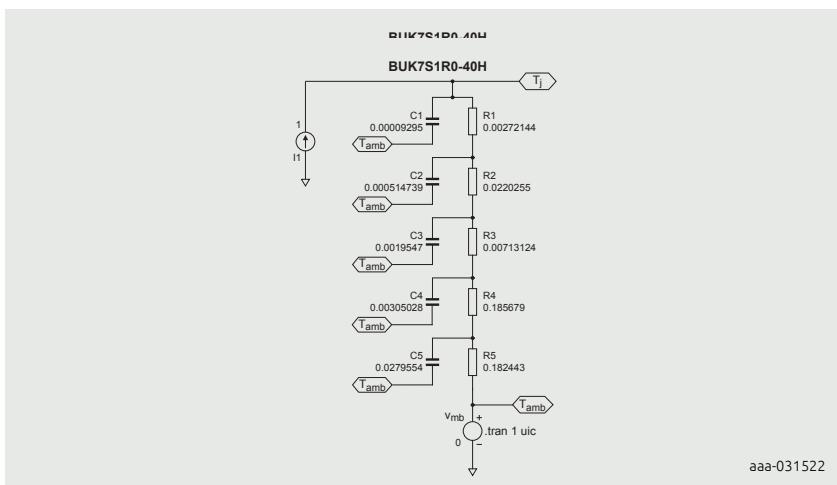


Figure 8 | BUK7S1R0-40H thermal model setup in SPICE

The simulation result in Figure 9 shows the junction temperature (voltage at T_j) which is also the thermal impedance of BUK7S1R0-40H. The values of Z_{th} at different times can be read using the cursors on this plot within SPICE.

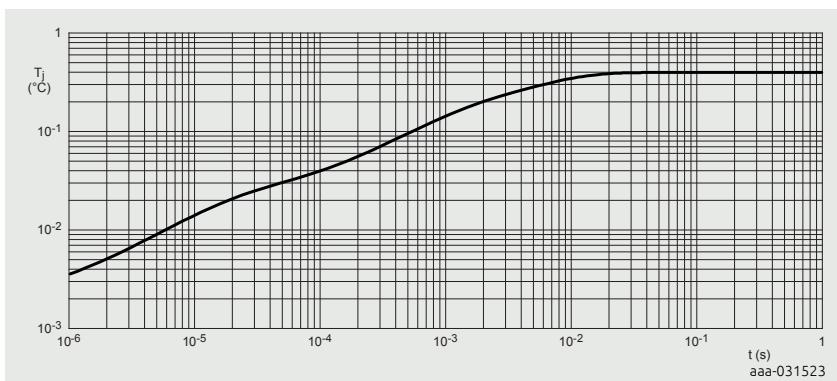


Figure 9 | A plot of T_j from simulation

The value of the current source in this example is set to 1 A to represent 1 W dissipating through the device. It can be easily changed to represent any value of power. The simulation command can be changed for any duration to represent a range of square power pulses.

6.2 Example 2

Another method of generating the power profile, is to use measurements from the actual circuit. This information is presented to the SPICE simulation in the form of a comma-separated value (CSV) file giving pairs of time/power values. It can be generated either as a summary of observations showing the points of change or from an oscilloscope waveform capture.

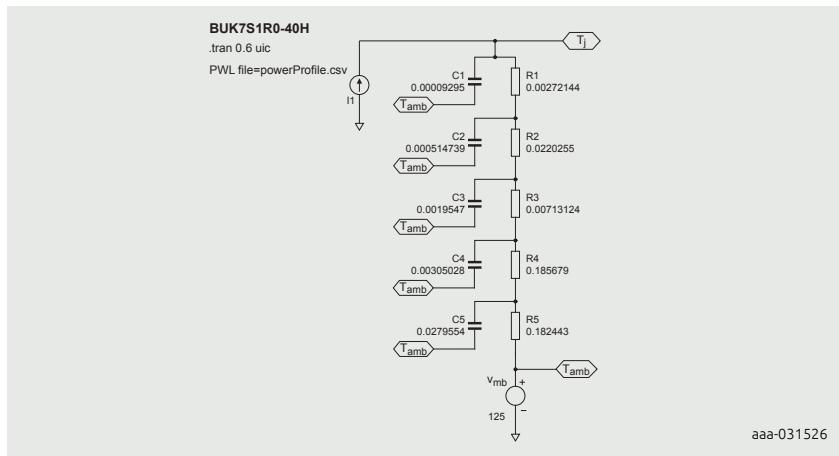
Two further methods of generating a power profile are discussed. One method is using a PWL file. The other is to generate the power from an MOSFET electrical circuit modeled in SPICE. The former is outlined first.

A source within a SPICE simulator can use a PWL file as an input. The contents of a typical PWL file is shown in Table 3. It can list the current, voltage or in this example, power over time. These files can be generated by typing values into a spreadsheet editor and saving as a .csv file, or alternatively exporting waveforms from an oscilloscope. The actual file itself should not contain any column headings. To implement this procedure within a SPICE environment, follow the same steps as described in Section 6.1 “Example 1”, but with the exceptions:

1. Set the property value of the current source to read from a PWL FILE and point it to a .csv file for example: C:\Pulse file\filepulse.csv, which contains the power profile listed in Table 3
2. Set the mounting base T_{mb} (V_{mb}) to 125 °C
3. Set the simulation run time to 0.6 s

Table 3: Data example for use in a PWL file

Time (seconds)	Power (Watts)
0.000000	0
0.000001	120
0.004000	120
0.004001	24
0.004002	24
0.100000	24
0.100001	24
0.100002	80
0.200000	80
0.200002	80
0.200003	0
0.300000	0
0.300001	80
0.315000	80
0.315001	24
0.400000	24
0.400001	0
0.500000	0
0.500001	120
0.515000	120

**Figure 10 |** SPICE circuit implementing a PWL file with the thermal model of the BUK7S1R0-40H

The simulation result is shown in Figure 11. The junction temperature and thermal impedance values labeled in Figure 11 demonstrate that the Z_{th} value at 4 ms, and R_{th} value, are in line with Figure 12. It represents the thermal impedance waveform shown in the BUK7S1R0-40H data sheet.

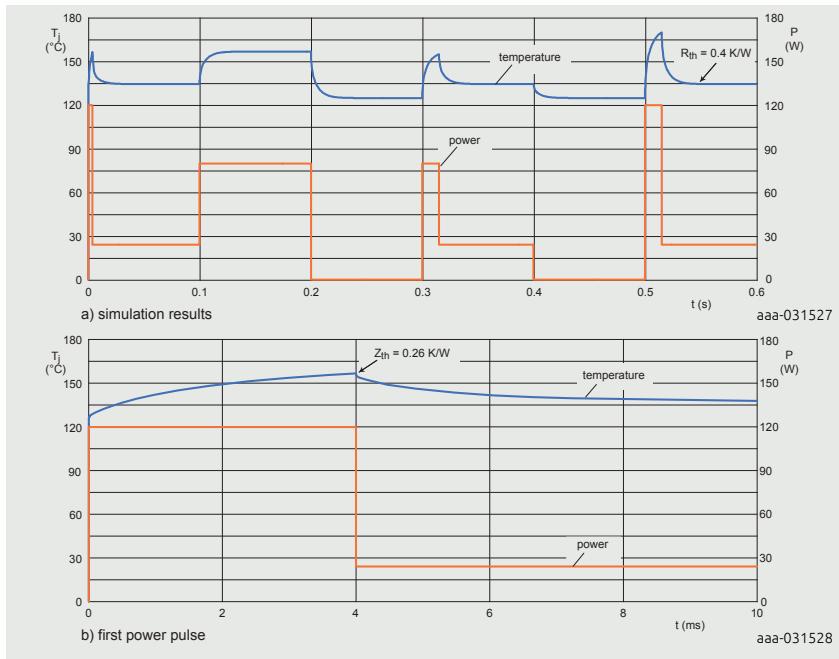


Figure 11 | Simulation results and first power pulse

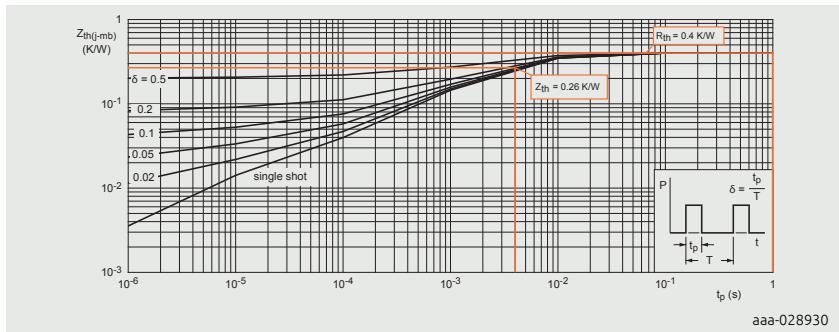


Figure 12 | Transient thermal impedance for BUK7S1R0-40H

The red lines highlight the thermal resistance and impedance for the example shown in Figure 11

6.3 Example 3

The aim of this example is to show how to perform thermal simulation using the power profile generated from a MOSFET circuit.

Following the steps in Section 6.1, set up the thermal model of BUK7S1R0-40H, and set the mounting base temperature to 85 °C.

To set the power value in the current source, construct a MOSFET electrical circuit as provided in Figure 13. The power supply is 12 V. The gate drive supply is assigned a value of 10 V. It is set to run for 50 cycles with a 1 ms period and a 50 % duty cycle.

The power dissipated in the MOSFET can be calculated from Equation 6 or for greater accuracy; the gate current can be included into the calculation to give Equation 7:

$$P = V_{DS} \cdot I_D \quad [6]$$

To improve accuracy:

$$P = V_{DS} \cdot I_D + V_{GS} \cdot I_G \quad [7]$$

The current source into the thermal model can now be defined as:

$$I = V_{(D)} \cdot I(V_D) + V_{(G)} \cdot I(V_G) \quad [8]$$

Figure 13 demonstrates the link between the electrical circuit and the thermal model circuit.

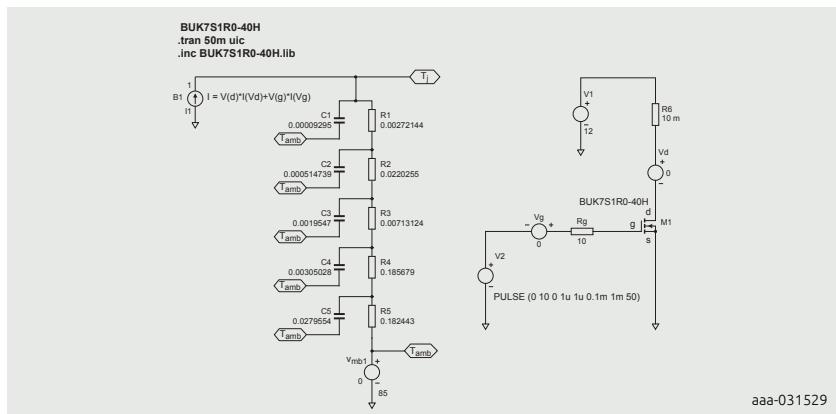


Figure 13 | SPICE circuit illustrating how to integrate an electrical circuit with a thermal model

The resultant plot of T_j is shown in Figure 14. The maximum temperature of the junction can once again be calculated from data sheet values by following the steps outlined in Ref. 1.

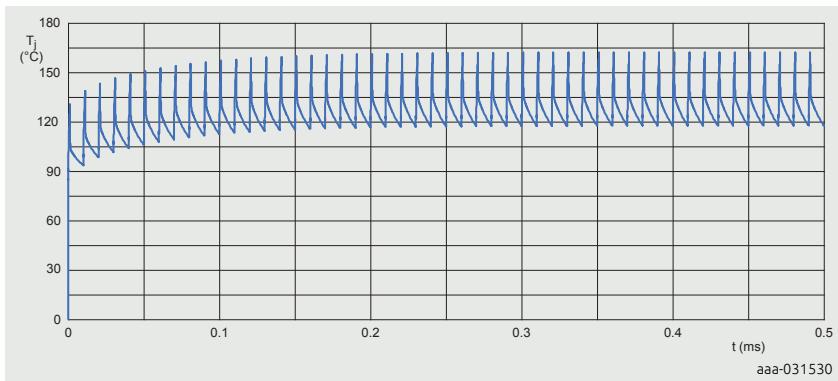


Figure 14 | Inferred junction temperature (T_j) rise provided by Figure 12

7 Discussions

RC thermal models are not perfect. The physical materials used to build Semiconductors have temperature-dependent characteristics. These characteristics mean that thermal resistance is also a temperature-dependent parameter. Whereas in Ohm's law, the Ohmic resistance is usually considered to be constant and independent of the voltage. So the correspondence between electrical and thermal parameters is not perfectly symmetrical but gives a good basis for fundamental thermal simulations.

In power electronic systems, the thermal resistance of silicon amounts to 2 % to 5 % of the total resistance. The error resulting from the temperature dependence is relatively small and can be ignored for most cases. To obtain a more accurate analysis, replace the passive resistors in the RC model with voltage-dependent resistors. In these resistors, the change in temperature can correspond to change in voltage.

A further limitation of the models presented is that the mounting base temperature of the MOSFET T_{mb} , is set as an isothermal. This is rarely the case in real applications where a rise in the mounting base temperature must be considered. This rise is determined by calculating the temperature rise due to the average power dissipation (i.e. the heat flow) from the mounting base through to ambient. It means that the models are of limited use for pulses greater than 1 s, where heat begins to flow into the environment of the MOSFET. In this situation, the thermal model for the MOSFETs, PCB, heat sink and other materials in proximity must be included.

8 Summary

RC thermal models are available for Nexperia power MOSFETs on the Nexperia website. The models can be used in SPICE or other simulation tools to simulate the junction temperature rise in transient conditions. They provide a quick, simple and accurate method for application engineers to perform the thermal design.



RC thermal simulation of power MOSFETs

9 References

1. Application note AN11156 - "Using Power MOSFET Z_{th} Curves". Nexperia
2. Application note AN10273 - "Power MOSFET single-shot and repetitive avalanche ruggedness rating". Nexperia
3. Combination of Thermal Subsystems Modeled by Rapid Circuit Transformation. Y.C. Gerstenmaier, W. Kiffe, and G. Wachutka
4. JEDEC Standard JESD51-14 Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices with Heat Flow Through a Single Path

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Chapter 6

Designing RC snubbers

Application Note: AN11160

1 Introduction

This chapter describes the design of a simple “RC snubber circuit”. The snubber is used to suppress high-frequency oscillations associated with reverse recovery effects in power semiconductor applications.

2 Test circuit

The basic circuit is a half-bridge and shown in Figure 1.

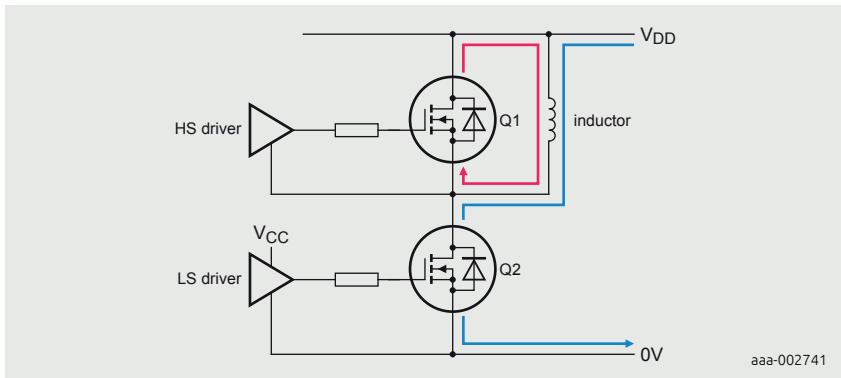


Figure 1 | The half-bridge circuit

Q1 and Q2 are BUK761R6-40E devices. The inductor could also be connected to 0 V rather than V_{DD} .

Inductor current is established in the red loop; Q2 is off and current is flowing through Q1 body diode. When Q2 is turned on, current “commutes” to the blue loop and the reverse recovery effect occurs in Q1. We observe the effect of Q1 reverse recovery on the V_{DS} waveform of Q2; see Figure 2.

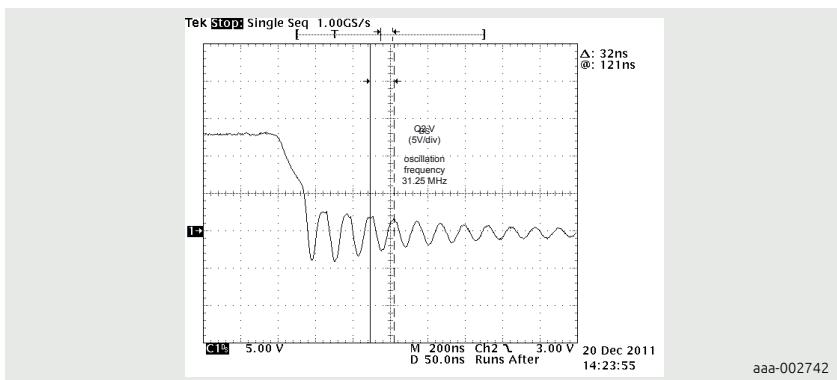


Figure 2 | Reverse recovery-induced oscillation in Q2 V_{DS}

The equivalent circuit is shown in Figure 3.

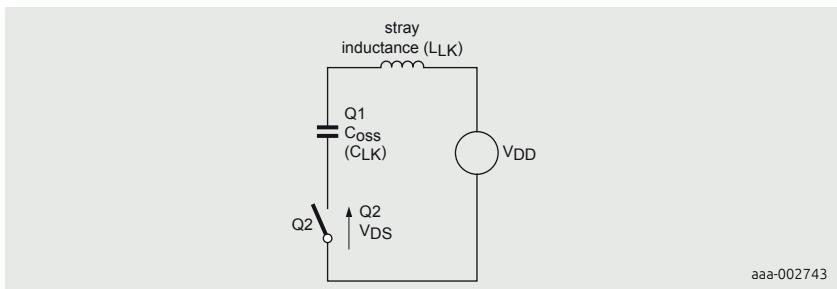
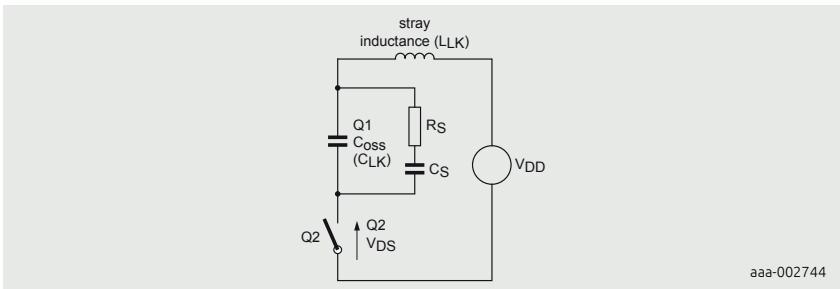


Figure 3 | Equivalent circuit

We are primarily interested in the parasitic elements in the circuit:

- L_{LK} is the total stray or “leakage” inductance comprised of PCB trace inductance, device package inductance, etc.
- The parasitic capacitance C_{LK} is mainly due to C_{oss} of the upper ($Q1$) device.

$Q2$ is treated as a simple switch. The oscillation can be eliminated (snubbed) by placing an RC circuit across $Q1$ drain-source; see Figure 4



aaa-002744

Figure 4 | Equivalent circuit with snubber components R_S and C_S

3 Determining C_{LK} and L_{LK}

Before we can design the snubber, we must first determine C_{LK} and L_{LK} . We could attempt to measure C_{LK} and L_{LK} directly, but a more elegant method can be used. For this LC circuit, we know that:

$$f_{RING0} = \frac{1}{2\pi\sqrt{L_{LK}C_{LK}}} \quad [1]$$

where f_{RING0} is the frequency of oscillation without a snubber in place; see Figure 2. If we add an extra additional capacitor across Q1 (C_{add}), the initial oscillation frequency from f_{RING0} to f_{RING1} ($f_{RING1} < f_{RING0}$) will change. It can be shown that (see Section 7 “Appendix A; determining C_{LK} from C_{add} , f_{RING0} and f_{RING1} ”):

$$C_{LK} = \frac{C_{add}}{x^2 - 1} \quad [2]$$

where:

$$x = \frac{f_{RING0}}{f_{RING1}} \quad [3]$$

So if we measure f_{RING0} (without C_{add}), then add a known C_{add} and measure f_{RING1} , we can determine C_{LK} and L_{LK} (two equations, two unknowns).

$C_{add} = 3200$ pF was added in circuit, and f_{RING1} found to be 22.2 MHz (f_{RING0} previously found to be 31.25 MHz; see Figure 2).

from Equation 3:

$$x = \frac{31.25}{22.2} = 1.41 \quad [4]$$

and from Equation 2:

$$C_{LK} = \frac{3200 \text{ pF}}{1.41^2 - 1} = 3239 \text{ pF} \quad [5]$$

Rearranging Equation 1:

$$L_{LK} = \frac{1}{(2\pi f_{RING0})^2 C_{LK}} \quad [6]$$

So with $f_{RING0} = 31.25$ MHz and $C_{LK} = 3239$ pF:

$$L_{LK} = \frac{1}{(2\pi \times 3.125 \times 10^7)^2 \times 3.239 \times 10^{-9}} = 8.01 \times 10^{-9} H = 8.0 nH \quad [7]$$

and with $f_{RING1} = 22.2$ MHz and $(C_{LK} + C_{add}) = 3239$ pF + 3200 pF = 6439 pF:

$$L_{LK} = \frac{1}{(2\pi \times 2.22 \times 10^7)^2 \times 6.439 \times 10^{-9}} = 7.98 \times 10^{-9} H = 8.0 nH \quad [8]$$

In other words, the calculated value of L_{LK} remains almost unchanged when we add the additional 3200 pF capacitance. This is a good sanity check of the method for determining C_{LK} and L_{LK} .

4 Designing the snubber - theory

If we replace C_S in Figure 4 with a short-circuit, then we simply have the classic RLC circuit found in text books. The response of this circuit to a step change in voltage (that is Q2 turning on) depends on the degree of damping (ζ or zeta) in the circuit; see Figure 5.

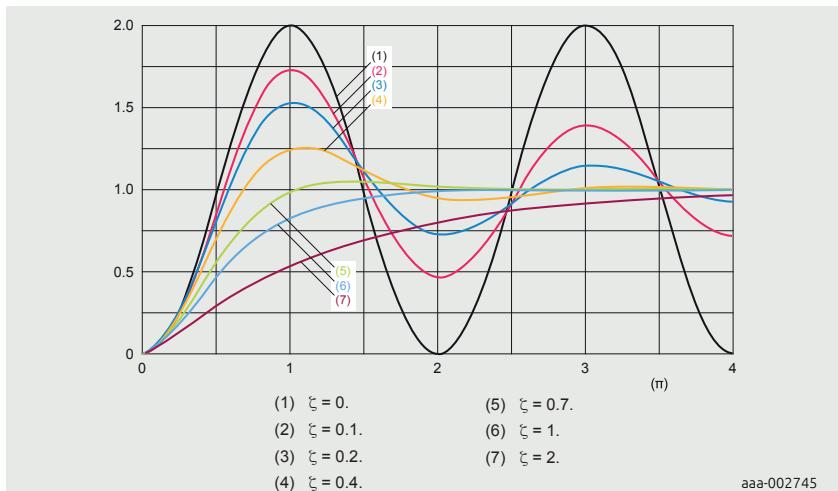


Figure 5 | Step response of an RLC circuit for various values of zeta (ζ)

In theory the circuit oscillates indefinitely if $\zeta = 0$, although this is a practical impossibility as there is always some resistance in a real circuit. As ζ increases towards one, the oscillation becomes more damped that is, tends to decrease over time with an exponential decay envelope. This is an “underdamped” response. The case $\zeta = 1$ is known as “critically damped” and is the point at which oscillation just ceases. For values of greater than one (overdamped), the response of the circuit becomes more sluggish with the waveform taking longer to reach its final value. There is therefore more than one possible degree of damping which we could build into a snubber, and choice of damping is therefore part of the snubber design process.

For this configuration of RLC circuit, the relationship between ζ , R_S , L_{LK} and C_{LK} is:

$$\zeta = \left(\frac{1}{2R_S} \right) \sqrt{\frac{L_{LK}}{C_{LK}}} \quad [9]$$

The snubber capacitor C_S does not appear in Equation 9.

In some circuits, it is possible to damp the oscillations with R_S alone. However, in typical half-bridge circuits we cannot have a resistor mounted directly across Q1 drain source. If we did, then Q1 is permanently shorted by the resistor and the circuit as a whole would not function as required. The solution is therefore to put C_S in series with R_S , with the value of C_S chosen so as not to interfere with normal operation.

The snubber is a straightforward RC circuit whose cut-off frequency f_C is:

$$f_C = \frac{1}{2\pi R_C C_S} \quad [10]$$

Again, we must choose which value of f_C to be used, and there is no single correct answer to this question. The cut-off frequency of the snubber must be low enough to effectively short-circuit the undamped oscillation frequency f_{RINGO} , but not so low as to present a significant conduction path at the operating frequency of the circuit (for example 100 kHz or whatever). A good starting point has been found to be $f_C = f_{RINGO}$.

5 Designing the snubber - in practice

We now have sufficient information to design a snubber for the waveform shown in Figure 2. To recap:

$$C_{LK} = 3239 \text{ pF}$$

$$L_{LK} = 8.0 \text{ nH}$$

$$f_{RINGO} = 31.25 \text{ MHz}$$

$$\zeta = \left(\frac{1}{2R_S} \right) \sqrt{\frac{L_{LK}}{C_{LK}}} \quad [11]$$

$$f_C = \frac{1}{2\pi R_C C_S} = f_{RINGO} \quad [12]$$

The first task is to choose a value of damping (Figure 5). We have chosen $\zeta = 1$, that is, critical damping. Rearranging Equation 11 we have:

$$R_S = \left(\frac{1}{2\zeta} \right) \sqrt{\frac{L_{LK}}{C_{LK}}} = \left(\frac{1}{2} \right) \sqrt{\frac{8.0 \times 10^{-9}}{3.239 \times 10^{-9}}} = 0.78 \Omega \quad [13]$$

use $2 \times 1.5 \Omega$ in parallel to give 0.75Ω .

Rearranging Equation 12 we have:

$$C_S = \frac{1}{2\pi R_S f_{RINGO}} = \frac{1}{2\pi \times 0.75 \times 3.125 \times 10^7} = 6.79 \text{ nF} \quad [14]$$

use $4.7 \text{ nF} + 2.2 \text{ nF}$ to give 6.9 nF .

The snubber was fitted across Q1 drain source. The resulting waveform is shown in Figure 6 together with the original (non-snubbed) waveform from Figure 2

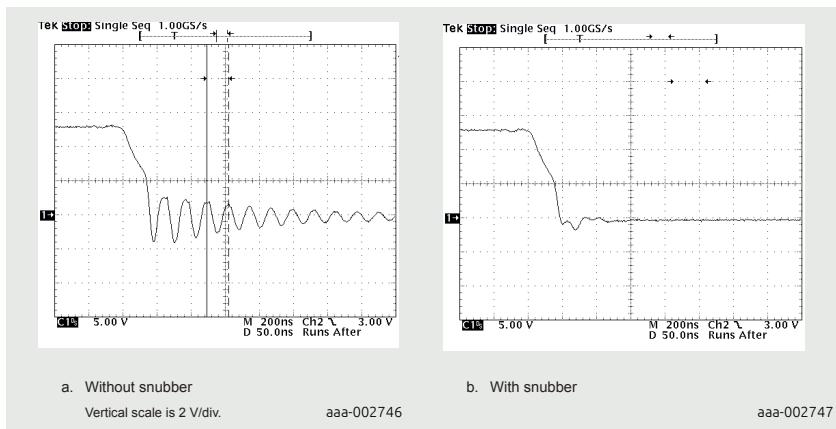


Figure 6 | Q2 V_{DS} waveform with and without snubber

As seen in Figure 6, the snubber has almost eliminated the ringing in the V_{DS} waveform. This technique could also be applied to the MOSFET in the Q2 position.

6 Summary

- Reverse recovery effects in power devices can induce high frequency oscillations in devices connected to them.
- A common technique for suppressing the oscillations is the use of an RC snubber.
- Design of an effective snubber requires the extraction of the circuit parasitic capacitance and inductance. A method has been demonstrated for doing this.
- The snubbed circuit has been shown to be a variation on the classic RLC circuit.
- A method of determining values of snubber components has been demonstrated. The method has been shown to work well, using the example of BUK761R6-40E MOSFETs

7 Appendix A; determining C_{LK} from C_{add} , f_{RING0} and f_{RING1}

We know that:

$$f_{RING0} = \frac{1}{2\pi\sqrt{L_{LK}C_{LK}}} \quad [15]$$

where f_{RING0} is the frequency of oscillation without a snubber in place and L_{LK} and C_{LK} are the parasitic inductances and capacitances respectively.

If we add capacitor C_{add} across Q1 drain-source, f_{RING0} is reduced by an amount "x" where:

$$\frac{f_{RING0}}{x} = \frac{1}{2\pi\sqrt{L_{LK}(C_{LK} + C_{add})}} \quad [16]$$

therefore

$$\frac{1}{2\pi\sqrt{L_{LK}C_{LK}}} = \frac{x}{2\pi\sqrt{L_{LK}(C_{LK} + C_{add})}} \quad [17]$$

$$\frac{1}{\sqrt{L_{LK}C_{LK}}} = \frac{x}{\sqrt{L_{LK}(C_{LK} + C_{add})}} \quad [18]$$

$$\sqrt{L_{LK}C_{LK}} = \frac{\sqrt{L_{LK}(C_{LK} + C_{add})}}{x} \quad [19]$$

$$C_{LK} = \frac{C_{LK} + C_{add}}{x^2} \quad [20]$$

$$C_{LK}x^2 - C_{LK} = C_{add} \quad [21]$$

$$C_{LK}(x^2 - 1) = C_{add} \quad [22]$$

$$C_{LK} = \frac{C_{add}}{x^2 - 1} \quad [23]$$

where:

$$x = \frac{f_{RING0}}{f_{RING1}} \quad [24]$$

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Chapter 7

Half-bridge MOSFET switching and its impact on EMC

Application Note: AN90011

1 Introduction

Measuring and improving MOSFET switching behaviour to meet EMC requirements and optimize reliability and efficiency in half-bridge switching circuits.

Modern switching converters for low voltages (< 100 V) predominantly use power MOSFETs as the switching devices.

Switching converter applications include inverters to synthesise AC waveforms, or for use in DC-to-DC converters. The switching devices are often arranged in a simple half-bridge configuration. At some point in time one of the MOSFETs will be actively switching (sometimes called the control FET in DC-to-DC applications) and the other one will be switched off and acting as a diode during the commutation event – this will be switched on once the switching event has finished and acts as a synchronous rectifier, (in DC-to-DC converters this MOSFET is referred to as a syncFET).

The behaviour of the MOSFETs during the switching event strongly influences efficiency and electromagnetic interference (emissions) goals.

In switch mode (PWM) designs, the switching behaviour of the MOSFET (or more generally the switching power devices) can influence the efficiency and the emissions from the system. This will apply to MOSFETs from any vendor, not just those from Nexperia.

This application note describes a technique to measure the switching efficacy and various measures that can be taken to improve the switching behaviour, thus meeting efficiency, EMC requirements and reliability goals.

2 Double pulse testing

This is a relatively simple method of determining the switching behaviour of a pair of MOSFETs in a half-bridge switching circuit. MOSFET Q1 is switched off and acts only as a diode, MOSFET Q2 is actively switched on and off twice: hence "double pulse testing". The behaviour at a particular current level and DC voltage level can be analysed. This testing is useful for comparing MOSFETs from different suppliers, since the detailed design – the technology - of the devices is unlikely to be exactly the same. Figure 1 shows the simplified schematic diagram of the double pulse test circuit.

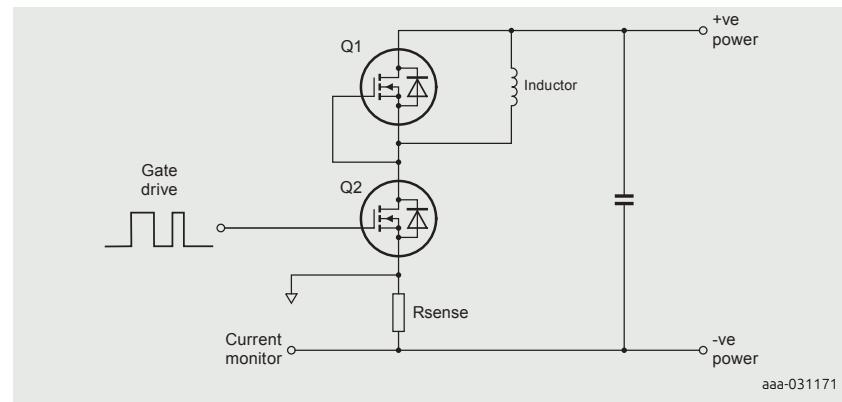


Figure 1 | Simplified schematic diagram of the double pulse test circuit

Simplified switching behaviour is shown in Figure 2

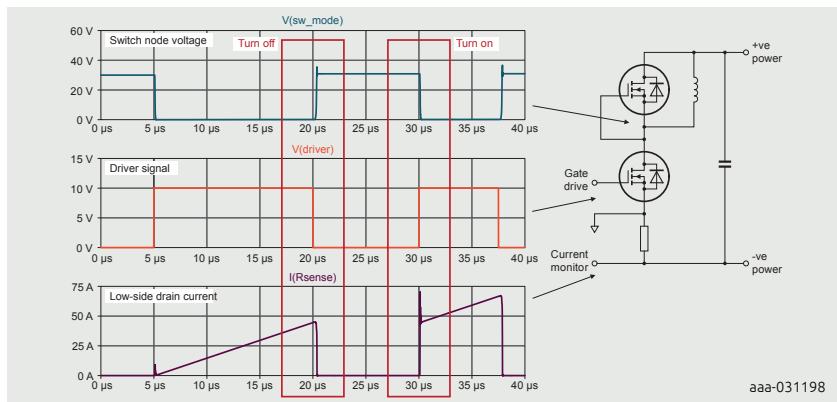


Figure 2 | Simplified switching behaviour

Three waveforms are shown in Figure 2: the top one shows the switch node voltage, the middle one shows the gate driver waveform to the low-side MOSFET and the lower waveform shows the current in the low-side device. The regions of interest are at turn-off of the low-side switch and then at turn-on for the second pulse. Assuming the gap between the first pulse and second pulse is relatively short (but long enough to ensure proper switch off of the switched device before it is switched on again) then the current will be maintained at the target level since the diode will present a voltage of around 1 V to the inductor, so dI/dt will be low.

The MOSFET gate driver can be to the user's choice however Nexperia uses a high current driver so that the external gate drive resistor strongly determines the

switching speed, rather than this being influenced by the gate driver IC itself.

2.1 Measurement system

Current sensing is a critical consideration. A high bandwidth sensor is required. A coaxial shunt is used in Nexperia's test circuit since the bandwidth can be more than 1 GHz however the additional circuit inductance is in the region of 5 nH. Other methods of measuring current are possible such as Rogowski coils, Hall Effect probes or current transformers but these also suffer from various compromises either in bandwidth or significant additional circuit inductance. Some specialist Rogowski based probes can reach ~80 MHz bandwidth. The goal is to have sufficient bandwidth in the current sensor whilst minimising the additional circuit inductance. It may also be a requirement to have isolation of the probe signal from the circuit (especially if double pulse testing is performed on high voltage systems).

Here are a few tips regarding the measurement system: the current rise time may be in the area of up to 5 ns, so the current signal bandwidth would be 70 MHz, $BW \approx 0.35/\text{trise}$, see ref (1). A voltage rise time of 5 ns would also be of 70 MHz. The probe BW should be 3x to 5x signal BW to take into account the 3 dB at the quoted BW. The oscilloscope should therefore have an analogue bandwidth the same or higher than the probes when used with x10 voltage probes ($1\text{ M}\Omega$ input impedance, note that the nominal oscilloscope bandwidth might quoted for a $50\text{ }\Omega$ input impedance). The probes should be correctly compensated before use. The sampling rate needs to be at least 2.5x the analogue bandwidth for reasonable resolution. In this example the probes and oscilloscope would need to be 200 MHz analogue BW minimum and the sampling rate would need to be 500 Msamples/s minimum.

Note also that it can take some time for signals to travel along probe cables so the voltage probes and current probe cables should be the same length or the difference in time delay compensated for: a cable difference of 0.5 m could introduce a time difference of around 4 ns. This could have a significant effect on the measurement of switching energy. It is always worth spending a little time to make sure that the measurement system is correctly set up for accuracy, see ref (1). In double pulse testing, the waveforms of interest are low-side V_{DS} (switch node voltage measured as close to the MOSFET terminals as possible), high-side V_{DS} (may be measured using a differential probe method using high-side V_D minus low-side V_{DS}), low-side V_{GS} and low-side I_D . Ideally high-side V_{GS} should also be measured.

2.2 MOSFET switching simulation

SPICE simulation is used to produce some example waveforms. The BUK7S1R0-40H is used for most of this chapter, except where otherwise stated. The simulation circuit is an approximate model of the physical double pulse test circuit with parasitic elements added, see Figure 3. Nexperia has found that there can be a good correlation between SPICE simulation and physical measurements of the real circuit, as long as the device models are accurate (as is the case for Nexperia MOSFET models) and the circuit is realistically modelled, see Appendix A.

Figure 4 shows the MOSFET turn-off event and Figure 5 shows the MOSFET turn-on event.

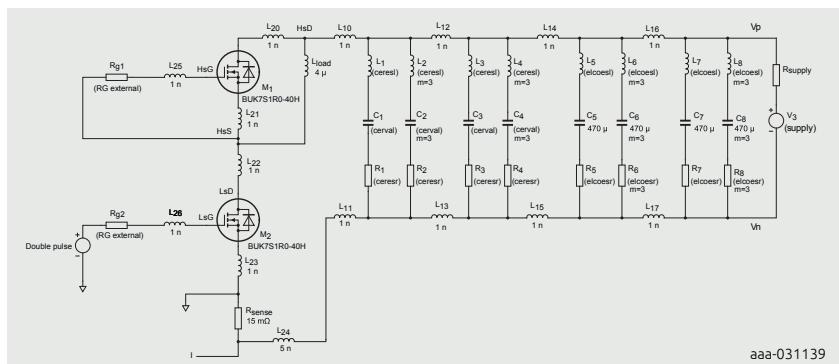


Figure 3 | SPICE simulation circuit for double pulse test circuit

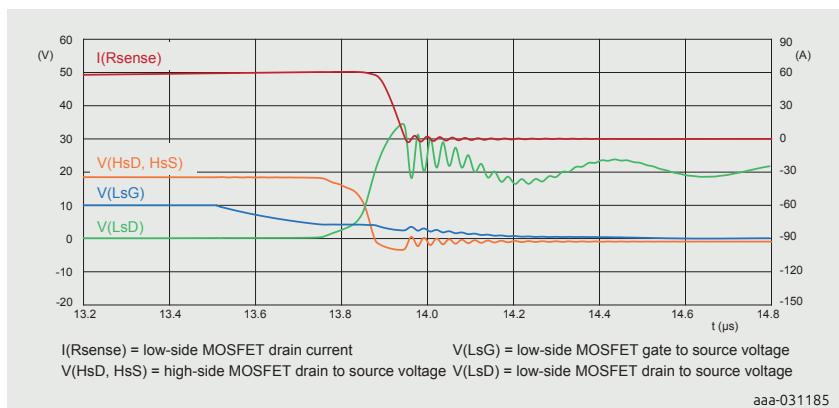


Figure 4 | Turn-off waveform

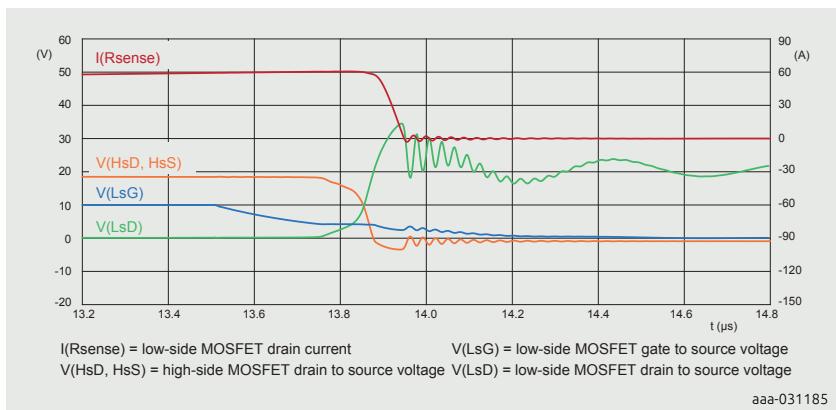


Figure 5 | Turn-on waveform

2.3 MOSFET turn-off waveform description

These waveforms require some explanation as to why they look the way they do. Reference is made to MOSFET capacitances, see Figure 7. Consider first the turn-off waveform in Figure 6. This is divided into 6 time periods t_0 to t_5 .

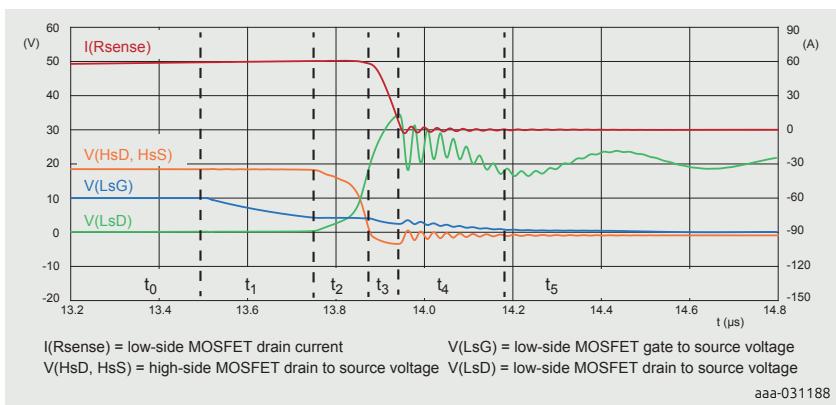


Figure 6 | MOSFET turn-off waveforms, showing reference time periods

During period t_0 , the low-side device is on and the high-side device is off. This is a steady state condition. During time period t_1 , the device turn-off process begins as the gate driver removes charge from the gate capacitance ($C_{ISS} = C_{GS} + C_{GD}$, see Figure 7) of the device and the gate-source voltage starts to fall. V_{DS} rises very

slightly as the $R_{DS(on)}$ of the device begins to increase, in accordance with the "drain-source on-state resistance as a function of gate-source voltage" characteristic found in Nexperia MOSFET data sheets.

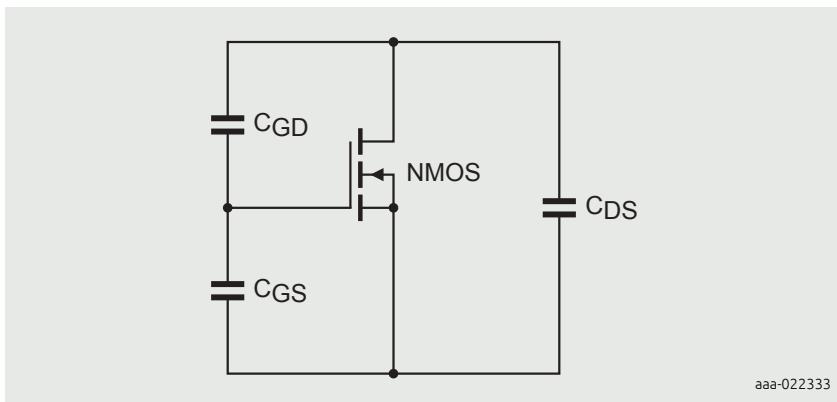


Figure 7 | MOSFET internal capacitances

During t_2 , once V_{GS} falls to the minimum value required to sustain the output inductor current (as determined by the output characteristic, see Figure 8), V_{GS} is approximately constant (this is the "Miller Plateau" and the V_{GS} value = V_p). During this time the gate driver current discharges C_{GD} (causing V_{GS} to fall and V_{DG} to rise), until the switch node voltage has risen to a voltage that allows the diode to conduct current. At this point V_{GS} can fall to its threshold voltage (during t_3) as current is commuted from the low-side MOSFET to the high-side MOSFET body diode.

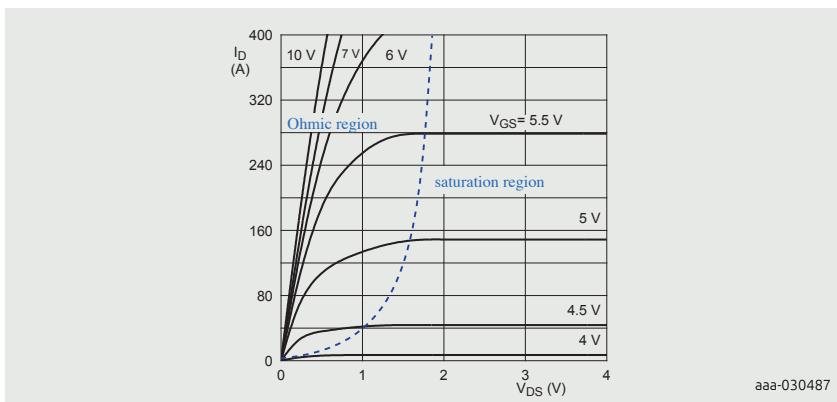


Figure 8 | Example of MOSFET output characteristics

Towards the end of t_2 and moving into t_3 , the low-side MOSFET V_{DS} reaches the level of the DC supply voltage and continues to increase. At this point the body diode of the high-side device can start to turn on and the I_D of the low-side MOSFET can commute to the high-side device.

The rate at which this happens is now controlled by the gate driver discharging C_{iss} as in period t_1 and the incremental slope of the MOSFET transfer curve (transconductance) of the MOSFET (the transfer curve can be found in Nexperia Power MOSFET data sheets). The resulting rate of change of drain current dI_D/dt causes a voltage to be produced across all circuit inductances affected by the change in I_D . Referring to Figure 3, the inductances affected by dI_D/dt include L10, L11, L20, L21, L22, L23 and L24, as well as any component package inductances (for example L1, L2 and others not shown in Figure 3). This is known as the loop inductance. This results in the large voltage overshoot seen on the low-side MOSFET V_{DS} , the overshoot is 14.5 V. The peak value corresponds to the peak dI_D/dt . The equal change of current in the high-side MOSFET source IS results in a small negative voltage spike across the high-side device due to L20 and L21: note that the measuring point for the voltages includes some circuit impedance contribution in this example and that the MOSFET model includes package parasitics.

This also adds to the voltage spike observed on the low-side MOSFET. The total circuit inductance from the capacitors through both MOSFETs is often referred to as the loop inductance. The sum of the layout (PCB) inductances is 10 nH in Figure 3 however another 1 nH comes from the device internal inductances, then there are additional inductances coming from the DC link capacitors and layout which are not so simple to describe. The peak dI_D/dt is 1.1 A/ns in Figure 4 so 12.1 V is due to the inductances and the voltage overshoot is 13.0 V. Note that the high-side body diode is conducting, so this accounts for about 0.7 V of the difference.

At the end of t_3 and start of t_4 , I_D in the low-side MOSFET reaches zero. All the current has transferred to the high-side MOSFET body diode. At this point, the voltage across the low-side MOSFET is still more than 30 V given a supply voltage of 20 V. Oscillation is inevitable and a simple circuit model as shown in Figure 9 illustrates the situation.

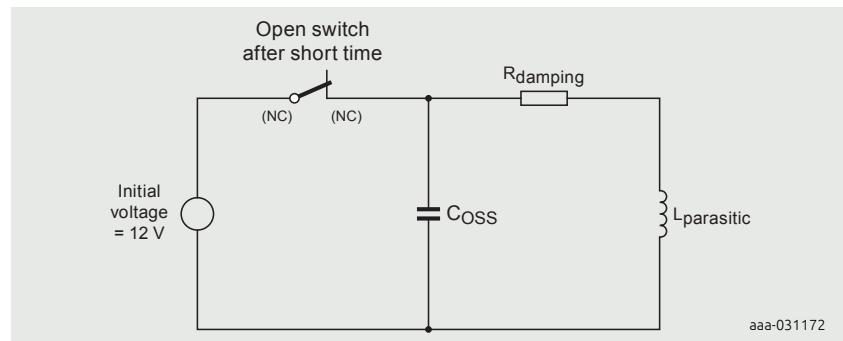


Figure 9 | Oscillation at MOSFET turn-off

C_{OSS} is the low-side MOSFET effective capacitance (C_{DS} in parallel with C_{GD} , C_{GS} is shorted out by the gate driver). This is V_{DS} dependant and the value at 32 V is used in this example). $L_{parasitic}$ is the loop inductance. If C_{OSS} is averaged to 1.6 nF and $L_{parasitic}$ is 11 nH then the oscillation frequency will be 37.9 MHz. This is quite close to the observed oscillation frequency around 35 MHz. The damping resistance which is due to the device construction and resistance due to the layout will reduce the frequency and non-linearity of C_{OSS} results in a slightly bigger effective capacitance being present.

In period t_5 , the MOSFET turn-off switching transition is complete. The low frequency oscillation is due to resonance of the ceramic capacitors with the ESL of the electrolytic capacitors and layout inductance. The resonant frequency is approximately 2 MHz in this example. The ceramic capacitors are 100 nH and the ESL of the electrolytic capacitor is 20 nH in the simulated example, on its own the resonant frequency is calculated at of 3.6 MHz. Factoring in the layout inductance would account for the discrepancy. See Section 3.2.1 for more details about low frequency ringing.

The switching loss in the low-side MOSFET at turn-off, (over the t_2 and t_3 time periods), is given by:

$$\int V(LsD) * I(R_{sense})dt \quad [1]$$

Where $V(LsD)$ = low-side MOSFET drain to source voltage. The switching loss in the high-side MOSFET is negligible.

2.4 MOSFET turn-on waveform description

A typical turn-on waveform is shown in Figure 10. In time period t_0 the low-side MOSFET is off. Current is flowing in the body diode of the high-side MOSFET. During t_1 the gate voltage on the low-side MOSFET starts to rise. Nothing happens until the threshold voltage is reached.

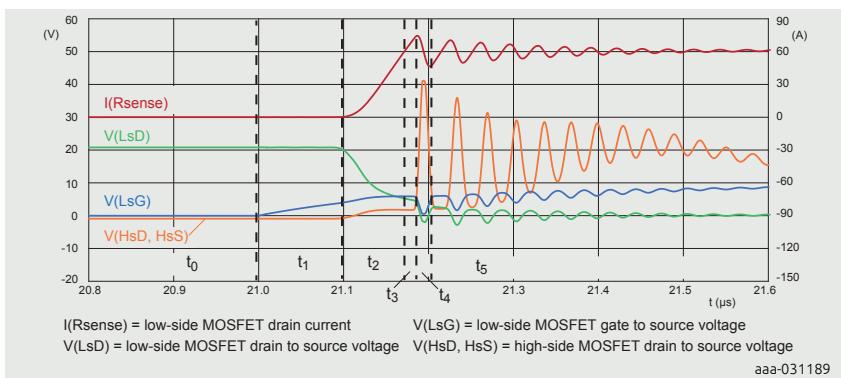


Figure 10 | MOSFET turn-on waveforms, showing reference time periods

At the start of time period t_2 , the gate voltage continues to rise until significant current starts to flow. The rate of change of drain current dI_D/dt increases and then becomes more constant, as defined by the transfer characteristic (see Nexperia MOSFET data sheet) dI_D/dt is also dependant on gate driver current in C_{iss} . The circuit inductances start to interact with the MOSFET. Notice how the MOSFET V_{DS} falls and then plateaus at around 5 V in this example. This corresponds with the highest dI_D/dt observed, interacting with the loop inductance (see Section 2.3). dI_D/dt is therefore limited by the supply voltage and the loop inductance, rather than the MOSFET capability.

Another limitation to dI_D/dt is due to the device source and layout inductance to the connection of the gate drive (represented by L_{23} in Figure 3). Packages with a source clip such as LFPAK will have a higher dI_D/dt capability compared to wire bonded packages such as DPAK due to the package source inductance. Notice also the high-side V_{DS} shows a “hump” due to dI_D/dt interacting with L_{20} and L_{21} (see Figure 3). V_{GS} as observed at the pins of the low-side device is also affected due to inductance of the source leg, the actual V_{GS} applied to the MOSFET die will be fairly constant due to the MOSFET gate capacitance C_{GS} , however the voltage across the package source inductance is added. This can just be observed in Figure 10. At the end of period t_2 the low-side drain current reaches the load inductance current. The low-side V_{DS} doesn't fall at this point. This is because the high-side body diode must be turned off first. Note that the low-side MOSFET is experiencing a relatively high current and also a relatively high V_{DS} , hence there will be some switching loss

associated with this condition.

At the start of time period t_3 , the current in the low-side MOSFET increases beyond the load current. The high-side MOSFET body diode is being switched off, a negative current is flowing in it and the depletion layer inside the body diode is forming in order to support reverse voltage, charge is being stored in the diode junction. This can be considered as a capacitance (sometimes referred to as the diffusion capacitance C_d , the associated charge may be referred to as Q_s). The low-side drain current approaches its peak value.

Once the depletion layer begins to form, the high-side V_{DS} will begin to increase. This happens at the start of period t_4 . The low-side V_{DS} will fall. The low-side drain current will still increase a little further before reaching a peak, partly due to charging the diffusion capacitance C_d but also due to charging the junction capacitance C_J in the high-side body diode. The pn junction can be considered as a parallel plate capacitor, with the distance between the “plates” containing the depletion region as the dielectric material. There comes a point where the current flowing into the depletion region becomes relatively small and the current flowing into the junction capacitance dominates. This is just before the peak current is observed in the low-side MOSFET. The junction capacitance characteristic (especially with respect to V_{DS}) now determines the rate of change of current observed in the body diode and low-side MOSFET. It also determines the rate of rise of the high-side V_{DS} . This is unlike the situation seen during turn-off, where the gate driver and C_{GD} control the dV_{DS}/dt , now this is controlled by the energy stored in the loop inductance and C_{OSS} . The charge stored in C_{OSS} ($C_J = C_{DS}$, $C_{OSS} \approx C_{DS} + C_{GD}$) is referred to as Q_{OSS} . The process of switching off the high-side MOSFET body diode during time periods t_3 and t_4 is known as reverse recovery and is described in ref (5) and other references.

The high-side V_{DS} will usually exceed the nominal DC supply level due to the dI_D/dt and loop inductance. This is referred to as a V_{DS} “spike” and can be problematic. Notice also that the observed low-side V_{GS} waveform shows some oscillations. V_{DS} oscillations are coupled into the MOSFET gate directly as a result of the capacitive divider formed by C_{GD} and C_{GS} (see Figure 7). Secondly, the observed waveform is affected by source lead and layout inductance, represented by L23.

In period t_5 , a high-frequency decaying oscillation is observed superimposed on a lower frequency DC link oscillation. The high-frequency oscillation is due to the resonance of the high-side C_{OSS} and the loop inductance $L_{parasitic}$. The low frequency oscillation is due to the resonance of the DC link ceramic capacitors and inductance of the electrolytic capacitors and circuit layout as discussed in the MOSFET turn-off condition, (see Section 3.2.1). The oscillations decay over time.

The switching loss in the low-side MOSFET at turn on, (over the t_2 , t_3 and t_4 time periods.), is given by:

$$\int V(LsD) * I(Rsense)dt \quad [1]$$

The switching loss in the high-side MOSFET, (over the t4 time period), is given by:

$$\int V(HsD, HsS) * (I(Rsense)-I(Lload))dt \quad [2]$$

3 Methods to improve switching performance

In Section 2, the switch on and switch off transients were explored using double pulse testing. In the waveforms presented, some undesirable effects can be seen such as the large voltage spike on the high-side V_{DS} when the low-side MOSFET switches on, also some oscillations at turn-on and turn-off. This is a cause of unwanted noise which may propagate to the outside world and may interfere with the operation of radio systems but may also cause disturbances in other analogue and digital systems (hence the use of the terms such as electromagnetic compatibility or electromagnetic interference: EMC / EMI).

3.1 Voltage spikes

V_{DS} spikes are observed in both the switch off and switch on waveforms. At low-side turn on, it is possible that the high-side V_{DS} might experience a spike which may reach or exceed the rating of the MOSFET. It is good practice to limit this spike to < 80% of the MOSFET rating to achieve good reliability and also to keep the amplitude of the following oscillations quite small.

The following sections consider some methods to minimise these voltage spikes.

3.1.1 Circuit layout

The loop inductance was described in Section 2.3 and Section 2.4. This total inductance should be minimised as far as possible by using compact layout methods, so that the loop area is reduced: if the loop is considered as a turn of a coil then a large coil diameter will result in a larger self inductance. Furthermore, the magnetic field generated by the loop can interfere with nearby wiring according to Faraday's law.

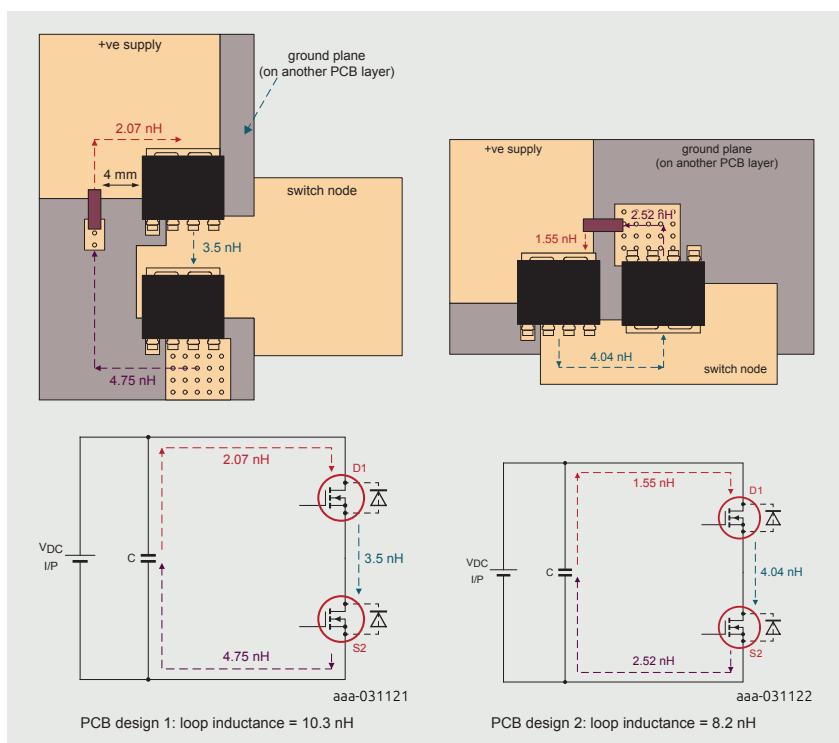


Figure 11 | Half-bridge layout possibilities showing inductances

A layout arrangement as shown in Figure 11 helps to reduce the loop inductance. Design 1 has a loop inductance of 10.3 nH compared to design 2 with a loop inductance of 8.1 nH, according to simulation (ignoring device inductances). Using smaller devices can help to reduce the loop area further.

It was seen in Section 2 that switching behaviour depends on the gate driver voltage and impedance, the package layout source inductance in the gate driver loop and the loop inductance.

3.1.2 Reducing dI/dt

In the case of the low-side MOSFET switch off waveform (Figure 4, Figure 6), the voltage spike depends on the loop inductance and the dI/dt . Since the current is falling, the parasitic inductance will add to the supply voltage as seen at the drain terminal of the MOSFET. The ringing was due to the step voltage change when the drain current (and dI/dt) reaches zero. This can be achieved by slowing the gate drive by some method such as slew rate control at the driver IC, increasing gate

resistance or adding capacitance between gate and source. This will increase the switching time and therefore the switch off loss.

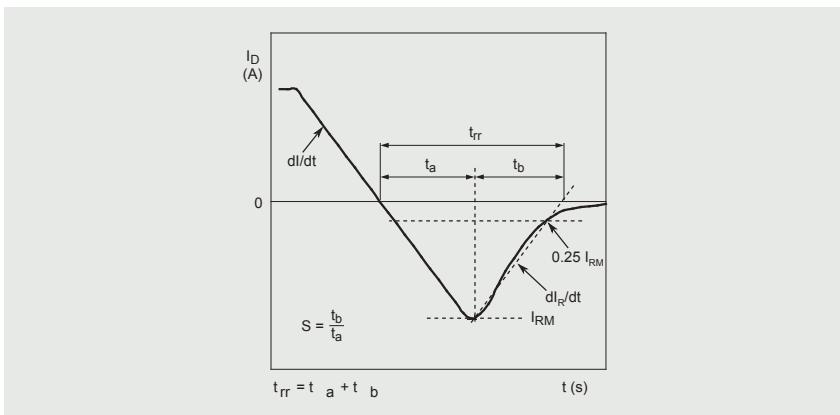


Figure 12 | Reverse recovery waveform definitions

In the case of the low-side MOSFET switch on, it was seen in Figure 10 that there is a significant V_{DS} spike across the high-side MOSFET which is acting as a diode. The spike is due to the loop inductance and dI_R/dt (see Figure 12) which cannot be directly controlled but which is a function of the di/dt that is controllable. The time t_a is approximately constant and it depends on the time it takes for the depletion region to form in the pn junction of the body diode (i.e. recombination time). A higher di/dt will therefore result in a higher I_{RM} value and higher energy in the loop inductance.

di/dt and dI_R/dt are related by the softness factor of the body diode (t_b/t_a), which is reasonably constant over a range of di/dt values. dI_R/dt multiplied by the loop inductance causes a voltage overshoot. This can be absorbed by the MOSFET output capacitance C_{oss} . This capacitance is non-linear with respect to V_{DS} , (see Figure 13), which doesn't help with keeping V_{DS} spikes under control. C_{oss} defines the shape of the t_b region (and consequently the dI_R/dt) and is a characteristic of the MOSFET technology.

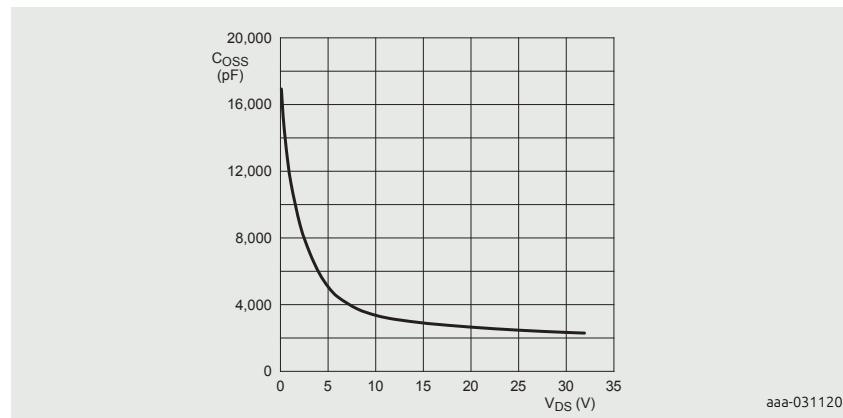


Figure 13 | C_{oss} as a function of V_{DS}

Adding additional capacitance external to the MOSFET can help to “linearise” the capacitance and reduce the V_{DS} spike. This is the capacitance part of an RC snubber.

3.2 Ringing

This occurs because a stimulus is applied to a resonant circuit. In the half-bridge, inductances are usually attributed to the circuit layout and parasitics within the components, usually the loop inductance. Capacitances are attributed to the MOSFETs (e.g. C_{oss}) and bypass capacitors

3.2.1 Bypass capacitors

Bypass capacitors should be placed as close to the half-bridge as possible (to minimise the loop area as discussed in 3.2.1), ideally using surface mount devices. The value should be chosen such that resonance will be well damped. A 100 nF 100 V C0G capacitor has an ESL of approximately 1.1 nH and an ESR of 20 mΩ. A 1 μF 100 V X7R capacitor has similar ESL and ESR. This means that the 1 μF capacitor has a better damping capability compared to the 100 nF capacitor, since the characteristic impedance will be closer in value to the capacitor's ESR. The C0G is a more stable dielectric however a higher capacitance is more beneficial. It was shown that the 2 MHz oscillation is due to the capacitance of the ceramic bypass capacitors and the inductance of the layout and electrolytic capacitors. This is also borne out in practice.

In the example simulation circuit, 100 nF capacitors are compared with 1 μF capacitors, see Figure 14.

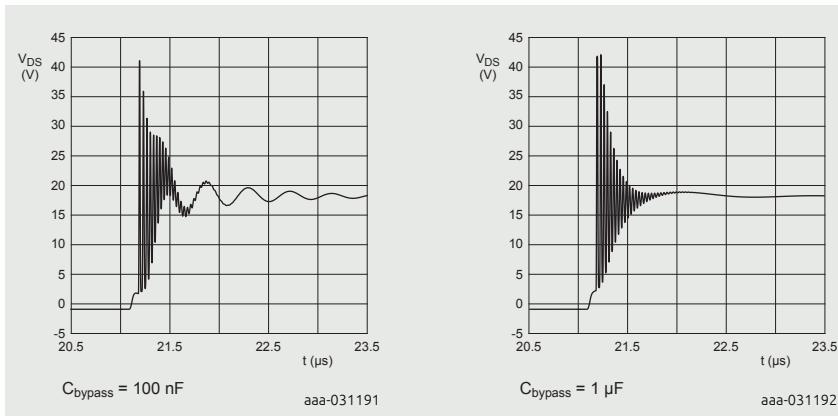


Figure 14 | Effect of bypass capacitor selection: 100 nF vs. 1 μF

The 2 MHz oscillation is shifted to a lower frequency and is a lower amplitude, the ESR and PCB track resistance is providing damping. However the higher frequency oscillation of around 35 MHz remains and is changed only slightly.

3.2.2 Adding a snubber

By adding an RC snubber across the MOSFET drain and source, oscillations can be minimised. AN11160 (chapter 6 in this book) - Designing RC snubbers (ref 3) covers this topic. Another good reference is (ref 4) which proposes a method to optimise the snubber capacitor. The snubber will attenuate the unwanted high frequency oscillations as shown in Figure 15. A 10 nF + 2.2 Ω snubber is applied to the high-side and low-side devices. V_{DS} for the high-side device is shown at low-side turn-on (i.e. high-side body diode turn-off). This also damps the oscillations at low-side turn-off. SPICE programs allow a sweep of parameters to give an indication of the snubber values which are likely to give the desired outcome.

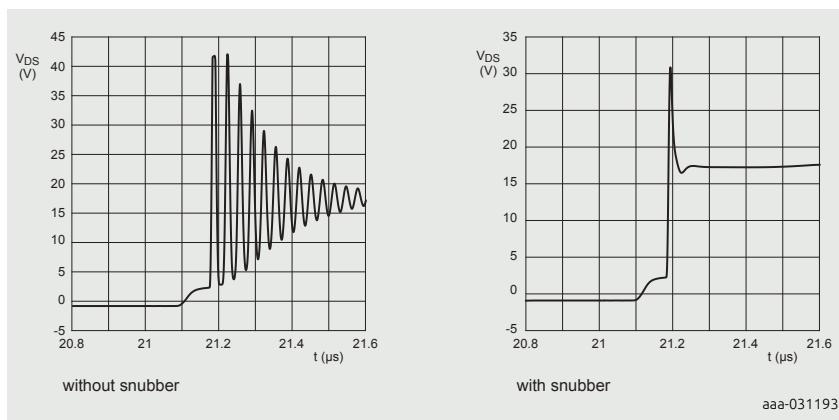


Figure 15 | Effect of adding a snubber

3.3 Feedback into the gate signal

There is a risk of feedback into the gate signal due to high dV_{DS}/dt . If this exceeds the gate threshold voltage ($V_{GS(th)}$) then a significant shoot through current can flow in the half-bridge. This is due to the MOSFET capacitances C_{GD} , C_{DS} and the external gate drive resistance forming a potential divider. If a shoot through current occurs, this will significantly increase the switching losses. This is illustrated in Figure 16, see ref (7).

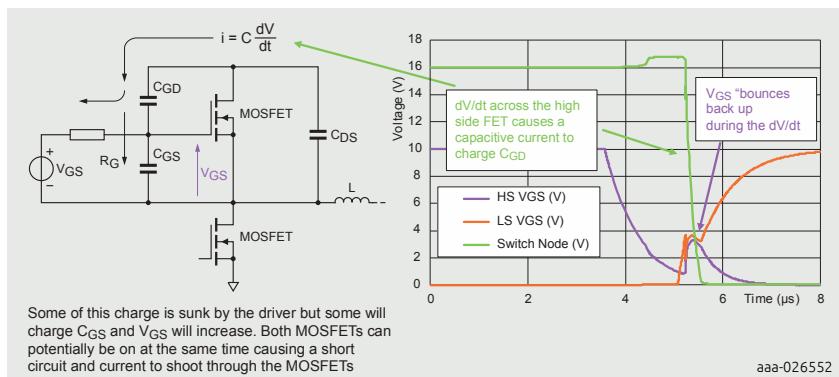


Figure 16 | Dynamic behaviour of a MOSFET half-bridge

Additional external capacitance is used to control dV/dt . C_{rss} is relatively small and non-linear giving rise to gate glitches and sudden shoot through current. The external capacitance would be much larger in value and quite linear, producing a controlled dV/dt . See section 3.4.2.

3.4 Switching speed control

3.4.1 Effect of varying R_G

Varying the external gate resistance will affect switching losses in the low-side MOSFET; see Figure 17, Figure 18 and Figure 19. In this case, measurements have been made using the BUK7S1R5-40H.

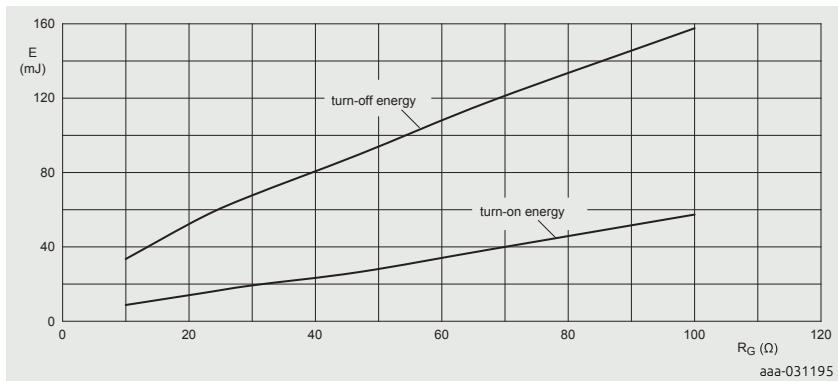


Figure 17 | Effect of varying R_G on switching loss (example values only)

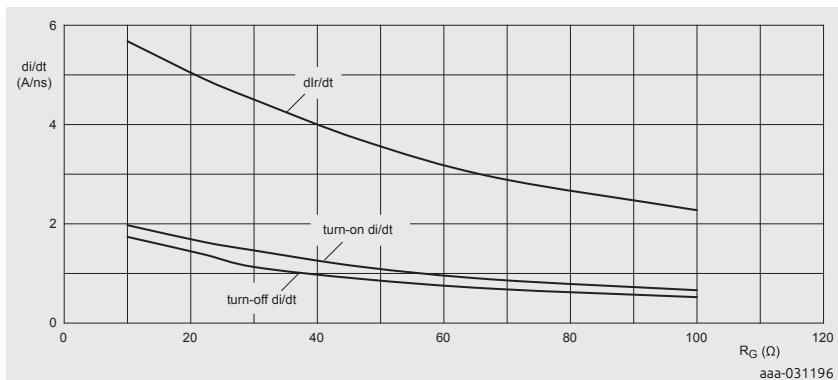


Figure 18 | Effect of varying R_G on di/dt , dI/dt and turn-off di/dt (example values only)

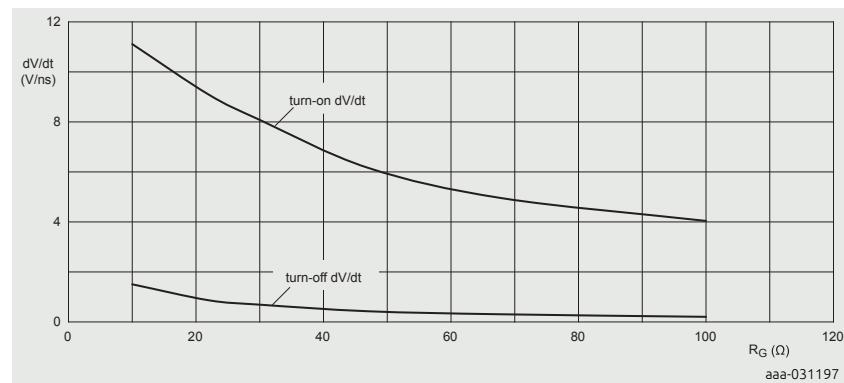


Figure 19 | Effect of varying R_G on turn-on dV/dt and turn-off dV/dt (example values only)

Increasing R_G will increase switching loss but the benefit is better controlled switching and improvements in spiking and ringing. There may also be an increased risk of gate bounce so it may be necessary to add a small capacitor between gate and source.

For best performance, R_G for turn-on should be large than R_G for turn-off. di/dt is controlled by the V_{GS} value around the Miller plateau voltage V_p :

$$I_G = (V_{GS} - V_p) / R_G \text{ for example:}$$

$$I_{G(on)} = (10 - 4.3) / 10 = 0.57 \text{ A}$$

$$I_{G(off)} = (0 - 4.3) / 10 = -0.43 \text{ A}$$

Hence turn on di/dt may be different to turn off di/dt depending on the value of R_G . di/dt can also be controlled by carefully selecting the location of the gate drive ground connection point, this is equivalent to adjusting L23 in Figure 3.

3.4.2 Effect of adding external gate to source capacitance

In case of gate bounce risk, (see Section 3.3), an external C_{GS} can be added to reduce the high frequency impedance of the gate driver whilst still having relatively high R_G . The effect on switching speed (dl/dt) is relatively modest, as seen below in Figure 20. This is for a BUK7S1R0-40H with an R_G external value of 22 Ω.

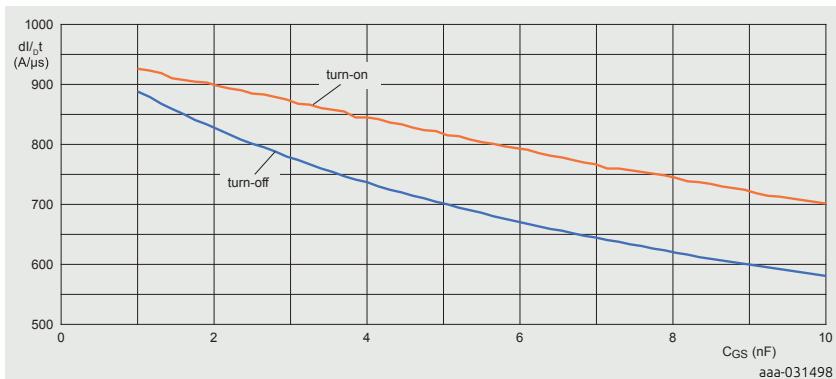


Figure 20 | C_{GS} effect on MOSFET dI/dt

3.4.3 Effect of adding gate to drain capacitance

Adding some drain voltage feedback via a gate – drain capacitor would reduce dV/dt without affecting dI/dt and will reduce the voltage spike at turn-off. Losses are increased. Reducing dV/dt is beneficial because in a motor drive, the switch node voltage is presented directly to the motor windings. The motor windings can act as antennae so that the frequency domain content of the waveform can radiate into the environment. The highest frequency component of the waveform will be approximately 0.35/rise time or 0.35/fall time.

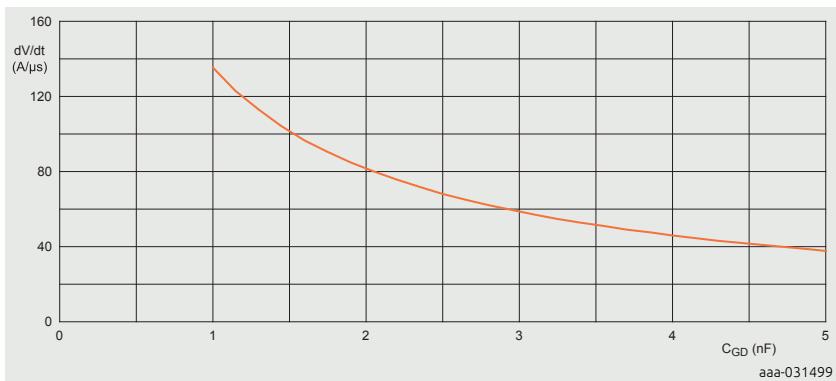


Figure 21 | External C_{GD} effect on controlling MOSFET turn-off

Figure 21 shows the effect of adding a capacitor to a BUK7S1R0-40H with a series resistor of 10 Ω. Usually a series resistor R_{GD} is added to C_{GD} in order to prevent oscillations, see Figure 22. The value of C_{GD} can be in the range of 1 – 5 nF for a

device such as BUK7S1R0-40H, much bigger than the value of the MOSFET internal C_{rss} . The value of R_{GD} can be in the range of $10 - 50 \Omega$ for this device, higher values start to diminish the effect of having the external C_{GD} . Note that Figure 22 applies to the low-side controlling switch in the case of the double pulse test circuit.

In the case of the MOSFET acting as a synchronous rectifier then the effect of adding external C_{GD} will reduce dV/dt however the value of dV/dt can be much higher. See Figure 23.

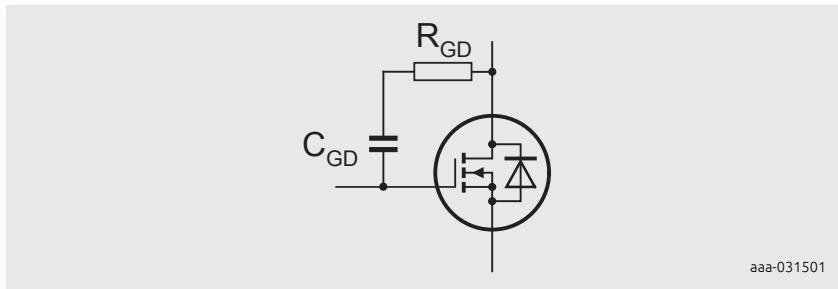


Figure 22 | Adding C_{GD} and R_{GD}

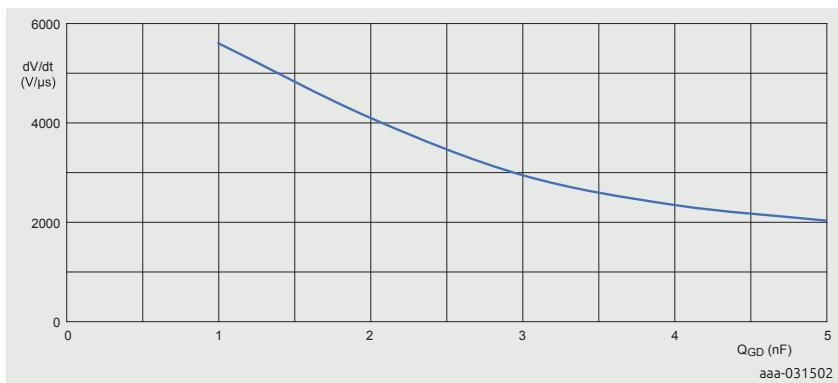


Figure 23 | External C_{GD} effect on the synchronous rectifier MOSFET

It is recommended that some SPICE simulation is performed first before experimenting to determine the optimum values of external resistors and capacitors.

4 Impact on EMC and efficiency

The significant voltage transients and oscillations which have been described in Section 2 are the source of electromagnetic interference. This must be suppressed in order to meet CISPR25 based requirements for automotive and CISPR 11 and the like for industrial, telecoms and consumer equipment. These kinds of standards consider conducted and radiated emissions. How do these transient voltages and currents cause interference? In the next paragraphs, emissions from digital circuits will be ignored however the same basic principles apply, the difference being that the voltages are much lower than in the power circuit and the frequency rise and fall times are much faster.

In an ideal PWM controlled half-bridge MOSFET circuit, it is still necessary to take care of EMI by using screening and filters. This is because simple analysis of the half-bridge waveforms feature rectangular blocks of current with fast rising and falling edges from the DC link and the output switch node will feature fast rising and falling voltages. See Figure 24.

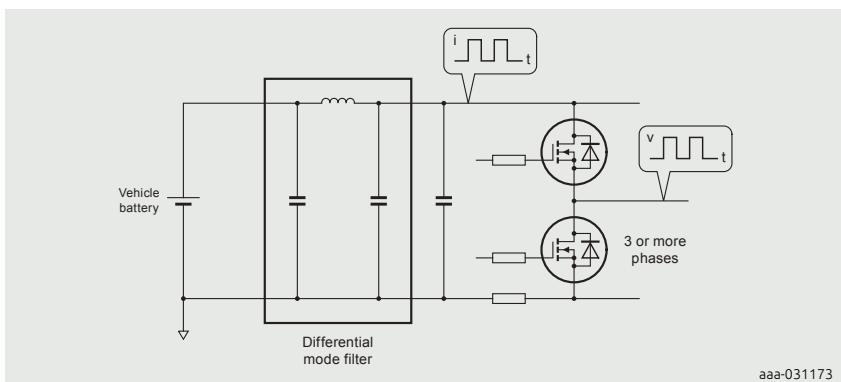


Figure 24 | Sources of electromagnetic noise in a half-bridge circuit

5 Conclusions

This chapter is intended to give the reader a reasonably detailed understanding of how the half-bridge switching circuit is a source of electromagnetic noise and power loss. In particular, the reverse recovery characteristic of the MOSFET body diode can be a key factor to achieving good EMC behaviour and lower losses. Some techniques to reduce switching noise at source have been considered and a brief overview of how the noise propagates to the outside world have been considered.



Benefits of low Q_{rr}
MOSFETs in motor
control applications



Benefits of low Q_{rr}
MOSFETs in switching
applications



Developing reliable
MOSFETs how difficult
can it be



Visit blog
Q_{rr} overlooked and
underappreciated in
efficiency battle



Visit blog
Automotive Trench 9
Power MOSFETs designed
for performance and
endurance

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7 Appendix A: Comparison between SPICE simulation and practical measurements for the BUK7S1R0-40H in a double pulse test circuit

The SPICE circuit used is as shown in Figure 3. The following values were used in the simulation: ceresr = 20 m, ceresl = 1.13 n, cerval = 100 n, cerval1 = 100 n, elcoesr = 40 m, elcoesl = 20 n.

Both turn-on and turn-off conditions are considered.

SPICE model is modified from standard: TT parameter is approximately half of published value (to give better reverse recovery alignment with double pulse measurements).

The following test conditions were applied: $R_G = 30 \Omega$, $I_L = 60 \text{ A}$, $V_{DC} = 20 \text{ V}$.

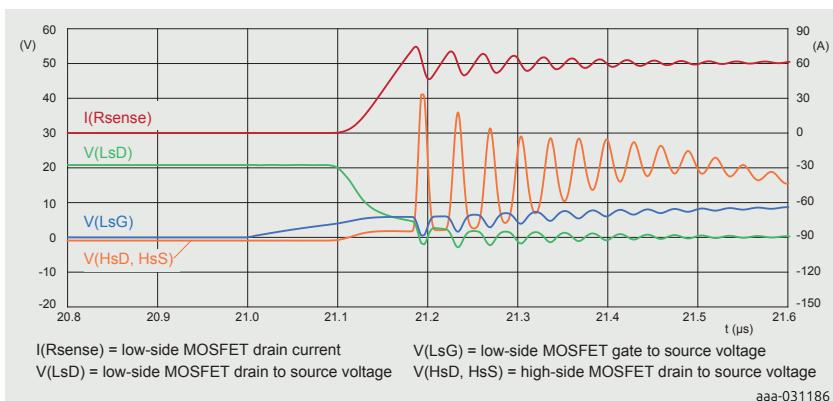


Figure 25 | SPICE turn-on waveform

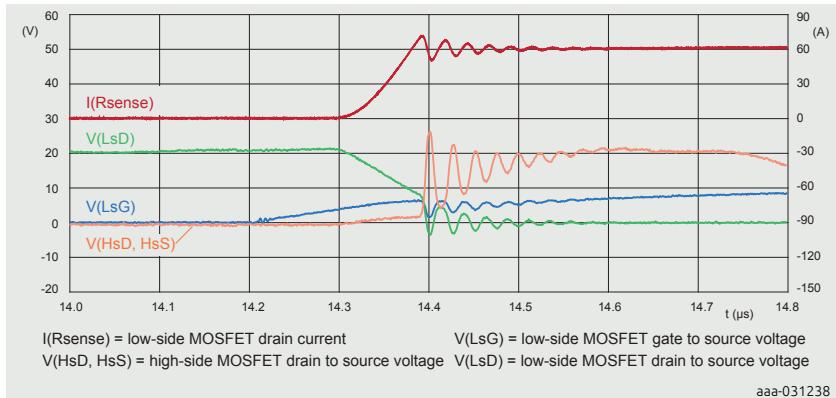


Figure 26 | Measurement turn-on waveform

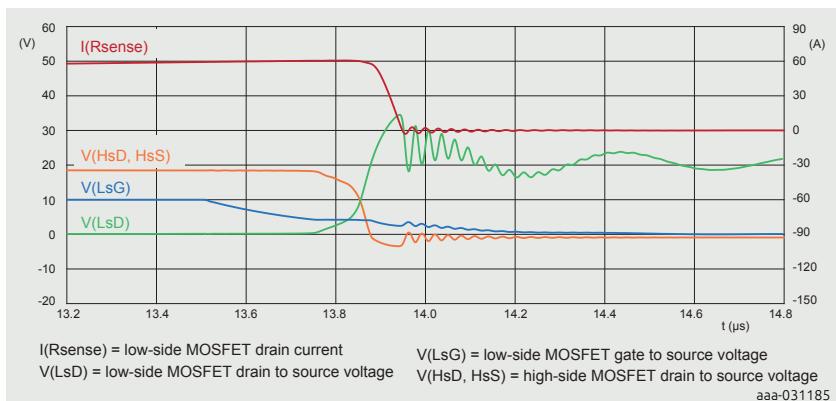


Figure 27 | SPICE turn-off waveform

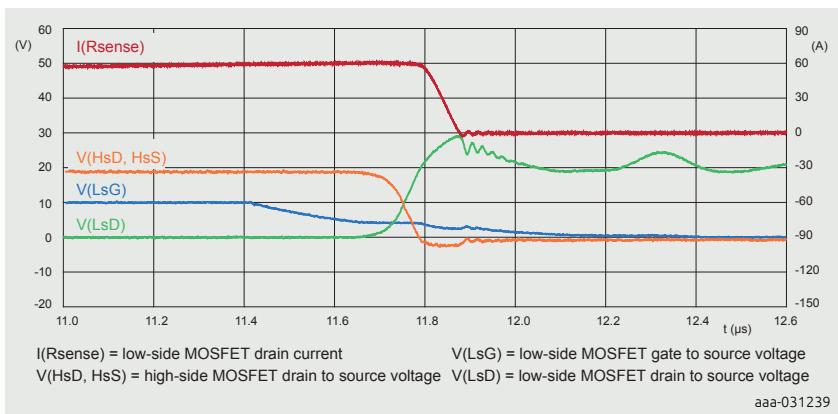


Figure 28 | Measurement turn-off waveform

Table 1: Meausrement and SPICE simluation values

	Turn-on (measured)	Turn-on (SPICE)		Turn-off (measured)	Turn-off (SPICE)
dI/dt	1.12 A/ns	1.12 A/ns	dI/dt	0.82 A/ns	1.05 A/ns
dI_{R}/dt	2.96 A/ns	2.78 A/ns	dV/dt	0.31 V/ns	0.45 V/ns
ΔI_{RM}	10.09 A	12.2 A	$V(LsD)$	29 V	34.2 V
t_a	11.43 ns	12.8 ns	-	-	-
t_b	5.17 ns	7.2 ns	-	-	-
dV/dt	4.54 V/ns	5.7 V/ns	-	-	-
$V(HsD, HsS)$	27 V	41.2 V	-	-	-

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Chapter 8

Failure signature of electrical overstress on power MOSFETs

Application Note: AN11243

1 Introduction

When Power MOSFETs fail, there is often extensive damage. Examination of the size and location of the burn mark, the failure signature, provides information about the type of fault condition which caused the failure. This chapter provides a catalogue of failure signatures from common electrical overstress failure modes. The catalogue can be used in forensic investigation of the underlying root cause of failure to improve module design and reliability.

Power MOSFETs are used to switch high voltages and currents, while minimizing their own internal power dissipation. Under fault conditions however, it is possible to apply voltage, current and power exceeding the MOSFET capability. Fault conditions can be either due to an electrical circuit failure or a mechanical fault with a load such as a seized motor. This leads to Electrical Overstress (EOS). Typically the consequence of EOS is the short circuiting of at least 2 of the 3 MOSFET terminals (gate, drain, source). In addition, high local power dissipation in the MOSFET leads to MOSFET damage which manifests as burn marks, die crack and in extreme cases as plastic encapsulation damage.

Examination of the size and location of the burn mark, the failure signature, provides information about the type of fault condition which caused the failure. Common fault conditions are:

- ElectroStatic Discharge (ESD)
- Unclamped Inductive Switching (UIS) - commonly called Avalanche or Ruggedness
- Linear Mode operation
- Over-current

Packaged MOSFETs have been deliberately destroyed under these conditions. Images recorded of the ensuing burn marks on the silicon surface, provide a 'Rogue's Gallery' to aid the explanation of EOS failures.

Section 1.1 to Section 1.4 gives an overview of the common failure signatures. Appendices in Section 2.1 to Section 2.17 provide further images.

1.1 ESD - Human body model

1.1.1 EOS method

ESD pulses were applied using a standard Human-body Model ESD circuit; for details see *AEC - Q101 - REV - May 15, 1996*. Voltage of the applied pulse was progressively increased until device failure was observed.

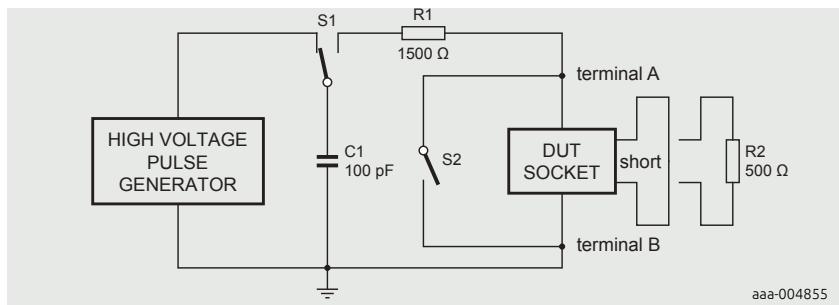


Figure 1 | Typical circuit for Human body Model ESD simulation

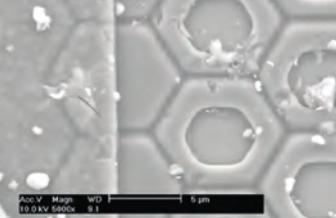
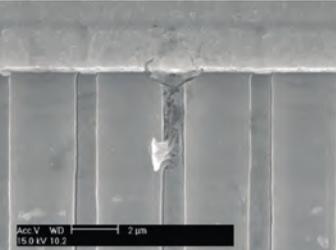
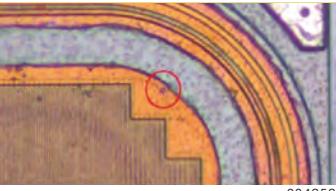
1.1.2 Fault condition simulated

Human body model ESD simulates situations when a voltage spike is applied to the MOSFET exceeding the maximum voltage that can be sustained by the gate oxide of either gate-source or gate-drain. The pulse is applied with $1500\ \Omega$ series resistance between the voltage origin and the MOSFET, which limits the rate of rise of the MOSFET gate voltage. Either human handling, electrical test equipment or malfunctioning circuits can easily apply such voltage pulses.

1.1.3 Signature

Failure site is found in an edge cell of the MOSFET structure. Outer edge cells and cells near the gate are the first to be subjected to the incoming voltage pulse and are thus the first sites where the voltage exceeds the gate-oxide capability. The signature differs from Machine Model failures in that the fail site does not show such a strong tendency to group near the gate, due to the slower rise in gate voltage.

Table 1: Examples of Human Body Model ESD failure signature

Device name	Cell pitch (μm)	Image	Comments
BUK9508-55A	9 (hexagon)		Fail site is gate oxide of edge cell; see Section 2.1 "Human body model EOS of BUK9508-55A" for further images aaa-004856
BUK9Y40-55B	4 (stripe)		Fail site is gate oxide of edge cell; see Section 2.2 "Human body model EOS of BUK9Y40-55B" for further images aaa-004857
PSMN011-30YL	2 (stripe)		Fail site is gate oxide of edge cell; see Section 2.3 "Human body model EOS of PSMN011-30YL" for further images aaa-004858
PSMN8R5-100PSF	2.5 (stripe)		Fail site is gate oxide of edge cell, see Section 2.4 "Human body model EOS of PSMN8R5-100PSF" for further images.
BUK7Y3R0-40H	1.5 (stripe)		Fail site is gate oxide of edge cell, see Section 2.5 "Human body model EOS of BUK7Y3R0-40H" for further images.

1.2 Unclamped Inductive Switching (UIS) (Avalanche or Ruggedness)

1.2.1 EOS method

Inductive energy pulses were applied using a standard UIS circuit; for details see AEC - Q101-004 - REV - May 15, 1996. A fixed inductance value is selected. Current in the inductor prior to switching the MOSFET was progressively increased until device failure was observed.

Table 2. UIS ruggedness test circuit and waveforms

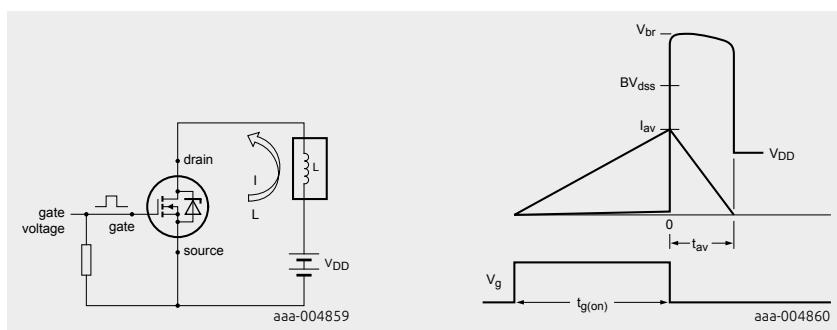


Figure 2 | Circuit diagram for UIS ruggedness test

Figure 3 | Waveforms obtained from UIS test

1.2.2 Fault condition simulated

UIS simulates situations when a MOSFET is switched off in a circuit in which there is inductance. The inductance can be deliberate (such as an injector coil in a diesel engine system), or parasitic. As the current cannot decay to zero instantaneously through the inductance, the MOSFET source-drain voltage increases to take the device into avalanche breakdown. The energy stored in the inductance is then dissipated in the MOSFET.

1.2.3 Signature

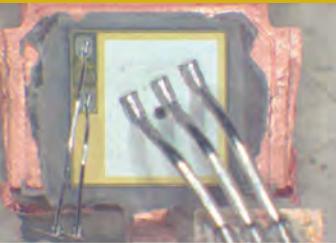
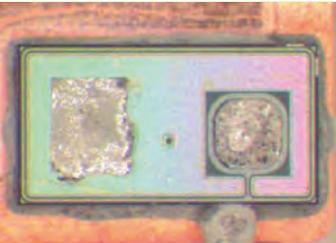
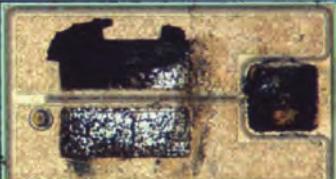
Failure site is found in an active MOSFET cell. The burn-mark is usually round in shape, indicating a central failure site and subsequent thermal damage.

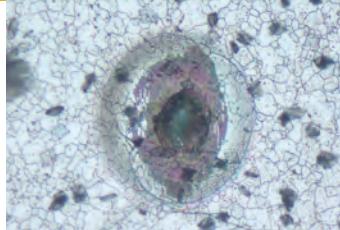
If the avalanche event is long in duration (~ ms), then burn marks locate at central sites on the die, where there is maximum current flow and reduced heat

dissipation. The sites are often adjacent to wire bonds/clip bonds where current density is high, but not directly under the wire bond/clip bond as it provides a local heat sink. Failure is at the hottest location of the die.

For short avalanche events ($\sim \mu\text{s}$), the burn marks can take on more random locations over the die surface. The temperature rise in the chip is more uniform with negligible chance for current crowding and local heating on these time scales. For even shorter avalanche events, the burn marks can locate at die corners due to the discontinuity in cell structure at these locations.

Table 3: Examples of Unclamped Inductive Switching failure signature

Device name	Cell pitch (μm)	Image	Comments
BUK7L06-34ARC	9 (hexagon)	 aaa-004861	Round burn in active area; see Section 2.6 “Unclamped inductive switching EOS of BUK7L06-34ARC” for further images
BUK9Y40-55B	4 (stripe)	 aaa-004862	Round burn in active area; see Section 2.7 “Unclamped inductive Switching EOS of BUK9Y40-55B” for further images
PSMN7R0-30YL	2 (stripe)	 aaa-004863	Round burn in active area; see Section 2.8 “Unclamped inductive switching EOS of PSMN7R0-30YL” for further images

Device name	Cell pitch (μm)	Image	Comments
PSMN8R5-100PSF	2.5 (stripe)		Round burn in active area; see Section 2.9 "Unclamped inductive switching EOS of PSMN8R5-100PSF" for further images.
BUK7Y3R0-40H	1.5 (stripe)		Round burn in active area; see Section 2.10 "Unclamped inductive switching EOS of BUK7Y3R0-40H" for further images.

1.3 Linear mode operation

1.3.1 EOS method

A Safe Operating Area (SOA) graph is included in all power MOSFET data sheets. Outside the defined safe region, the power dissipated in the FET cannot be removed, resulting in heating beyond the device capability and then device failure. MOSFETs were taken and a fixed source-drain voltage applied. Current pulses of defined duration were applied and the current was increased until MOSFET failure was observed.



Figure 4 | Safe operating area; continuous and peak drain currents as a function of drain-source voltage

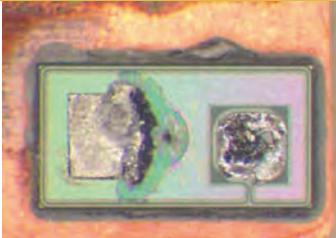
1.3.2 Fault condition simulated

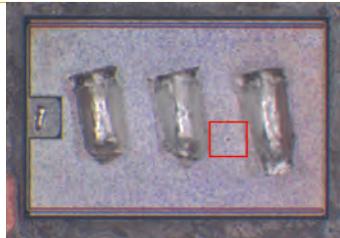
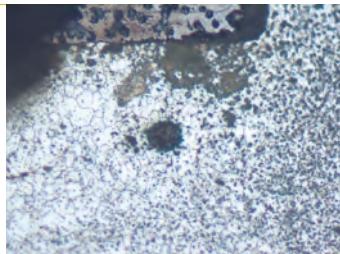
Linear mode operation is common during device switching or clamped inductive switching and is not a fault condition unless the SOA is exceeded. Linear mode EOS simulates situations when a MOSFET is operated in Linear mode for too long. This situation can also occur if, when intending to turn the FET on, the gate signal voltage to the FET is too low. This condition can also arise when intending to hold the FET in the Off-state with high drain-source voltage. If the gate connection is lost, the gate voltage capacitively rises and the same Linear mode fault condition occurs.

1.3.3 Signature

The hottest location of the die is a failure site that is usually at central sites on the die. The center of the die is where there is maximum current flow and reduced heat dissipation. The sites are often adjacent to wire bonds/clip bonds where current density is high, but not directly under the wire bond/clip bond as it provides a local heat sink.

Table 4: Examples of linear mode failure signature

Device name	Cell pitch (µm)	Image	Comments
BUK7L06-34ARC	9 (hexagon)	 aaa-004865	Burns located in center of die adjacent to wire-bonds; see Section 2.11 "Linear mode EOS of BUK7L06-34ARC" for further images
BUK9Y40-55B	4 (stripe)	 aaa-004866	Burn adjacent to location of clip bond in center of die; see Section 2.12 "Linear mode EOS of BUK9Y40-55B" for further images

Device name	Cell pitch (μm)	Image	Comments
PSMN7R0-30YL	2 (stripe)		Burn adjacent to location of clip bond in center of die; see Section 2.13 "Linear mode EOS of PSMN7R0-30YL" for further images aaa-004867;
PSMN8R5-100PSF	2.5 (stripe)		Burn between source bond wires in active area, see Section 2.18 "Linear mode EOS of PSMN8R5-100PSF" for further images
BUK7Y3R0-40H	1.5 (stripe)		Burn close to the source clip location in the active area, see Section 2.19 "Linear mode EOS of BUK7Y3R0-40H" for further images

1.4 Over-current

1.4.1 EOS method

The maximum current-handling capability is specified on the data sheet for Power MOSFETs. This capability is based on the current handling capability of wires or clips, before which fusing will onset, combined with the ability to dissipate heat. Exceeding this rating can result in catastrophic failure.

I_D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 100^\circ\text{C}$; see Figure 1	-	53	A
		$V_{GS} = 10 \text{ V}; T_{mb} = 25^\circ\text{C}$; see Figure 1	-	76	A
I_{DM}	peak drain current	$t_p \leq 10 \mu\text{s}$; pulsed; $T_{mb} = 25^\circ\text{C}$; see Figure 3	-	260	A
aaa-005071					

Figure 5 | Example of maximum current rating from the data sheet of PSMN7R0-30YL

1.4.2 Fault condition simulated

Over-current occurs if a FET is turned on with no element in the circuit to limit the current, resulting in a supply voltage being applied fully over the drain-source terminals of the FET. Typically this occurs if a load has been short-circuited. Alternatively if 2 FETs are operating in a half-bridge, over-current can ensue if both are turned on together.

1.4.3 Signature

Failure site is initially where the current handling connections (wires or clips) meet the die. Normally damage is extensive however in over-current conditions, and spreads over the entire die surface with evidence of melted metallization and solder joints.

For wire-bonded packages, there is often evidence of fused wires. For clip-bonded packages, die crack is commonly observed.

Table 5: Examples of over-current failure signature

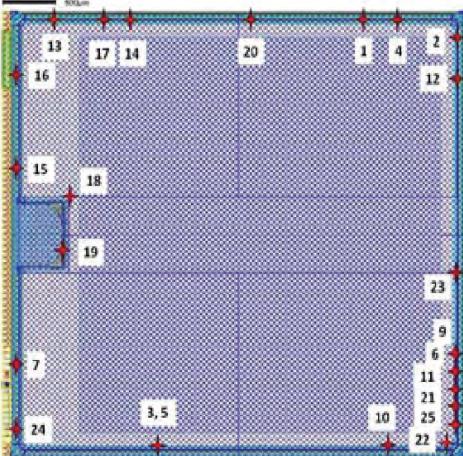
Device name	Cell pitch (μm)	Image	Comments
BUK7L06-34ARC	9 (hexagon)	 aaa-004868	Burns located in center of die adjacent to wire-bonds. Secondary damage of remelted top metal and solder die attach; see Section 2.14 "Over-current EOS of BUK7L06-34ARC" for further images

Device name	Cell pitch (μm)	Image	Comments
PSMN7R0-30YL	2 (stripe)		Burn adjacent to location of clip bond in center of die; see Section 2.1.5 “Over-current EOS of PSMN7R0-30YL” for further images aaa-0048691

2 Appendices

2.1 Human Body Model EOS of BUK9508-55A

Table 6: Human body model EOS

BUK9508-55A
<p>Cell structure: 9 mm hexagons Package: TO-220 Die size: 5.5 mm x 4.5 mm EOS condition: 5 kV HBM pulse</p>  <p>aaa-004899</p>

Fails located in edge cells, distributed around edge of device

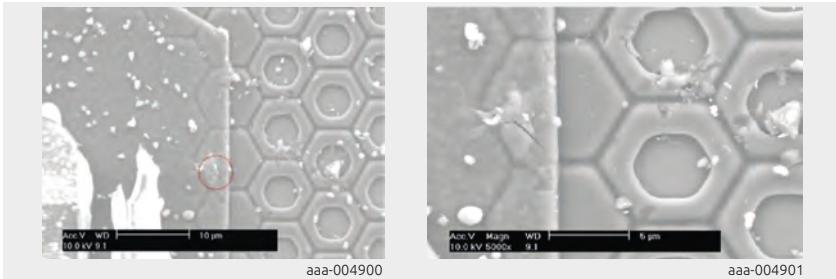


Figure 6 | Sample image 4; after Al removal

Figure 7 | Sample image 4; after Al removal, close-up

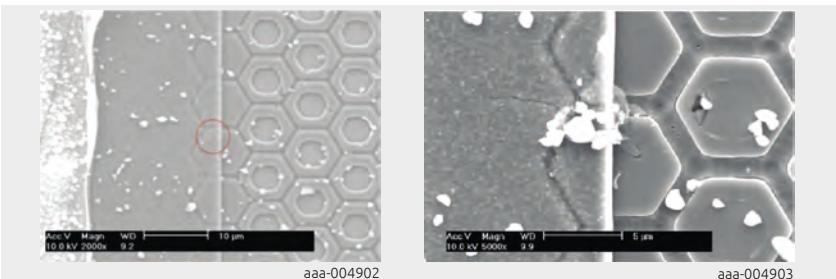
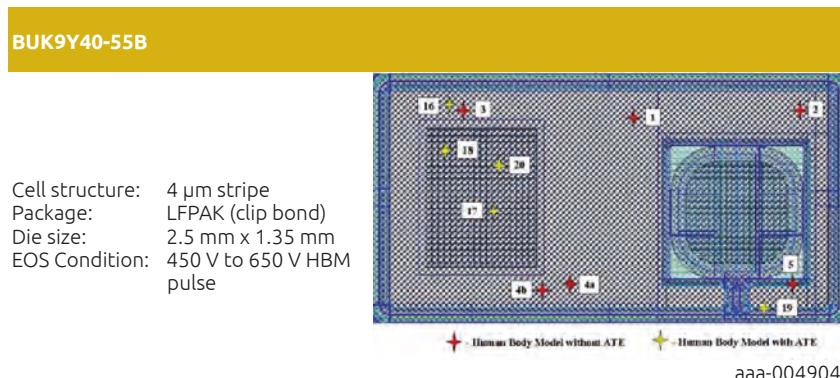


Figure 8 | Sample image 19; after Al removal

Figure 9 | Sample image 19; after TEOS removal, close-up

2.2 Human Body Model EOS of BUK9Y40-55B

Table 7: Human body model EOS



Fails located randomly over die with increased grouping in edge cells. Some fails subjected to ATE testing to create additional damage to highlight fail site

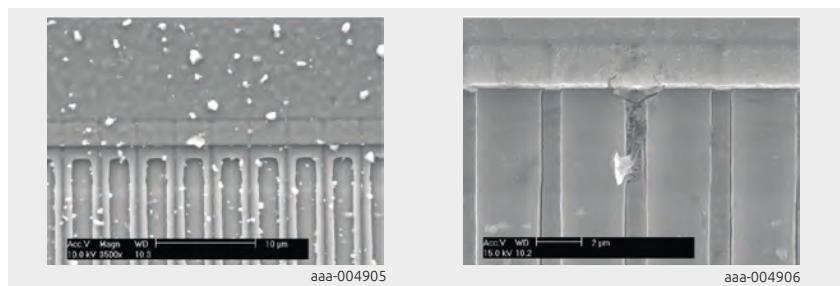
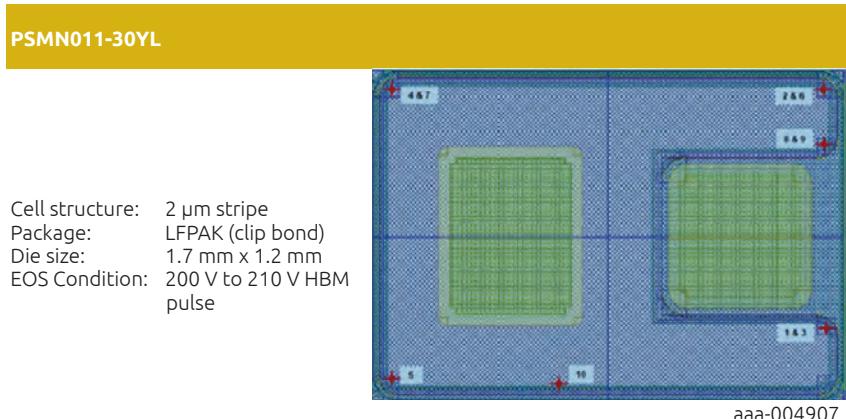


Figure 10 | Sample image 5; after Al removals

Figure 11 | Sample image 5; after TEOS removal, close-up

2.3 Human Body Model EOS of PSMN011-30YL

Table 8: Human body model EOS



Fails located in edge cells

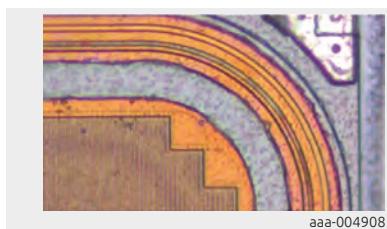


Figure 12 | Device 4; after Al removals

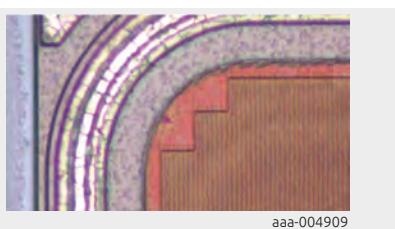


Figure 13 | Device 7; after Al removal

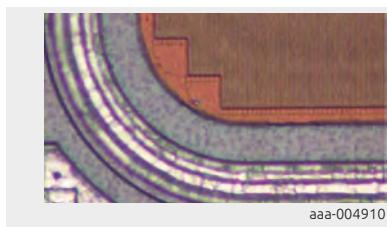


Figure 14 | Device 5; after Al removals

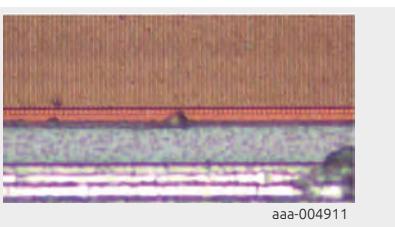
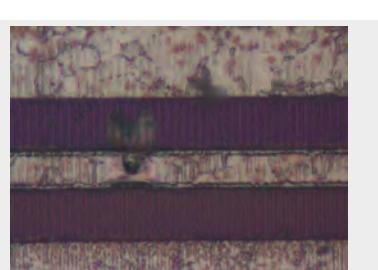
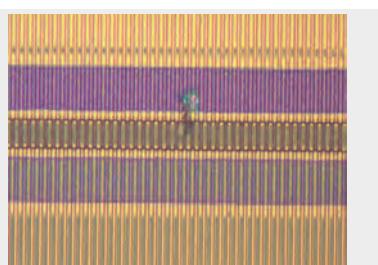
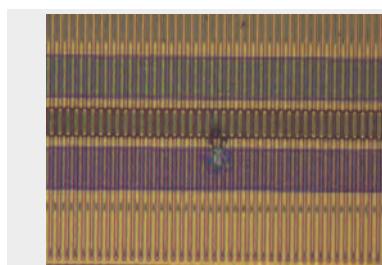


Figure 15 | Device 10; after Al removal

2.4 Human Body Model EOS of PSMN8R5-100PSF

Table 9: Human body model EOS



2.5 Human Body Model EOS of BUK7Y3R0-40H

Table 10: Human body model EOS



Figure 20 | Device 2 after Al, barrier and TEOS etch

Figure 21 | Device 3 after Al, barrier and TEOS etch

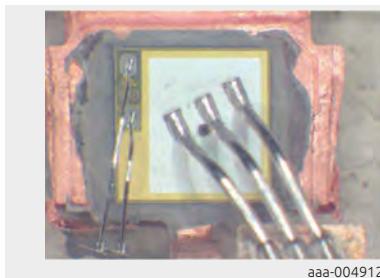
2.6 Unclamped Inductive Switched EOS of BUK7L06-34ARC

Table 11: Unclamped inductive switching EOS

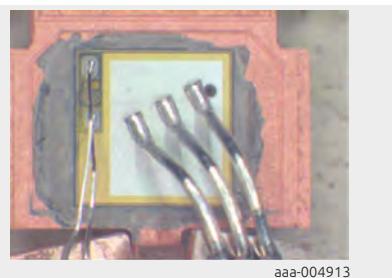
BUK7L06-34ARC

Cell structure: 9 mm hexagons
Package: TO-220 (clip bond)
Die size: 4.3 mm x 4.3 mm
EOS Condition: 0.2 mH; 80 A to 110 A

Small round burn marks, randomly distributed over active area, close to but not directly under wire-bonds



aaa-004912



aaa-004913

Figure 23 | Sample image 1

Figure 24 | Sample image 2



aaa-004914



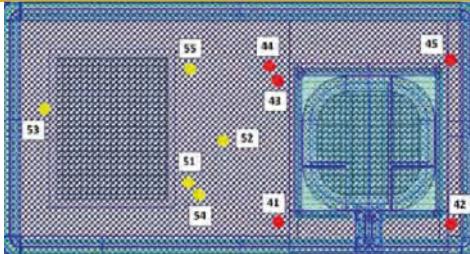
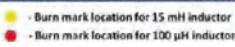
aaa-004915

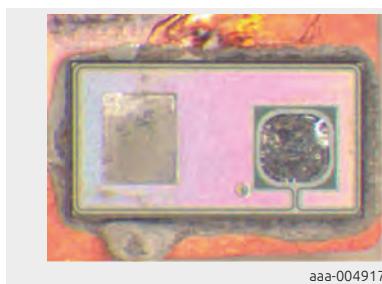
Figure 25 | Sample image 3

Figure 26 | Sample image 4

2.7 Unclamped Inductive Switched EOS of BUK9Y40-55B

Table 12: Unclamped inductive switching EOS

BUK9Y40-55B	
Cell structure:	4 µm stripe
Package:	LFPACK (clip bond)
Die size:	2.5 mm x 1.35 mm
EOS Condition:	Red dots: 0.1 mH, 76 A to 80 A Yellow dots: 15 mH, 7 A to 9 A
	
	
aaa-004916	
Small round burn marks, randomly distributed over active area, close to but not directly under clip bond	



aaa-004917



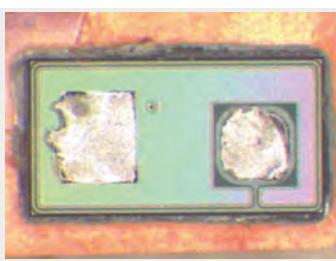
aaa-004918

Figure 27 | Sample image 41; 0.1 mH

Figure 28 | Sample image 43; 0.1 mH



aaa-004919



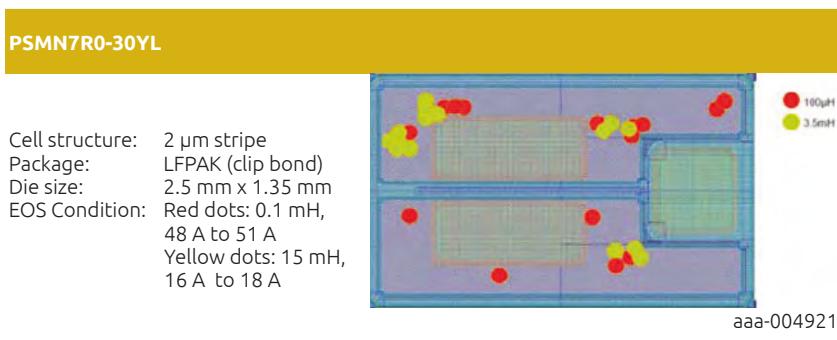
aaa-004920

Figure 29 | Sample image 51; 15 mH

Figure 30 | Sample image 55; 15 mH

2.8 Unclamped Inductive Switched EOS of PSMN7R0-30YL

Table 13: Unclamped inductive switching EOS



Small round burn marks, randomly distributed over active area, close to but not directly under clip bond



Figure 31 | Sample image 6; 0.1 mH

Figure 32 | Sample image 8; 0.1 mH

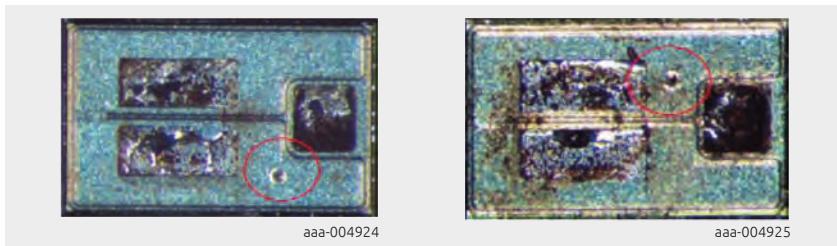


Figure 33 | Sample image 18; 3.5 mH

Figure 34 | Sample image 20; 3.5 mH

2.9 Unclamped Inductive Switched EOS of PSMN8R5-100PSF

Table 14: Unclamped inductive switching EOS

PSMN8R5-100PSF	
Cell structure: 2 µm stripe	
Package: SOT78	
Die size: 4 mm x 2.67 mm	
EOS Condition: Teal dot - 25 mH Orange dot - 100 uH	
	

Figure 35 | Device 1 upper (orange) hotspot

Figure 36 | Device 1 lower (orange) hotspot

Figure 37 | Device 4 upper (orange) hotspot

Figure 38 | Device 4 lower (orange) hotspot

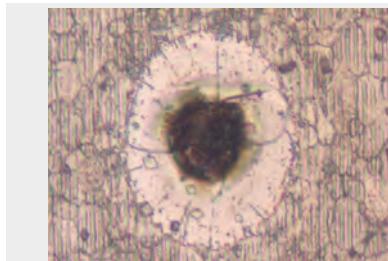


Figure 39 | Device 6 (teal) hotspot

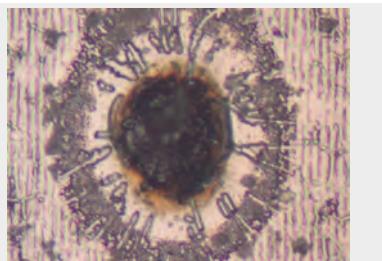


Figure 40 | Device 7 (teal) hotspot

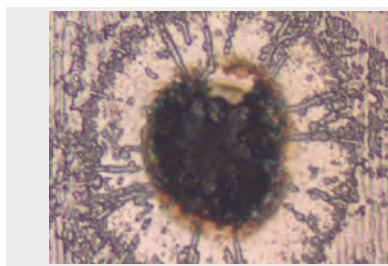


Figure 41 | Device 8 (teal) hotspot

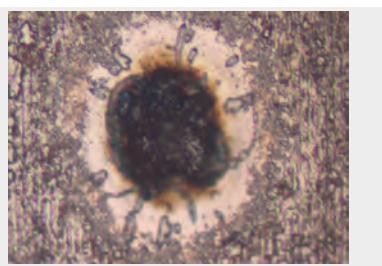


Figure 42 | Device 9 (teal) hotspot

2.10 Unclamped Inductive Switched EOS of BUK7Y3R0-40H

Table 15: Unclamped inductive switching EOS

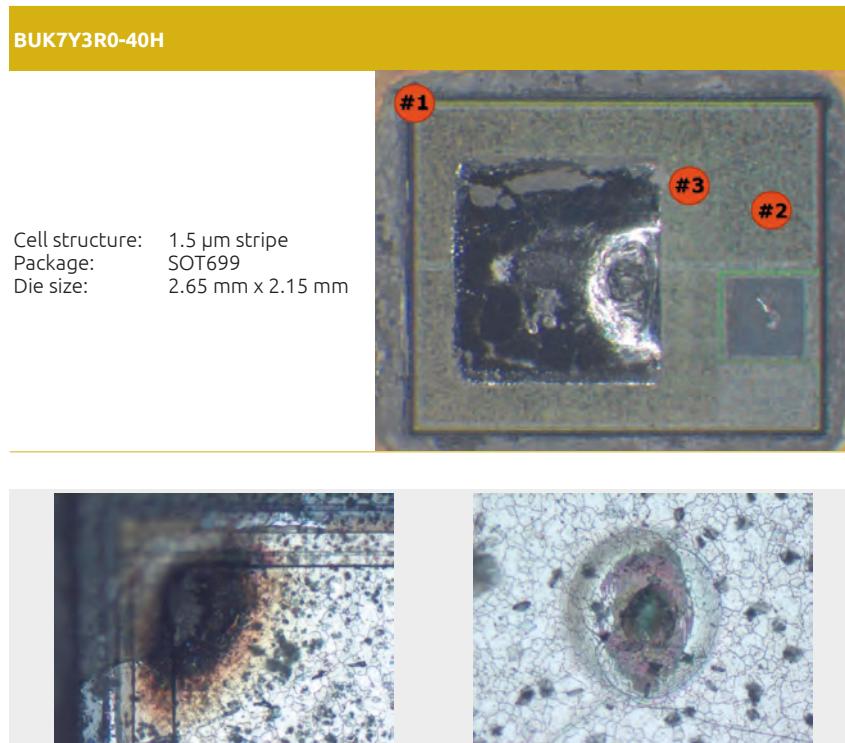


Figure 43 | Device 1

Figure 44 | Device 2

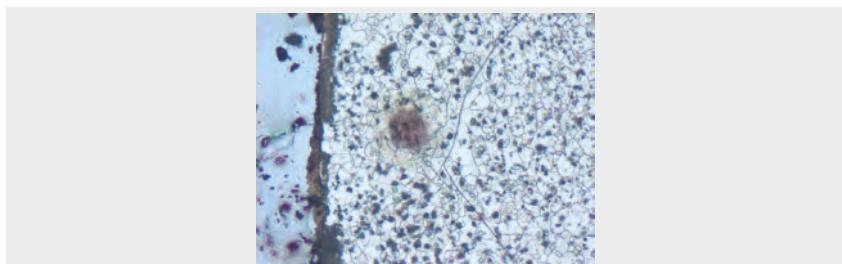


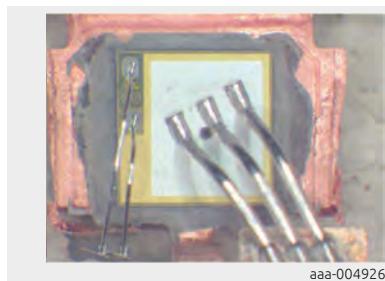
Figure 45 | Device 3

2.11 Linear mode EOS of BUK7L06-34ARC

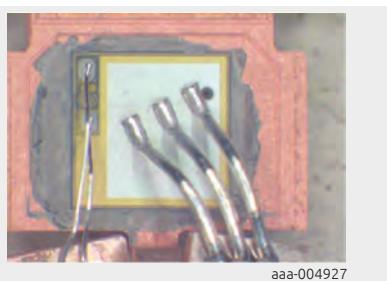
Table 16: Linear mode EOS

BUK7L06-34ARC

Cell structure: 9 mm hexagon
Package: TO-220 (clip bond)
Die size: 4.3 mm x 4.3 mm
EOS condition: 15 V, 3 A Burn marks located in middle of the die adjacent to wire bonds
30 V, 1.5 A Burn mark and location are more discrete at 20 V, 1.5 A



aaa-004926



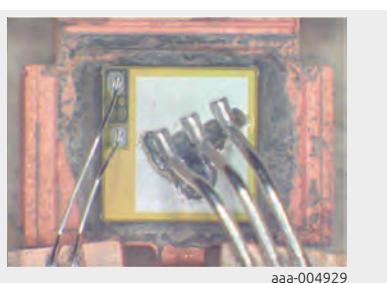
aaa-004927

Figure 46 | Sample image 1: 15 V, 3 A

Figure 47 | Sample image 2: 15 V, 3 A



aaa-004928



aaa-004929

Figure 48 | Sample image 3: 15 V, 3 A

Figure 49 | Sample image 4: 15 V, 3 A



Figure 50 | Sample image 1: 30 V, 1.5 A



Figure 51 | Sample image 2: 30 V, 1.5 A



Figure 52 | Sample image 3: 30 V, 1.5 A

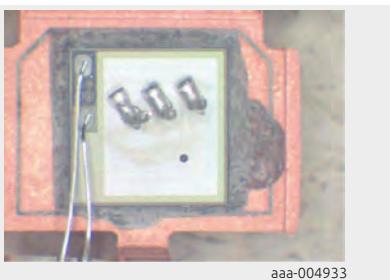
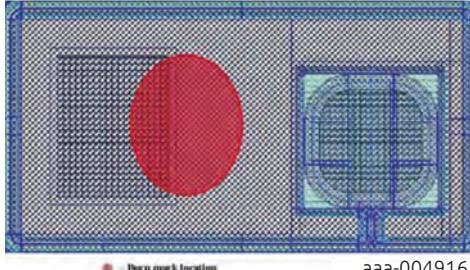


Figure 53 | Sample image 4: 30 V, 1.5 A

2.12 Linear mode EOS of BUK9Y40-55B

Table 17: Linear mode EOS

BUK9Y40-55B	
Cell structure:	4 μm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm x 1.35 mm
EOS condition:	20 V, 3.5 A, 30 ms 20 V, 3 A, 60 ms 30 V, 1.4 A, 60 ms
	
aaa-004916	
Burn marks in center of die, adjacent but not directly under clip bond	

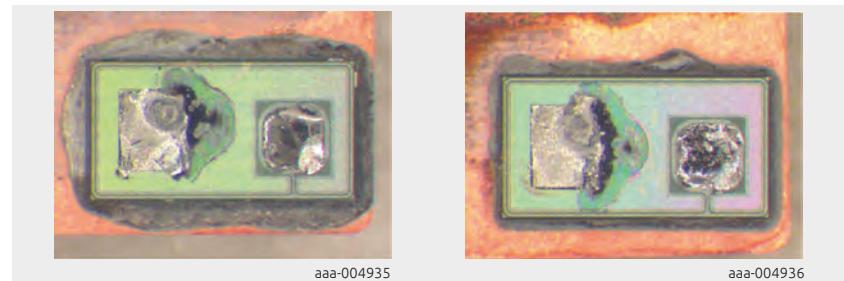


Figure 54 | Sample image 61; 20 V, 3.5 A, 30 ms

Figure 55 | Sample image 62; 20 V, 3.5 A, 30 ms



Figure 56 | Sample image 63; 20 V, 3.5 A, 30 ms

Figure 57 | Sample image 64; 20 V, 3.5 A, 30 ms



Figure 58 | Sample image 66; 20 V, 3 A, 60 ms



Figure 59 | Sample image 67; 20 V, 3 A, 60 ms

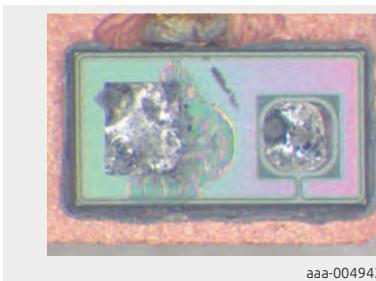


Figure 60 | Sample image 68; 20 V, 3 A, 60 ms



Figure 61 | Sample image 69; 20 V, 3 A, 60 ms

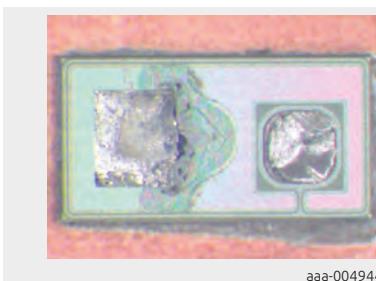


Figure 62 | Sample image 71; 30 V, 1.4 A, 60 ms



Figure 63 | Sample image 72; 30 V, 1.4 A, 60 ms



aaa-004945



aaa-004947

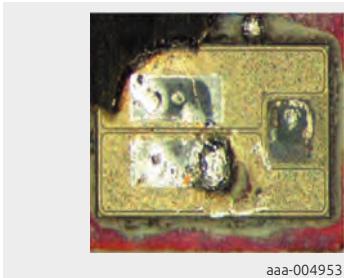
Figure 64 | Sample image 73; 30 V, 1.4 A, 60 ms**Figure 65 | Sample image 74; 30 V, 1.4 A, 60 ms**

2.13 Linear mode EOS of PSMN7R0-30YL

Table 18: Linear mode EOS

PSMN7R0-30YL	
Cell structure:	2 μm stripe
Package:	LFPAK (clip bond)
Die size:	2.3 mm x 1.35 mm
EOS condition:	0.1 mH, 48 A to 51 A 3.5 mH, 16 A to 18 A
Burn marks in center of die, adjacent but not directly under clip bond	

**Figure 66 | Sample image 1; 15 V, 2.5 A, 100 ms****Figure 67 | Sample image 2; 15 V, 2.5 A, 100 ms**



aaa-004953



aaa-004954

Figure 68 | Sample image 4; 15 V, 2.5 A, 100 ms**Figure 69** | Sample image 5; 15 V, 2.5 A, 100 ms

aaa-004955



aaa-004956

Figure 70 | Sample image 11; 15 V, 5 A, 1 ms**Figure 71** | Sample image 12; 15 V, 5 A, 1 ms

aaa-004957

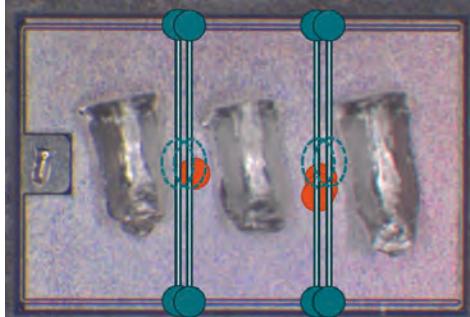
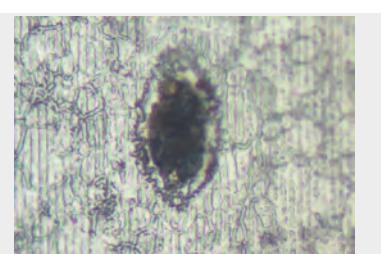
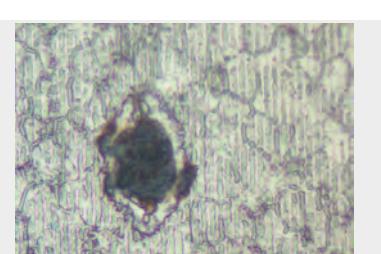


aaa-004958

Figure 72 | Sample image 13; 15 V, 5 A, 1 ms**Figure 73** | Sample image 14; 15 V, 5 A, 1 ms

2.14 Linear mode EOS of PSMN8R5-100PSF

Table 19: Linear mode EOS

PSMN8R5-100PSF	
Cell structure:	2.5 μm stripe
Package:	SOT78
Die size:	4 mm x 2.67 mm
EOS condition:	Teal dot - 50 V 10 ms pulse length Orange dot - 70 V 1 ms pulse length
	
	
	
Figure 74 Device 5 upper (orange) hotspot	
	
	
Figure 75 Device 6 lower (orange) hotspot	
Figure 76 Device 7 upper (orange) hotspot	
Figure 77 Device 8 lower (orange) hotspot	

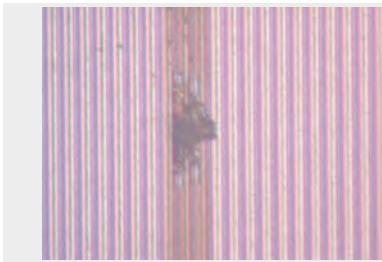


Figure 78 | Device 1 (teal) hotspot

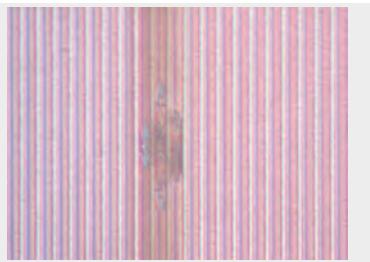


Figure 79 | Device 2 (teal) hotspot

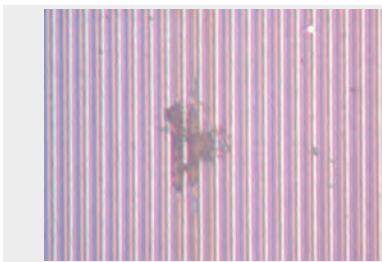


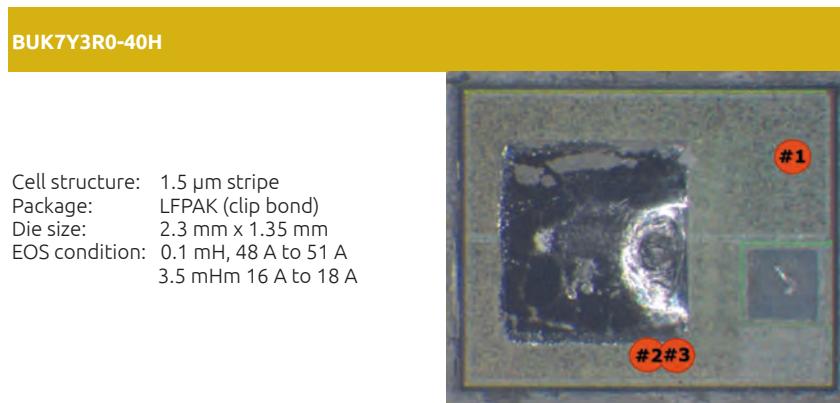
Figure 80 | Device 3 (teal) hotspot



Figure 81 | Device 4 (teal) hotspot

2.15 Linear mode EOS of BUK7Y3R0-40H

Table 20: Linear mode EOS



Burn marks in center of die, adjacent but not directly under clip bond

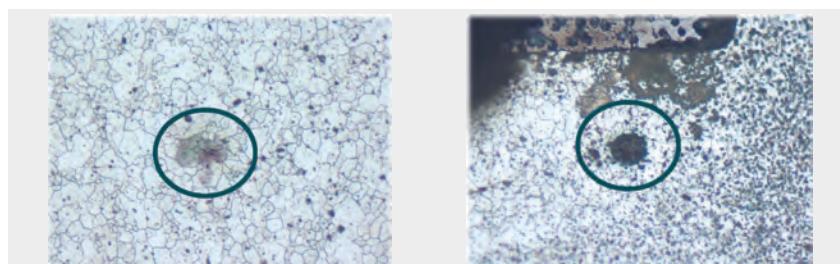


Figure 82 | Sample image 1; 15 V, 2.5 A, 100 ms

Figure 83 | Sample image 2; 15 V, 2.5 A,
100 ms

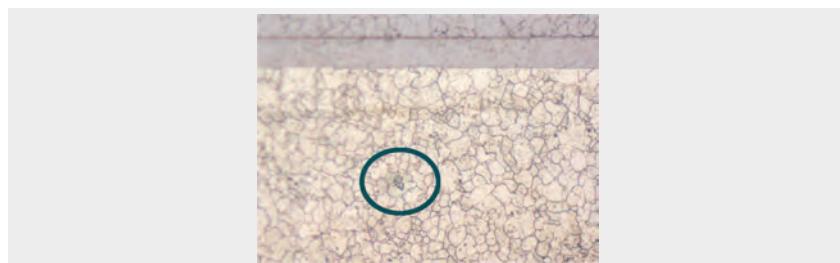


Figure 84 | Sample image 4; 15 V, 2.5 A, 100 ms

2.16 Over-current EOS of BUK7L06-34ARC

Table 21: Over-current EOS

BUK7L06-34ARC

Cell structure: 9 mm hexagon
Package: TO-220 (clip bond)
Die size: 4.3 mm x 4.3 mm
EOS condition: 120 A

Extensive damage starting from die where wire bonds meet die.
Secondary damage of reflowed solder and even fused wires are visible.



aaa-004959



aaa-004960

Figure 85 | Sample image 1

Figure 86 | Sample image 2



aaa-004961



aaa-004962

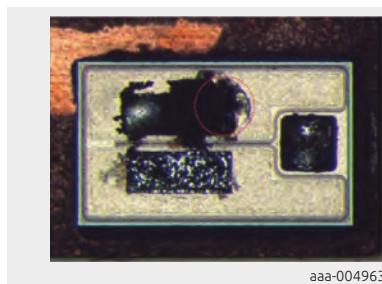
Figure 87 | Sample image 3

Figure 88 | Sample image 4

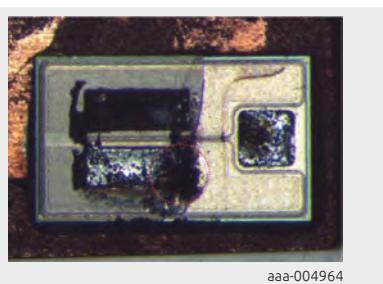
2.17 Over-current EOS of PSMN7R0-30YL

Table 22: Over-current EOS

PSMN7R0-30YL	
Cell structure:	2 μm stripe
Package:	LFPAK (clip bond)
Die size:	2.3 mm x 1.35 mm
EOS condition:	35 A, 35 ms
	Burn marks in center of die, adjacent but not directly under clip bond Some evidence of die-cracking.



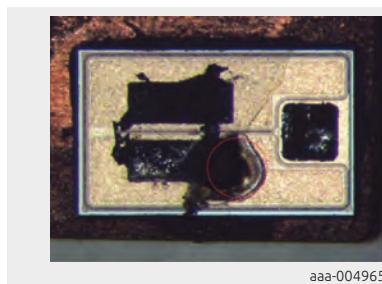
aaa-004963



aaa-004964

Figure 89 | Sample image 6

Figure 90 | Sample image 7



aaa-004965



aaa-004966

Figure 91 | Sample image 8

Figure 92 | Sample image 9

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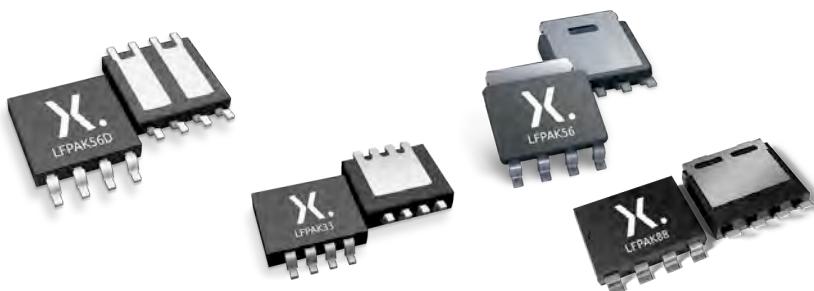
Chapter 9

LFPACK MOSFET thermal design guide

Application Note: AN90003

1 Introduction

This chapter is a guide to assist design engineers in understanding the power dissipation limits of the LFPAK family of packages. The maximum power that a MOSFET can dissipate is considered as a function of the Printed Circuit Board (PCB) design, using some common configurations. The application notes comprises of three main sections. The first section gives some background on MOSFET power loss and the thermal environment. The next two sections address separately the low power LFPAKs (LFPAK56D and LFPAK33) and the high power LFPAKs (LFPAK56 and LFPAK88).



2 MOSFET power dissipation and the design environment

During normal operation, MOSFETs can exhibit three kinds of power losses:

- Switching losses – due to voltage and current being non-zero during the transition between the ON and OFF states.
- Conduction losses – when the device is fully on due to its on-state resistance $R_{DS(on)}$.
- Avalanche losses – if the device breakdown voltage is exceeded and an avalanche event occurs.

The shape of the power can change depending on the nature of the load. A generalized model of the total power dissipated by a MOSFET is the sum of these three losses, see Equation (1).

$$P_{tot} = P_{sw} + P_{cond} + P_{av} \quad [1]$$

In addition to electrical requirements another challenge is often the harsh environment that a device needs to operate in, particularly in terms of

temperature. For instance, in automotive and industrial applications it's not uncommon to encounter high ambient temperature requirements, (from 85 °C up to 125 °C), this limits the amount of power that a MOSFET can safely handle.

Semiconductor devices are not the only parts to consider when dealing with high temperatures. For instance, the PCB material FR4 has a maximum operating temperature of around 130 °C, depending on manufacturer and chemistry, this is much lower than the limit specified for the junction of a silicon die (175 °C).

Modern applications continue to push the limits of power MOSFETs, while searching for better and better performances. As a consequence thermals have become one of the most important aspects of systems design. One way to address thermal issues is to carefully choose a device with the appropriate performances and provide a good enough path through which heat can flow freely, avoiding any impact on the device reliability.

2.1 Heat propagation phenomena

Heat propagates because of a temperature difference between the junction and the outside/ambient. Propagation occurs from junction and the outside/ambient through different material, from solids (silicon, copper, FR4, aluminum) to fluids (surrounding air or even air pockets trapped in the solder joints on the PCB). Heat finds a path whether it's defined by an engineer or not. This means that if the path is not designed correctly then heat might get trapped and raise the temperature of one or multiple mediums.

The physical phenomena by which heat can propagate are: conduction, convection and radiation.

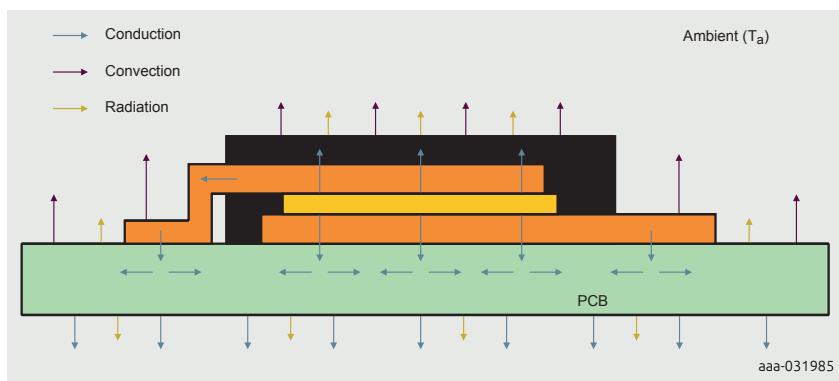


Figure 1 | Thermal propagation phenomena

2.1.1 Conduction

Conduction is the propagation of heat in a solid medium due to a temperature difference within it, and it is caused by the random movement of atoms and molecules. The rate of heat flow Q is directly proportional to the cross-section area A , temperature difference and thermal conductivity k . It is inversely proportional to the length x of the heat path, see Equation (2).

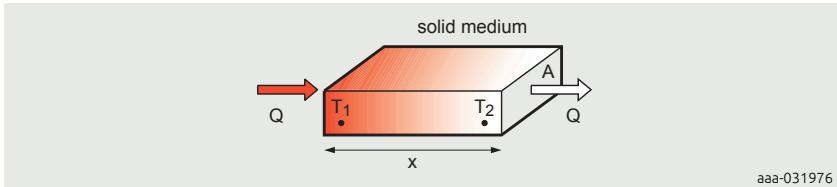


Figure 2 | Conduction in a solid medium

$$Q = k \cdot A \cdot \frac{T_1 - T_2}{x} \quad [2]$$

Thermal conductivity, measured as $\text{W}/(\text{mK})$, is a physical property of a material and defines its ability to conduct heat. The higher its value the higher the rate of heat transfer, therefore the better thermal conductor. From Equation 2 it can be derived that rate of heat flow is measured in W . Therefore, heat is measured in Joule (Ws).

Table 1 lists some materials with their thermal conductivity values. Air is a very bad conductor of heat, thus a good thermal insulator. Its thermal conductivity is 2,000 times lower than that of steel. Notice how thermal glue has a very low thermal conductivity of less than 2, (generic brand). Thermal glue is not a good thermal conductor, however its main function is to create a good fit between two surfaces that otherwise would form trapped pockets of air, which is 100 times a better insulator than the glue itself.

Table 1: Typical thermal conductivity values

Material	k (W/mK)
Air (not moving)	0.024
Brick	0.6
Glass	0.8
Thermal glue	1.78
Steel	50.2
Brass	109
Silicon	130

Material	k (W/mK)
Aluminium	205
Copper	385
Silver	406
Diamond	1000

2.1.2 Convection

Convection is the transfer of heat from a solid body to a fluid due to its movement with respect to the surface of the body, and it is promoted by a difference in temperature between the two mediums. The fluid may be a gas (air) or a liquid.

Here the rate of heat flow depends only on surface A, temperature difference and convection coefficient h, see Equation (3).

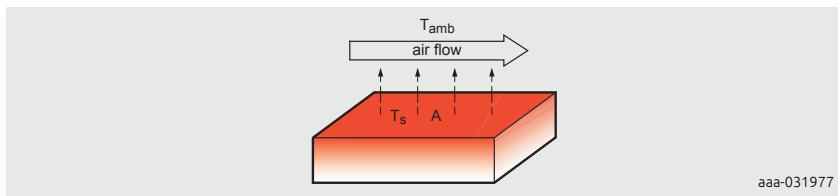


Figure 3 | Convection in free air

$$Q = h \cdot A \cdot (T_s - T_{amb}) \quad [3]$$

The convection coefficient is not a physical property of the fluid (like the conduction coefficient) but an abstract quantity verified by experimentation. It depends on fluid density, velocity, viscosity, turbulence and on the solid medium surface geometry.

The convection coefficient is measured in W/(m²K). Table 2 lists some values measured in different scenarios of free/natural and forced cooling.

Table 2: Thermal convection coefficient values

Flow type	h (W/m ² K)	Forced cooling
		Free air
Gases	2 - 20	25 - 300
Air	10	100
Liquids	50 - 1,000	100 - 40,000
Phase change	2,500 - 100,000	

As can be seen during a phase change the convection coefficient rises dramatically up to 100,000. This is due to the fact that during a phase change all the energy

involved, and transferred to the fluid, is used to rearrange molecules structure and does not result in a temperature change.

2.1.3 Radiation

Radiation is the propagation of heat via infrared radiation.

The main benefit of radiation is that as the ambient temperature increases, and the component temperature with it, the heat transfer by radiation increases as well. As you can see in Equation (4), it depends on the fourth power of temperature. The radiation is bigger but not by a lot and the overall effect is that radiation does not help a body get cooler.

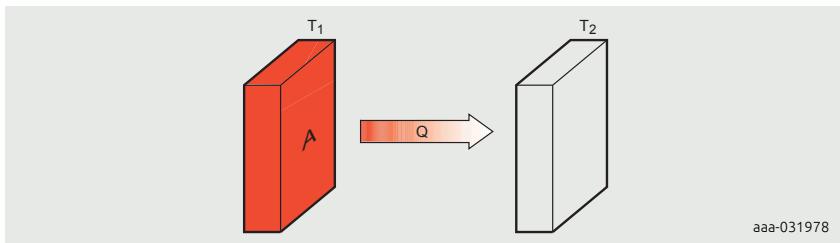


Figure 4 | Radiation

$$Q = \epsilon \cdot \sigma \cdot A \cdot (T_1^4 - T_2^4) \quad [4]$$

The amount of radiation is determined by the surface emissivity. Emissivity of a material is measured between 0 and 1. A perfect emitter is called a black body because it emits 100% of the energy it absorbs, and is assigned an emissivity value of 1. Table 3 below gives emissivity values for different materials.

Table 3. Typical emissivity values

Material	Emissivity coefficient (ϵ)
Aluminum, polished	0.05
Aluminum, oxidized	0.25
Black electrical tape	0.95
Copper, polished	0.01
Copper, oxidized	0.65
Steel, oxidized	0.88
Water	0.98

A new piece of polished aluminum has emissivity of 0.05, (not good), its emissivity increases as it oxides by 5 times. Every object emits thermal radiation, the amount

of radiation that a particular object emits as a function of wavelength looks as a bell shaped curve. Energy is emitted at all frequencies but the major part of the emission occurs at a certain wavelength range which depends on the source temperature. The higher the temperature the higher the frequency (lower the wavelength), that is why we see materials change color as they heat up.

At the receiving side, for most of the surfaces, the same graph looks quite flat but to a very small range of wavelengths at which the object absorbs all the impinging radiation. These surfaces are called selective surfaces, because they absorb only certain wavelengths.

2.2 Thermal – Electrical analogy

When considering thermal propagation, classical methods of analysis may be used. These are based on the thermal equations and thermal networks. These describe the paths through which heat propagates through mediums or from one medium to another.

Any thermal network can be modelled by means of an electrical circuit. An analogy for every thermal parameter can be found in the electrical domain. The respective analogues of electric potential and current are temperature difference and rate of heat flow. Based on these it may be observed that the thermal resistance is the ratio of temperature and rate of heat flow similarly to how the voltage and current ratio defines the electrical resistance using Ohm's law. The main analogies may be seen in Table 4 below. Based on these, thermal networks can be solved using many of the electrical theory laws such as Ohm's and Kirchhoff's laws. Also circuits can be simplified by means of series and parallel resistor equivalences.

Table 4. Thermal and electrical analogous parameters

Thermal	Electrical
Temperature T (°C)	Voltage V (V)
Rate of heat flow Q (W)	Current I (A)
Thermal resistance R_{th} (K/W)	Resistance R (Ω)
Thermal capacitance C_{th} [W·s/K]	Capacitance C (A·s/V = F)

An example of a thermal circuit modelled in the electrical domain using a SPICE software may be seen in Figure 5. Figure 6 shows the response of this example circuit as a temperature plot, where the transient and steady state thermal behaviour may be seen.

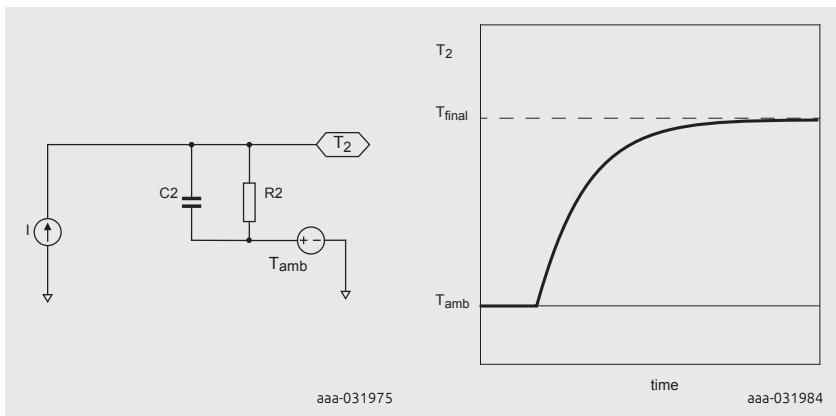


Figure 5 | SPICE model

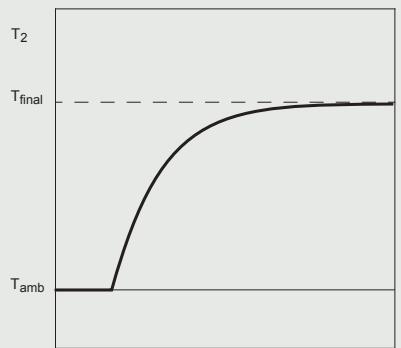


Figure 6 | Response

2.2.1 Thermal resistance

Thermal resistance is a measure of the inertia of a material or medium towards heat flow, just like the electrical resistance is to the movement of electrons. It is therefore a physical property of the specific component. It is calculated as the ratio of the temperature difference between two points and the rate of heat flow, therefore as K/W. The thermal and electrical models may be seen in the pictures below.

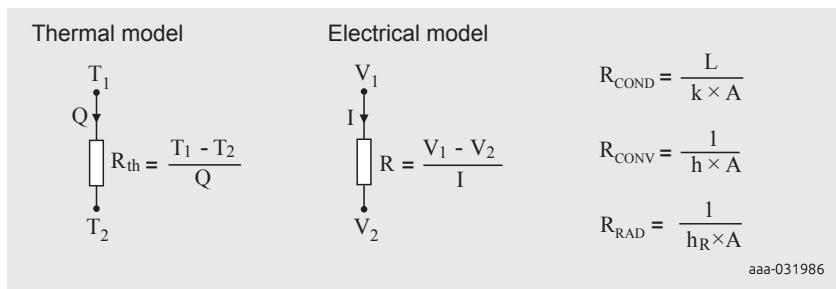


Figure 7 | Thermal and electrical resistance models

Every phenomenon governing how heat flows, namely conduction, convection and radiation, has its own thermal resistance. Each one of them depends inversely on a coefficient and surface or cross section area of the material from where heat is generated or simply passing through. In conduction the resistance depends directly to the length of the medium.

2.2.2 Thermal capacitance

Thermal capacitance, sometimes known also as thermal mass, is a property of a material which represents how much heat (thermal energy) it can store in time, similar to its electrical counterpart with electrical energy. Thermal capacitance provides also a quantity of the inertia against temperature fluctuations, the higher the value the harder it will be to drive the stored energy in or out.

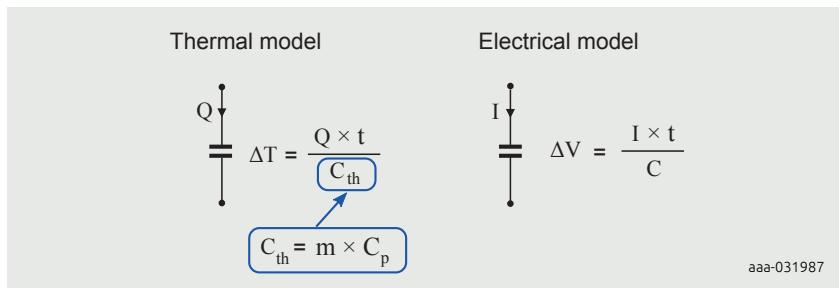


Figure 8 | Thermal and electrical capacitance models

Thermal capacitance is typically referred to using the symbol C_{th} , and it's measured as J/K . For a body of uniform composition, it can be approximated as the product of mass (m) of the body and specific heat capacity (C_p), which is the heat capacity of a sample of the substance divided by the mass of the sample.

2.2.3 Transient and steady state thermal behavior

- Thermal transients describe temperatures which are changing, even at the end of the analysis window. An example may be observed below in the yellow part of the junction temperature plot.
- Steady state thermals describe the stable region where temperatures show minimal to no change at all. These temperatures remain unchanged with the passing of time and thus represent the final values a system might show under constant conditions.

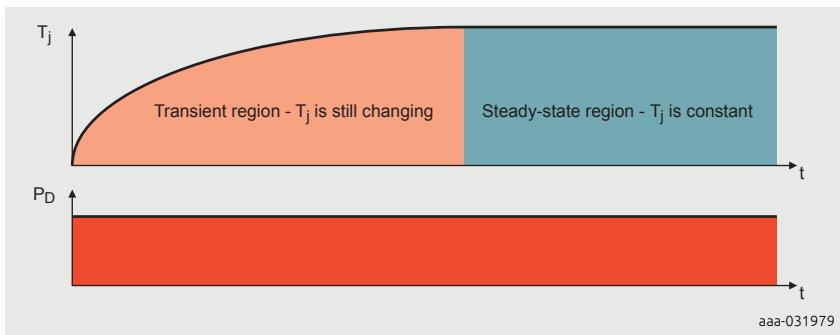


Figure 9 | Transient and steady state thermal behavior

2.3 MOSFET steady state thermal characteristics

This section focuses on two important MOSFET thermal aspects. The junction to mounting base thermal resistance as well as the junction to ambient thermal resistance. The aim in this chapter is to overview the two thermal paths and to show the thermal network which describes these paths.

2.3.1 Thermal resistance junction to mounting base - $R_{th(j\text{-}mb)}$

The thermal heat path between the MOSFET junction to its mounting base is one of the most important thermal specifications on a data sheet. It is represented by the overall junction to mounting base thermal resistance which is a value describing the ease with which heat is conducted along this path due to the different materials it is going through. In Figure 10, a MOSFET depiction is represented with the thermal resistive network between the junction to mounting base.

As the MOSFET and its parts are 3 dimensional so is the mentioned heat path, thus the 2 dimensional resistor network seen below is actually 3 dimensional in reality. Referring back to the $R_{th(j\text{-}mb)}$, it is important to remember that the value encompasses the whole network. Lastly, the parameter describes the steady state thermal characteristics, thus one should use average power dissipation values in order to obtain the temperatures reached by the MOSFET.

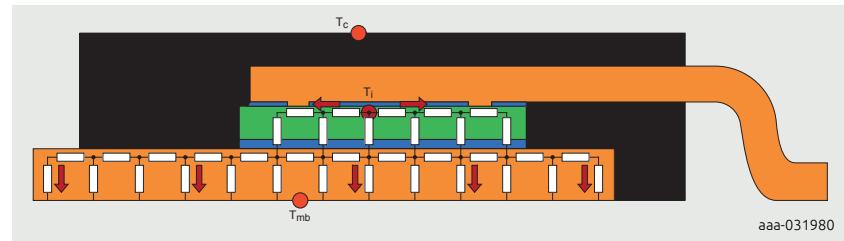


Figure 10 | Thermal path junction to mounting base

2.3.2 Thermal resistance junction to ambient - $R_{th(j-a)}$

The thermal heat path between the MOSFET junction and the ambient encompasses paths within the MOSFET itself as well as additional ones when a MOSFET is mounted onto a PCB. Hence, heat may spread from the junction towards the mounting base and the case. Afterwards, when the extremities of the MOSFET are reached, the heat will flow into the surroundings via the PCB or directly from the case. These heat paths are depicted in Figure 11.

Figure 11 a) shows the heat moving from the junction to the mounting base and to the case top and afterwards to the ambient. Figure 11 b) shows the heat moving from the mounting base to the PCB and through it in order to reach the ambient.

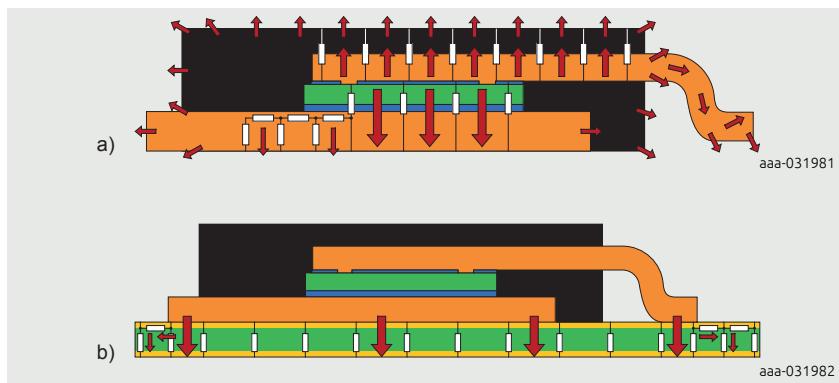


Figure 11 | Thermal path junction to ambient

A simplified thermal circuit may be seen in Fig. 12. It is important to notice that the two thermal paths from the component to the ambient are in parallel, thus improving both may be redundant.

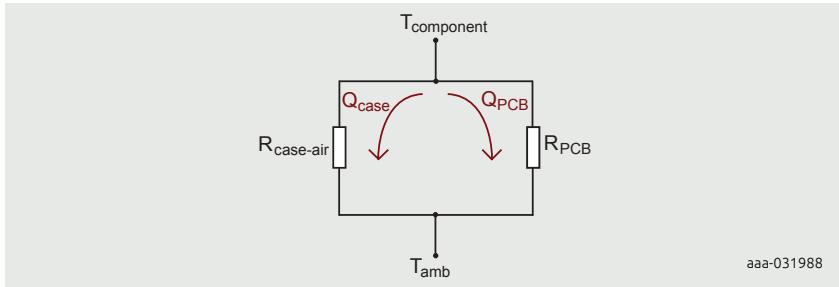


Figure 12 | Simplified $R_{\text{th(j-a)}}$ thermal paths

A more cost effective method of reducing the thermal resistance between the MOSFET to the surroundings may be to focus on one of the thermal paths and improve it in the best way possible.

Figure 13 shows a thermal circuit which encompasses the MOSFET the PCB and the environment, it may be observed that the three heat spreading methods are shown by individual thermal resistors. In this particular case, the heat spreads:

- Through conduction from the junction towards the outside of the MOSFET, represented by the mounting base and the case.
- From the case to the ambient the heat propagates through convection and radiation.
- From the mounting base to the PCB and into it, conduction is again the main way of propagation.
- From the PCB into the environment convection and conduction are the main methods through which heat propagates to the ambient, radiation is usually negligible.

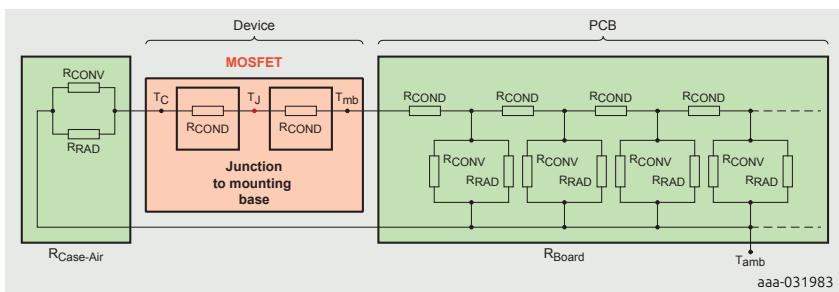


Figure 13 | Thermal circuit, MOSFET, PCB and environment

The thermal circuit seen in Figure 13 is also represented in Figure 1. Finally, the two thermal resistor networks highlighted in green are also represented in Figure 12.

2.3.3 PCB thermal limitation and the 1 Watt rule

As previously described, the junction to ambient thermal path contains the board or PCB. This is often made from FR4 material, which from a thermal and electrical perspective is an insulator. Moreover, planes, pours and traces of copper are also present as these provide the circuit interconnections. Altogether we can consider them as forming the board and giving it a certain thermal characteristic called the board thermal resistance. It was found that this value is approximately **50-60 K/W**, depending on the amount of copper, insulation layer thickness and other factors. Since this is specific to the materials and dimensions of a board, this limit is imposed.

Moreover, the ambient temperature in which a board operates, the thermal limitations of a system, the FR4 temperature limit of 120 °C to 140 °C, as well as the temperature ranges within which a board needs to function in, gives rise to a power limitation. These same dependencies can be noted from the following equations:

$$\text{Thermal resistivity} \left[\frac{W}{mK} \right] = \frac{1}{\text{Thermal conductivity} \left[\frac{mK}{W} \right]} \quad [5]$$

$$\text{Thermal resistance} \left[\frac{K}{W} \right] = \text{Thermal resistivity} \left[\frac{W}{mK} \right] \times \frac{\text{Thickness} [m]}{\text{Area} [m^2]} \quad [6]$$

$$\text{Thermal resistance} \left[\frac{K}{W} \right] = \frac{\text{Temperature difference} [K]}{\text{Power} [m]} \quad [7]$$

PCB thickness, area and thermal resistivity determine the PCB thermal resistance, given in K/W. Hence, given a specific ambient temperature and a maximum FR4 temperature, or the system maximum operation temperature, a ΔT is obtained.

Example: calculate the power dissipation of a MOSFET mounted on an FR4 PCB within an automotive environment where the ambient temperature is 80 °C.

- The FR4 PCB material has a thermal resistance $R_{th(FR4\ PCB)} = 50\text{ K/W}$
- The FR4 PCB material maximum temperature ($T_{FR4(max)}$) = 130 °C
- The ambient temperature $T_{amb} = 80\text{ }^{\circ}\text{C}$

$$\Delta T = T_{FR4(max)} - T_{(amb)} = 130\text{ }^{\circ}\text{C} - 80\text{ }^{\circ}\text{C} = 50\text{ }^{\circ}\text{C} \quad [8]$$

$$P = \frac{R_{th(FR4\ PCB)}}{\Delta T} = \frac{50\text{ K}}{50\text{ K/W}} = 1\text{ W} \quad [9]$$

Given the above ambient temperature and FR4 PCB characteristics, approximately 1 watt of power may be dissipated in a MOSFET within this automotive environment.

2.3.4 Thermal nomenclature

Terminology surrounding thermal characterization of power MOSFETs has been revised multiple times over the years. Regardless of these efforts, standards organizations and semiconductor manufacturers may still use different names when referring to the same thermal parameter, or to slightly different variations of it. The terms often used to indicate one or the other type of thermal resistance are: R and θ . In the case of junction to ambient, the $R_{th(j\text{-amb})} = R_{\theta(j\text{-amb})} = \theta_{(j\text{-amb})}$.

3 LFPAK56D and LFPAK33

3.1 Simple configuration with a single layer

In this section, we will present the maximum power dissipation results for a simple PCB configuration using a single layer with varying copper area.

Results for the LFPAK56D and LFPAK33 packages are given, for the LFPAK56D with only one or with both MOSFETs conducting.

3.1.1 LFPAK56D

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.1 W, 0.5 W and 1 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer, see Figure 14.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of the top copper area.

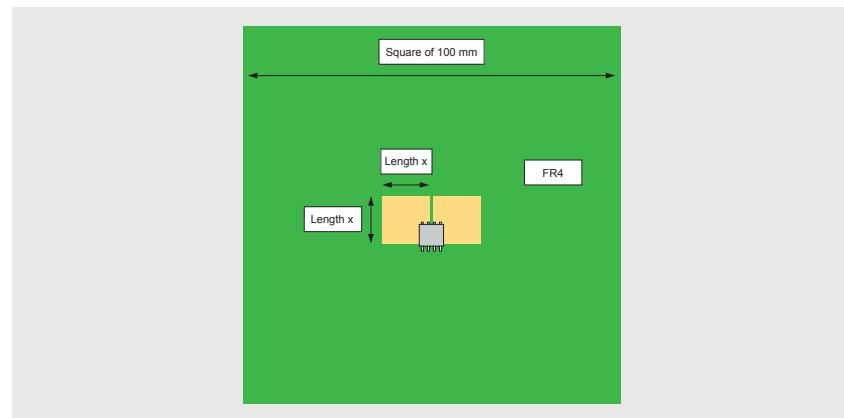


Figure 14 | Copper area configuration: LFPAK56D, single top copper layer

The graph in Figure 15 captures two important factors:

- T_j depends greatly on length "x" and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a "law of diminishing returns". In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j . As can be seen from Figure 15 below, T_j will plateau at around 50 °C (for 0.5 W per MOSFET) no matter how much copper area we provide.

Care must be taken for T_j above 120 °C as PCB temperature directly under the transistor would be close to the MOSFET T_j .

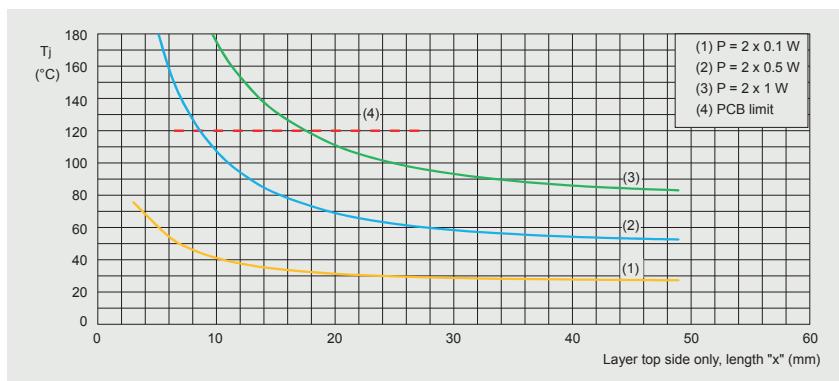


Figure 15 | Junction temperature as a function of copper side length x for LFPAK56D

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(\max)} = 175^\circ\text{C}$ (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In Figure 16 the maximum power for the conditions given is as follows:

$T_{\text{amb}} = 20^\circ\text{C}$: Max power is 2.6 W per MOSFET (2×2.6 W permissible in this package)

$T_{\text{amb}} = 80^\circ\text{C}$: Max power is 1.65 W per MOSFET (2×1.65 W permissible in this package)

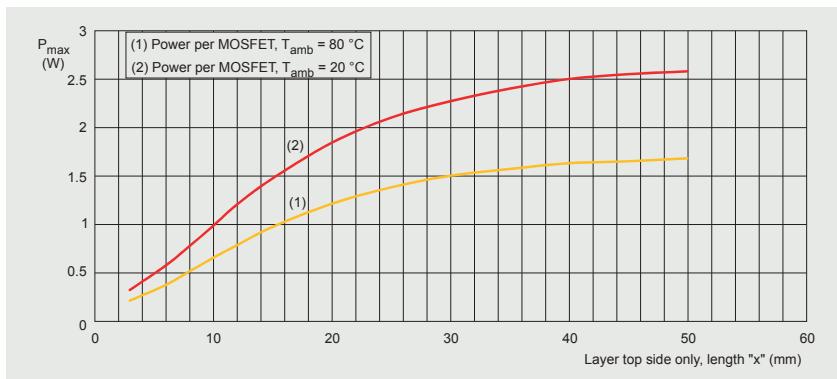


Figure 16 | Maximum permissible power dissipation as a function of copper side length x for LFPAK56D

3.1.2 LFPAK56D only one MOSFET active at a time

In a typical half bridge application only one MOSFET conducts at a time. In the graph below, Figure. 17, 1 W is dissipated in the left MOSFET (blue curve). We can see that 1 W dissipation in one MOSFET is not equivalent to 0.5 W dissipation in each of the two MOSFETs (yellow curve).

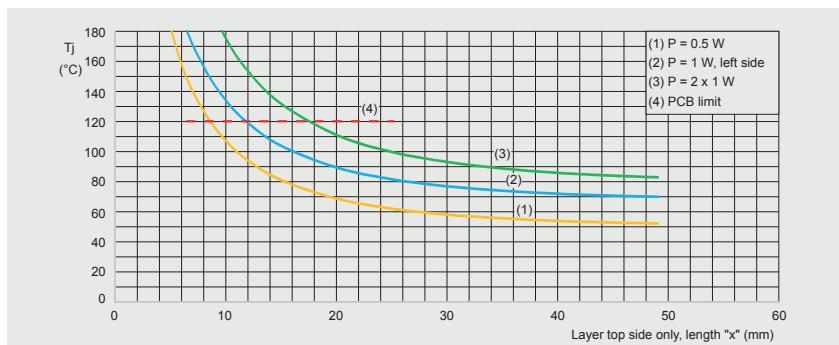


Figure 17 | Junction temperature as a function of copper side length x for LFPAK56D; one MOSFET conducting

As can be seen temperature is higher in the case of one MOSFET dissipating 1 W than it is with two MOSFETs each dissipating 0.5 W. When only one MOSFET is active the second MOSFET does not make a significant contribution to the total dissipation capability - meaning that if one MOSFET is off the heating is not shared equally between the two. This is further explained by the thermal network shown in Figure 19.

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(\max)} = 175 \text{ }^{\circ}\text{C}$ (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB. In Figure 18 the maximum power for the conditions given is as follows:

- $T_{\text{amb}} = 20 \text{ }^{\circ}\text{C}$: Max power is 3.35 W with only left MOSFET
- $T_{\text{amb}} = 80 \text{ }^{\circ}\text{C}$: Max power is 2.1 W with only left MOSFET

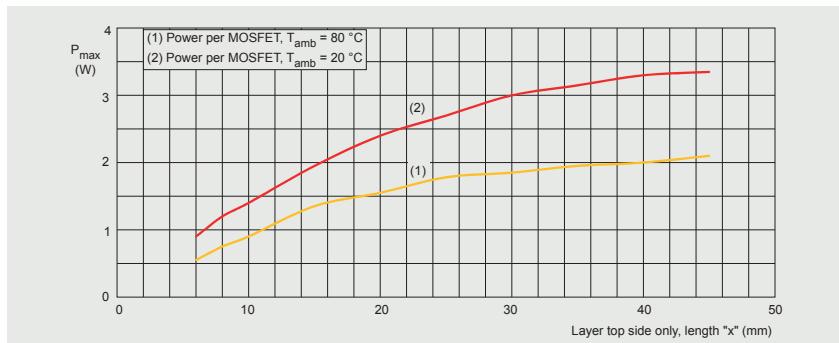


Figure 18 | Maximum power as a function of side length x for LFPAK56D; one MOSFET conducting

The concept of the second MOSFET half-sharing the thermal dissipation when turned off is not true
– see Figure 19

Dual MOSFET thermal resistance configuration:

We can see that the thermal path between both MOSFETs inside the package is highly resistive (100 K/W).

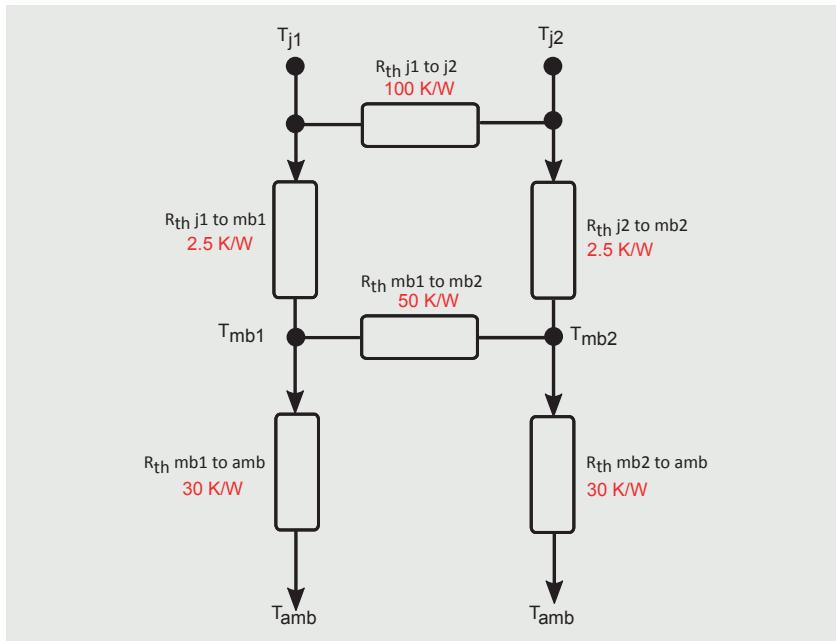


Figure 19 | Thermal resistance configuration

3.1.3 LFPAK33

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.1 W, 0.5 W and 1 W applied in the MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer

- There is no forced air cooling applied i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

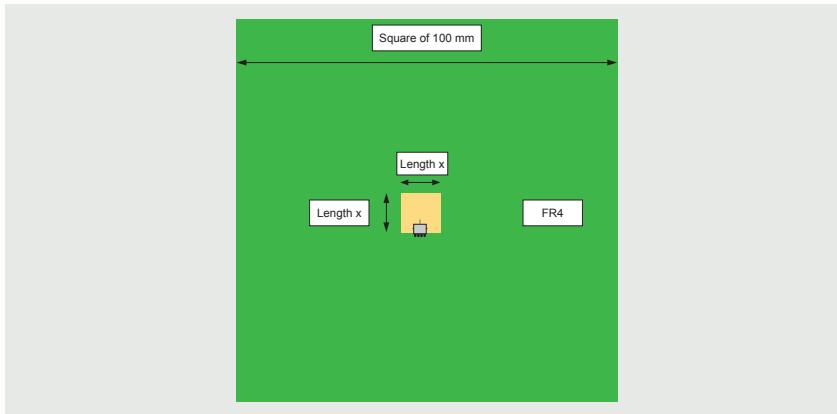


Figure 20 | Copper area configuration: LFPACK33, single top copper layer

The graph in Figure 21 captures two important factors:

- T_j depends greatly on length "x" and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a "law of diminishing returns". In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j . As can be seen from Figure 21 below, T_j will plateau at around 40 °C (for 0.5 W per MOSFET) no matter how much copper area we provide.

Care must be taken for T_j above 120 °C as PCB temperature directly under the transistor would be close to the MOSFET T_j .

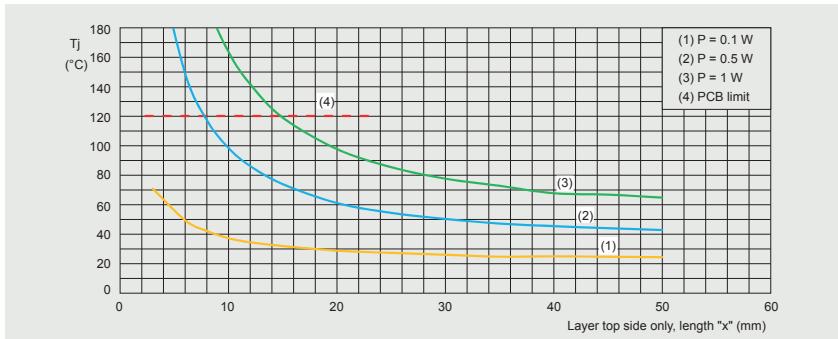


Figure 21 | Junction temperature as a function of copper side length x for LFPAK33

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(\max)} = 175 \text{ }^{\circ}\text{C}$ (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In the graph below, Figure 22, the maximum power for the conditions given is as follows:

$T_{\text{amb}} = 20 \text{ }^{\circ}\text{C}$: Max power is 3.7 W in the MOSFET

$T_{\text{amb}} = 80 \text{ }^{\circ}\text{C}$: Max power is 2.4 W in the MOSFET

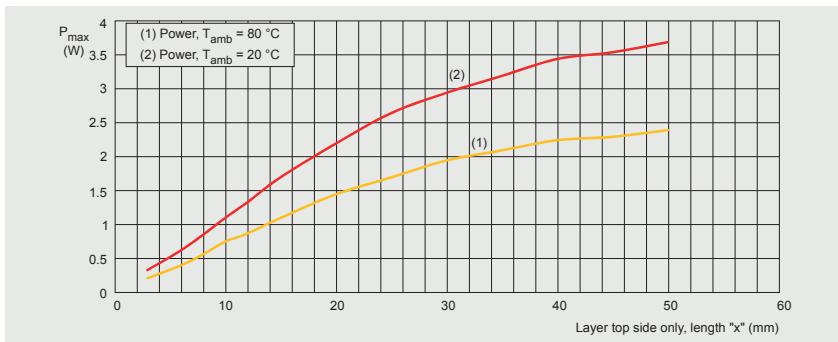


Figure 22 | Maximum permissible power dissipation as a function of copper side length x for LFPAK33

3.2 Usual configuration: 4 layers + vias

In this section, we will present the maximum power dissipation results for a PCB configuration using 4 layers + vias for dissipation on the bottom layer, with varying copper area.

Results for the LFPAK56D and LFPAK33 packages are given, for the LFPAK56D with only one or with both MOSFETs conducting.

3.2.1 LFPAK56D

Set-up:

- 4 layers + vias (vias number increases with the copper area with a maximum of 25 vias for each side)
- MOSFET power dissipation is 0.1 W, 0.5 W and 1 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness on all layers (external and internal) is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied i.e. only natural convection is modeled

The common PCB stack-up is 4 layers with vias under MOSFETs to create a dissipation path to the heatsink.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area. In Figure 23 below, we can see the vias configuration:

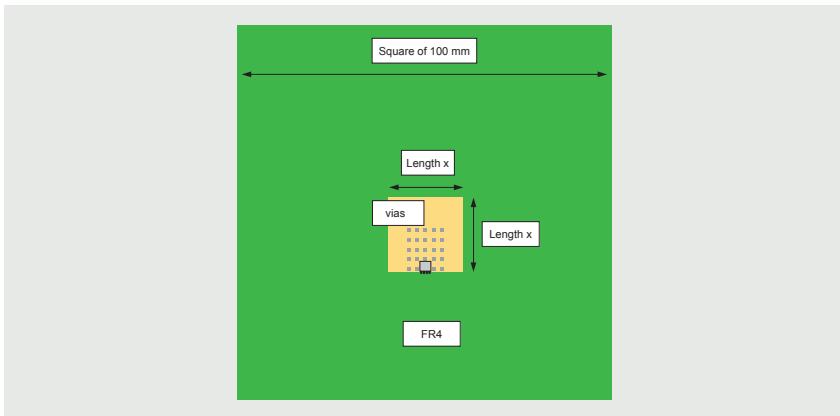


Figure 23 | Copper area configuration: LFPAK56D, 4 layers with vias

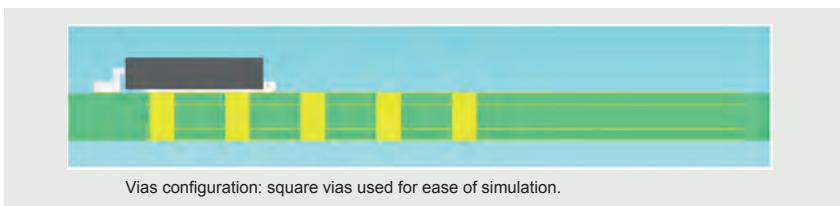


Figure 24 | Sectional view: LFPAK56D

Table 5: Limitation of number of vias

X (mm)	Vias configuration	Comments	Vias information
minimal footprint	2+2 vias	Maximum number of vias able to be inserted in the copper surface	
6	9+9 vias		
8	12+12 vias		
10	20+20 vias		
15	25+25 vias		
20	25+25 vias		
25	25+25 vias		
30	25+25 vias	25 vias maximum	
35	25+25 vias		
40	25+25 vias		
50	25+25 vias		

The graph in Figure 25 captures two important factors:

- T_j depends greatly on length "x" and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a "law of diminishing returns". In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j . As can be seen from the graph in Figure 25, T_j will plateau at around 36 °C (for 0.5 W per MOSFET) no matter how much copper area we provide.

Care must be taken for T_j above 120 °C as the PCB temperature directly under the transistor would be close to the MOSFET T_j .

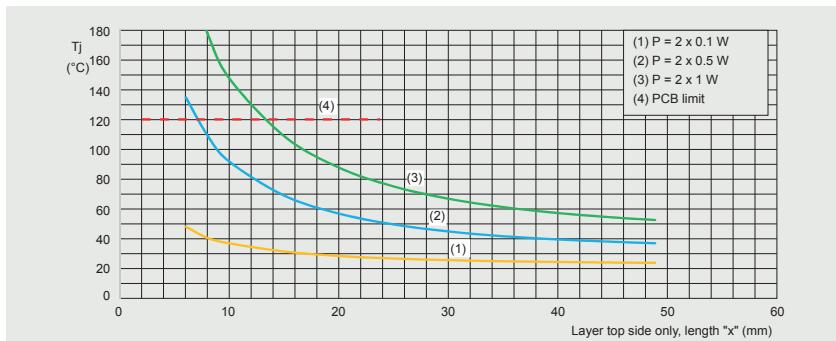


Figure 25 | Junction temperature as a function of copper side length x for LFPAK56D

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(\max)} = 175$ °C (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In the graph below, Figure 26 the maximum power for the conditions given is as follows:

$T_{\text{amb}} = 20$ °C: Max power is 5.3 W per MOSFET (2 × 5.3 W permissible in this package)

$T_{\text{amb}} = 80$ °C: Max power is 3.55 W per MOSFET (2 × 3.55 W permissible in this package)

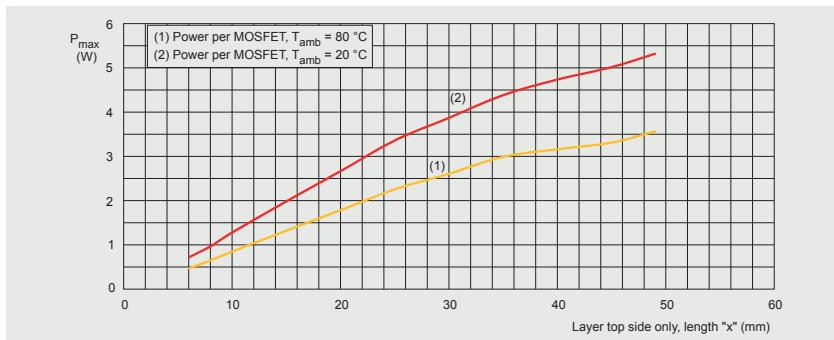


Figure 26 | Maximum permissible power dissipation as a function of copper side length x for LFPAK56D

3.2.2 LFPAK56D only one MOSFET active at a time

In a typical half bridge application only one MOSFET conducts at a time. Figure 27 below shows the results for 1 W applied to the left MOSFET (blue curve). We can see that 1 W dissipated in one MOSFET is not equivalent to 0.5 W dissipation in each of the two MOSFETs (yellow curve).

As can be seen temperature is higher in the case of one MOSFET conducting with 1 W than it is with two MOSFETs each dissipating 0.5 W.

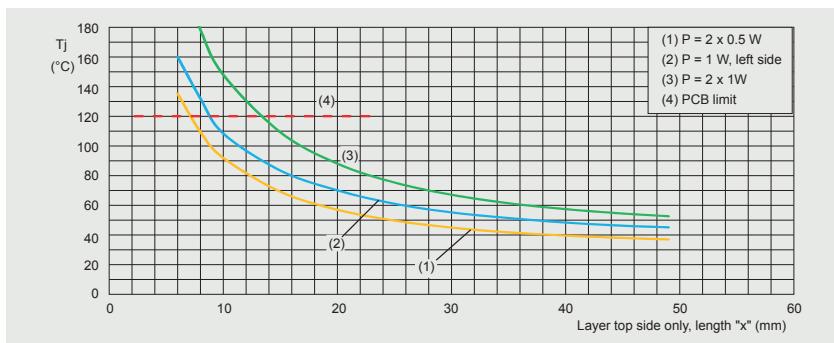


Figure 27 | Junction temperature as a function of copper side length x for LFPAK56D; one MOSFET

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(\max)} = 175$ °C (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In Figure 28 the maximum power for the conditions given is as follows:

- $T_{amb} = 20^{\circ}\text{C}$: Max power is 6 W with only left MOSFET
- $T_{amb} = 80^{\circ}\text{C}$: Max power is 4 W with only left MOSFET

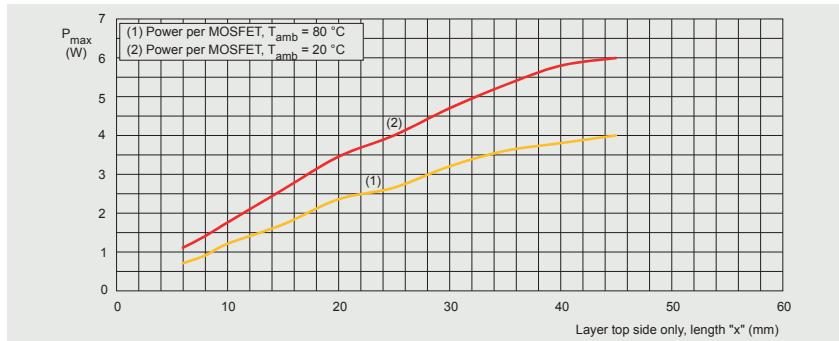


Figure 28 | Power dissipation as a function of copper side length x for LFPACK56D; one MOSFET

As previously mentioned, when only one MOSFET is active the second MOSFET does not make a significant contribution to the total dissipation capability – see Figure 19.

3.2.3 LFPACK33

Set-up:

- 4 layers + vias (vias number increases with the copper area with a maximum of 25 vias for each side)
- MOSFET power dissipation is 0.1 W, 0.5 W and 1 W applied in the MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness on all layers (external and internal) is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied i.e. only natural convection is modeled

The common PCB stack-up is 4 layers with vias under the MOSFETs to create a dissipation path to the heatsink.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

In Figure 29 below, we can see the vias configuration:

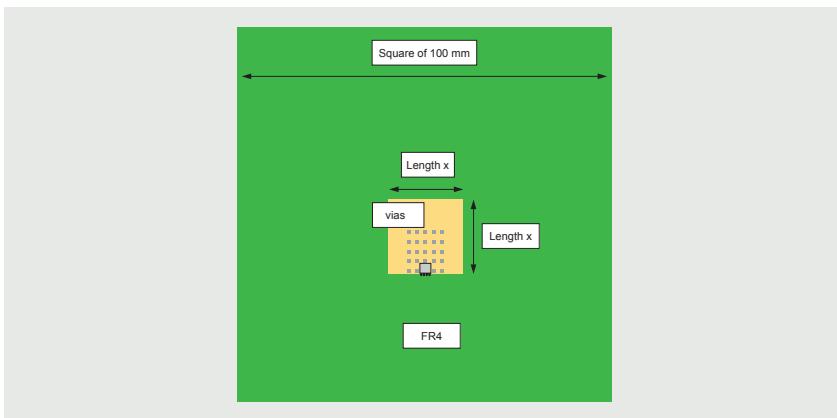


Figure 29 | Copper area configuration: LFPAK33, 4 layers with vias

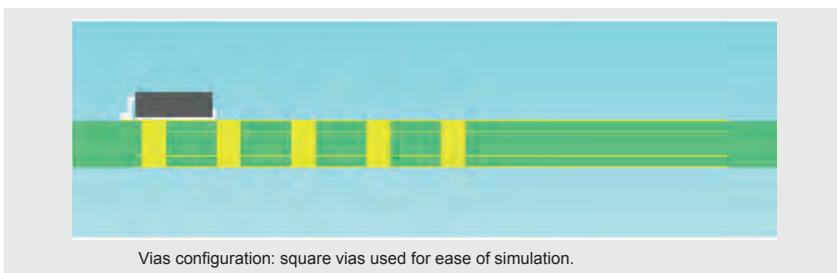


Figure 30 | Sectional view: LFPAK33

Table 6: Vias configuration

X (mm)	Vias configuration	Comments	Vias information
minimal footprint	1 via	Maximum number of vias able to be inserted in the copper surface	
6	6 vias		
8	9 vias		
10	20 vias		
15	25 vias		
20	25 vias		
25	25 vias		
30	25 vias	25 vias maximum	Vias pitch 2.5 mm Vias side length 0.7 mm Copper thickness 70 µm No solder fill
35	25 vias		
40	25 vias		
50	25 vias		

The graph Figure 31 captures two important factors:

- T_j depends greatly on length "x" and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a "law of diminishing returns". In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j . As can be seen from Figure 31 below T_j will plateau at around 33 °C (for 0.5 W per MOSFET) no matter how much copper area we provide.

Care must be taken for T_j above 120 °C as PCB temperature directly under the transistor would be close to the MOSFET T_j .

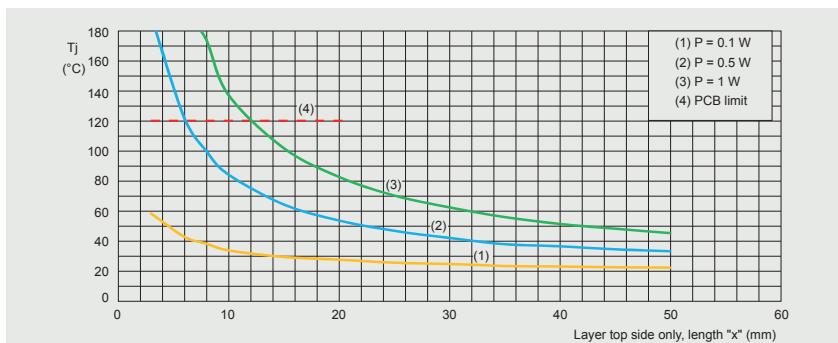


Figure 31 | Junction temperature as a function of copper side length x for LFPAK33

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(\max)} = 175$ °C (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In the graph below the maximum power for the conditions given is as follows:

$T_{\text{amb}} = 20$ °C: Max power is 6.5 W in the MOSFET

$T_{\text{amb}} = 80$ °C: Max power is 4.3 W in the MOSFET

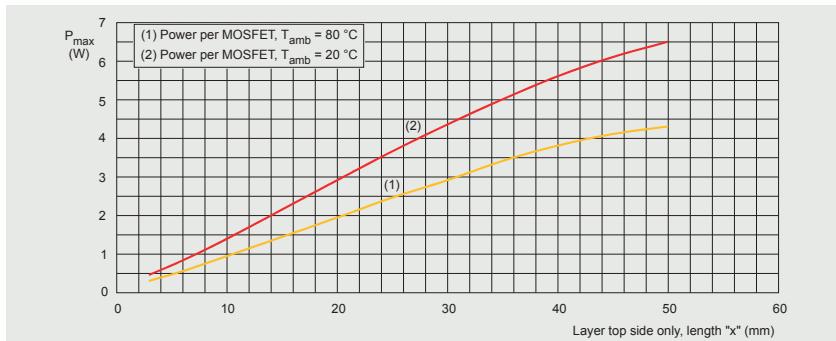


Figure 32 | Maximum permissible power dissipation as a function of copper side length x for LFPAK33

3.3 Placement advice for improved dissipation

In this section, we will present some results for two MOSFETs placed close to each other on a single layer PCB with varying copper area.

3.3.1. LFPAK56D

Simulation of two MOSFETs placed next to each other is carried out and checked against results seen in section 2.1. The aim is to understand the dissipation effect that the two LFPAK56D have on one another.

Set-up

- 1 layer on the top side
- MOSFET power dissipation is 0.5 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 200 x 150 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness on all layers (external and internal) is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

- 2 mm gap between right and left copper layers
- Simulation carried out for different length "x"
- 0.5 W applied on each internal MOSFET

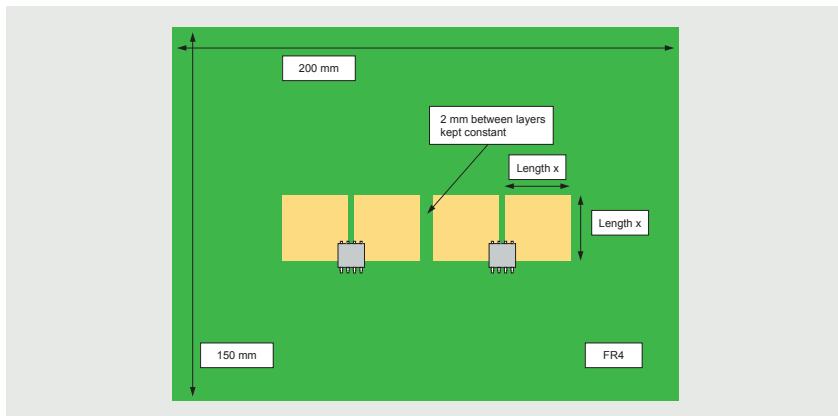


Figure 33 | Copper area configuration: LFPACK56D, single top copper layer

The graph in Figure 34 shows:

- The results (in green) are similar to the ones observed in section 2.1 (slightly higher +3 °C)
- This is due to the low conductivity of FR4, despite only 2 mm gap it showed no heat transfer from one copper area to the other

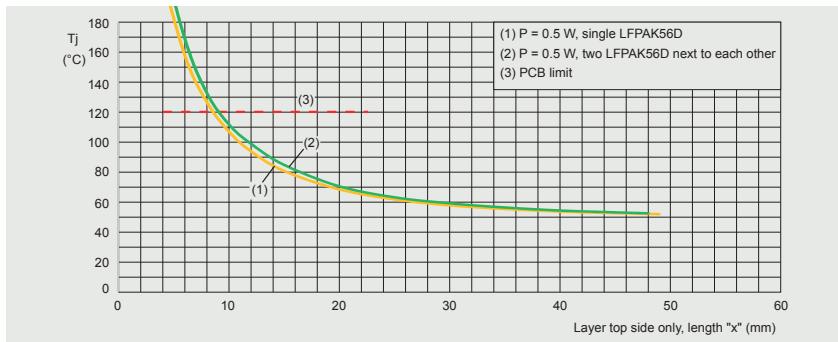


Figure 34 | Junction temperature as a function of copper side length x for 2 LFPACK56D

3.3.2 LFPACK33

Simulation of two MOSFETs placed next to each other is carried out and checked

against results seen in section 2.3. The aim is to understand the dissipation effect that the two MOSFETs have on one another.

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.5 W applied in the MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 200 x 150 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

- 2 mm gap between right and left copper layers
- Simulation carried out for different length "x"
- 0.5 W applied on each MOSFET

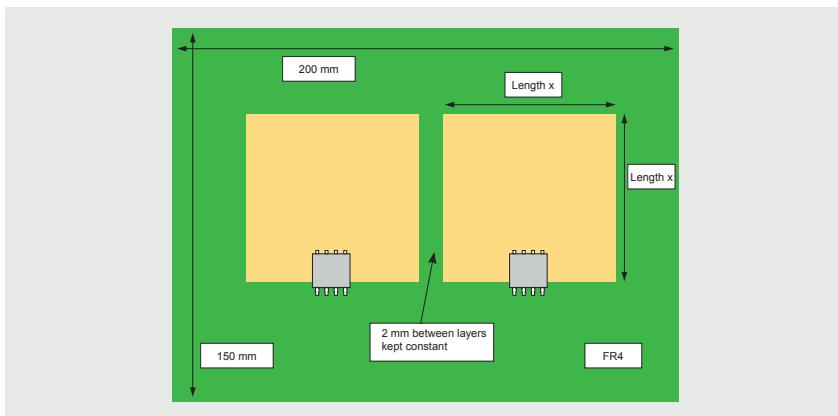


Figure 35 | Copper area configuration: LFPAK33, single top copper layer

The graph in Figure 37 shows:

- The results for $x > 20$ mm are similar to the ones observed in section 2.3 (slightly higher +3 °C)
- This is due to the low conductivity of FR4, despite only 2 mm gap it showed no

heat transfer from one copper area to the other

- For $x < 20$ mm results show up to 20 °C higher compared to the results from section 2.3.
- This is due to the MOSFETs being brought closer to each other as a result of reduced copper area – note that in this case the space between MOSFETs is half the space between MOSFETs in the case of LFPAK56D

In Figure 36 you can see that for $x = 10$ mm, the distance between the LFPAK33 MOSFETs is approximatively 10 mm. Less than 20 mm apart, the MOSFETs are close enough to heat each other, hence we start to see a temperature difference.

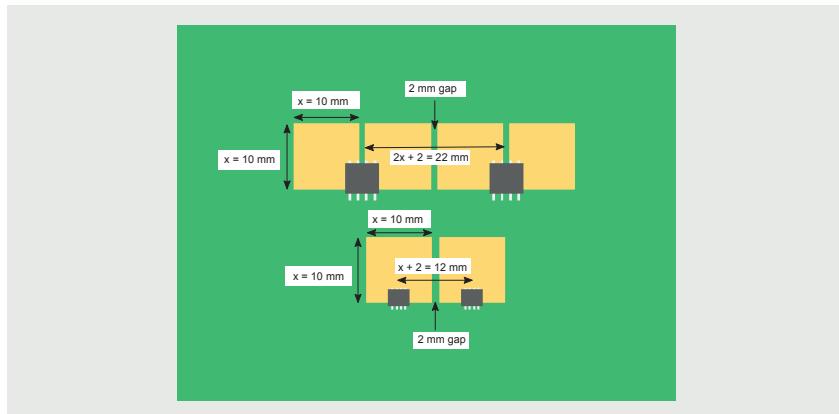


Figure 36 | Copper area configuration: 2 x LFPAK33, 2 x LFPAK56D; separation between MOSFETs

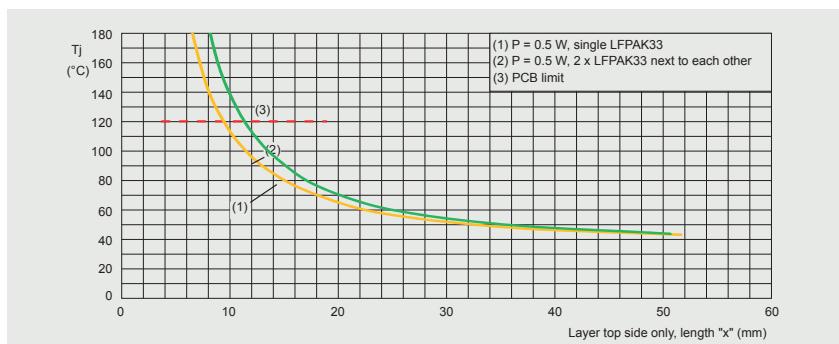


Figure 37 | Junction temperature as a function of copper side length x for 2 LFPAK33

3.4 Comparison between two LFPAK56 and one LFPAK56D, then one LFPAK56D and two LFPAK33

In this section we will present some comparative results for different package devices on a single layer board with varying copper area.

3.4.1 Two LFPAK56 to LFPAK56D

In this section the results of two single LFPAK56 MOSFETs are compared to the results of one dual LFPAK56D MOSFET (see Section 3.1.1)

The aim is to highlight the benefit of using one LFPAK56D dual MOSFET instead of two single LFPAK56 MOSFETs.

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.5 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

- Same gap between copper layer was used for both single LFPAK56 and dual LFPAK56D
- Simulation carried out for different length "x".
- 0.5 W applied on each MOSFET

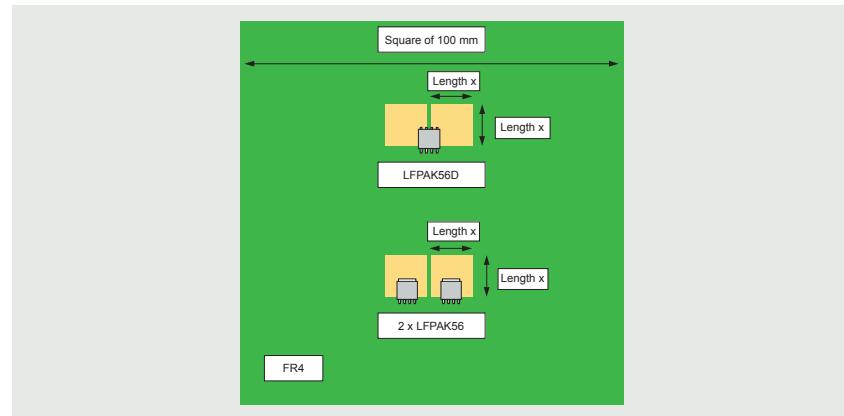


Figure 38 | Copper area configuration: 1 x LFPAK56D, 2 x LFPAK56, single top copper layer

The graph in Figure 39 shows:

- Overall two single LFPAK56 show better heat dissipation than one dual LFPAK56D by up to approximately 10 °C. This is due to the larger surface area of the LFPAK56 drain tab giving improved heat spreading and thermal dissipation.
- Note that the 10 °C is the relative figure between the two packages, the most important factor is the operating junction temperature
- If there is enough margin before reaching 175 °C at the junction, then LFPAK56D offers an attractive option due to its space saving

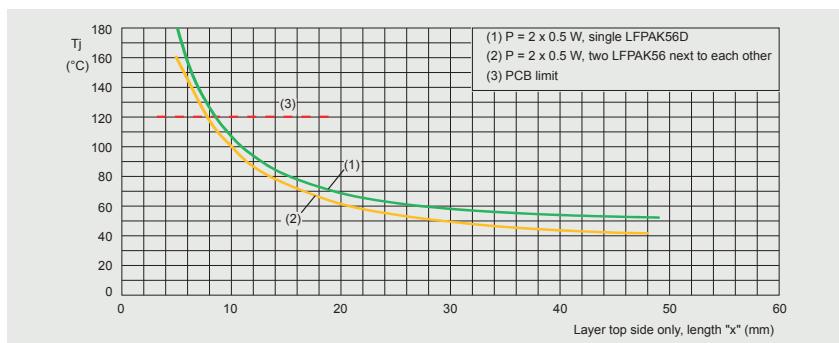


Figure 39 | Junction temperature as a function of copper side length x for 2 LFPAK56 and 1 LFPAK56D

3.4.2 LFPAK56D to two LFPAK33

In this section the results of one dual LFPAK56D MOSFET are compared to the results of two single LFPAK33 MOSFETs (see section 4.2)

Aim is to highlight the benefit of using one LFPAK56D dual instead of two single LFPAK33.

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.5 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./Ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

- Same gap between copper layer was used for both single LFPAK33 and dual LFPAK56D
- Simulation carried out for different length "x"
- 0.5 W applied on each MOSFET

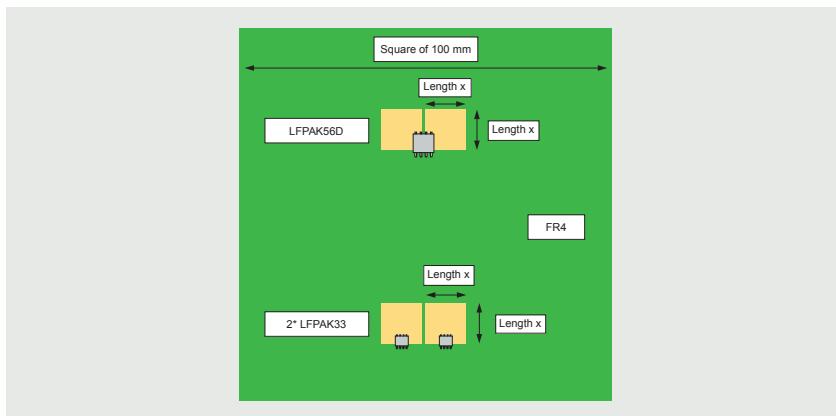


Figure 40 | Copper area configuration: 1 x LFPAK56D, 2 x LFPAK33, single top copper layer

The graph in Figure 41 shows:

- Overall two single LFPAK33 show better heat dissipation than a dual LFPAK56D by up to approximately 5 °C. This is due to the larger drain surface area of the LFPAK33 offering better thermal dissipation, (less improvement than with LFPAK56 as LFPAK33 is a smaller package).
- Note that the 5 °C is the relative figure between the two packages, the most important factor is the operating junction temperature.
- If there is enough margin before reaching 175 °C at the junction, then LFPAK56D offers an attractive option due to all the advantages that one component offers versus two in terms of PCB layout, placement, cost effectiveness, etc.

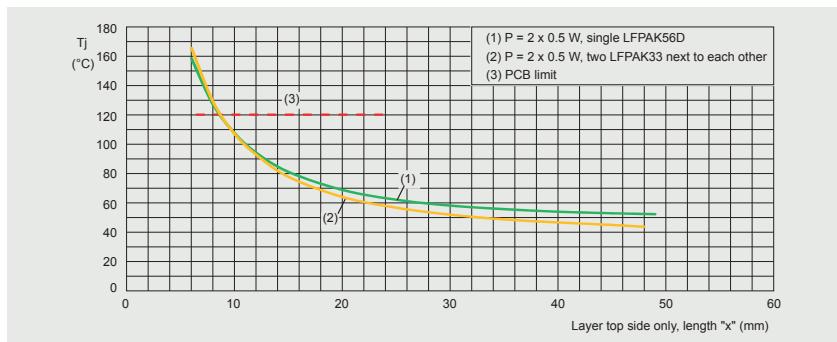


Figure 41 | Junction temperature as a function of copper side length x for 1 LFPAK56D and 2 LFPAK33

3.5 Impact of $R_{th(j\text{-mb})}$ compared to $R_{th(mb\text{-amb})}$

Dissipation losses from the MOSFET junction are not mainly limited by the thermal resistance $R_{th(j\text{-mb})}$ as this is very low. The high thermal path for heat dissipation is presented by the thermal resistance $R_{th(mb\text{-amb})}$ (mounting base to PCB to ambient).

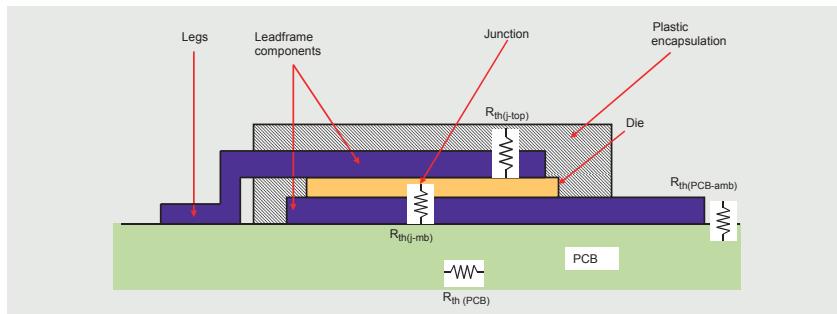


Figure 42 | View of thermal resistances in and outside the MOSFET

Example: for the part number BUK7M15-60E (LFPAK33, 15 mΩ, 60 V) the maximum thermal resistance junction to mounting base is 2.43 K/W:

Table 7: Thermal resistance BUK7M15-60E

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-mb})}$	thermal resistance from junction to mounting base	Fig. 5	-	2.01	2.43	K/W

Using thermal simulation (Flotherm) with the following conditions:

0.5 W of losses in the MOSFET, air ambient is 20 °C, 35 µm copper, we can calculate some thermal resistance.

- $R_{th(j\text{-mb})}$ is 0.8 K/W
 - This is a lower value than given in the data sheet due to the simulation using ideal conditions
- As can be seen in Table 8 below, thermal resistance for other items have high value compared $R_{th(j\text{-mb})}$
- The total thermal resistance, junction to ambient, is 59.4 K/W when using 65.4 °C as (ambient) reference point.

Table 8 lists temperatures for different points captured in the simulation and shown in Figure 43.

Table 8: Breakdown of thermal resistance for a simple case

Thermal resistance part	Temperature (°C)	R_{th} (K/W)
Junction	95.1	-
Mounting base	94.7	0.8
PCB under MOSFET	88.6	12.2
PCB to the right of the MOSFET	86.6	4
Ambient air 0.5 mm over the top of the PCB	79.1	15
Ambient air 1 mm over the top of the PCB	65.4	27.4

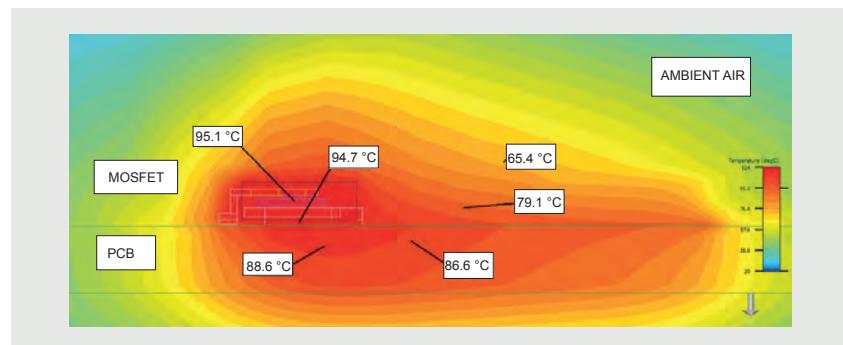


Figure 43 | Thermal result, LFPAK33, 0.5 W, 20 °C ambient

Due to the very low thermal resistance between junction and mounting base it is very important to take care of design surrounding the MOSFET, (i.e. thermal vias, copper area, heat sink, water cooling, air cooling), in order to reduce the total thermal resistance.

4 LFPAK56 and LFPAK88

4.1 Simple configuration with a single layer

In this section, we will present the maximum power dissipation results for a simple PCB configuration using a single layer with varying copper area.

Results are given for the LFPAK56 and LFPAK88 packages. Models used are based on 1 mΩ LFPAK56E and LFPAK88.

4.1.1 Set-up:

- 1 copper layer on the top
- MOSFET power dissipation is 1 W, 1.5 W and 2 W
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- PCB operating temperature of 120 °C and T_j of 175 °C are highlighted in graphs
- Copper thickness is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer, see Figure 44.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of the top copper area and calculate the maximum power that can be safely dissipated in the MOSFET to reach a T_j of 175 °C.

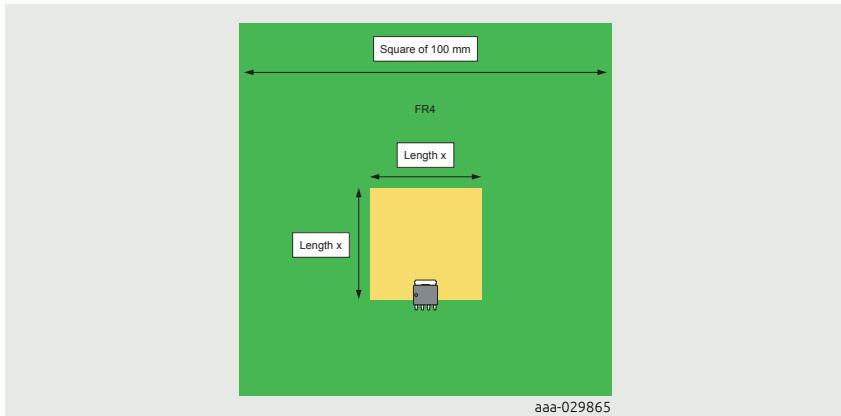


Figure 44 | Copper area configuration: LFPAK56, single top copper layer, the configuration is the same for LFPAK88

4.1.2 Junction temperature as a function of copper area

The graphs in Figure 45 and Figure 46 capture two important factors:

- T_j depends greatly on length "x" and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a "law of diminishing returns". In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j . As can be seen from Fig. 45 below, for LFPAK56, 1 W profile, T_j will plateau at around 55 °C.

Note: Standard FR4 PCBs operate at a maximum temperature of 120 °C, care must be taken for $T_j > 120$ °C as the PCB area directly under the transistor will be close to the MOSFET junction temperature, (due to low $R_{th(j-mb)}$).

The graphs below also shows the absolute minimum copper area needed for $T_j \leq 175$ °C.

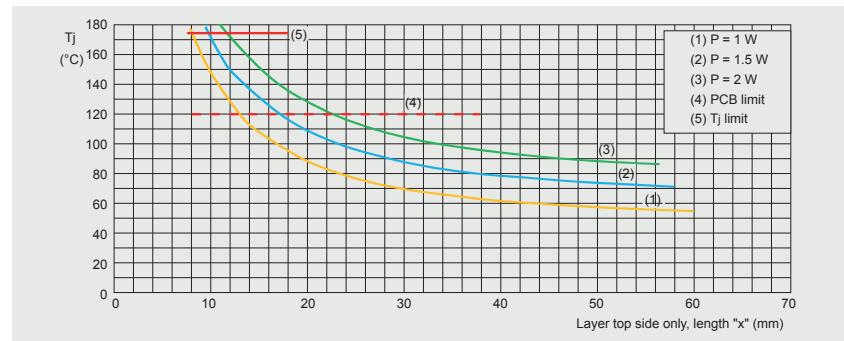


Figure 45 | Junction temperature as a function of copper side length x for LFPAK56

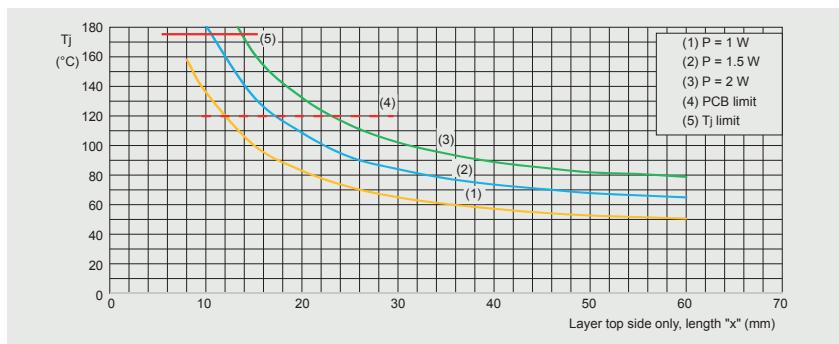


Figure 46 | Junction temperature as a function of copper side length x for LFPAK88

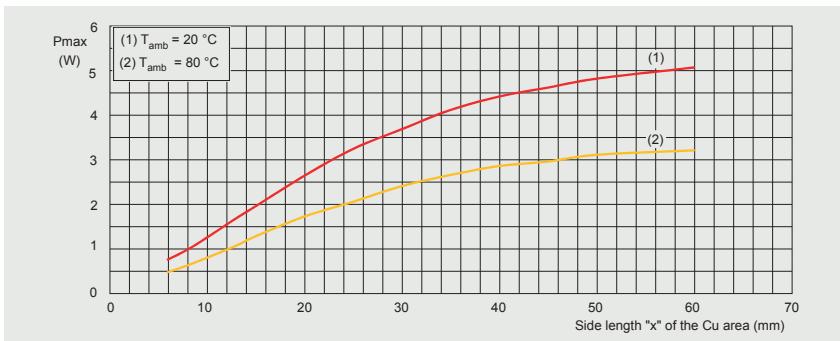
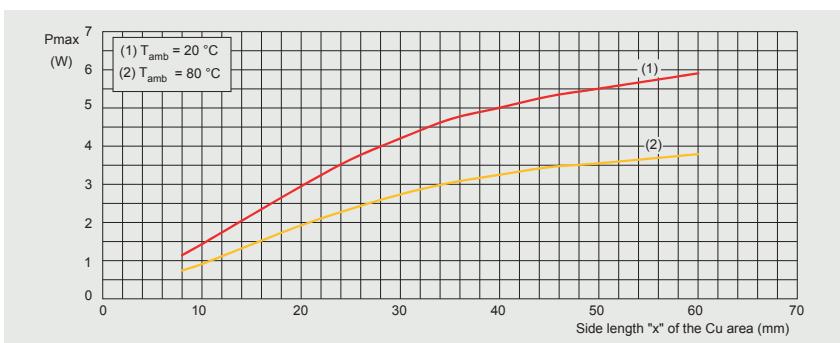
4.1.3 Maximum allowed power dissipation as a function of copper area

The maximum allowed power dissipation is shown in Figure 47 and Figure 48 below, for different ambient temperature and copper side length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

From graphs in Figure 47 and Figure 48 the maximum permissible power, ($T_{amb} = 20\text{ }^{\circ}\text{C}$), is 5.05 W and 5.9 W for the LFPAK56 and LFPAK88 packages respectively:

Table 9: Maximum power dissipation

Device	$T_{amb} = 20\text{ }^{\circ}\text{C}$	$T_{amb} = 80\text{ }^{\circ}\text{C}$
LFPAK56	5.05 W	3.2 W
LFPAK88	5.9 W	3.8 W

**Figure 47** | Maximum permissible power dissipation as a function of copper side length "x" for LFPAK56**Figure 48** | Maximum permissible power dissipation as a function of copper side length "x" for LFPAK88

4.2 Usual configuration: 4 layers + vias

In this section, we will present the maximum power dissipation results for a PCB configuration using 4 layers + vias for dissipation on the bottom layer, with varying copper area.

Results are given for the LFPAK56 and LFPAK88 packages.

4.2.1 Set-up:

- Four layers with vias (max number of vias is 25 and for small copper areas this number will decrease accordingly, see Table 10)
- MOSFET power dissipation is 1 W, 1.5 W and 2 W
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- PCB operating temperature of 120 °C and T_j of 175 °C are highlighted in graphs
- Copper thickness of all layers is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The common PCB stack-up is 4 layers with vias under the MOSFET to create a dissipation path to heatsink (no heat sink was used in simulation).

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of copper area (same area size applied to all layers).

The configuration of the vias is shown below in Figure 49 and Figure 50:

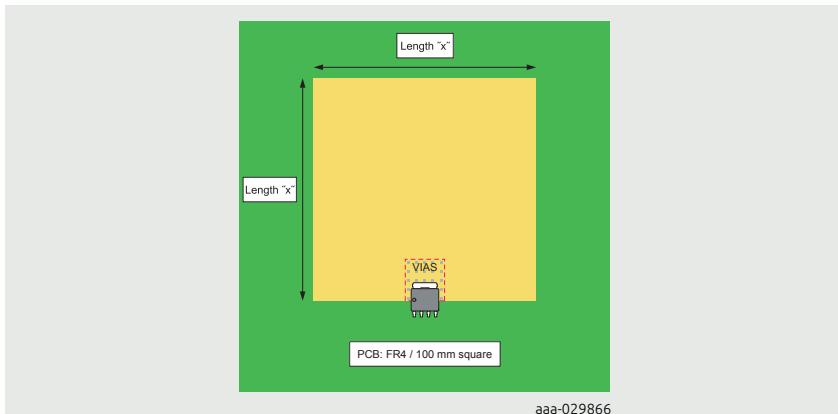


Figure 49 | Copper area configuration: LFPAK56, 4 layers with vias, the configuration is similar for LFPAK88

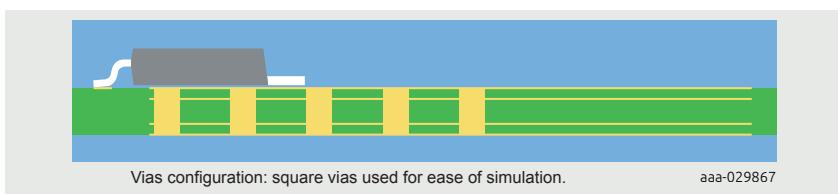


Figure 50 | Sectional view: LFPAK56

Table 10: Limitation of number of vias

X (mm)	Vias configuration	Comments	Vias information
6	9 vias		
8	9 vias	Maximum number of vias able to be inserted in the copper area	
10	20 vias		
15	25 vias		Square vias length 0.7 mm
20	25 vias		Vias pitch: 2.5 mm
25	25 vias		(between vias in columns) 2.0 mm
30	25 vias		(between vias in rows)
35	25 vias	25 vias maximum	Copper thickness: 70 µm
40	25 vias		No solder fill
45	25 vias		
50	25 vias		
60	25 vias		

4.2.2 Junction temperature as a function of copper area (4 layers and vias)

The graphs in Figure 51 and Figure 52 below show the junction temperature as a function of drain copper area following the same trend as the single layer PCB configuration in that:

- T_j depends greatly on copper area
- The ability of the top copper to provide heatsinking for the MOSFET shows a “law of diminishing returns”.

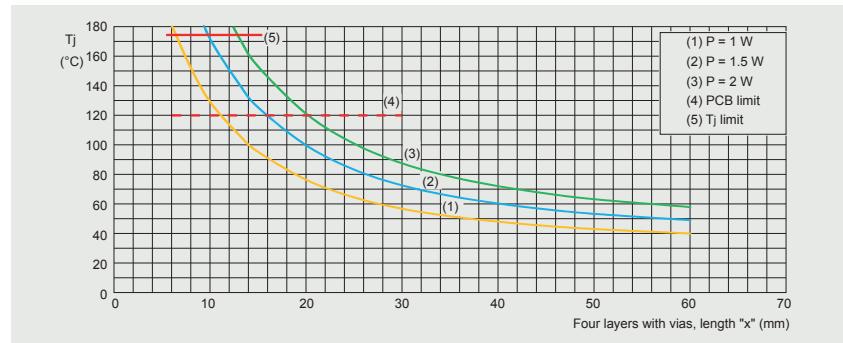


Figure 51 | Junction temperature as a function of copper side length x for LFPAK56

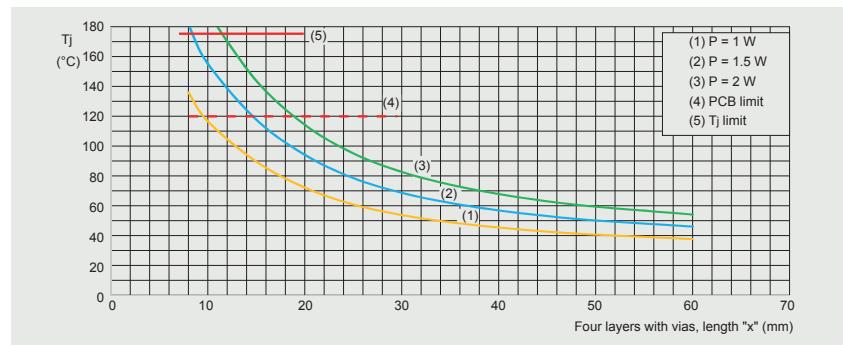


Figure 52 | Junction temperature as a function of copper side length x for LFPAK88

4.2.3 Maximum allowed power dissipation as a function of copper area (4 layers and vias)

From graphs in Figure 53 and Figure 54 the maximum power for a given package and conditions are as follows:

Table 11: Maximum power dissipation

Device	$T_{amb} = 20\text{ }^{\circ}\text{C}$	$T_{amb} = 80\text{ }^{\circ}\text{C}$
LFPAK56	9.6 W	6.3 W
LFPAK88	10.65 W	6.9 W

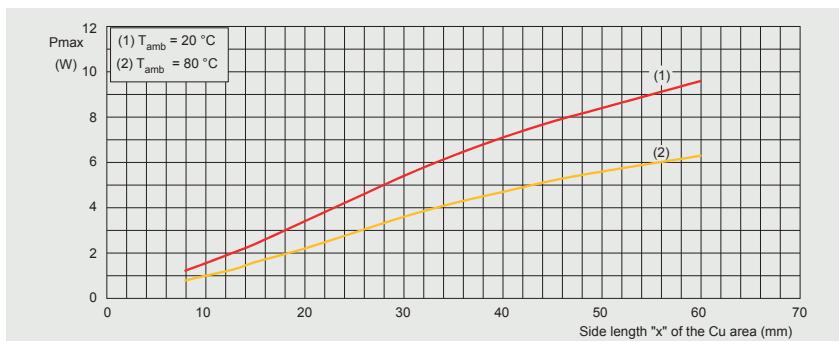


Figure 53 | Maximum permissible power dissipation as a function of copper side length “x” for LFPAK56

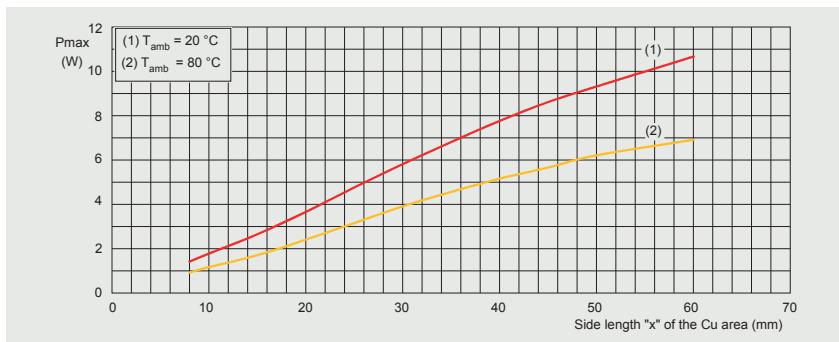


Figure 54 | Maximum permissible power dissipation as a function of copper side length “x” for LFPAK88

4.3 Simple configuration with a single split layer of copper

In this section, we will present the maximum power dissipation results as per the previous section for a simple PCB configuration using a single layer and varying copper area, but with copper layer split in two part (one part placed under the drain tab of the MOSFET and the other under the source pins).

Results are given for the LFPAK88 package only.

4.3.1 Set-up:

- 1 copper layer on the top - split into two areas:
 - 3/5 of area under drain tab
 - 2/5 of area under source pins
- MOSFET power dissipation is 1 W, 1.5 W and 2 W
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- PCB operating temperature of 120 °C and T_j of 175 °C are highlighted in graphs
- Copper thickness is 2 oz./ft² (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer, see Figure 55.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of the top copper area.

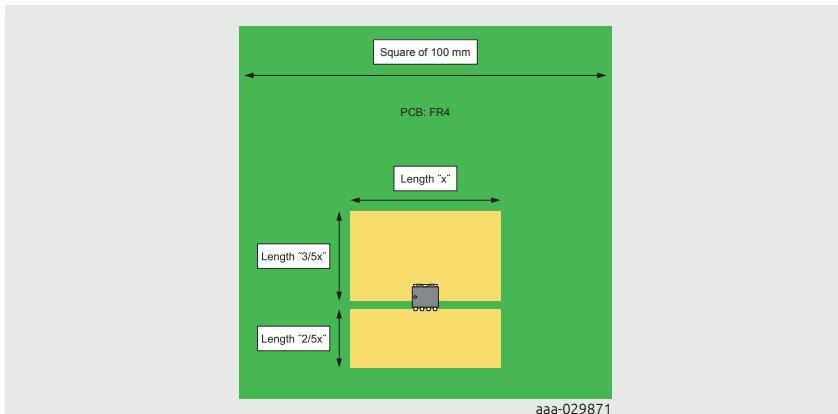


Figure 55 | Split copper area configuration: LFPAK88, single top layer with copper

The graph in Figure 56 captures what has been previously mentioned in terms of copper area and heat dissipation i.e. the bigger the area the better the thermal performance. More importantly in this configuration, it shows the importance in considering the source pins of an LFPAK MOSFET as a thermal path for efficiently dissipating heat.

The graph in Fig. 56 also shows that copper area of length "x" = 40 mm in split copper configuration provides a performance equivalent of that provided in the solid (non-split) copper area of length "x" = 60 mm.

Split copper configuration for length "x" = 40 mm is as follows:

- 24 mm x 40 mm copper area placed under the drain tab of the LFPAK MOSFET
- 16 mm x 40 mm copper area placed under the source pins of the LFPAK MOSFET

Note: Standard FR4 PCBs operate at maximum temperature of 120 °C, care must be taken for $T_j > 120$ °C as PCB area directly under the transistor would be close to the MOSFET junction temperature (due to low $R_{th(j-mb)}$).

Results are for LFPAK88, but the principle applies to all Nexperia clip bond LFPAK devices. $T_{amb} = 20$ °C: Max power of ~6 W is achieved with an area of 40 mm x 40 mm single copper layer in split configuration, whilst previously shown to require an area of 60 mm x 60 mm for single solid copper layer.

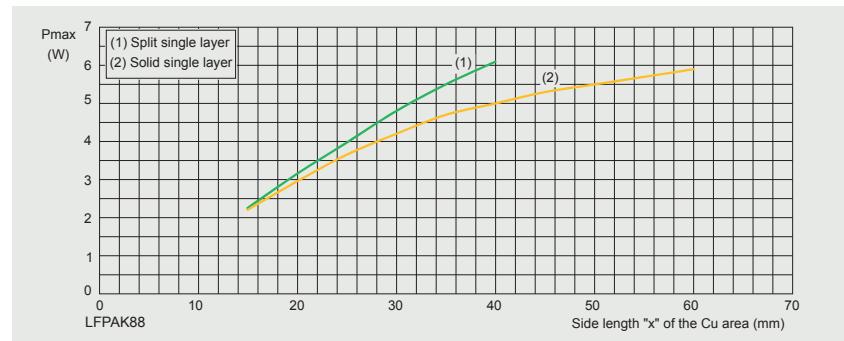


Figure 56 | Maximum permissible power dissipation as a function of copper side length “x” for LFPAK88

4.4. Impact of $R_{th(j\text{-mb})}$ compared to $R_{th(mb\text{-amb})}$

The thermal resistance $R_{th(j\text{-mb})}$ of the MOSFET is very low and therefore dissipation losses are mainly limited by the high thermal resistive path presented by $R_{th(mb\text{-amb})}$ (mounting base to ambient).

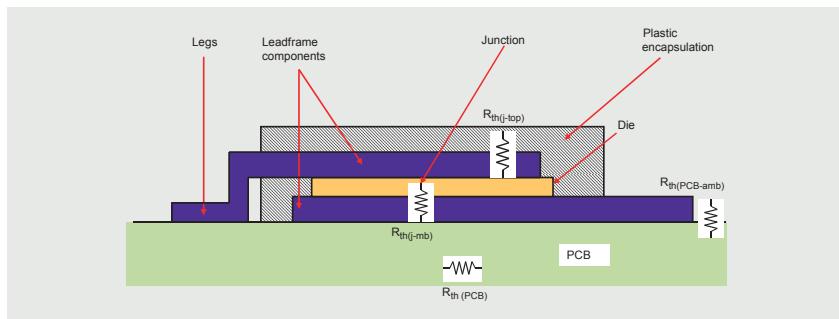


Figure 57 | View of thermal resistances in and outside the MOSFET

Example: for the part number BUK7S1R0-40H (LFPAK88, 1 mΩ, 40 V) the maximum thermal resistance junction to mounting base is 0.4 K/W, see Table 12:

Table 12: Thermal resistance BUK7S1R0-40H

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	-	0.35	0.4	0.4	K/W

Using thermal simulation (Flotherm) with the following conditions:

- 1 W of losses in the MOSFET
- Ambient air temperature of 20 °C
- 70 µm copper

we can calculate the thermal resistance for different paths, example:

- 1 W of losses in the MOSFET
- Junction temperature = 52.2 °C
- Mounting base temperature = 52.0 °C
- $R_\Theta = \Delta T / P \Rightarrow R_{th(j\text{-}mb)} = 0.2 \text{ K/W}$.

This is lower than the measured value given in the data sheet due to simulation using ideal conditions.

As can be seen in Figure 58 below, the thermal resistance between mounting base and ambient is of much higher value (~30 K/W) than $R_{th(j\text{-}mb)}$.

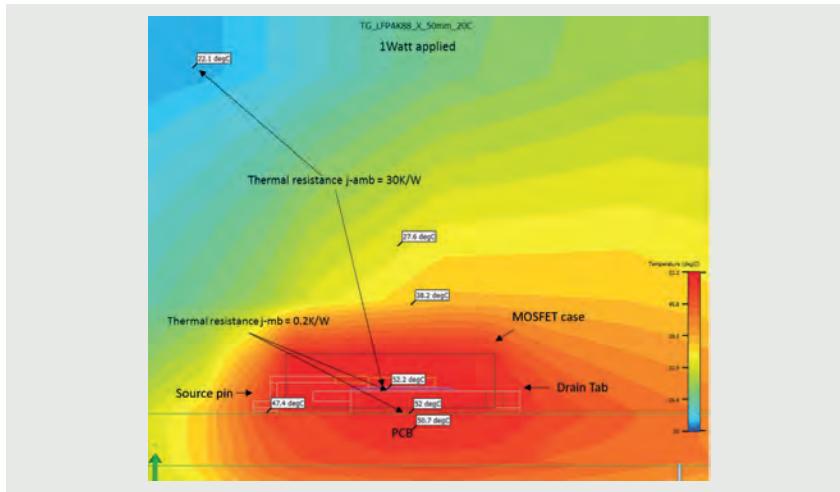


Figure 58 | Thermal resistance LFPAK88: single layer copper profile (50 x 50 mm)

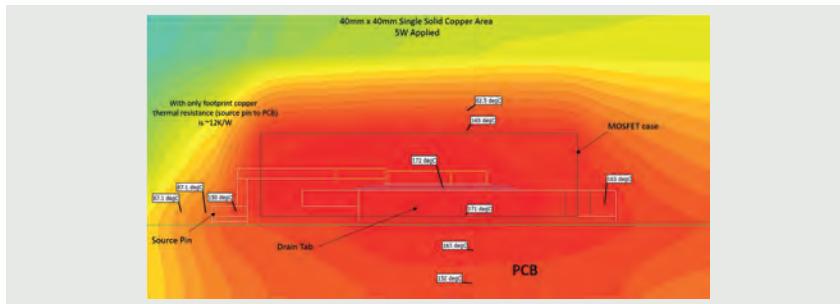


Figure 59 | Thermal resistance LFPAK88: single layer copper profile (40 x 40 mm)

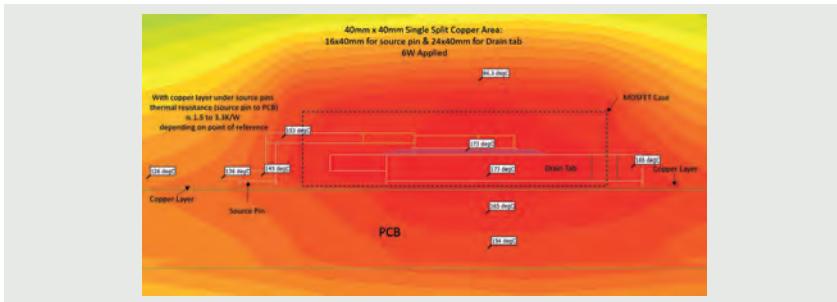


Figure 60 | Thermal resistance LFPAK88: single split layer copper profile (40 x 40 mm: split into 24 x 40 mm and 16 x 40 mm)

5 Conclusion

All the LFPAK packages offer a very good junction to mounting base thermal performance, meaning that the mounting base can be near to the junction temperature, but this is often limited by the PCB high temperature capability.

It is very important for designs to reduce the thermal resistance between mounting base and the ambient environment as this will present the bottleneck in heat dissipation. All of Nexperia LFPAK packages use clip bond technology making their source pins a good thermal path in addition to the thermal path provided by the drain tab. To take full advantage of this feature, it is important for PCB layout designs to consider placing a good amount of copper under the source pins. The drain tab still presents the main thermal path for heat dissipation and should be the focus for any thermal design layout.

In all cases a configuration with 4 layers with vias substantially improves the heat dissipation.

This thermal guide establishes the necessary principles in thermal design approaches, combined with LFPAK packages features (i.e. low $R_{th(j\rightarrow mb)}$) and source clip bond) offer the designer good options in optimizing PCB thermal design.

Good thermal design practices should be applied to take advantage of the very good thermal performance LFPAK packages and $T_{j(max)}$ must be kept $< 175^{\circ}\text{C}$ for safe operation.

		
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<p> Visit blog</p> <p>LFPACK56D taking the heat out of engine management systems</p>	<p> Visit blog</p> <p>Weighing the benefits of LFPACK</p>	<p> Visit blog</p> <p>LFPACK88 A very cool customer</p>
		
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Chapter 10

Maximum continuous currents in Nexperia LFPAK power MOSFETs

Application Note: AN90016

1 Introduction

This chapter examines the factors that determine the maximum permissible current ratings for LFPAK (copper-clip package) MOSFETs.

Modern electronics using low-voltage (<100 V) MOSFETs has seen an increase in high-power demand in both automotive and industrial applications. Power output in kilowatt terms for applications such as motor drive is now a very common requirement. Combined with the existing space constraint in modules this means that the need to handle more power is being passed on to the components, particularly MOSFETs.

The current limit given in data sheets for power MOSFETs is one of the most important parameters in such high-power applications where the handling of very high currents is required.

As the MOSFET is a three terminal device – Gate, Source and Drain – current can flow through any of these terminals as I_G , I_S and I_D respectively. Only maximum continuous current I_D (drain- source) and continuous current I_S (source-drain/body diode) will be considered. Leakage currents (I_{GSs} , I_{DSs}) and pulsed currents such as I_{DM} are not in the scope of this document

This chapter gives a comprehensive insight into the methodology in determining the maximum continuous current rating of Nexperia power MOSFETs.

It is critical to fully understand the capabilities, the boundaries and the relevant environmental conditions so that electronics engineers and designers select the right MOSFET for the right application - all of which will be discussed and addressed in this document.

This chapter is specific for LFPAK and its copper clip bond technology – Nexperia's flagship package.

2 LFPAK, superior performance

LFPAK packages are compact in size, they offer much higher power density and reduced parasitic inductances compared with wire bond devices. Combined with their copper clip bond technology, they have played an important role in MOSFETs achieving a very high current capability.

As illustrated in Figure 1 below, LFPAK copper clip bond packages have the following benefits:

- Prevents localised current crowding shown in Fig 1 b) D²PAK wire bond package

- Allows for a more uniform current spread
- Acts as a heat sink to the die

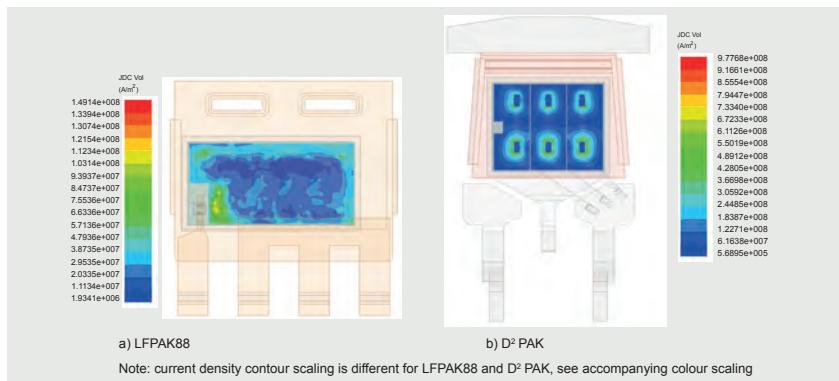


Figure 1 | Current crowding contours for a) LFPAK88 and b) D²PAK packages

3 Key parameters that set out the boundaries

Before discussing what maximum current a MOSFET can achieve, it is important to highlight the parameters governing the boundaries of the environment within which the MOSFET must operate. These boundaries are mainly set by the thermal environment, but also by the conditions that impact the MOSFET data sheet parameters; both have a direct effect on the performance and the capabilities of the MOSFET.

Thermal environment and thermal parameters

This section discusses the thermal parameters and explains their direct impact on the maximum current in a MOSFET.

Temperature range and the 175 °C limit

-55 °C is the lowest temperature given in the data sheet. Although normally this is associated with storage temperature, MOSFETs' characteristics in Nexperia data sheet are given against this value. Note - the lowest temperature associated with real life application is usually **-40 °C**

25 °C (unless otherwise stated) is the reference temperature that all maximum capabilities of MOSFETs are based upon. In Nexperia MOSFET data sheets, this is given as a mounting base temperature parameter – **T_{mb}** – referring to the central point of the MOSFET drain tab. Note - other MOSFET vendors commonly use T_c

(case temperature), which refers to the same point, i.e. drain tab and not to the plastic part of the MOSFET.

175 °C refers to the junction, i.e. the silicon die, temperature of the MOSFET and the parameter for this is given as T_j . All MOSFETs must operate below this temperature – more details are given later.

The 175 °C limit explained

With high temperatures, it is understandable to think that the plastic mould should be the first cause of concern.

Historically plastic moulds have caused issues and although improvements have been made in this industry, if the right compound is not properly selected it can still cause issues and leads to device failures. However, plastic mould compound alone does not give the full story nor is it the source of setting the 175 °C limit, as will be discussed in the next section.

4 MOSFET structure

This section briefly discusses the main components in the internal structure of LFPAK MOSFETs and their temperature properties:

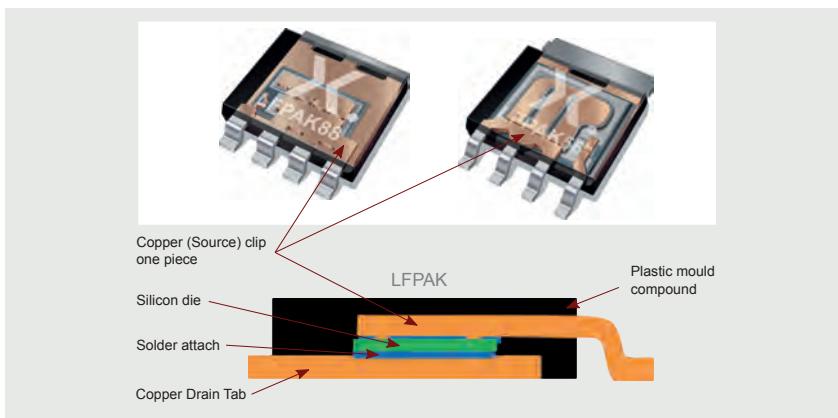


Figure 2 | LFPAK internal structure

Silicon / die: 250 °C. Pure silicon melting temperature is 1,414 °C. However, silicon in the MOSFET is doped and at ~250 °C there will be thermal activation where current will flow across the PN junction and the MOSFET no longer acts as a switching device – i.e. there is no control over turn-on / turn-off.

Copper clip: melting temperature of copper is 900 °C. This is to highlight the fact

that it can handle very high temperature and not used for any calculation purposes. The criteria used to make sure that the copper in the MOSFET is capable for current handling is explained later in the note.

Solder attach: melting point >300 °C.

Plastic mould compound: Can potentially harden and becomes brittle around 190 °C and above. The composition of the plastic mould compound is carefully selected to withstand high temperature specification.

As shown above, the internal components of the MOSFET are either naturally capable of withstanding temperatures >175 °C or specifically selected to do so.

Limiting the MOSFETs maximum junction temperature T_j to 175 °C is driven by the reliability requirements MOSFETs need to meet. And thus, 175 °C is the temperature limit used by Nexperia for qualification and life test of MOSFETs in line with industry standard.

All automotive power MOSFETs must meet the 175 °C junction temperature specification. Although this requirement is not applicable to non-automotive devices which meet T_j of 150 °C, most of Nexperia industrial MOSFETs are life tested and qualified to 175 °C.

5 Maximum power and maximum current

5.1 Maximum power

With the junction temperature limit set to a maximum of 175 °C, the maximum amount of power allowed in the MOSFET can then be determined.

The key parameters needed to calculate this maximum power allowance are the thermal impedance between the die and the mounting base; $Z_{th(j\text{-}mb)}$ and thermal resistance between the die and the mounting base $R_{th(j\text{-}mb)}$.

$R_{th(j\text{-}mb)}$ is the thermal resistance which means that the thermal response has reached steady state conditions (also referred to as DC conditions).

$Z_{th(j\text{-}mb)}$ is the term used to represent thermal impedance in its entirety, steady state as well as transient conditions (more details are given later).

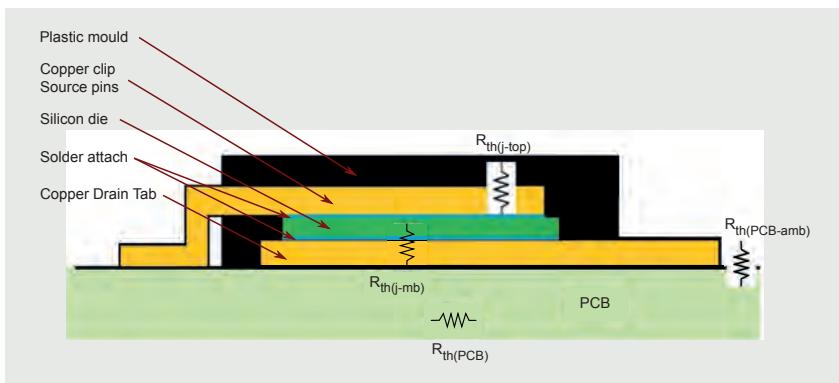


Figure 3 | Thermal resistances inside and outside the MOSFET

Figure 3 illustrates the main thermal paths that exist from the MOSFET silicon die to the external surroundings and ambient environment. The dominant path in dissipating heat from the die is through the MOSFET drain tab and therefore the thermal impedance of most relevance is $Z_{th(j-mb)}$ (also referred to as $R_{th(j-mb)}$).

It is worth pointing out that the source clip in the LFPAK package also provides an important thermal path. Having the right amount of copper in the PCB layout for the source pins is beneficial and should be considered in the design.

The LFPAK thin plastic mould adds another option of dissipating heat from the top of the device should the design consider a heat sink at the top. For more details about thermal performance and recommendations please refer to the application note AN90003 (chapter 9 of this book) - LFPAK MOSFET thermal design.

As previously mentioned all maximum capabilities of the MOSFET are given in reference to $T_{mb} = 25^{\circ}\text{C}$.

The maximum power allowance can then be derived from the following formula:

$$P_{(max)} = \frac{T_{j(max)} - T_{(mb)}}{R_{th(j-mb)}} \quad [1]$$

The junction to mounting base thermal impedance values can be obtained from the graph provided in the data sheet; the parameter used is transient thermal impedance $Z_{th(j-mb)}$.

For references the device used in the application note is PSMNR70-40SSH (LFPAK88 0.7 mΩ, 40 V, standard level) qualified to 175 °C.

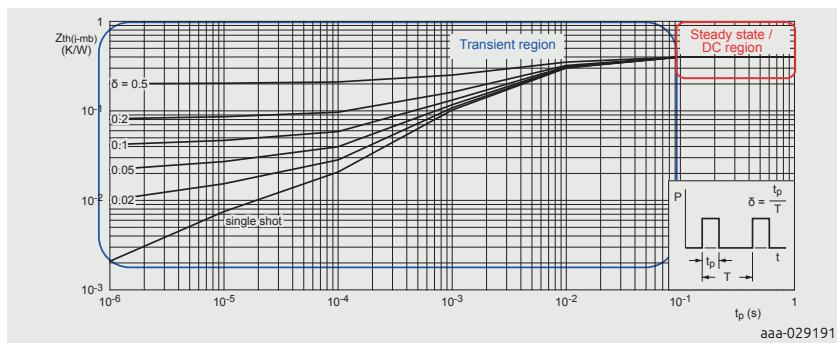


Figure 4 | Transient thermal impedance from junction to mounting base as a function of pulse duration

As can be seen from the graph in Fig. 4 the MOSFET thermal response is similar to an RC network electrical response – hence the thermal models provided on Nexperia support page representing this response are referred to as RC thermals – see the Support tab of the PSMNR70-40SSH product information page. For detailed information about RC thermal models see application note AN11261 (chapter 5 of this book) - Using RC Thermal models.

The curve in the graph showing pulses up to 100 ms is known as the transient condition section (transient region) and the parameter used is $Z_{th(j\text{-mb})}$. It is given in single shot pulse or repeated PWM pulses with various duty cycles. The transient region is relevant to situations such as short circuits, power surges or switching transitions, they tend to be high power for short periods of time. Larger devices normally perform better in this region due to their bigger drain tab areas.

For pulses above 10 ms, as can be seen from the graph the curves start to plateau and will flatten after 100 ms. This section of the graph is referred to as steady state and is given as thermal resistance parameter $R_{th(j\text{-mb})}$.

From 100 ms onwards the MOSFET will transition into thermal stability and is considered in DC state. In this region the thermal impedance reaches its maximum value and the steady state capabilities of the MOSFETs are given against this maximum value.

Note: the time it takes the MOSFET to reach steady state is not necessarily the same for the PCB where the MOSFET is mounted on as the PCB thermal response is slower. Therefore it is important to use the right thermal impedance for each the PCB and the MOSFET when running thermal analysis for a given condition. RC Cauer models found in Nexperia support page allow for PCB RC network to be added if known.

5.2 Maximum continuous drain current

The maximum current a MOSFET can achieve is primarily derived from the maximum power allowance in the MOSFET. When calculating maximum continuous current, the maximum steady state power must be used.

Example:

Device Name: PSMNR70-40SSH

$T_{mb} = 25 \text{ }^{\circ}\text{C}$

$T_{j(max)} = 175 \text{ }^{\circ}\text{C}$

$R_{th(j-mb)} = (0.4 \text{ K/W max})$

Table 1. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	0.35	0.4	K/W

$$P_{(max)} = \frac{T_{j(max)} - T_{(mb)}}{R_{th(j-mb)}} = \frac{175 - 25}{0.4} = 375 \text{ W} \quad [2]$$

This value for maximum power can be found in data sheet limiting values table:

Table 2. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^{\circ}\text{C}$	-	375	W

Using the power formulae:

$$P = I^2 \times R \quad [3]$$

Where I is the drain current (I_D) and R is the on-state resistance of the MOSFET ($R_{DS(on)}$). I_D can then be calculated as:

$$I_D = \sqrt{\frac{P}{R_{DS(on)}}} \quad [4]$$

The on-state resistance value that must be used to calculate $I_{D(\max)}$, is the MOSFET $R_{DS(on)}$ at T_j max – in this case $R_{DS(on)}$ at $T_j = 175^\circ\text{C}$.

$$I_{D(\max)} = \sqrt{\frac{P_{(\max)}}{R_{DS(on)} @ 175^\circ\text{C}}} \quad [5]$$

A factorisation graph is provided in the data sheet for $R_{DS(on)}$ as a function of junction temperature, (see Figure 5). This can be useful to calculate the current for a specific temperature requirement. For PSMNR70-40SSH the $R_{DS(on)}$ multiplication factor for $T_j = 175^\circ\text{C}$ is 2.19. Note: this graph is based on measured values.

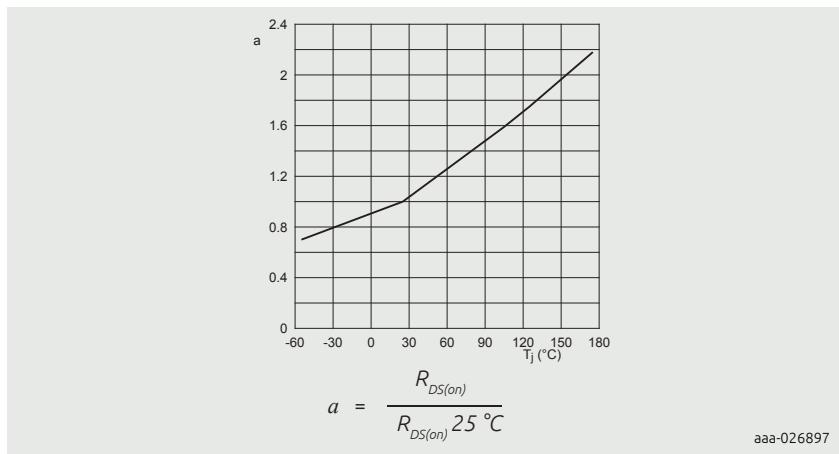


Figure 5 | Normalized drain-source on-state resistance factor as a function of junction temperature

From the data sheet characteristics table,
Max $R_{DS(on)} = 0.7 \text{ m}\Omega$ ($V_{GS} = 10 \text{ V}$, $T_j = 25^\circ\text{C}$):

Table 3. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25^\circ\text{C}$	0.43	0.62	0.7	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175^\circ\text{C}$	0.85	1.23	1.53	$\text{m}\Omega$

The resulting $R_{DS(on)}$ at $V_{GS} = 10 \text{ V}$, $T_j = 175^\circ\text{C} = 1.53 \text{ m}\Omega$, ($2.19 \times 0.7 \text{ m}\Omega$). This value is also included in the data sheet characteristic table. For further details about MOSFET data sheet parameters please refer to application note AN11158 (chapter

1 of this book) - Understanding power MOSFET data sheet parameters..

$$I_{D(max)} = \sqrt{\frac{P}{R_{DS(on)}}} = \sqrt{\frac{375}{0.00153}} = 495 \text{ A} \quad [6]$$

495 A is considered to be the theoretical capability at $T_j = 175^\circ\text{C}$. Another term commonly used is silicon capability.

Once the theoretical maximum I_D is established, the next stage is to validate this value through test and verification. This will allow for other limiting factors to be highlighted and considered in finalising and protecting the $I_{D(max)}$ given in the data sheets.

In the case of PSMN70-40SSH, the validated $I_{D(max)}$ @ $T_{mb} = 25^\circ\text{C}$ is 425 A.

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25^\circ\text{C}$	[1]	0.43	0.62	0.7 mΩ
		$V_{GS} = 10 \text{ V}; T_{mb} = 100^\circ\text{C}$	-	350	A	mΩ

[1] 425A. Continuous current has been successfully demonstrated during application. Practically, the current will be limited by the PCB, thermal design and operating temperature.

The formulae:

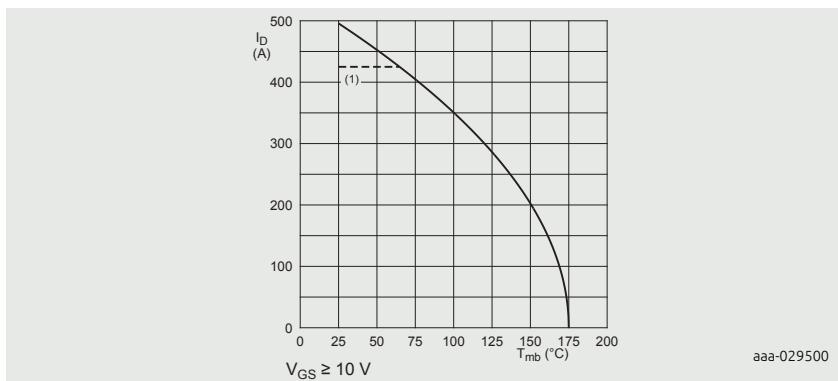
$$I_{D(max)} = \sqrt{\frac{P_{(max)}}{R_{DS(on)} @ 175^\circ\text{C}}}$$

can also be used for different temperatures. For example $I_{D(max)}$ at 100°C can be calculated as follows:

$$P_{(max)} = \frac{T_{j(max)} - T_{(mb)}}{R_{th(j-mb)}} = \frac{175 - 100}{0.4} = 187.5 \text{ W} \quad [7]$$

$$I_{D(max)} = \sqrt{\frac{187.5}{0.00153}} = 350 \text{ A} \quad [8]$$

The same principle applies across the full operating temperature range. MOSFET data sheets contain a drain current de-rating graph in the limiting values section, see Figure 6.



(1) 425 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Figure 6 | Continuous drain current as a function of mounting base temperature

Fig. 6 shows:

- $I_{D(\max)}$ for silicon capability @ 175 °C (solid curve)
- $I_{D(\max)}$ capped value (dashed line)

As stated in Nexperia data sheets the continuous $I_{D(\max)}$ value in the limiting table is not given as a figure verified by design i.e. theoretical, but rather demonstrated through testing. Some of the reasons for capping the continuous $I_{D(\max)}$ value at lower limits than the solid curve given in the graph are as follows:

Package limit

- This is normally associated with wire bond MOSFETs.
- Historically old parts (10 years or older) experienced issues with the package
 - this was due to a combination of:
 1. Wire bond fuse - being a major reason for lowering the current rating
 2. Plastic mould compound.
- This limited $I_{D(\max)}$ to 100 A - 120 A, and this legacy approach had been carried on for some devices even if they were clip bond LFPAK and less than 10 years old.
- As MOSFETs capabilities have reached a much higher level than has been possible in the past, it is only appropriate to select the right plastic compound and adapt a more accurate approach so that these new limits are achieved.
- By making the package not the limiting factor Nexperia MOSFETs can operate to their optimum level, giving the designer full advantage of these capabilities.

Test boards

- Test boards are important part in verifying the $I_{D(\max)}$ capabilities more so at

Nexperia as they may be the limiting factor – as mentioned previously only $I_{D(\max)}$ values that are verified through test are used.

- Improvement have been made in recent years so the right test boards are used to maintain T_{mb} at 25 °C.
 - Note that some MOSFETs vendors state continuous max current as verified by design and some limit the rating to a one second test. Although for R_{th} thermal stability is considered to be reached at one second, (represented by the flat line in Z_{th} graph) and for the MOSFET this is steady state condition. The length of time for max I_D test at Nexperia exceeds 30 seconds continuous.

$T_{j(\max)}$ exceeded

- Junction temperature T_j is monitored during continuous I_D testing. Higher I_D values resulting in T_j exceeding 175 °C are not considered.

Silicon limit

- The silicon capability at 175 °C given in the data sheet as the solid curve is the absolute limit. Meaning only the I_D values that PASS the test at the curve level or below are validated. Instances where MOSFETs I_D measure values above the curve can be explained by the fact that most MOSFETs operate at their typical $R_{DS(on)}$ values while the curve only considers the $R_{DS(on)(\max)}$ values.

Source pins

- Calculations based on the source pins dimensions i.e. length, width, cross-section area, size, etc., as well as the alloy/copper property are used to make sure the current density and capability of the pins meet the I_D rating.

In summary the final maximum continuous I_D rating is based on the lowest limit met by any of the above criteria.

5.3 Maximum continuous source current

Although I_S has always been given as a separate parameter, its value had historically been linked to I_D . The value of I_S was based on calculation and was either lower than I_D or made the same even if it was calculated to be a higher value. A more accurate approach is to rate the current capabilities for both I_D and I_S separately. This approach is now standard and verification through testing in the same way as explained previously is applied.

Determining the I_S limiting value

As far as the maximum power in the MOSFET is concerned, it is the same power allowance whether it is applied through the MOSFET channels (I_D) or the MOSFET body diode (I_S). Therefore the simple power formulae to use is $P = V \times I$, where V is the body diode voltage drop (V_{SD}) and I is the source-drain current I_S . Therefore the power calculated in the previous sections still applies, and in the case of the device example given, $P = 375$ W.

- The power through the MOSFET channel is $P = I^2 \times R$
- Power through the MOSFET body diode is $P = V \times I$, where V is the diode voltage drop (V_{SD}) and I is the source-drain current I_S

The V_{SD} maximum value given in the data sheet characteristics table is 1 V, (see Table 5 below).

Table 5: Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25^\circ\text{C}$	-	0.75	1	V

In theory I_S should be = 375 A, ($I = P/V$, $P = 375$ W, $V = 1$). In reality though V_{SD} is typically around 0.75 V and this would be the case for more than 90% of all devices. Furthermore, V_{SD} is temperature dependant and the voltage will drop as temperature goes up. It is also true to say that the voltage V_{SD} goes up when current increases, but the heating element (induced by the current as self-heating) has a bigger impact.

The continuous source current that has been measured and is validated in the data sheet for PSMNR70-40SSH is 500 A, see Table 6 below.

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Source-drain diode					
I_S	source current	$T_{mb} = 25^\circ\text{C}$	[1]	-	500 A

[1] 500A. Continuous current has been successfully demonstrated during application. Practically, the current will be limited by the PCB, thermal design and operating temperature.

Source-drain characteristic

MOSFET data sheets include a V_{SD} characteristic graph, see Figure 7 below.

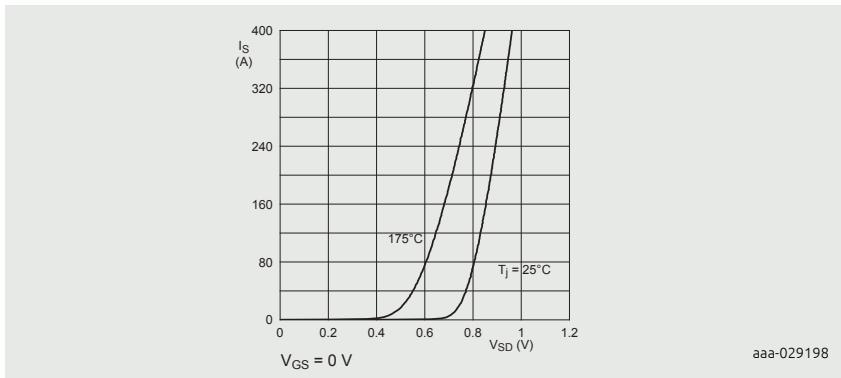


Figure 7 | Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical value

The above graph is obtained by testing the device with pulsed current to avoid self-heating, (which would result in higher values for V_{SD}). In real applications self-heating will most likely occur, as currents lasting more than 100 ms will be sufficient to get R_{th} in steady state region and allow the device to heat up.

To help determine V_{SD} values at higher temperatures Figure 7 includes curves for $T_j = 25^\circ\text{C}$ and for $T_j = 175^\circ\text{C}$. This shows that the V_{SD} value reduces with increased junction temperature. As can be seen from Figure 7 ($T_j = 175^\circ\text{C}$ curve), with $I_S = 400\text{ A}$, V_{SD} is just over 0.8 V and with power = 375 W this will result in $I_S = 440\text{ A}$. The rating for I_S given in data sheet is = 500 A, this difference can be explained by the following: power of 375 W is based on max R_{th} of 0.4 K/W. However, a typical R_{th} is = 0.35 K/W resulting in power = 428 W. With $I_S = 500\text{ A}$, $V_{SD} = 0.85\text{ V}$.

Note: the I_S value given in the data sheet (in this case 500 A) has been proven through testing and the value is validated.

6 Practical application examples

This section details the function and configuration of power MOSFETs in a basic application circuit. Three key application stages will be discussed - RPP (Reverse Polarity Protection), isolation and load drive. Figure 8 below shows a simplified circuit capturing some basic operations of the different MOSFET configurations.

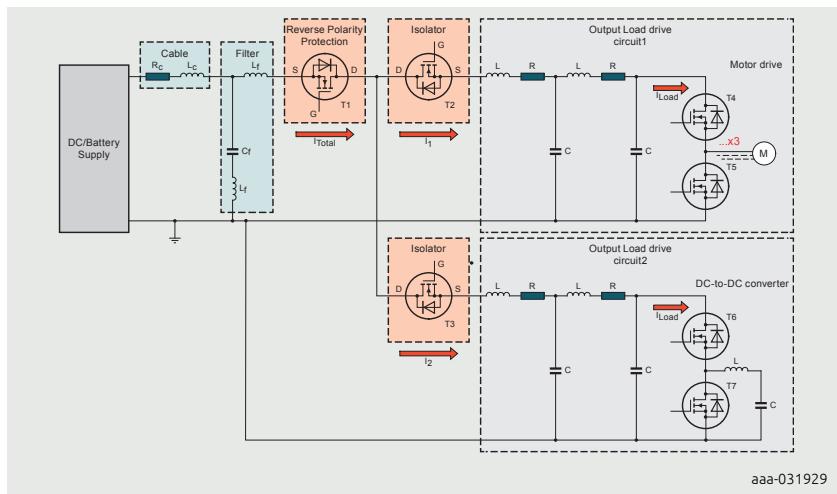


Figure 8 | Simplified motor drive and DC-to-DC converter application diagram

6.1 Output load drive MOSFETs T4, T5, T6 and T7

The circuits shown in Figure 9 and Figure 10 both show a pair of power MOSFETs implemented as a half-bridge, a common configuration for motor drive (T4 and T5 see Figure 9) and DC-to-DC converters (T6 and T7, see Figure 10) – for details on half-bridge MOSFET switching parameters and performance refer to Nexperia application note AN90011 (chapter 7 of this book) - Half-bridge MOSFET switching and its impact on EMC.

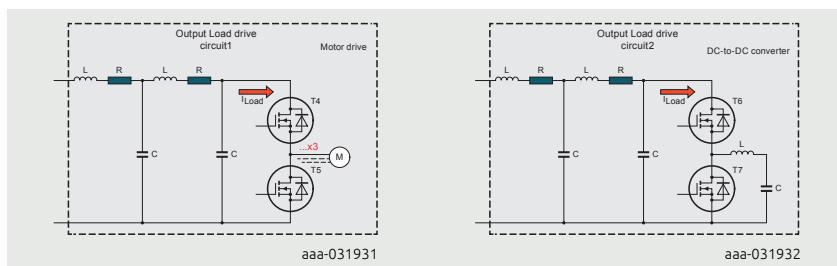


Figure 9 | Output load drive circuit 1 (motor drive)

Figure 10 | Output load drive circuit 2 (DC-to-DC)

In this example we look at output load drive circuit 1, T4 and T5 in relation to current demand which will be gated by the type of motors driven and the power requirement of the application.

Motor drive application

Parameters profiling a motor can be summarised in Figure 11 below:

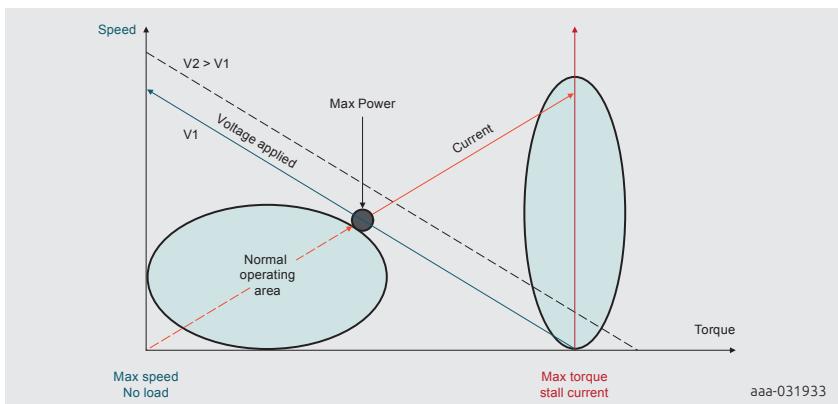


Figure 11 | Motor operation parameters

Normal operating area is where a motor is designed and specified to spend most of its working life. However, it is expected that motors will go through situations of stalled rotation a number of times in their operating life. These stalled motor situations, albeit don't happen on a prolonged periods, are considered part of the a normal operation. Adding to this profile, fault conditions situation such as short circuit where motor drive circuit are expected to recover from, one can appreciate the type of power capabilities that need to be considered in selecting a power MOSFET driving such application. Note: although stall conditions may last few tens or hundreds milliseconds, as explained previously this will be enough to make the MOSFET operate in DC conditions and therefore continuous current capability is key.

6.2 Output isolator MOSFETs T2 and T3

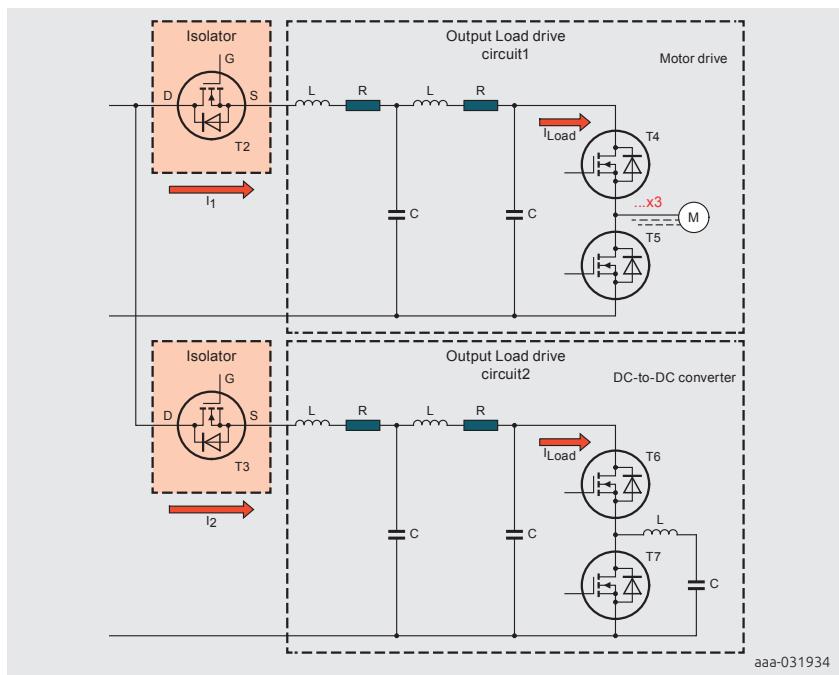


Figure 12 | MOSFETs used as isolators T2 and T3

Some designs may drive two different output loads. A representation of such circuits is given in Figure 12 above. MOSFETs T2 and T3 are used to isolate their respective circuits as they may not need to operate at the same time.

MOSFETs are also used as isolators in designs using the same circuit duplicated to drive one common output. This may be due to redundancy requirement in order to meet a safety standard (usually associated with automotive application to allow continuous operation even in cases of failure – such redundancy circuit is not part of this example here, but the same principle applies).

In such applications particular attention should be given to:

- Current capability in MOSFETs. T2 and T3 need to cater not only for the current needed to drive the loads, but also for the immediate drive circuits current drawn (Figure 12 circuit 1 & circuit 2 respectively).

- Some designs require large capacitors in the drive circuit. The drive circuit itself can be treated as a capacitive load and therefore high inrush current or soft start capabilities are important in the selection of MOSFETs – soft start mode is applied to MOSFET's turn on so that high inrush currents are brought under control and this type of operation requires a MOSFET with strong SOA performance. For SOA related details please see Nexperia application note AN11158 (chapter 1 in this book) - Understanding power MOSFET data sheet parameters.
- Another issue that might result from such large capacitors used in the drive circuits is the current they supply in a case of a fault incident explained as follows: In a case where T3 is off (circuit 2 is disabled) and T2 is ON, if a short circuit occurs in drive circuit 1, charged capacitors from drive circuit 2 can supply very high current to drive circuit 1 through the MOSFET body diode of T3 and through T2 (the same can occur in the opposite direction). In this example it is important to pay attention to I_S capability in a MOSFET

MOSFETs T2 and T3 require strong capabilities in continuous I_D , I_S and depending on implementation of soft start, strong SOA.

6.3 Reverse polarity protection MOSFET T1

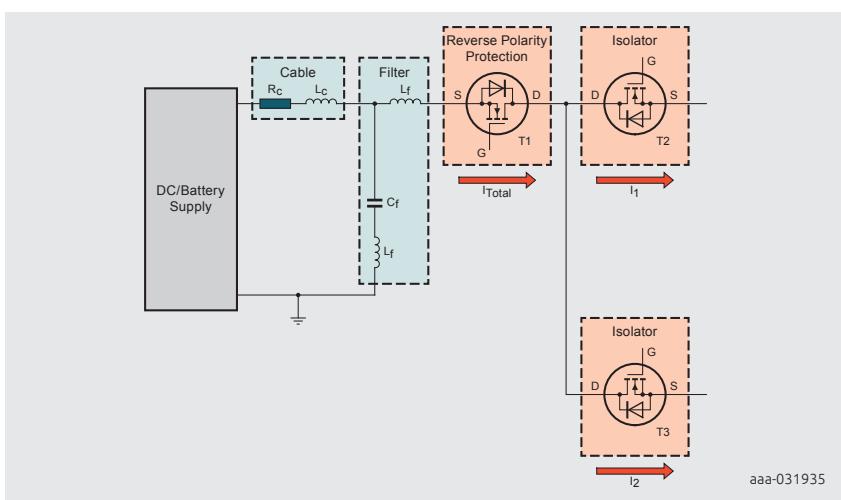


Figure 13 | Reverse polarity protection MOSFET T1

See Figure 13 continuous current capability is of most relevance here as the MOSFET T1 is implemented on the supply line which allows the flow of all the

current needed for the whole module on a continuous basis.

It can also be seen that current flows through T1 from the supply regardless of whether the MOSFET is ON or OFF – when MOSFET is OFF it will still conduct through its body diode. As such it is important to pay attention to I_S capability. To avoid current flowing through MOSFET body diode some designs implement two MOSFETs back to back for reverse polarity protection, see Figure 14.

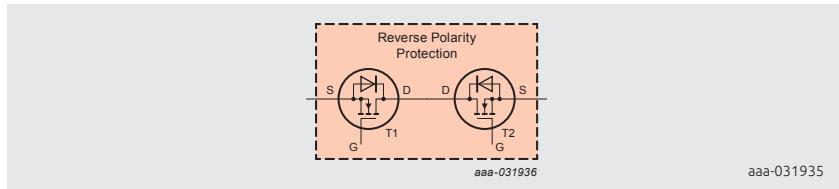


Figure 14 | Reverse polarity protection using back-to-back MOSFETs

In a back-to-back configuration the other parameter that becomes of relevance is the avalanche performance of the MOSFETs. A situation where a fault condition occurs and T2 turns off as part of a protection mechanism. Due to inductances in the cable and/or the circuit a build-up of a voltage at the drain of T2 might occur and potentially lead to an avalanche event. For details on avalanche topic see Nexperia application note AN10273 (chapter 7 of this book) - Half-bridge MOSFET switching and its impact on EMC.

Multiple MOSFET parameters are highlighted in the application examples given above, all showing the importance of, and the need to use a MOSFET that is capable of handling high continuous current.

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1 Introduction

This chapter explains the parameter thermal resistance from junction to ambient and how it can be reduced by careful PCB layout.

Nexperia MOSFET data sheets contain a parameter $R_{th(j-a)}$ which is the thermal resistance from junction to ambient. This is a guide to how much heat can be dissipated from the device to its surroundings in a typical application. For a surface-mounted device such as an LFPACK MOSFET this is highly dependent on the type of Printed Circuit Board (PCB) on which it is mounted. The type of material, the thickness of copper and the shape of the copper footprint all contribute to $R_{th(j-a)}$.

This application note looks at the structure of an LFPACK MOSFET and the way it is mounted on a PCB. It uses thermal modelling techniques to analyse how heat, generated inside the device, is transferred to its surroundings. Various circuit layouts are considered and tested so that developers can use a value for $R_{th(j-a)}$ that closely reflects practical applications.

2 Definition of thermal resistance $R_{th(j-a)}$

$R_{th(j-a)}$ is the thermal resistance from the active surface of the silicon crystal to the surrounding environment. It is a value that represents the net effect of all the possible series and parallel paths from the semiconductor junction to ambient and includes heat transfer by means such as conduction, convection and radiation. $R_{th(j-a)}$ is defined as the temperature difference between junction and ambient that transfers one watt of power to the environment. It is given by:

$$R_{th(j-a)} = \frac{T_j - T_a}{P} \quad [1]$$

where $R_{th(j-a)}$ is measured in K/W T_j is the junction temperature ($^{\circ}$ C)

T_{amb} is the ambient temperature ($^{\circ}$ C)

P is the heating power dissipated inside the MOSFET (W)

2.1 Test method

The method used to measure $R_{th(j-a)}$ is defined by JEDEC standard 51-1 and 51-2A. The approach is a static implementation, meaning heating power is applied on continuous basis while monitoring the junction temperature. The formula for $R_{th(j-a)}$ shown above can be used once a known power is applied and steady state is

reached. The Device Under Test (DUT) is soldered to a FR4 test board and placed in the geometric centre of the test enclosure as shown in Figure 1 and Figure 2. The enclosure comprises a 305 mm cube made from low thermal conductivity materials such as cardboard, polycarbonate, polypropylene, wood, etc.

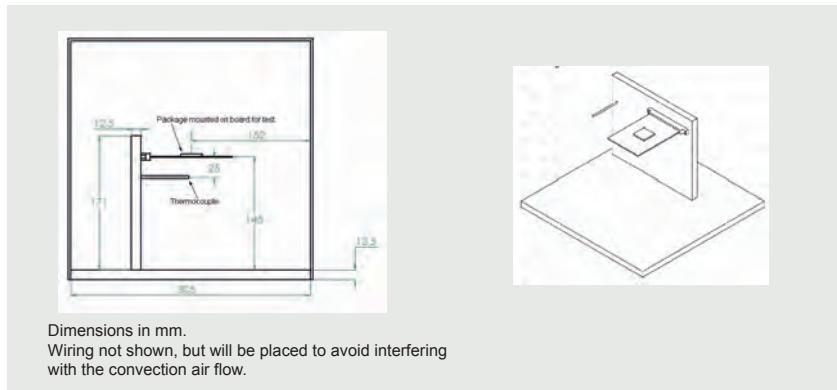


Figure 1 | Side view of the test fixture and enclosure

Figure 2 | Isometric view of the test board and fixture without the enclosure

2.2 Heat transfer in the JEDEC enclosure

Within the JEDEC enclosure, heat is transferred from the DUT to the PCB and surroundings by three basic mechanisms; conduction, convection, and radiation. Conduction is the process by which heat transfers from high temperature regions to low temperature regions that are in contact with each other. Figure 3 shows how heat is transferred from the semiconductor junction to the copper clip and from the clip to the encapsulant. Also, from the junction through the silicon die to the mounting base, and from the mounting base to the PCB.

Convection refers to the heat transfer process caused by displacement of air surrounding the test fixture. The movement is caused by the tendency of hotter and therefore less dense air to rise, and colder, denser air to sink under the influence of gravity, which consequently results in transfer of heat.

Radiation does not depend on contact as heat conduction and convection do. Thermal radiation is when an object loses energy in the form of electromagnetic radiation in the infrared part of the spectrum. In the example shown in Figure 3, heat is radiated from the surfaces of the MOSFET and the PCB into the space inside the box.

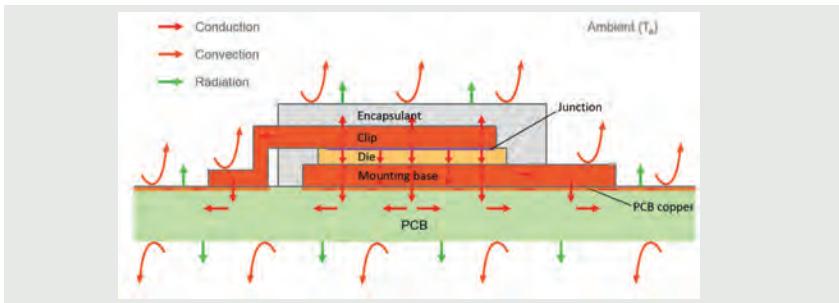


Figure 3 | LFPAK MOSFET - heat transfer model

The measured thermal resistance of a MOSFET, $R_{th(j-a)}$, depends upon the package size, the material properties and the internal structure of the device. It also depends on the PCB that is used in the test fixture. Modern surface-mount MOSFETs are designed to use the PCB as a heat sink and rely on the copper traces to spread the heat over a large area to assist with cooling.

Nexperia power MOSFET data sheets usually specify two values for $R_{th(j-a)}$ – one with a minimum footprint that conforms with the JEDEC standard, and another with a 25.4 mm (1") square of 70 μm thick (2 oz) copper on the top surface. See Table 1 also Figure 4 and Figure 5 below.

Table 1 | Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	0.56	0.63	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Figure 4	-	50	-	K/W
		Figure 5	-	125	-	K/W

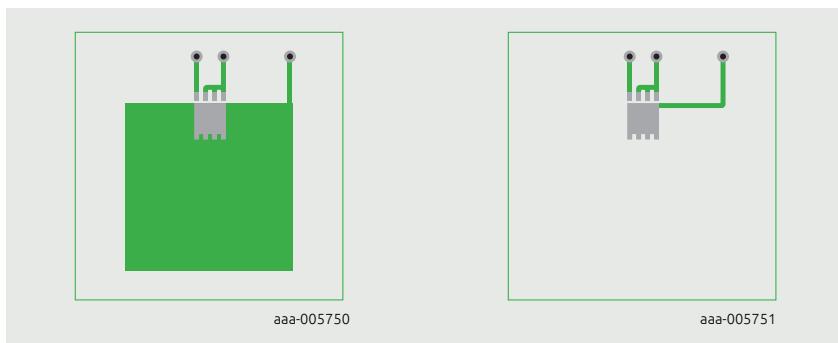


Figure 4 | PCB layout for thermal resistance junction to ambient 1" square pad;
FR4 Board; 2oz copper

Figure 5 | PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

3 MOSFET drain-source current path

Modern power MOSFETs have an on-state resistance in the order of milliohms and surface-mount variants are capable of switching hundreds of amps. In these cases consideration must be given to the Joule heating effect, i.e. induced heat due to current flowing through the conductor, in this case current through the device and the PCB traces.

Figure 6, below, shows the current path through a LFPAK MOSFET. The clip is attached directly to the semiconductor junction and at low current it acts as a heat sink, conducting heat away from the junction to the PCB. At high current, however, it becomes heated by its own resistance and requires cooling by being connected to a cooling surface connected to the source terminal.

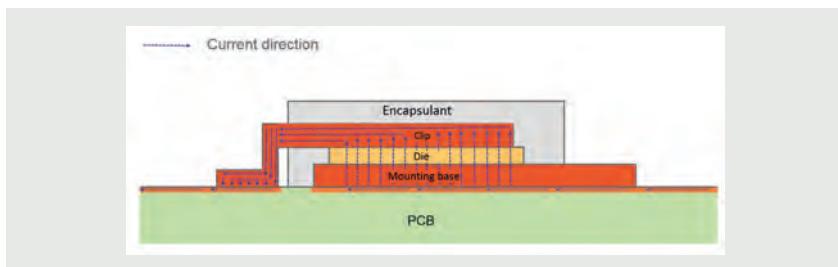


Figure 6 | LFPAK package MOSFET current path

4 PCB layout optimization

4.1 PCB trace width calculation

To examine the heating effect of the PCB trace let us consider as an example a Nexperia LFPACK MOSFET; PSMN1R0-30YLD. This has an on-state resistance $R_{DS(on)} = 1 \text{ m}\Omega$ ($V_{GS} = 10 \text{ V}$; $T_j = 25^\circ\text{C}$).

At a typical current of 55 A, the simplified power dissipation, given by I^2R will be $552 \times 0.001 = 3 \text{ W}$. This power can be dissipated with the appropriate PCB layout applying the right amount of copper to spread the heat.

Many PCB manufacturers websites include a trace width calculation tool based on the IPC-2221 Generic Standard on Printed Board Design. Using an IPC-2221 trace width calculator we can determine the size of trace required to carry 55 A.

Assuming 70 μm (2 oz) thick copper and allowing for manageable 30 $^\circ\text{C}$ rise in the trace temperature, Figure 7 shows that a trace almost 20 mm wide is required.

Printed Circuit Board Width Tool

This Javascript web calculator calculates the trace width for printed circuit board conductors for a given current using formulas from IPC-2221 (formerly IPC-D-275).

Inputs:

Current	55	Amps
Thickness	70	um

Optional Inputs:

Temperature Rise	30	Deg C
Ambient Temperature	25	Deg C
Trace Length	10	mm

Results for Internal Layers:

Required Trace Width	50.4	mm
Resistance	0.0000538	Ohms
Voltage Drop	0.00296	Volts
Power Loss	0.163	Watts

Results for External Layers in Air:

Required Trace Width	19.4	mm
Resistance	0.000140	Ohms
Voltage Drop	0.00769	Volts
Power Loss	0.423	Watts

Figure 7 | Example IPC-2221 trace width calculator

4.2 PCB layout simulations

A number of thermal simulations have been carried out using a PSMN1R0-30YLD as an example to find the optimum PCB layout that extracts the maximum amount of heat from the device and therefore gives the lowest possible value for $R_{th(j-a)}$. All the simulations were on a 25.4 mm square of 70 μm thick copper. The MOSFET was fully turned on with a constant current that produced a 3 W power loss in the device.

The investigation examined different positions of the MOSFET within the copper square. It also considered allocating different percentages of the copper square to the source and drain.

Finally, it examined the heating effect of trace width on the temperature of the MOSFET and the consequences for $R_{th(j-a)}$ measurement.

Test layout 1

In Figure 8 the device is mounted on the edge of a 25.4 mm square copper pad. $R_{th(j-a)} = 41.8 \text{ K/W}$ according to the simulation result.

This layout assumes that the main heat transfer path is from the junction, through the silicon die to the mounting base. All of the copper pad is allocated to cooling the mounting base. We see from the thermal profile that very little heat reaches parts of the copper furthest away from the MOSFET and these contribute little to the cooling. The source trace is very hot because of inefficient cooling of the source pins. This is evidently not an optimum solution resulting in a relatively high value for $R_{th(j-a)}$.

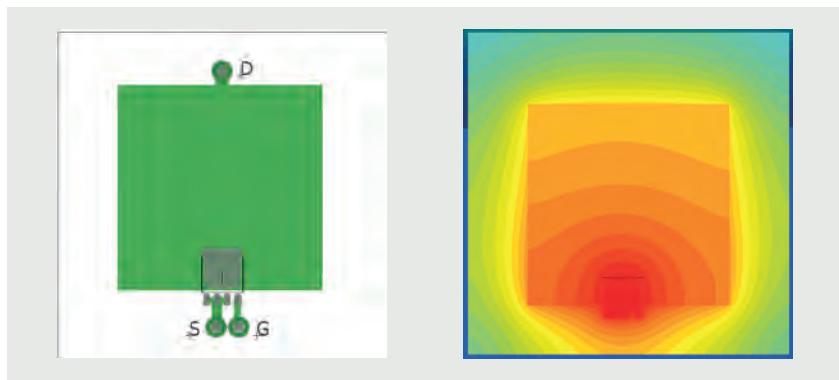


Figure 8 | Test layout 1 and surface temperature profile

Test layout 2

The test layout of Figure 9 shows the MOSFET mounted in the middle of the 25.4 mm copper square with the copper area divided equally between source and drain.

The simulation result gives: $R_{th(j-a)} = 39.1 \text{ K/W}$

Placing the device in the middle of the copper has improved the cooling and reduced the thermal resistance. However, the copper area connected to the drain tab is hotter than that connected to the source pins which suggest that more heat flows through the drain tab. Selecting the proper ratio of source to drain copper is important to obtain the optimum $R_{th(j-a)}$ value.

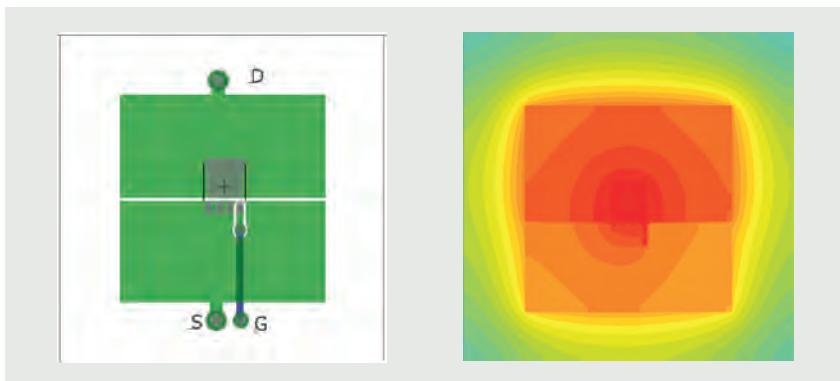


Figure 9 | Test PCB layout 2 and surface temperature profile

Test layouts 3, 4 and 5

In Figure 10, Figure 11 and Figure 12 different layouts examine the effect of various trace widths for the source connection.

Layout 3 has the MOSFET located in the centre of the copper pad and the Joule heating effect of the source trace is not considered.

The simulated result gives: $R_{th(j-a)} = 38.6 \text{ K/W}$.

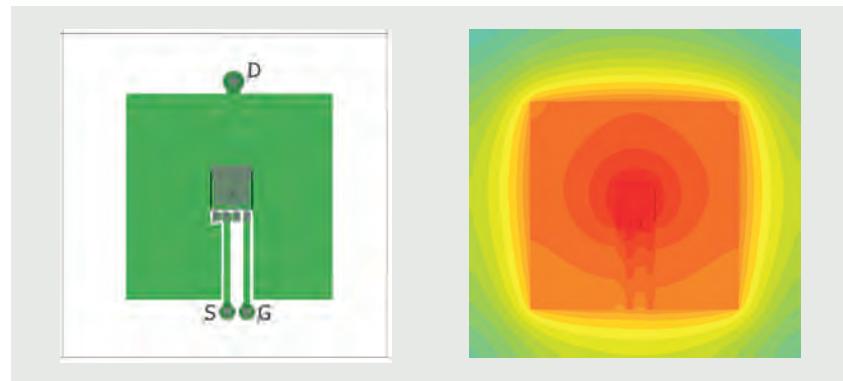


Figure 10 | Test PCB layout 3 and surface temperature profile

However in a practical working circuit when low $R_{DS(on)}$ MOSFETs are fitted, the drain-source current can reach tens or even hundreds of amperes, and the heat generated in the PCB traces cannot be neglected.

Layout 4 shows what happens when the Joule heating of the source trace is taken into account. In this case the trace width is 0.8 mm. The power loss in the MOSFET is 3 W as before, but the power loss in the trace is 8.8 W. Figure 11 shows the rise in temperature of the source trace which is higher than the die temperature of the MOSFET and is therefore heated significantly.

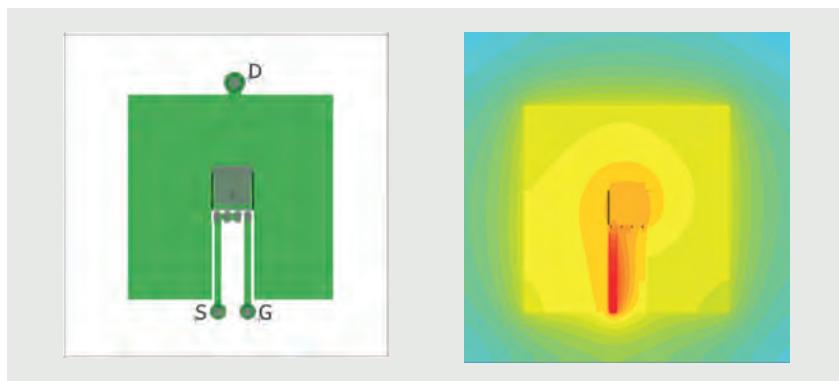


Figure 11 | Test PCB layout 4 and surface temperature profile

Layout 5 has the source trace increased to 3 mm. The test conditions are the same as in layout 4. This time the power loss in the source trace is reduced to 2.4 W but Figure 12 shows that the temperature still exceeds that of the die.

The simulated result gives: $R_{1111} = 56.7 \text{ K/W}$.

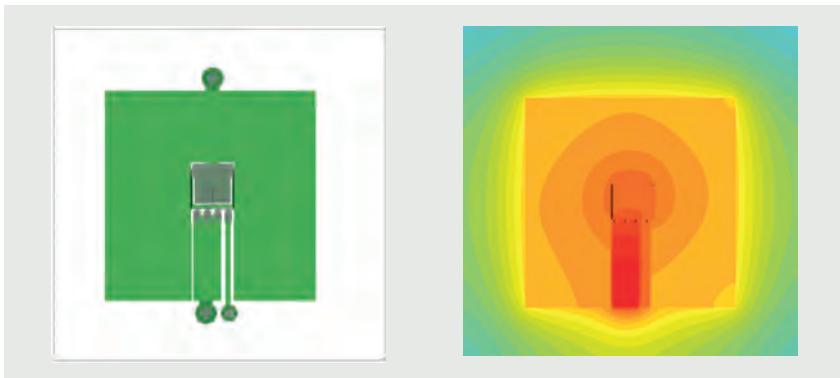


Figure 12 | Test PCB layout 5 and surface temperature profile

We can deduce from test layouts 4 and 5 that in a practical application involving an LFPAK MOSFET careful consideration must be given to trace thickness and width so that the Joule heating of the current path does not contribute to the heating of the MOSFET.

Optimal PCB layout - layout 6

Layout 6, shown in Figure 13, attempts to optimise the copper traces to obtain the lowest possible $R_{th(j-a)}$. Approximately 1/3 of the 25.4 mm copper pad is allocated to the source pins whilst the width of the source trace is a maximum.

The simulation result gives: $R_{th(j-a)} = 37.1 \text{ K/W}$.

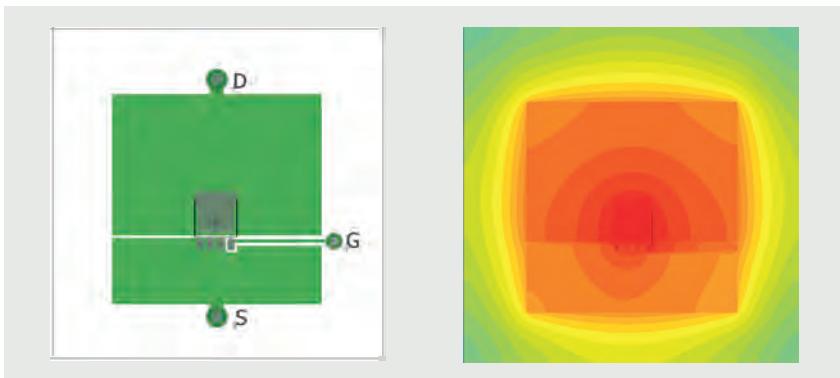


Figure 13 | Test PCB layout 6 and surface temperature profile

5 Conclusion

Nexperia LFPACK MOSFETs are designed to handle high levels of current, 300 A in the case of PSMN1R0-30YLD and in excess of 400 A for packages such as LFPACK88. To take full advantage of the MOSFET's ability to handle these levels of current, designers are faced with the challenge of dissipating the resulting power through the PCB and therefore care must be taken in the design of the layout.

A larger amount of copper and a larger area used under the MOSFET's drain tab will provide better thermal performance and thus better power dissipation. Perhaps less obvious is the PCB layout/ trace for source pins and the importance of the amount/area of copper used. LFPACK packages provide a good thermal path from the junction to the source pins as they use one piece copper-clip (i.e. not two pieces of copper soldered together or copper-ribbon combination). It is therefore very important, for an efficient thermal design to consider a layout with the right amount and area of copper for the source pins.

As shown in this application note the best $R_{th(j-a)}$ can be achieved when this layout approach is applied. Another important factor to consider is the width and thickness necessary for PCB traces providing the electrical connections to the MOSFETs, in order to handle the high currents.



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