

# The 13 most common PCB design mistakes – and how to avoid them

In this document we have created a tool for engineers, designers and anyone else involved in the PCB design or production process, that identifies some common mistakes, the implications these may have on the finished PCB and how to avoid them. At NCAB we work closely with both our customers and our approved PCB factories producing a wide variety of technologies.

We have extensive experience working with designs which need modifications; in fact approximately 30% of the designs we see, need some level of correction. There are many reasons for such mistakes. Whether it's a default in your CAD program which was missed because of a variance, all the way to complex designs which

require the implementation of very specific rules. These are the top most common design mistakes we come across. The ultimate goal of this tool is to provide support in producing high reliability PCBs. As always, you can reach out to NCAB's technical team if there are any questions on this, or anything having to do with your PCB design.

## DESIGN MISTAKES

- 1 Annular ring issues**
- 2 Plated Through Hole (PTH) to Copper**
- 3 Non-plated Through Hole (NPTH) / NPTH slots to copper**
- 4 Holes located on edge of surface mount device (SMD) pad, or very close to SMD**
- 5 Trace width and isolation spacing doesn't work with the selected base copper foil thickness**
- 6 Stubs (unterminated traces) on copper layer**

- 7 Slivers and same net spacing in copper layers**
- 8 Copper to edge – distance between copper features and profile**
- 9 Improper SMD/BGA pads design**
- 10 Soldermask is oversized / lack of oversize in the same design**
- 11 Soldermask bridge / web to small**
- 12 Coverage of soldermask**
- 13 Legend print problems**

## 1 Annular ring issues

This is a mistake where there is not sufficient annular ring to be able to fulfil the requested IPC class of the PCB. The risk is the hole may break through the edge of the annular ring. Think of the ring like a bulls eye in darts. The smaller the annular ring, the more difficult it becomes to hit precisely with the drill. We should also keep in mind that the holes after production will not be drilled in the center of the pads, so larger annular rings are necessary for quality plated holes.

### HOW TO AVOID THIS

In this case, we recommend following the rules in IPC-2221, section 9.1.1 for recommended annular ring both on outer and inner layer, and IPC-2222 section 9.1.3 for inner layer clearances in plane layers. The default design standard shall be Level B where the optimal amount of space exists. Based on the complexity of the PCB, the chart below which we created can provide further guidance. Additionally, adding in teardrops for the pad to track intersection, or allowing your fabricator to add them, can help support a sufficient annular ring.

	GENERAL		MODERATE		ADVANCED	
	IL	OL	IL	OL	IL	OL
<b>ANNULAR RING OF VIAS (ACCEPT 90°BROKEN PER IPC CLASS 2) (mm)</b>						
1/3 oz					0.100	0.100
1/2 oz	0.200	0.200	0.150	0.150	0.100	0.125
1 oz	0.200	0.200	0.150	0.175	0.125	0.150
2 oz	0.250	0.300	0.225	0.250	0.175	0.200
3 oz	0.300	0.400	0.275	0.350	0.225	0.250

FIG 1

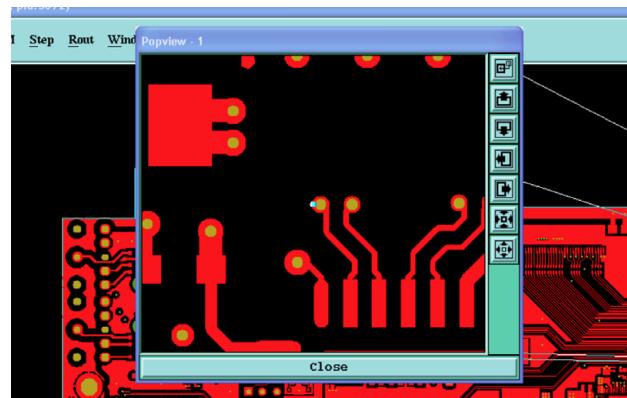


FIG 2 This is an example of holes with very small annular ring on outer layer.

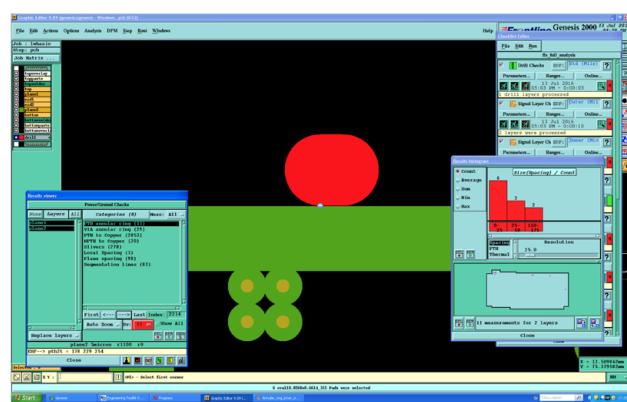


FIG 3 This displays an example of a plated slot without an annular ring in power-ground inner layer. This power-ground layer and after production the copper will be on all the areas where there is black.

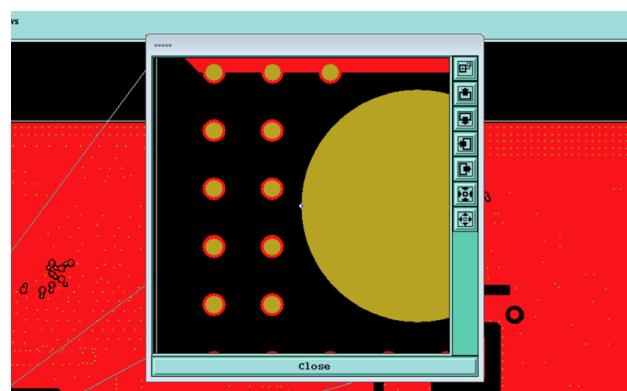


FIG 4 This is an example of a plated hole without an annular ring on outer layer. This example displays that there is nothing to hold the wall in place if there is no annular ring, leading to reliability issues.

## 2 Plated Through Hole (PTH) to Copper

This is an issue where there is not enough distance between the hole peripheral and other copper areas which belong to another electrical net. In the worst-case, this can result in a shorted circuit due to misalignment of inner layer and material movements.

### HOW TO AVOID THIS

In this case we recommend following IPC-2221 & IPC-2222 for clearance to other nets in terms of using the right setting in your CAD program. Based on the complexity of the PCB, we have also developed the chart below for guidance.

	GENERAL		MODERATE		ADVANCED	
	IL	OL	IL	OL	IL	OL
<b>PTH TO COPPER (mm)</b>						
1/3 oz					0.175	0.200
1/2 oz	0.350	0.400	0.250	0.300	0.200	0.225
1 oz	0.350	0.450	0.250	0.350	0.225	0.300
2 oz	0.450	0.600	0.300	0.500	0.250	0.425
3 oz	0.550	0.750	0.400	0.650	0.300	0.525

FIG 5



FIG 6 This image displays an example of PTH to Copper on outer layer.

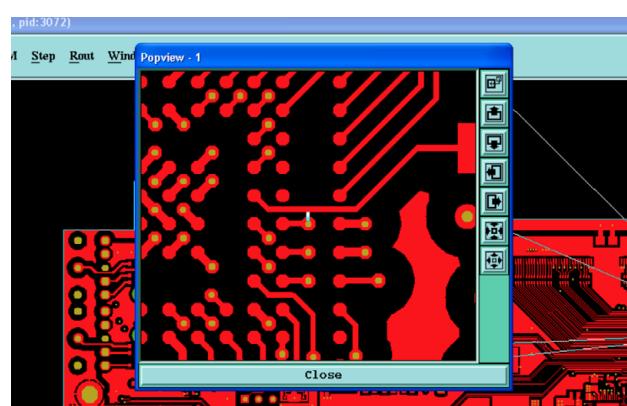


FIG 7 This image displays another example of PTH to Copper on outer layer.

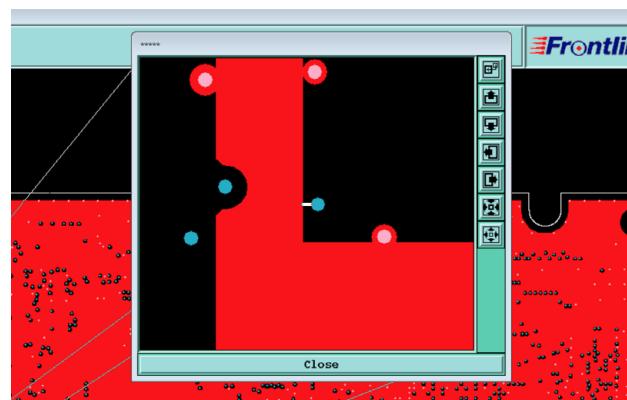


FIG 8 This image displays a very small PTH to copper on the inner layer.

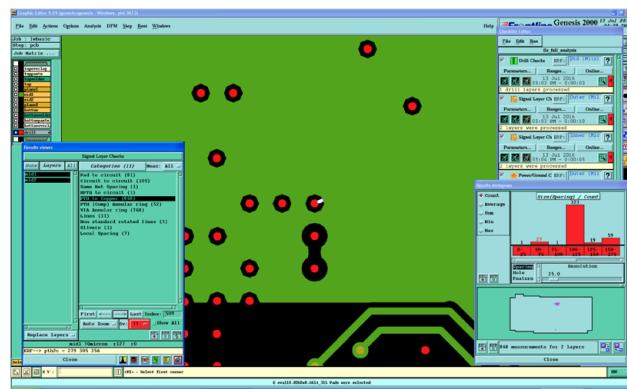


FIG 9 This image is an example of very small PTH to Copper on inner layer. In this case, to address the issue, we simply need to make the opening in the copper larger. Typically when this problem occurs, it is because designers will set up rules in the CAD system once, and then the system will always default to the same copper thickness, when this should be manually changed.

### 3 Non-plated Through Hole (NPTH) / NPTH slots to copper

This is a mistake where there is not enough distance between the hole peripheral and copper features such as lands / traces / planes. If this is not addressed, these holes can be plated instead of non-plated, and the location accuracy may be less than ideal and display evidence of haloing. Or, if drilled during a later step in the production process after plating, will cause worse position tolerances for these holes compares to the PTH.

#### HOW TO AVOID THIS

Based on the complexity of the PCB, in this case we recommend following our Design Guidelines 'Circuitry' section in the image below. When possible the maximum allowable distance from NPTH to copper feature should be allowed to avoid the issue.

	GENERAL		MODERATE		ADVANCED	
	IL	OL	IL	OL	IL	OL
<b>NPTH TO COPPER (mm)</b>						
1/3 oz					0.200	0.200
1/2 oz	0.300	0.300	0.250	0.250	0.200	0.200
1 oz	0.300	0.300	0.250	0.250	0.200	0.225
2 oz	0.400	0.400	0.300	0.300	0.225	0.250
3 oz	0.400	0.400	0.300	0.300	0.250	0.275

FIG 10

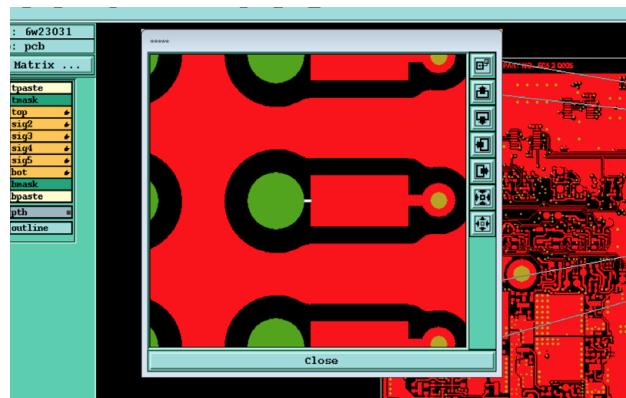


FIG 11 This image displays (NPTH) too close to the SMD pad.

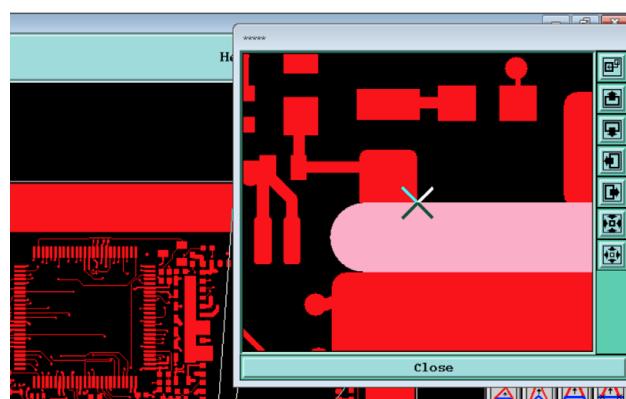


FIG 12 This displays a bad example of a NPTH slot between SMD pad and copper surface. We must have free copper area around the NPTH or slots to avoid the SMD's damage during drilling or routing NPTH or slots.

## 4 Holes located on edge of surface mount device (SMD) pad, or very close to SMD

When a hole is placed too close to a SMD pad, there is always a risk that due to drill registration and soldermask registration that the hole is left partially open which can result in solder paste evacuation during reflow, and a higher risk for contamination, or risk for undefined soldermask to flow up on the SMD area.

### HOW TO AVOID THIS

In this case we recommend to have at least 0.40mm between SMD area and holes in the same net (see illustration below). If the holes for some reason need to be closer than 0.40mm, in your fabrication notes request them to be epoxy plugged according to IPC-4761 type VI-b. If for some reason the holes need to be placed partially or fully inside the SMD area, in your fabrication notes request them to be epoxy plugged and overplated according to IPC-4761 type VII, as illustrated in image below.

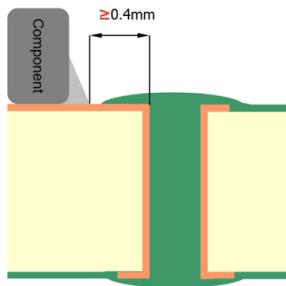


FIG 13

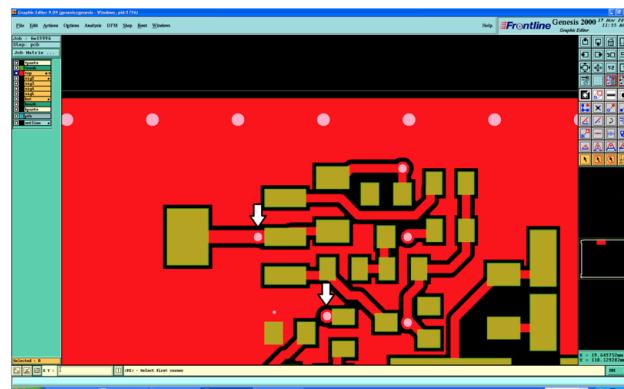


FIG 14 This image displays holes very close to SMD pad.

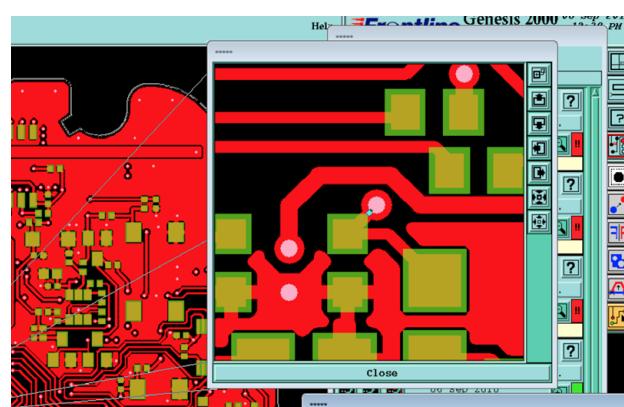


FIG 15 This image is another example of a design where holes are very close to SMD pad.

## 5 Trace width and isolation spacing doesn't work with the selected base copper foil thickness

This is a rather typical problem where the design has no room for applying the correct etch compensation, and therefore we have no opportunity to control either the spacing or the trace width according the rules given by IPC's class. This problem can apply on both outer and inner layers.

### HOW TO AVOID THIS

In this case we recommend following the chart image below from NCAB's design guidelines in the 'Circuitry' section based on selected base foil on both outer- and inner-layers. Please note the minimum track and gap values increase as the copper weight increases. These values are minimums and when possible, features should be kept as far above them as possible to avoid unnecessary difficulty/complexity on the PCB fabricator.

TRACK&GAP (mm)	GENERAL		MODERATE		ADVANCED	
	IL	OL	IL	OL	IL	OL
1/3 oz					0.075 / 0.075	0.075 / 0.075
1/2 oz	0.150 / 0.200	0.150 / 0.200	0.100 / 0.150	0.125 / 0.150	0.075 / 0.075	0.075 / 0.100
1 oz	0.150 / 0.200	0.200 / 0.250	0.125 / 0.150	0.150 / 0.175	0.100 / 0.100	0.125 / 0.150
2 oz	0.200 / 0.250	0.250 / 0.300	0.175 / 0.225	0.200 / 0.250	0.150 / 0.175	0.175 / 0.225
3 oz	0.250 / 0.300	0.300 / 0.350	0.225 / 0.275	0.250 / 0.300	0.200 / 0.250	0.225 / 0.275

FIG 16

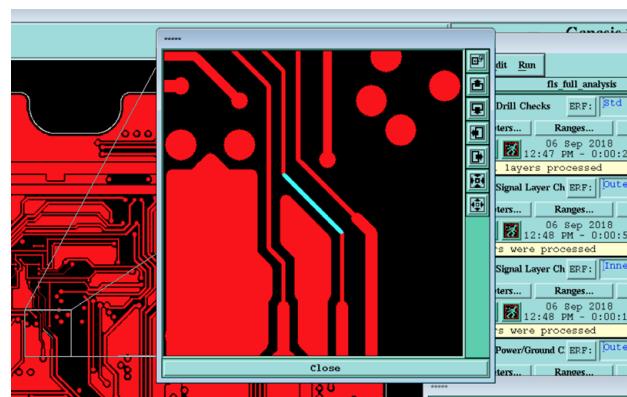


FIG 17 This image is an example of insufficient track width for thicker base copper foil.



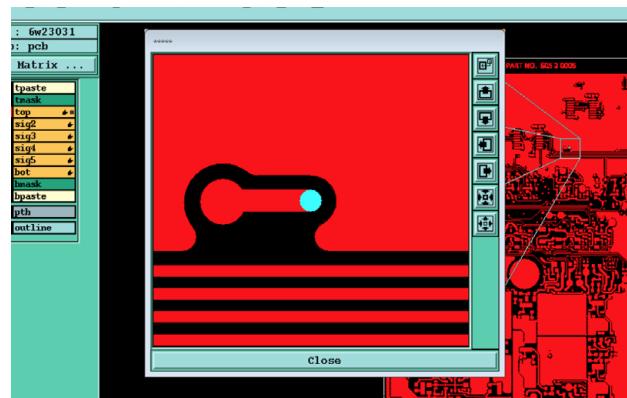
FIG 18 This image displays insufficient space for thicker base copper foil.

## 6 Stubs (unterminated traces) on copper layer

Stubs are defined as an unterminated trace which is connected with a pad on one end, but not on the other end. This always creates engineering questions (EQs). The factory will question this and ask if these stubs are intentional or not. An unintentional stub could be the result of a missing pad or misrouted track where an intentional stub could be intended for use as an antenna.

### HOW TO AVOID THIS

According to our experience, often these unintentional stubs are a result of a redesign from an existing design where the designer has not updated the redesign. A good rule is to always run checks when the designer has completed a redesign and remove these stubs. This will certainly save time in EQ stage. If intentionally present, adding a fabrication note stating 'X aperture track is intentionally left unterminated,' can help avoid confusion or unnecessary questions.



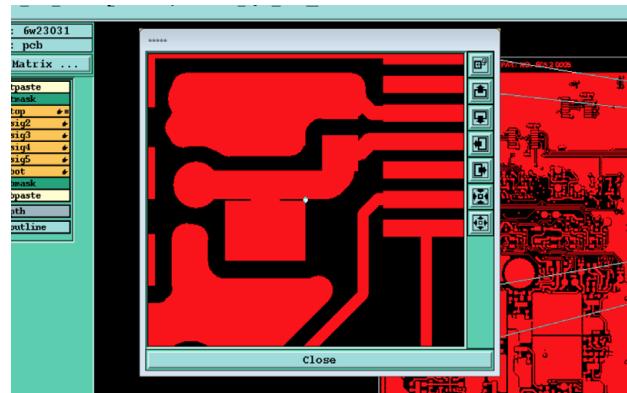
**FIG 19** This image displays stubs in the copper layers.

## 7 Slivers and same net spacing in copper layers

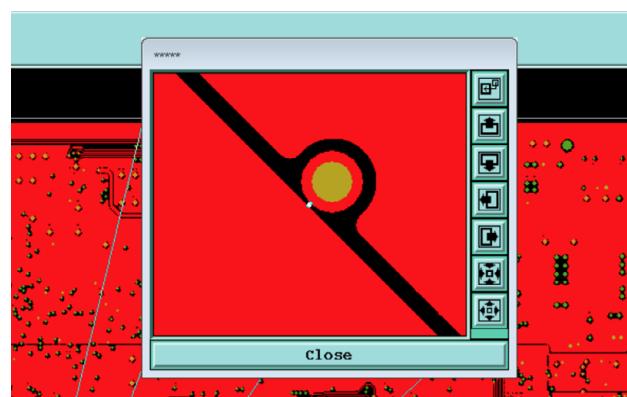
This mistake occurs when the nominal space is not respected when belonging to the same net. These will not be accepted in the production of the PCB since there is a severe risk many small dryfilm slivers will detach from board during etching & plating. This will result in a low production yield with a lot of unwanted shorts / opens.

### HOW TO AVOID THIS

In a good modern CAD program, it is normal to have a parameter setting for this. Often this parameter is missed / ignored. Also, this has sometimes been overlooked since trace routing becomes easier. The minimum isolation must always be respected even if it is the same net.



**FIG 20** This image displays slivers in copper layers.



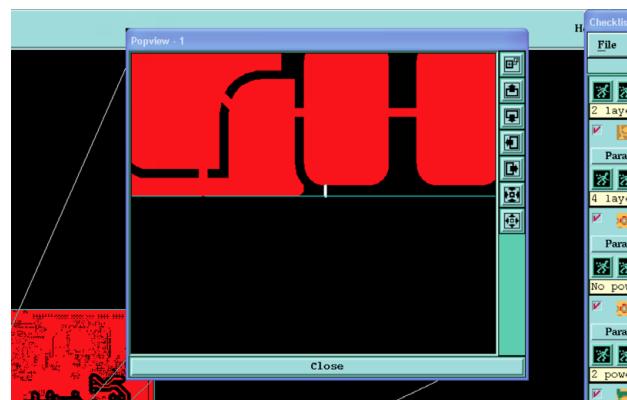
**FIG 21** This image displays same net spacing in copper layers.

## 8 Copper to edge – distance between copper features and profile

This is a mistake where both flooded copper and component pads have very little or no clearance against the edge of the board. Due to both alignment tolerances of copper pattern and also profile tolerance, this can result in nasty burrs and damaged pads when the outline tool cuts into the copper. Since today's laminates are more brittle in nature some haloing can also appear. Additionally we have seen instances when a trace is routed too closely to the board profile which can have the same consequence.

### HOW TO AVOID THIS

In this case we recommend following IPC-2222 section 10.1.1 to have at least 0.40mm + minimum intended spacing between the copper and the profile when selecting routing for profiling. For V-cut it is a good practice to have at least 0.80mm + minimum (1.60mm thick board) intended spacing between the copper and the score line.



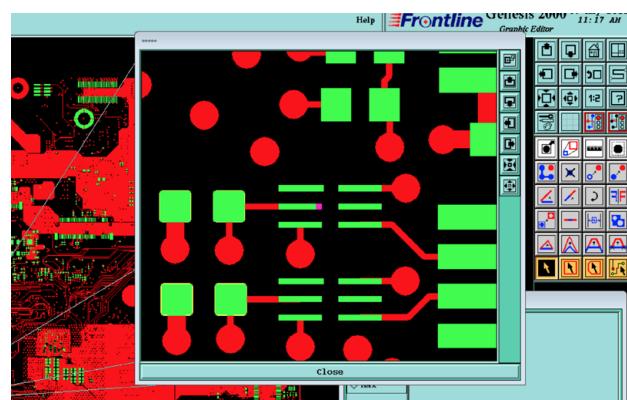
**FIG 22** This image displays an example of rout to copper in copper layers with no clearance to the edge of the board.

## 9 Improper SMD/BGA pads design

In this mistake, rather often we can see pad sizes that are too small so most likely the solder joint quality will be compromised. This can be related to the incorrect pad stack in the customer CAD system component library. Failure to follow the recommended footprints puts unnecessary strain on the assembly house and can result in poor yield of the assembly.

### HOW TO AVOID THIS

In this case, it is best to always check the recommended footprint in the datasheet of the component, and also by double-checking it against the IPC-7351 land pattern calculator same net.



**FIG 23** This image displays thin SMD pads.

## 10 Soldermask is oversized / lack of oversize in the same design

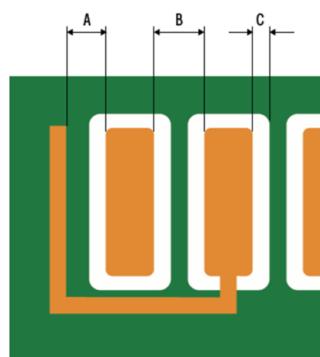
Inconsistencies in soldermask openings are very common. On the same boards there can be a soldermask opening without oversize in combination with a large oversize that it exposes unwanted copper such as other trace, planes etc., without taking into consideration the alignment tolerance in PCB production. This dramatically increases the risk for unwanted shorts during population.

### HOW TO AVOID THIS

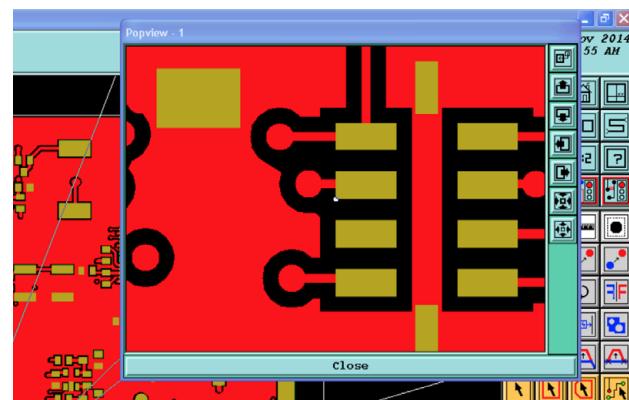
According to the guideline in IPC-2221 section 11.4.3, there are two methods which can be used.

The first method is to provide an oversize in the soldermask of each land. In this case it is vital to have a close dialog with the PCB supplier to understand what tolerances are required (**C** in **image below**). Once understood what tolerances are needed to keep copper out of the way, which are intended to be coved by the soldermask by at least ((2\* tolerances required) + 25 $\mu$ m) (**A** in **image below**).

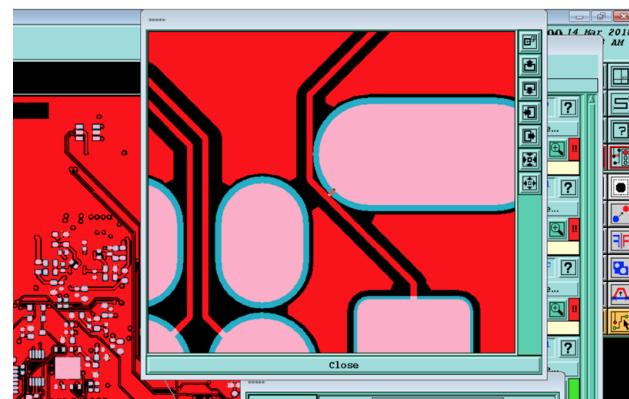
The second method is to provide the openings in the soldermask equal in size as each land, and let the PCB fabricator do the enlargement of the openings. Also in this case it is vital to have a close dialog with your PCB supplier to understand what tolerances are required (**C**). When utilizing this method, maximum clearance value should be specified on the master drawing. In addition, keep copper out of the way at least ((2\* maximum clearance value) + 25 $\mu$ m) (**A**) which is intended to be coved by the soldermask.



**FIG 24** Detailed design capabilities can be found in our “NCAB\_Design\_Guidelines\_1.0” and the section “Soldermask / Via hole plugging.” Please note that these tolerances are only applicable on green soldermask and copper thickness  $\leq$  35 $\mu$ m. If other colors / copper weights are desired or required, please contact your local NCAB technical team.



**FIG 25** This image displays Soldermask with no oversize against pads.



**FIG 26** This image displays a soldermask opening too large, exposing unwanted areas.

## 11 Soldermask bridge / web to small

This mistake displays soldermask bridges which are too small to produce. During application of the soldermask some undercut normally occurs, and when the anchor point between the soldermask and the laminate becomes too small, the soldermask bridge will either break or detach from the laminate. See illustration below.

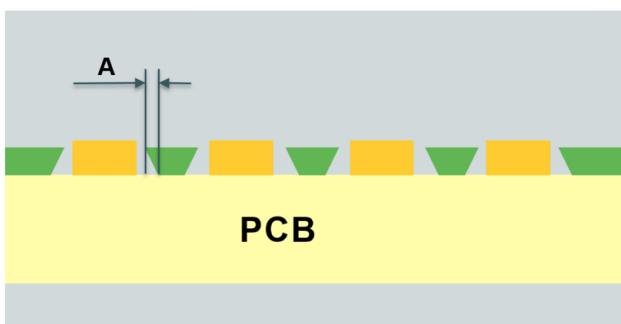


FIG 27

### HOW TO AVOID THIS

A general rule is to follow 0.10mm for the minimum soldermask bridge / web on PCB with normal green color and also standard copper weights. If designing boards with different color, or higher copper weights, be sure have a close dialog with your PCB supplier to understand what guidance to follow, as the minimum achievable soldermask web per color can vary greatly from fabricator to fabricator.

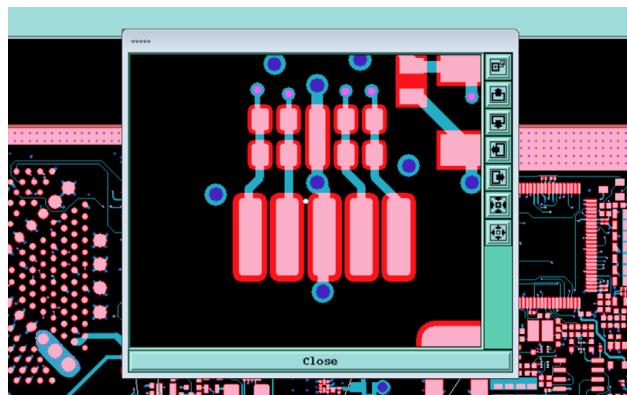


FIG 28 This image displays a design with small solder web in solder mask.

## 12 Coverage of soldermask

In this mistake, the coverage area is too small to secure, that unwanted areas will be exposed due to normal alignment tolerance in the soldermask process. This highly increases the risk of shorts in the PCB assembly process.

### HOW TO AVOID THIS

In this case we recommend having a close dialog with your PCB supplier to understand what tolerances are required for the soldermask alignment. The copper should be kept away from the areas which are intended to be coved by the soldermask by at least  $((2 * \text{maximum tolerance}) + 25\mu\text{m})$  (**A**), to secure that copper intended to be cover by soldermask is not exposed.

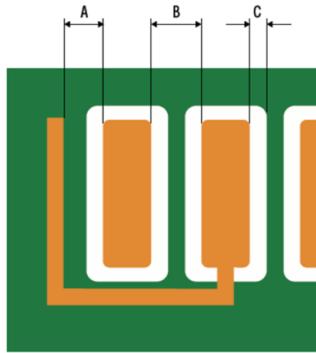
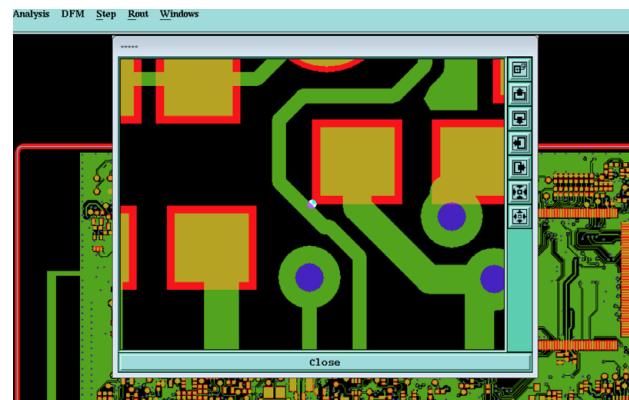
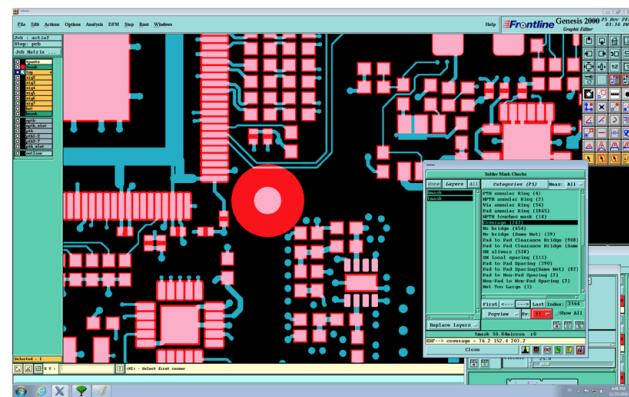


FIG 29



**FIG 30** This image displays coverage which is compromised by soldermask coverage.



**FIG 31** This image displays openings in soldermask for fiducial, or aiming point, are too large.

## 13 Legend print problems

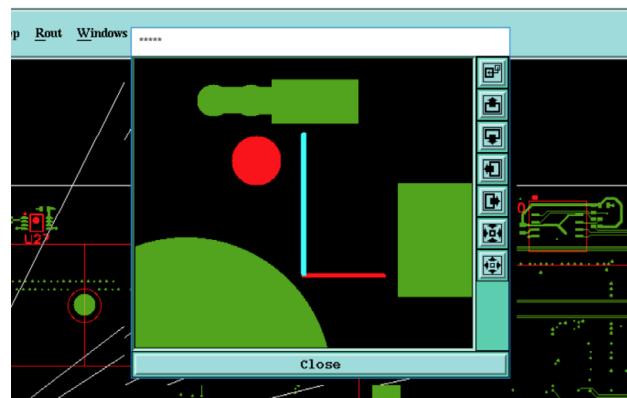
We see several mistakes with legend prints including:

- Legend print on coppers areas intended for soldering
- Line width of text too small to be screen printed
- Text height too small be screen printed

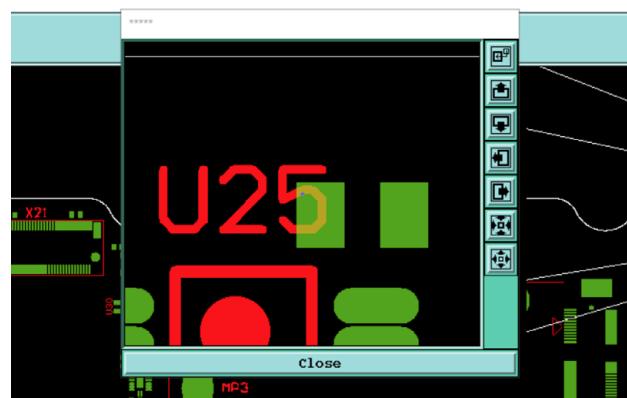
### HOW TO AVOID THIS

We recommend following these rules:

- Minimum line width text of 0.15mm, recommended 0.20
- Minimum text height of 1.00mm
- Minimum distance between text and areas intended for soldering.
- Add fabrication notes allowing your supplier to clip the silkscreen from any copper features pending legibility is maintained.



**FIG 32** This image displays the legend text too small.



**FIG 33** This image displays the legend text on pads, which will not be printed properly.