

# THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...<sup>TM</sup>

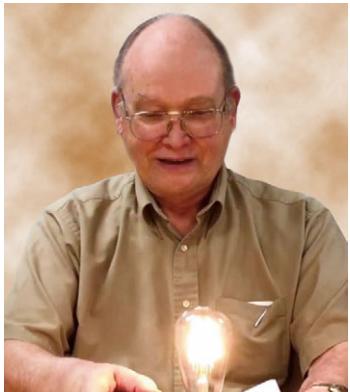
## Fundamentals of RF/Microwave PCBs



**John Bushie and Anaya Vardya**  
American Standard Circuits

# PEER REVIEWER

*This book has been reviewed for technical accuracy by the following expert from the PCB industry.*



**Happy Holden**

Consulting Technical Editor, I-Connect007

Happy Holden is the retired director of electronics and innovations for Gentex Corporation. Happy is the former chief technical officer for the world's largest PCB fabricator, Hon Hai Precision Industries (Foxconn). Prior to Foxconn, Happy was the senior PCB technologist for Mentor Graphics and the advanced technology manager at Nan Ya/Westwood Associates and Merix. Happy previously worked at Hewlett-Packard for over 28 years as director of PCB R&D and manufacturing engineering manager. He has been involved in advanced PCB technologies for over 47 years.

# MEET THE AUTHORS



**John Bushie**

Director of Technology at American Standard Circuits

John has over 20 years of experience in the PCB industry supplying and supporting the manufacture of PCBs as well as high-frequency RF/microwave circuit board laminates. He has provided product and design support to PCB and system designers throughout North America, Europe, and Asia. His extensive background in problem solving and process engineering has allowed him to support many customers through detailed and focused application engineering. It is this close relationship with customers that drives his passion for new product design and design for manufacturability.



**Anaya Vardya**

President and CEO of American Standard Circuits

Anaya has over 33 years of experience in electronics manufacturing, including in the United States, Canada, and the Far East. He also has over a decade of executive management experience in public companies manufacturing PWBs. One of Anaya's peers, Brad Hammack of Dell EMC, described him as "...one of the most driven engineering managers I have ever worked with. He has a keen eye for details and also sees the big picture." He has an extensive understanding of

virtually every aspect of PCB manufacturing operations, such as supply chain management and quality control. Anaya not only serves as ASC's CEO, but also as an expert ready to assist you with any questions you may have.

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## **Fundamentals of RF/Microwave PCBs**

**John Bushie and Anaya Vardya**

American Standard Circuits

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Creative Innovations In Flex, Digital & Microwave Circuits

# The Printed Circuit Designer's Guide to...™

## Fundamentals of RF/Microwave PCBs

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## INTRODUCTION

We conceived, developed, and published this guidebook in an effort to educate the radio frequency RF/microwave PCB designer from a PCB fabricator's perspective, based on the many conversations we have had with designers over the years. This book is fundamentally about providing the knowledge needed to understand the unique challenges RF PCBs present, and the importance of early engagement between the original design manufacturer (ODM) and the PCB fabricator.

In our experience with PCB designers and RF engineers throughout the years, the most frequently asked question is, "What is the correct material to use for this particular project?" While certainly an important question, it has an extremely broad impact on the final design, and is actually only a portion of the puzzle facing the designer, and ultimately the end-users of the product. This is because the material choice will play a large part in determining the following factors: cost, thickness, weight, rigidity, mounting possibilities, connector types, circuit layout, cutouts, and edge features. In fact, it will determine a large portion of the function of the particular item, and these are only a few of the design aspects affected by the choice of material.

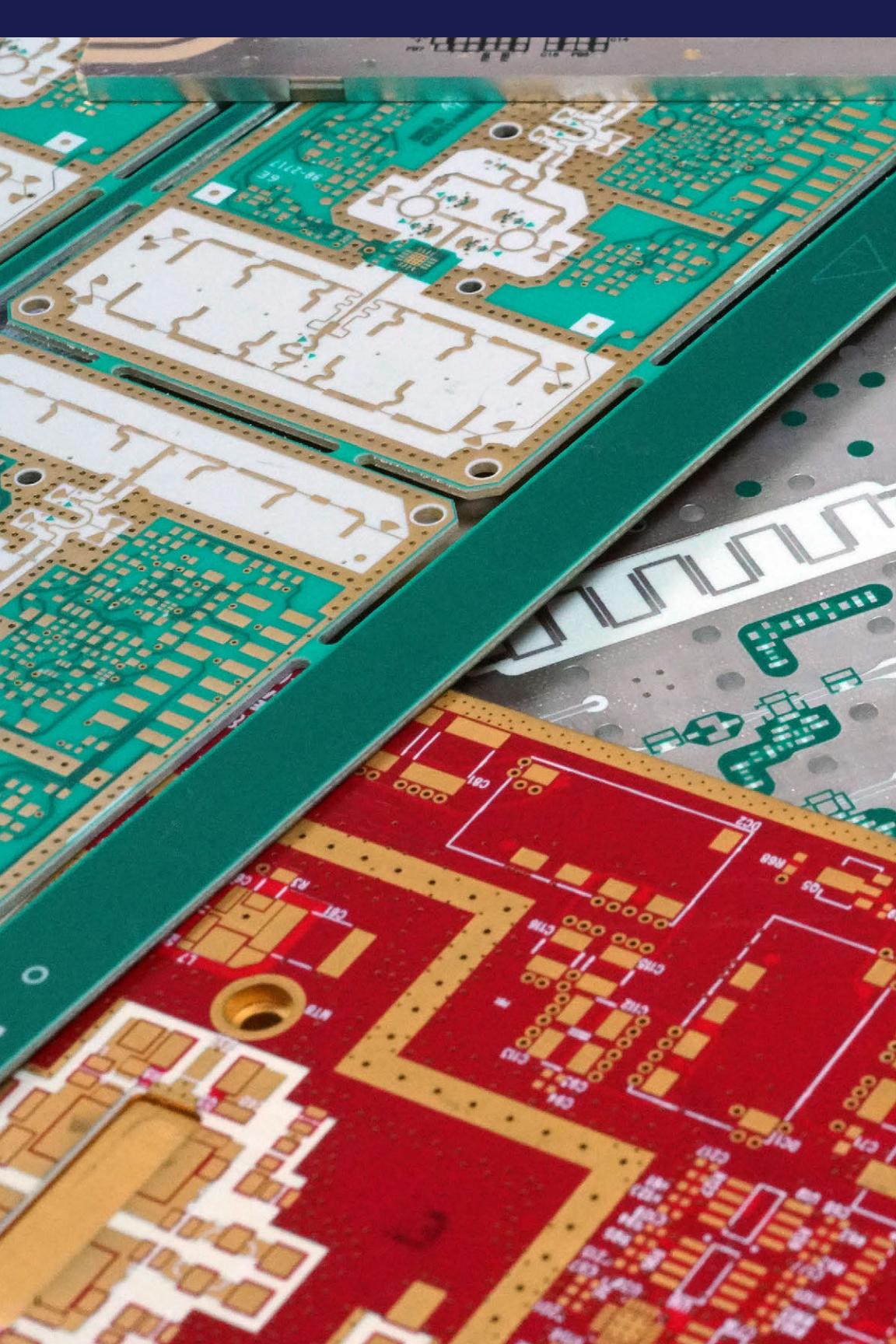
The question we wish was most often asked is, "What can we do at the design stage to make our product more manufacturable?" The impact of not asking this question can be even more important than material selection. The disconnect between what the ODM wants and what the printed circuit fabricator can produce is the biggest reason for an unsuccessful build of a new PCB design.

We have focused this book on answering these two questions as they relate to RF/microwave technology. RF and microwave designs present some of the most challenging technologies in PCB manufacturing, where the impact of poor material choices and design considerations are extremely costly to both the ODM and the PCB fabricator.

Printed circuit boards are the backbone of RF technology, and they are big business. Demand for RF and microwave modules are on an incredible trajectory—a multibillion-dollar market. RF technology touches everybody. In today's 24/7/365 connected world, RF powers our wireless networks, cell phones, smart TVs, and tablets. We can even check what's in our refrigerator from the grocery store and adjust the lights and temperature in our homes while on vacation courtesy of RF technology! RF is how the world works today. It drives satellite communication systems, broadband access, and optical data networks. In addition, an increasing number of automotive, industrial, military, homeland security, scientific, and medical applications are using RF technology to perform detection, measurement, and imaging functions.

The absolute, fundamental key to success in RF applications is early engagement between the ODM and the PCB fabricator. This early engagement will save time, headaches, and money. Understanding the current state-of-the-art in PCB manufacturing technology and capabilities is critical to the success of any RF project. Collaboration between the designer and PCB experts will ensure not only manufacturability, but also functionality.

While nothing can replace direct early design collaboration, the intent of this book is to answer the opening two questions by providing a reference guide for ODMs on some of the most important factors that need to be considered during the design process to maximize success. We hope you find this effort valuable.



# CHAPTER 1

## Material Selection

When discussing the right choice for materials to use in designs, today's engineers are much more knowledgeable than they were during the early years of RF PCB technology. At that time, there were only a couple flavors of low-loss Teflon materials, and most of them contained the word *Duroid*. Today, there are literally dozens of controlled-Dk and low-loss materials available on the market, many of which contain proprietary resin systems that allow the PCB fabricator to manufacture them using similar processes to standard FR-4 materials.

That being said, there is no particular material that is more effective across the board for every application, or even more cost effective than another. There will always be a cost-benefit component to these choices based on performance and functional requirements. As with most things, total cost must be the guide. The initial material cost may be higher than other alternatives, but if the net result is a product that meets design specifications, then it still may be considered the right material (Figure 1.1).

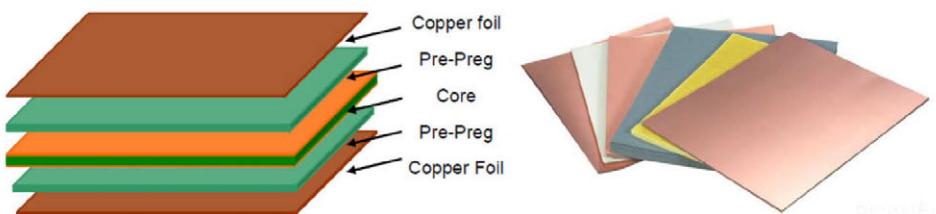


Figure 1.1: Exploded view of typical PCB materials.

Designers of digital logic and RF/microwave products have very different needs, which result in different material requirements. Typically, digital designers are more interested in circuit speed and density. Accordingly, they are primarily interested in thin materials and specific dielectric constants because permittivity is a major concern in the digital world. RF and microwave designers, however, are more interested in frequency-based issues. They need materials that help them minimize energy loss and that provide dielectric uniformity. They also require tight control over material thickness and electrical properties, and are especially concerned with factors such as loss tangent and dielectric constant stability throughout a range of operating conditions.

## **Two Key Parameters**

RF and microwave circuits usually process precision and/or low-level signal transmissions. This means that these circuits require much tighter control of parameters pertaining to signal losses. The two greatest concerns are losses caused by signal reflections due to impedance mismatch, and the loss of signal energy into the dielectric of the material. Material choice (laminates and copper) can have a major impact on all these sources of energy loss. As a result, materials geared to the RF arena tightly control the two key parameters of loss tangent and dielectric constant.

### **Parameter 1: Loss Tangent**

The primary consideration here is how much loss the particular design can tolerate, or in other words, how much power in versus how much power out. With an infinite supply of power, loss is unimportant. Adjustments can always be made to compensate for the loss of the materials or conductors. The exception to this is in the heat generated by conductor and return losses, but fortunately this is seldom a reality.

### **Parameter 2: Dielectric Constant**

The primary consideration here is the required dielectric material thickness and conductor width to achieve a given impedance value. This turns into a copper loss and power handling issue. The secondary issue is the ability to dissipate the heat that occurs both at the power devices and in the conductors. This needs to be transmitted somewhere, and the materials need to be of a low enough dielectric constant or have thick enough conductor widths to carry whatever power the circuitry requires. A careful consideration of these two parameters will provide guidance to the proper material type and thickness required for the PCB being designed.

## **Dimensional Stability**

An understanding of how materials react under operating conditions—dimensional stability—is also important when making selections for a RF PCB. There are three types of materials related to dimensional stability:

1. **Homogeneous:** Material of uniform composition throughout that cannot be mechanically separated into different materials such as plastic, glass, and/or resin.
2. **Isotropic:** Material with properties that are equal in all directions (X, Y, and Z), such as glass microfiber RT/duroid®.
3. **Anisotropic:** Material with properties that might vary depending on direction, such as woven glass fabric in traditional FR-4 and certain glass fabric-reinforced PTFE materials.

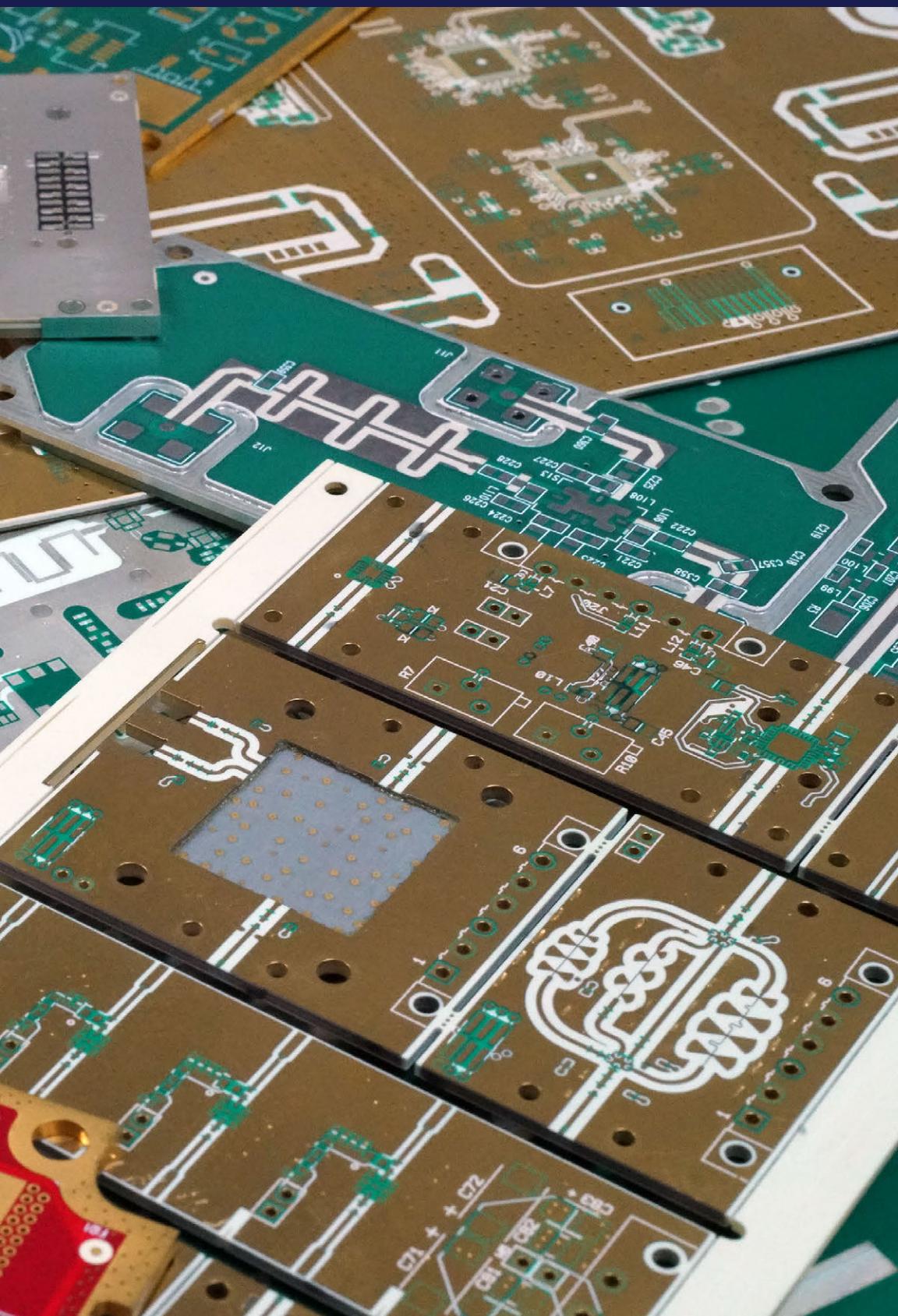


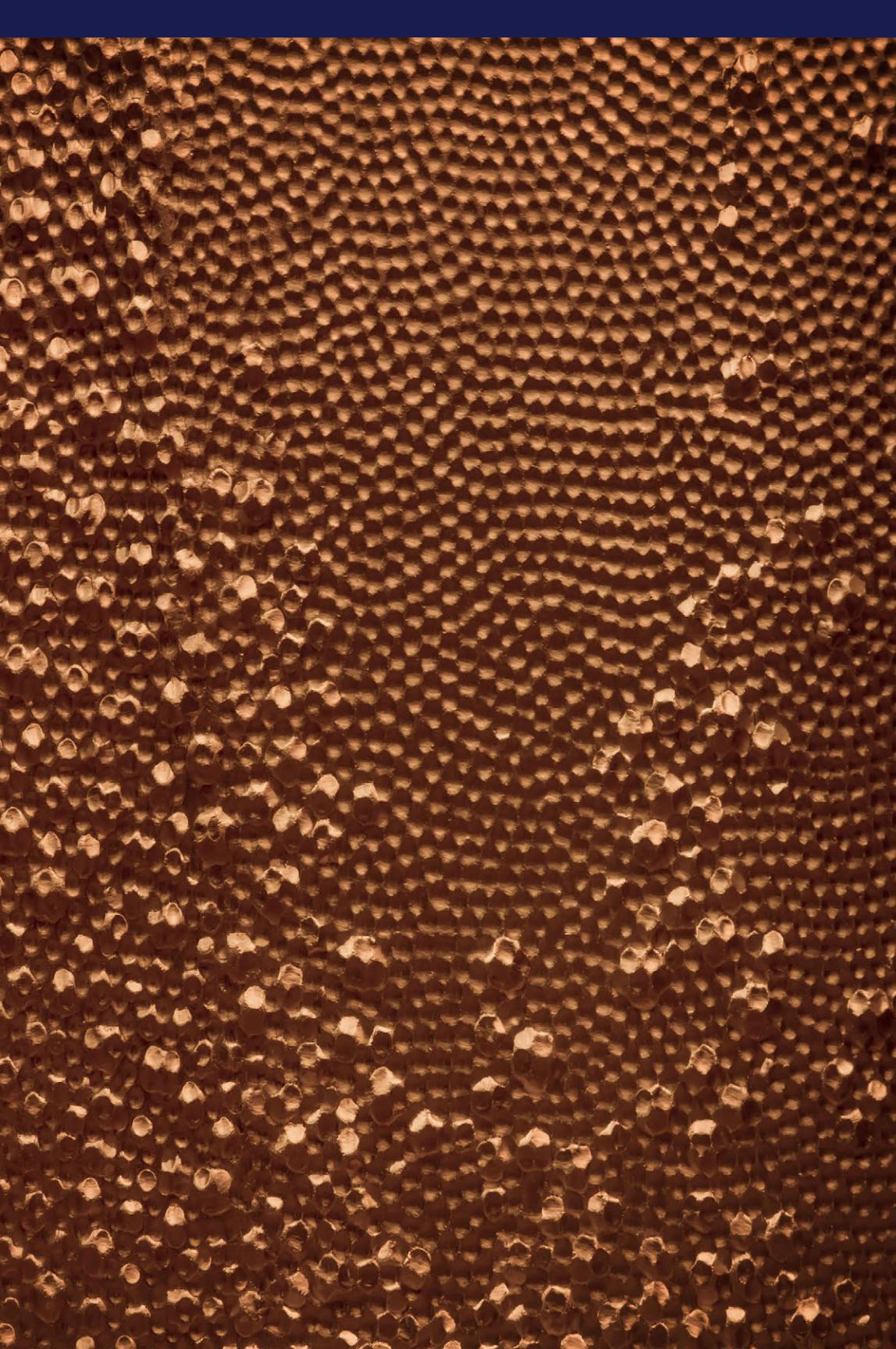
## **Best Practices for Material Selection**

There are several best practices that will help a designer choose the right laminate substrate and copper foil for high-frequency RF applications.

- **Match Dielectric Constants:** In RF PCB design, a dielectric constant (Dk) match is highly desired. If a PCB substrate is made of resin and woven material, they may have different Dks. Non-uniform Dks in a substrate may cause problems. Working with the PCB fabricator will ensure as close a Dk match as possible in all of the substrates being considered.
- **Match Coefficient of Thermal Expansion (CTE):** The degree of expansion in response to temperature increase is important on its own, but it can also impact the function of the PCB. Differing CTEs of the laminate substrate layers in a PCB will expand at different rates during fabrication or operation, and thus create functional failures and reliability concerns.
- **Tight Substrate Weave:** The woven properties of the laminate substrate need to mesh tightly, and may directly impact Dk. Working with the PCB fabricator will help avoid choosing a material set that may negatively impact performance.
- **FR-4:** It must be understood that if FR-4 is used for high-frequency applications, it will not have the same level of precise dielectric constant and thickness control as specially-formulated RF material.
- **Smooth Foil:** Referencing the previously discussed skin effect, a smooth copper foil will ensure lower resistive losses at extremely high frequencies.

Our two material selection guides can be found in the appendices. As you review this guide, remember that a number of suppliers may have similar materials, but price points and lead times may vary. If you are open to trying different options, a good idea is to work with your PCB fabricator who can educate you on these aspects. We have also worked with customers who require parallel builds with multiple materials in the early stages of honing their designs.





## CHAPTER 2

# Copper Surface Roughness

We often discuss circuit design in terms of loss: loss in the conductor related to circuit geometry, conductivity of the metal itself in terms of resistance, and the losses caused by the dielectric material on which the circuit is placed or insulated. However, as RF technology has continued to develop and push manufacturing limits, another factor has proven to have a critical impact on conductor loss: copper surface roughness.

Aside from the raw copper roughness, it is critical for RF designers to also factor in the impact copper treatments used by the fabricator will have on RF performance. The trend is to move away from traditional copper treatments, like oxide, to increase the surface area, and instead choose pure copper for a smoother surface. There are tradeoffs to be considered between adhesion and RF performance. Therefore, working with the PCB fabricator is critical because there are alternative processes available, such as using an acid wash and/or coupling agents.

### Surface Copper Foil

In high-frequency signals, the current in the PCB copper circuit is concentrated within a small depth near its surface, which is referred to as the “skin effect” or “skin depth.” Skin depth is a measure of how (and where) electrical conduction takes place in a conductor, and is a function of frequency (Figure 2.1).

One common misconception about skin depth is about which surface of a conductor is carrying the RF current. The lay person assumes it is on the top surface of the base material copper foil, but in most cases, the opposite is true. Circuit conduction occurs at the surface nearest the dielectric from

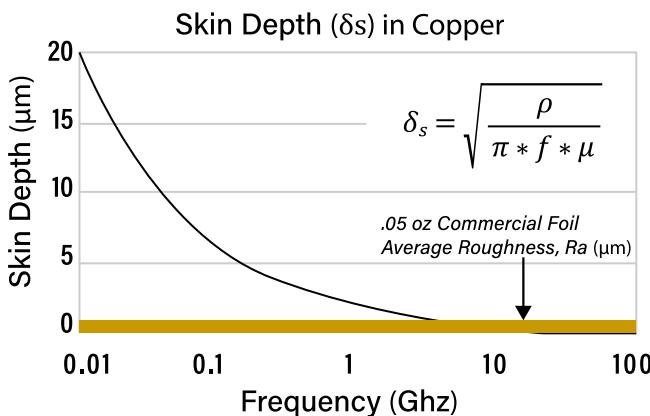


Figure 2.1: Skin depth calculation. (Source: Isola)

which the EM wave propagates: in other words, the bottom copper surface that is against the laminate in a microstrip design.

Figure 2.2 illustrates this in a cross-section of a high-frequency signal. As you can see, the RF currents are highest in the lower surface (against the laminate) of the circuit. This is why the first metal (copper foil) is the most important to conductivity in a high-frequency multi-metal stackup. This means that the roughness of surface copper is extremely important to signal integrity and performance. There are two types of commercial copper foils typically used with the raw laminate copper foil for PCBs: electrodeposited (ED) and rolled annealed (RA) copper.

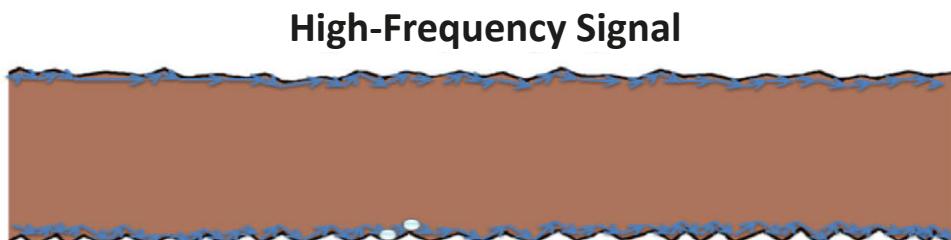


Figure 2.2: High-frequency current conductivity. (Source: Isola)

## Electrodeposited (ED) Copper Foil

ED copper is formed by electrolytic deposition onto a slowly rotating polished drum from a copper-sulfate solution. When an electric field is applied, copper is deposited on the drum as it rotates at a very slow pace; the slower the pace, the thicker the copper. The side against the drum provides the smoother finish (Figure 2.3).

There are also different classifications of ED copper that all relate to the profile, or roughness, of the copper surface. There is a tradeoff between adhesion and conductor loss; higher profiles increase adhesion at the expense of conductor loss, and vice versa. To minimize high-frequency conductor loss, the lower the profile, the better. We will discuss a few options here.

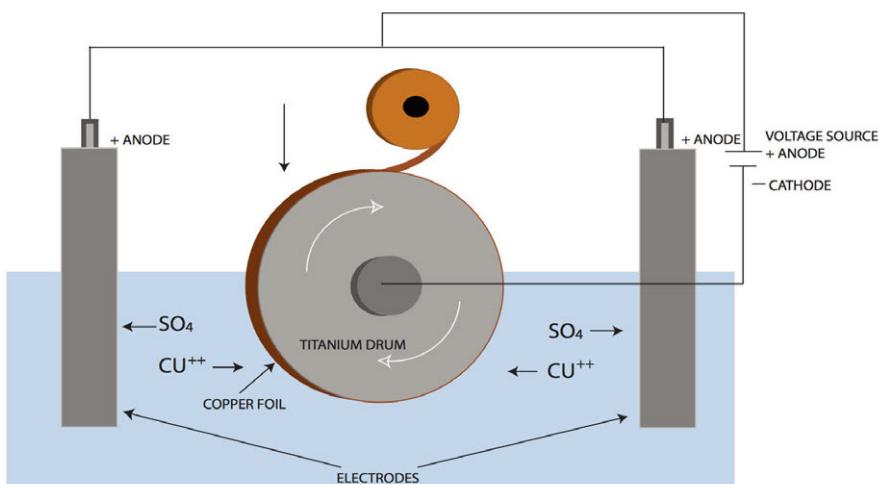


Figure 2.3: The ED copper process.

## Reverse Treated Foil (RTF)

Electrodeposited foils that have had subsequent treatment of the smooth side of the copper are referred to as reverse treated foil (RTF). These treatments are very thin, rough coatings that improve adhesion. Figure 2.4 shows typical profiles of 1/2 ounce and 1 ounce RTF copper foil.

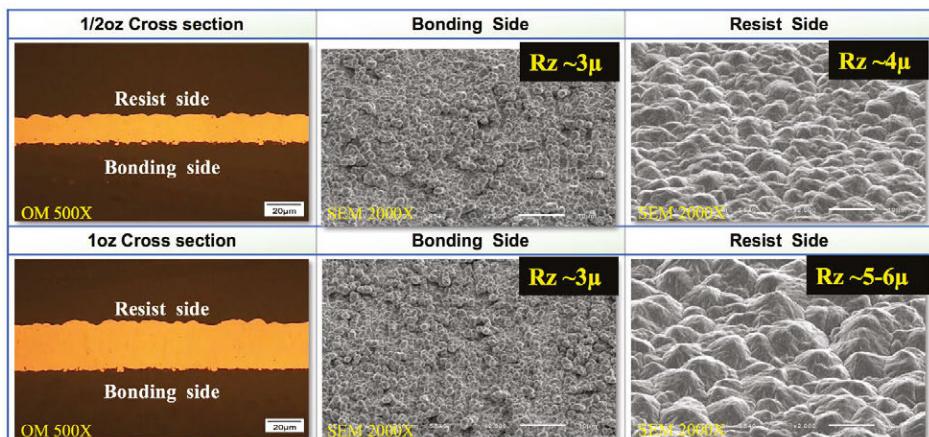
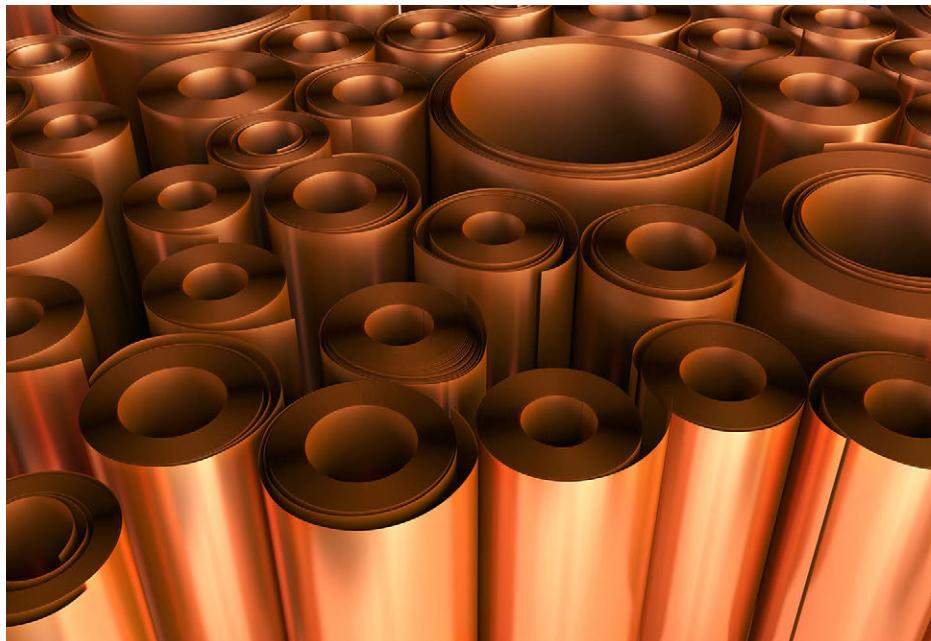


Figure 2.4: Cross-section and SEM of RTF copper foil. (Source: Isola)



## Very Low-Profile Foil (VLP)

Extremely smooth copper foil is called very low-profile (VLP), which has a greatly reduced surface roughness. Figure 2.5 shows the typical VLP profiles, and Figure 2.6 compares the profiles of RTF to VLP.

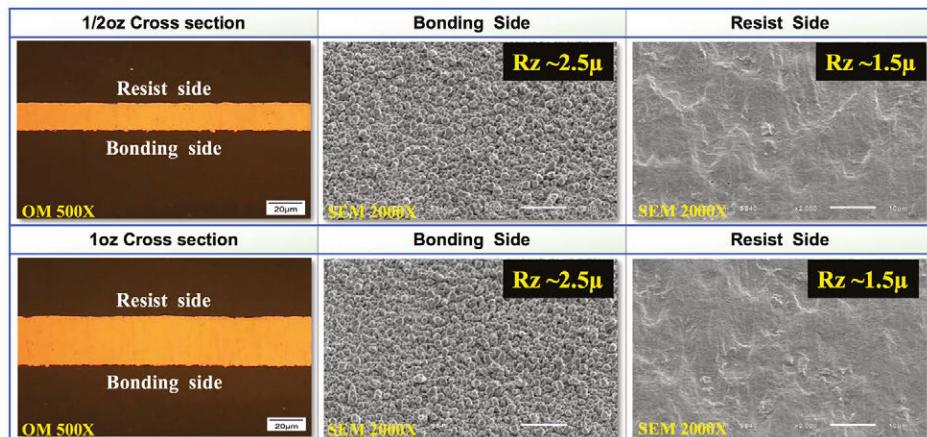


Figure 2.5: Cross-section and SEM of typical VLP copper profile. (Source: Isola)

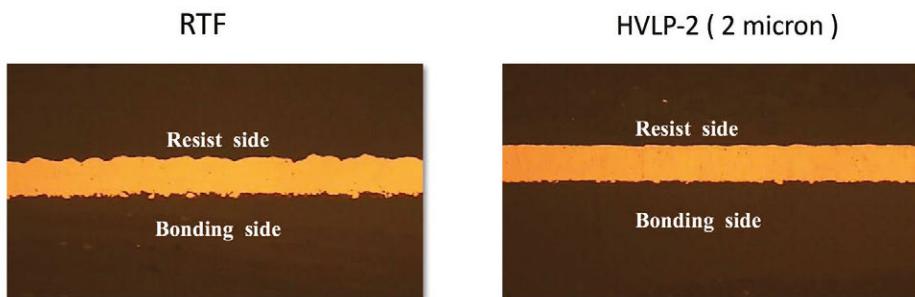


Figure 2.6: RTF versus VLP copper profile. (Source: Isola)

## Rolled Annealed (RA) Copper Foil

Rolled annealed (RA) copper foils are created by successively passing an ingot of solid copper through a rolling mill, and then applying high temperature to anneal the copper (Figure 2.7).

Each type is used for different applications. ED excels when mechanical stress will be a factor, and RA provides better performance when thermal stress will be induced. Each copper type is available in varying grain struc-

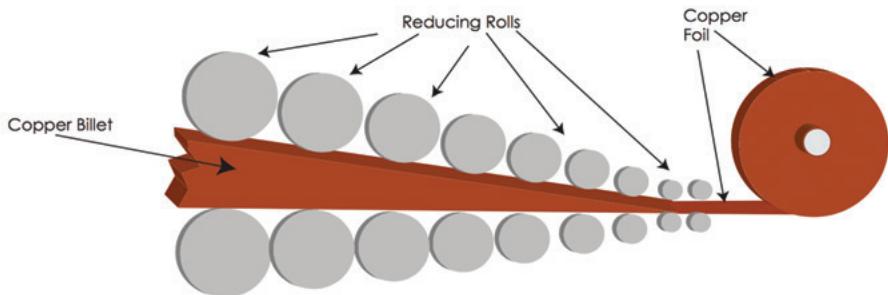


Figure 2.7: The RA copper process.

tures that translate into differing surface roughness profiles. This is important because typically the rougher the copper surface profile, the worse the signal loss performance and greater the phase variations. Smoother copper surface profiles also benefit the PCB fabricator with improved etch definition for fine-line circuits usually found in high-frequency designs. Understanding these differences in copper foils for PCBs can allow the designer to select the best circuit material for a particular RF application.

### The Effect of Oxide Treatments

The PCB fabricator may use an oxide as a surface treatment to improve adhesion, but this will impact the profile of the copper foil. As Figure 2.8 shows, there can also be a dramatic difference between different manufacturers of the oxide, which must be considered.

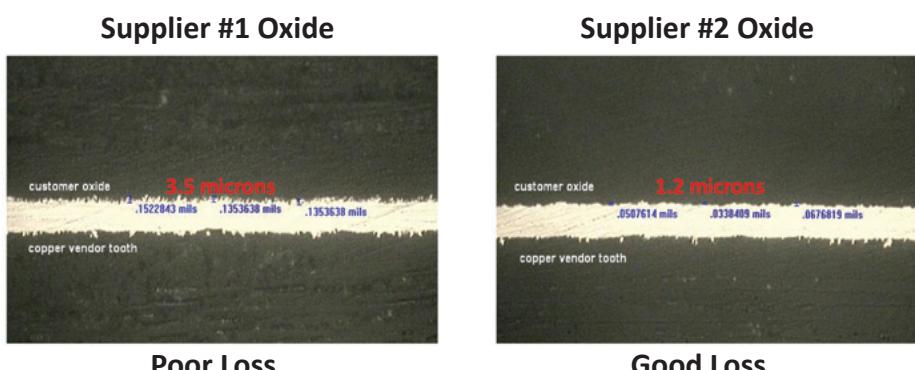


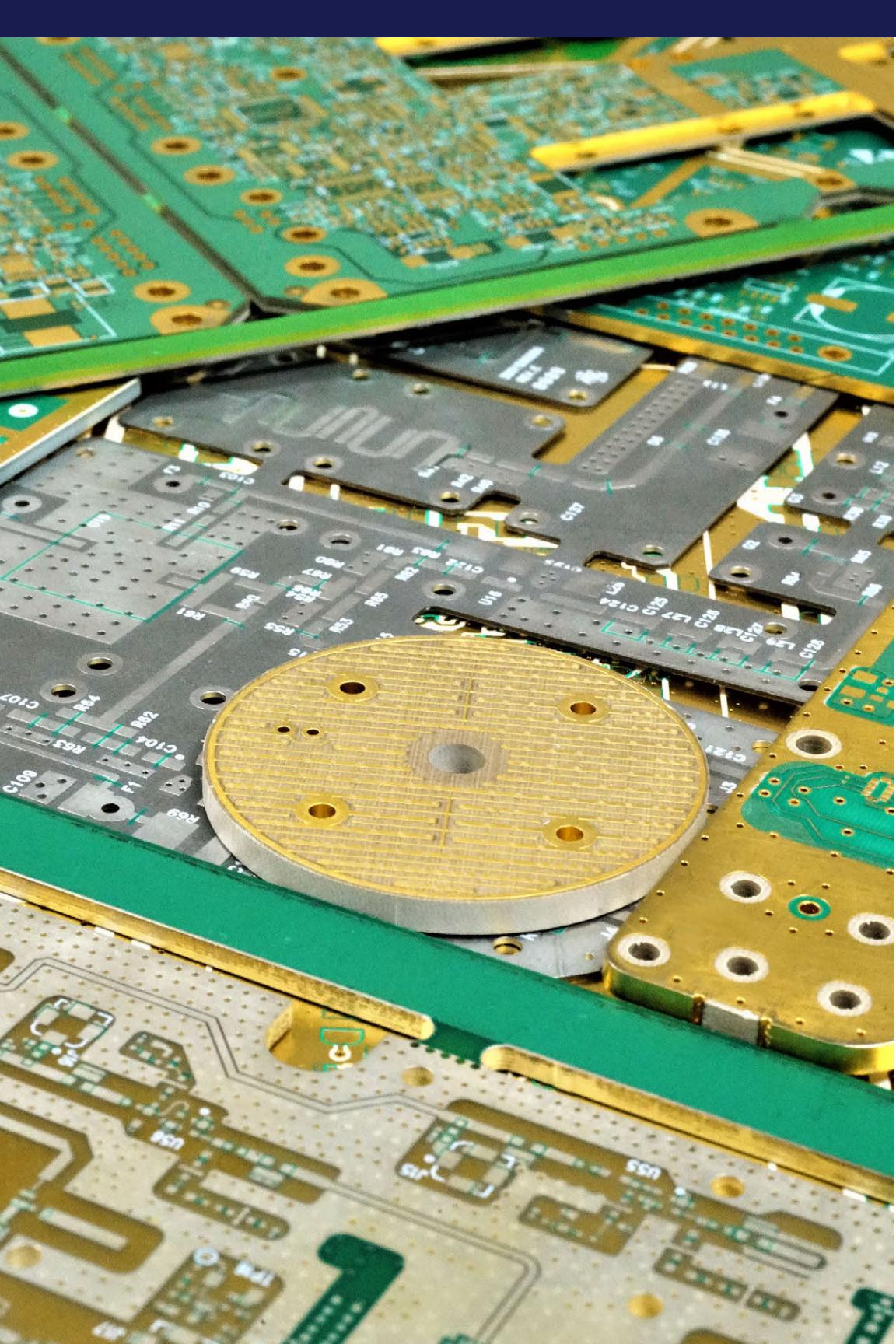
Figure 2.8: Effect of oxides on copper profile. (Source: Isola)

Consider the path of any given signal that represents not only the length of the copper circuit defined by the design and fabrication process, but also the function of the roughness of the bottom of the circuit and the roughness of the areas not directly against a dielectric material. As the circuit roughness increases, it directly impacts the speed at which the signal propagates. The effect is to slow the signal, effectively increasing the dielectric constant that the circuitry perceives.

For the non-RF engineer, perhaps, an oversimplification would be to explain this phenomenon using the following example. Think of the conductor path in terms of hiking a distance of five miles during vacation. If the hiking path were smooth like a paved sidewalk, it could be traveled at a higher walking speed in a lesser amount of time. Now, imagine this same five-mile hike were very hilly with trees and boulders that you had to navigate. While your linear path on both hikes would be equal to five miles, it would actually take much longer to traverse the rough, hilly path to reach your destination. It is this effect on the signal that produces the perceived dielectric constant that circuitry experiences.

This effect is even more pronounced with thinner dielectric material because it has an even greater impact on the effective dielectric constant as the signal propagation tends to decrease relative to the copper circuit roughness. Conversely, this effect will decrease as the dielectric material thickness increases. As thickness increases, the perceived circuitry dielectric constant will decrease toward the bulk-measured dielectric constant of the pure laminate. This has been referred to as the process dielectric constant.





# CHAPTER 3

## RF PCB Layer Stackup

### Pure Build Versus Hybrid Build

The term “pure build” refers to a multilayer PCB material construction that is composed of the same type of material throughout the stackup, such as a construction entirely of FR-4, PTFE, or another high-frequency material. A “hybrid build” multilayer PCB uses materials with significantly different critical properties than those associated with a traditional pure multilayer PCB. A hybrid could use a mix of FR-4 materials with high-frequency materials, or a mix of high-frequency materials with different dielectric constants, etc.

The reasons for using a hybrid construction in RF multilayer PCB designs are typically driven by cost, reliability, or electrical performance. Specially formulated material for high-frequency applications are typically more expensive than standard FR-4. When designs feature a number of noncritical circuit layers, these can usually be built on the more cost-friendly FR-4 material only using high-frequency RF materials on the critical circuit layers. Hybrid construction is becoming more popular as technology evolves, but hybrids bring both benefits and challenges that need to be understood. Working closely with the PCB fabricator will ensure the best construction methodology that balances RF performance and PCB manufacturability.

For example, Figure 3.1 shows a material stackup where PTFE high-performance materials are used only on the RF circuit layers while standard FR-4 is used elsewhere. RF printed circuit designers are finding that the individual circuit layers do not need to be the same dielectric materials. There is an increasing trend in RF designs that are utilizing this hybrid approach where different materials are used among the layers. This allows the choice of materials to be tailored to the various functions on the different layers of the PCB.

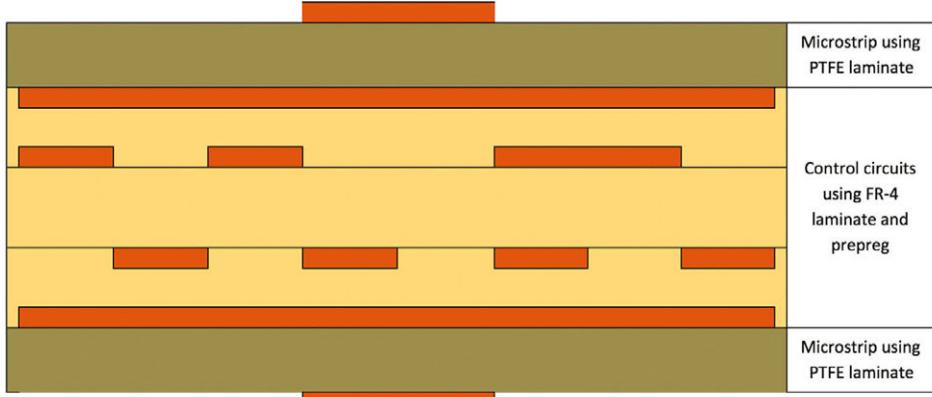


Figure 3.1: FR-4/PTFE hybrid material set.

## Balanced Structure

Regardless of the material used, maintaining a balanced construction (layup, stackup, etc.) in relation to the z-axis median of the board will ensure minimum bow and twist. This balance includes the following: dielectric thickness of layers, copper thickness of layers, distribution and location of circuits, and plane layers. A higher number of layers normally means an increased number of plane layers. Whenever possible, planes should be balanced around the z-axis median line of the layup and ideally located internal to the board. If industry-standard multilayer design rules are adhered to, boards will meet a maximum allowable bow and twist specification of 0.0075" per inch (0.75%) or better. A balanced construction is important with any PCB design, but is even more critical with a hybrid material set using mixed dielectrics. Figure 3.2 shows the difference between a non-balanced and balanced construction.

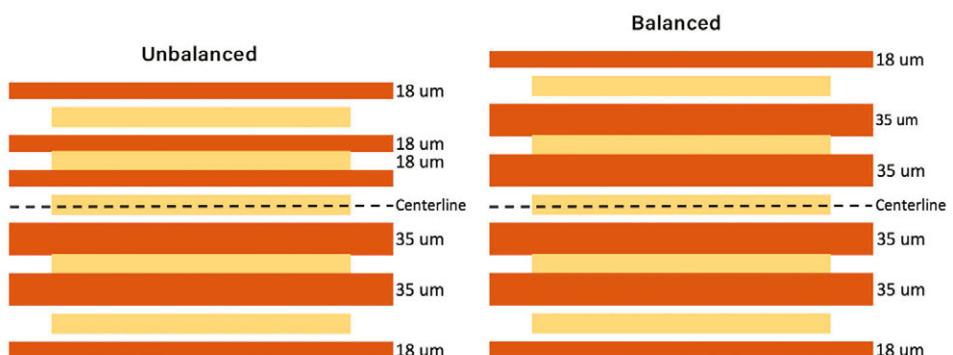


Figure 3.2: Unbalanced versus balanced construction.

## Stripline and Microstrip Structures

The two most common RF/microwave transmission-line formats are microstrip and stripline. The decision on which transmission-line technology should be used is based on a number of factors, including expected performance and ease of implementation. RF PCB designers need to recognize the differences between the two technologies to be able to select the right approach.

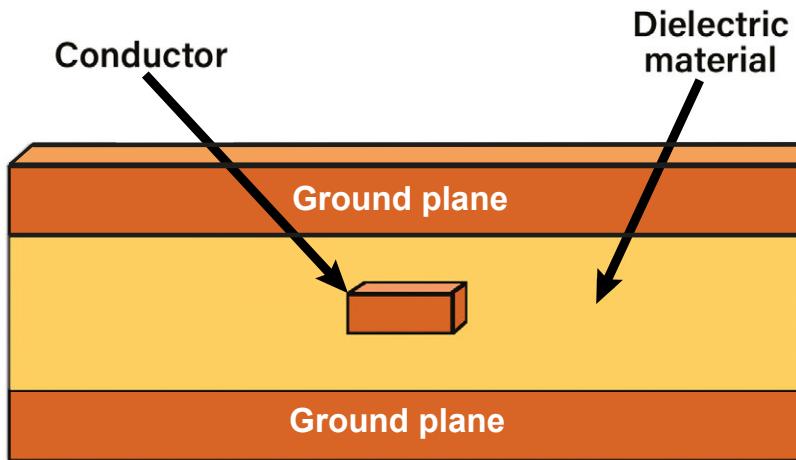


Figure 3.3: Stripline example.

A stripline is a high-frequency transmission-line technology that is essentially a trace on an internal layer that has a ground plane above and below it (Figure 3.3). Due to being surrounded by insulator (dielectric) material, stripline transmission lines do not radiate and are described as being non-dispersive. Because of this, stripline circuits can be closely spaced and densely packed, thus lending themselves to miniaturization at microwave frequencies.

There are a few stripline variations that impact differential impedance:

- **Edge-Coupled Stripline:** A configuration with two adjacent traces on an internal layer that is centered between a reference plane (above and below it).
- **Edge-Coupled Dual Stripline or Offset Stripline:** An edge-coupled stripline that is offset between the two reference planes. It is generally used when two adjacent signal layers are routed orthogonal and have reference planes outside of them.

- **Broadside-Coupled Stripline:** A configuration with the two differential lines on adjacent layers directly above one another. These are offset striplines centered between their two reference planes.

A microstrip high-frequency transmission-line technology is a simpler structure with a single ground plane, conductive trace, and dielectric layer separating the signal conductor and ground plane (Figure 3.4). Since a microstrip is not insulated with dielectric, it tends to radiate more with increased spacing between the transmission lines and the ground plane. As a result, microstrip is often a favored transmission-line format for radiating structures, such as miniature microstrip patch antennas. There are two types of microstrips that impact differential impedance:

- **Edge-Coupled Microstrip:** Composed of two adjacent traces on an outer layer with a single reference plane below it.
- **Edge-Coupled Embedded Microstrip:** An edge-coupled microstrip line that is covered by a dielectric. Solder mask will change a microstrip into an embedded microstrip line.

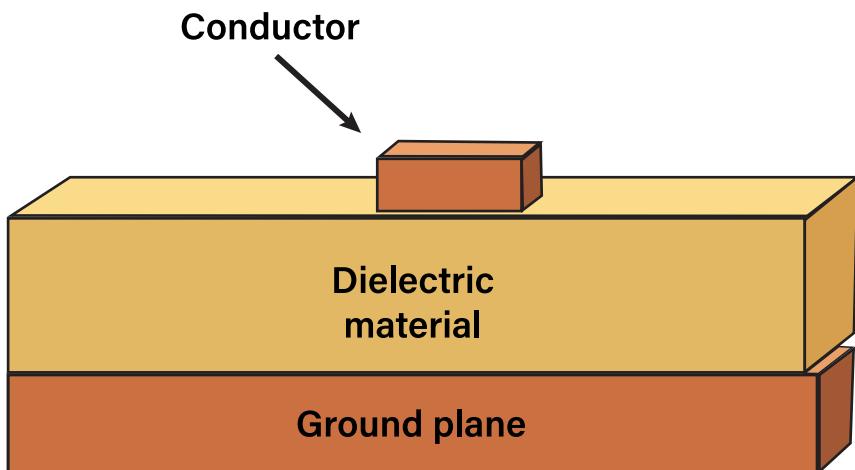


Figure 3.3: Microstrip example.



## STACKUP & IMPEDANCE REPORT

DFM Engineer:  
Dan Tozer

Job Name: Sample Job

Customer Required Finished Thickness: 345.00 ( $\pm 10.00$ ) mils

Customer: \*

Estimated Finished Thickness: 345.16 (Over mask on plated copper)

Estimated Over Lam Thickness: 342.36

Imp	Lyr	Type	Image	Foil	Plt (mil)	Thk (mil)	Er	Generic Name	Family	Vendor
SST						0				
Drill1										
TOP										
SB2		Mixed Signal			0.5oz	1.4	125	3.50	0.125 SHxSH	TC350 Taconic
					0.5oz	0				
Drill2										
ST3										
SB4		Signal								
Drill3										
ST5										
SB6		Signal								
Drill3										
ST7										
SB8		Signal								
Drill2										
ST9										
BOT		Signal								
Drill1		Mixed								

Impedance Table													
Layer	Zone	Req'd Imp (Ohms)	Tolerance (Ohms)	Calc'd Imp (Ohms)	Impedance Type	Upper Ref	Lower Ref	Design L/W (Mil)	Design Space (Mil)	Finished L/W (Mil)	Finished Space (Mil)	CoPlanar Spacing (Mil)	Artwork L/W (Mil)
****										...	...	...	...

Figure 3.4: Stackup model.



# CHAPTER 4

## Via Structures

Layers are electrically interconnected through vias (vertical interconnect accesses), which are used to carry signals or power between layers. One area that needs to be considered when designing vias is aspect ratio (ratio of the depth of the via to the diameter). While aspect ratio capabilities vary from shop to shop, we will discuss the general capabilities by hole type. Also, it is important to point out that the specific via structure design that is selected will have an impact on copper surface thickness (there are tradeoffs). The copper thickness impact is covered in Chapter 5.

### Through Vias

Through vias are the oldest and simplest via structure. They go through the entire PCB from the top layer to the bottom, and make connections on a number of inner layers (Figure 4.1). Vias are basically a smaller-diameter version of a standard component through-hole. General guidelines for the aspect ratio for through vias are 10:1 for standard technology and 20:1 for advanced technology.

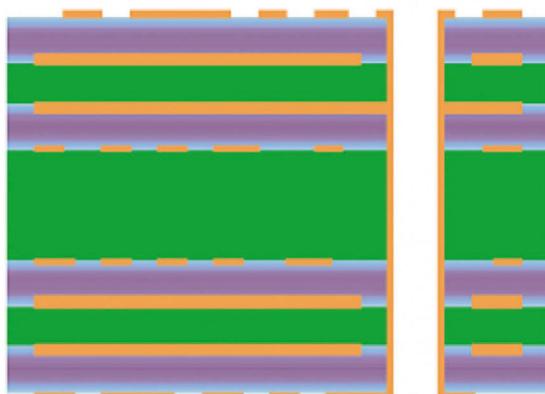


Figure 4.1: Through via.

## **Blind and Buried Vias**

Blind vias connect an outer layer to inner layers (with access to only one external layer). There are two primary methods for producing blind vias:

1. Processing the sub-assembly stackup and through drilling the vias, followed by lamination (may be multiple sequential laminations required). One may choose to fill these blind vias either in the lamination stage with resin from the prepreg/bondply, or utilize an independent non-conductive via fill prior to lamination. The aspect ratio of a hole processed in this way is based on through-hole plating capability.
2. Control depth drilling or laser drilling and plating from the top surface to the pad on the blind layer. Each type of via has its benefits and challenges; so, it is important that the PCB fabricator select the right process sequence for the specific design. The advantage with these methods is that one can plate the through vias and the blind vias at the same time. This eliminates an extra plating cycle and possibly a lamination cycle. The disadvantage is that the aspect ratio of the hole that can be formed utilizing these methods is greatly reduced to 0.7:1 for standard technology and 1.2:1 for advanced technology.

Meanwhile, buried vias connect inner layers preferably on the same core or multiple cores (with no access to external layers). Overall, blind and buried vias are unlike through-hole vias, which have access to both external layers (Figure 4.2).

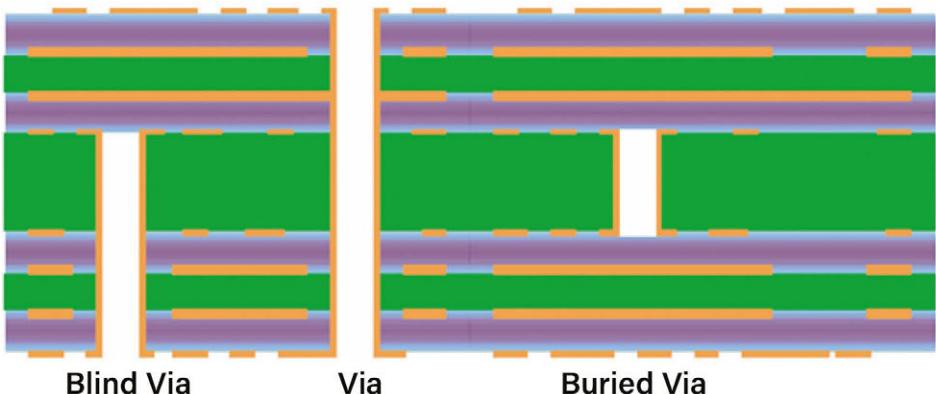


Figure 4.2: Blind and buried vias.

## **Advantages of Blind and Buried Vias**

- Only connects functionally required layers
- Circuit board real estate is conserved
- Increased wiring density (vias do not occupy all layers)
- Product safety (minimize creepage and optimize clearance distances for electrical insulation)

## **Challenges of Blind and Buried Vias**

- Restricted choice of suppliers
- More complex process (impacts cost and reliability)
- Multiple lamination and plating cycles
- Increased structural stresses
- Longer lead times
- Registration

## **Blind and Buried Via Design Constraints**

- Minimum core thickness: 0.003"
- Minimum drill size: 0.0059" with a maximum aspect ratio of 10:1 for blind/buried via substrates
- The ability to register drilled holes to inner layers is impacted after each lamination cycle
- Minimum annular ring drilled before first press cycle: 0.004" per side
- Drilled after first press cycle: 0.004" per side
- Drilled after second press cycle: 0.006" per side
- Drilled after third press cycle: 0.009" per side

## Take Note

- Copper of 1/4 or 1/2 oz. is usually required for BBV layers. Individual BBV layers will receive 0.0012–0.0014" electrolytic copper during the through-hole plating process, which brings the total copper thickness to 0.00155–0.0019" for 1/4-oz. copper foil (in this example). This is due to the surface plating to hole plating ratio that ranges from 1.2–1.4:1, dependent on hole aspect ratio.
- All BBV holes will be plugged with epoxy during subsequent lamination cycles.
- The drawing hole chart must list plated through-holes separately from the blind and/or buried via holes.

## Filled Vias, Via in Pad, and Via in Pad Plated Over (VIPPO)

Filled vias can improve routing density (Figure 4.3) and board assembly, and aid with electrical and thermal performance. Via fill should only be used if absolutely required. The benefits of via in pad technology include the following:

- Increased capture pad
- Solder mask clarity/registration
- Elimination of "pad cratering"

Vias require pads on each layer to which they connect. Because the holes are not guaranteed to be perfectly aligned due to process tolerances and material movement, there will need to be an annulus of copper around the plated hole. This is to ensure a complete 360° electrical connection around the hole. Pads on inner layer vias are larger than external layer pads to allow for greater dimensional tolerances. A clearance hole is required where

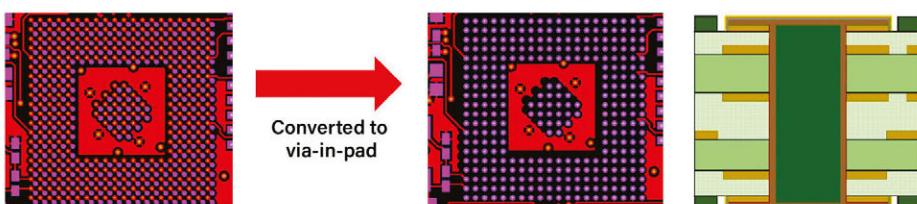


Figure 4.3: Via-in-pad.

a via passes through a plane (i.e., not connected to the plane). A thermal relief structure is generally recommended (usually four small metal bridges between the via and plane) where a via is supposed to connect to a plane. Thermal relief may be beneficial to facilitate soldering in the assembly process.

### **Advantages of Via Fill**

- Allows via-in-pad technology (microvia-in-pad and through-hole via-in-pad)
- Creates more space on the surface of the PCB for components
- Allows the size of the PCB to be smaller
- Provides more design options for improved signal performance
- The two basic types of vias that can be filled are through vias and  $\mu$ vias
- Blind or buried vias can also be filled prior to subsequent lamination since they are actually through vias prior to lamination

### **Through-Hole Via Fill**

The holes that need to be via filled are drilled first (the drill file is usually split to drill the via holes first and the balance of the holes later). This is usually filled on a specialized machine with either conductive or non-conductive paste. Conductive paste is significantly more expensive than non-conductive via fill, and it also has some greater process challenges. We always recommend that customers use non-conductive via fill instead of conductive via fill. After via fill, the part is usually plated so that the areas where the via is filled become virtually flat. Next, any plated holes that were not filled are drilled and plated. As a result, there may be multiple drilling and plating cycles. It is these multiple drilling and plating cycles that cause the most concern to the PCB fabricator related to via fill and the issues it can cause during fabrication.

Firstly, due to the increased copper thickness on the outer layer surfaces, it becomes more difficult to realize finer spaces and lines. This issue is covered in more detail in the following chapter. Secondly, the need to "split" the drills may also lead to registration issues between the two drills. These

two different tool operations may result in difficulty maintaining minimum annular ring requirements. This is particularly important when split drill is employed on thin or weak laminate, such as the highest-performing PTFE products.

General design rules for this process are as follows:

- Board thickness: 0.020–0.120"
- Drill size: 0.008" minimum and 0.20" maximum
- Copper thickness: IPC class II
- Outer layer features: 0.004" minimum trace and 0.005" maximum trace
- Non-conductive materials are less expensive than conductive materials

Table 4.4 shows the most commonly used manufacturers of via fill material.

CONDUCTIVE	NON-CONDUCTIVE
Tatsuta AE 3030	Taiyo THP-100 DX1
CB 100	Peter PP2795
	Sanei PHP 900 IR 10F

Table 4.4: Via fill materials.

### **Microvias Hole Fill**

- May be plated shut, filled separately, or filled at the same time as the through-holes, which is dependent on the type of bath and rectifiers utilized.
- Epoxy filled and plated over. This is not a preferred process over copper filling. The epoxy fill of microvias must be processed in a vacuum chamber to prevent air entrapment.

## Stacked Microvias

When the design calls for extreme routing density and even a staggered via construction will not solve the problem, stacked vias may be the solution. Stacked vias are vias that are literally “stacked” one on top of another to achieve the highest possible routing density (Figure 4.4).

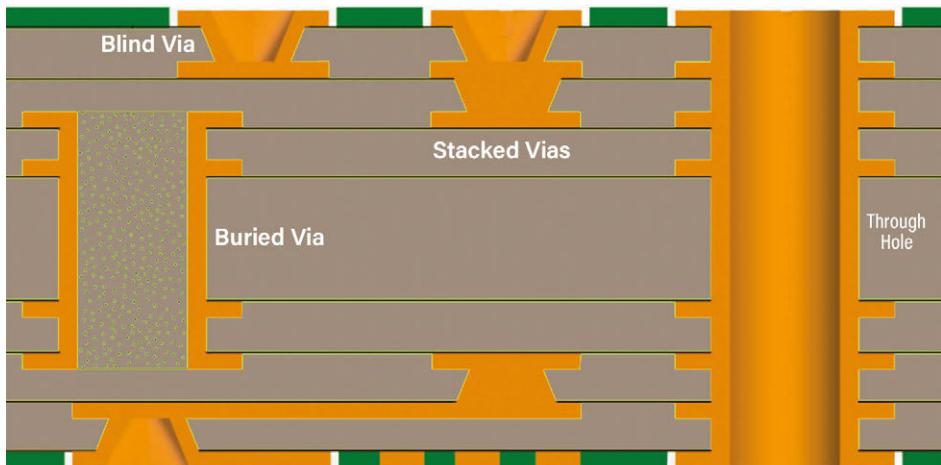
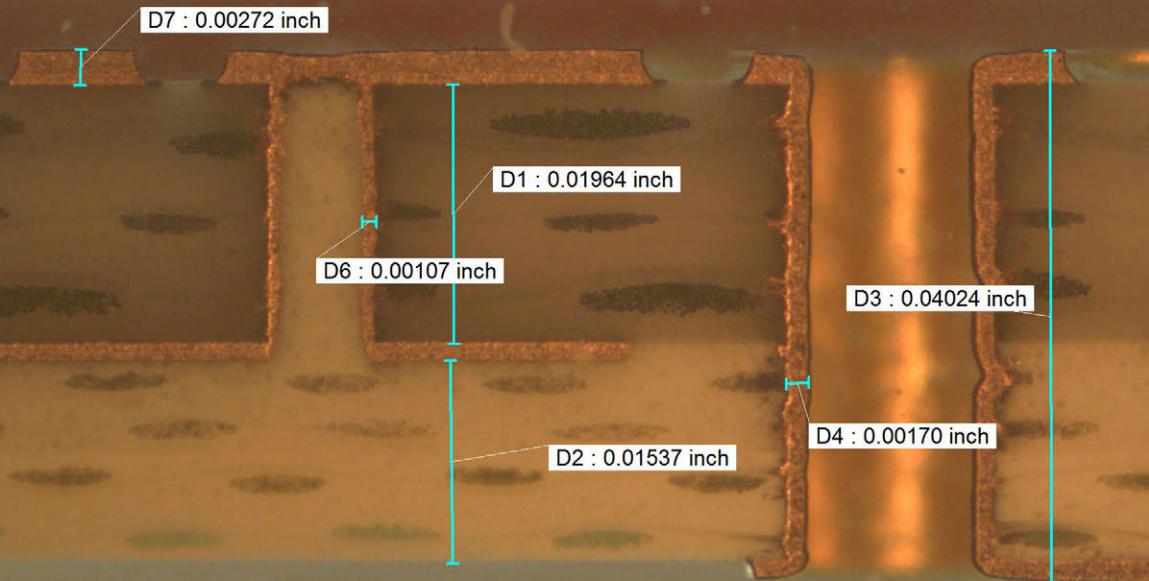


Figure 4.4: Stacked microvia construction.



## CHAPTER 5

# Impact of Copper Thickness Based on Structures of the PCB

### PCB Plating Methods

There are two methods of plating copper on PCBs: panel plating and pattern plating. The panel plating method eliminates most of the copper plating distribution issues, but because it adds copper thickness to the base layer, it makes maintaining fine line definition and consistency difficult. Base copper is measured in ounces of copper per square foot of surface area. Copper foil is available in the weights listed in Table 5.1.

Foil Weight	Approximate Thickness	Circuit Spacing Minimum	
		Innerlayer	Outerlayer/Sub-Assembly
1/4 ounce	.00035"	.002"	.003"
3/8 ounce	.0005"	.002"	.003"
1/2 ounce	.0007"	.003"	.004"
1 ounce	.0014"	.005"	.006"
2 ounce	.0028"	.006"	.0075"

Table 5.1: Base copper foil thickness.

### Take Note

It is important to mention that the guidance presented in Table 5.1 is for the raw copper foil weights, not any additional design features like via fill or sequential blind laminations that will add copper thickness to the foil. A common misconception is thinking the use of thin foil materials will solve these problems. However, it will not, as these features result in the outer layer(s) being panel plated. Thus, what originally started with a 1/4- or 3/8-oz. foil ends up close to 2 mils of copper, which is prohibitive for etching 3-mil and possibly 4-mil spaces. Final copper weight must always be considered when factoring spacing requirements.

ASC fabricates most printed circuit boards with the pattern plating process (Figure 5.1). This process has major advantages, since only the base copper requires etching. This process may offer benefits, such as achieving a finer, well-defined line. Another possible advantage is the variation in track height due to surface density.

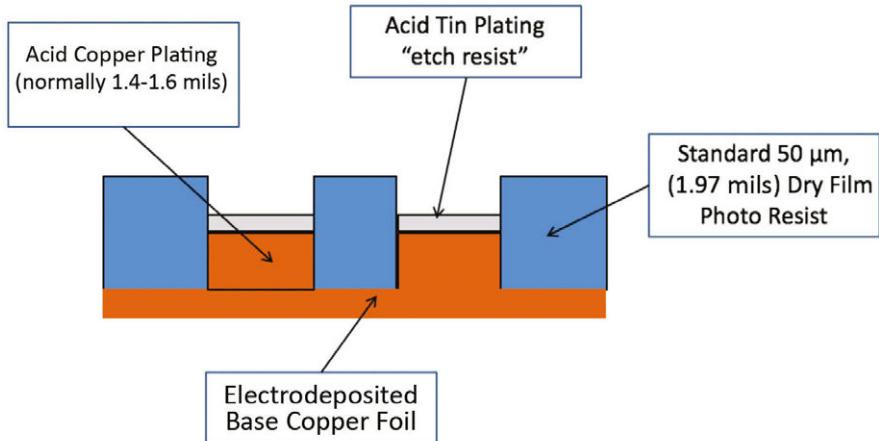


Figure 5.1: Components of pattern plating.

## Design Compensation

Due to the physics of producing printed circuits, the PCB fabricator first needs to plate the circuit pattern (pattern plate), then use a chemical etching (subtractive process) to define the circuit line width and space. To accomplish this, the initial circuit definition will need to be compensated for line-width loss due to etching to ensure that the final circuit will meet the design criteria. Spacing between circuits also needs to be considered because any positive adjustment to the circuit width will have a reverse effect on the spacing between circuits. This creates issues when the design encroaches on the lower end of the fabrication tolerance and eliminates the fabricator's ability to properly compensate for processing.

For example, a design that has circuit spacing of 4.61 mils will be reduced to 3.21 mils after a standard compensation of line width for 1-oz. copper (1.4 mils). This begins to introduce manufacturability concerns, particularly on outer layers that receive additional copper plating for subsequent processing (discussed later). This is not as big of a concern on inner layers of multilayer PCBs since spacing of 3 mils and slightly below is easily accommodated. Figure 5.2 illustrates this process and shows the typical trapezoidal-edge profile that the etching process produces.

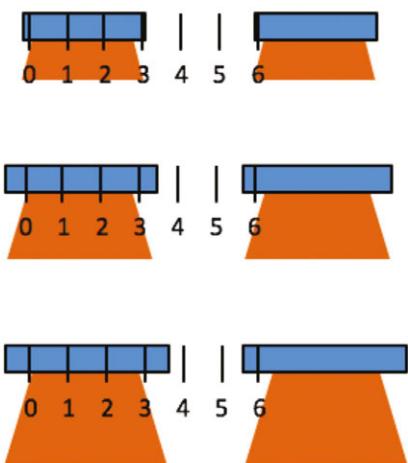


Figure 5.2: Panel-plating thickness on etched space and profile.

## Surface to Hole Plating Ratio

Regardless of how much copper a fabricator begins with (1/2 oz., 1 oz., or more), additional copper on the surface will be plated (pattern plating) as the plated through-holes are metallized (Figure 5.3). The key is that this is not a 1:1 ratio; more copper will always be deposited on the surface than in the holes due to a higher plating-current density on the surface. A working guide would be to calculate that 1.2–1.4 times the average minimum hole thickness will be deposited on the surface.

Using the industry standard requirement of 1 mil in the hole, the surface would receive 1.2–1.4 mils of *plated* copper on the surface *plus* any base copper thickness.

For example, starting with a 1-oz. base copper thickness (1.4 mils), the total surface thickness would be 2.6–2.8 mils. For a 1/2-oz. base copper, the total would be 1.9–2.1 mils of copper. If the desired final surface copper thickness

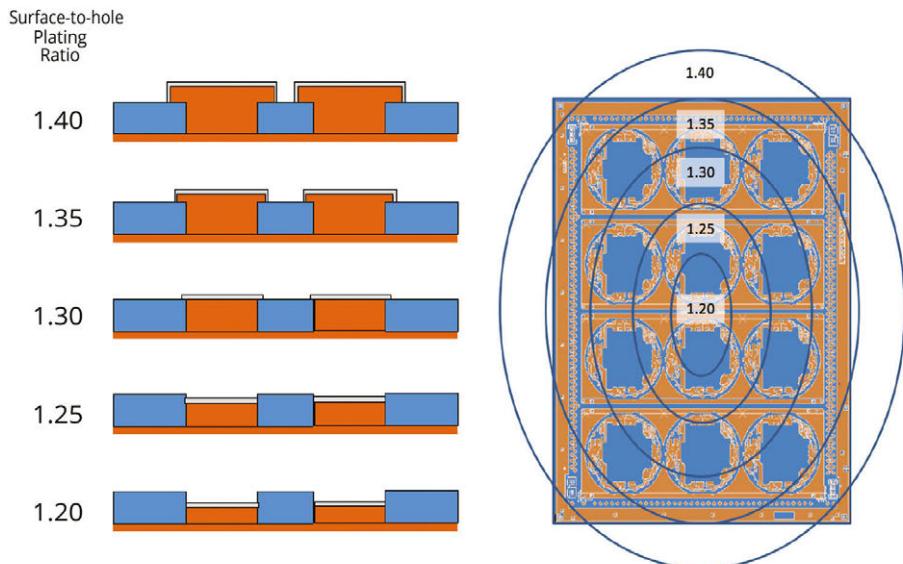


Figure 5.3: Surface-to-hole plating and current density relationship.

is close to 2 mils of copper, starting with 1/2-oz. base copper will provide a twofold benefit: It will decrease the amount of copper the fabricator needs to etch through, which reduces the likelihood of space/gap formation issues; and it will increase the line width consistency, which reduces circuitry width and gap variation throughout the PCB. The takeaway here is that if you do not need heavy copper for high current-carrying capability, start with 1/2 oz. copper.

## Impact of Sequential Laminations and Via Fill

Sequential lamination (sub-assembly processing) is used to manufacture buried/blind vias, via fill, microvias, etc. These technologies further compound the final surface copper thickness considerations, which were discussed previously, because each process requires additional plating and etching processes. Figure 5.4 illustrates these considerations. A growing problem is that designers keep adding complexity to RF stackups without fully understanding the impact of additional plating processes on the final thickness of copper traces and surfaces.

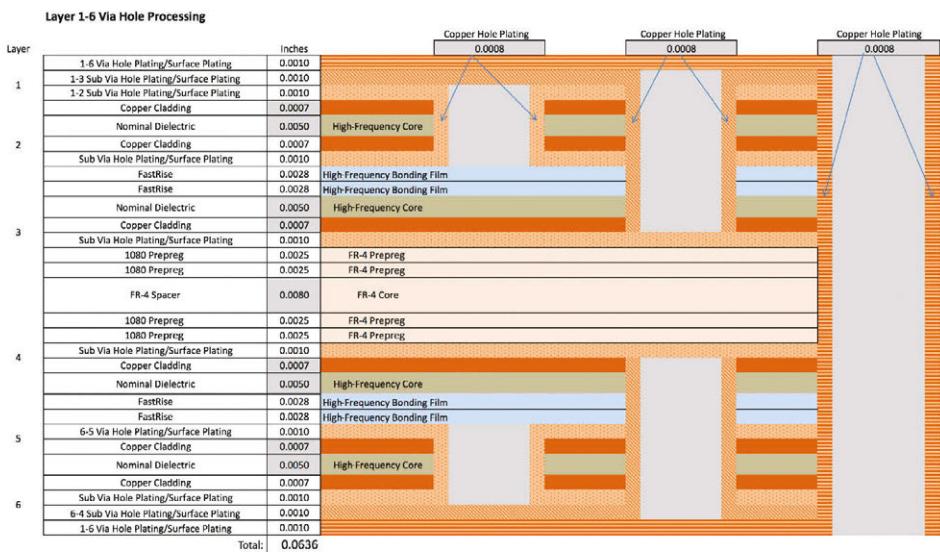


Figure 5.4: Chart showing the impact of sequential lamination.

## Via Wrap Plating

As mentioned earlier, buried/blind vias and microvias are created by sequential lamination processes that add additional layers of copper plating as each sub-assembly of buried/blind vias and/or microvias are formed. In the process of plating copper, as the barrel is plated to a minimum thickness, the surface is also plated with each sub-assembly. As the plating transitions from the barrel to the surface, it wraps around the knee of the hole (the right-angle interface of the hole wall and the surface). As the copper thickness builds up on the surface, it is necessary to remove some of the excess copper (and in some cases, via fill material) through a mechanical process called *planarization*.

Planarization typically removes a small amount of surface copper (0.0001–0.0002") and creates a flat, or planarized, surface to facilitate the image, etching, and lamination of the sub-assemblies. There are two critical manufacturing conditions that the PBC fabricator must tightly control: the wrap needs to extend onto the top of the PCB pad a sufficient distance for electrical and thermal integrity (IPC-6012 specifies that the wrap thickness will be a minimum of 0.0002" for Class 2 and 0.0005" for Class 3); and the PCB fabricator must take into account that the planarization process does not reduce the knee of the plated via below minimum design requirements (Figure 5.5).

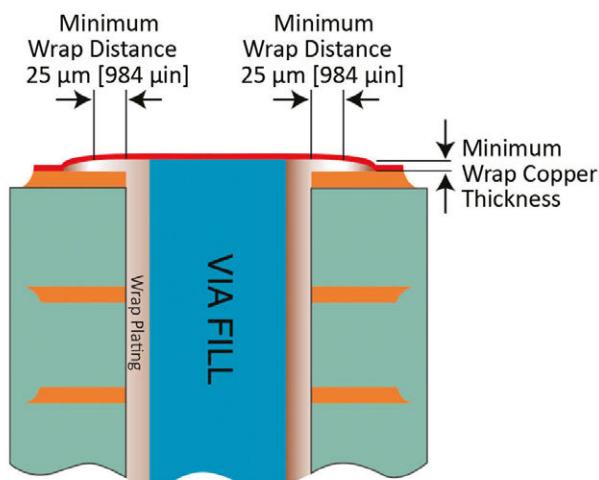


Figure 5.5: Wrap plating. (Source: IPC-6012)



# CHAPTER 6

## Edge Plating

Encapsulating the edges of printed circuit boards with plating may be required to improve EMI shielding of higher frequency designs and to improve chassis ground in electronic systems (Figure 6.1). The requirement for edge plating is being implemented for single-axis and multiple-axis edges of the circuit board, including all four edges. Edge plating is created when a rout path operation is performed prior to the metallization of the circuitry features of the printed circuit board, and is sometimes referred to as a “plated rout” feature. The design requirements for implementing this technology are dependent on the requirement for the number of edges of each board, the size of the board, and whether the boards will be delivered in a multi-up array.

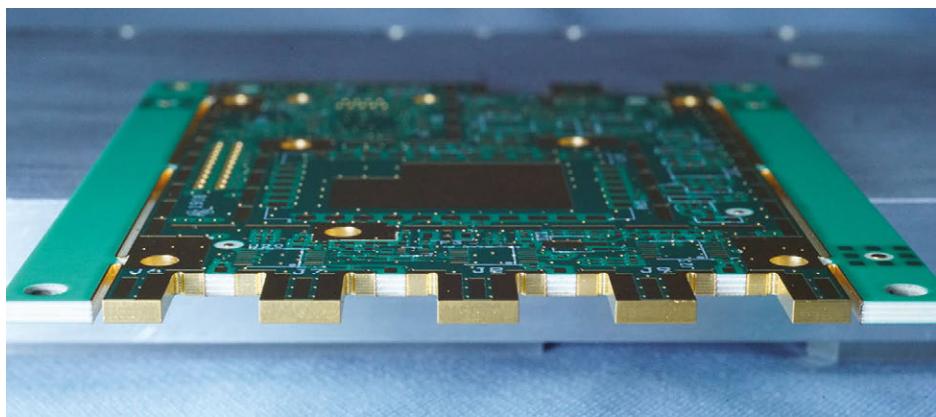


Figure 6.1: Edge plating.

The stability of the material used for the manufacturing of the board will also play a part in the development of the routing requirements. Non-standard materials without glass reinforcement may require a special routing design to ensure sufficient stability of the partially routed panel to hold up through the remaining manufacturing operations. The parts are processed

still intact inside the carrier panel used for manufacturing, which requires the development of tabs (in some cases) for edge plating. Tabs may not be required for stability for a single edge requiring plating.

### Development of Tabs for Transporting the Panels

The left image in Figure 6.2 shows how perforated tabs are implemented for a PCB that is manufactured in a multiple-up array. The requirement is that the tabs being used to hold the board in the array will be broken off after the assembly operation. The right image in Figure 6.2 shows a solid tab that is placed at the plated rout locations. In both cases, the internal and external layer artwork around the tabs must be void of metal. This will prevent the metal from being exposed in the de-tab process. When a solid tab is used, the tab is removed at the final fabrication stage using a router (the same router that removes standard parts from the carrier panels). Removal of the tab will leave a small protrusion along the edge of the part.

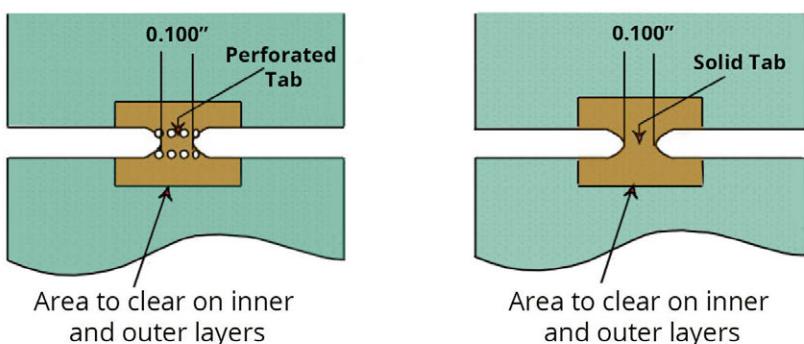


Figure 6.2: Edge plate tab design guidelines.

Figure 6.2 also details the minimum requirements for the dimensions of the tabs. Placement of the tabs is based on assembly requirements and the materials being used to construct the circuits. Less dimensionally stable materials—typically non-reinforced materials—and panels that are exceptionally thin ( $<0.060"$ ) or thick ( $>0.200"$ ) will require additional tabs for stability in processing. Conservatively, the tabs are placed every 2" along the plated edges.

### Design Rules for Plated Edges

It is required that the plating not only encapsulate the edge of the panel, but also that the plating wrap around to the surface of the panel. This is detailed in Figure 6.3 where the minimum distance the plating is required to

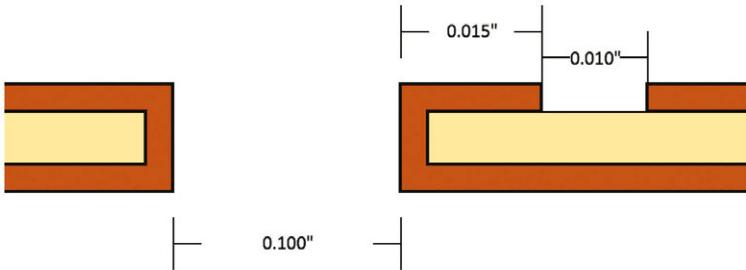


Figure 6.3: Edge plate feature minimums.

wrap around the surface is 0.015". The wraparound is required for internal processing and adhesion of the plating to the edge. Figure 6.3 also shows the minimum distance a feature can be placed to the wrap around plating (0.010") and the distance required for an adjacent routed feature (0.100").

It is typical that the plating be continuous along the entire edge of the circuit. Interruptions in the plating can be designed with two methods: placing a tab at the interruption and subsequently removing it to prevent the plating; or removing plating interruptions at the final routing stages. The subsequent removal of the plating will leave a small tab or an indentation on the circuit

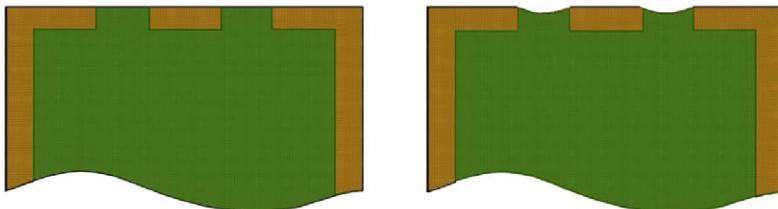
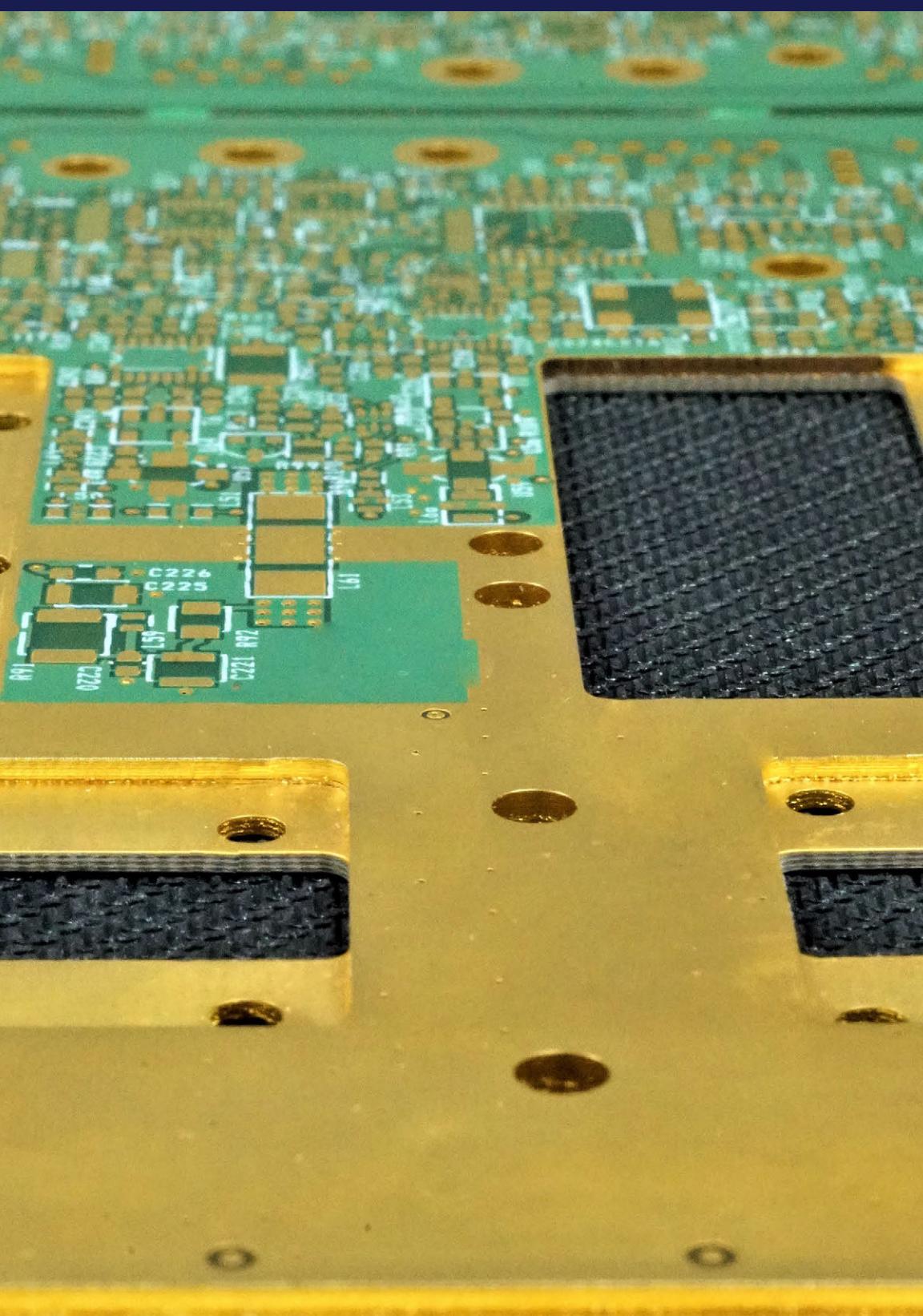


Figure 6.4: Edge plate tab removal.

similar to the right image in Figure 6.4. The indentation is created when the router bit contacts the edge where the plating is removed, and advances into the circuit to completely remove the plating. When the interruption of the plating is a minimum of 0.200", the use of a tab to prevent the continuous plating can be used. When less than 0.200", the edge will be plated entirely across and subsequently removed by the routing process described.

Edge plating typically involves the connection of one or more of the internal planes in a board. These planes extend to the edge of the board and are electrically connected by the plating process. Those layers are usually fabricated with a polarity border (ref. 0.050") to prevent exposed copper when they are routed and removed from a panel.



## CHAPTER 7

# Cavity Constructions

Cavity PCBs have structural recesses to enable additional functionality compared to a standard printed circuit board. This type of feature allows the insertion of heat sinks, often referred to as "coins," which are used to position electronic components below the surface, thereby giving the assembled PCB a thinner overall profile. The inner cavity surfaces can also be used for electrical contact, normally a ground connection. While there are many ways to create a cavity in a PCB, the most common method is by mechanically removing material from a PCB structure to create a "window-type" cavity in a multilayer PCB. As the laminate and prepreg layers are assembled, the layers forming the windows will create the walls of the soon-to-be cavity. If the cavity is functioning as a RF/microwave resonant cavity, the frequency is determined by the size of the cavity and the PCB manufacturer must tightly control the X, Y, and Z dimensions of the cavity. Cavity designs can be applied in multiple locations at different depths on a single printed circuit board, and they can also be edge plated (Figure 7.1).

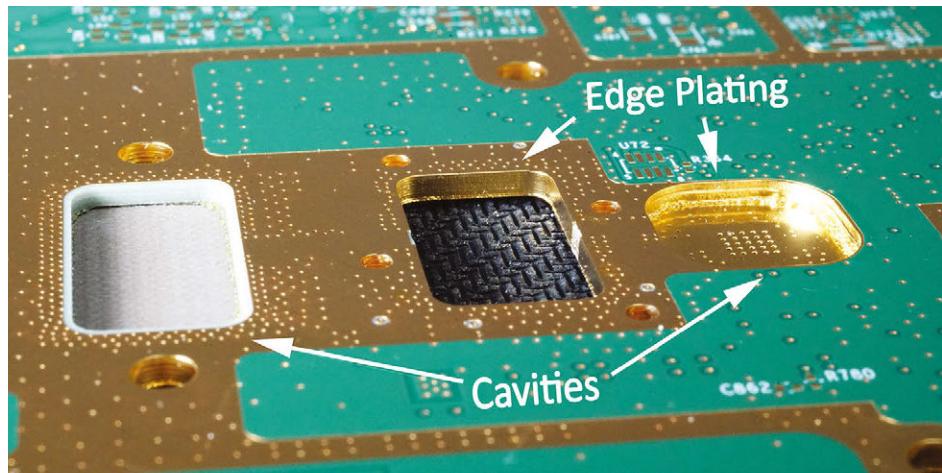


Figure 7.1: Cavity construction.

## Prepreg Materials

Prepreg is a shorthand expression for "PRE-imPREGnated"—a fiberglass or other fabric reinforcement that has been saturated with a partially-cured resin system at the laminate manufacturer. Prepreg is also called B-stage or bonding sheet. When the prepreg is laminated (bonded) in the multilayer package at the PCB manufacturer, the prepreg "flows" under heat and pressure. In a standard multilayer construction, preps with high-flow characteristics are desired to ensure the encapsulation of circuits, filling of holes, and elimination of voids. However, when bonding cavity PCBs, a no/low-flow prepreg is preferred. It is important for designers to understand that even no/low-flow preps flow, but the flow can be more controllable and predictable. Additionally, it is important to recognize that the flow characteristics are impacted by the underlying PCB circuit/plane pattern and the configuration of the bonded heat sink.

To compensate for the flow, the PCB manufacturer will engineer the prepreg route program to recess all the edges so that after lamination, the prepreg flows back to the desired position (Figure 7.2).

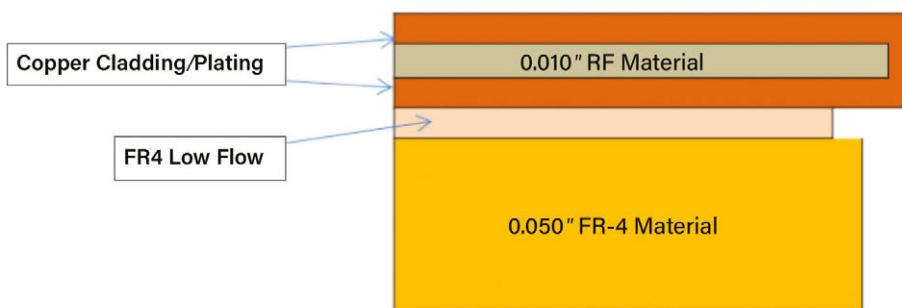


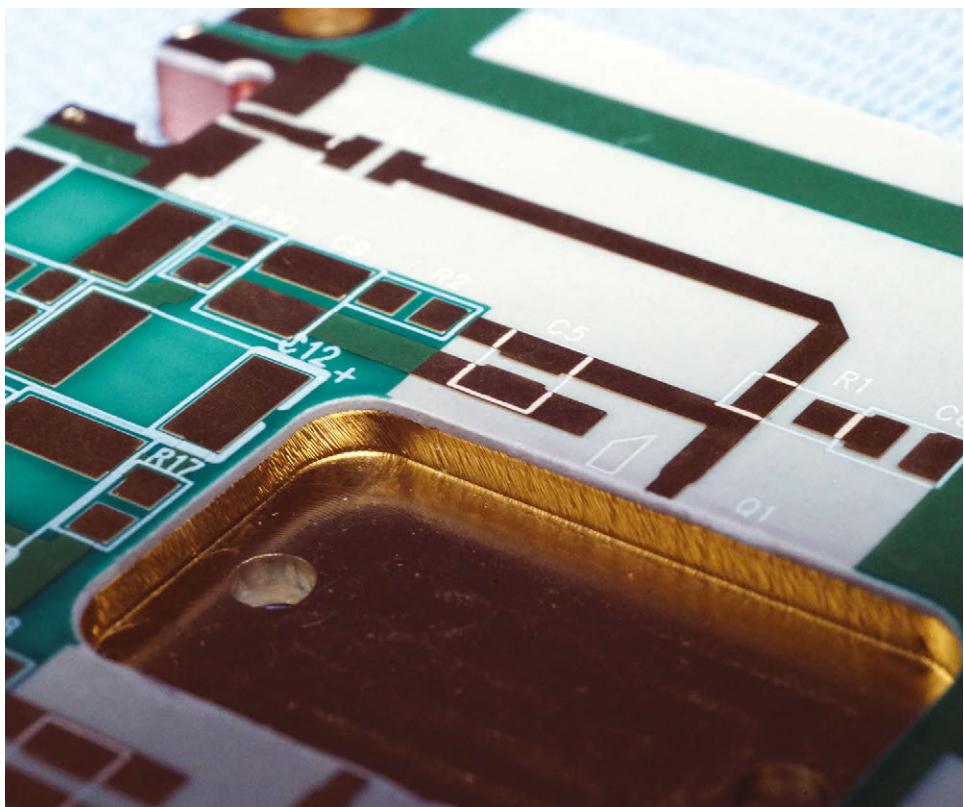
Figure 7.2: Low-flow prepreg cutback.

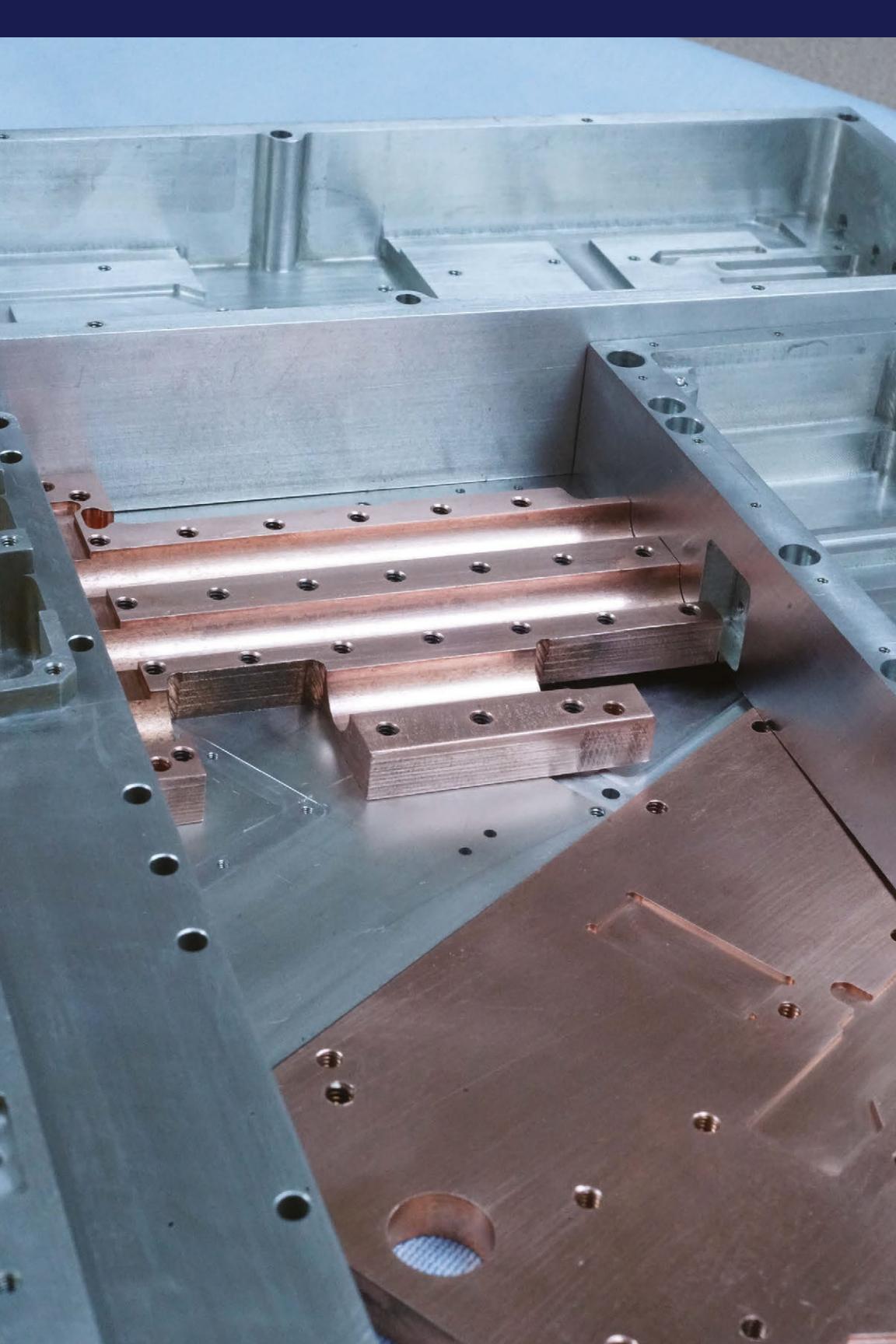
Each no/low-flow prepreg has a unique resin-flow percent tolerance that needs to factor into this adjustment. However, even with the best flow-characteristic modeling, some trial-and-error lamination cycles may need to be run before the bonding profile can be finalized. Another critical consideration is that some flow bleed into the cavity is desired to ensure complete

bonding. By collaborating with the PCB manufacturer, RF designers can avoid selecting bonding materials that lack good flow control and might flow into the resonant window or cavity area. In a resonant cavity design, changing the dimensions of the resonant cavity will change the operating frequency.

## Cavity Design Considerations

- Cavity designs should utilize no/low-flow prepreg
- Acceptable bleed into cavity needs to be defined (IPC 6018 allows 0.029")
- Critical registration (special tooling, fixturing, and bonding profiles are required)





## CHAPTER 8

# Thermal Management

Rapid advances in the use of RF/microwave frequency bands have forced increased density of RF/microwave devices to achieve escalating frequencies to support the “smaller, faster, cheaper” design evolution. These constraints require efficient thermal management. Thermal management plays a very important role in the design of RF/microwave electronic devices. A fairly large quantity of heat is generated when signals are processed in high-frequency applications, particularly in the amplification of high-frequency signals. Reliable performance of an RF/microwave device depends on maintaining a constant value of the dielectric constant of the PCB’s dielectric layer.

The dielectric constant varies as a function of temperature. Thus, it will have a direct impact on the high-frequency performance of the circuit because changes in the dielectric constant will result in changes in the RF/microwave circuit impedance. Variation in the dielectric constant occurs because any rise in temperature will result in an increase of thermal conductivity. As a result, this will lead to a decrease in the dielectric constant (since the dielectric constant is inversely proportional to the thermal conductivity). Tightly controlling characteristics of the PCB material, such as the thermal coefficient of the dielectric constant and the CTE, is required to ensure signal and power level performance.

Thermal management of an RF/microwave component, circuit, or system is simply a matter of removing heat from sensitive areas of a design that can suffer damage or performance degradation from the heat. This chapter primarily focuses on the different methods of using metal to enable improvements in thermal management. It is also important to understand that apart from the thermal management function, the metal also acts as a grounding layer. Heat sinks and PCBs are typically connected thermally and electrically, and utilize the metal heat sink to control thermal dissipation and grounding of circuits.

At a high level, there are two ways to achieve thermal management of RF PCBs that utilize metal: the first is pre-bonded, and the second is post-bonded. Pre-bonded laminate has a cost premium and is typically single-sided, although ASC has a proprietary capability to pre-bond within a multi-layer. In a pre-bonded circuit board, the PCB supplier buys the laminate material pre-bonded to the metal. The post-bonded process is the most common in multilayer applications. Most of the available RF/microwave laminate materials can also be bought in a pre-bonded configuration. The two laminate suppliers that have a majority of this market are Rogers and Taconic. The PCB manufacturer is then tasked with processing this material, making circuits, and machining the metal. In a post-bonded circuit, the PCB supplier manufactures the PCB and the metal concurrently and separately, and then bonds the two together using a variety of methods.

There are a number of pros and cons to these various methods. Pre-bonded PCBs are typically used in high-reliability, military, aviation, and telecom applications because they offer precise dielectric constant control, no risk of delamination, and high reliability. The two disadvantages of this methodology are: that it is restricted to a single layer of circuitry; and the costs tend to be significantly higher with pre-bonded versus post-bonded largely due to the premium price and increased risk of processing low-loss materials in conjunction with a thick metal layer. Simply put, the costs are higher because the laminate materials are significantly more expensive, processing is more challenging, and any yield issues result in very expensive scrap. There are cases where pre-bonded PCBs can be converted to post-bonded PCBs for a cost reduction. Any multilayer applications that require metal for thermal management will need to utilize post-bonding.

### **Pre-Bonded Laminates**

There are several design parameters that need to be considered, starting with the laminate selection. The first step is to determine dielectric material, dielectric thickness, and the copper foil weight appropriate for the design application. The next step is to determine the thickness and type of metal to be used. Typical metals used include aluminum 6061-T6 and copper C110, but depending on the application, brass may be used. Figure 8.1 shows a typical pre-bonded material. Again, a cost-benefit balance must be considered because although aluminum is lighter and cheaper than copper, it's more difficult for the PCB manufacturer to process in pre-bonded applications.

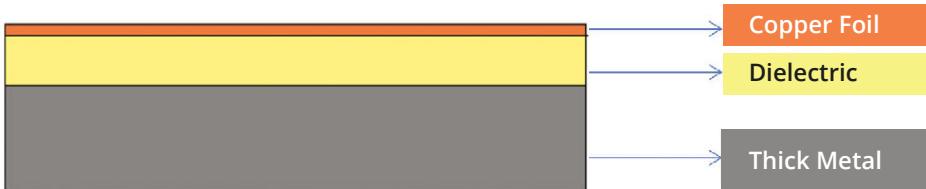


Figure 8.1: Pre-bonded metal.

Table 8.1 shows typical properties of aluminum and copper. Once the laminate selection has been determined, engagement with the PCB supplier and/or the laminate manufacturer is critical to ensure the selection is both available and manufacturable. Depending on machining requirements, a metal thickness that is higher than the finished thickness may be required.

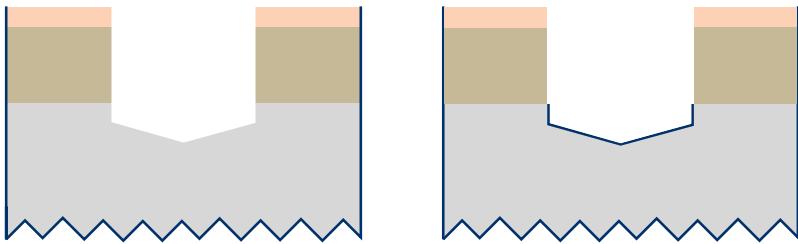
Property, Units	Aluminum	Copper
Alloy Number	6061	110
Tensile Strength, kpsi	20	35
Specific Gravity	2.7	8.9
Specific Heat, J/kg°K	960	385
Thermal Conductivity, W/mK	180	390
Thermal Expansion, ppm/°K	24	17

Table 8.1: Metal properties.

## Heat Dissipation

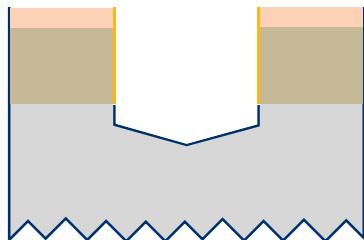
Post-bonding dissipates heat through the mechanical connection between the bottom-side PCB ground plane and the heat sink. This is more challenging because dissipation is dependent on the integrity of the bonding material. The pre-bonding method uses a blind via process, which requires some special equipment and processes, but results in a more robust thermal management solution. Figure 8.2 shows the progression of the blind via process.

The blind via aspect ratio is another critical design factor. Ideally, one wants the blind via to be an aspect ratio of <1:1. However, ASC has been successful with blind via aspect ratios up to 1.2:1. One can also build pre-bonded boards with through vias. It is best to work closely with the PCB manufacturer on the proper via approach for the application.

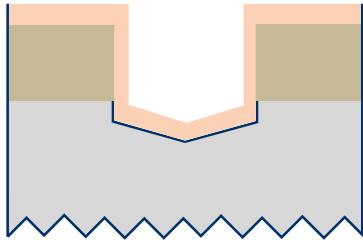


Control Depth Drilled Blind Hole  
Exposing Aluminum

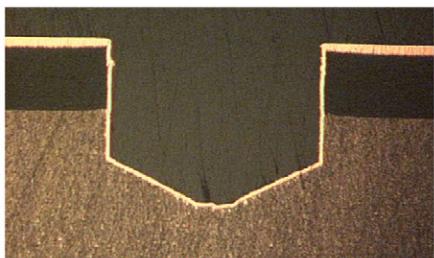
Zincate and Nickel Barrier  
on Aluminum



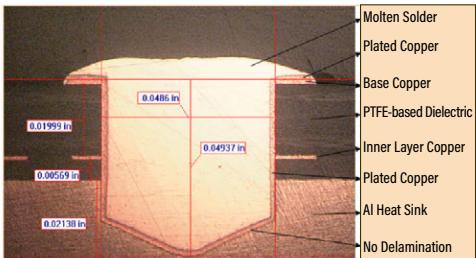
Sputtered Copper Metalization  
Covering Dielectric and Barrier



Acid Copper Plating  
Over Metalization



Sputter Ar Ion Activation  
and Cu Deposition



Cross-section of Solder  
Stressed Blind Hole

Figure 8.2: Blind via plating process.

## Post-Bonding

In a post-bonded application, a double-sided PCB or multilayer PCB is manufactured first. Typically, the bottom layer is mainly a ground layer and occasionally contains a few circuits. While the PCB is being manufactured, the metal can be simultaneously machined on a CNC machining center. There is a lot more flexibility in terms of the shape and features in a post-bonded application, which allows for the metal to be plated independently of the PCB. The form factor of the metal can be quite different than the PCB. Once the PCB and metal are completely manufactured, they can be bonded together. This is usually done in piece form (i.e., a single-up PCB bonded to

the metal). However, there are some special applications where multiple PCBs may be bonded to the same piece of metal. Since the bonding is done post PCB processing, these different PCBs do not need to be the same material set or thickness.

PCBs are typically post-bonded using one of two methods: sweat solder or sheet film adhesive. A custom bonding fixture will be required to ensure registration between the PCB and the metal carrier, and to control the pressure being applied in the bonding process. Table 8.2 shows the requirements for bonding registration holes. Figure 8.3 shows two different examples of how the registration holes can be managed and the impact on overall registration.

	BONDING MEDIUM	Fixture Type	REGISTRATION	Preferred Hole size
Electrically & Thermally Conductive	Electrasil-1 & -2	High Temp FR4, Polyimide, or Metal Al 6061	2 diagonal holes preferably 3 holes at outermost edge of the part	.125" or larger
	CF3350/Ablefilm	High Temp FR4, Polyimide, or Metal Al 6061	2 diagonal holes preferably 3 holes at outermost edge of the part	.125" or larger
	Sweat Solder	Metal-AL 6061	Scattered holes throughout the part as equally distributed as possible for even pressure distribution.	2-56 or 4-40 tapped

Table 8.2: Bonding registration requirements.

#### Same Hole Size in PCB and Carrier



#### Tight Fit Hole in Carrier and Larger Hole Size in PCB



#### Preferred Method of PCB to Carrier Alignment

Figure 8.3: Registration examples.

Most often, the bottom layer is primarily a ground layer and has very little or no solder mask. Sweat solder and sheet film adhesive are two of the bonding techniques that will be explored in the next section.

## Sweat Solder

High temperature solder is used to bond the PCB to the metal. The solder used has no risk of debonding in subsequent assembly-soldering operations. One of the biggest discussions associated with this technique is void volume. Since the solder paste is a mixture of flux plus solder, the flux creates air gaps as it volatizes. Figure 8.4 shows how a sweat solder board is assembled.

### Sweat Solder Joined PCBs

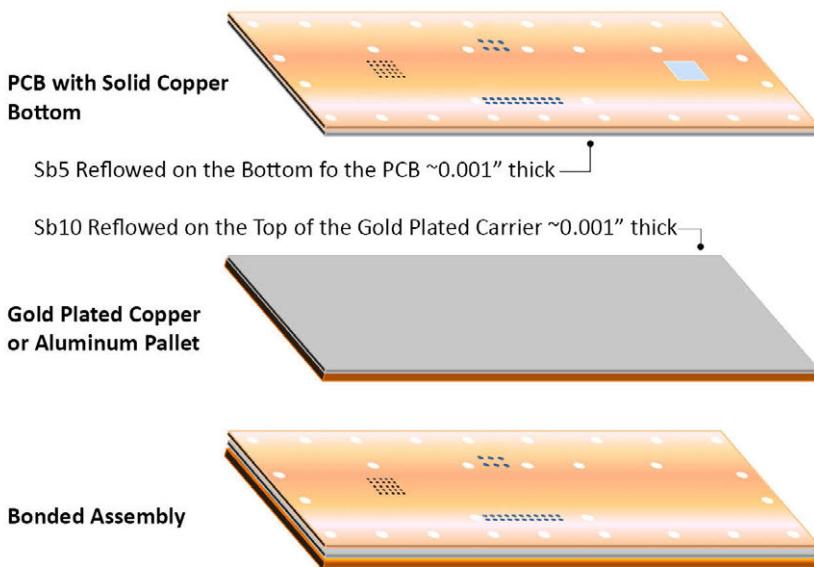


Figure 8.4: Sweat solder construction.

## Critical Design Factors

• **Solder/Paste Selection:** It is important to ensure that the solder used does not debond in subsequent component assembly operations. Some of the options that ASC has successfully used on sweat-soldering applications are:

- **Eutectic Tin/Lead**
  - Sn 63/Pb 37
  - Melting point of 183°C or 361°F

- **SAC305 RoHS Compliant**

- Sn 96.5/Cu 3.0/Ag 0.5
- Liquidus temperature of 220°C or 428°F
- Solidus temperature of 217°C or 422°F

- **Tin Antimony**

- Sn 95/Sb 5
- Liquidus temperature of 240°C or 464°F
- Solidus temperature of 235°C or 450°F

- **Sweat Solder Stencil Design:** The stencil to screen solder on the PCB or metal has to be custom designed to minimize voids, especially in the critical areas. The PCB fabricator will design this. It is preferred to screen paste on the metal; however, depending on the features of the metal, this may not be practical. In those cases, the solder is screened on the PCB.
- **Sweat Solder Fixture Design:** This is also custom designed by the PCB fabricator to help minimize solder voids and ensure good registration between the PCB and the metal. It is important to work with a fabricator that has extensive experience custom designing both stencils and fixtures.
- **Metal Selection:** Typical choices include aluminum, copper, and occasionally brass.
- **Metal Surface Finish:** If aluminum is the metal being used, it needs to at least be plated on the side being soldered since it is not possible to solder to bare aluminum.
- **PCB Surface Finish:** The following surface finishes are preferred: Ag, Au, Sn, and bare Cu.
- **Hot Vias on Ground Layer:** If there are hot vias or circuit lines on the bottom layer, they should be covered with solder mask. In addition, the metal should either be partially milled out or cut out completely.

## Sheet Film Adhesive

- Silver-Filled Conductive Epoxy Films: These are commercially available, some of which include CF3350 and Ablefilm 5025E. The PCB and metal are bonded using temperature and pressure with a sheet film adhesive.
- Silver-Filled Conductive Silicone Films: These are patented ASC materials that have some differences from the commercially-available materials. The PCB and metal are bonded using temperature and pressure with a sheet film adhesive.

Figure 8.5 shows how a sheet film bonded assembly is put together.

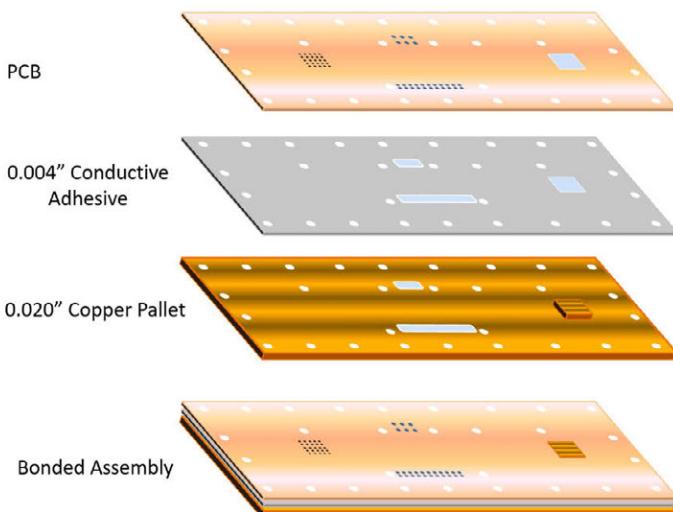


Figure 8.5: Sheet film construction.

## Critical Design Factors

- **Adhesive Selection:** There are a number of different options available, including ASC's patented material Electrasil-2. Table 8.3 compares the properties of some of the various sheet film adhesives available.
- **Bonding Fixture Design:** This is also custom designed by the PCB fabricator to help ensure there is strong adhesion between the PCB and metal, and good registration between the PCB and the metal. It is important to work with a fabricator that has extensive experience custom designing bonding fixtures. Figure 8.6 shows a typical setup of how a PCB is bonded to metal using a sheet film adhesive.

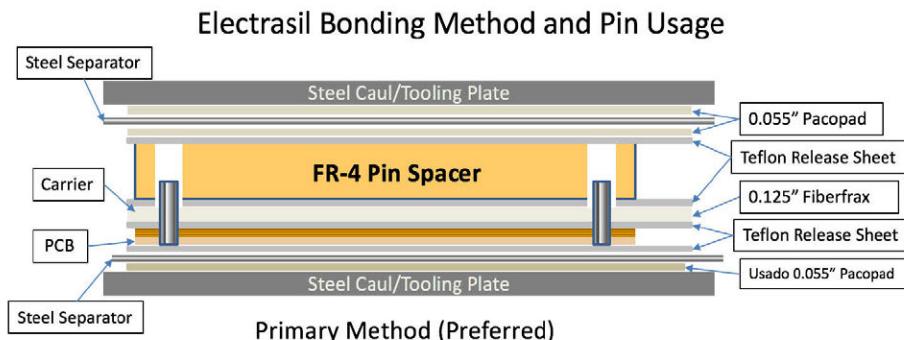


Figure 8.6: Bonding method and pin usage.

- **Metal Selection:** Typical choices include aluminum, copper, and occasionally brass.
- **Metal Surface Finish:** The metal typically needs to be plated with a metal compatible with the sheet film adhesive being utilized.
- **PCB Surface Finish:** Gold and silver tend to be preferred surface finishes. HASL or LF HASL are not acceptable surface finishes. It is also important to review the data sheets of the sheet film adhesive or discuss any specifics related to surface-finish choices with the PCB fabricator.
- **Hot Vias on Ground Layers:** If there are hot vias or circuit lines on the bottom layer, they should be covered with solder mask. In addition, the metal should either be partially milled out or cut out completely.

Material →	Electrasil-2	E&C CFC 3350	Ablefilm ECF563	Ablefilm 5025E	Sweat Solder
Thickness	3-250 mils	2-6 mils	2-6 mils	2-4 mils	1-3 mils
Cure Condition	30 min. @ 150 °C	30 min. @ 285 °C			
Thermal Conductivity, W/mK	25	7	1.7	6.5	40

Table 8.3: Post-bonding material properties.

## Final Finishes

There are a number of final finishes available for both the PCB and the metal, as illustrated in Table 8.4. Discussions with the PCB manufacturer will ensure the proper final finish is chosen for the application.

Available Final Finish	
PCB	Heat Sink
ENIG	ENIG
Electrolytic Hard	Electrolytic Hard Gold
Gold	Electrolytic Soft Gold
Electrolytic Tin	Electrolytic Silver
Electrolytic Soft Gold	Electrolytic Nickel
Immersion Silver	Electrolytic Tin
Immersion Tin	Alodine/Conversion Coat
OSP	Anodize
Bare Copper	
HASL	

Table 8.4: Available final finishes.

## Machining

From a manufacturing standpoint, machining copper, aluminum, or brass heat sinks is considerably different than machining the raw PCB. Unique tools, feeds, speeds, and precise multiple-axis control is required. A PCB manufacturer who has a dedicated machining center for this type of work will yield much better results than one that uses standard PCB fabrication equipment for machining. Figure 8.7 shows a machining center, and Figure 8.8 illustrates a few examples of aluminum- and copper-machined heat sinks.



Figure 8.7: Machining center dedicated to metal heat sinks.

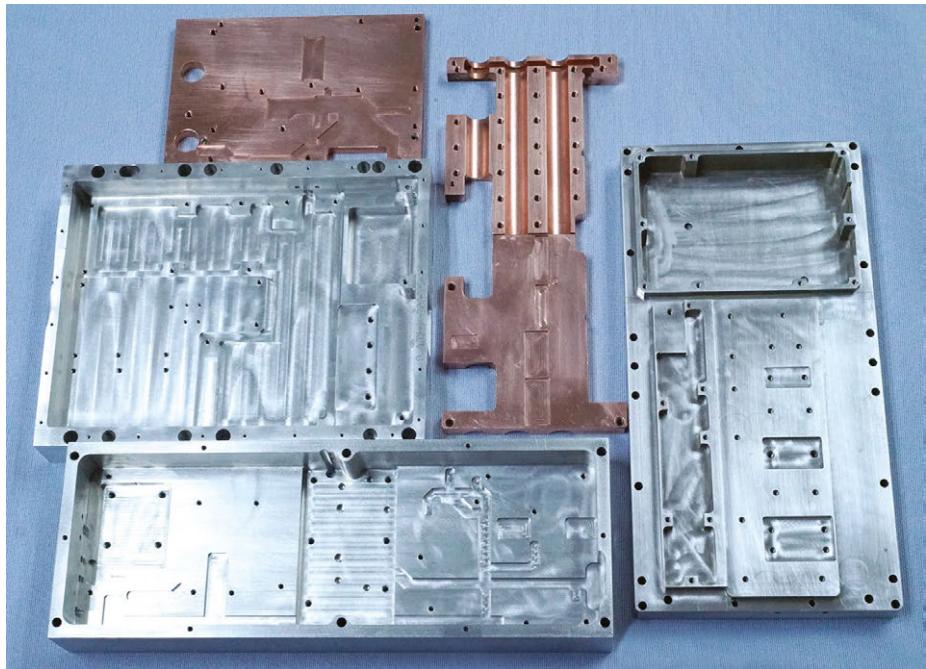


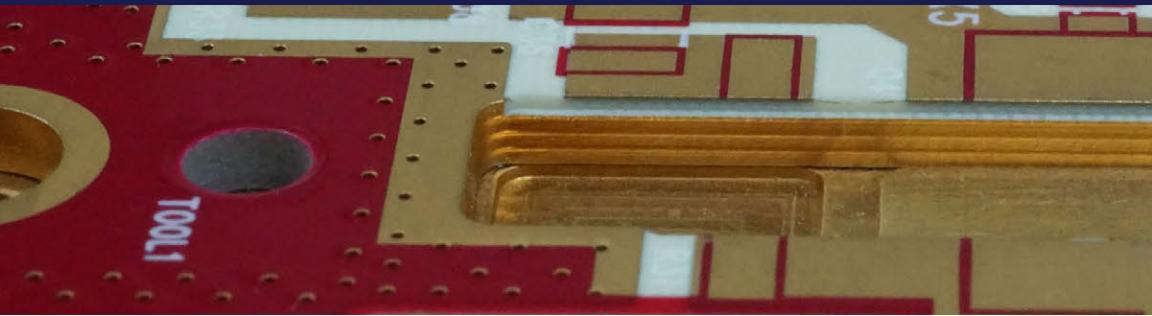
Figure 8.8: Aluminum- and copper-machined heat sinks.

## Summary

Table 8.5 presents a process comparison of the various thermal management options.

Material	Adhesive Cost	Process Notes	Ability to Bond	Electrical Performance	Rework
Electrasil-2	Lower in cost than E&C - comparable to sweat solder	Bleed or flash cleans up easily - good CTE mismatch	Good - can bond to bare metal or any metal finish	Works up to 50 GHz	Possible
E&C silver-filled epoxy		Performs well - easily lays on heat sink	Good - can bond to bare metal or any metal finish	Works up to 50 GHz	Not possible
Sweat solder	Lowest cost	Bonds at 5-10 psi	Good bond between PCB and heat sink	<ul style="list-style-type: none"> <li>Flux layer needed</li> <li>Bare Al can't bond</li> <li>Bond to Ni finish difficult</li> <li>Low volume resistivity and good grounding</li> </ul>	Not possible
Pre-bonded laminates	Most expensive	Very costly - custom fixture needed	N/A	N/A	Not possible

Table 8.5: Comparison of thermal management options.



## Conclusion

Today's RF/microwave designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing RF/microwave PCBs. In addition to the traditional military/aerospace, medical, and telecom applications, the explosion of wireless technologies in all aspects of our lives and businesses will ensure the need for high-frequency PCBs will continue to grow exponentially.

However, as has been shown in this book, there are many issues related to their design and manufacture that require proper consideration and expertise to fully address. We suggest that the key to success for those about to embark on an RF/microwave project seek early engagement and expert consultation with their PCB manufacturer.



# **References & Acknowledgements**

## **References**

- IPC-6012:** Qualification and Performance Specification for Rigid Printed Boards
- IPC-6018:** Qualification and Performance Specification for High-Frequency (Microwave) Printed Boards
- IPC-T-50:** Terms and Definitions for Interconnecting and Packaging Electronic Circuits
- IPC-4761:** Design Guide for Protection of Printed Board Via Structures

## **Acknowledgements**

The authors would like to acknowledge our RF customers and designers we have worked with over the years who have challenged us in many ways and have helped us grow in this sector. We would also like to acknowledge the various laminate suppliers in the RF sector who have helped us to better understand these materials and their applications in the RF/microwave space. In addition, we would like to thank Richard Kohn for the various photographs he has taken for this book.



# Appendices

## Appendix A: Laminates

GRADE NAME	SUPPLIER	MATERIAL TYPE	Dk (+/- tol)	DF (.0000) @ 10 GHz When Available	X	Y	Z	THICKNESS RANGE (mils)	Tol @ .020" ± mils
CuFlon	Polyflon	Pure PTFE	2.05 (.05)	4.5	129	129	129	(9x9" 2.5, 5, 1, 2, 3, 5) (12x18" 10, 15, 20, 31, 62, 125)	
NY9208	Neltec	Woven Teflon	2.08 (.02)	6	25	35	220-260	10, 15, 20, 30, 60	IPC 4103 Class B
RO4725JXR	Rogers	Hydrocarbon / Thermoset	2.55 (.05)	26	14	19	26	30, 60	
IsoClad 917	Rogers	Random Teflon	2.17 (.02)	10	31	35	236	5, 10, 15, 20, 30, 61, 125	1.5
DiClad 880	Rogers	Woven Teflon	2.17 (.02)	9	25	34	252	5, 10, 15, 20, 30, 61, 125	1.5
CuClad 217	Rogers	Woven Teflon	2.17 (.02)	9	25	34	252	5, 10, 15, 20, 30, 62, 125	1.5
NY9000	Neltec	Woven Teflon	2.17-2.20 (.02)	9	25	35	220-260	5, 10, 15, 20, 24, 31, 45, 62, 125	IPC 4103 Class B
TLY-5,5A	Taconic	Woven PTFE	2.17-2.25 (.02)	9	20	20	280	5, 10, 15, 20, 25, 31, 45, 60	1.5
RT/duroid 5880	Rogers	Random Teflon	2.20 (.02)	9	31	48	237	5, 10, 15, 20, 31, 62, 125	1
TLY-1,2,3,3A	Taconic	Woven PTFE	2.30-2.40 (.02)	12	20	20	250	5, 10, 15, 20, 25, 31, 45, 60	1.5
NY9233	Neltec	Woven Teflon	2.33 (.02)	11	25	35	220-260	5, 10, 15, 20, 24, 31, 62, 125	IPC 4103 Class B
RT/duroid 5870	Rogers	Random Teflon	2.33 (.02)	12	22	28	173	5, 10, 15, 20, 31, 62, 125	1
IsoClad 933	Rogers	Random Teflon	2.33 (.02)	14	25	28	203	5, 10, 15, 20, 30, 61, 125	1.5
DiClad 870	Rogers	Woven Teflon	2.33 (.02)	13	17	29	217	5, 10, 15, 20, 30, 60, 125	1.5
CuClad 233	Rogers	Woven Teflon	2.33 (.02)	13	17	29	217	5, 10, 15, 20, 30, 61, 125	1.5
NX9240	Neltec	Woven Teflon	2.40 (.04)	16	12	18	220-260	5, 10, 15, 20, 24, 30, 60, 125	IPC 4103 Class B
NX9245	Neltec	Woven Teflon	2.45 (.04)	16	12	18	220-260	5, 10, 15, 20, 24, 30, 60, 125	IPC 4103 Class B
TLX-6,7,8,9,0	Taconic	Woven PTFE	2.45-2.65 (.04)	18	9	12	140	5, 10, 15, 20, 25, 31, 45, 60	1.5
TLT-6,7,8,9,0	Taconic	Woven PTFE	2.45-2.65 (.05)	18	9	12	140	5, 10, 15, 20, 25, 31, 45, 60	1.5
AD250C	Rogers	Woven, Ceramic PTFE	2.50 (.04)	14	13	15	150	20, 30, 45, 60, 90, 125, 250	2

## Appendix A: Laminates (continued)

NX9250	Neltec	Woven Teflon	2.50 (.04)	17	12	18	150-200	5, 10, 15, 20, 24, 30, 60, 125	IPC 4103 Class B
DiClad 527	Rogers	Woven Teflon	2.45-2.60 (.04)	20	14	21	182	5, 10, 15, 20, 30, 60, 125	2
CuClad 250	Rogers	Woven Teflon	2.50 (.04)	20	14	21	182	5, 10, 15, 20, 30, 60, 125	2
DiClad 522	Rogers	Woven Teflon	2.50 (.05)	10	14	21	182	7, 10, 15, 20, 31, 47, 62, 125	2
CuClad 250	Rogers	Woven Teflon	2.50 (.05)	10	14	21	182	10, 15, 20, 31, 47, 62, 125	2
AD255C	Rogers	Woven, Ceramic PTFE	2.55 (.04)	14	13	15	150	30, 45, 60, 90, 125, 250	2
NX9255	Neltec	Woven Teflon	2.55 (.04)	20	12	18	150	10, 15, 20, 24, 30, 45, 60, 90, 125	IPC 4103 Class B
NorClad	Polyflon	PPO Unreinforced	2.55 (.05)	11	53	53	53	60, 90, 125, 250, 375, 500	
AD260C	Rogers	Woven, Ceramic PTFE	2.60 (.04)	14	13	15	145	30, 45, 60, 90, 125, 250	
NX9260	Neltec	Woven Teflon	2.60 (.04)	20	12	18	150-200	10, 15, 20, 24, 30, 45, 60, 90, 125	IPC 4103 Class B
NX9270	Neltec	Woven Teflon	2.70 (.04)	25	12	18	150-200	10, 15, 20, 24, 30, 45, 60, 90, 125	IPC 4103 Class B
TLC-27,30,32	Taconic	Woven PTFE	2.70-3.20 (.05)	25	9	9	70	15, 20, 31, 45, 62	1.5
EZ-10	Taconic	Woven PTFE	2.80	12	13	24	63	5, 10, 20, 30	2
TSM-DS	Taconic	Woven, Ceramic Loaded PTFE	2.85 (.05)	10	11	18	57	5, 10, 20, 30, 60, 90	
TLG-29	Taconic	BT Epoxy, Woven, Ceramic Loaded PTFE	2.87 (.05)	27	21	23	135	10, 20, 30, 60, 120	1.5
ULTRALAM 3850	Rogers	LCP	2.90 (.04)	25	17	17	150	1, 2, 4	-
TSM-29	Taconic	Woven, Ceramic Loaded PTFE	2.94 (.04)	12	23	28	78	5, 10, 20, 30, 60	1.5
NX9294	Neltec	Woven Teflon	2.94 (.04)	22	9	12	71	5, 10, 15, 20, 24, 30, 60, 125	IPC 4103 Class B
NL9294	Neltec	Woven Ceramic loaded PTFE	2.94 (.05)	17	9	12	130-150	5, 10, 20, 30, 31	IPC 4103 Class B
NH9294	Neltec	Woven Ceramic loaded PTFE	2.94 (.07)	22	9	12	100-150	5, 10, 15	IPC 4103 Class B
RT/duroid 6002	Rogers	Ceramic Teflon	2.94 (.04)	12	16	16	24	5, 10, 20, 30, 60, 120	1
CLTE (Low TCer)	Rogers	Woven Ceramic Teflon	2.94 (.04)	25	12	15	35	5, 10, 15, 20, 25, 31, 50, 62, 125	2

## Appendix A: Laminates (continued)

CLTE-XT (Low TCEr)	Rogers	Woven Ceramic Teflon	2.94 (.03)	12	8	8	20	5, 10, 15, 20, 25, 30, 60, 125	1
TLE-95	Taconic	Woven PTFE	2.95 (.05)	28	9	12	70	5, 10, 15, 20, 31, 62	1.5
IT-88GMW	ITEQ	Thermoset, Halogen-free	3.00	12	16	16	58	5, 10, 20, 30, 60	1
Astra MT, 200 Tg	Isola	Thermoset	3.00	17	12	13	55	5, 10, 20, 30, 60	
TerraGreen, 200 Tg, Halogen-free	Isola	Halogen-free	3.00	35	16	18	55	2 - 18 mil, 20, 30 and 60	
NX9300	Neltec	Woven Teflon	3.00 (.04)	30	12	18	150	10, 15, 20, 24, 30, 45, 60, 90, 125	IPC 4103 Class B
NL9300	Neltec	Woven Ceramic Loaded PTFE	3.00 (.05)	17	9	12	130-150	5, 10, 20, 30, 31	IPC 4103 Class B
NH9300	Neltec	Woven Ceramic Loaded PTFE	3.00 (.07)	23	9	12	100-150	5, 10, 15	IPC 4103 Class B
N9300-13RF	Neltec	PTFE / Thermoset Hybrid	3.00 (.04)	40	13	20	75	5, 10, 15, 20, 30, 45, 60, 90, 125	2
RO3003	Rogers	Ceramic Teflon	3.00 (.04)	12	17	17	24	5, 10, 20, 30, 60	1
CLTE-AT	Rogers	Woven Ceramic Teflon	3.00 (.04)	12	8	8	20	5+ in increments of 5 mils	1.5
IS680AG-300	Isola	Thermoset	3.00 (.05)	20	19	20	45	20, 30, 60	
TSM-DS3	Taconic	Woven, Ceramic Loaded PTFE	3.00 (.05)	13	23	28	78	5, 10, 20, 30, 60	1.5
TLG-30	Taconic	BT Epoxy, Woven, Ceramic Loaded PTFE	3.00 (.05)	27	21	23	135	10, 20, 30, 60, 120	1.5
AD300C	Rogers	Woven Ceramic Teflon	3.00 (.05)	20	12	12	125	20, 24, 31, 50, 62, 125	2
RO4730JXR	Rogers	Hydrocarbon/ Thermoset	3.00(.05)	27	11	14	21	30, 40, 60	
RO3730	Rogers	Woven Ceramic Teflon	3.00 (.06)	16	11	12	65	30, 60	1
RF-30	Taconic	Woven, Ceramic Loaded PTFE	3.00 (.07)	17	11	21	125	10, 20, 30, 60	1.5
IT-988G	ITEQ	Thermoset, Halogen-free	3.0-3.5	30	15	15	50	2-30	
IT-988GSE	ITEQ	Thermoset, Halogen-free	3.0-3.6	20	15	15	45	2-30	
I-Tera MT, 200 Tg	Isola	Thermoset	3.00 to 3.45	35	12	13	55	2 - 18, 20, 30 and 60	
Tachyon	Isola	Thermoset	3.02	21	15	16	55	2	
RO3203	Rogers	Woven Ceramic Teflon	3.02 (.04)	16	13	13	58	10, 20, 30, 60	1

## Appendix A: Laminates (continued)

N4000-13SI	Neltec	High Tg Thermoset	3.20	90	9	13	45	2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 20, 24, 28, 30, 45, 59	2
N9320-13RF	Neltec	PTFE Thermoset Hybrid	3.20 (.04)	45	13	20	70	5, 10, 15, 20, 30, 45, 60, 90, 125	2
NX9320	Neltec	Woven Teflon	3.20 (.04)	30	12	18	130	10, 15, 24, 30, 45, 60, 90, 125	IPC 4103 Class B
NL9320	Neltec	Woven Ceramic Loaded PTFE	3.20 (.05)	17	9	12	130-150	20, 30, 31	IPC 4103 Class B
NH9320	Neltec	Woven Ceramic Loaded PTFE	3.20 (.07)	24	9	12	100-150	5, 10, 15, 20	IPC 4103 Class B
AD320A	Rogers	Woven Ceramic Teflon	3.20 (.04)	30	14	14	128	20, 24, 31, 50, 62, 125	2
TLG-32	Taconic	BT Woven, Ceramic Loaded PTE	3.20 (.05)	30	8	12	61	10, 20, 30, 60, 120	1.5
RF-32	Taconic	Woven, Ceramic Loaded PTFE	3.20 (.07)	24	15	15	110	10, 20, 30, 60	1.5
N4000-13SI/-13EPSI	Neltec	High Tg Thermoset	3.20	70	10	14	45	2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 20, 24, 28, 30, 45, 59	2
XT/duriod 8000 (PEEK)	Rogers	Very High Tg Thermoplastic	3.23 (.05)	35	18	23	68	2	na
TMM-3	Rogers	Thermoset Ceramic	3.27 (.016)	16	16	16	20	15, 20, 25, 30, 40, 50, 60	1.5
TLG-33	Taconic	BT Epoxy, Woven, Ceramic Loaded PTFE	3.30 (.05)	30	8	12	61	10, 20, 30, 60, 120	1.5
XT/duriod 8100 (PEEK)	Rogers	Very High Tg Thermoplastic	3.32	38	19	21	76	2, 4	na
NH9338	Neltec	Woven Ceramic Teflon	3.38 (.04)	25	9	12	71	10, 15, 20, 24, 31, 62	IPC 4103 Class B
N9338-13RF	Neltec	PTFE / Thermoset Hybrid	3.38 (.04)	45	13	20	67	5, 10, 15, 20, 30, 45, 60, 90, 125	2
IT-8338G	ITEQ	Thermoset, Halogen-free	3.38 (.05)	25	18	18	50	10, 20, 30, 60	5-8%
RO4003C	Rogers	Hydrocarbon/Thermoset	3.38 (.05)	27	11	14	46	8, 12, 16, 20, 32, 60	1.5
IT-968	ITEQ	Thermoset	3.6	35	15	15	40	2-30	5-8%

## Appendix A: Laminates (continued)

Megtron6 R-5775K	Panasonic	PPE glass reinforced	3.4	40	15	15	45	2, 2.5, 2.9, 3.9, 5, 4.9, 5.8, 5.7, 7.8, 9.6, 11.5, 15, 19.4, 21-35	
Meteorwave 2000	Neltec	PPO glass reinforced	3.4 (3.23-3.47)	40	10	14	55	2 - 250	
N4000-20Si	Neltec	High Tg Thermoset-	3.4	60	10	14	45	2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 20, 24, 28, 30, 45, 59	2
RF-34	Taconic	Woven, Ceramic Loaded PTFE	3.40 (.07)	34	15	15	110	10, 20, 30, 60	1.5
Syron 7000	Rogers	Very High Tg Thermoplastic	3.40(.05)	45	18	23	68	2	-
IT-8350G	ITEQ	Thermoset	3.5(.05)	25	15	15	45	10, 20, 30,60	5-8%
RO4350	Rogers	Hydrocarbon/Thermoset	3.48 (.05)	40	14	16	50	7, 10, 20, 30, 60	1.5
RO4835	Rogers	Hydrocarbon/Thermoset	3.48 (.05)	37	11	9	26	6.6, 10, 13.3, 16.6, 20, 23.3, 30, 40, 60	
NH9348	Neltec	Woven Ceramic Loaded PTFE	3.48 (.10)	30	9	12	100-150	10, 15, 20, 30, 31, 45, 60, 62, 125	IPC 4103 Class B
NL9350	Neltec	Woven Ceramic Loaded PTFE	3.50 (.05)	17	9	12	130-150	20, 30, 31	IPC 4103 Class B
NH9350	Neltec	Woven Ceramic Loaded PTFE	3.50 (.10)	30	9	12	100-150	10, 15, 20, 30, 31, 45, 60, 62, 125	IPC 4103 Class B
Meteorwave 4000	Neltec	PPO Glass Reinforced	3.5 (3.29-3.63)	25	10	14	55	2 - 250	
Meteorwave 3350	Neltec	PPO Glass Reinforced	3.5	48	10	14	55	6.8, 10, 12, 20, 30, 60	
M-Ply	Neltec	PPO Glass Reinforced	3.26 - 3.29	48	10	14	55	2.7, 4.0	
N4350-13RF	Neltec	RF Thermoset	3.50 (.04)	65	10	14	70	4, 5, 6, 7, 8, 10, 12, 14, 20, 30, 60	2
N9350-13RF	Neltec	PTFE / Thermoset Hybrid	3.50 (.04)	55	13	20	67	5, 10, 15, 20, 30, 45, 60, 90, 125	2
N8000	Neltec	Cyanate Ester	3.50 (.05)	70	11	13	50	3, 4, 5, 6, 8, 10, 12, 14, 20, 24, 30, 45, 59	2.5
TLG-35	Taconic	BT Epoxy, Woven, Ceramic Loaded PTFE	3.50 (.05)	30	8	12	61	10, 20, 30, 60, 120	1.5
RF-35TC	Taconic	Ceramic Teflon	3.50 (.05)	11	11	13	34	5, 10, 20, 30, 60	
RO3035	Rogers	PTFE/Ceramic	3.50 (.05)	17	17	17	24	5, 10, 20, 30, 60	1.5
RT/duroid 6035HTC	Rogers	PTFE/Ceramic	3.50 (.05)	13	19	19	39	10, 20, 30, 60	

## Appendix A: Laminates (continued)

RF-35A2	Taconic	Woven, Ceramic Loaded PTFE	3.50 (.05)	16	10	13	106	10, 20, 23, 30, 60	1.9
RF-35	Taconic	Woven, Ceramic Loaded PTFE	3.50 (.10)	18	19	24	64	10, 20, 23, 30, 60	1.5
AR 350	Rogers	Woven Ceramic Teflon	3.50 (.15)	25	33	34	107	5, 10, 15, 20, 24, 31, 50, 62, 125	2
AD350A	Rogers	Woven Ceramic Teflon	3.50(.05)	30	5	9	35	20, 30, 60, 125	15
TC350 (Thermally Conductive)	Rogers	Woven Ceramic Teflon	3.50(.05)	25	8	8	17	20, 60, 125	15
N7000-2 HT/ N7000-3 HT	Neltec	Thermoset Polyimide-Toughened	3.50	90	12	15	15	3, 5, 10, 14, 21, 28, 44, 59	2
25FR Laminate & Prepreg	Arlon	Ceramic Olefin	3.58(.06)	35	16	16	59	10, 12, 18, 20, 24, 30, 60, 125	2
Megtron7 R-5785	Panasonic	PPE Glass Reinforced	3.61	30	15	15	42		
IT-958G	ITEQ	Thermoset, Halogen-free	3.6	70	15	15	45	2-30	IPC
IT-150DA	ITEQ	Thermoset	3.6	70	15	15	45	2-30	IPC
I-Speed, 180 Tg	Isola	Thermoset	3.63	71	16	18	55	2 - 60	
IT-200LK	ITEQ	Thermoset Mid Loss	3.6	90	16	16	46	2-30	IPC
IT-170GRA1	ITEQ	Thermoset Mid Loss	3.7	95	15	15	45	2-30	IPC
FR408 180 Tg	Isola	Thermoset	3.65	120	13	13	65	3, 5, 10, 14, 21, 28, 31, 44, 59, 62, 93, 125	2
FR408HR, 200Tg	Isola	Thermoset	3.65	95	16	18	55	2 - 60	
Meteorwave 1000	Neltec	PPO Glass Reinforced	3.7 (3.32-3.97)	55	10	14	55	2-250	
N4000-13/-13EP	Neltec	High Tg Thermoset	3.70	75	10	14	45	2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 20, 24, 28, 30, 45, 59	2
N4000-20	Neltec	High Tg Thermoset	3.8	75	10	14	45	2, 3, 4, 5, 6, 7, 8, 10, 12, 14, 20, 24, 28, 30, 45, 59	2
FR406 170 Tg	Isola	Thermoset	3.8	160	13	13	65	3, 5, 10, 14, 21, 28, 31, 44, 59, 62, 93, 125	2
Megtron4 R-5725	Panasonic	PPE Glass Reinforced	3.8	50	13	14	35	2, 2.5, 2.9, 3.9, 5, 4.9, 5.8, 5.7, 7.8, 9.6, 11.5, 15, 19.4, 21, 35	
Meteorwave 3000	Neltec	PPO Glass Reinforced	3.8 (3.40-4.04)	48	10	14	55	2-250	
N4380-13RF	Neltec	RF Thermoset	3.80 (.04)	70	10	14	70	4, 5, 6, 7, 8, 10, 12, 14, 20, 30, 60	2

## Appendix A: Laminates (continued)

Generic FR4 140 Tg	Various	Thermoset	3.9	150	10	14	14	3, 5, 10, 14, 21, 28, 31, 44, 59, 62, 93, 125	2
N4000-7 170 Tg	Neltec	Thermoset	3.90	150	14	15	4	3, 5, 10, 14, 21, 28, 31, 44, 59, 62, 93, 125	2
N7000-1	Neltec	Thermoset Polyimide	3.90	95	12	15	15	3, 5, 10, 14, 21, 28, 44, 59	2
185HR, 180 Tg	Isola	Thermoset	4.00	190	13	13	45	2.5 - 0.059	
AD410	Rogers	Woven, Ceramic Loaded PTFE	4.10 (.06)	30	9	9	40	30, 62, 75, 120, 125, 250	
RF-41	Taconic	Woven, Ceramic Loaded PTFE	4.10 (.10)	38	9	12	93	60, 125	N/A
370HR 180 Tg	Isola	Thermoset	4.17	210	13	13	45	3, 5, 10, 14, 21, 28, 31, 44, 59, 62, 93, 125	2
180A	ITEQ	Thermoset	4.10	200	13	13	40	2-30	
N4000-29	Neltec	Thermoset- Epoxy HighTg, Lead-Free	4.10	160	12	15	15	2-250	2
N4000-6/- 6FC	Neltec	Thermoset- Epoxy HighTg	4.30	230	12	15	15	2-250	2
AD430	Rogers	Woven, Ceramic Loaded PTFE	4.30 (.06)	30	9	9	40	30, 62, 75, 120, 125, 250	
RF-43	Taconic	Woven, Ceramic Loaded PTFE	4.30 (.10)	33	9	11	96	10, 20, 30, 62, 125	1.9
R-1755V 170 Tg	Panasonic	Thermoset	4.4	16	12	14	44	2, 2.7, 3, 3.2, 3.5, 3.7, 4, 4.5, 5, 5.3, 6, 7, 7.5, 8, 10, 12, 145, 155, 18, 21, 18, 35, 39, 47, 59	
TMM-4	Rogers	Thermoset Ceramic	4.50 (.045)	17	14	14	20	15, 20, 25, 30, 40, 50, 60	1.5
RF-45	Taconic	Woven, Ceramic Loaded PTFE	4.50 (.10)	37	9	13	96	20, 31, 62, 125	1.9
AD450A	Rogers	Woven Ceramic Teflon	4.50 (.10)	30	9	9	40	78, 93, 98, 117, 125, 160, 250	2
AD450	Rogers	Woven Ceramic Teflon	4.50 (.20)	35	9	11	42	10+ by 10 mil increment	2
TMM 6	Rogers	Thermoset Ceramic	6.00 (.08)	18	16	16	20	15, 20, 25, 30, 40, 50, 60	1.5

## Appendix A: Laminates (conclusion)

AD600	Rogers	Woven Ceramic Teflon	6.00 (.40)	3	11	10	45	10, 15, 20, 24, 31, 50, 62, 125	15
RO3006	Rogers	Ceramic Teflon	6.15 (.15)	25	17	17	24	5, 10, 25, 50	1
RT/duriod 6006	Rogers	Ceramic Teflon	6.15 (.15)	19	34	47	117	10, 25, 50, 75, 100	1
RO3206	Rogers	Woven Ceramic Teflon	6.15 (.15)	27	13	13	34	25, 50	
RF-60A	Taconic	Woven, Ceramic Loaded PTFE	6.15 (.20)	28	9	8	69	10, 25, 31, 50, 60, 125	1.9
RO4360G2	Rogers	Hydrocarbon, Ceramic, Glass Reinforced	6.15(.15)	38	17	15	30	8, 12, 16, 20, 32, 60	
TC600 (Thermally Conductive)	Rogers	Woven Ceramic Teflon	6.15(15)	2	9	9	35	10, 15, 20, 25, 30, 60, 125	15
RO2808	Rogers	Fluoropolymer Composite	7.60 (.35)	15	30	30	23	Jan-00	-
TMM-10	Rogers	Thermoset Ceramic	9.20 (.23)	17	16	16	20	15, 20, 25, 30, 40, 50, 60	1.5
TMM-10i	Rogers	Thermoset Ceramic	9.80 (.25)	15	16	16	20	15, 20, 25, 30, 40, 50, 60	1.5
AD1000	Rogers	Woven Ceramic Teflon	10.0 (.35)	23	8	10	20	5, 10, 15, 20, 24, 31, 50, 62, 125	2
CER-10	Taconic	Woven, Ceramic Loaded PTFE	10.0 (.50)	35	13	15	46	15, 25, 47, 50, 62	1.9
RO3210	Rogers	Woven Ceramic Teflon	10.2 (.05)	30	13	13	34	25, 50	1
RT/duriod 6010LM	Rogers	Ceramic Teflon	10.2 (.25)	20	24	24	24	10, 25, 50, 75, 100	1
RO3010	Rogers	Ceramic Teflon	10.2 (.30)	35	17	17	24	5, 10, 25, 50	1
RF-10	Taconic	Woven Ceramic Teflon	10.2 (.30)	25	16	20	25	10, 20, 25, 60, 125	2
TMM-13i	Rogers	Thermoset Ceramic	12.85 (.35)	19	19	19	20	15, 20, 25, 30, 50, 60, 75, 100, 125, 150, 200, 250, 275, 300, 500	1.5

## Appendix B: Prepreg/Bonding Films

PREPREG NAME	SUPPLIER	RESIN SYSTEM	Dk @ 10 GHz	Diss Factor (.0000)	Tg Deg C	Td Deg C	Cure Stage	THICKNESS RANGE (mils)	Flow
NY9205BP	Park	Thermoplastic	2.05	0.0007				260-270°C	50µm
FEP	Dupont	PTFE	2.2	70	500	-	Plastic	1.5, 2.0	Flow
3001	Rogers	Chloro-Fluorocopolymer	2.28	30	186	-	Plastic	1.5	Flow
CuClad 6250	Rogers	Polyethylene / Polyolefin blend	2.32	13	102	-	Plastic	1.5	Flow
CuClad 6700	Rogers	Chloro Tri-Fluoro Ethylene	2.35	25	186	-	Plastic	1.5, 3.0	Flow
HT1.5	Taconic	PCTFE	2.35	25	-	-	-	1.5	N/A
NX9240BP	Park	Thermoplastic	2.40	0.0025				205_210°C	50µm
fastRise 27 (FR-27)	Taconic	Thermoset	2.7	14	188	376	B	4, 4.5, 5	Flow
GenClad 280 Prepreg	Rogers	Thermoset	2.8	20	190	460	B	2.6, 3.4	Low Flow
TLG-29	Taconic	BT/Epoxy/PTFE	2.87	27	165	300	B	5	Flow
2929	Rogers	Ceramic Filled HydroCarbon	2.94	30	170	400	B	1.5, 2.0, 3.0	Flow
IT-88GMW	ITEQ	Thermoset, Halogen Free	3.00	12	180	405	B	(TBD, likely 2.0 to 6.0)	Flow
IT-98BGSE	ITEQ	Thermoset, Halogen free	3.0-3.6	14	190	405	B	1.7 to 6.0	Flow
IT-980G	ITEQ	Thermoset, Halogen free	3.0-3.5	30	190	405	B	1.7 to 6.0	Flow
TPG-30	Taconic	BT/Epoxy/PTFE	3.0	38	165	300	B	5	Flow
TPG-30	Taconic	BT Epoxy,Woven, Ceramic Loaded PTFE	3.00	38	21	23	28	4.5, 5	N/A
IT-8338G	ITEQ	Thermoset, Halogen Free	3.38(.05)	25	>190	405	B	10, 20, 30,60	Flow
M-Ply	Park		3.00 to 3.4	21	200				
I-Tera MT	Isola	Thermoset	3.00 to 3.45	35	200	360	B	2.0, 2.2, 2.5, 3.0, 3.4, 3.5, 3.8, 4.0, 4.2, 4.3, 4.5, 5.0, 5.6, 6.1	Flow
TerraGreen Halogen Free	Isola	Halogen Free	3.00 to 3.45	35	200	390	B	2.0, 2.2, 2.5, 3.0, 3.4, 3.5, 3.8, 4.0, 4.2, 4.3, 4.5, 5.0, 5.6, 6.1	Flow
IT-968	ITEQ	Thermoset	3.6	35	185	400	B	1.7 to 6.0	Flow
Megtron6 R-5670	Panasonic	PPO/PP Glass Reinforced	3.19-3.61	40	185	410	B	2.4, 2.7, 2.9, 3.0, 3.4, 3.5, 3.9, 4.1, 4.2, 4.6, 4.9, 5.2	Flow
TacLam TL-32	Taconic	BT/Epoxy/PTFE/Ceramic	3.2	30	128	300	B	4.5, 5	Flow
N4000-13SI	Neltec	Epoxy	3.3	70	210	385	B	1.5, 2.5, 4.0	Flow
N4350-13	Neltec	Epoxy	3.5	65	210	365	B	5	Flow
TacLam TL-35	Taconic	BT/Epoxy/PTFE/Ceramic	3.5	30	128	300	B	4.5, 5	Flow
TPG-35	Taconic	BT Epoxy,Woven, Ceramic Loaded PTFE	3.50	40	21	23	28	4.5	N/A
IT-8350G	ITEQ	Thermoset	3.5(.05)	25	>190	405	B	(TBD, likely 2.0 to 6.0)	Flow
RO4450F	Rogers	Ceramic Filled HydroCarbon/glass reinforced	3.54	40	280	390	A	4	Low Flow
Megtron4 R5620	Panasonic	PPO/PP Glass Reinforced	3.57	80	176	360	B	2.0, 2.3, 2.8, 3.0, 3.4, 3.5, 4.0, 4.1, 4.6, 4.8, 5.0, 5.5,	Flow
IT-958G	ITEQ	Thermoset, Halogen Free	3.60	70	175	400	B	2.0 to 6.0	Flow
IT-150DA	ITEQ	Thermoset	3.60	70	180	370	B	2.0 to 8.0	Flow
IT-200LK	ITEQ	Thermoset mid loss	3.60	90	200	370	B	2.1 to 5.1	Flow
Megtron7 R5680	Panasonic	PPP Glass Reinforced	3.61	30	200	400	B	1.9, 2.7, 2.9, 3.0, 3.5, 3.9, 4.1, 4.2, 4.6, 5.2	Flow
I-Speed	Isola	Thermoset	3.63	71	180	360	B	2.0, 2.3, 2.4, 2.6, 2.7, 3.0, 3.2, 3.4, 3.5, 3.9, 4.0, 4.1,	Flow
IT-170GRA1	ITEQ	Thermoset mid loss	3.70	75	180	380	B	2.0 to 8.0	Flow
FR408	Isola	Thermoset	3.65	120	180	360	B	2.4, 3.2, 3.5, 4.0, 4.1, 4.5, 5.2, 6.0, 7.5	Flow
FR408HR	Isola	Thermoset	3.65	95	200	380	B	2.0, 2.3, 2.7, 3.2, 3.5, 4.0, 4.1, 4.2, 4.8, 4.9, 5.4	Flow
N4000-13	Neltec	Epoxy	3.7	80	210	365	B	1.5, 2.5, 3.3, 4.0, 7.0	Flow
IS620	Isola	Epoxy	3.79	89	215	363	B	3.0, 4.0, 5.4, 6.0	Flow
FR406	Isola	Epoxy	3.8	160	170	300	B	1.5, 2.5, 3.3, 4.0, 7.0	Flow
N4350-18	Neltec	Epoxy	3.8	70	210	385	B	5	Flow
R1650V	Panasonic	Thermoset	3.9	23	173	350	B	2.0, 2.2, 2.4, 2.5, 2.6, 3.0, 3.1, 3.2, 3.5, 3.6, 3.7, 3.9, 4.1, 4.3, 4.8, 5.2, 5.5, 6.9, 7.6, 8.1	Flow
185HR	Isola	Phenolic Epoxy	4	190	170	340	B	2.5, 3.2, 3.9, 4.2, 4.4, 5.1, 6.0, 7.7, 8.2	Flow
180A	ITEQ	Thermoset	4.10	200	175	345	B	2.0 to 8.6	Flow
370HR	Isola	Phenolic Epoxy	4.17	210	170	340	B	2.3, 2.5, 2.7, 3.0, 3.1, 3.5, 3.6, 3.8, 4.0, 4.8,	Flow
FR406N	Isola	Epoxy	4.3	250	165	300	B	1.7, 2.7, 4.5	Low Flow

# Glossary

**Anisotropic:** Material with properties that change with direction along the object. Common examples of anisotropic materials are wood and composites.

**Base Material:** Insulating material upon which a conductive pattern may be formed.

**Dielectric Constant (Dk):** The measure of the capacitance or energy between a pair of conductors in the vicinity of the laminate compared to that pair of conductors in a vacuum.

**Dielectric Material:** A material with a high resistance to the flow of current.

**ED Copper:** Electrodeposited copper is less flexible than RA copper and is typically used to manufacture rigid boards.

**Flame Retardant Material:** A material that is capable of achieving a UL rating of 94-VO.

**Grain Direction:** In rolled annealed copper, the grain direction results from the rolling and annealing process. The raw laminate supplier always sells the raw material with the grain direction indicated.

**Homogeneous Material:** A material of uniform composition throughout that cannot be mechanically separated into different materials. Examples of homogeneous materials include certain types of plastics, ceramics, glass, metals, alloys, paper, board, resins, and coatings.

**Hot Via:** A thermal via that carries heat away from power devices, which are typically used in arrays of about a dozen.

**Impedance:** The measure of the opposition that a circuit presents to a current when voltage is applied.

**Isotropic Material:** Material having identical values of a property in all directions. Glass and metals are examples of isotropic materials.

**Laminate:** The plastic material, usually reinforced by glass or paper, that supports the copper cladding from which circuit traces are created.

**Loss Tangent:** A measure of how much of the signal pulse (electromagnetic wave) propagating down the PCB transmission line will be lost in the dielectric region (insulating material between copper layers).

**Microstrip:** A type of transmission line configuration that consists of a conductor over a parallel ground plane, separated by a dielectric.

**Microwave:** The portion of the electromagnetic spectrum between the far infrared and conventional radio-frequency range. The microwave frequency range extends from 1 GHz to 300 GHz.

**No/Low-Flow Prepreg:** Prepregs that are uniquely formulated to have limited and controlled flow.

**Pad Cratering:** A mechanically induced fracture in the resin between the copper foil and outermost layer of fiberglass of a PCB. It may be within the resin or at the resin-to-fiberglass interface.

**Prepreg:** Glass cloth that has been pre-impregnated with a thermosetting resin used for making rigid circuits.

**RA Copper:** Rolled annealed copper is much more flexible than ED copper, and is required for dynamic-flexing applications.

**Registration:** The degree of conformity of the true position of a pattern with its intended position, or with that of any other conductor layer of a board.

**RF:** Radio frequency.

**Sequential Lamination:** A set of multilayer layers processed as sub-assemblies to be laminated together; typically used to construct blind or buried vias.

**Signal Integrity:** A set of measures of the quality of an electrical signal.

**Skin Depth:** Penetration of the signal into the trace is measured in skin depths with approximately 66% of the energy penetrating to one skin depth and about 97% of the energy penetrating to three skins depths.

**Skin Effect:** The tendency of a signal transmission to have the largest distribution near the surface of the conductor, and decreasing distribution through greater depths in the conductor.

**Solder Mask:** A thin lacquer-like layer of polymer that is usually applied to the copper traces of a printed circuit board for protection against oxidation, and to prevent solder bridges from forming between closely-spaced solder pads.

**Stripline Circuit:** A stripline circuit has a trace layer that is sandwiched between two parallel ground planes with a dielectric in between.

**Thermosetting Resin:** Thermosetting resin is a material that hardens when heated and cannot be remolded, softened, or reshaped by subsequent heating.



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