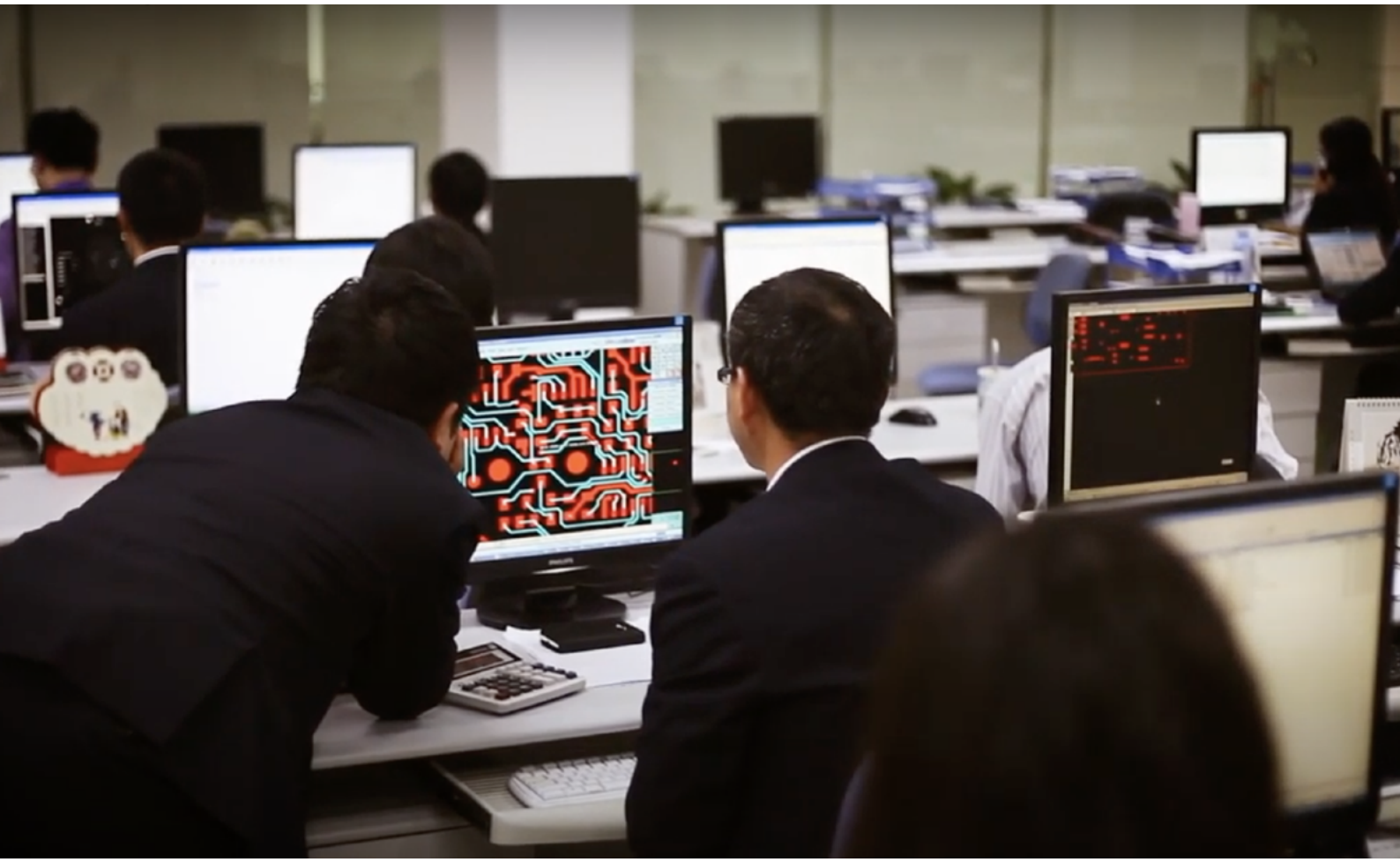


PCB Design Checklist

Once a new PCB has been designed it's time to start production, right? While it's understandable that it may be the highly-anticipated next step, we caution all designers to take some time to first take a look and make sure the critical areas of the design are covered. Is your soldermask larger than the component pad? Have you considered any possible mechanical assembly problems using a 3D model of the assembly? This is why we created the PCB Design Checklist. This checklist can aid you in your own design work. Alongside our PCB Design Guidelines, this will provide a total solution to further help you get it right from the start.

CHECKLIST

1 **Component Packaging**
2 **Placement Check**
3 **Mechanical Check**
4 **Technical Check**
5 **Constraint Rules**
6 **Routing Check**
7 **Timing Design**
8 **Power Design Check**
9 **DRC Check**
10 **Test Pin**
11 **Silkscreen Check**
12 **Gerber Review**

1 Component Packaging

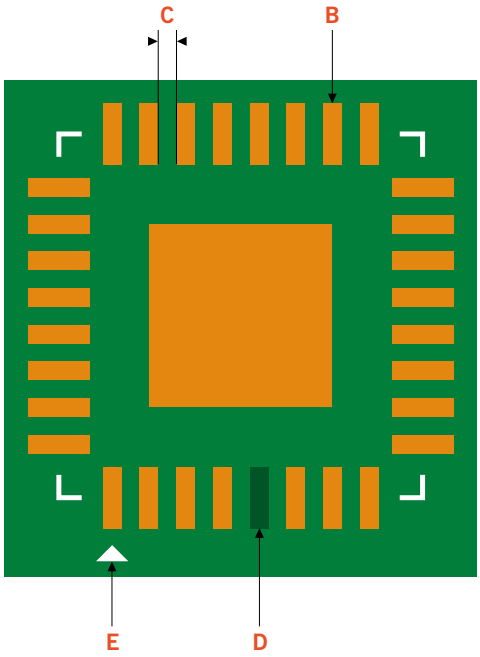
A SMD component must have solder mask and paste mask layers.

B Solder mask must be larger than the component pad by at least 0,05 mm (for NCAB advanced tech non-solder mask defined pads).

C Solder mask web between component pads must be at least 4 mils for green solder mask, 0,127 mm for black or white.

D Paste mask should be the same size as the component pad.

E A pin 1 marker must be present on the silkscreen layer to show component orientation.



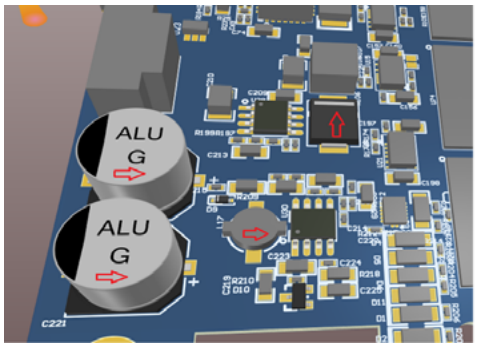
2 Placement Check

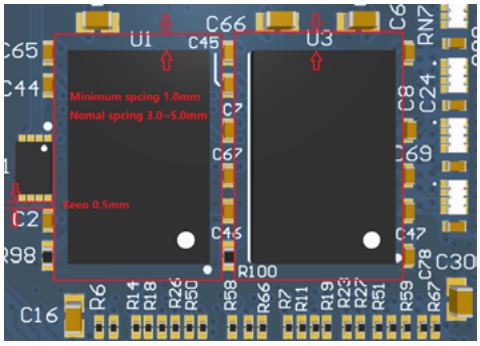
A Confirm component to component spacing is within assembly house capability and meets mechanical drawing requirements (If provided).

B Confirm component placement matches component polarity (Positive “+” Pad to Positive “+” Pad, Negative “-” Pad to Negative “-” Pad).

C Make sure larger components allow space for rework / repair (Example BGA, QFN, Connectors). Graphic shows 1.5 mm keep out around BGA.

D Ensure functional circuit layout meets PI, SI, and EMC requirements.





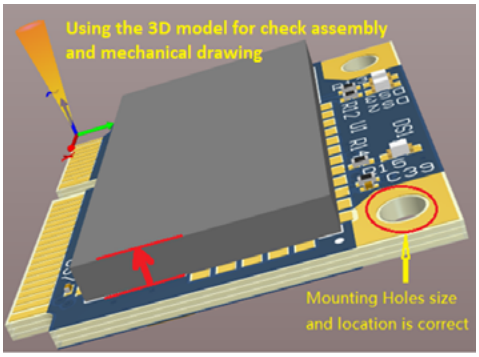
3 Mechanical Check

A Identify any mechanical assembly problems using a 3D model of the assembly.

B Make sure components origin and height are consistent with the mechanical drawing.

C Ensure mounting hole size and location is correct to provided mechanical drawing or industry standard.

D Ensure mechanical drawing version is up to date and correct.



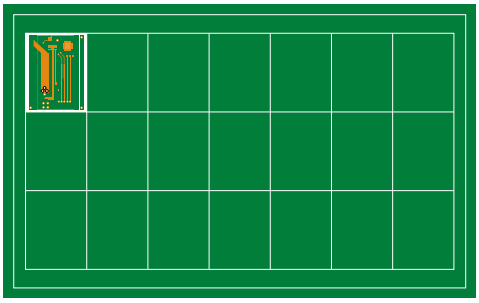
C

4 Technical Check

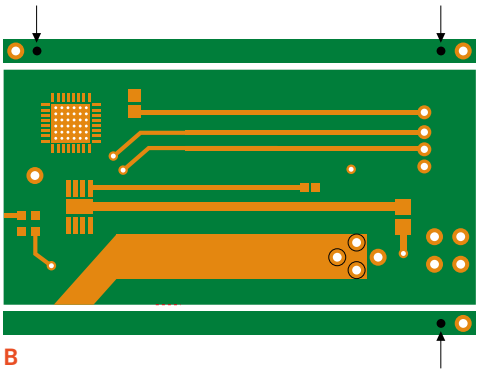
A Board size less than 50 mm X 50 mm must be panelized or in an array. Example Circuit size 24 mm X 40 mm, Panel size 48 mm X 120 mm, Panelisation = 222 Circuits / 37 Panels, with utilization of 76.5%".

B Ensure 3 global mark points/fiducials are present on the panel edges, 5 mm from the edge, not in a v-score or mill route path, oriented in an "L" shape with solder mask clearances for each one.

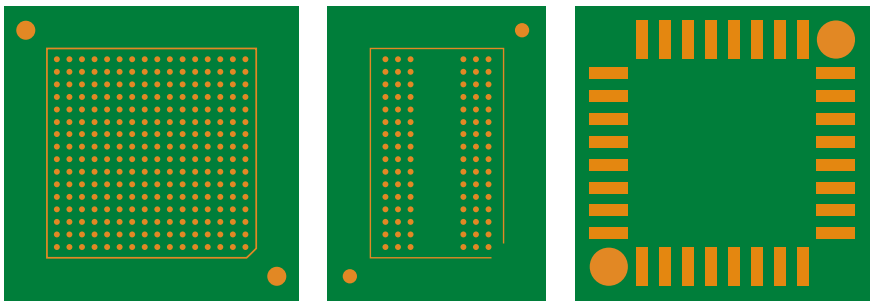
C Ensure large components (BGA, QFP, QFN) have corner mark points/fiducials.



A



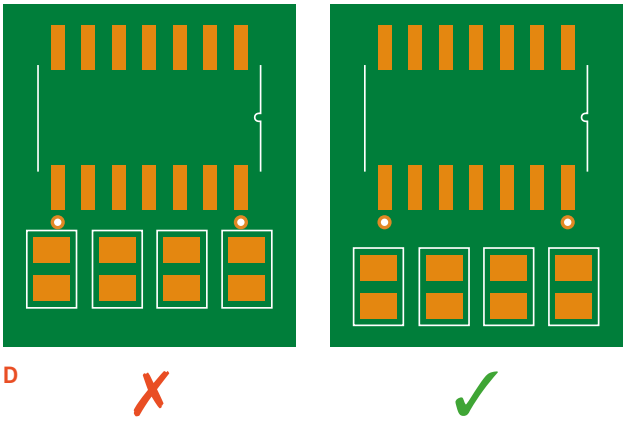
B



C

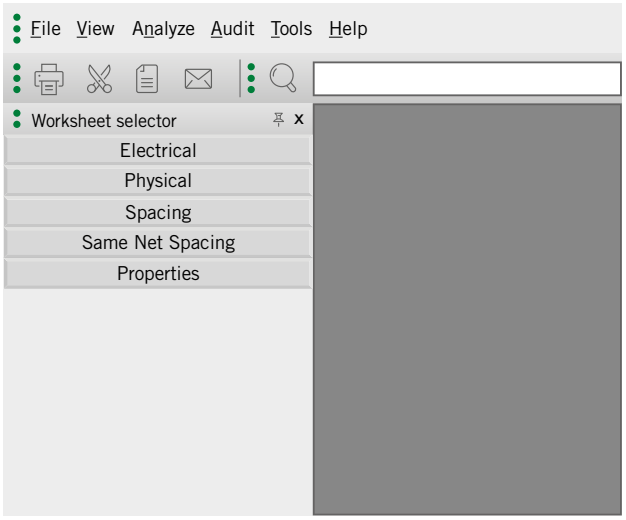
4 Technical Check

D Check component footprint placement to ensure components do not overlap or interfere with the placement of other components.



5 Constraint Rules

A Confirm the constraints rules of the “Spacing”, “Electrical”, and “Same Net Spacing” which can be set according to design tools.



6 Routing Check

A High speed signals routed with shortest possible length to maintain SI.

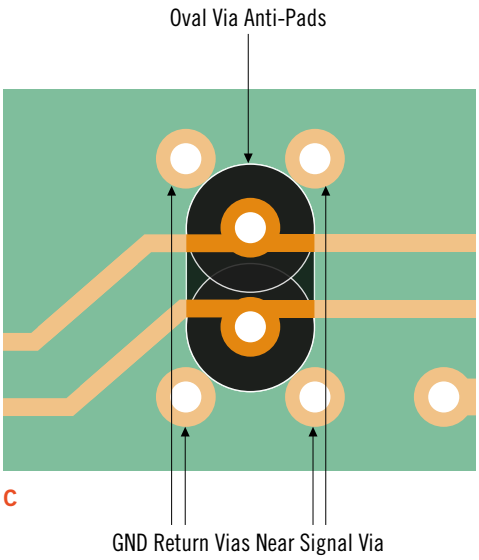
B High speed signals use as few vias transitions as possible to maintain SI (2 or fewer vias recommended).

C Ensure that each high speed via transition has return path stitching via's for GND reference.

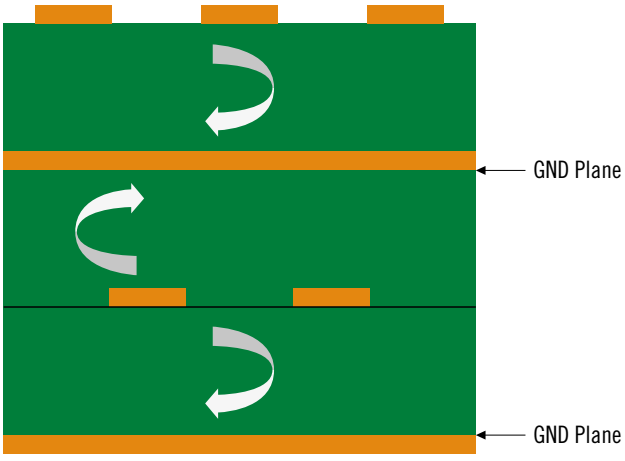
D Ensure impedance requirements are clearly defined.

E Ensure there is a gap between important signal lines that matches the space rule. This improves SI and field coupling between signals lines.

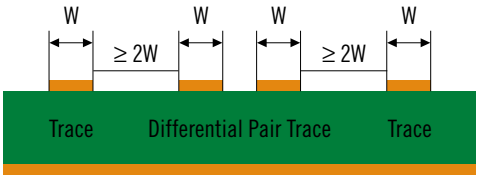
F Ensure correct impedance control details are present.



C



D



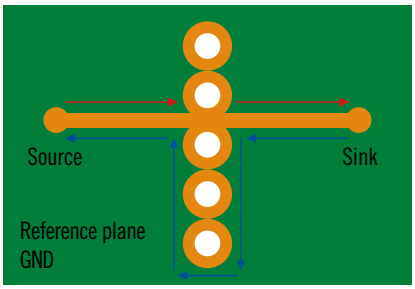
E

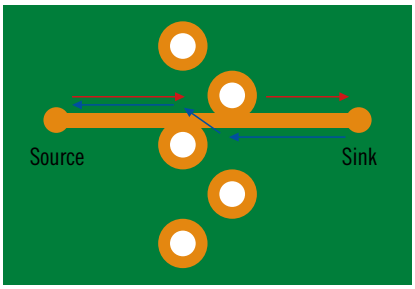
Signal Type	Impedance (ohm)	Single/Differential
General Single	50	Single
General Diff	100	Differential
USB	90	Differential
PCIE3.0	85	Differential
Video signal	75	Single
RF signal	50	Single

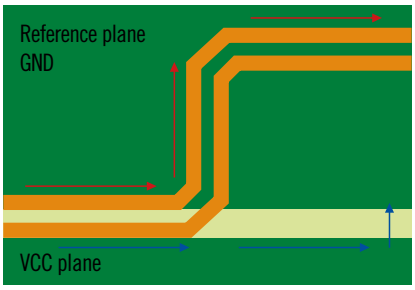
F

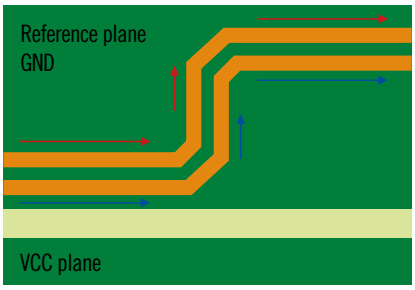
6 Routing Check

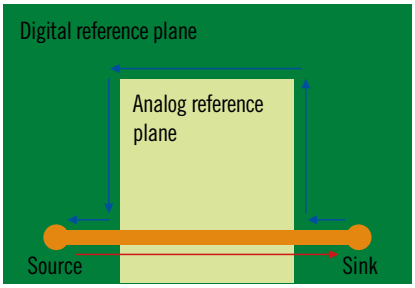
G Ensure that signals are routed over solid reference planes with no voids.

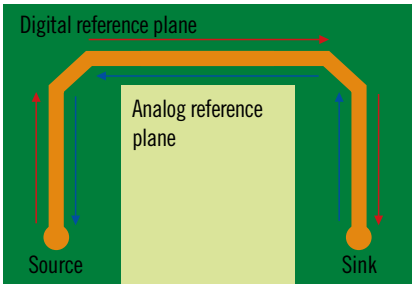












✗ ✓

7 Timing Design

Time delay requirements

A Check the length rules are set correctly to match design requirements.

B When differential length tuning high speed signals, ensure the clearance meets the x4 line width rule.

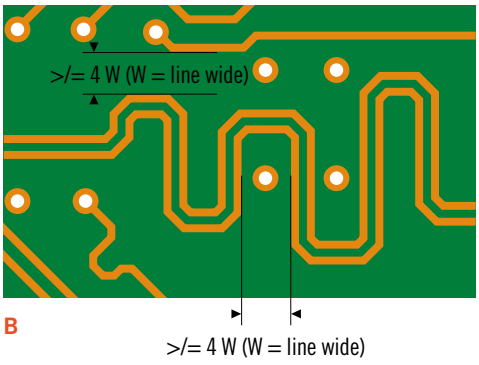
Length matching

C If available, check that the Pin Delay of a component is correctly configured.

Delay (length match)

Bus/frequency (Mhz)	Tolerance (mil)
100-200 Mhz (bus)	+/-300
300-500 Mhz (bus)	+/-200
2500 Mhz (Differential Pair)	+/-5
≥5000 Mhz (Differential Pair)	+/-1

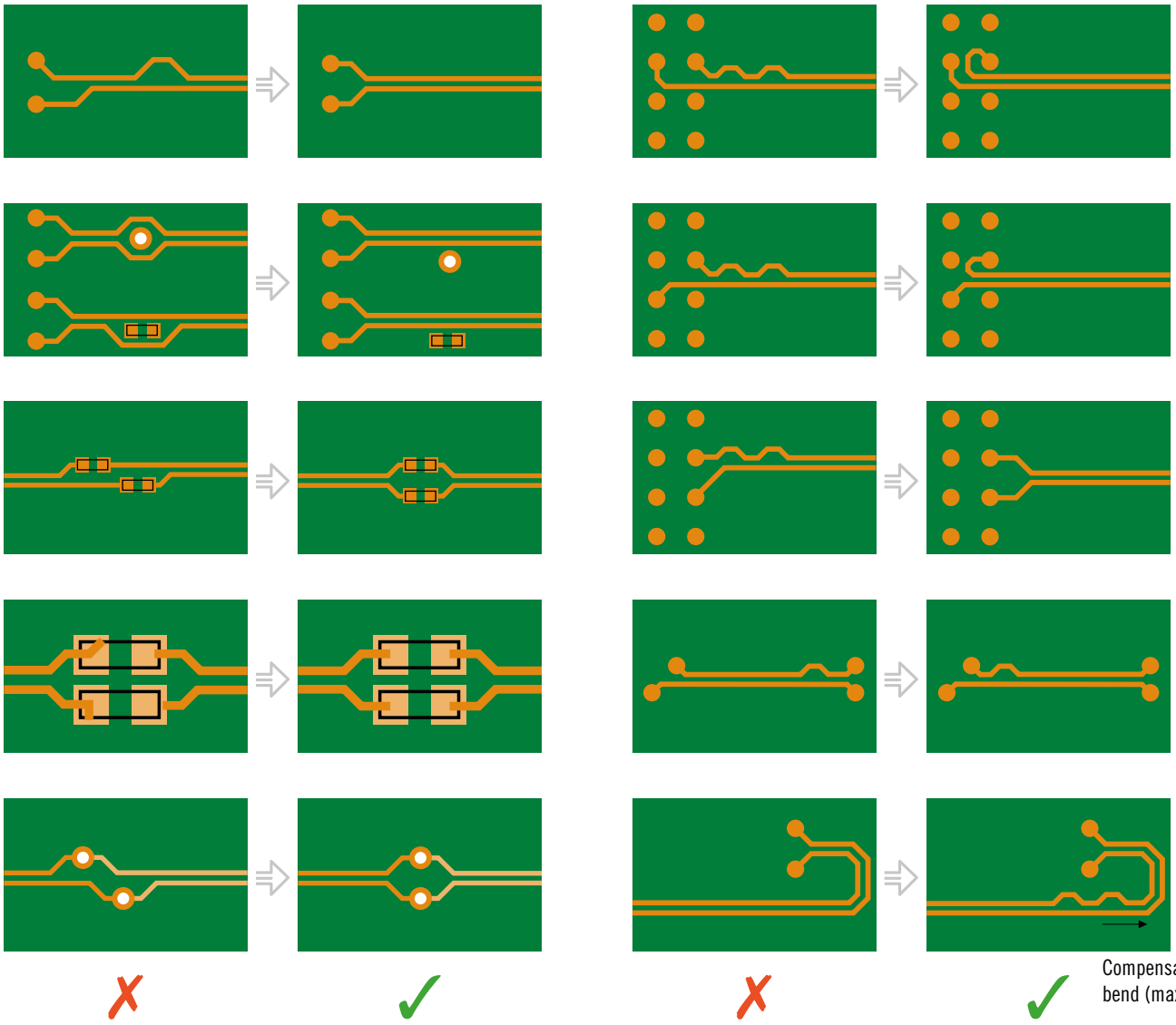
A



B

7 Timing Design

D Ensure that the length of the traces meet the rule requirements as stated above. This can be accomplished using length/delay tuning following the guidelines below.



8 Power Design Check

A Check if the copper weight and line width can support the current carrying capacity required.

Copper thickness & Electric current					
35um		50um		70um	
Trace width(mm)	Electric current(A)	Trace width(mm)	Electric current(A)	Trace width(mm)	Electric current(A)
0.15	0.2	0.15	0.5	0.15	0.7
0.2	0.55	0.2	0.7	0.2	0.9
0.3	0.8	0.3	1.1	0.3	1.3
0.4	1.1	0.4	1.35	0.4	1.7
0.5	1.35	0.5	1.7	0.5	2.0
0.6	1.6	0.6	1.9	0.6	2.3
0.8	2.0	0.8	2.4	0.8	2.8
1.0	2.3	1.0	2.6	1.0	3.2
1.2	2.7	1.2	3.0	1.2	3.6
1.5	3.2	1.5	3.5	1.5	4.2
2.0	4.0	2.0	4.3	2.0	5.1

Info for reference only.

B Ensure that high voltage power supply safety rule requirements detailed below are met.

Electrical clearance and creepage distance

Primary Side				Secondary Side			
Working Voltage(V)	Air gap (mm)	Creepage distance(mm)	With GND areas(mm)	Working Voltage(V)	Air gap (mm)	Creepage distance(mm)	With GND areas(mm)
50	1.0	1.2	6.3	71	0.7	1.2	2.5
150	1.4	1.6		125	0.7	1.5	
200	2.0	2.0		150	1.7	1.6	
250	2.0	2.5		200	1.7	2.0	
300	2.5	3.2		250	1.7	2.5	
300	3.5	4.0					
400	5.8	6.3					

Electrical clearance and creepage distance

1	Peak value of rated voltage 0,1/V	60	90	190	375	550	750	1000	1300	1550
2	Creepage distance/mm	3	4	8	10	15	18	25	36	40
3	Creepage distance under insulation coating/mm	1	1.3	2.6	3.3	5	6	8.3	12	13.3
4	Electrical clearance/mm	3	4	6	6	6	8	10	14	16

C Ensure that the Power Supply feedback point is selected correct.

D Ensure that the Power Supply is close to the load.

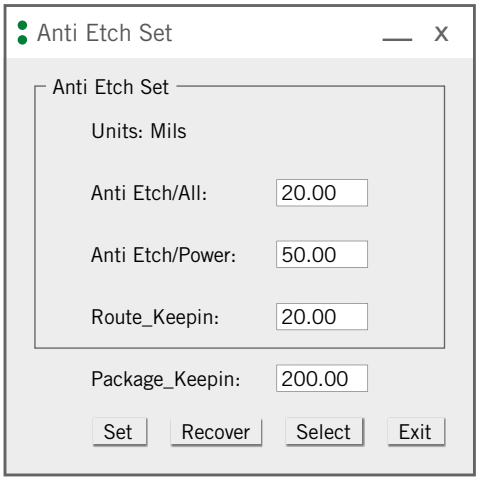
9 DRC Check

A On Plane layers, BGA internal cross channel are not isolated due to via grid.

B Ensure on differential pairs that positive and negative lines are correctly connected.

C Check that the power plane is pulled back 0,762 mm from the GND plane.

D Check that the plane layer does not have isolated copper pattern.

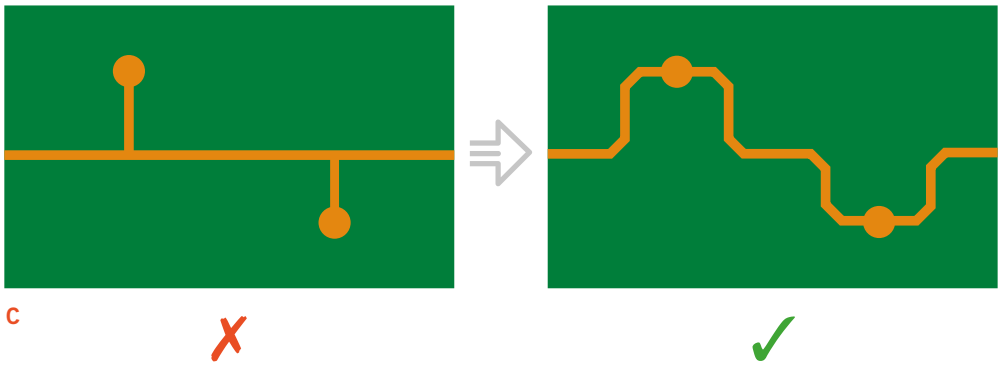


10 Test Pin

A Confirm test point spacing is correct. ICT test point spacing should be more than 1,27 mm.

B Ensure the test point is on the same side and is not placed within the device courtyard/silkscreen.

C Ensure that high speed test points are in line and do not add unnecessary decoupling, signal integrity, or via stub concerns. Follow up the high speed signal test point rules as outlined herein.



11 Silkscreen Check

A Text size consistent - Font Number 3 by default (W:0,584 mm, H:0,787 mm, LS:0,991 mm PW:0,102 mm, CS:0,076 mm).

B Silkscreen text in tight places can be reduced to Number 2 Font, however photo width must be greater than 0,101 mm.

C Silkscreen prohibited on-block solder mask, pad, test point.

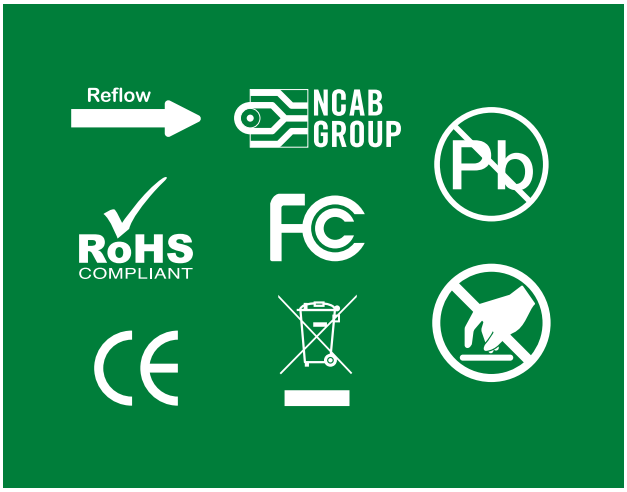
D Silkscreen prohibited to overlap with other silkscreen.

E Ensure that any customer's required text (Example: PB Free Logo, EMI Logo, Name, Part Number, Serial Number, etc…) is added to the PCB.

Electrical clearance and creepage distance (mils)

Text Blk	Width	Height	Line Space	Photo Width	Char Space
1	16.00	25.00	31.00	4.00	3.00
2	21.00	29.00	35.00	4.00	3.00
3	23.00	31.00	39.00	4.00	3.00
4	47.00	63.00	79.00	6.00	3.00
5	56.00	75.00	96.00	6.00	3.00
6	60.00	80.00	100.00	6.00	3.00
7	69.00	94.00	117.00	6.00	3.00
8	75.00	100.00	125.00	6.00	3.00
9	93.00	125.00	156.00	6.00	3.00
10	117.00	156.00	156.00	6.00	3.00
11	393.70	314.96	118.11	6.00	3.00

A



E

12 Gerber Review

A The Gerber information of each layer is correct (solder mask layer, silkscreen layer, paste mask layer, negative plane layer, signal layer, FAB layer, and placement origin file).

B There are no Warning or Errors in the Gerber file when loading into Gerber viewer.

C Visually check each layer checks to confirm that there are no obvious design problems.

D Check open/short circuit by utilizing the netlist compare.

E Check for unconnected pads.