EMC and System-ESD Design Guidelines for Board Layout

About this document

Scope and purpose

This document provides information for EMC optimized PCB design and system ESD design. The topics covered include PCB Design considerations regarding the routing of high speed signals, selecting stack-up of the PCB, selecting decoupling components, impedance controlled design of the traces, and termination of high speed signal paths. Special considerations for microcontrollers are also provided.

Attention: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by the customer, based on their specific implementation choices.

Intended audience

This document is intended for anyone who needs to design EMC optimized application boards using microcontrollers and other components from Infineon Technologies AG.

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1 Overview

The topic of ElectroMagnetic Compatibility (EMC) is important for the functionality and security of electronic devices. Today's designers have to deal with permanently increasing system frequencies, changing power limits, high density layouts by more complex systems, and the need to keep manufacturing costs low.

In this EMC design guideline we concentrate on the rules, examples, simulations, and measurements for Printed Circuit Board (PCB) layout. By using these rules it is possible to prevent high electromagnetic emission through a well-designed PCB.

This design guide is made for various applications, and each application will show a different reaction on the realized EMC design improvements. Many of the rules are around the problem of ElectroMagnetic Emission (EME). Due to the fact that an EME-optimized board layout is not so sensitive to interference, using these rules will also decrease the susceptibility (EMS).

Electromagnetic compatibility is the quality of a subsystem or circuit to not affect and to not become affected in the system where it is used. The measures to realize good EMC-behaviour in an application have to be started and implemented in the first development steps. In other words, EMC measures have to be considered as a system or circuit specification. Measures and actions taken later on, for an already manufactured PCB, are not as effective and will lead to higher costs.

Electromagnetic disturbance is the interference to the normal function of an electric circuit by coupling in an additional voltage. There are various paths to couple into a circuit and various ways to avoid these interferences.

EM disturbance counter-measures

The EM disturbance countermeasures follow three steps:

- The source
  - This is the place where the noise or disturbance is created. Reason for this can be for example the switching noise of a circuit with high current (high di/dt), fast signals, fast rise time, resonance, antenna structures, wrong termination, reflections and electric potential differences.
  - Goal: RF noise suppression at the source.
- The coupling path
  - The path or medium where the disturbance is distributed from the 'source' to the 'victim'.
  - Goal: The 'coupling path' has to be made inefficient.
- The victim
  - The electrical circuit which becomes influenced by the disturbance coming from the 'source'. This disturbance can lead to some imperceptible noise added on a signal. But this disturbance can also have some major impact on the functionality of a signal or the whole application.
- Goal
  - Low susceptibility to emission at the 'victim'.

At each step it is possible to dampen or even eliminate the electromagnetic disturbance using the design measures we will discuss.

1.1 Noise Sources

This is the place where the noise or disturbance is created. There are a lot of sources which can cause RF noise. The most important sources are microcontrollers, oscillator circuits, digital ICs, switching regulators, transmitters, ESD and lightning.

The primary goal must be RF noise suppression at the source.

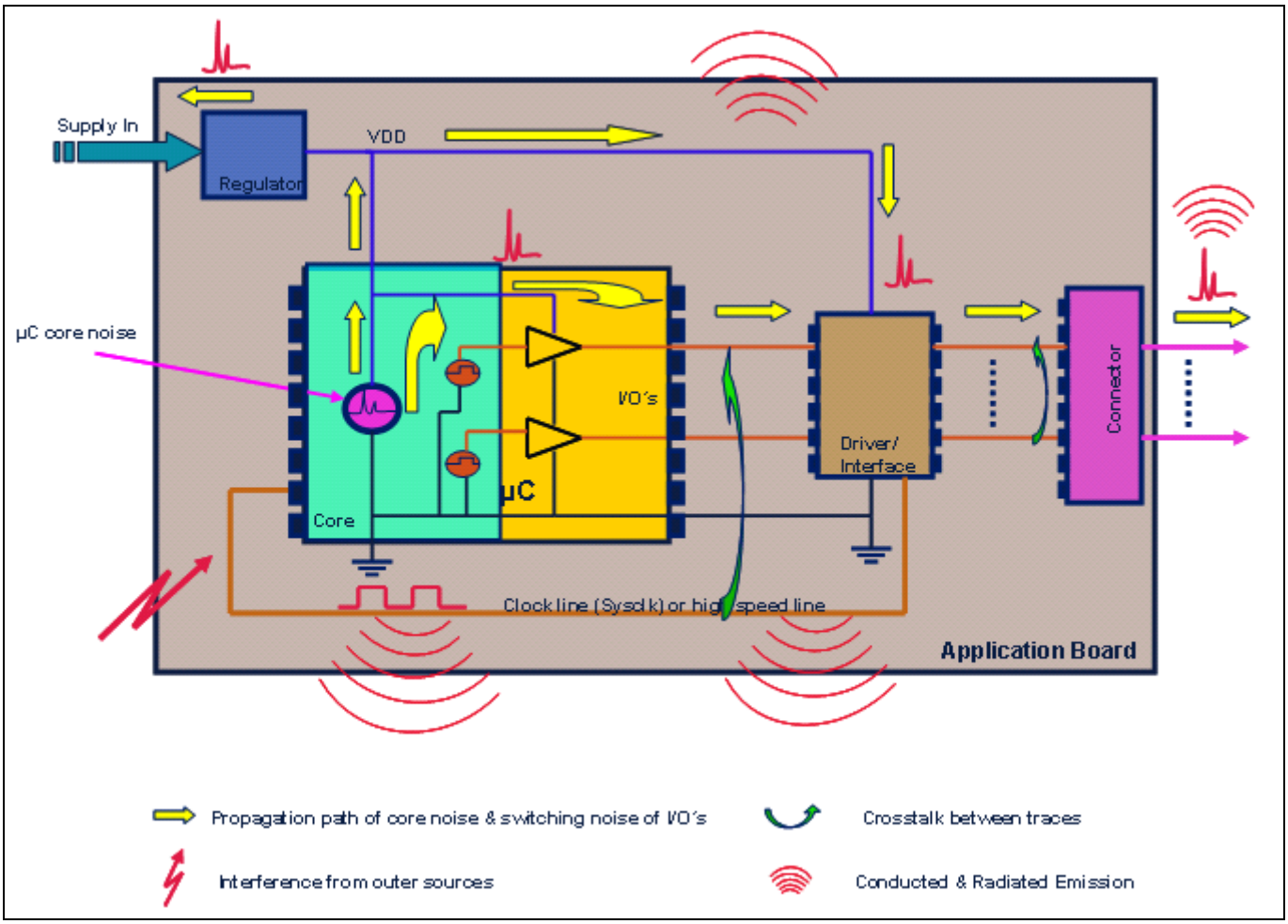


Figure 1 Typical application board and noise source paths

From the PCB design perspective, the most common cause of radiation is from the supply network due to the switching noise of the core activity and toggling I/O ports of the microcontrollers, or from other ICs which have driving I/O ports. Generally the driver outputs are connected to long traces on the board which are also connected to the cables. These cables are running to the other system components. The nature of the traces and cables is very close to the antenna behaviour, and the radiation of energy through these antennas can cause very serious problems. The emission (radiated and conducted) of the switching noise through the power pins and the connected planes is a significant portion of the EMC behavior of the microcontrollers. The capacitive and inductive coupling between adjacent traces can provide a path to distribute the noise on the board.

Oscillator circuits produce a trapezoid wave which has a fundamental frequency and harmonics. If careful placement on the board is not realized, then a coupling to the nearest components and traces is probable.

In digital systems the radiation behavior of a switching circuit depends on the form of the digital signal. As shown in the next figure, the emission spectrum is related to the duty cycle and the rise/fall times of the

Overview

switching signals. The high time determines the point where the spectrum begins to fall with 20 dB/decade, and rise/fall time gives the second point where it begins to fall with 40 dB/decade.

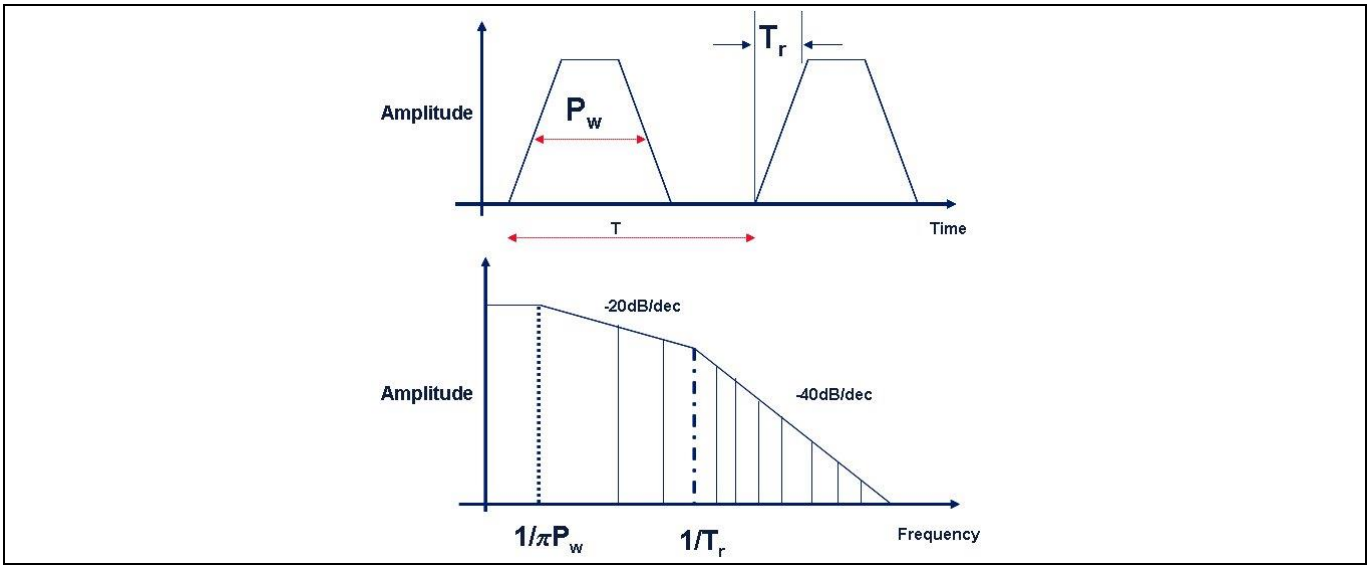


Figure 2 Spectrum of a trapezoidal signal

The next figure shows the calculation results, which depict the spectrum of a periodic pulse for different pulse widths and clarifies the relationship between pulse width and the resulting spectrum. The magnitude in spectrum increases as the pulse width increases.

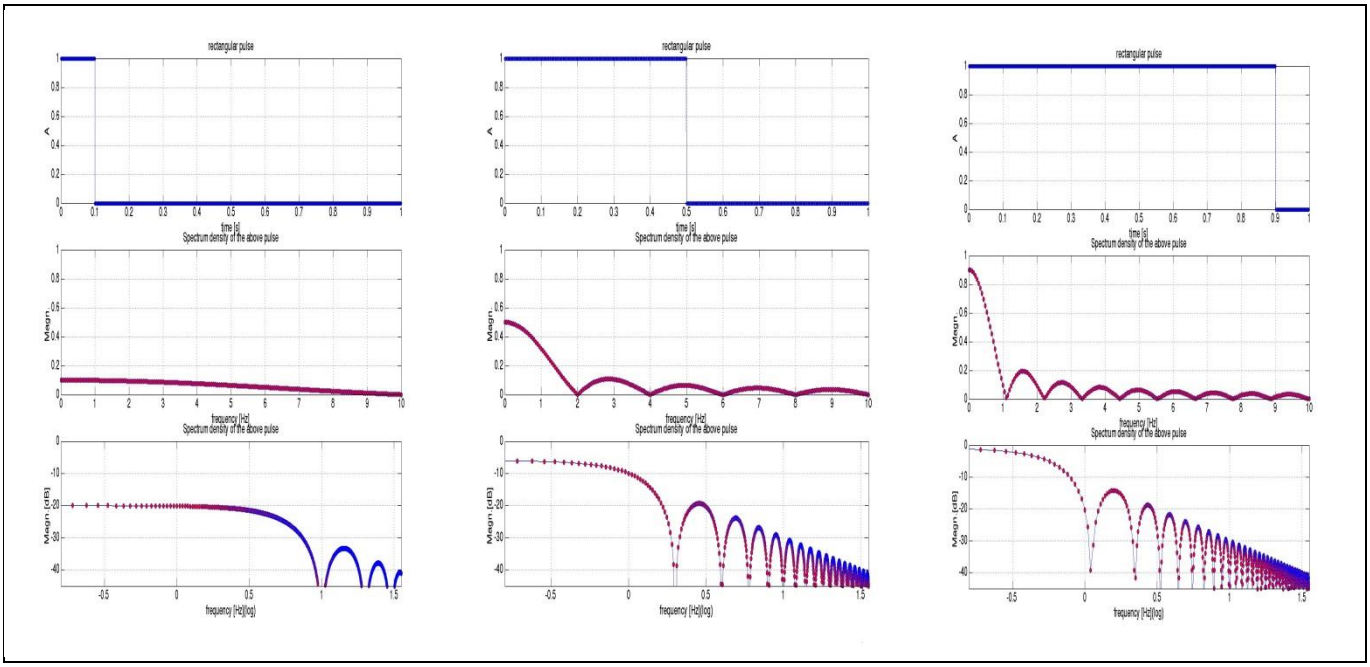


Figure 3 Relation of spectrum and pulse width

For the high speed design of PCBs, it is important to decide how to handle the traces if they carry high speed signals and under which circumstances the line length is critical.

Generally we can say that if the one half rise/fall time of the signal is smaller than the propagation delay of the PCB trace, the trace should be treated as transmission line and should be routed applying additional measures and terminated with its characteristic impedance (see also Layout Structures).

Overview

The next important point is the design of the integrated circuits. Most designs of microcontrollers are synchronous clock systems, which cause some EMC problems on the power supply network of the ICs due to the synchronous construction of the logic circuits. A careful design of the IC´s power supply network is also required.

1.2 Coupling paths

'Coupling paths' refer to the path or medium where noise is distributed from the 'source' to the 'victim'.

The goal is to make the 'coupling path' inefficient.

The coupling can be effective in two ways; radiated and conducted:

Radiated coupling paths

The radiated coupling paths are electromagnetic fields and crosstalk (inductive or capacitive). The radiation path of the signals less then 30MHz is conducted and for the signals above the 30MHz the noise will increasingly radiate.

Conducted coupling paths

The conducted coupling paths are galvanic coupling, supply network (power & ground). Interference current and voltage of an electrical system can be described as common-mode (CM) or differential-mode (DM).

1.2.1 Common-mode and differential-mode

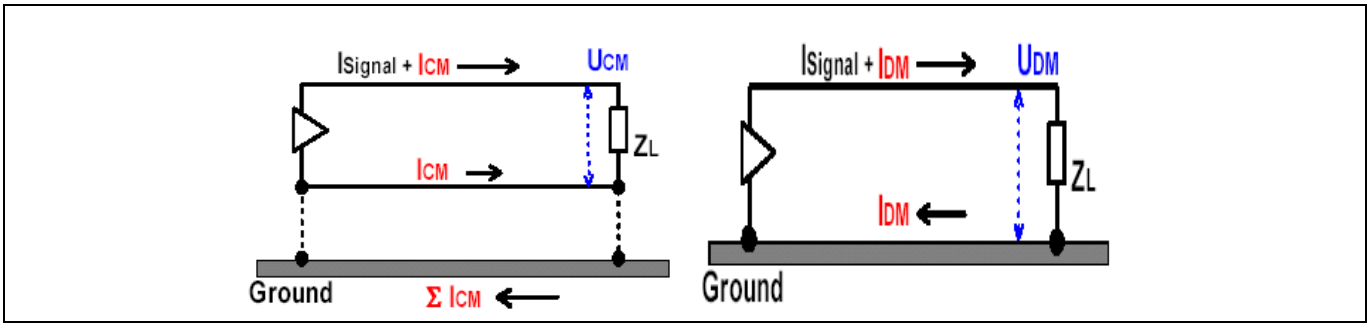


Figure 4 Common-mode and differential-mode

Common-mode

Interference is an asymmetrical disturbance. It often occurs between a cable system and its electrical reference potential. Signal and noise current have the same (common) direction in the loop. The cables radiate the energy caused by the ground system noise. Common-mode radiation can be reduced by reducing the impedance of the ground system.

Differential-mode

Interference is a symmetrical disturbance which occurs between two traces or lines. One of these lines can also be the ground path. Signal and noise current have different directions in the electrical loop. If the loop area of the signal and return path increases, then the differential-mode radiation also increases.

Overview

Current loops

Switching a signal produces a current transition that goes through the trace and receiving device and returns over the power system (VDD or VSS) to the transmitting device. This path forms a current loop.

Current loops have significant inductance and can be modeled as a coil of a transformer. The inductance of the loop depends on the loop size and increases with it. Usually on a PCB there are many such loops which interact with each other:

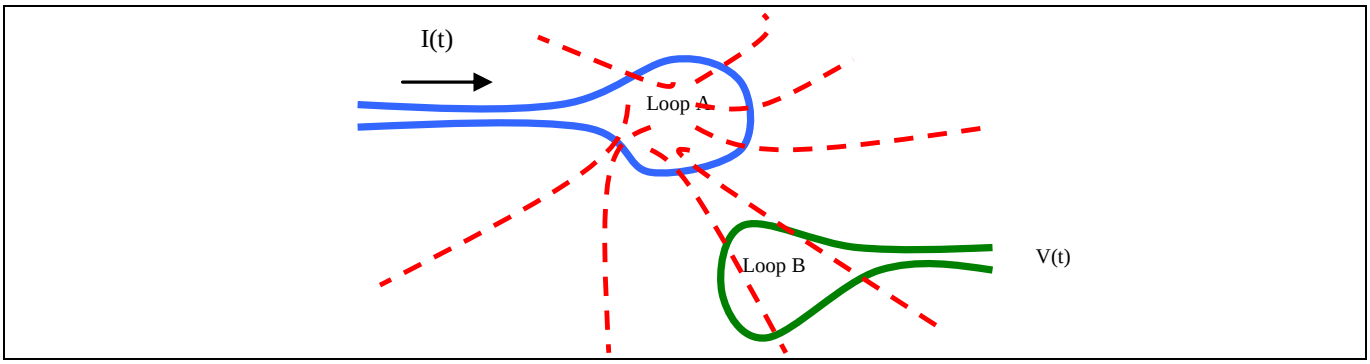


Figure 5 Interaction of two loops

If any change occurs in loop current A it induces a proportional voltage in loop B, because a part of the total flux from loop A goes through the loop B and induces the voltage v(t). To minimize the inductive coupling between the loops, the loop inductance has to be reduced. This can be done by reducing the loop size. Using power planes gives a very low impedance connection possibility for VDD and VSS power buses.

Due to the fact that the low frequency signals follow the least resistance path and the high frequency signals follow the least impedance path, the signal return paths have to be designed so that the loop inductance is as low as possible. In case of the power plane design, the power plane must show no break or discontinuity in the signal return path, so that the least impedance path can be used.

Crosstalk

Crosstalk is the coupling between two adjacent traces. The crosstalk effectiveness depends on two parameters: capacitance and inductance between adjacent traces.

In case of the inductive crosstalk, both of the traces form a loop which acts like two windings of a transformer. The loops are the traces on the PCB with their signal and return paths. The distance and loop area determine the crosstalk. To reduce the inductive crosstalk the loop area should be reduced.

The circuit in **Figure 6** shows two adjacent traces, one trace acting as source and one trace acting as receiver. Because of the capacitance between the lines, the noise generated by the source can couple to the other trace. The noise generates a current which is coupled through the capacitance to the next signal line.

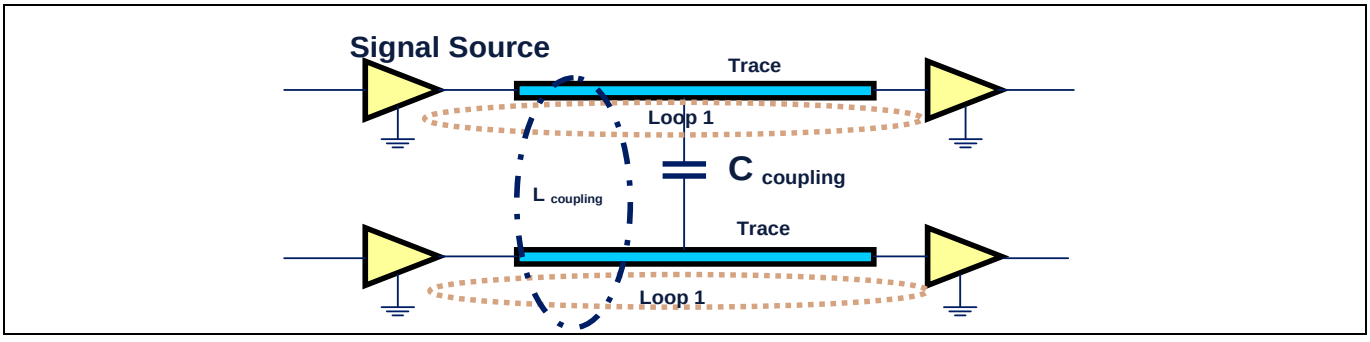


Figure 6 Capacitive and inductive coupling

Overview

The dV/dt of a signal source produces a current depending on the coupling capacitance between the two traces.

$$I = C\frac{dV}{dt}$$

The di/dt of a signal source produces a voltage depending on the mutual inductance between the two loops.

$$V = L\frac{di}{dt}$$

The capacitive crosstalk can be reduced by separating the traces/loops. More distance between traces leads to less crosstalk. But in many applications the PCB area is limited so that a separation of the traces is not always possible. In this case the placement of a guard trace between the traces can help. The guard trace can be an approach for two-layer boards, but for multi-layer boards the benefit is not so high because in most cases a solid ground plane is designed. The most effective measure is the proper termination of the signal lines.

2 PCB considerations

A good EMC-optimized PCB design includes three design stages:

- component selection/placement
- design of the grounding concept (power supply system)
- decoupling concept

Before the placement, the critical paths and circuits have to be identified so that a functional grouping can be made. The analog circuits should be isolated from the source of noisy signals. High-speed ground and analog ground must be separated from each other. The ground areas of different circuits should not overlap.

For reason of EMS and signal integrity, external logic with high input threshold (Vih) should be chosen. For example, prefer HC (High Speed CMOS) or AC (Advanced CMOS) standard ICs due to higher Vih. Select optimum (i.e. not unnecessarily fast) rise-/fall times to decrease di/dt noise. Use the criterion of low cross-currents for the selection of other ICs.

Supply voltage

When a higher supply voltage is used, more power is inside the electrical system. This implies that a higher voltage fluctuation happens and therefore higher emissions will be created. Consequently, to minimize electromagnetic emission, use the lowest possible supply voltage. If susceptibility is a matter of concern, the supply voltage should not be too low. A low voltage level implies a small signal-to-noise ratio.

Oscillator

Use the lowest speed for oscillator and crystal. Adjust this to the demands of the application hardware and software.

Use PLL for higher frequencies. An isolated ground plane under the oscillator circuit can be used to reduce the propagation of the clock noise to the board. This ground isle should be connected (high impedant) at one point to the board ground (see Layout example for crystal oscillator circuit).

Attaching cables to a PCB

Group connectors by function. Separate analog signals from high speed signals for example. Provide decoupling measures (capacitors, ferrites, optical systems, for example).

Note: Do not let any noise go from the PCB on the cables since this increases emissions dramatically. Do not let any noise go from the cables to the PCB since this may cause functional instabilities.

Provide enough GND pins for a cable transferring critical signals. Avoid cables if possible. If they are necessary, make them as short as possible. Fix them so they will not move, otherwise their EMC behaviour is unpredictable.

Twist power or signal cables with the corresponding GND cable. This means that the flow of current and the back current will be close together. Both electromagnetic fields will compensate each other.

Two-layer / multi-layer boards

Multilayer boards provide many advantages compared to two-layer boards with respect to EMC behaviour, but in some cases two-layer boards are preferred because of their low cost. Multilayer boards cost more than two-layer boards.

PCB considerations

With multi-layer boards it is possible to design low impedance power supply and ground connections using power/gnd planes, which cover at least one layer or a part of one layer. Realizing EMC-related measures is easier with a multi-layer board than with a two-layer board.

Traces

In high-speed designs the reference (ground) for the traces is very important. The design of a trace can affect the emission and/or signal integrity behavior of the trace. Two types of traces can be used:

- microstrip
- stripline

(See also Construction of microstrip and stripline).

The stripline has the reference plane on both sides which results in lower impedance than for the microstrip.

To avoid EMC disturbances of adjacent traces, try to keep the distance between sensitive traces as big as possible. For high speed signals guard traces might be necessary. This means that between two signal traces a ground trace should be designed.

In general, sensitive traces should not be designed in parallel to high speed or noisy traces. If you cannot avoid such a design, make the parallel paths as short as possible.

Vias

Because of EMC it can be an advantage to use different kinds of vias on a high-speed signal application.

- Microvias
  - These have a hole diameter of about 100µm and can be designed into the pads of discrete components. Because of the small diameter space can be saved on the PCB and therefore the power plane structures are not cut as much as by bigger vias. For the same reasons multiple microvias can be designed instead of one big via. That lowers the inductance of the connection since they behave like inductors in parallel.
- Buried vias
  - These can be used at a multi-layer design. They are connecting some signals or power traces at the inner layers of the PCB (from the 3th to the 4th layer for example). They are not drilled from the top to bottom layer but just through the inner layers. With buried vias, some layers of a multi-layer board can be made high-frequency sealed while not cutting the outer planes. In addition area for trace design can be saved.
- Blind vias
  - They are drilled from an outer layer to one of the inner layers. Because of that not all layers of a PCB are cut for a signal or power trace connection with the first or last few layers. Blind vias are most efficient if used in combination with buried vias.

High impedance traces

By using traces with higher impedance (smaller or narrower traces), disturbances can be kept locally; for example traces to the voltage regulator.

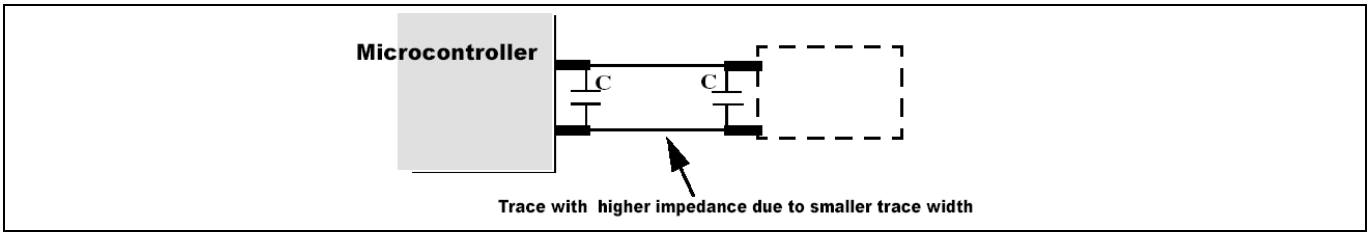


Figure 7 High impedance traces

PCB considerations

Package

For BGA (Ball Grid Array) packages most Vss pins are grouped in the center of the microcontroller. In general the corresponding Vdd pins are located on the inner row of the outer circle. This pinning allows a short connection to the decoupling capacitors (decaps) when placed on the opposite side of the PCB. For lead-frame packages the decaps must be placed between VDD and GND pins. The connection to the supply and ground planes or traces has to be made by vias placed on the “outer” side of the capacitor:

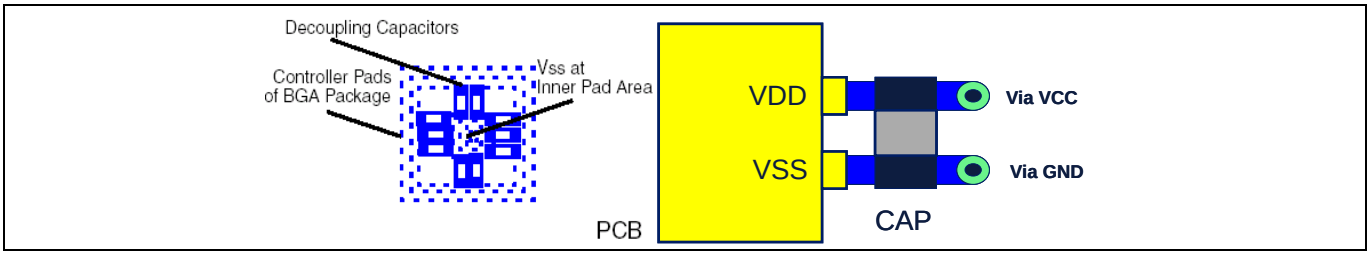


Figure 8 Decoupling of a typical BGA (left) and lead-frame (right) package

PCB material

The dielectric permittivity εr is an important parameter for calculating the wave impedance of a trace or a plane. For the PCB material this constant, at the frequency of 1 MHz, can be provided from the board manufacturer. For fast signals it has to be considered that the dielectric permittivity is frequency dependent. Example: FR4 material has εr of 4.7 at 1 kHz, 4.5 at 1 MHz and 4.35 at 16 MHz.

In high-speed systems above 4GHz it is recommended to use other materials than FR4, such as Teflon or BT-material.

The impact of the dielectric permittivity εr on the PCB impedance is shown by a simulation with different εr boards (εr = 4, 10, 100). For the simulation a board with 10x10 cm² dimensions and a PCB thickness of 20mil was used. The following figure shows that with increasing εr value, the impedance of the board gets lower. The resonance frequency is shifted towards higher frequencies with lower εr values.

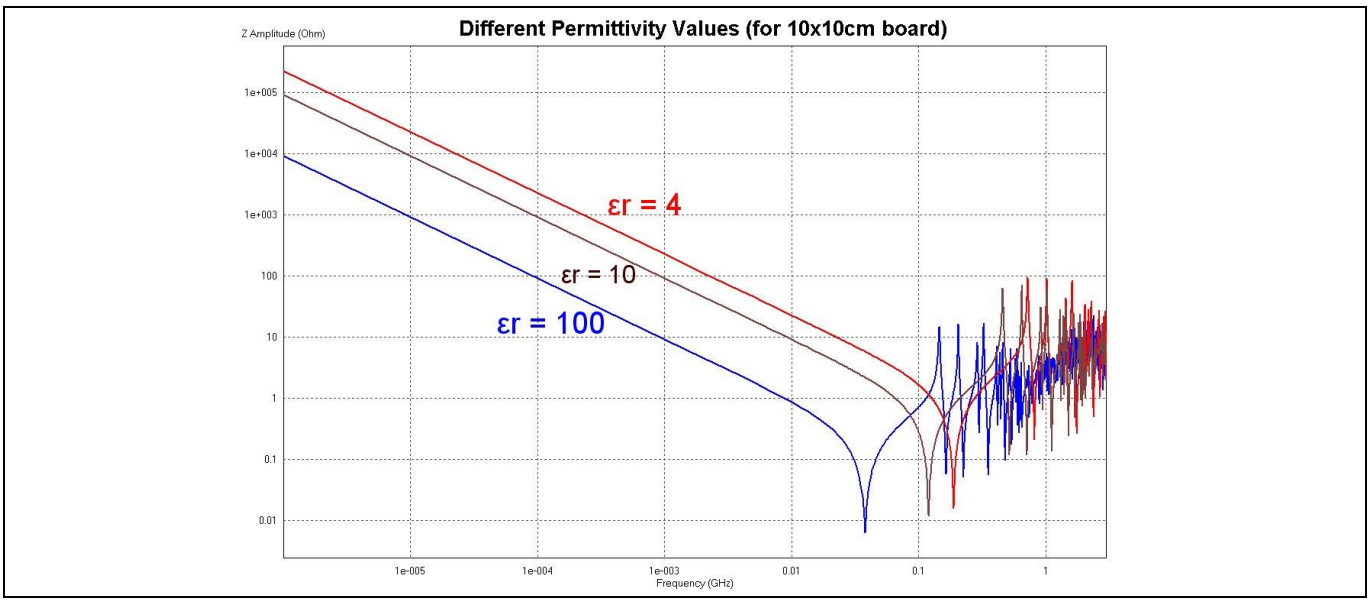


Figure 9 Impedance of PCB for different εr values

3 Design measures

The following guidelines are recommended, however each measure described here must be evaluated for each application. The realization of all measures can be very difficult, particularly in complex applications, so that a trade-off has to be made.

For more complex structures it is not possible to determine general design rules. These structures have to be investigated and optimized using SPICE simulation in conjunction with 2D or 3D-field solvers.

General design recommendations

- Define functional units.
  - Classify also by speed: analog / sensor, digital low speed, digital high speed, power elements.
  - Place all components operated with the same clock together.
- Keep elements of same functional unit in close distance to keep critical signal traces as short as possible.
- High speed traces should be placed near the center of the board, far from the edge of the board.
- Provide enough space for decoupling capacitors close to the IC and spread them over the whole PCB.
- Keep the lead length of the decoupling capacitors as short as possible and locate the capacitors as close as possible to the VDD/VSS pins of the component.
- Consider the usage of special “low-inductance” capacitors.
- Before beginning the routing, identify critical signals according to the highest carried frequency and shortest rise/fall time of the signal.
- Place high current carrying lines as close as possible to the voltage regulator´s output.
- Provide connections for series resistors within high speed traces close to the driver.
  - Take care that the signal timing does still meet the specification.
- Place oscillators adjacent to the clock driver.
  - If an asymmetrical board stack design is used, place the crystal oscillator on the side of the PCB which has the largest distance from the reference ground layer. This can prevent a direct coupling from the crystal oscillator package into the ground system of the PCB. To reduce the radiation / coupling from oscillator circuit, a separated ground isle on the GND layer should be made (see **Figure 18**).
- For two-layer boards keep a minimum distance between functional units by geometry (**Figure 19** and **Figure 20**).
- Separate parallel running traces by not less than 2x trace width.
- Changing of layers affects also the impedance, which causes reflections at these points.
- Remove 20*H of metal from the edges of the VCC supply plane to reduce edge radiation. ‘H’ is board layer height or thickness (see **Figure 10**).
- Place I/O connectors carrying external signals on one edge of the PCB.
- Prefer manual routing to the auto router of the layout tools for critical signals.
- Do not place the connectors close to high speed circuits.
- Place crystals, oscillators and clock generators away from I/O ports and board edges.

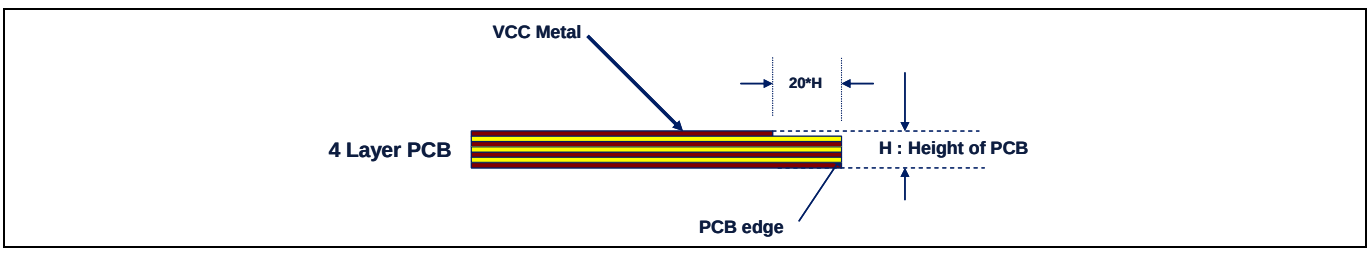


Figure 10 Removing metal of power plane from the edge of PCB (20*H rule)

3.1 Power Supply

In the first step of the PCB layout the power supply system should be designed. A proper power bus and grounding design is a basic requirement for voltage stability and reduced electromagnetic emission. Decide on the PCB technology: either two-layer or multi-layer board. For the multi-layer boards a proper stack-up of the PCB should be designed (See Multilayer boards).

Note: With regards to EMC, a good design of a two-layer board is more difficult to realize than a four or more layer board. A trade-off between the lower cost of a two-layer board plus additional filter components, and the higher cost of a multi-layer board without additional filter components, needs to be carefully examined.

Depending on the selected PCB technology, different grounding systems can be used. For power systems the most common distribution method is a single or star connection type (see Two-layer). But in high speed systems the star grounding is not the best solution. Because of the high frequency path of the noise, an increase in radiation can result.

For a multi-layer PCB the use of power layers is a good solution. Covering one layer with metal provides much less impedance for the connection to the decoupling components.

Voltage regulator: canalize the RF current

Energy which is transformed to heat or is otherwise canalized cannot radiate anymore. See the example to position capacitors to isolate and disturb reflected (high frequency) energy. In fact the high frequency current is created inside the IC. By using block capacitors this RF energy will not leave the circuit via this supply line. But be aware that energy can couple out via other paths which are connected to the µC.

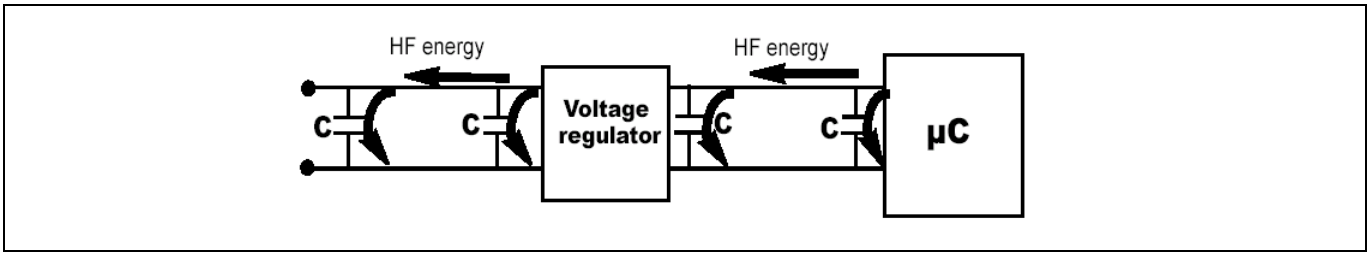


Figure 11 Flow of the canalized energy

Separate the digital from the analog supply system. Use at the output of the voltage regulator decoupling capacitors and inductors to reduce the noise propagated over the powerlines. For the decoupling at the supply level, tantalum capacitors are preferred.

Since supply systems themselves have a parallel resonance frequency, it has to be considered to shift this resonance out of the range of critical frequencies. This can be done by shortening the length of the supply trace. Since board geometries are given from the application functionality, this is not always possible. In this case a capacitor in the range of 100nF can be implemented into the current path. This has the effect of shifting the electrical length of the system with the resulting parallel resonance frequency getting higher.

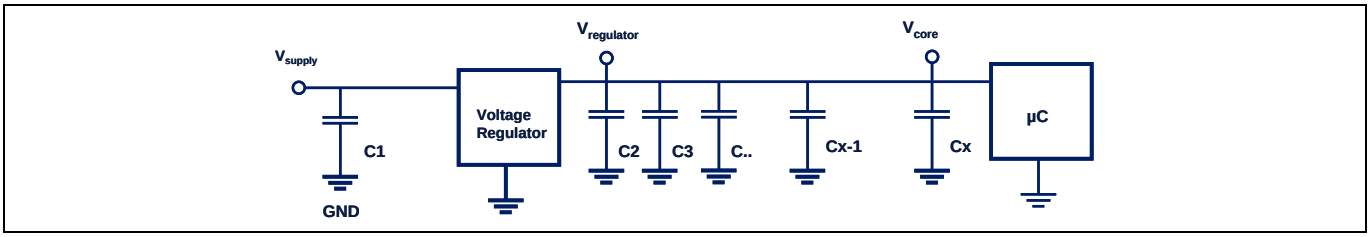


Figure 12 Decoupling of the power circuit

3.1.1 Layout Structures

Keep power and ground nets which belong to each other close together in order to reduce impedance. The GND trace should be as close to the VDD trace as possible. The best choice is to design them in parallel. If the current and its corresponding ground trace have to go different ways, there will be different potentials and common mode problems. The following figure shows GND-trace and VDD-trace on different sides of the PCB:

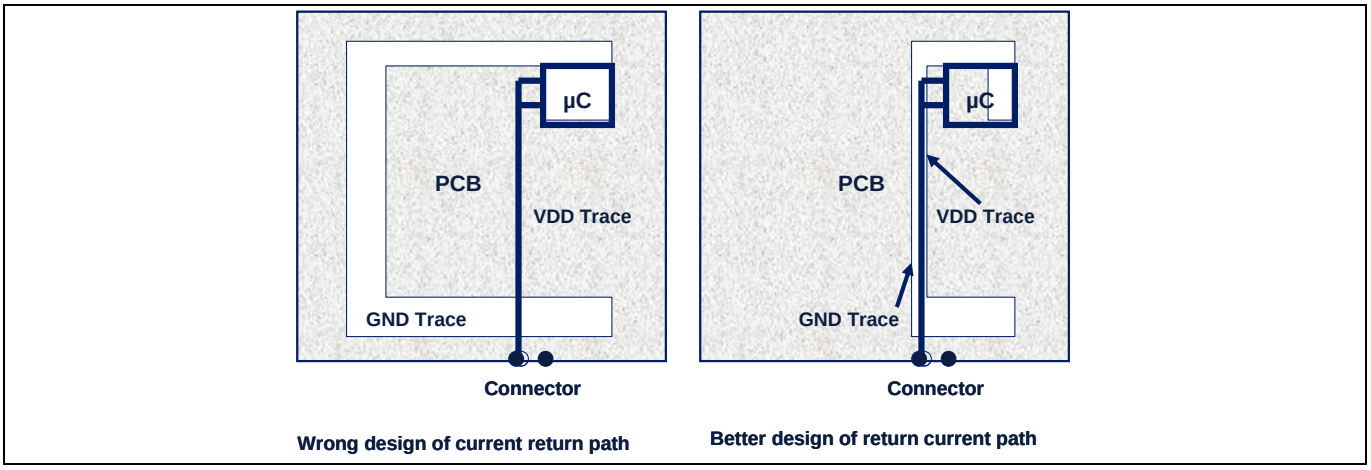


Figure 13 Design of ground traces

In general, power and ground traces should lead directly from the supply connector to each component / functional unit. If possible, use one side as a complete ground plane for an optimized current flow. Ground area fills have to be handled with care, otherwise the emissions may increase because of resonance structures and antenna effects. Connect them by several vias or wide traces to the reference ground of the board. Since there are various effects which influence the radiation and susceptibility of the PCB, each application has to be handled individually.

Signal currents use both power plane and ground plane as return paths. Keep supply planes as “clean” as possible; Avoid areas of high impedance (groups of vias, gaps).

Avoid segments in the ground planes to keep the current return path short. The supply planes should also be as small as possible to reduce the coupling and radiation of the noise to the power system and it should use enough area to deliver power to all components which are connected to the power system.

Examples for placements of vias are shown here:

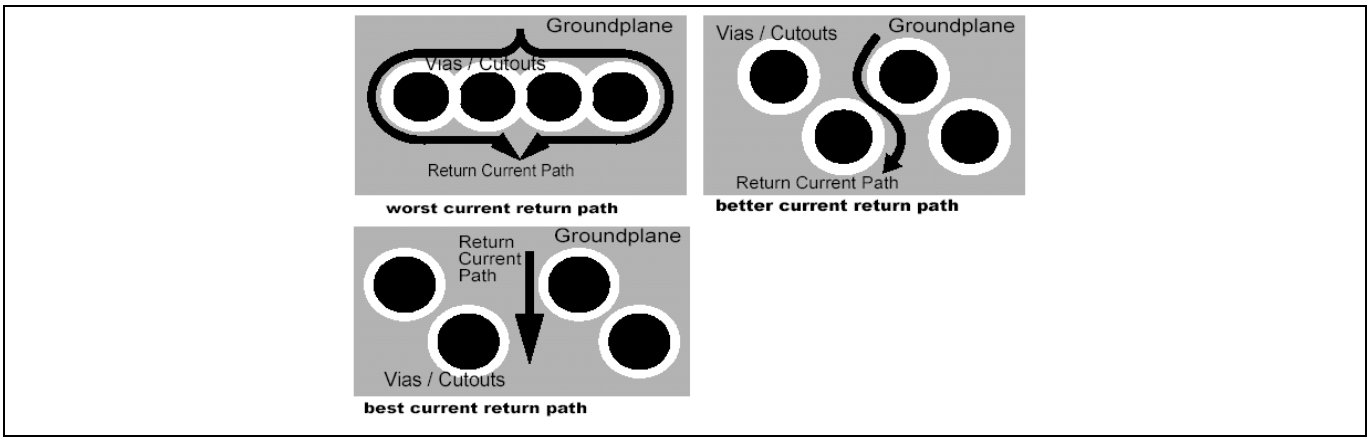


Figure 14 No blocking of Current Return Path

Design measures

In the upper-left case the return current is forced to flow around the group of vias. In the upper-right case the current can flow nearly directly from one side to the other. The best solution for a current return path is shown in the lower-left configuration.

In some cases splitting power or ground planes can cause a big improvement in the EMC behaviour and for signal integrity. This splitting has to be done under several considerations of the signal and current flow. A separation of very sensitive parts from noisy areas of a PCB keeps the disturbance low and minimizes the possibility of galvanic coupling. If the VDD plane is to be divided into segments, provide one area for every functional unit. These zones should still be connected together if they have the same power supply. That influences the way and the impedance of the current flow. For the ground plane a path with low impedance has to be guaranteed. The separated zones should be connected together again at a common supply starpoint, which should be close to the power supply connector or voltage regulator on the PCB.

A functional unit can contain all RF-components, all analog components, and so on. Another way of building functional units is to distinguish them by supply voltage (5.0V, 2.5V, etc.).

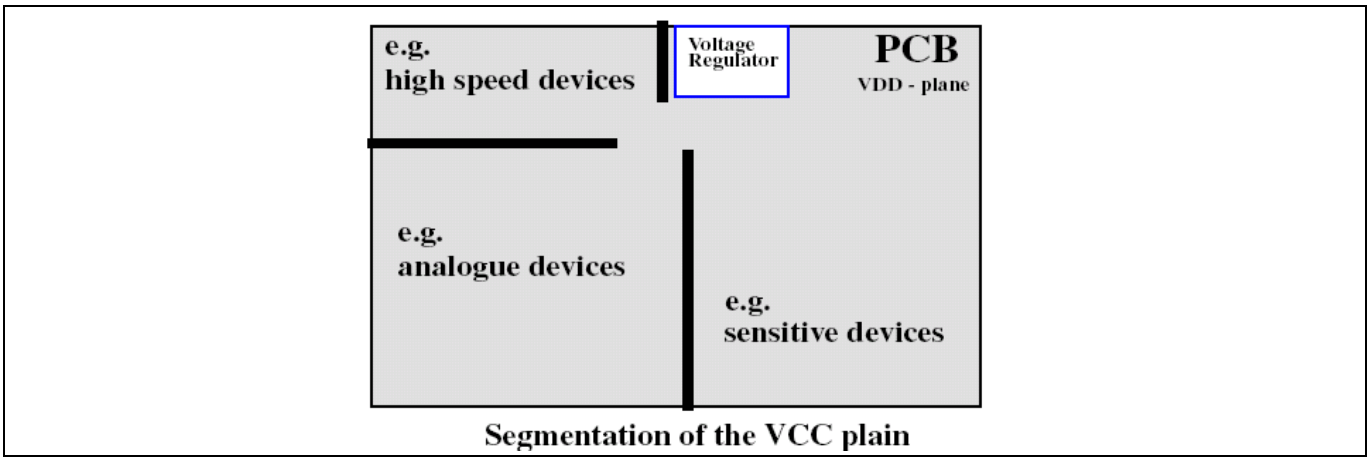


Figure 15 Example: Segmentation of the supply plane with voltage regulator as common ‘supply star-point’

Resonances of the board structures influence the EMC behavior in a direct way. If the harmonics of the work frequencies have the same frequency as the parallel resonances, significantly high amplitude may be produced. These harmonics can then couple to the other supply paths and traces. The board structures should be selected so that no parallel resonances are in the interested range. As it can be seen in the simulation results in **Figure 17**, the smaller the board structures are, the higher is the resonance. These parallel resonance frequencies can be seen on the emission spectra and can be critical for signal integrity.

Since board resonance is mainly caused between two planes, one option is to realize the VDD power by traces (i.e. power star-point, separate traces for different board sections, distance to ground plane).

Traces have higher impedance compared to a plane structure. Using VDD traces, local disturbances on the PCB can be prevented from spreading over the whole board. To provide the necessary current potential for switching operations, locally decoupled ’power islands’ should be realised directly underneath the microcontroller and logic devices. From these islands the noise has a path of high impedance to other devices and will be kept locally.

Design measures

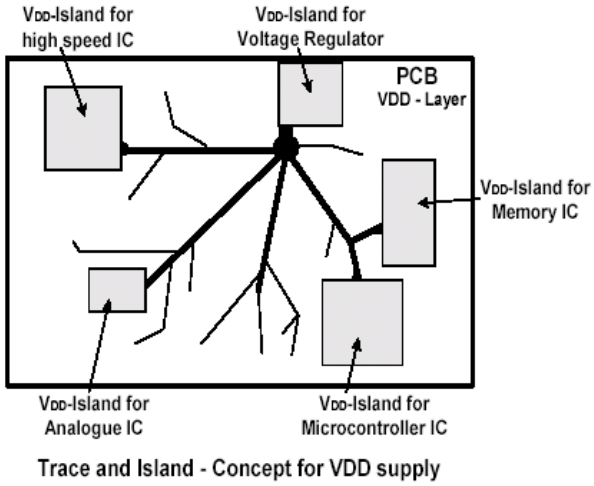


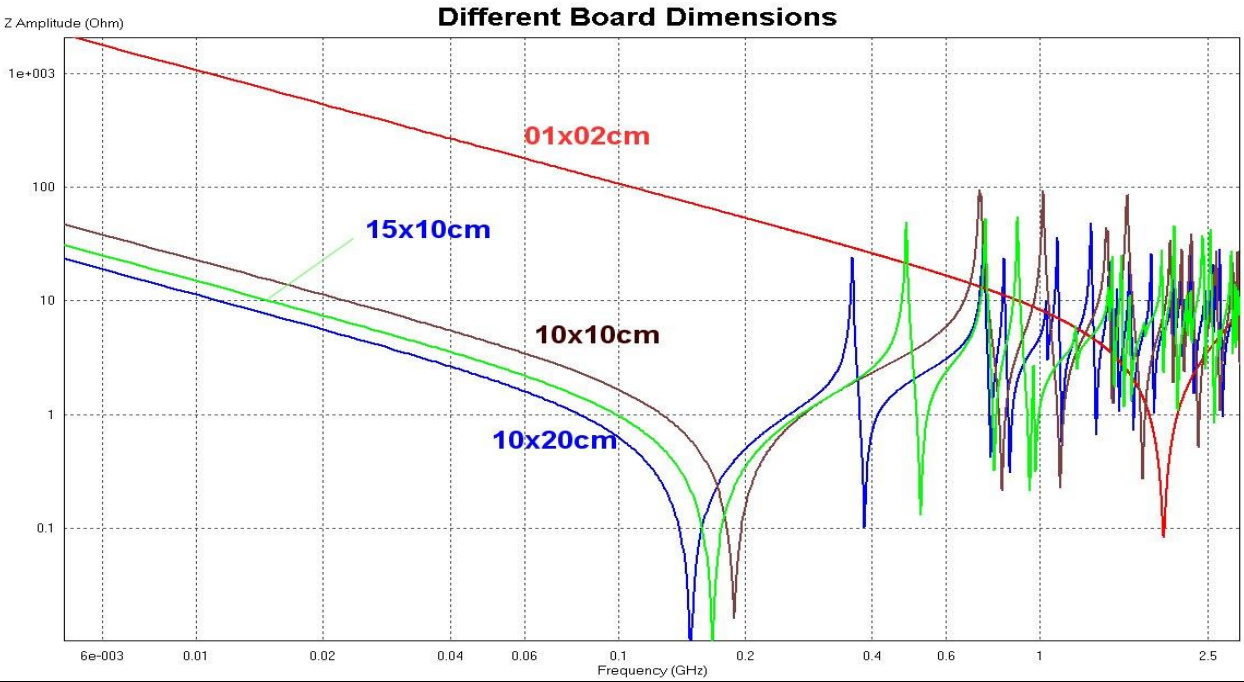
Figure 16 Example: Using VDD islands and traces over ground plane.

The capacitance and inductance of the planes cause a high frequency resonance, depending on their values.

In some high-speed applications, the power plane capacitance can be used as a distributed capacitance to reach an attenuation of the total impedance of the power network on the PCB in high frequency range. In this case it is important to calculate the impedance and determine the dimension of the power plane to reach an adequate decoupling effect. The capacitance of a plane structure depends on the board thickness, dimensions and dielectric permittivity of the board.

Figure 17 shows the change of the power plane impedance if the thickness of the board varies and the change of the board impedance if the dimensions of the power plane vary.

The first board resonance shifts to higher frequencies if the plane area gets smaller.



Design measures

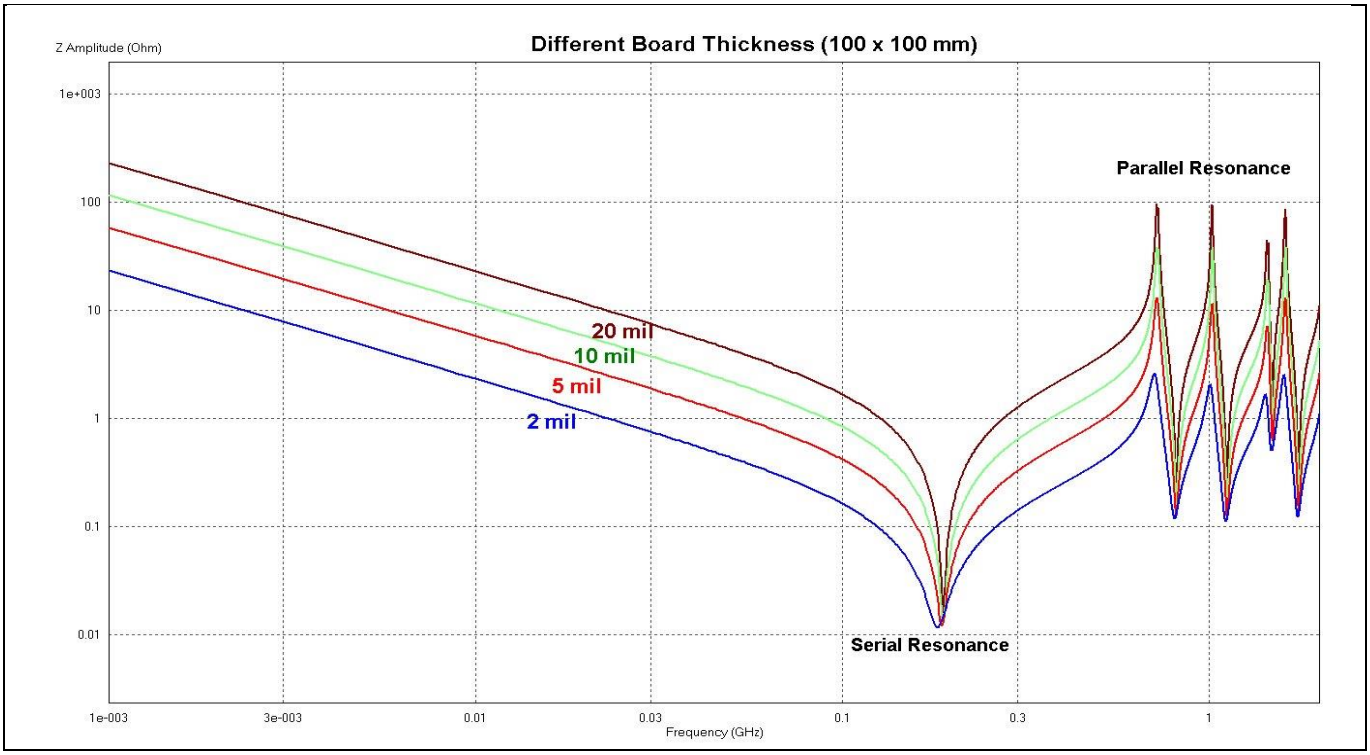


Figure 17 Impedance for different board thickness and plane dimensions

In some cases the grounds should be separated to reduce propagation of noise. This is possible only in low speed systems. In high speed systems care should be taken because a cut in the ground plane may affect the high frequency noise path. High frequency signals require a homogenous ground reference.

Figure 18 gives an example of a local oscillator ground island which is carved out of the global ground plane.

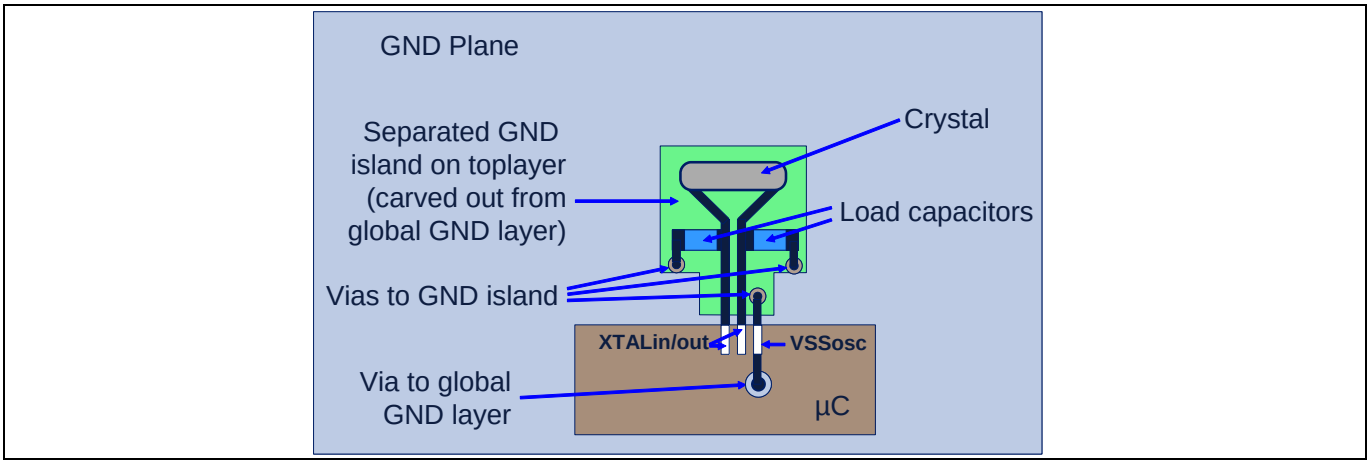


Figure 18 Layout example for crystal oscillator circuit

The oscillator current loop formed between the external oscillator components (crystal, capacitors) and the oscillator VSS pin VSSosc at the microcontroller must not contain any contact to the global ground plane. The global ground plane should be connected on the opposite side of the VSSosc pin. Ensure that the two load capacitors are placed between the microcontroller's oscillator pins and the crystal.

3.1.1.1 Two-layer boards

Each component should have its own power/ground system. It is not easy to realize this in two-layer boards. Generally there are two concepts to design a power distribution on two-layer boards (see **Figure 19**).

The power connections over the whole board can be designed as a star connection. The distribution of the power to each component can be routed from the regulator output by traces. A power island can be placed at the regulator output to realize the star point. It is also important that all supply traces have ground as their reference.

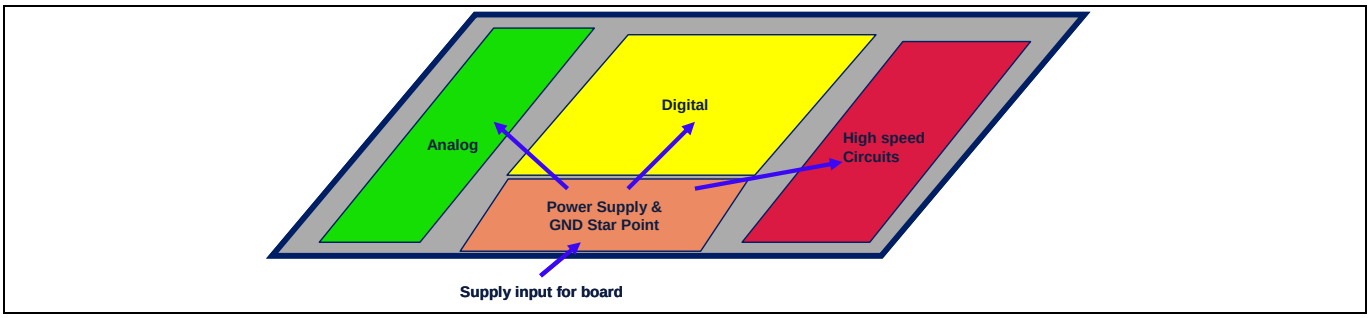


Figure 19 Power/Ground distribution example with star connection system

Another good solution for the power network in two-layer boards is to build a grid system with ground and supply nets:

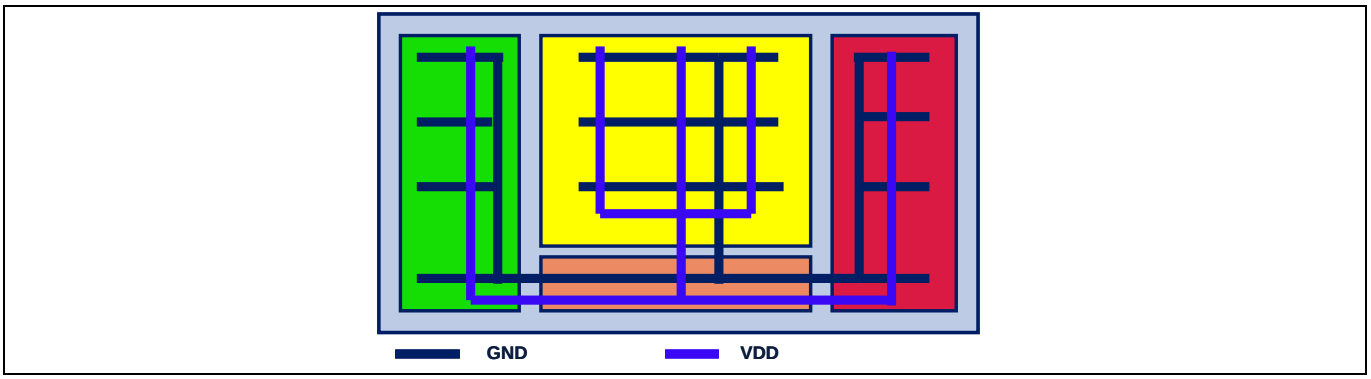


Figure 20 Example for the grid power system on the PCB shown in Figure 19

The ground and supply nets are routed over the whole board on each layer. The traces of each power system (GND/VDD) on each layer are connected by vias. With this grid it is possible to provide a low-impedance connection of the power system to each location on the board. Generally, traces on the top-layer of the board are routed in vertical and on bottom layer in horizontal direction so that it will be easy to realize the grid system. But this solution requires a trade-off with signal traces changing layers which cause impedance changes of the traces.

3.1.1.2 Multilayer boards

For the design of a multi-layer board, the selection of the construction plan is very important. This construction plan, called stack-up, can be built with the technological data of the manufacturer. It depends on the requirements of the high speed design. Some samples of 4-layer and 6-layer board stack-ups are shown:

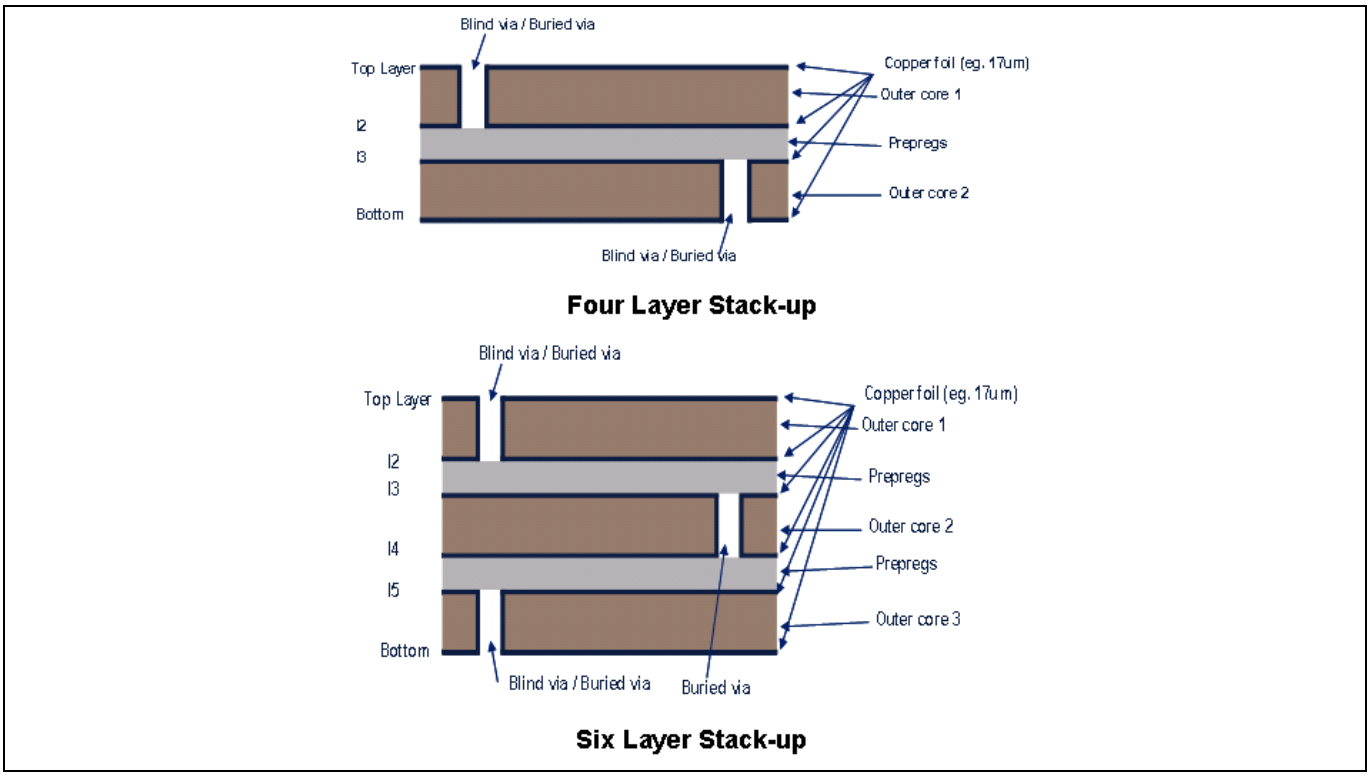


Figure 21 Stack-up examples for four and six layer PCBs

Design at least one power/ground layer pair. Realize power and ground planes on adjacent layers. The smaller the distance between power and ground layer, the lower becomes the impedance of the power supply. The target distance between the layers can be reached with substrates and prepregs of different thickness.

Use the shielding effects of supply planes to reduce electromagnetic emission. If you have more than four layers, you may route a signal layer for critical traces between two continuous ground/power layers. This provides a good current return path which is not interfering with other signals. It is also effective as a shield against radiation to the outside of the PCB. If there is enough space, implement more extra ground planes in your layer stack so that each signal layer has its own corresponding ground layer. Having an extra ground plane for a signal layer makes it possible to keep the determined characteristic wave impedance.

Different stack-ups for the VDD and GND layers can also be considered for an EMC- optimized board design. The simulation results in **Figure 23** show a comparison of the effect of three different stack-ups:

Design measures

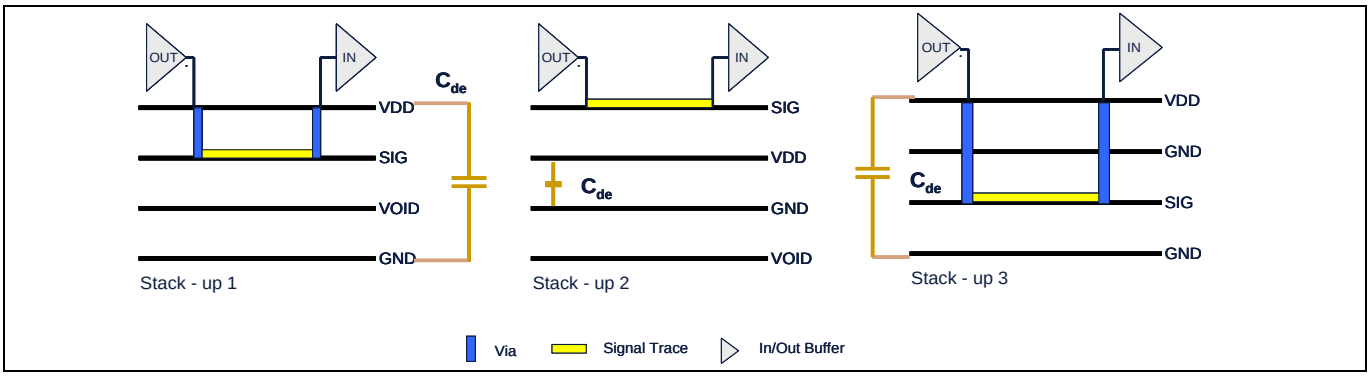


Figure 22 Different stack-ups for reference plane

In the first case the signal layer is placed between the VDD/GND layers. In the second case the signal layer is placed on the top-layer. In the third case the signal layer is placed between two GND layers.

The resulting currents flowing through the decoupling capacitor are displayed in the next figure:

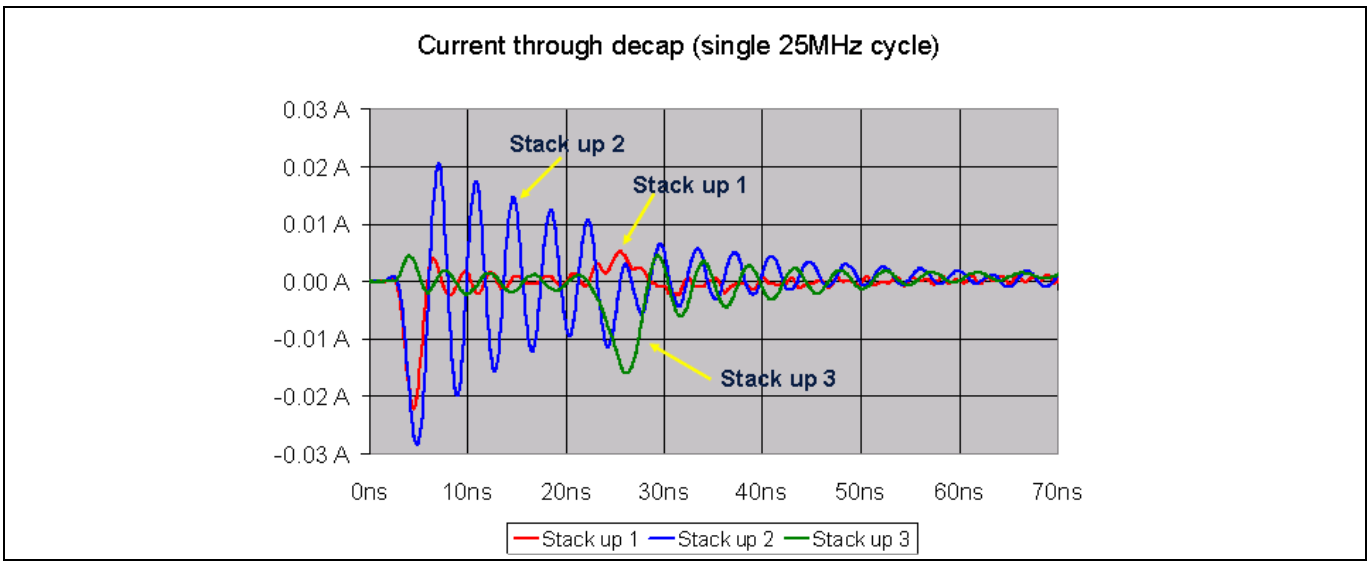


Figure 23 Current through decap for different stack-ups

The stack-ups with the signal layer embedded between the GND/GND or VDD/GND layers deliver best results. But it must also be taken into account that an increased distance between the VDD and GND layers decreases the plane capacitance of the board. The plane capacitance supports the decoupling effect of the board at high frequencies.

Placing noisy signals like clock traces between two ground layers can avoid a lot of radiation problems.

It is also important to select the right layer for critical signals. Designing critical signals as stripline can reduce the switching noise on the power network VDD. **Figure 24** shows a comparison of noise levels on VDD in case of different layer routing of a signal trace (stripline versus microstrip). The advantage of a stripline layout can be seen clearly up to 500 MHz. For the construction of stripline and microstrip configurations see **Figure 43**.

Design measures

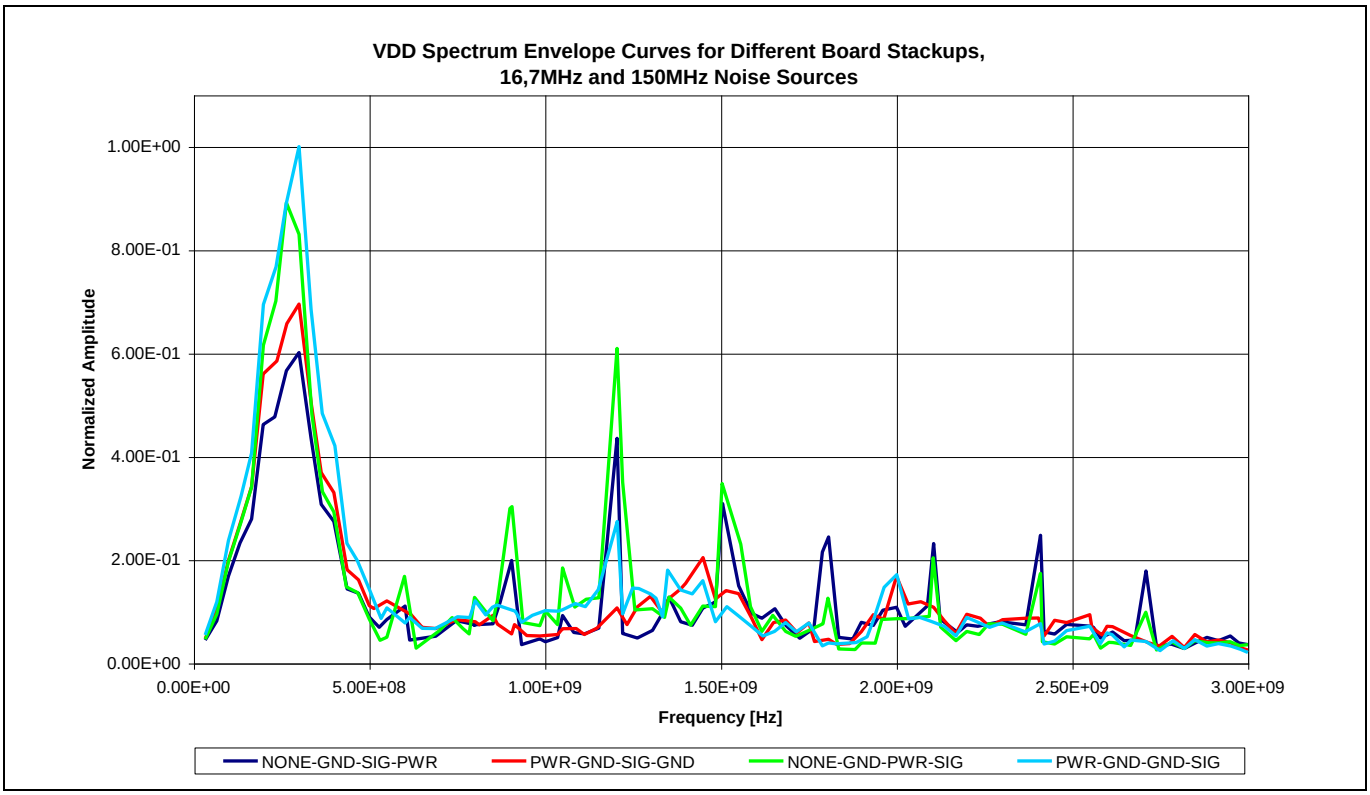


Figure 24 Noise level on power network with different stack-up configurations for the signal line

The connection of the decoupling capacitors is important in the high frequency range. While the connection on two-layer PCBs are made with traces, on multi-layer PCBs the connection can be made through vias directly to the power/ground layers. Depending on the length and width of the traces, the parasitic inductance takes effect on the impedance and also on the decoupling efficiency. A comparison between the via and trace connection of a decoupling capacitor shows that a via connection has lower impedance above 400 MHz. Additionally it can be seen that the trace thickness also plays a role as the impedance decreases with increasing trace thickness.

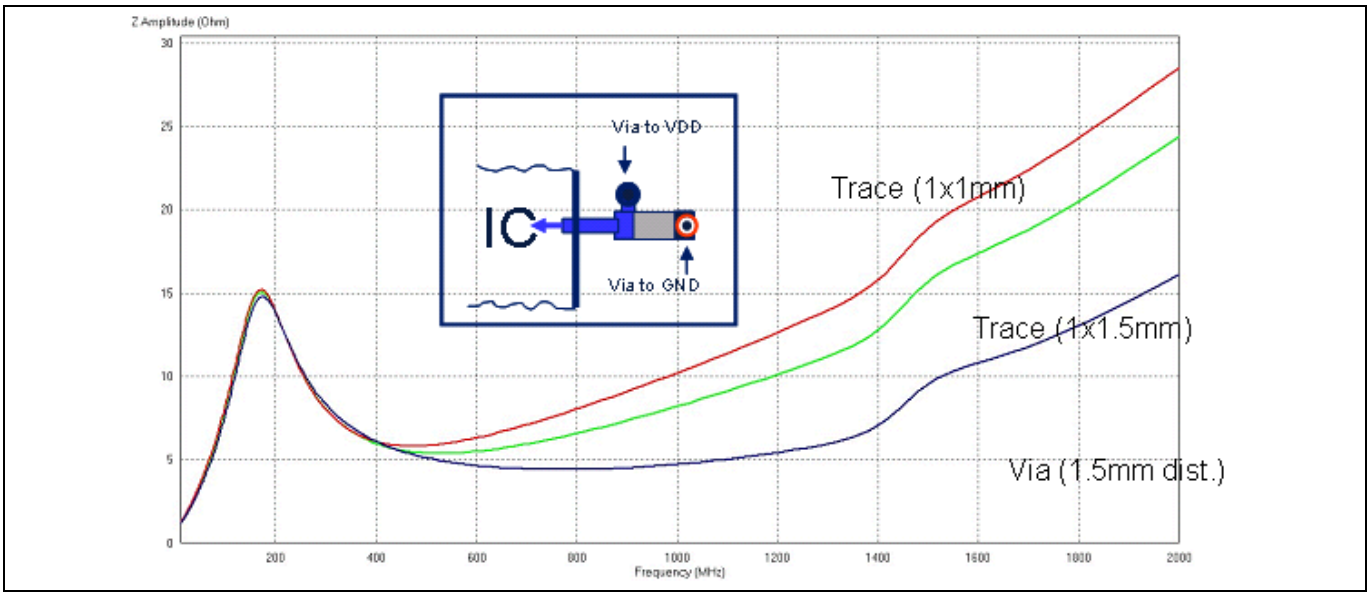


Figure 25 Impedance comparison of different connection types (via connection versus trace connection of decoupling caps)

3.1.2 Components

Passive components are used to reduce the electromagnetic emission in circuits. For the optimum usage of these components, their behavior has to be understood.

3.1.2.1 Capacitors

Capacitors are used to deliver required energy locally while circuits are switching. They reduce the power supply radiation loops.

There are two types of common capacitors: aluminum/tantalum and ceramic capacitors.

- Aluminum / tantalum capacitors
  - Used mainly for bulk decoupling at supply lines. The capacitance value decreases with increasing frequency. But tantalum/aluminum capacitors have a very stable temperature and bias behavior. For the applications where high values are required, tantalum capacitors should be preferred.
- Ceramic capacitors
  - Due to their low ESR they are preferred for the decoupling at ICs. They are more stable in the high frequency range. For filtering, both tantalum and ceramic work well. The impedance at interesting frequencies is very important for the decision of capacitor type and value.

The following figure shows the equivalent RF circuit of a capacitor. Besides the pure capacitance there is an equivalent series inductance ESL and an equivalent series resistance ESR as parasitics of the capacitor.

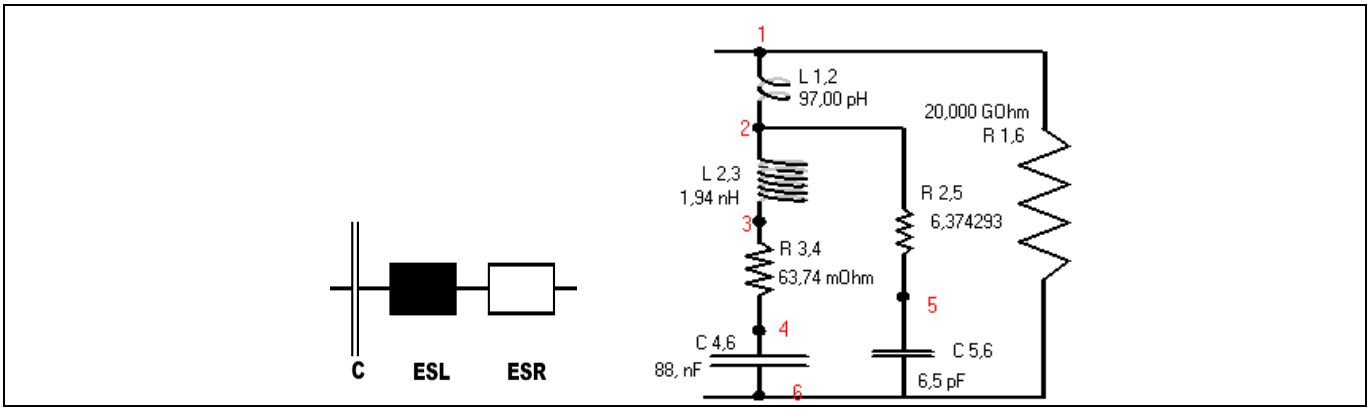


Figure 26 Equivalent circuit of capacitor (simplified manufacturer model)

A capacitor shows capacitive behaviour in the lower frequency range; for frequencies higher than the series resonance frequency its behavior becomes inductive. Optimum decoupling effect is found at series resonance frequency. This information is available in capacitor data sheets.

The next figure shows the impedance curves of different capacitor values (1nF, 10nF, 100nF, 470nF).

Design measures

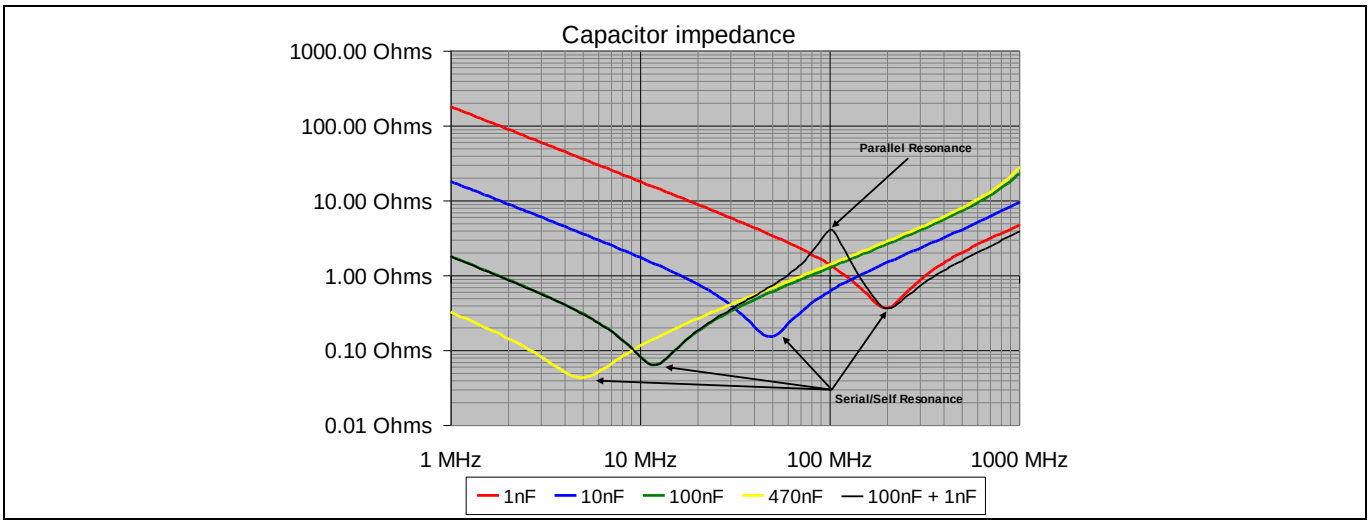


Figure 27 Impedance characteristics of different capacitors

One impedance curve in this figure shows the effect of the parallel connection of two capacitors. A positive resonance (increasing of the impedance at 100 MHz) occurs due to the resonance of inductance of the 100nF and capacitance of the 1nF capacitor. Between the resonance peaks of each capacitor there is an increase in impedance. This is caused by the L of the 100nF and the C of the 1nF capacitor. The 100nF is inductive in this range and the 1nF is still capacitive, so that a resonance is formed. The parallel combination of these parameters forms a parallel resonance which increases the impedance. To avoid or reduce this effect, connect capacitors in parallel with a one or two decade value difference.

For the supply lines, the main target is to reach impedance as low as possible in a wide frequency range. The lower the impedance of the supply system, the higher is the ability of the system to respond to switching current demands. A low impedance supply system can deliver this high frequency current and prevent the RF energy from propagating elsewhere. With the parallel connection of capacitors the impedance can be reduced in a wide frequency range. But one important rule has to be obeyed; the parallel connected capacitors should have value differences of at least factor 10 (for example 100nF and 10nF parallel connection) to prevent higher peaks on the impedance curve due to the parallel resonance.

Selection of decoupling capacitors

For the selection of decoupling capacitors the working frequencies of the application have to be taken into account. The self-resonance frequency of the capacitor must be in the range of the clock or working frequency of the application. The total decoupling concept has to cover some harmonics of the fundamental frequency. The self-resonance frequency can be calculated by the equation:

$$X_c = \frac{1}{2\pi f C}$$

Where:

- Xc = capacitance reactance
- f = frequency
- C = capacitance value

Take care of additional resonance frequencies caused by decoupling.

Design measures

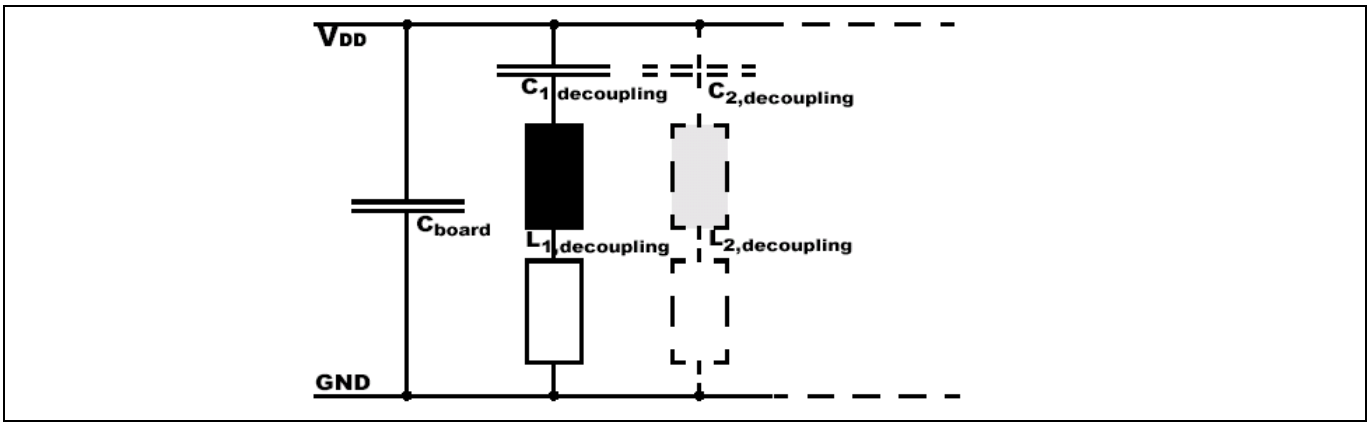


Figure 28 Additional resonance frequencies

The figure above shows an equivalent circuit of a decoupled power bus which consists of the capacity of the planes Cboard on one side, on the other side there is the equivalent circuit of the decoupling capacitor. This structure is an oscillator with certain resonance frequencies. If one decoupling C is used then there is just one resonance frequency. In case you use two or more values of capacitors, check for additional resonance frequencies.

Using Surface Mounted Device (SMD) capacitors reduces additional lead inductance. The inductance causes the increase of the impedance curve. To get an optimum decoupling effect, the total inductance along the connection path of decoupling capacitors has to be minimized.

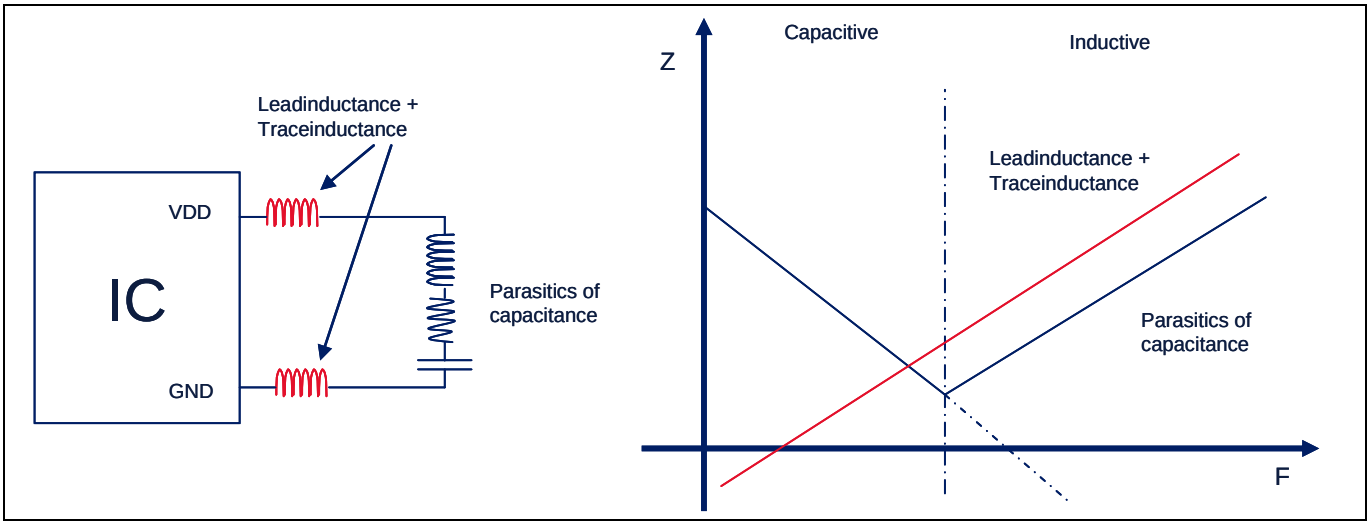


Figure 29 Effect of the inductance on impedance characteristics

Figure 30 clarifies the effect of lead inductance. The effect is mainly visible in the high frequency range. This means that the decoupling is less effective in high frequencies with increasing inductance along the decoupling path.

Design measures

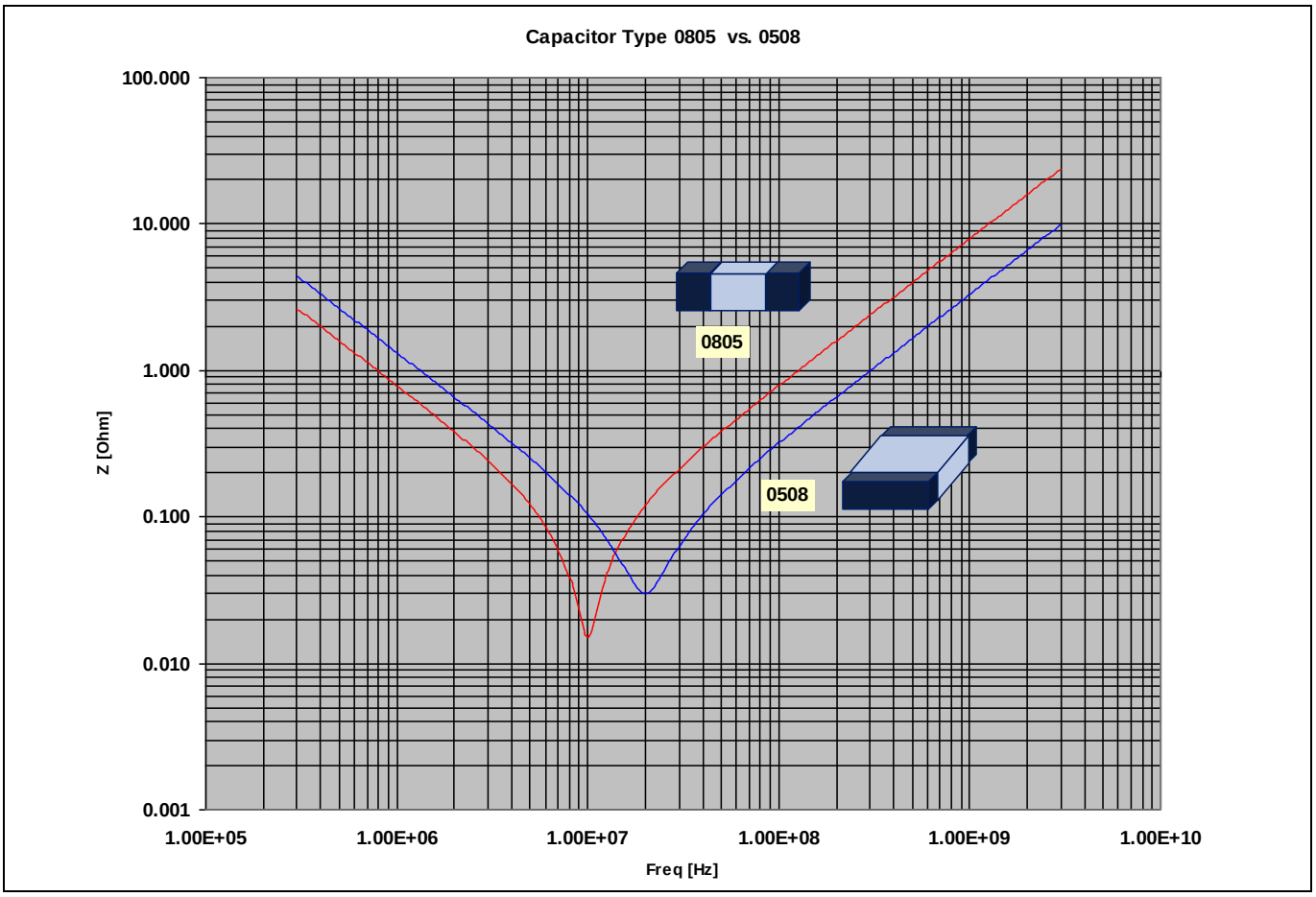


Figure 30 Low ESL package 0508 versus standard package 0805

The low ESL types of capacitors (**Figure 30**) have optimized packages with a reduced inductance value and provide further inductance reduction.

The development of new technologies have allowed the manufacture of high-value multi-layer ceramic capacitors which have values up to 10 ~ 22µF. Using these capacitors, lower impedance values can be reached and the total decoupling capacitor count can be reduced, so saving cost. But as it can be seen in **Figure 31**, the capacitors are only effective up to ca. 100 MHz.

Design measures

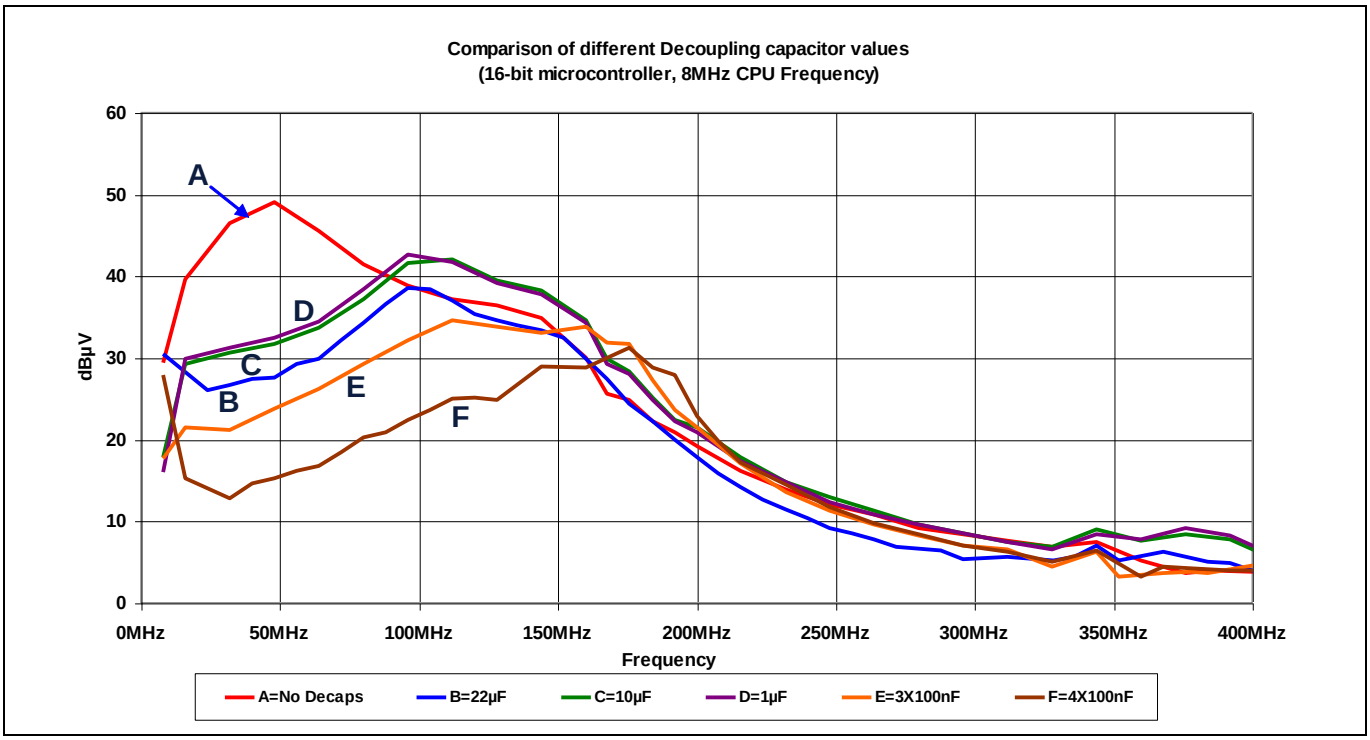


Figure 31 Comparison of different high value decoupling capacitors

In general the suggested value for ceramic capacitors to decouple the power pins of the microcontroller is in the range from 10nF to 100nF. Capacitors have a limited frequency response which prevents them from delivering power at higher frequencies. Therefore other values of capacitors have to be chosen if special frequencies are critical. For global decoupling of the power system, single capacitors in the value range of 10nF up to 100nF are typical. It is efficient to place different values in parallel (while considering the anti-resonance on impedance). Decoupling at the connectors and the power supply star point (e.g. voltage regulator) should be realized with additional tantalum-electrolyte capacitors.

Beside the capacitive effect of the ground plane under the microcontroller, the fast current has to be delivered from the discrete decoupling capacitors. Decide on pin-decoupling or/and global decoupling strategies.

Layout measures for decoupling capacitors

By pin-decoupling each pair of VDD-GND pads is first contacted to the capacitor(s) and then to the supply layers/nets.

- Advantage;
  - Optimised decoupling for every pin possible.
- Disadvantage;
  - High number of capacitors required.

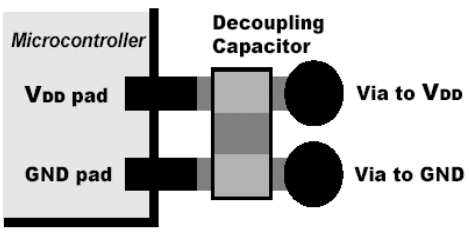


Figure 32 Placement of blocking capacitor

Design measures

Place the capacitor pads as close as possible to the microcontroller's VDD/GND pins. First contact the capacitor, then contact the vias to GND and VDD plane (see **Figure 32**). The connection from the decoupling capacitor to the ground plane can also be realized by several microvias inside the outline of the capacitor pad. This guarantees a low impedance and low inductive connection to ground.

If possible keep the decoupling capacitors on the same side as the microcontroller. Remember that vias cause additional inductance. Design traces between pads and capacitor as wide as possible.

If you have to place the capacitors on the bottom side of the board, provide two or more vias in parallel to reduce the connection inductance and think about using microvias if possible. Keep GND-vias and VDD-vias as closely together as possible.

The next figure shows four different connection types of decoupling capacitors to the VDD/VSS planes. The impedance curves of the connection types show a reduction of the impedance if two vias are connected in parallel and further reduction in case of placing the vias directly on the capacitor pads.

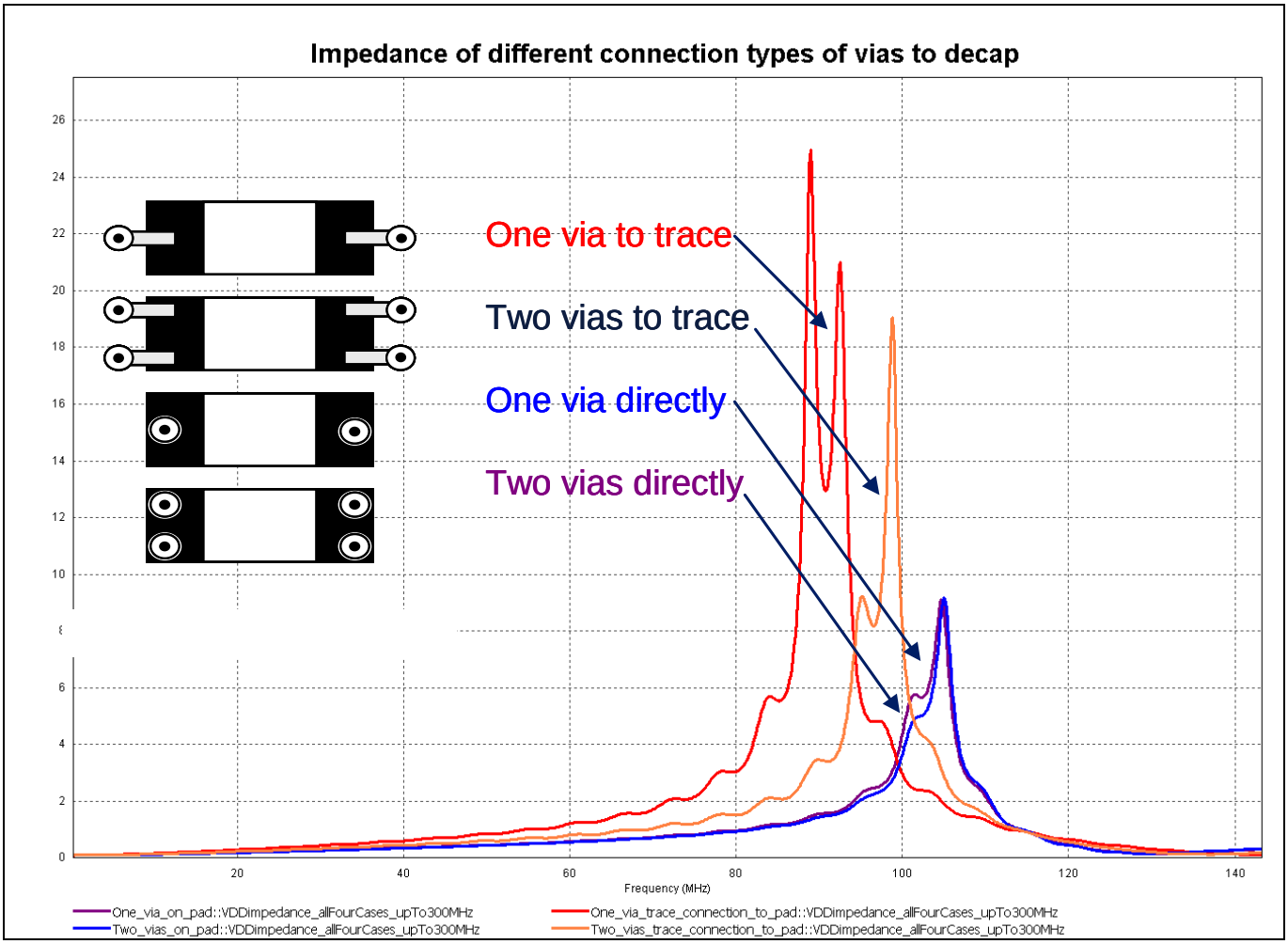


Figure 33 Impedance change caused by different types of decap connections

By global decoupling, each pair of VDD-GND pads is first contacted to the supply layers. The capacitors are placed around the microcontroller, directly contacted to the supply plane.

- Advantage
  - Lower number of capacitors required since some VDD-GND pairs can share one capacitor.
- Disadvantage
  - Larger current loops compared to pin-decoupling.

Design measures

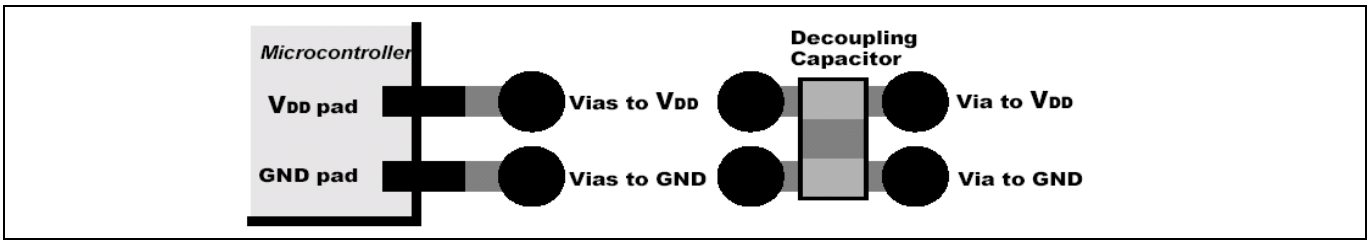


Figure 34 Global decoupling on multi-layer PCB

- Provide at least half as many capacitors of the same value as there are supply pairs at your microcontroller.
- Avoid long traces between µC pads and vias to supply plane (additional inductance).
- Provide two vias in parallel if possible.
- Keep GND-vias and VDD-vias as closely together as possible.

Global decoupling cannot be used on two-layer boards since there are no power supply planes for VDD and GND.

The best decoupling concept is a combination of local and global decoupling. This will imply additional cost for discrete components, but can save much development time and redesign activities for critical applications.

Calculation of decoupling capacitor values

To determine the requirements of optimum decoupling capacitors, the capacitive and inductive values must be calculated. The capacitive value has to be large enough to support local switching current and the inductive value has to be small enough to get low impedance paths to the capacitors.

The steps of calculation of decoupling capacitors are:

1. Determine the tolerable noise level on the power supply.
   - Example: ΔV = 5% -> ΔV= ±125mV for VDD=5V
2. Average current at application: ΔI
   - Determine the maximum impedance:

$$Z = \frac{\Delta V}{\Delta I}$$

3. On-board required minimum capacitance:

$$C = \frac{1}{2\pi F_{tran} Z}$$

Ftran ~ 1 MHz (up to this frequency the current changes will be delivered from the voltage regulator)

4. Calculation of maximum board inductance for the power supply connection to the capacitors:

$$F_{tran,\max} = \frac{1}{2\pi C_{on} Z}$$

Ftran, max = highest frequency where the on-chip capacitance is still effective

C_{on} = on-chip capacitance (from specification of chip or from manufacturer)

$$L_{\max} = \frac{1}{2\pi F_{tran,\max}}$$

Lmax = maximum inductance on supply connection path (trace + via + package)

3.1.2.2 Inductors and Ferrite Beads

The next important components for lower electromagnetic emission are inductors and ferrite beads. If the current produced by the microcontroller cannot be supplied from the decoupling loop, the noise will couple to the power supply lines. The ferrite prevents the noise from spreading out over the power supply line. Even though the ferrite beads were not so popular in the past because of area requirement on board and cost issues, with new technologies it is possible to manufacture multi-layer ferrite chip beads, which have very good impedance characteristics. They are available in standard SMD packages.

As shown in the following figure, the equivalent circuit of the ferrite contains some parasitics and builds a parallel resonance.

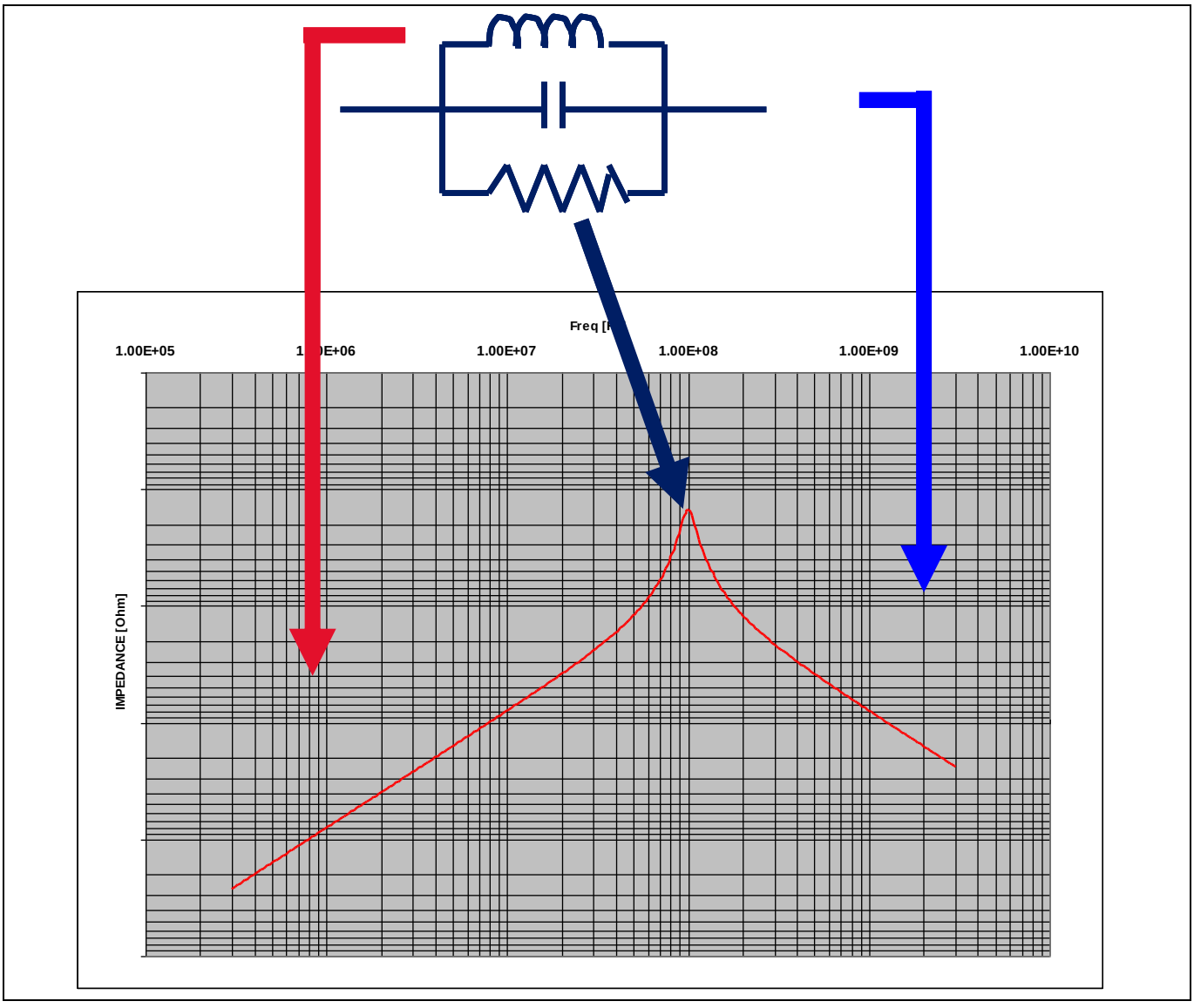


Figure 35 Typical impedance characteristics of an inductor

Design measures

The ferrites have to be placed on the supply line:

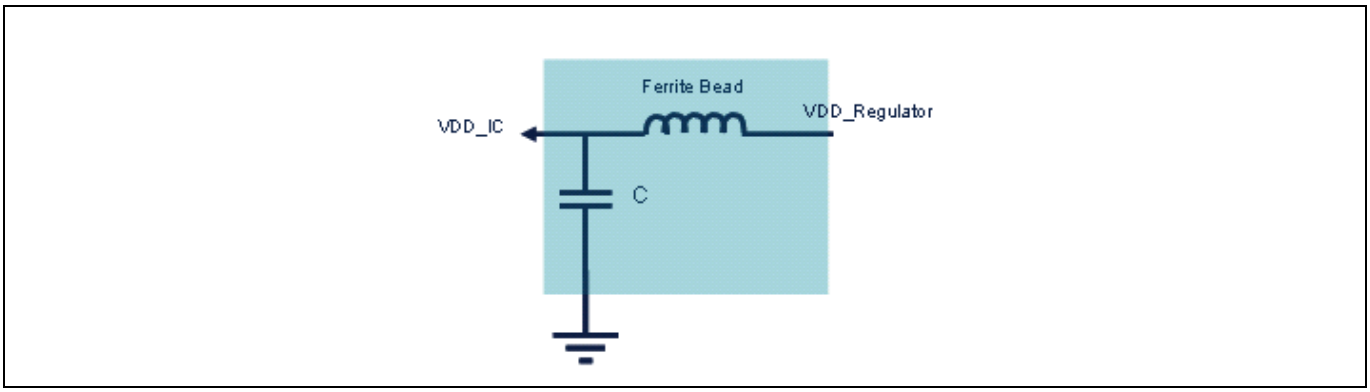


Figure 36 Placement of ferrite beads

The current consumption of the supply path must also be considered with the selection of the ferrite beads. A high current ferrite bead can cause a voltage drop on the supply line.

The noise suppression mechanism is shown:

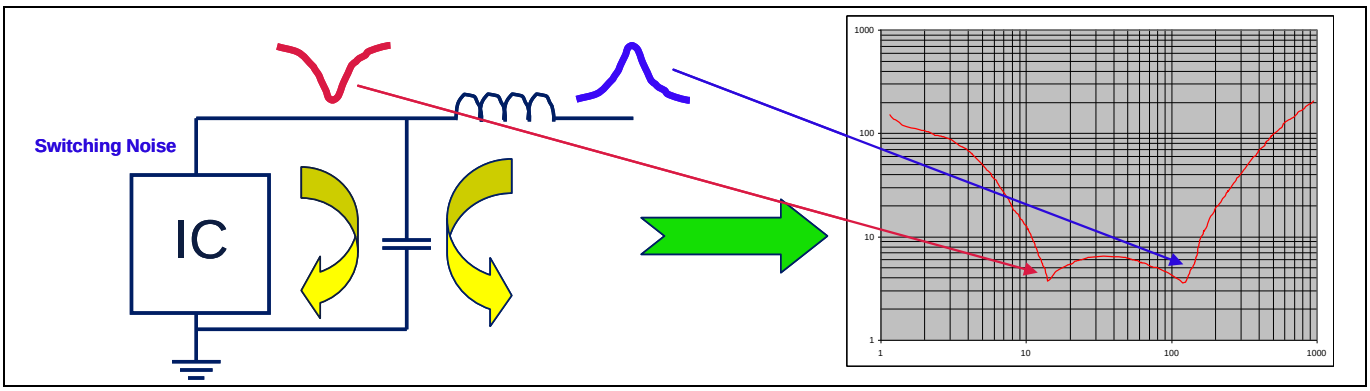


Figure 37 Total impedance of the noise filter circuit with capacitor and chip ferrite bead

The decoupling capacitor has a series resonance in the lower frequency range and the ferrite has a parallel resonance in the higher frequency range. The total frequency behavior of the circuit (seen from the IC side) is drawn in the diagram on the right side.

Some measurement results of a 16-bit microcontroller are shown in **Figure 38** with a ferrite in the supply line (no decaps used). The ferrite blocks the noise on regulator side but the noise on IC side (red curve) is as much as without ferrite (blue curve). The maximum improvement of the ferrite on regulator side (green curve) is about 30dBµV.

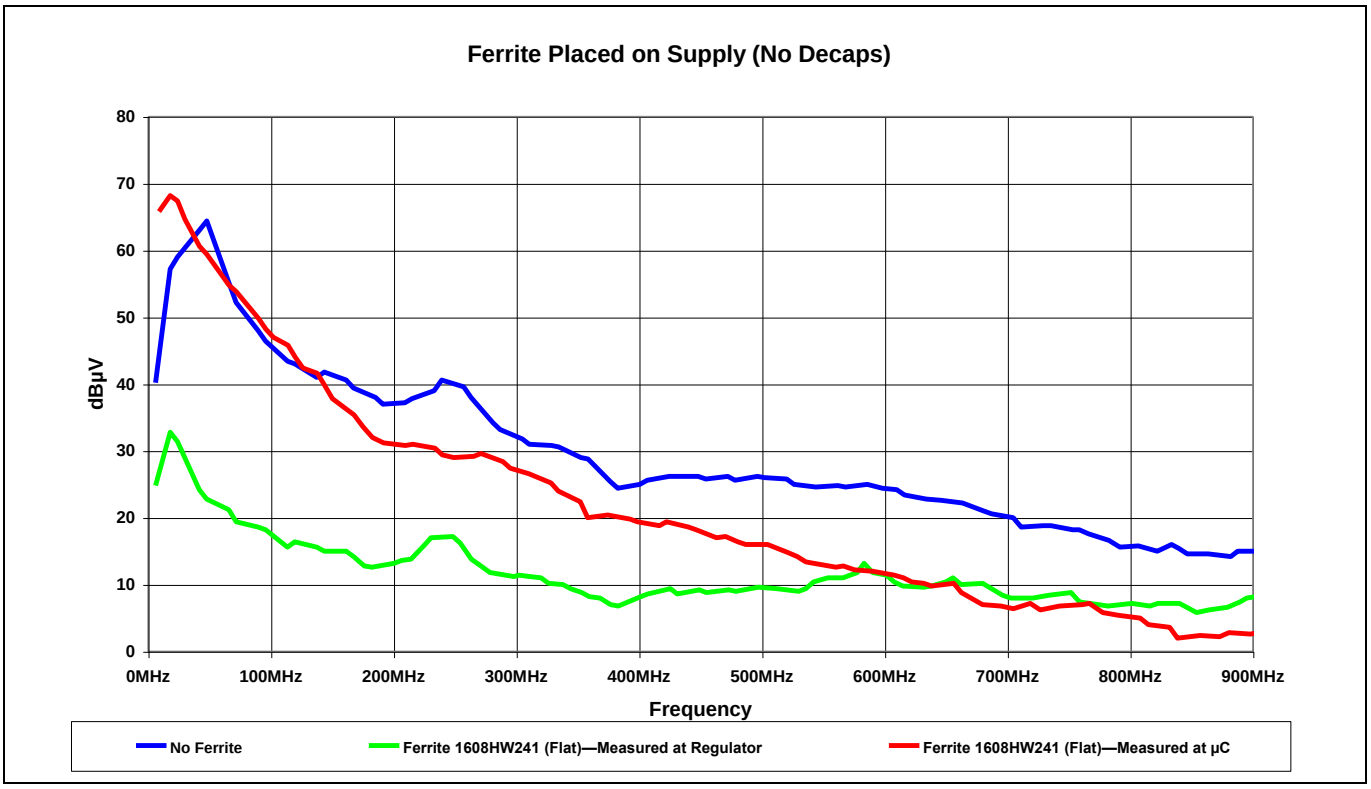


Figure 38 Measurement with ferrite on different points on board (no decaps)

Figure 39 shows the same measurements with additional use of decoupling capacitors. The additional emission reduction by the capacitors delivers an emission level on the regulator side below 10 dBµV.

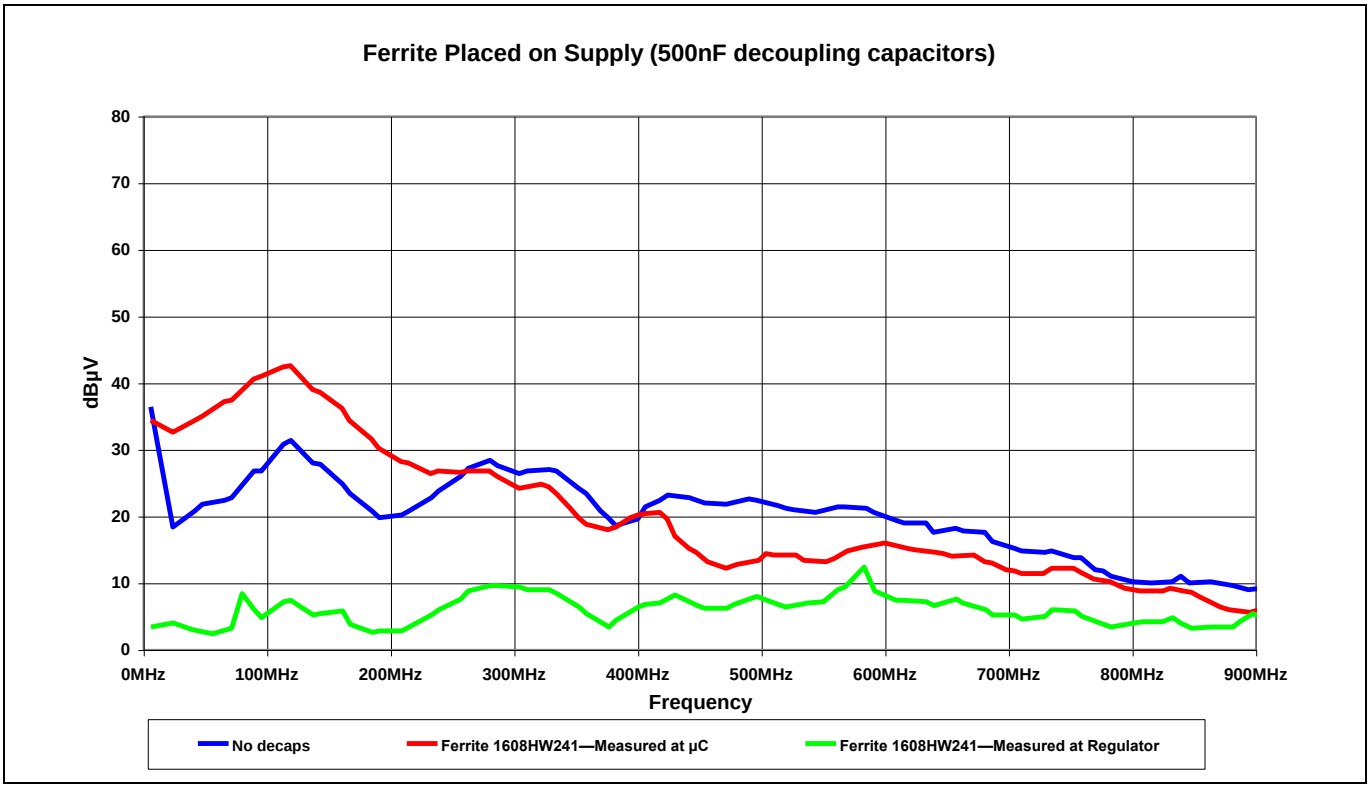


Figure 39 Measurement with ferrite beads on different points on board (with 500nF decoupling capacitors)

3.2 Signals

Before routing, determine critical nets by their rise and fall times, and driver strength. The shorter the rise and fall times are, the more high-frequency components are contained in the spectrum. The higher the signal frequency becomes, the higher the corresponding harmonic frequencies, multiples of the base frequency, are.

This figure shows the spectra of signals with different rise times (worst case setting):

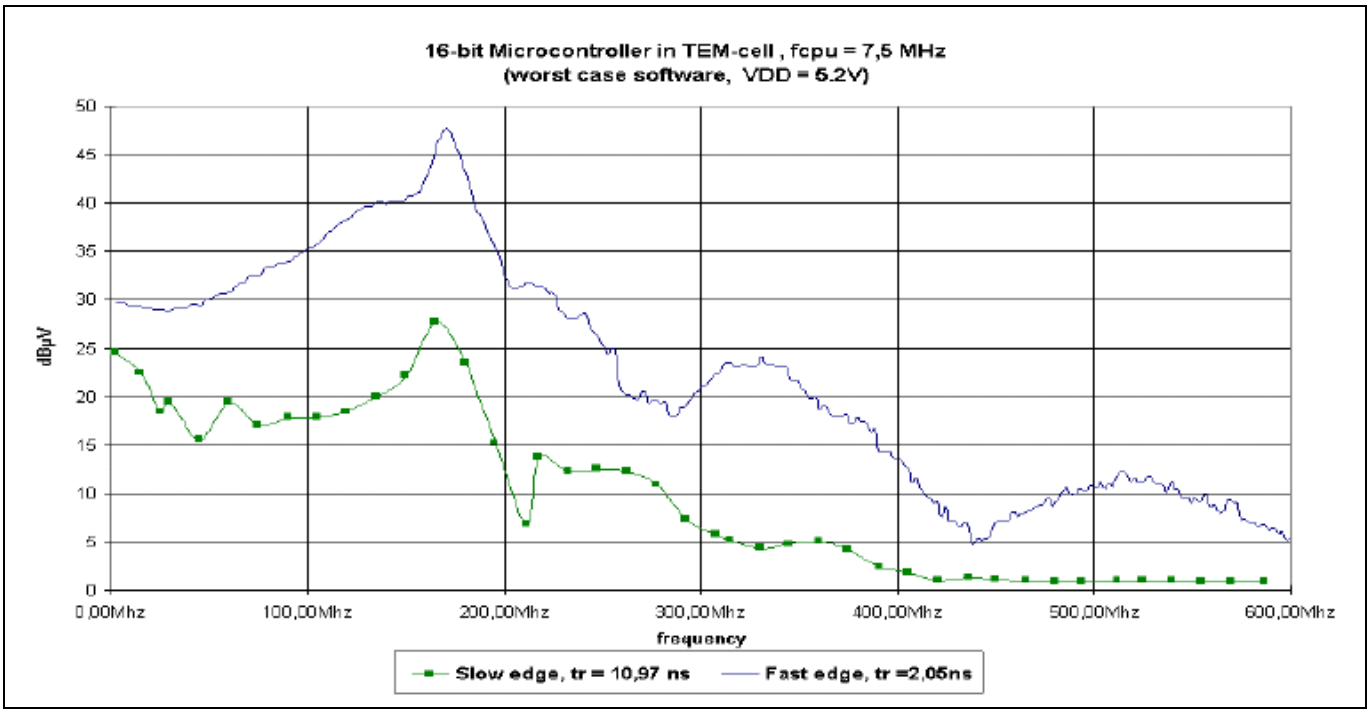


Figure 40 Effect of Rise time on the Spectrum

Typical critical nets (if available):

- Most critical signals in single chip applications are:
  - Clock out
  - SSC (Synchronous Serial Channel)
  - MLI
  - MSC
- Most critical signals in other applications are:
  - Clock out
  - ALE
  - Read
  - Data bus
  - Address bus
  - SSC (Synchronous Serial Channel)
  - MLI
  - MSC

3.2.1 Layout structures for two-layer and multi-layer boards

During the routing some important rules have to be considered:

- Avoid putting traces with high speed signals along the edges of a PCB. Disturbances can be coupled easily into a metal case/shielding of the application.
- Route high-speed signals as short as possible and without vias.
- For high-speed signals, route traces with a corner angle of 45°.
- Do not place sensitive signals close to traces of high current switching signals.
- Route critical signals with a low impedance trace (wide trace, micro-strip, stripline; see **Figure 43**) and if necessary with guard traces.

A simulation result shows that the improvement with guard traces is approximately 10dB:

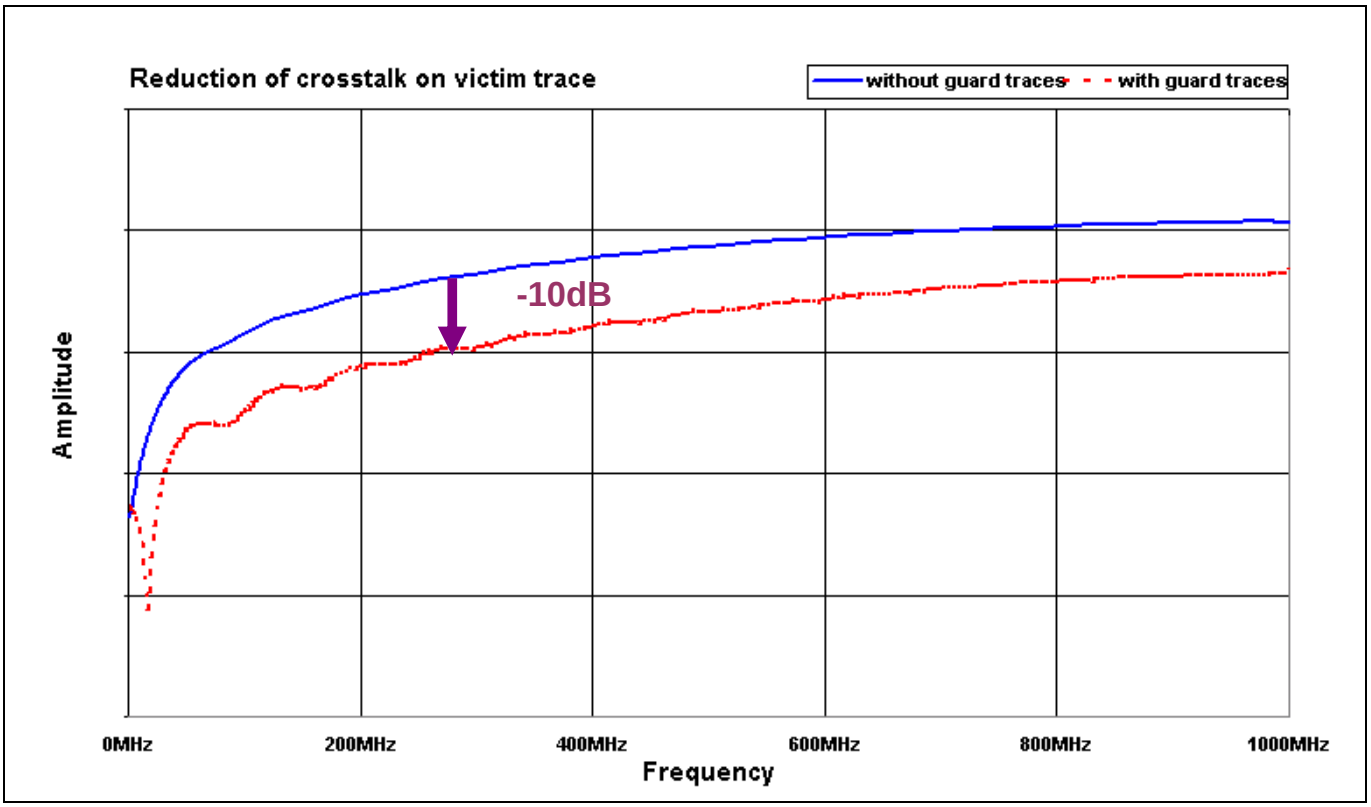


Figure 41 Effect of the guard trace

- Critical signals should be routed away from the signals and traces which lead to the connectors.
- Very critical signals (Interrupt Request and Reset) should be filtered properly. Any noise on these signals can cause malfunction of the whole circuit.
- Low frequency signal return path is along lowest resistance. High frequency (i.e. above 1 MHz) signal return path is along lowest inductance.

Design measures

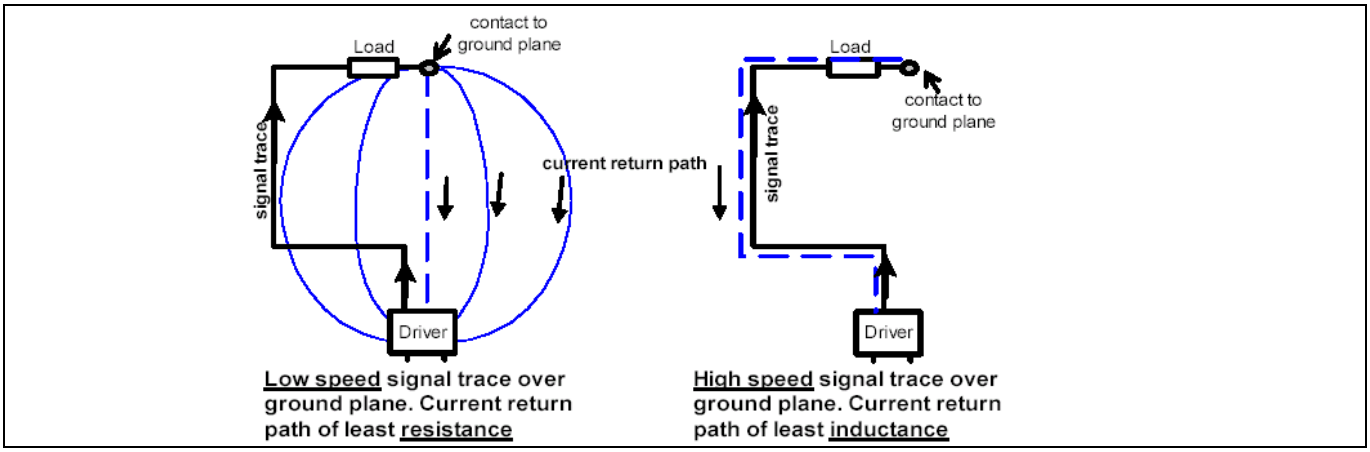


Figure 42 Return current of high-speed signals

- If possible, do not design any signal traces across the separation areas. Due to the slot in the power plane the loop size can be increased. In particular, avoid high-speed nets leading from one zone over to the other one. Design short traces.
- To limit crosstalk (XTalk):
  - Determine a maximum overshoot on crosstalk.
  - Determine a minimum distance / maximum parallel length between high speed nets in order to minimize crosstalk. Use simulation tools for this estimation.
- To ensure Signal Integrity (SI) and radiation:
  - Take care of the characteristic wave impedance of traces when using more than one layer. The possible types of signal lines are microstrip and stripline. A microstrip can be designed when the trace is routed over a ground plane and a stripline can be designed when the trace is placed on a layer between two ground planes.

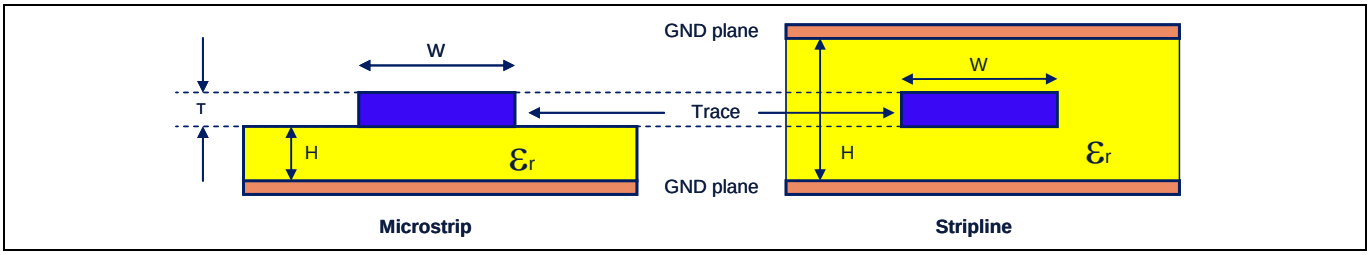


Figure 43 Construction of microstrip and stripline

- Determine widths of especially high-speed traces to guarantee the same characteristic wave impedance over the whole PCB.

The next figure shows the changes in characteristic wave impedance due to a smaller distance trace to ground-plane or due to a wider trace:

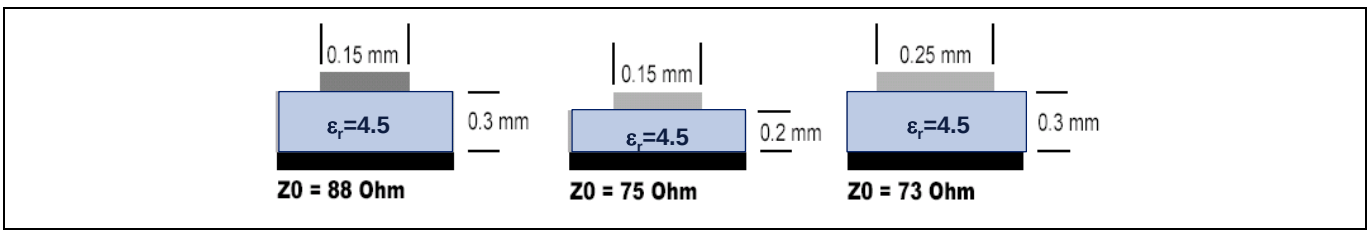


Figure 44 Wave Impedance

Design measures

- If the half rise/fall time of the signal is smaller than the propagation delay of the PCB trace, the trace should be treated as a transmission line. These traces should be terminated with their characteristic impedance. This means that if the critical length is exceeded then the trace should be terminated. The critical length of the traces can be calculated as follows:

$$L = \frac{T_r}{2T_{pd}}$$

$$T_{pd} = \frac{\sqrt{\varepsilon_r}}{c}$$

Where

- Tr is rise / falltime
- Tpd is propagation delay;
- C is speed of light

The characteristic impedance of the stripline can be calculated with:

(Valid when 0.1<W/H<2.0 and 1<ε_{rel} <15)

$$\frac{Z}{\Omega} = \frac{87}{\sqrt{\varepsilon_{rel} + 1.41}}\left[\ln\left(\frac{5.98H}{0.8W + T}\right)\right]$$

For micro-strips the following formula can be used:

(Valid when W/H<0.35 and T/H<0.25)

$$\frac{Z}{\Omega} = \frac{60}{\sqrt{\varepsilon_{rel}}}\left[\ln\left(\frac{4H}{0.67\pi(T + 0.8W)}\right)\right]$$

Where:

- H is height of dielectrica between trace and ground plane
- W is width of trace
- T is height of trace

Design measures

Termination methods

A mismatch between the output impedance of the driver and the line impedance causes reflections on the line. These reflections influence the performance of the circuits. The most popular measure against the reflections is to use terminations. There are different methods to realize the terminations.

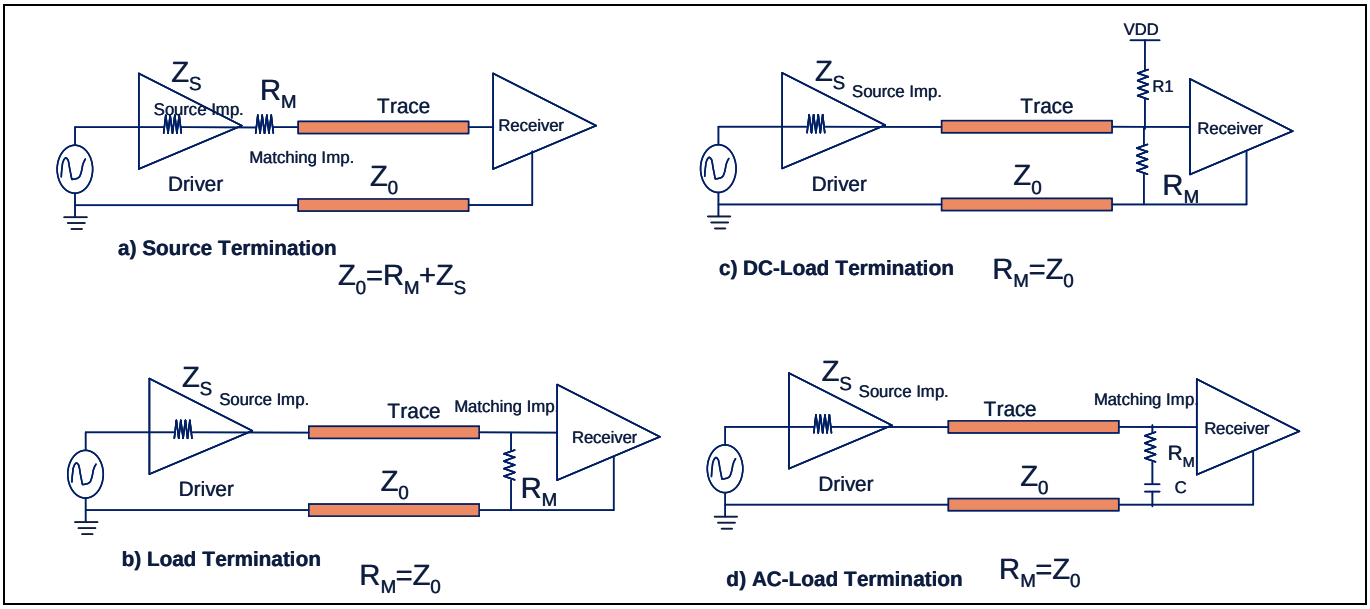


Figure 45 Source, load, DC-load and Ac-load terminations

- Source termination

If the characteristic impedance of the line is matched on the source side, the line is **source** terminated (**Figure 45a**). In this case the reflections will be cancelled at the source because of the matching and zero reflection coefficients. The output impedance of the driver should be subtracted from the ideal value of the source termination.

- Load termination

If the termination is placed at the end of the line, the line is **load** terminated (**Figure 45b**). The reflections will be cancelled at the end of the line. The received voltage is equal to the transmitted voltage. A variation of the load termination is the DC biasing termination, with a resistance connected to the supply in addition to the resistance to the ground. The parallel combination of both resistances must be equal to the characteristic impedance Z0. The source termination results in a slower rise time of the signal and smaller reflections than for load terminations.

- DC and AC load termination

Because of the often unacceptably high DC current consumption in case of **load** termination, two other types of termination can be used: DC-load termination (**Figure 45c**) and AC-load termination (**Figure 45d**).

Termination goals

There are three goals for termination:

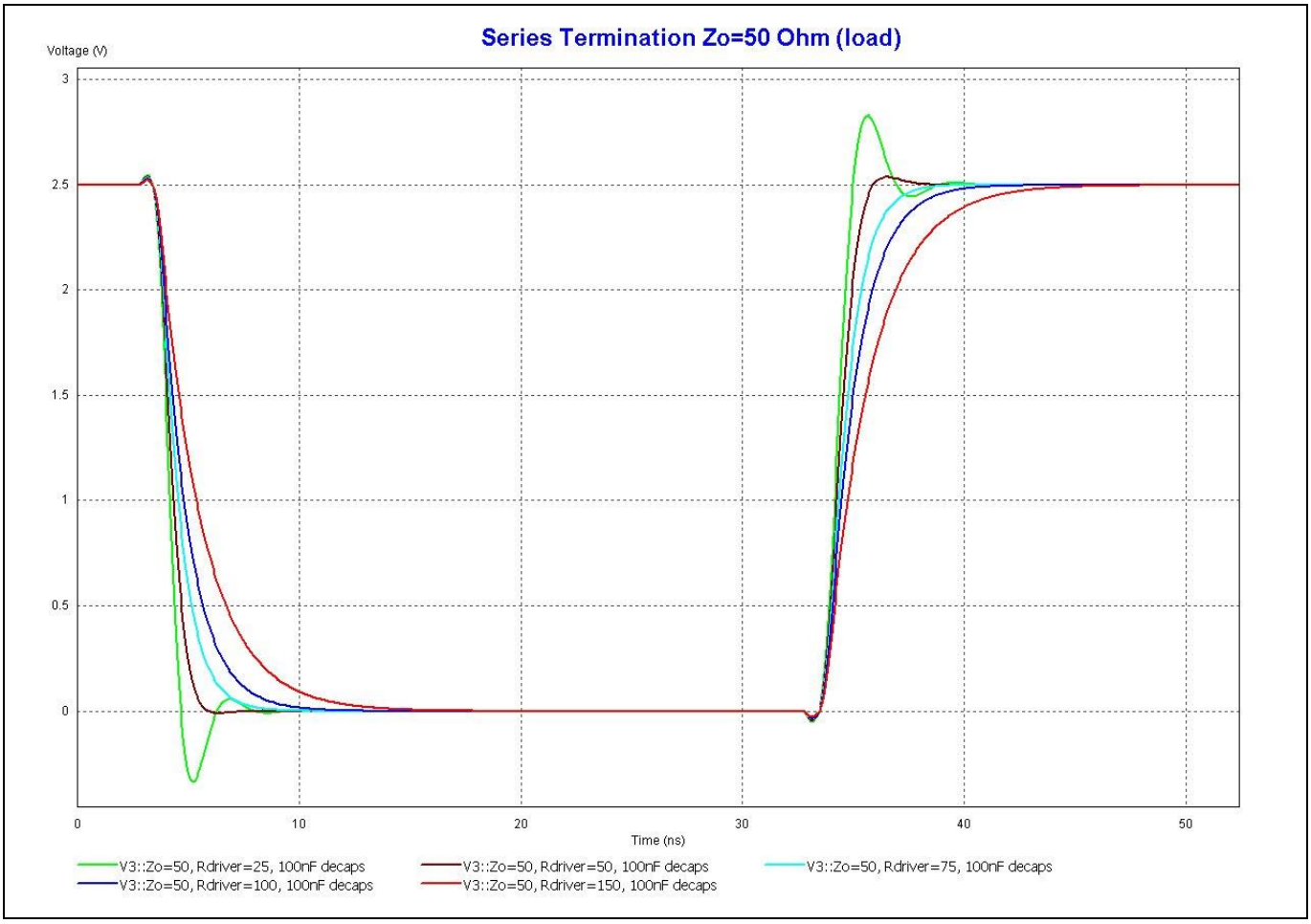
- minimize reflection
  - To minimize reflection, match the driver's Ri with Z0 by a series resistor Rx close to the driver. A matching termination of a high speed signal trace on both sides is very important, especially when the rise time of the driver signal is short in comparison to the signal propagation delay.

Design measures

- voltage swing
  - To optimize the voltage swing, determine a series resistor Rx that cuts half of the voltage swing on a two-point-net (with characteristic wave impedance Z0) while regarding the non-linear Ri.
- emission
  - To minimize electromagnetic emission, provide resistors (20-200 Ohms) and adjust for a smooth rising edge. If provided in the microcontroller, use software settings for edge and driver strength control.

To ensure signal integrity and reduce electromagnetic emission, you should provide series resistors close to the drivers. Optimize their values by simulation or by approximate calculation from VI-tables of the driver and the trace impedance.

The simulation results in **Figure 46-Figure 47** show that both series and parallel terminations deliver best signal integrity behavior if the source or load termination matches with the driver´s output or trace impedance.



Design measures

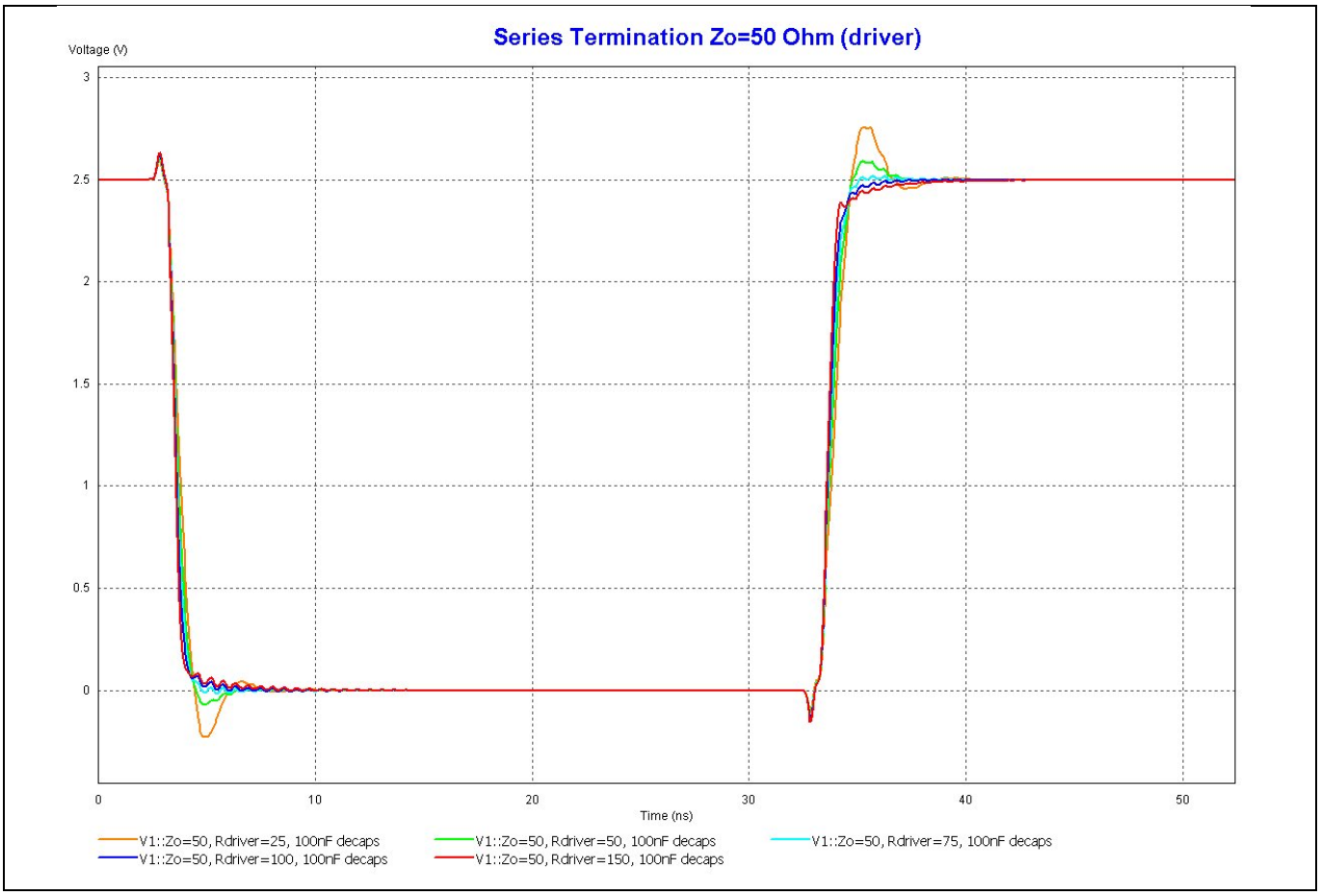
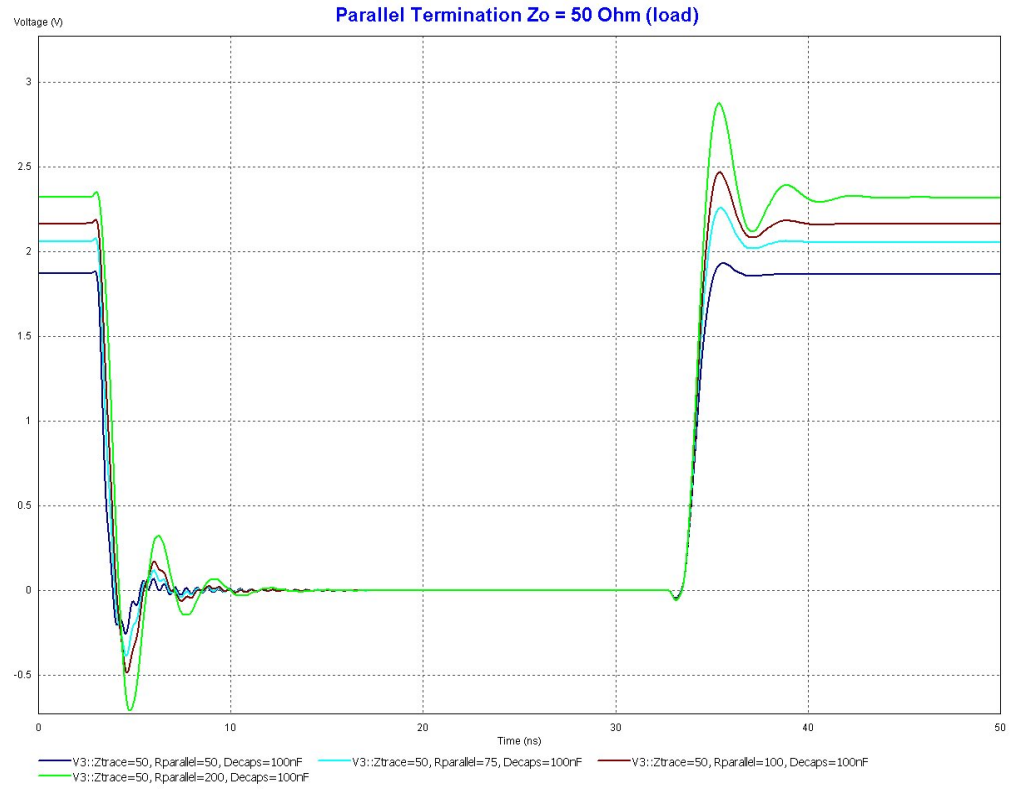


Figure 46 Series source termination of a 50 Ohm trace with 25/ 50/ 75/ 100/ 150 Ohm impedances (signals at source and load)

Design measures



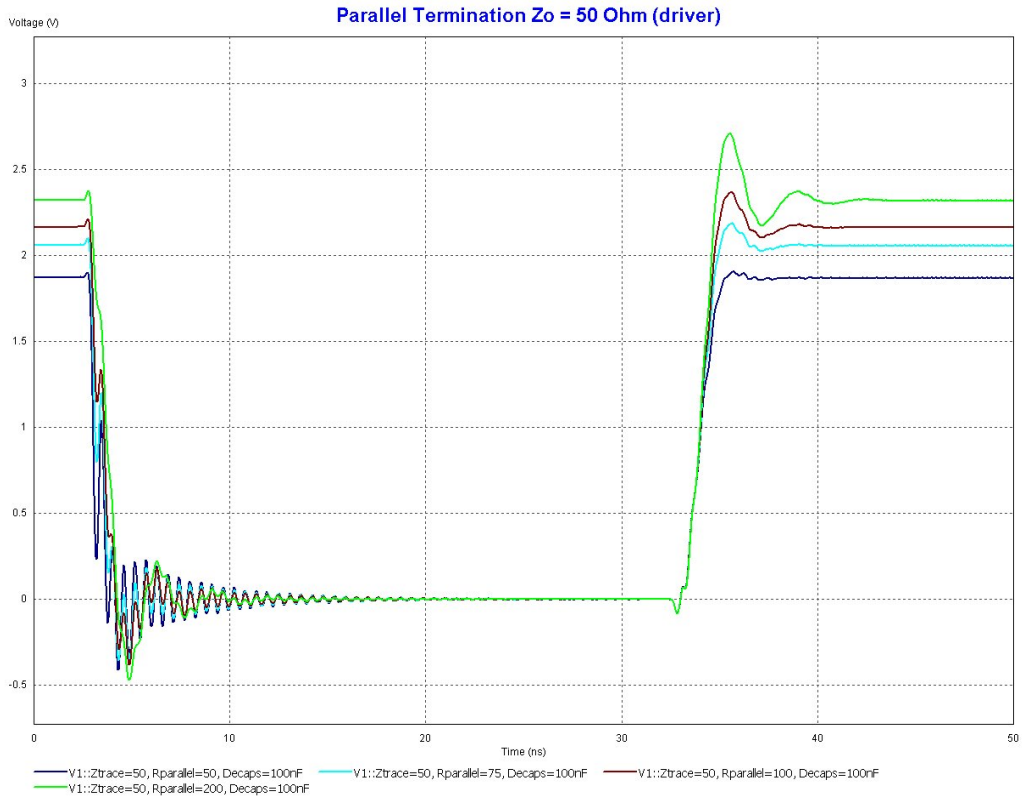


Figure 47 Load termination of a 50 Ohm trace with 50/ 75/ 100/ 200 Ohm impedances (signals at source and load)

Use controlled impedance for critical signals. To reach the termination targets (as explained above), calculate the impedance of the trace from the technological and geometrical data of the PCB.

Design measures

Critical signals should be routed with a ground reference, if possible as a strip line on a power layer surrounded with ground.

Avoid overlapping power planes in multi-layer boards because the noise is easily coupled between the different supply domains.

Keep the return current path as short as possible for high-speed traces. In boards of four or more layers, avoid gaps or batteries of vias within a ground plane in order to keep the loop of the current return path small. On two-layer boards provide power and ground nets close to the high-speed trace.

The smaller the return current loop the lower the electromagnetic emission will be.

Note: Keep in mind that return currents can also use the VDD system!

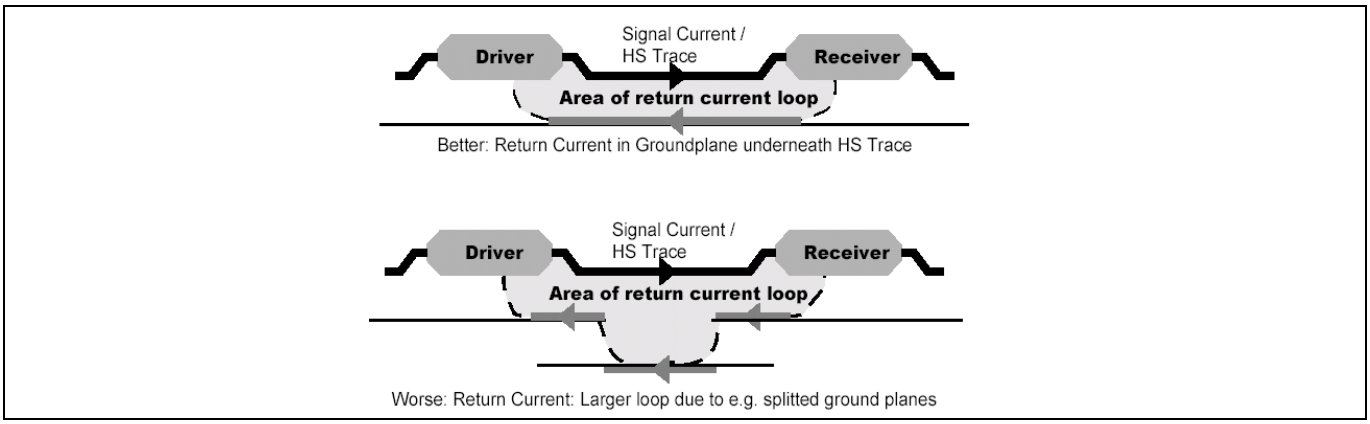


Figure 48 Return current loop area for multi-layer boards

If fast signals are provided on the PCB, design a ground ring around each layer of your board. This ground ring should be connected by several vias along the edge of the board to the reference ground plane. The distance from one via to the next should not be longer than 5mm. This builds a reference ground ring around the board which helps to decrease radiation from the inner layers. It also prevents the problem of currents at the edges of the PCB building antenna structures and radiating outside. If very high frequencies are transferred, the distance between the connecting vias has to be even smaller. The efficiency of this measure increases if you have more ground planes. Then this construction forms a faraday cage for the middle signal layers.

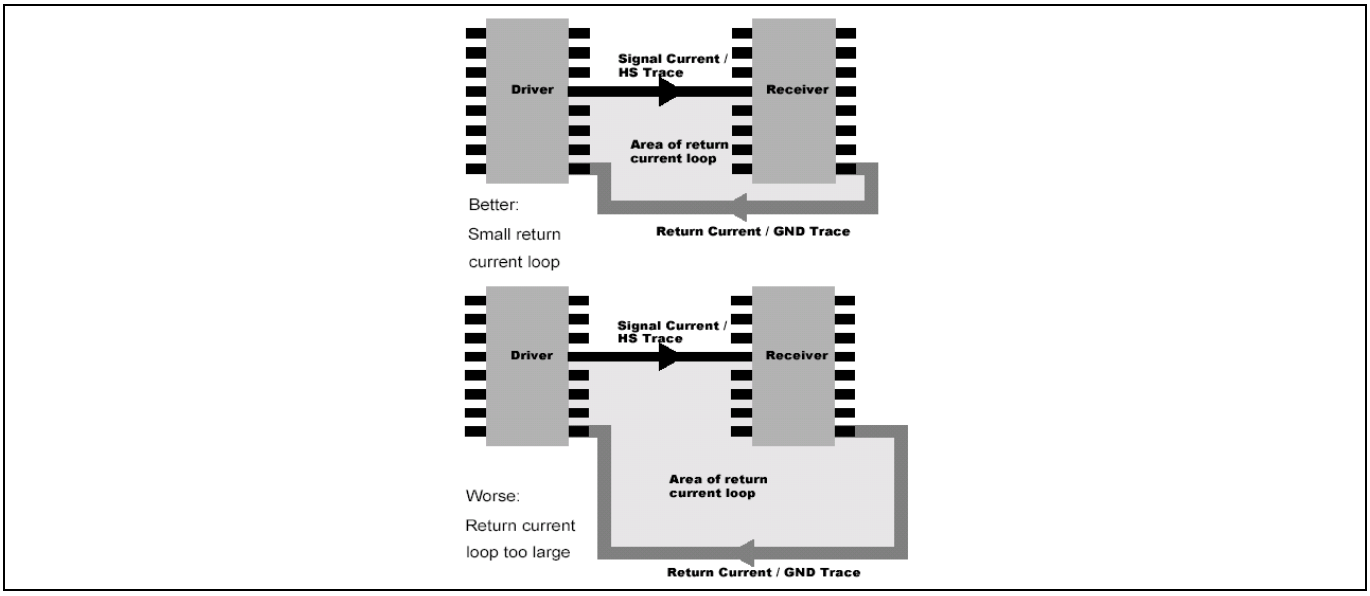


Figure 49 Return current loop area for two-layer boards

Design measures

Avoid vias in high speed traces and through the power planes. Vias through the power planes can cause coupling of the signal to the power supply network. Vias have an additional inductance of ca. 0.5nH ~ 1nH.

Avoid turns in high speed traces. Turns mean a change in the characteristic wave impedance of a trace. Better use 45 degree turns (or even less!) instead of 90 degree turns. 90 degree turns cause a change in the trace's width. Changes in the trace's width cause changes in the characteristic wave impedance which will result in undesired reflections.

Provide room for a series resistor close to the driving component. If you have not set up a specific design rule yet, optimize the resistor value.

If you have two adjacent signal layers, realize x-y-tracing to reduce crosstalk. Place and layout decoupling capacitors.

Finally, design all other traces. The guidelines in this section should also be kept in mind for those other traces.

3.2.2 Components

3.2.2.1 Resistors

Resistors are used for impedance matching, biasing, and pull-up / pull-down circuits. Resistors are commonly used in Surface Mount Packages (SMD). This package type has low parasitic elements compared to the lead packages.

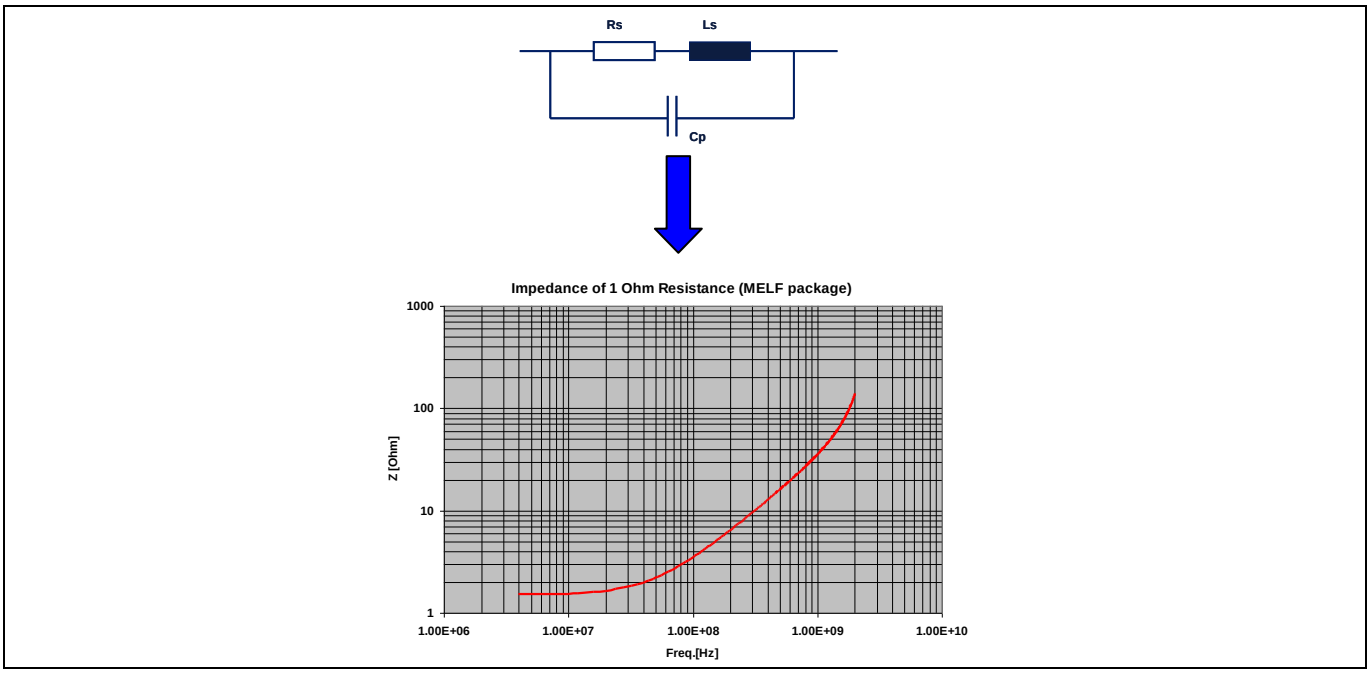


Figure 50 Equivalent circuit of a resistor and impedance of a 1 Ohm resistor

This figure shows the equivalent circuit of a resistor and the impedance characteristic of a 1 Ohm resistor. Impedance increases at higher frequencies because of the parasitic inductance. The inductance becomes dominant above 30 MHz.

3.2.2.2 EMI Filters

Filters are commonly used for the power lines, but they are also very effective in signal lines. Especially on clock and bus lines which are propagation paths for the noise in applications.

This figure shows the equivalent circuits of different types of EMI-filters together with their optimum application cases.

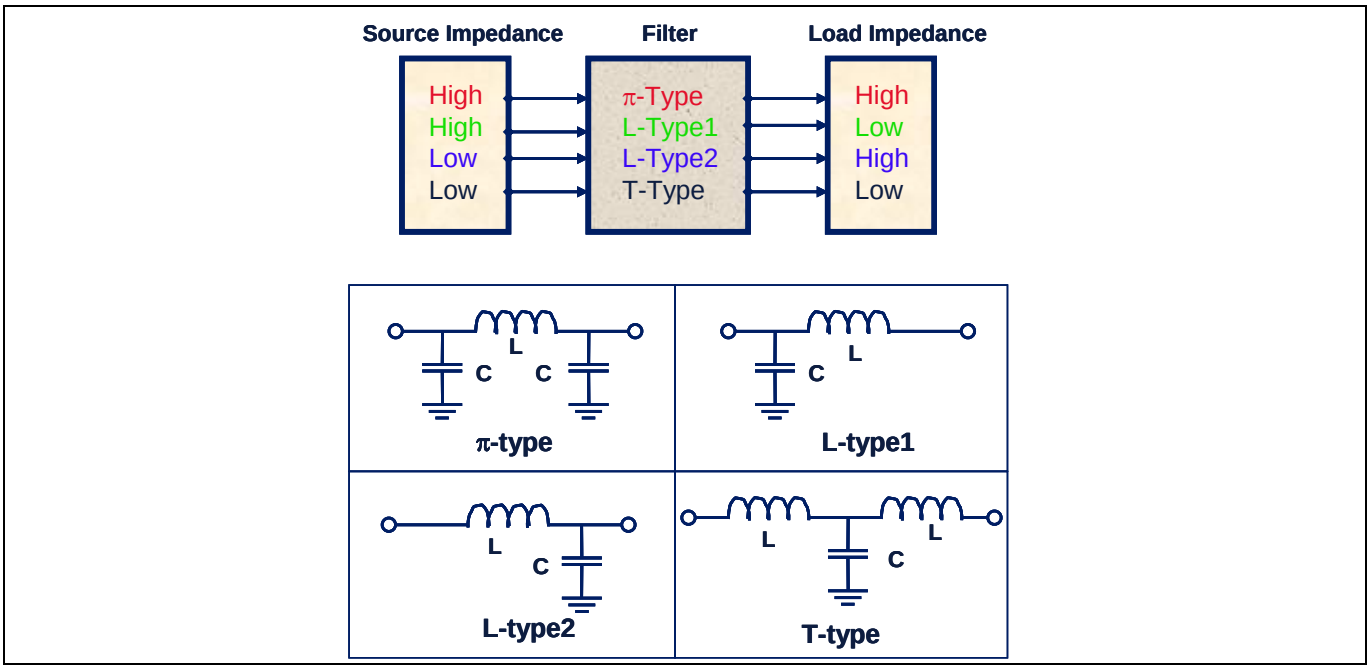


Figure 51 Different types of EMI-filters and usage conditions

The filters consist of L and C elements. Depending on the required insertion loss of the filter they are configured as π-, L- and T-filter.

If the source and load impedance is high, then a π -type filter is the best solution. The π -type filter has an inductor surrounded by two capacitors so that the capacitances are lowering the impedance on both sides according their selected frequency characteristics.

4 System-Level ESD

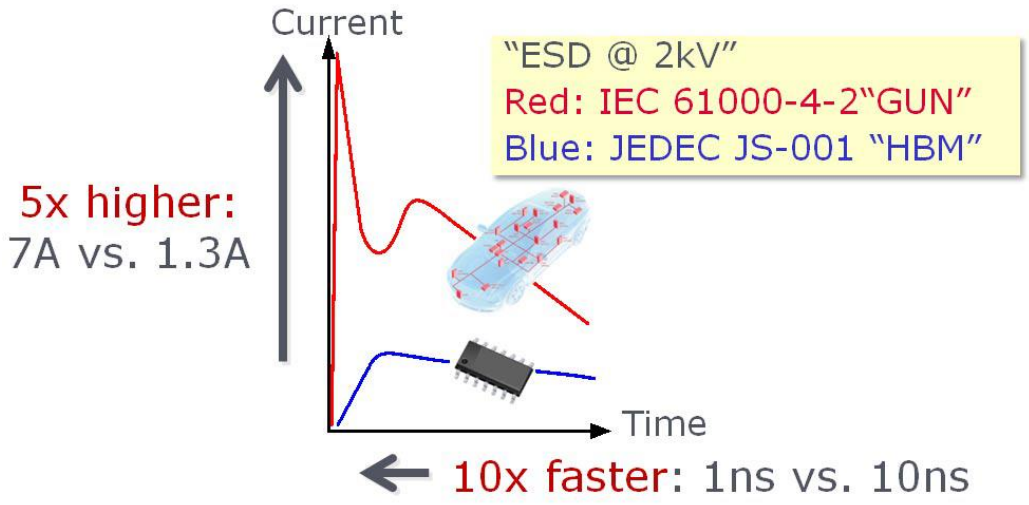
4.1 General

ESD tests divide the world into component level and system level:

- Component level tests should ensure that unpowered, single semiconductor devices survive handling during manufacturing, testing and assembly.
- System level tests are designed to prove that systems can withstand ESD in the real operational world.

Because of these very different requirements the two tests strongly vary in the discharge current waveform.

As you can see in the chart below, according to the variations of the current waveform the requirements of component and system-level ESD test are very different:

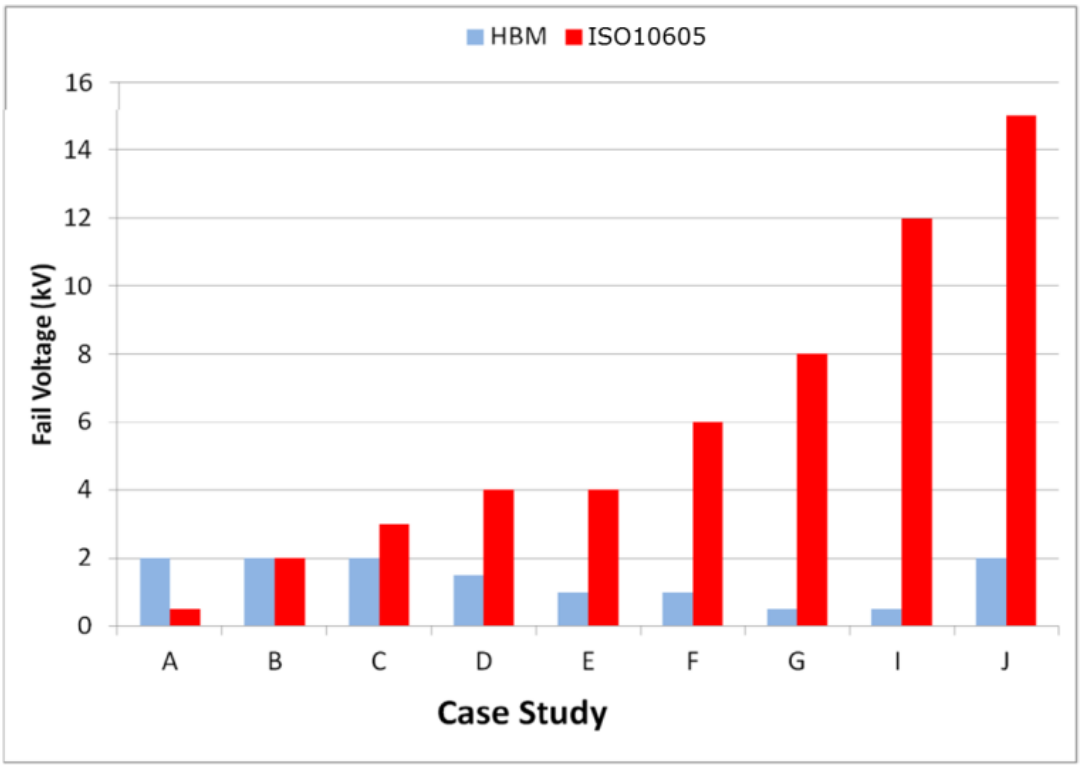


[JEDEC Publication 155 (JEP155), August 2008]

Figure 52 Difference between component-level (HBM) and system level (GUN) test standards

There is no correlation between component level ESD robustness, proved by the Human Body Model (HBM) test according to JEDEC JS-001, and system level ESD robustness, proved by ISO10605 or IEC 61000-4-2.

In **Figure 53** one can clearly see that there is no relation between component level and system level ESD robustness. This can be explained by differences in the test methods and purposes of the tests.



[Implementation of Effective ESD Robust Designs, ESD Association, 2012]

Figure 53 Comparison of IC level and system level ESD failure threshold of various systems (A-J) showing that HBM protection is not related to System level ESD robustness

4.2 On-Chip ESD protection

There are two basic concepts of On-chip ESD protection. One solution is the ‘breakdown’ behaviour of ESD protection structures, while a second is the so-called ‘snap-back’ behaviour. Both have their benefits and drawbacks and both are being used in the industry. ESD protection in general is a high-ohmic device up to the trigger-voltage. Above this voltage the device provides a low-ohmic path to GND and can carry a few amperes for a short period of time (typically 100-200ns).

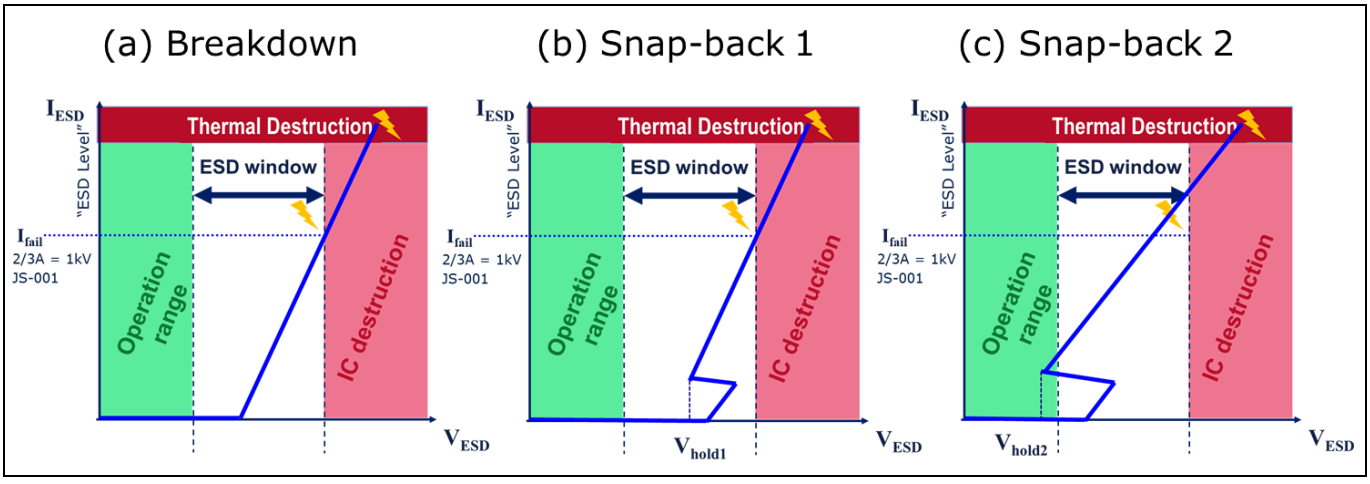


Figure 54 Breakdown (a) and Snap-back (b, c) ESD structure

The figure shows typical electrical characteristics of a breakdown (a) and two different snap-back structures:

(b) With its holding voltage beyond the operation range.

(c) With its holding voltage within the operation range.

To avoid accidental triggering of the ESD protection during normal operation it is necessary not to exceed the operation range with its upper limit AMR (Absolute Maximum Rating) in the application. If it is exceeded, the ESD device tries to shunt the current with a very low-ohmic path to ground, and it can be destroyed if the energy is too high.

Note: An ESD snap-back structure like that shown in (c) is dangerous because even after returning to an allowed voltage within the operation range the ESD structure remains on and will be destroyed, because it is not designed to withstand a DC current in snap-back mode.

4.3 System-Level ESD protection (On-Board)

External components are used to provide a system-level ESD protection on board-level:

- TVS diodes to clamp to a safe voltage
- Capacitors to take over current/charges of system-level ESD sources
- Resistors to limit current into chip

It is important to adapt the board-level protection concept to the electric characteristic of the on-chip ESD protection (co-design). This figure shows a bad and good example for co-design:

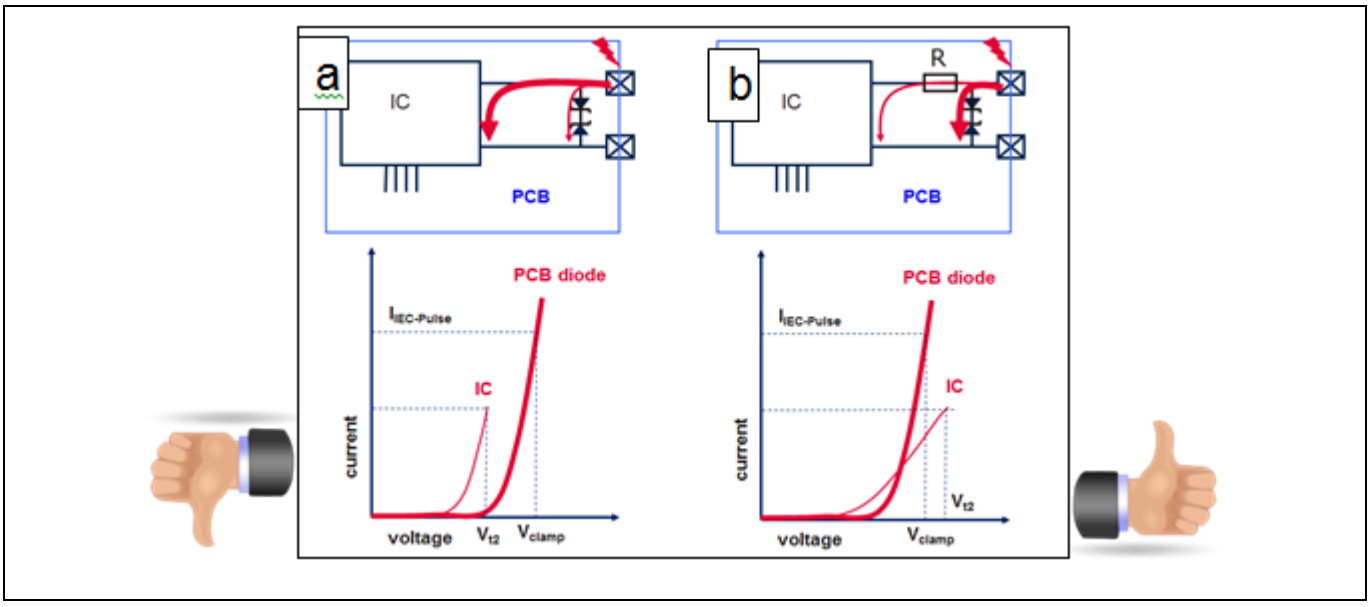


Figure 55 Bad (a) and good (b) example for on-chip/board-level ESD co-design

a) The turn-on and clamping voltage of the external TVS diode is higher than the corresponding internal on-chip voltages. Therefore the on-chip protection will take over nearly the whole ESD stress current (and will be destroyed if not designed for such high currents!).

b) The same on-chip and board-level protection elements as in case a) are used, but there is an additional resistor to limit the current into the chip, leading to a sufficient, high overall system level robustness.

It is not only the absolute amplitude of the current into the chip that is important. Consideration must also be given to the fact that the current pulse form will be re-shaped or modulated by the external components, and also by board intrinsic parasitic inductances/capacitances.

4.4 System-Level ESD Board Layout Design Guidelines

Generally, for chip in a typical board environment, two types of pins must be considered:

- External (or global) pins with direct connection to board entry points like connector or bus pins
- Inter-chip pins with only internal connections between neighbor chips

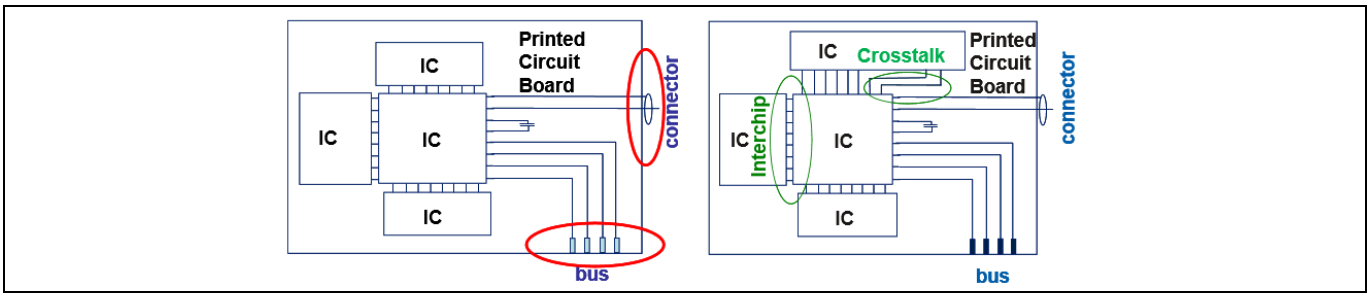


Figure 56 Externally (red) and internally (green) connected pins

It is obvious that external pins are of special interest for System-Level ESD protection. But also inter-chip pins can be distorted by cross-coupling with ESD stressed external pin trace lines.

A “golden” System-Level ESD rule is to shunt any ESD current by board-level ESD protection elements **as close as possible at the entry points** (connector or bus pins). The basic idea behind this is to shield sensitive devices by inhibiting the spread of the ESD distortion over the whole PCB’s:

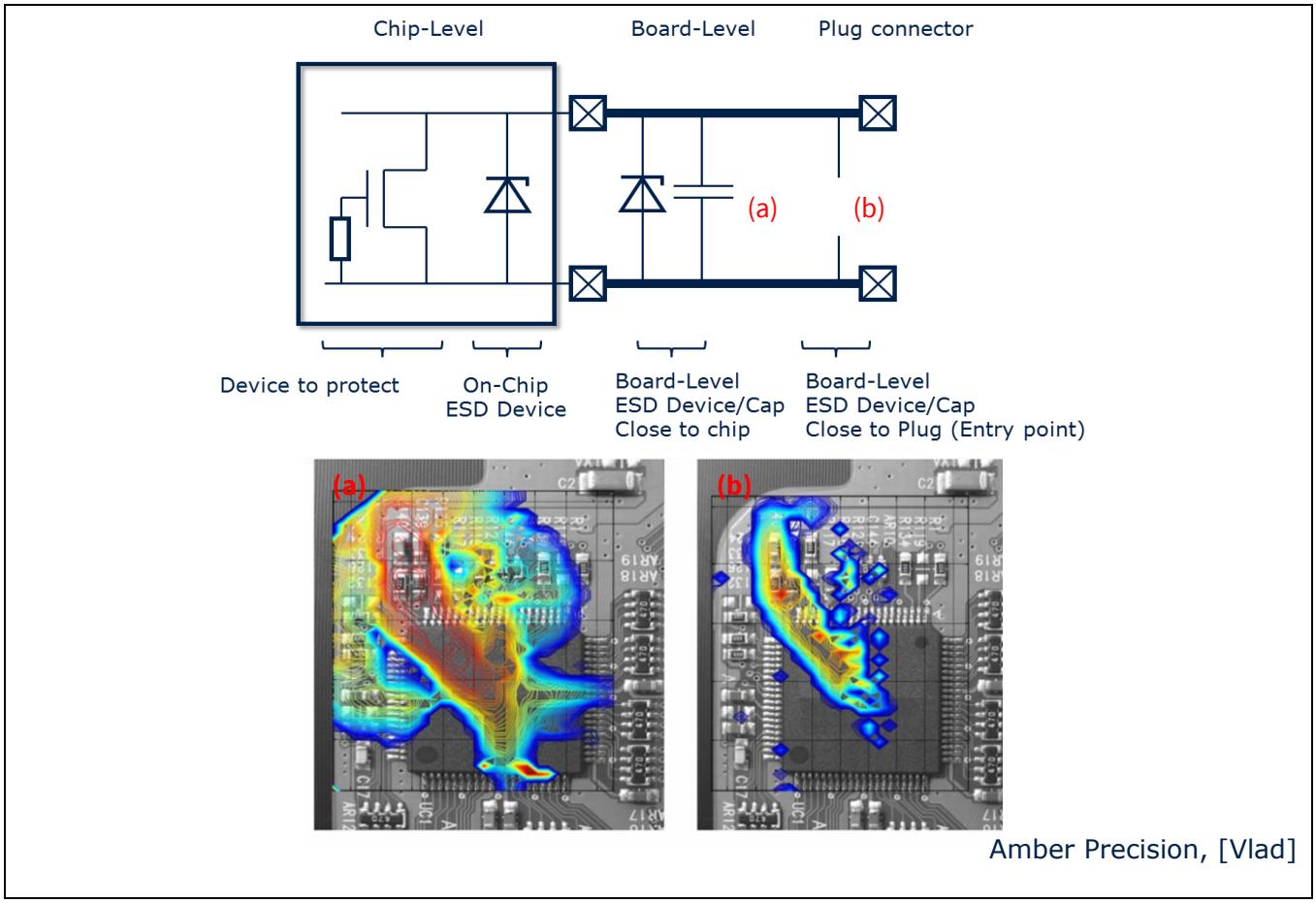


Figure 57 ESD distortion spread over PCB with ESD device close to chip (a) and close to entry point (b)

Attention: ***For ESD protection device placement, there is a trade-off between ESD (close to entry point recommended) and EMC (close to chip recommended). So it must be a clear decision at an early stage of PCB layout, which behavior should be optimized.***

4.5 Parasitic

Since a System-Level ESD pulse is a kind of high-frequency (GHz) signal (with high current amplitudes), high frequency behaviour of the board-level ESD protection elements as well as the PCB itself must be taken into account. For ESD protection elements it is mainly:

- the serial parasitic inductance of capacitors
- the voltage overshoot of TVS diodes

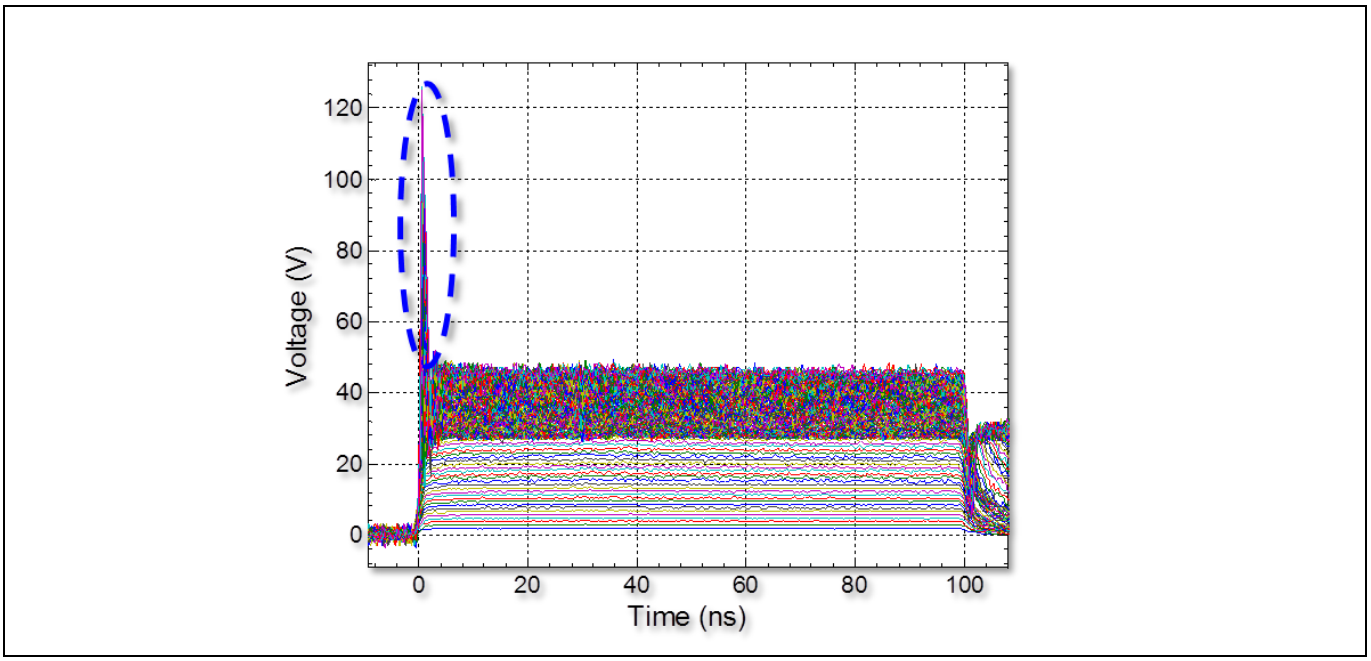


Figure 58 Transient voltages of a TVS diode with different current pulses with 1ns rise time 100ns length. During the first ns a voltage over shoot up to 120V (blue dashed line) occurs

On the board the proper layout of ground lines (without creating loops) low-impedant connection of board-level ESD protection elements must be ensured. For both the electrical behaviour and improvement measures are described in the sections on Layout Structures and Components.

It is obvious that a board-level ESD protection element with a serial inductance as low as possible must be used to avoid voltage overshoots. These overshoots are especially pronounced for the first current peak of an IEC-61000-4-2 pulse (**Figure 59**).

System-Level ESD

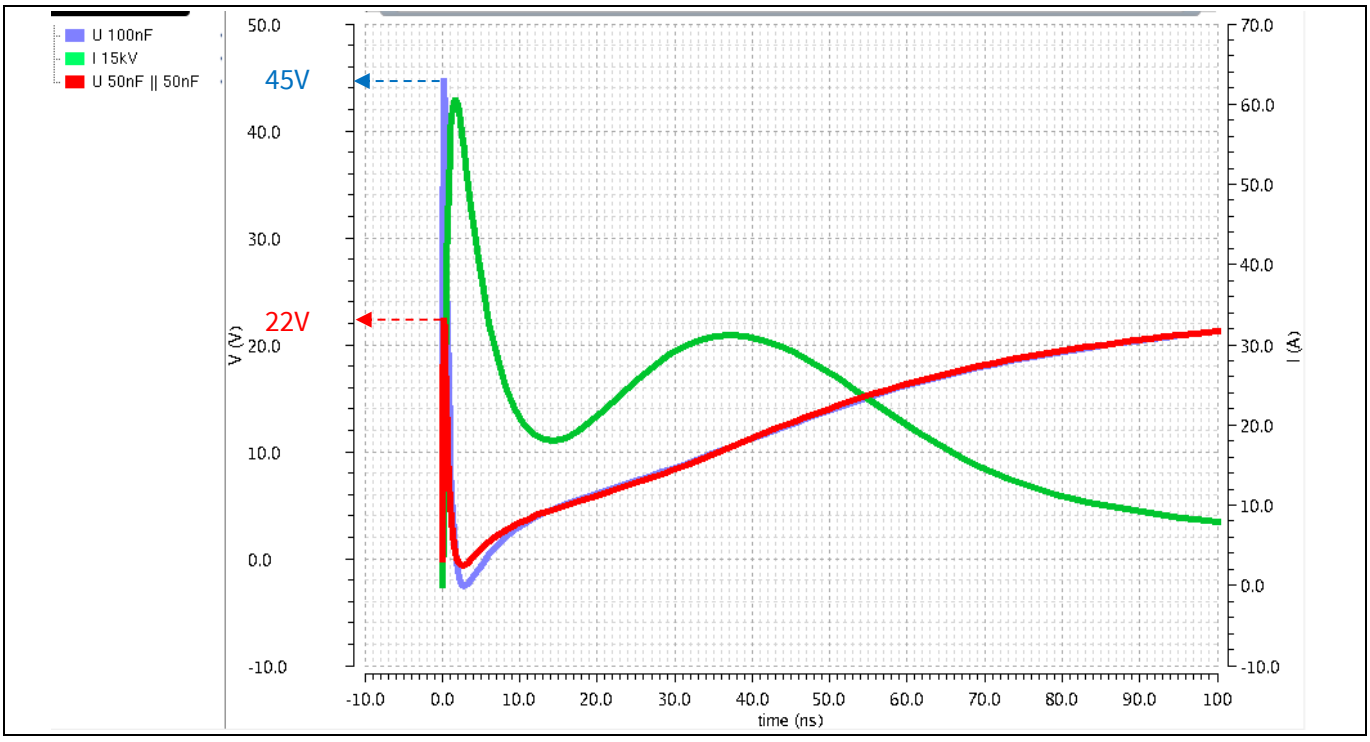


Figure 59 Voltage curves of a 15kV IEC-61000-4-2 current pulse (green) in one 100nF cap (blue) and in two 50nF caps (red) parallel. For each cap a serial inductance of 500pH was considered. The voltage overshoot during the first ns of the two caps is clearly reduced.

A way to improve this is to:

- select a capacitor in the smallest possible package (smaller inductance)
- divide the necessary capacitance in two capacitors in parallel
- avoid vias or to use as many as possible in parallel

By these measures the overall effective serial inductance, just as the voltage overshoot, will be reduced.

Board lines and vias add inductances and cause high voltage drops.

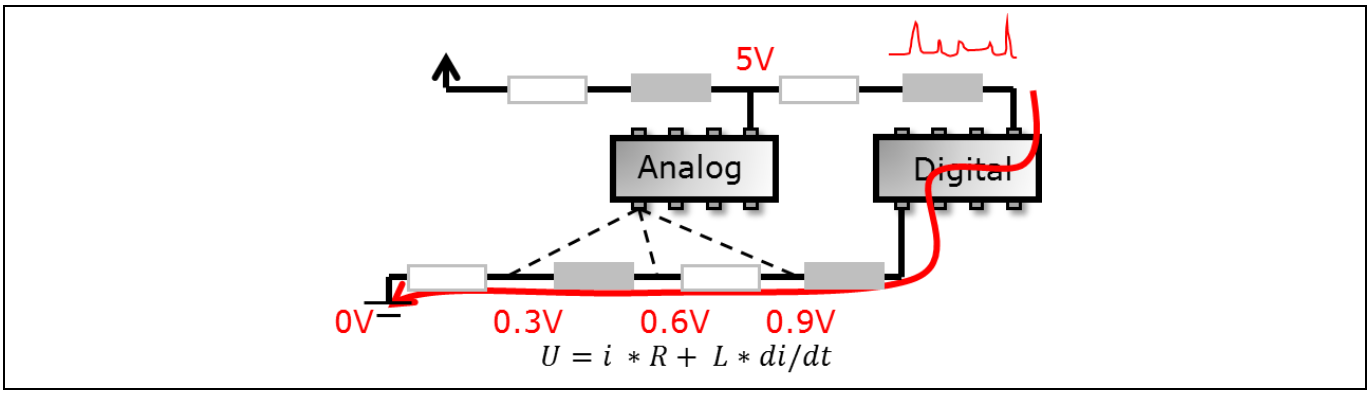


Figure 60 Voltage drop in ground path

- Assuming an inductance of 10nH/cm and a 10mA/ns pulse a voltage drop of 100mV/cm will occur. Depending on the ground connection point of the analog device, the supply vs. ground voltage in this example will differ between (5V-0.3V) = 4.7V and (5V-0.9V) = 4.1V. This may trigger a chip-reset event due to under-voltage detection functionality.

4.6 High-Ohmic Nodes

Since System-Level ESD qualification (for example IEC-61000-4-2) is performed with multi (3…10) subsequent stress pulses at the same pin combination, the charges can be stored and accumulate with every pulse.

The qualification standard recommends a discharging procedure after each pulse, but only for the pins-under_test (PUT). But internal high ohmic nodes (>> 100kΩ... MΩ) are able to cumulate charges of ESD events, means a voltage will remain till the next pulse. In other words, the following ESD pulse is applied to a system with internal pre-voltages. These pre-voltages can lead to the improper function of ESD protection devices (both board-level and component-level) or to a kind of power-up condition in a certain part of the circuit. Due to the high ohmic node the charges will stay even after the actual ESD pulse and extend the chip stress from initially some 100ns to up to 1s. This may lead to so called soft-fails, means there is no physical destruction (hard fails), but a malfunction caused by an undefined chip power state.

Under special consideration is the situation of a snap-back ESD protection in parallel to a capacitor, because as soon as the accumulated voltage is above the trigger voltage of the snap-back device, the capacitor will discharge through the snap-back device and may destroy (depends on capacitor size) this device.

5 Microcontroller special remarks

Dedicated input pins

These pins, when not used, should be tied to the level which represents the inactive level for the associated function. For example;

- NMI# (which has no internal pull-up) should be tied to V_{DD}.
- READY# (which has an internal pull-up) should be tied to V_{DD}.
- XTAL3# (input clock for auxiliary oscillator) should be tied to a defined level. Because there are various types of auxiliary oscillators, please specify this level according to the Application Note 24020 of Infineon Technologies.

Output, Supply, Input and I/O

For unused “Output, Supply, Input and I/O”pins the following points must be considered:

Table 1 Considerations for unused “Output, Supply, Input and I/O” pins

I/O Type:	Measure	Reason
Supply Pins (Modules)	See the User´s Manual.	-
I/O-Pins	• Should be configured as output and driven to static-low in the weakest driver mode in order to improve EMI behavior. • Configuration of the I/O as input with pull-up or pull-down is also possible. • Solder pad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).	• In case of an emergency stop, it is possible that the I/Os are switched to high state. This leads to damage of the I/O if it is connected to GND (electro migration stress current). • If output is active and the level is defined, no unexpected switching of the input path is possible.
Output Pins including LVDS	• Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solder pad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).	• Defined potential of the output stage reduces leakage current and improves immunity. *Note: In some cases multiplexer output has alternate function.*
Input Pins without internal pull device	• For pins with alternate function, see the product target specification to define the necessary logic level. • Should be connected with a resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is expected if a direct connection to GND is made. • Groups of 8 pins can be used to	• This avoids the initial current consumption peaks after reset of the device by defined level at inputs. These current peaks can be caused by uncontrolled switching of the Schmitt-trigger of the input due to leakage currents.

	reduce number of external pull-up/down devices (keep in mind leakage current).	
Input Pins with internal pull device	• For pins with alternate function please see the product specification to define the necessary logic level. • Should be configured as pull-down (Exception: if the User's Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solder pad should not be connected to any other net (isolated PCB-pad only for soldering)	• This avoids the initial current consumption peaks after reset of the device by defined level at inputs. These current peaks can be caused by uncontrolled switching of the Schmitt-trigger of the input due to leakage currents.

6 Simulations

An additional way to improve the design of an application is to test certain structures in the layout by simulation. Here we describe the most common tools and techniques which are offered by several software manufacturers. Through simulation of EMC-relevant parameters like emission, susceptibility and signal integrity of electrical systems, an assessment of the necessary effort and the most effective measures can be made. Electrical systems can be: modules, printed circuit boards (PCB), electrical circuits, sub-circuits and even integrated devices. More and better simulation models are provided from the different manufacturers or distributors.

In the last few years, there have been some efforts to get accurate models for the power supply network of the microcontrollers. These models are called Chip Power Models (CPM). The model describes the high frequency behavior of power supply networks of integrated circuits with an impedance part (RLC) and a current source part (PWL current sources). The models can today be used with most of the EMC simulators.

IBIS models are available for the 16-bit and 32-bit microcontrollers from Infineon Technologies.

SPICE

SPICE is a simulation program with integrated circuit emphasis. SPICE allows the analysis of electrical circuits. For EMI/SI items it allows the analysis of electrical systems (e.g. bus systems) regarding parasitic effects (coupling to adjacent nets, reflections, etc.). The parasitics themselves are calculated by using a 2D- or 3D-field solver. The driver and receiver models are supplied by the manufacturers as transistor based models or in the IBIS format. There exist plenty of SPICE-like programs.

Generation of SPICE models

To achieve good results from SPICE simulations, modelling know-how is a basic requirement. The better the SPICE models (sub-circuits) are, the more efficient the analysis becomes. For the analysis of for example a bus system, IBIS models (mostly provided by the chip manufacturer) and transmission line models (generation by 2D- and 3D- field solvers) are necessary.

2D-field-solver

A 2D-field solver is needed for the determination of the parasitics (capacitance, inductance and resistance values) for transmission lines or transmission line systems which are geometrically uniform in the 3rd dimension; i.e. traces or trace structures. These values can be used to model SPICE sub-circuits for the analysis of bus systems or other structures.

3D-field solver

For more complex structures like vias and rectangular traces, or structures in integrated circuits like packages, wirebonds and leadframe for example, a 3D-field solver is needed to determine the parasitics. Again, these values can be used to model SPICE sub-circuits.

The electric or magnetic field in any given point in the space around a conducting 3D-structure (especially a PCB) is calculated by adding the corresponding field vectors caused by all current-vectors of this structure for a given moment in time and a given frequency.

Pre-layout analysis

Pre-layout analysis means the investigation of certain design configurations (even in the specification phase) in order to find an optimum solution early. Pre-layout analysis also means the setup of a bundle of design rules for subsequent design stages (for example, minimum distance of traces to keep crosstalk low).

Simulations

Post-layout analysis

Post-layout analysis means the partial or full investigation of already designed electrical systems such as PCBs, in order to detect design hazards, such as areas of high electromagnetic emission, before any hardware prototype is built.

7 Formula appendix

Decibel calculation

Decibel [dB] is a dimensionless ratio of levels. Electromagnetic emission measurement results are expressed in spectra or limit curves with the unit [dBµV].

Power [dB] = 10 log(P1/P0), P[dBmW or dBm] = 10 log(P1/1mW);

dBm is defined for a 50Ohm system with P1 being the measured power and P0 being the reference power.

Voltage [dB] = 20 log (V1/V0), V[dBµV] = 20 log(V1/1µV);

With V1 being the measured voltage, V0 being the reference voltage.

(e.g. harmonic of 100µV amplitude = 20 log(100) = 40 dBµV)

8 Glossary

Table 2

Term	Definition
2D-field solver	Simulation tool for analysis (couplings, characteristic wave impedance, etc.) of two-dimensional trace structures.
3D-field solver	Simulation tool for analysis (couplings, characteristic wave impedance, etc.) of three-dimensional trace structures like via holes.
Cross (bar) current	Current which flows across two or more transistors connected in line, in case they are conducting at the same time.
Decap	De-coupling capacitor.
DUT	Device Under Test.
EMC	ElectroMagnetic Compatibility. Compatibility regarding emission and susceptibility of electromagnetic disturbances between →DUT and environment.
EME	ElectroMagnetic Emission. Radiated or conducted emission of electromagnetic noise by an electronic device.
EMI	Electromagnetic interference (undesired or illegal generation of electromagnetic signals; bandwidth DC to daylight.
EMS	ElectroMagnetic Susceptibility. An adverse reaction of electronic equipment to radiated or conducted signals.
ESL	Equivalent Series Inductance of capacitors at high frequency.
ESR	Equivalent Series Resistor of capacitors at high frequency.
GND	Board Ground net (trace or plane structure).
IBIS	Input/output Buffer Information Specification. A widely established standard for electrical behavioral specifications of digital integrated circuit input/output analog characteristics.
CPM	Chip Power Model.
Microvia	Via with a diameter of about 100µm.
PCB	Printed Circuit Board.
RF	Radio Frequency (high frequency).
SPICE	Name of a common simulation tool.
SI	Signal Integrity (reflection, timing, crosstalk).
VI - Table	Static behavioral driver description voltage versus current.
Vih	Input threshold voltage.
VCC	Board supply net (trace or plane structure).
VDD	IC supply pin.
VSS	IC ground pin.
XTK	Crosstalk (interference between two adjacent traces).
x-y-tracing	Orthogonally routed adjacent signal layers to minimize crosstalk.

Glossary

Term	Definition
Z0	Characteristic wave impedance.

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