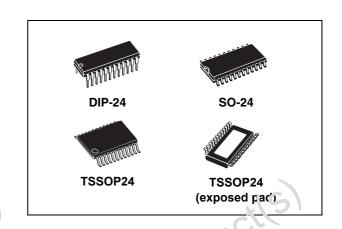




16-Bit, constant current LED sink driver

Features

- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Serial out change state on the falling edges of clock
- Output current: 15-120 ma
- 25MHz clock frequency
- Available in high thermal TSSOP exposed pad
- Efficiency package



Description

The STP16C596 is a monolithic, medium-voltage, low current power 16-bit shift register designed for LED panel displays. The STP16C596 contains a 16-bit serial-IN, parallel-OUT shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources are designed to provide 15-120mA constant current to drive the LEDs.

The serial output change state on the 'a'ling edges of clock, this special feature vil' provide an improved performance of the application when the clock signal is skewed because the daisy chain is too long.

Through an external resistor, users may adjust the STP16C59C partput current, controlling in this way the light intensity of LEDs.

The STP16C596 guarantees a 16V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 25MHz, also satisfies the system demand for high volume data transmission. Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a 2.5 factor.

Order codes

Part Number	Part Number Package	
STP16C596B1R	DIP-24	15 parts per tube
STP16C596M	SO-24 (Tube)	40 parts per tube
STP16C596MTR	SO-24 (Tape & Reel)	1000 parts per reel
STP16C596TTR	TSSOP24 (Tape & Reel)	2500 parts per reel
STP16C596XTTR	TSSOP24 Exposed-Pad (Tape & Reel)	2500 parts per reel

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STP16C596 Summary description

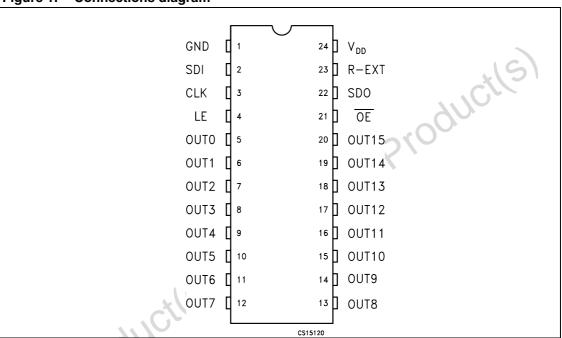
1 Summary description

Table 1. Current accuracy

Output voltage	Current a	Output current	
Output voltage	Between bits	Between ICs	Output current
≥ 0.7V	Typ. ± 3%	± 10%	15 to 120mA

1.1 Pin connection and description

Figure 1. Connections diagram



Note: The Exposed-Pad is electrically not connected

Table 2. Pin description

PIN N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	ŌĒ	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	V _{DD}	Supply voltage terminal

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Summary description STP16C596

1.2 Equivalent circuit of inputs and outputs

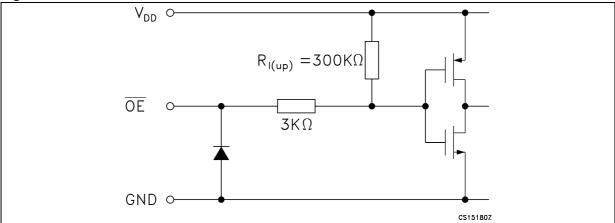


Figure 3. LE terminal

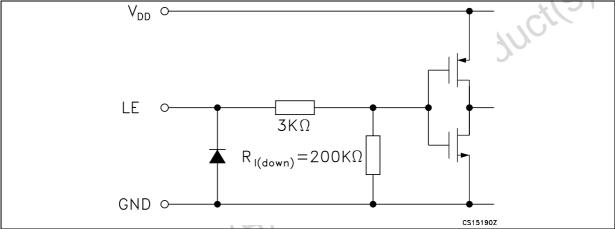
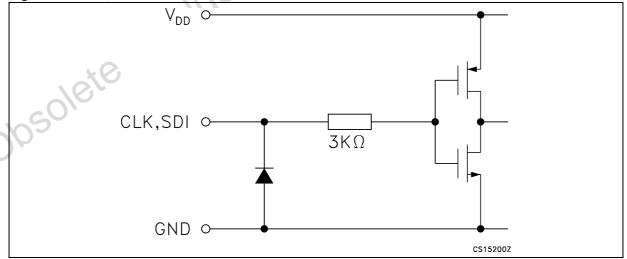
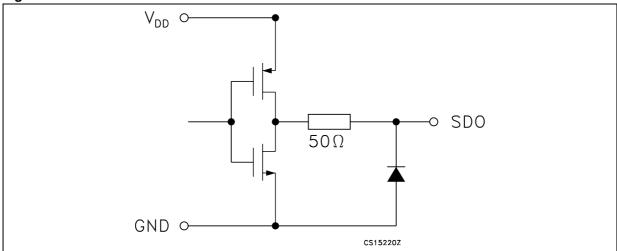


Figure 4. CLK, SDI terminal



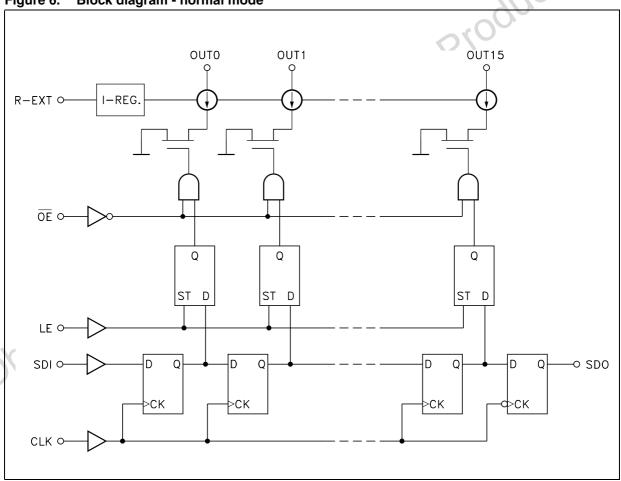
STP16C596 Summary description

Figure 5. SDO terminal



1.3 Block diagram

Figure 6. Block diagram - normal mode



Summary description STP16C596

1.4 Truth table

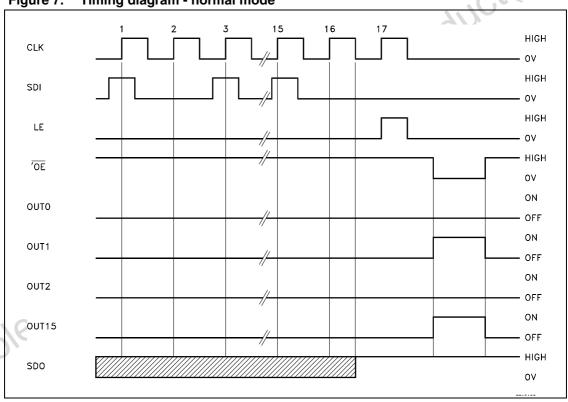
Table 3. Truth table

Clock	LE	ŌĒ	SERIAL-IN	OUT0 OUT7 OUT15	SDO
	Н	L	Dn	Dn Dn -7 Dn -15	Dn -15
	L	L	Dn + 1	No Change	Dn -14
	Н	L	Dn + 2	Dn -2 Dn -5 Dn -13	Dn -13
	Х	L	Dn + 3	Dn -2 Dn -5 Dn -13	Dn -13
7_	Х	L	Dn + 3	ON	Dn -13

Note: OUT0 to OUT15 = ON when Dn = H; OUT0 to OUT15 = OFF when Dn = L.

1.5 Timing diagrams

Figure 7. Timing diagram - normal mode



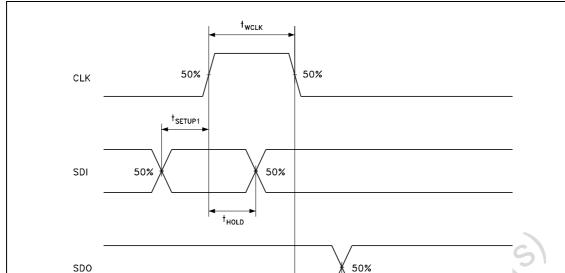
Note: Note: The latches circuit holds data when the LE terminal is Low.

When the LE terminal is at High level, latch circuit doesn't hold the data it passes from the input to the output.

When the \overline{OE} terminal is at Low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.

When the OE terminal is at High level, it switches off all the data on the output terminal.

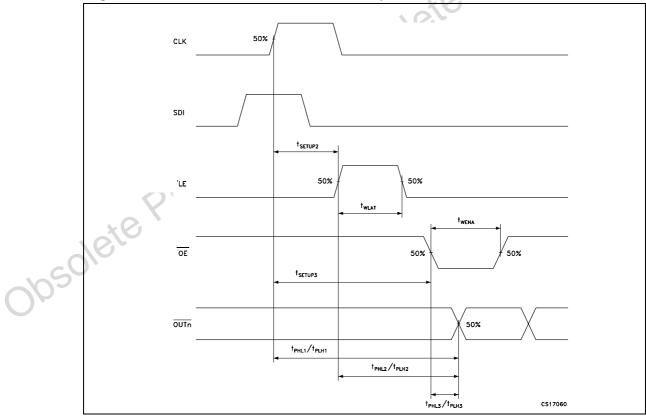
STP16C596 Summary description



t_{PLH} /t_{PHL}

Figure 8. Clock, Serial-In, Serial-Out



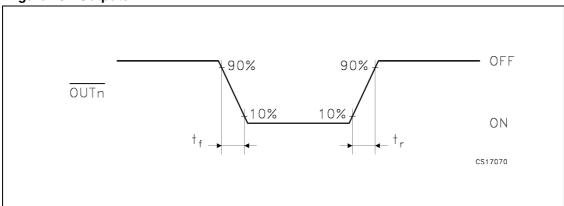


5//

CS17050

Summary description STP16C596

Figure 10. Outputs



Obsolete Product(s). Obsolete Product(s)

STP16C596 Maximum rating

Maximum rating 2

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
Vo	Output voltage	-0.5 to 16	V
Io	Output current	120	mA
VI	Input voltage	-0.4 to V _{DD} +0.4	V
I _{GND}	GND terminal current	1920	mA
f _{CLK}	Clock frequency	25	MHz
T _{OPR}	Operating temperature range	-40 to +125	°C
T _{STG}	Storage temperature range	-65 to +150	°C
Therm	al data Thermal data		

2.1 Thermal data

Table 5. Thermal data

Symbol	Parameter	DIP-24	SO-24	TSSOP-24	TSSOP-24 ⁽¹⁾ (exposed pad)	Unit
R_{thJA}	Thermal resistance junction-ambient	60	75	85	37.5	°C/W

^{1.} The Exposed-Pad should be soldered to the PBC to realize the thermal benefits opsolete P

Maximum rating STP16C596

2.2 Recommended operating conditions

Table 6. Recommended operating conditions

					, ,	
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{DD}	Supply voltage		4.5	5.0	5.5	V
V _O	Output voltage				16.0	V
I _O	Output current	OUTn	5		120	mA
I _{OH}	Output current	SERIAL-OUT			+1	mA
I _{OL}	Output current	SERIAL-OUT			-1	mA
V _{IH}	Input voltage		0.7V _{DD}		V _{DD} +0.3	V
V _{IL}	Input voltage		-0.3		0.3V _{DD}	V
t _{wLAT}	LE pulse width		20			ns
t _{wCLK}	CLK pulse width		20		.10	ns
t _{wEN}	OE pulse width	V _{DD} = 4.5 to 5.5V	400		Cil	ns
t _{SETUP(D)}	Setup time for DATA	V _{DD} = 4.3 to 3.3 v	20	-9/).	ns
t _{HOLD(D)}	Hold time for DATA		15	0		ns
t _{SETUP(L)}	Setup time for LATCH	A. C	15			ns
f _{CLK}	Clock frequency	Cascade operation ⁽¹⁾			25	MHz

If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please considered the timings carefully.

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STP16C596 Electrical characteristics

3 Electrical characteristics

Table 7. Electrical characteristics ($V_{DD} = 5V$, T = 25°C, unless otherwise specified.)

1	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{IH}	Input voltage high level		0.7V _{DD}		V_{DD}	٧
V _{IL}	Input voltage low level		GND		0.3V _{DD}	V
I _{OH}	Output leakage current	V _{OH} = 16V			10	μΑ
V _{OL}	Output voltage (Serial-OUT)	I _{OL} = 1mA			0.4	V
V _{OH}	Output voltage (Serial-OUT)	I _{OH} = -1mA	V _{DD} - 0.4V			٧
I _{OL1}	Outrot surrent	$V_{O} = 0.7V R_{EXT} = 910\Omega$	18.6	20.4	22.4	mA
I _{OL2}	Output current	$V_{O} = 0.7V R_{EXT} = 360\Omega$	45.7	50.2	55.2	mA
ΔI_{OL1}	Output current error	$V_{O} = 0.7V R_{EXT} = 910\Omega$		± 3	± 4	%
Δl _{OL2}	between bit (All Output ON)	$V_{O} = 0.7V R_{EXT} = 360\Omega$		± 3	± 4	%
R _{SIN(up)}	Pull-up resistor		150	300	600	ΚΩ
R _{SIN(down)}	Pull-down resistor		100	200	400	ΚΩ
I _{DD(OFF1)}		R _{EXT} = OPEN OUT 0 to 15 = OFF		0.3	0.6	
I _{DD(OFF2)}	Supply current (OFF)	$R_{EXT} = 470\Omega$ OUT 0 to 15 = OFF		5.5	7.7	
I _{DD(OFF3)}		$R_{EXT} = 250\Omega$ OUT 0 to 15 = OFF		10.1	14.1	mA
I _{DD(ON1)}	(3)	$R_{EXT} = 470\Omega$ OUT 0 to 15 = ON		5.5	7.7	
I _{DD(ON2)}	- Supply current (ON)	$R_{EXT} = 250\Omega$ OUT 0 to 15 = ON		10.1	14.1	

Switching characteristics STP16C596

4 Switching characteristics

Table 8. Switching characteristics ($V_{DD} = 5V$, T = 25°C, unless otherwise specified.)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{PLH1}	Propagation delay time, CLK-OUTn, LE = H, OE = L			200	280	ns
t _{PLH2}	Propagation delay time, LE-OUTn, OE = L			160	250	ns
t _{PLH3}	Propagation delay time, OE-OUTn, LE = H			145	200	ns
t _{PLH}	Propagation delay time, CLK-SDO	$V_{DD} = 5V$ $V_{IH} = V_{DD}$	1	15	30	ns
t _{PHL1}	Propagation delay time, CLK- \overline{OUTn} , LE = H, \overline{OE} = L	$V_{IL} = GND$ $C_L = 13pF$ $I_O = 40mA$ $V_L = 3 V$		15	30	ns
t _{PHL2}	Propagation delay time, LE-OUTn, OE = L	$R_{EXT} = 470\Omega$ $R_{L} = 65\Omega$ CLK = 1MHz		15	30	ns
t _{PHL3}	Propagation delay time, OE-OUTn, LE = H			45	60	ns
t _{PHL}	Propagation delay time, CLK-SDO			15	30	ns
t _r	Output rise time	, etc		160	200	ns
t _f	Output fall time			15	25	ns

Note: 1 To prevent current overshoot, during the Outputs switching, the overhead output voltage must be less than 1V

2 The Maximum suggested swithing frequency is up to 10KHz

STP16C596 Test circuit

5 Test circuit

Figure 11. DC characteristics

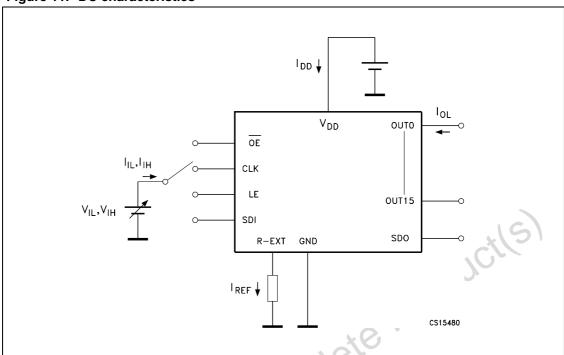
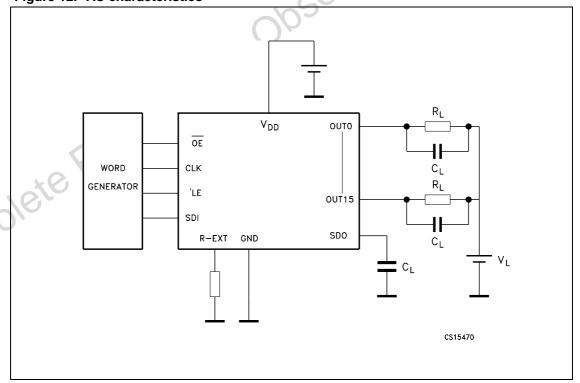


Figure 12. AC characteristics

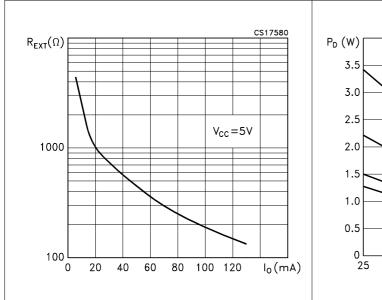


Typical characteristics STP16C596

6 Typical characteristics

Figure 13. Output current-R_{EXT} resistor

Figure 14. Power dissipation vs. temperature package



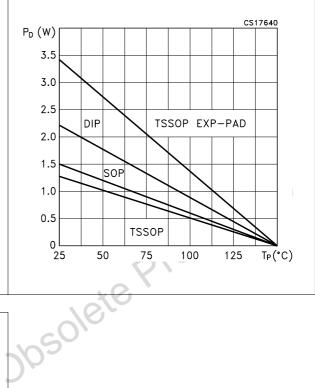
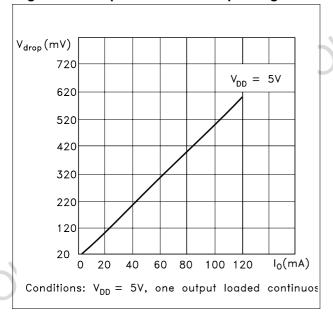
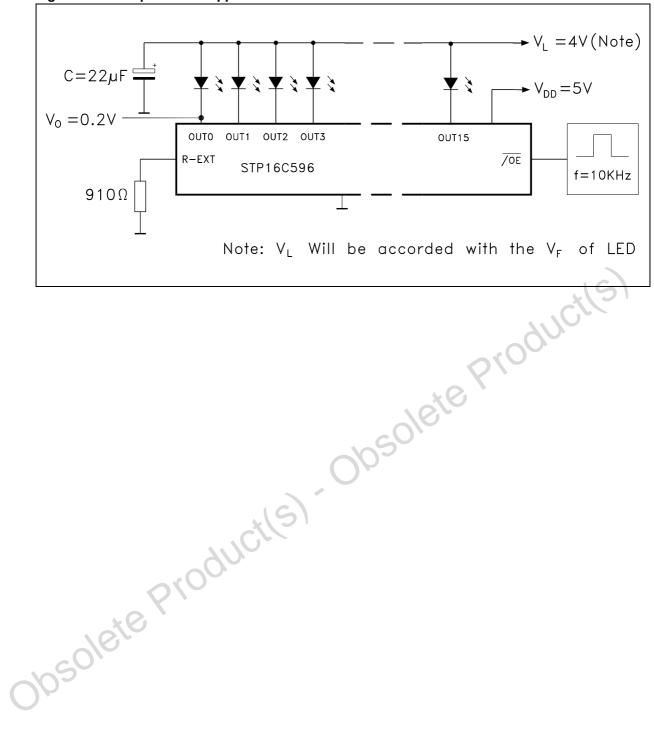


Figure 15. Output current vs. drop voltage



STP16C596 Typical characteristics

Figure 16. Blue powerLED application circuit



Package mechanical data STP16C596

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.



Table 9. Plastic DIP-24 (0.25) Mechanical data

Def		mm			inch		
Ref	Min	Тур	Max	Min	Тур	Max	
Α			4.32			0.170	
A1	0.38			0.015			
A2		3.3			0.130		
В	0.41	0.46	0.51	0.016	0.018	0.020	
B1	1.40	1.52	1.65	0.055	0.060	0.065	
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	31.62	31.75	31.88	1.245	1.250	1.255	
Е	7.62		8.26	0.300		0.325	
E1	6.35	6.60	6.86	0.250	0.260	0.270	
е		2.54			0.100		
E1		7.62			0.300	16/2	
L	3.18		3.43	0.125		0.135	
М	0°		15°	0°	00,0	15°	

Figure 17. Plastic DIP-24 (0.25) Package dimensions

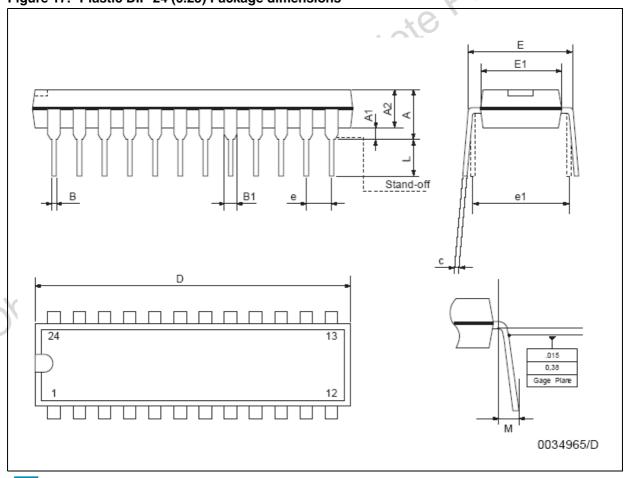


Table 10. TSSOP24 Mechanical data

D-4		mm			inch			
Ref	Min	Тур	Max	Min	Тур	Max		
Α			1.1			0.043		
A1	0.05		0.15	0.002		0.006		
A2		0.9			0.035			
b	0.19		0.30	0.0075		0.0118		
С	0.09		0.20	0.0035		0.0079		
D	7.7		7.9	0.303		0.311		
Е	4.3		4.5	0.169		0.177		
е		0.65 BSC			0.0256 BSC			
Н	6.25		6.5	0.246		0.256		
K	0°		8°	0°		8°		
L	0.50		0.70	0.020		0.028		

Figure 18. TSSOP24 Package dimensions

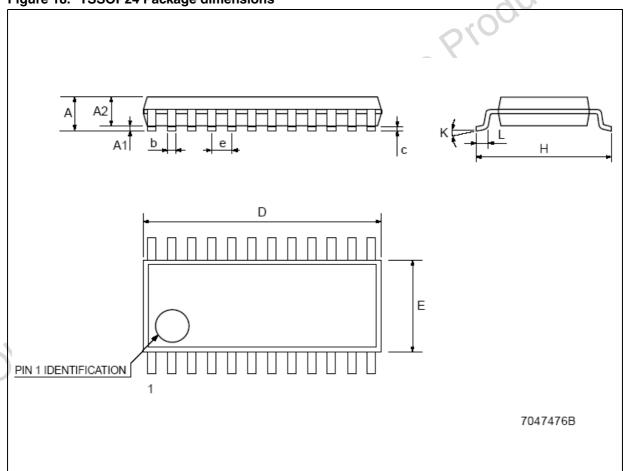


Table 11. Tape & Reel TSSOP24

D-4		mm			inch	
Ref	Min	Тур	Max	Min	Тур	Max
Α			330			12.992
С	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
Т			22.4			0.882
Ao	6.8		7	0.268		0.276
Во	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Ро	3.9		4.1	0.153		0.161
Р	11.9		12.1	0.468		0.476

Figure 19. Reel dimensions

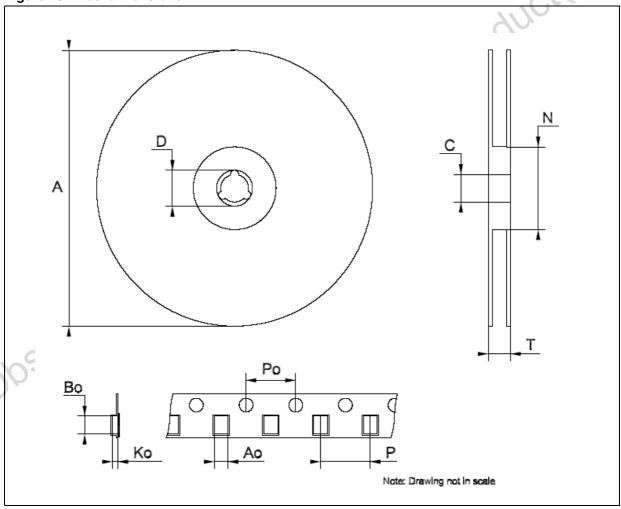


Table 12. SO-24 Mechanical data

Ref		mm			inch	
nei	Min	Тур	Max	Min	Тур	Max
Α			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
С		0.5			0.020	
c1			45°(typ.)		
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
е		1.27			0.050	
e3		13.97			0.550	4(2)
F	7.40		7.60	0.291	11)	0.300
L	0.50		1.27	0.020	100,0	0.050
S			°(ma	ax.) 8	010	

Figure 20. SO-24 Package dimensions

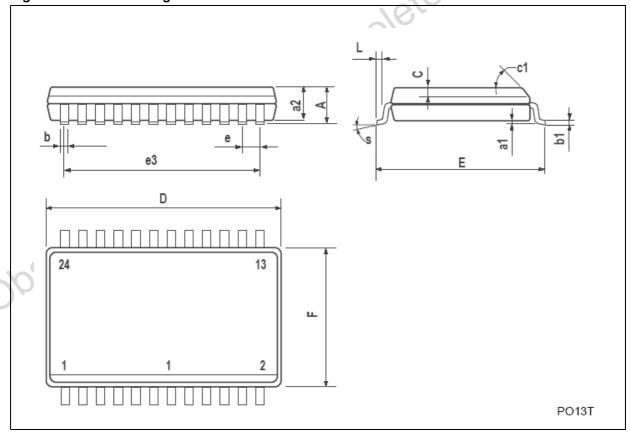


Table 13. Tape & Reel SO-24

Def		mm			inch		
Ref	Min	Тур	Max	Min	Тур	Max	
Α			330			12.992	
С	12.8		13.2	0.504		0.519	
D	20.2			0.795			
N	60			2.362			
Т			30.4			1.197	
Ao	10.8		11.0	0.425		0.433	
Во	15.7		15.9	0.618		0.626	
Ko	2.9		3.1	0.114		0.122	
Po	3.9		4.1	0.153		0.161	
Р	11.9		12.1	0.468		0.476	

Figure 21. Reel dimensions

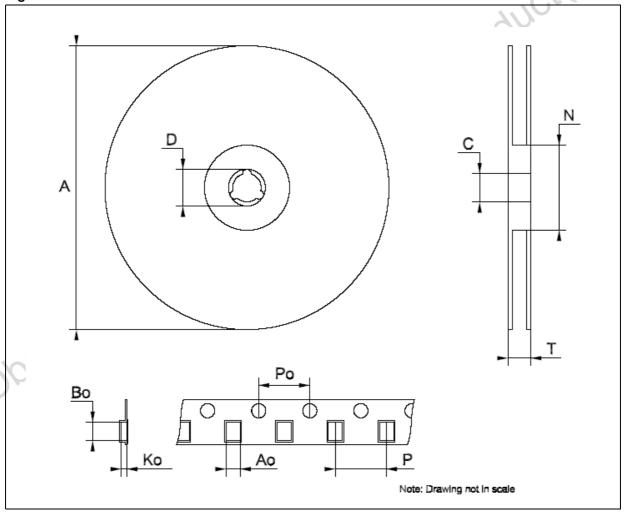
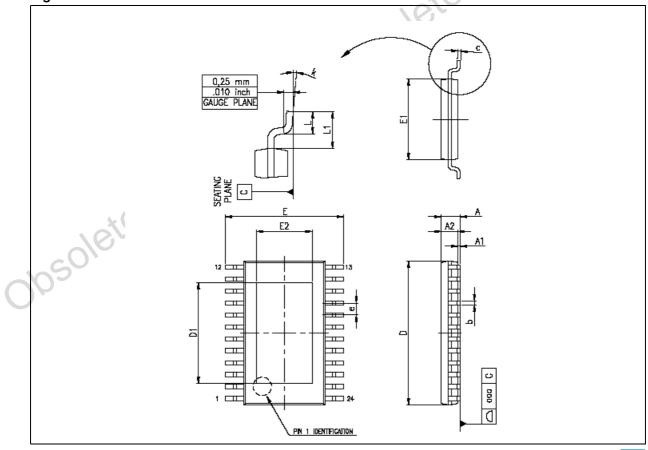


Table 14. TSSOP24 Exposed-pad

		mm			inch	
Ref	Min	Тур	Max	Min	Тур	Max
Α			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
С	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1		2.7		0.106		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2		1.5		0.059		4(2)
е		0.65			0.0256	000
K	0°		8°	0°	100,	8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 22. TSSOP24 Dimensions



STP16C596 Revision history

8 Revision history

Table 15. Revision history

Date 06-May-2004	1	
	Revision	Change
00 4 0004	4	Table 6 and Table 7 parameters changed.
03-Aug-2004	5	Figure 14 - pag. 10 is changed.
31-Mar-2005	6	Mistake on Fig. 7.
02-May-2005	7	Typing Error on the description features.
22-Jul-2005	8	Add note on Fig. 1 and Table 5.
16-May-2006	9	New template
26-Jul-2006	10	Block diagram Figure 6 on page 5 and Section 1.2: Equivalent circuit of inputs and outputs on page 4
		Block diagram Figure 6 on page 5 and Section 1.2: Equivalent circuit of inputs and outputs on page 4

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