

FEATURES

Low offset voltage: 13 μV maximum
Input offset drift: 0.03 $\mu\text{V}/^\circ\text{C}$
Single-supply operation: 2.7 V to 5.5 V
High gain, CMRR, and PSRR
Low input bias current: 25 pA
Low supply current: 180 μA

APPLICATIONS

Mobile communications
Portable instrumentation
Battery-powered devices
Sensor interfaces
Temperature measurement
Electronic scales

GENERAL DESCRIPTION

The AD8538 is a very high precision amplifier featuring extremely low offset voltage, low input bias current, and low power consumption. The supply current is less than 180 μA at 5.0 V. Operation is fully specified from 2.7 V to 5.0 V single supply (± 1.35 V to ± 2.5 V dual supply).

The AD8538 operates using very low power making this amplifier ideal for battery-powered devices and portable equipment.

The AD8538 is specified over the extended industrial temperature range (-40°C to $+125^\circ\text{C}$). The AD8538 amplifier is available in 5-lead TSOT-23, and 8-lead, narrow body SOIC packages.

PIN CONFIGURATION DIAGRAMS

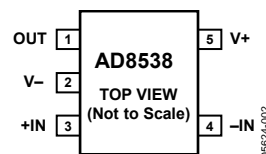


Figure 1. 5-Lead TSOT-23 (UJ-5)

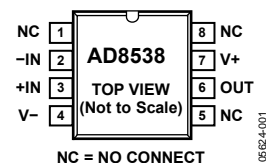


Figure 2. 8-Lead SOIC_N (R-8)

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	5
Applications.....	1	Thermal Resistance	5
Pin Configuration Diagrams.....	1	ESD Caution.....	5
General Description	1	Typical Performance Characteristics	6
Revision History	2	Outline Dimensions	12
Specifications.....	3	Ordering Guide	12
Electrical Specifications.....	3		

REVISION HISTORY

10/05—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

@ $V_S = 5.0\text{ V}$, $V_{CM} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	13	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		15	30	μV
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		35	25	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	100	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	50	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			150	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$; $V_{CM} = 0.2\text{ V to } 4.8\text{ V}$	115	150		dB
			100	135		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.1\text{ V to } 4.9\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	115	141		dB
			110	135		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.03	0.1	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.99	4.998		V
			4.98			V
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.95	4.970		V
			4.94			V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to V_+ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.9	5	mV
				2.8	7	mV
		$R_L = 10\text{ k}\Omega$ to V_+ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		17	20	mV
				20	30	mV
Short-Circuit Limit	I_{SC}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 25		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105	125		dB
			100	125		dB
Supply Current/Amplifier	I_{SY}	$I_O = 0$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		150	180	μA
				190	215	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.4		V/ μs
Settling Time 0.01%	t_s	$G = \pm 1$, 2 V step, $C_L = 20\text{ pF}$, $R_L = 1\text{ k}\Omega$		10		μs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			600		kHz
Phase Margin	ϕ_O	$R_L = 10\text{ k}\Omega$, $R_L = 100\text{ k}\Omega$, $C_L = 20\text{ pF}$		65		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.0		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		50		nV/ $\sqrt{\text{Hz}}$

AD8538

@ $V_S = 2.7\text{ V}$, $V_{CM} = 1.35\text{ V}$, $V_O = 1.35\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V _{OS}	−40°C ≤ T _A ≤ +125°C		5	13	μV
Input Bias Current	I _B	−40°C ≤ T _A ≤ +125°C			30	μV
		−40°C ≤ T _A ≤ +85°C		15	25	pA
		−40°C ≤ T _A ≤ +125°C		35	100	pA
Input Offset Current	I _{OS}	−40°C ≤ T _A ≤ +125°C		0.7	1.0	nA
		−40°C ≤ T _A ≤ +125°C		20	50	pA
		−40°C ≤ T _A ≤ +125°C			150	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = 0 V to 2.5 V	110	140		dB
		−40°C ≤ T _A ≤ +125°C	100	135		dB
Large Signal Voltage Gain	A _{VO}	R _L = 10 kΩ, V _O = 0.1 V to 1.7 V	110	140		dB
		−40°C ≤ T _A ≤ +125°C	105	135		dB
Offset Voltage Drift	ΔV _{OS} /ΔT	−40°C ≤ T _A ≤ +125°C		0.03	0.1	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V _{OH}	R _L = 100 kΩ to ground	2.68	2.698		V
		−40°C ≤ T _A ≤ +125°C	2.68			V
		R _L = 10 kΩ to ground	2.67	2.68		V
		−40°C ≤ T _A ≤ +125°C	2.66			V
Output Voltage Low	V _{OL}	R _L = 100 kΩ to V+		1.7	5	mV
		−40°C ≤ T _A ≤ +125°C		2.4	5	mV
		R _L = 10 kΩ to V+		14	20	mV
		−40°C ≤ T _A ≤ +125°C		20	25	mV
Short-Circuit Limit	I _{SC}			±8		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V _S = 2.7 V to 5.5 V	105	125		dB
		−40°C ≤ T _A ≤ +125°C	100	125		dB
Supply Current/Amplifier	I _{SY}	I _O = 0		150	180	μA
		−40°C ≤ T _A ≤ +125°C		190	215	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R _L = 10 kΩ		0.4		V/μs
Settling Time 0.01%	t _s	G = ±1, 1 V step, C _L = 20 pF, R _L = 1 kΩ		5		μs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			600		kHz
Phase Margin	∅ _O	R _L = 10 kΩ, R _L = 100 kΩ, C _L = 20 pF		65		Degrees
NOISE PERFORMANCE						
Voltage Noise	e _{n p-p}	f = 0.1 Hz to 10 Hz		2.0		μV p-p
Voltage Noise Density	e _n	f = 1 kHz		50		nV/√Hz

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	+6 V
Input Voltage	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Differential Input Voltage	$\pm 6\text{ V}$
Output Short-Circuit Duration to GND	Observe derating curve
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	-40°C to $+125^\circ\text{C}$
Junction Temperature Range	-65°C to $+150^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply at 25°C , unless otherwise noted.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead TSOT-23 (UJ-5)	207	61	$^\circ\text{C}/\text{W}$
8-Lead SOIC_N (R-8)	158	43	$^\circ\text{C}/\text{W}$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

$V_{SY} = 5\text{ V}$ or $\pm 2.5\text{ V}$, unless otherwise noted.

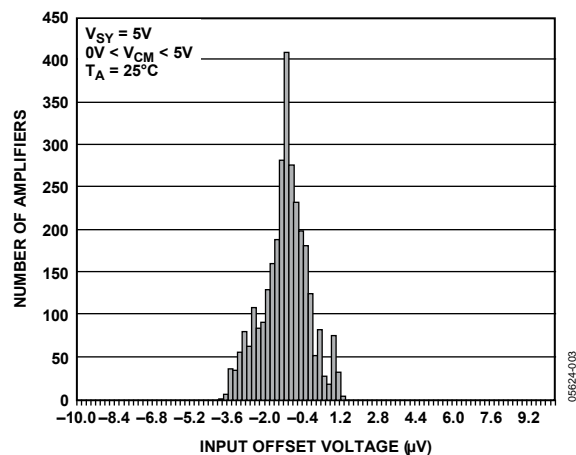


Figure 3. Input Offset Voltage Distribution

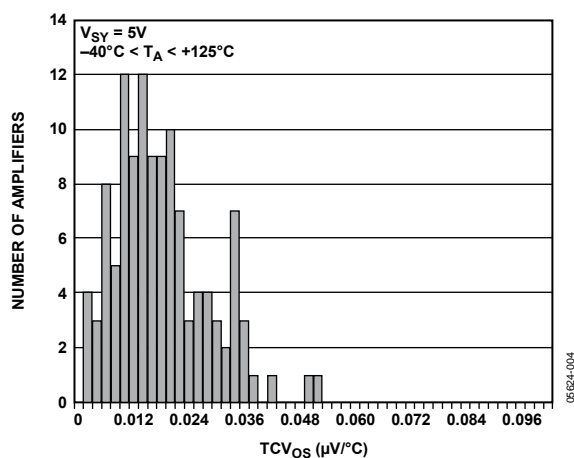


Figure 4. Input Offset Voltage Drift Distribution

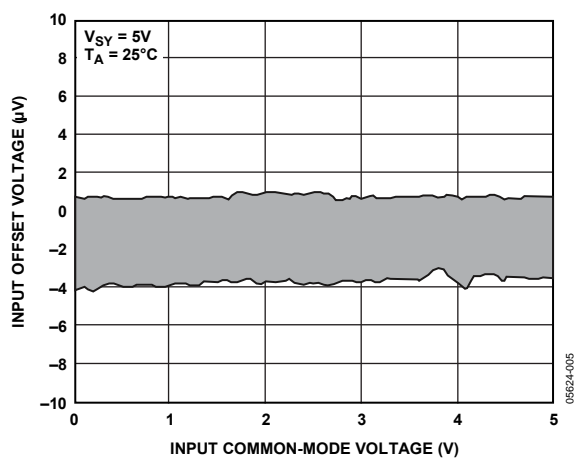


Figure 5. Input Offset Voltage vs. Input Common-Mode Voltage

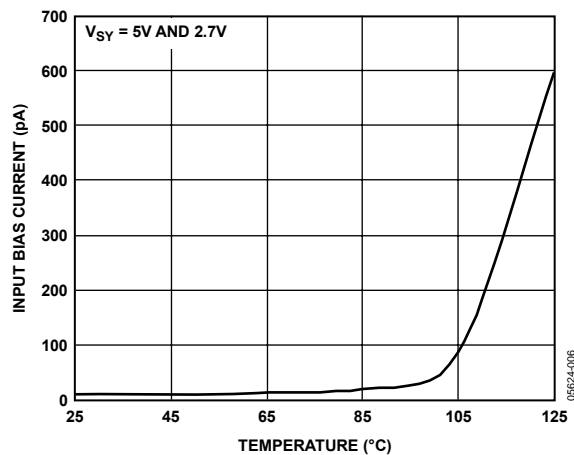


Figure 6. Input Bias Current vs. Temperature

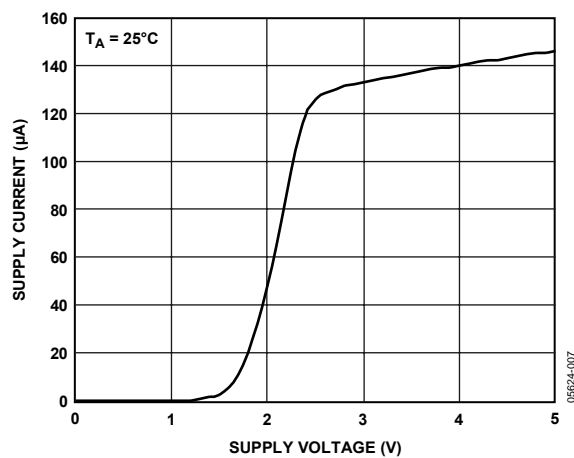


Figure 7. Supply Current vs. Supply Voltage

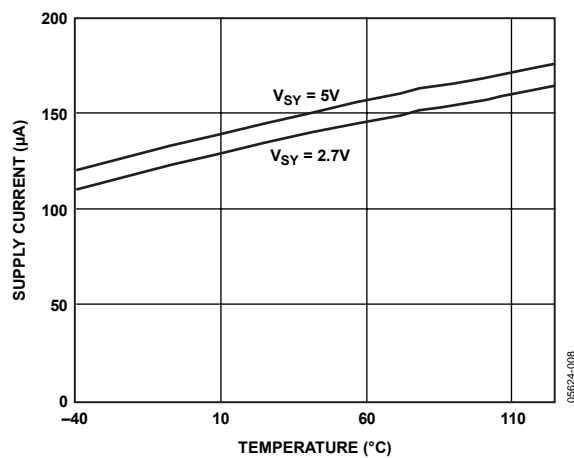


Figure 8. Supply Current vs. Temperature

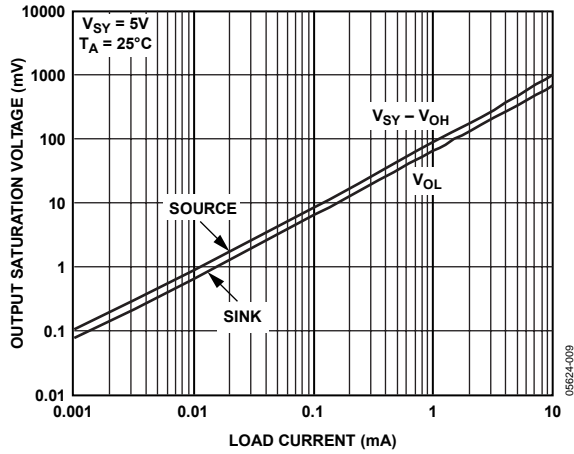


Figure 9. Output Saturation Voltage vs. Load Current

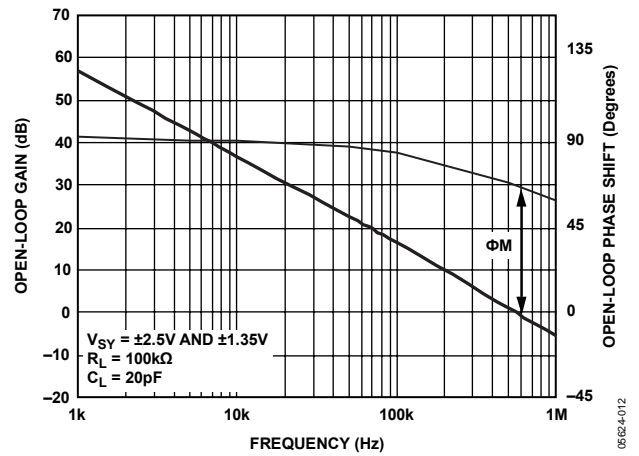


Figure 12. Open-Loop Gain and Phase vs. Frequency

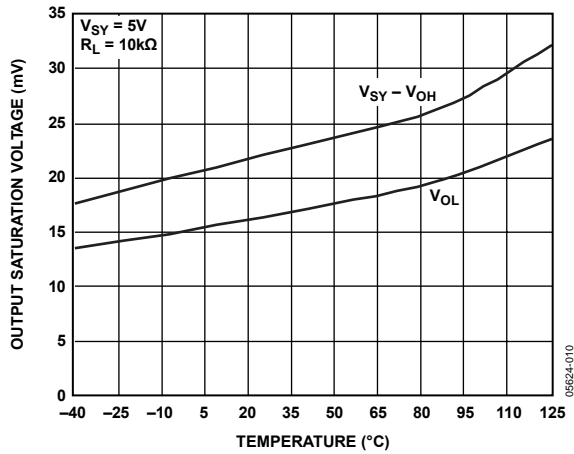


Figure 10. Output Saturation Voltage vs. Temperature

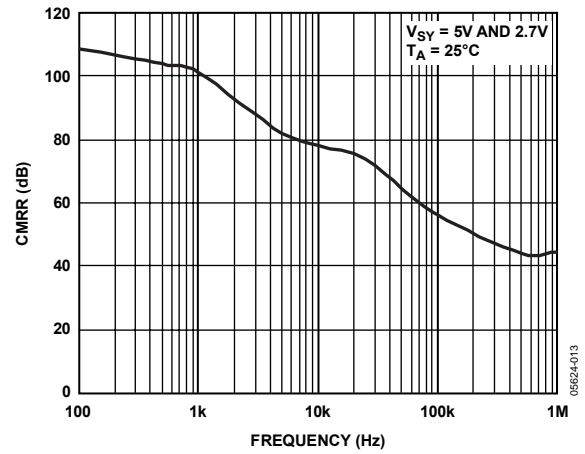


Figure 13. CMRR vs. Frequency

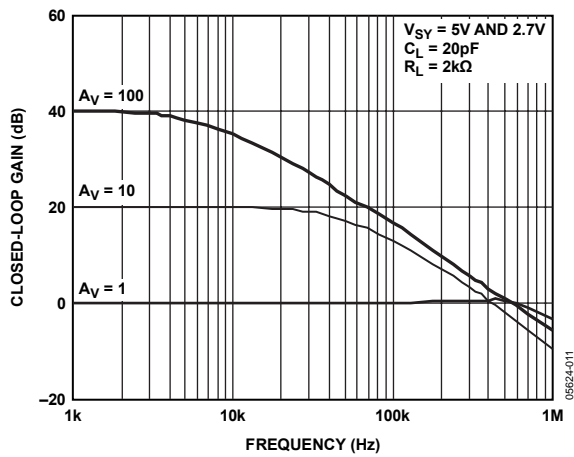


Figure 11. Closed-Loop Gain vs. Frequency

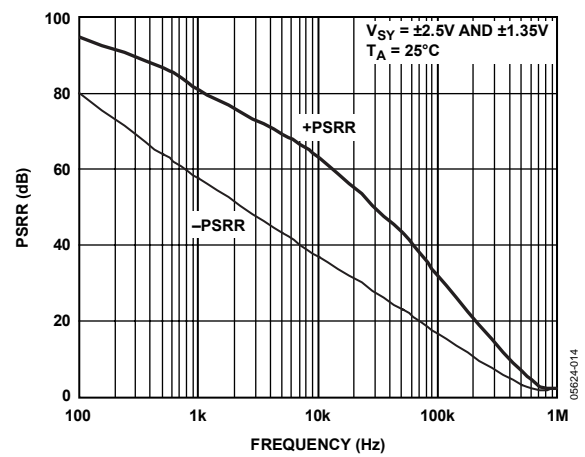


Figure 14. PSRR vs. Frequency

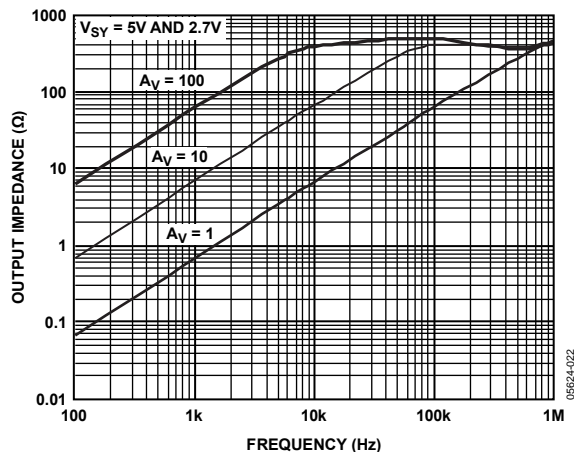


Figure 15. Closed-Loop Output Impedance vs. Frequency

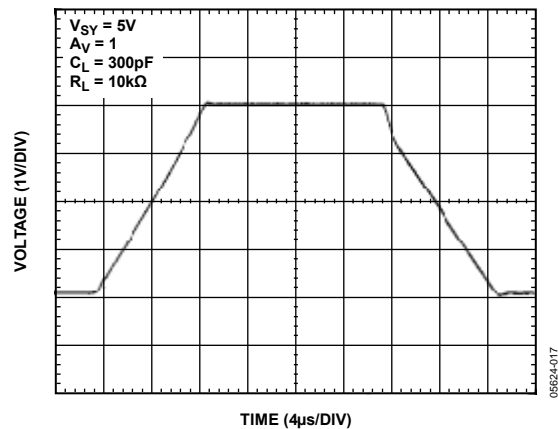


Figure 18. Large Signal Transient Response

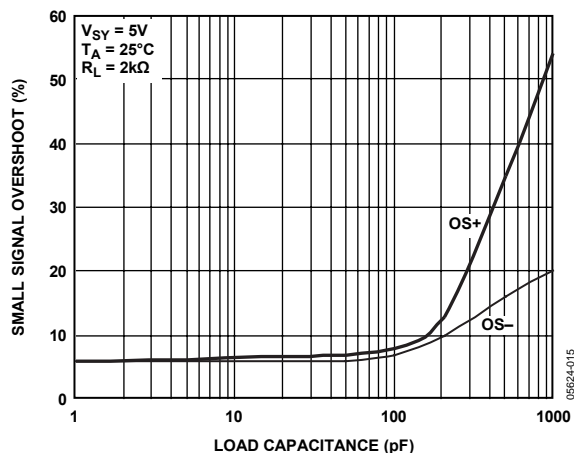


Figure 16. Small Signal Overshoot vs. Load Capacitance

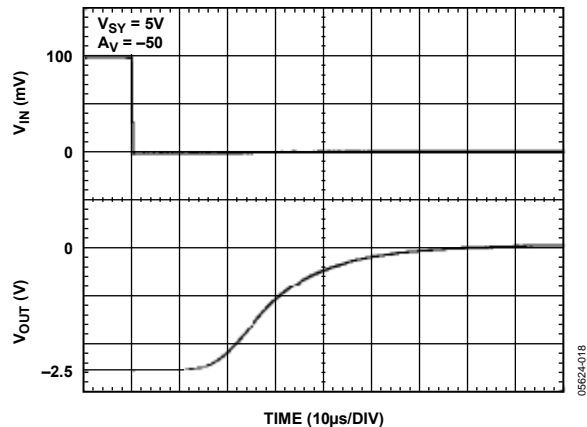


Figure 19. Positive Overload Recovery

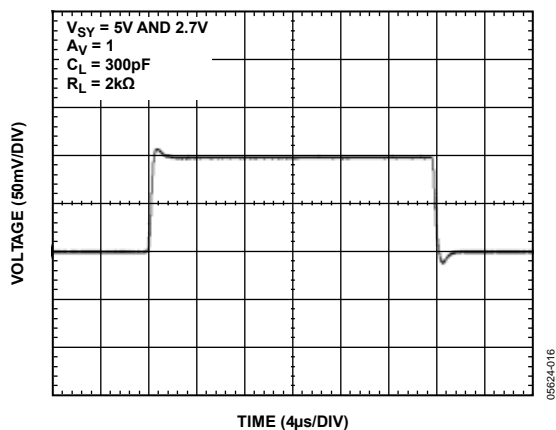


Figure 17. Small Signal Transient Response

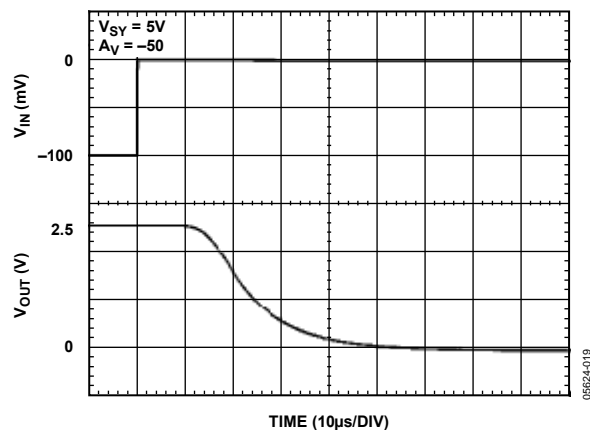


Figure 20. Negative Overload Recovery

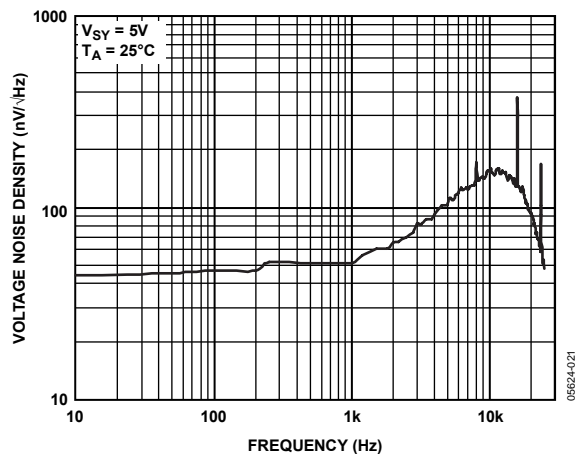


Figure 21. Voltage Noise Density

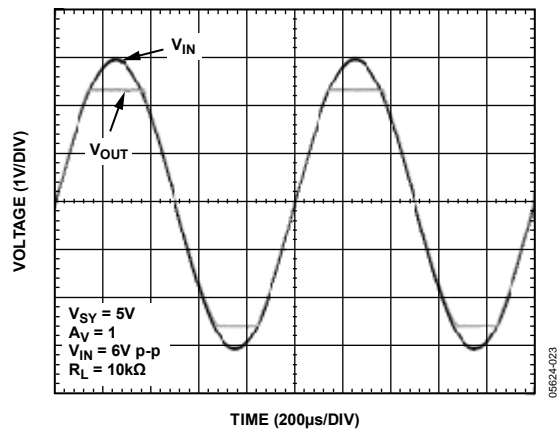


Figure 23. No Phase Reversal

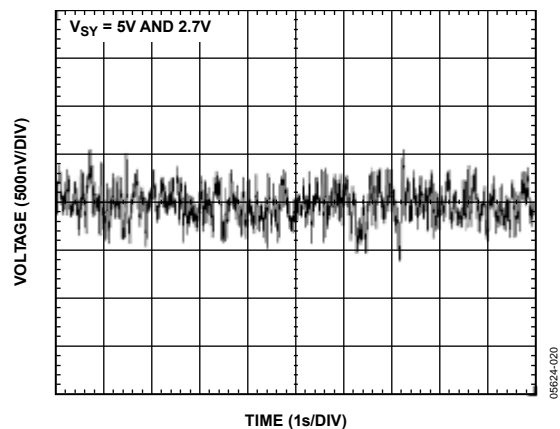


Figure 22. 0.1 Hz to 10 Hz Input Voltage Noise

$V_S = 2.7\text{ V}$ or $\pm 1.35\text{ V}$.

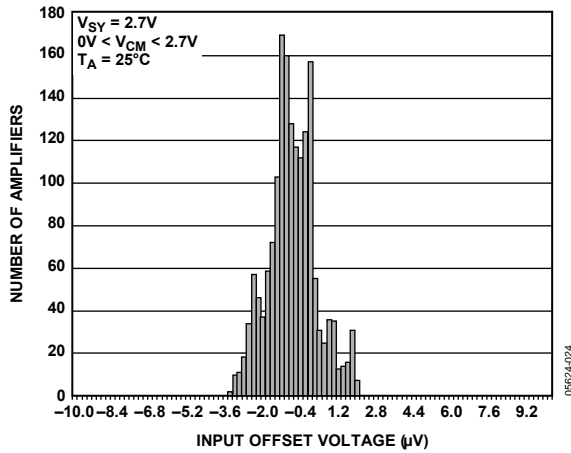


Figure 24. Input Offset Voltage Distribution

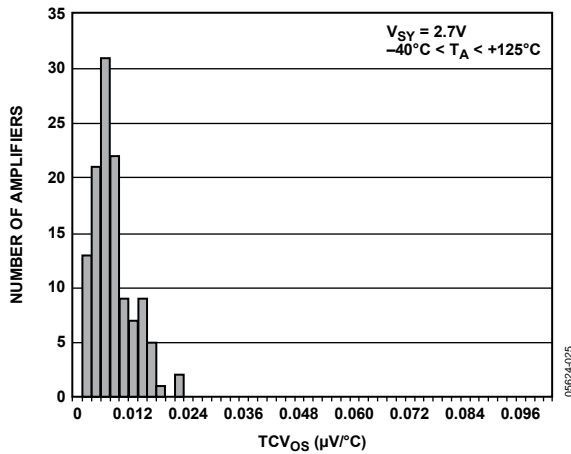


Figure 25. Input Offset Voltage Drift Distribution

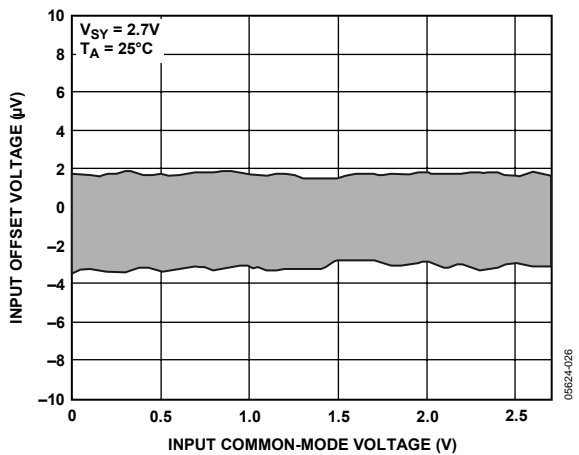


Figure 26. Input Offset Voltage vs. Input Common-Mode Voltage

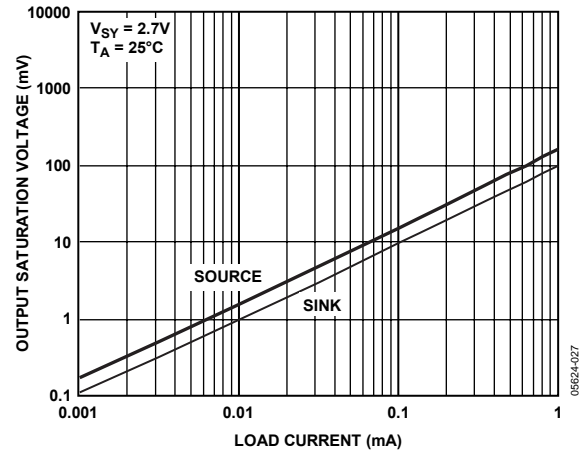


Figure 27. Output Saturation Voltage vs. Load Current

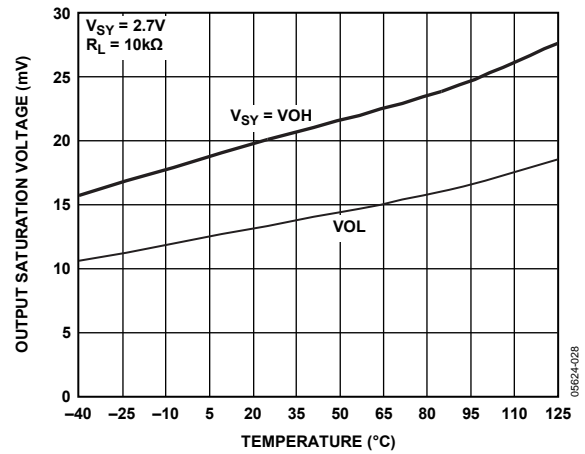


Figure 28. Output Saturation Voltage vs. Temperature

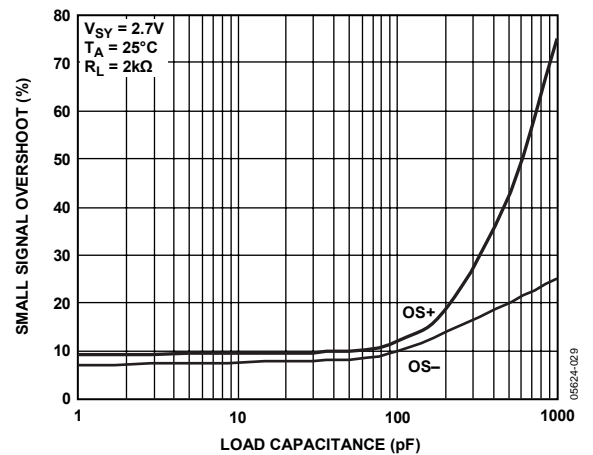


Figure 29. Small Signal Overshoot vs. Load Capacitance

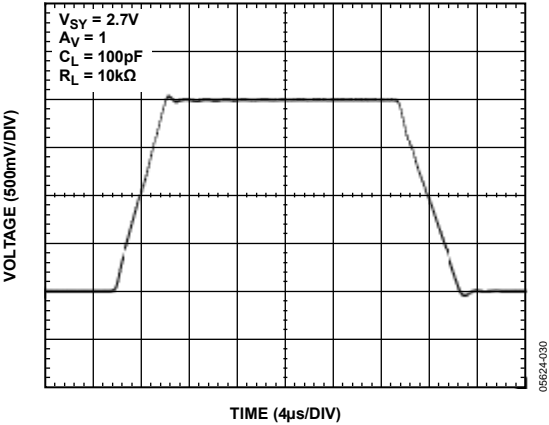


Figure 30. Large Signal Transient Response

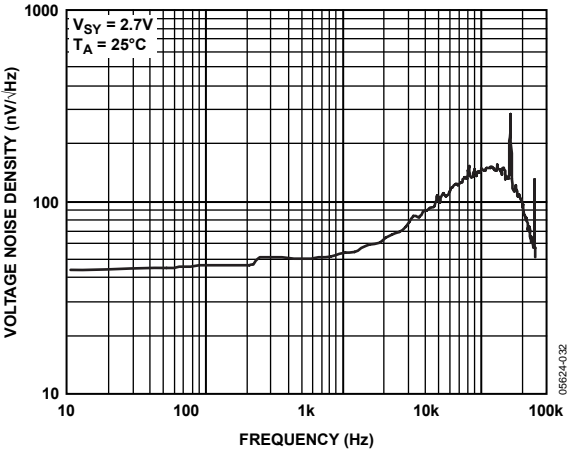
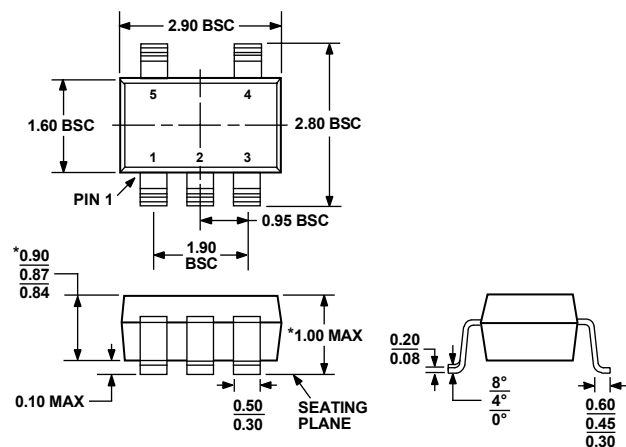


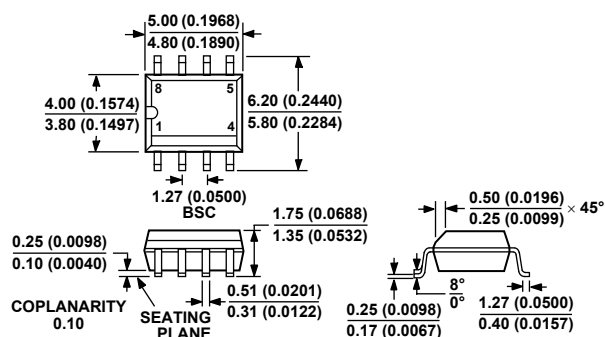
Figure 31. Voltage Noise Density

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 32. 5-Lead Thin Small Outline Transistor Package [TSOT_23] (UJ-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 33. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8538AUJZ-R2 ¹	−40°C to +125°C	5-Lead TSOT-23	UJ-5	AOC
AD8538AUJZ-REEL ¹	−40°C to +125°C	5-Lead TSOT-23	UJ-5	AOC
AD8538AUJZ-REEL7 ¹	−40°C to +125°C	5-Lead TSOT-23	UJ-5	AOC
AD8538ARZ ¹	−40°C to +125°C	8-Lead SOIC_N	R-8	AOC
AD8538ARZ-REEL ¹	−40°C to +125°C	8-Lead SOIC_N	R-8	AOC
AD8538ARZ-REEL7 ¹	−40°C to +125°C	8-Lead SOIC_N	R-8	AOC

¹ Z = Pb-free part.