HDMI Layout Guideline

Introduction

This FAQ presents a general guideline to laying out HDMI traces on circuit boards. Many of the problems we see in the forum threads can be traced back to routing and layout issues. The rules and notes I present here have been gleaned from various boards I have designed and seen over the years. I can not reference back to the original sources for this information however simple web searches will reveal many documents covering this topic.

HDMI 1.4b specification defines signaling up to 3 GHz requiring board designers to be very careful with HDMI signal integrity during layout. Following is a good set of rules that will allow you to transmit 3 GHz across FR-4 PCBs.

First Some Math

Let's assume we have a transmitter routed to a connector and we want to transmit a format with 297MHz clock rate.

- Tbit = time duration for a single bit across a TMDS channel
- Tcharacter = 10 x Tbit
- CLK = 297MHz
- Data = 10 x CLK
- Propagation Delay for FR4 ~= 6.67ps/mm

- Intra-pair skew = 0.15 Tbit
- Inter-pari skew = 0.20 Tcharacter

Therefore:

- Data rate = 10 x 297MHz = 2.97GHz = 336.7ps
- Intra-pair skew in time = 0.15 x 336.7ps = 50.50ps
- Intra-pair skew in distance = 50.50ps / 6.67ps/mm = 7.57mm

Layout Rules

Layout is key. The following is a general set of rules that has become part of my layout specification for boards. They are a bit tighter then the math above indicates but are easily met during layout. These rules can be added directly as constraints to your schematic or as part of the layout specification document.

1. Each HDMI channel is comprised of 4 TMDS pairs.
2. Each HDMI channel set shall be routed primarily on the top or bottom layer as a group or alternately routed as a group on internal layers.
3. Each TMDS signal shall have single ended impedance of 50 Ω ± 10%.
4. Each TMDS pair shall have differential impedance of 100 Ω ± 5%.
5. Signals within a TMDS pair shall have matching lengths of ± 3mm.
6. Signals within a TMDS pair shall not have any 90 degree corners. Corners shall be chamfered.
7. TMDS signal chamfer length to trace width ratio shall be 3 to 5.
8. TMDS signal distance between bends should be 8 to 10 times the trace width
9. TMDS pairs in each HDMI channel shall have matching lengths of ± 3mm.
10. TMDS pairs shall be separated from adjacent TMDS pairs by a minimum of 1.2 mm.
11. TMDS pairs shall be separated from adjacent non-pair signals by a minimum of 7.8 mm.
12. HDMI channel sets shall be separated from other HDMI channel sets by a minimum of 7.8 mm.
13. HDMI channel sets shall be referenced to an adjacent solid ground plane.
14. If a HDMI channel set must transition to another reference ground plane then ground plane to ground plane vias must be added adjacent to the channel transition vias.

Fabrication Notes

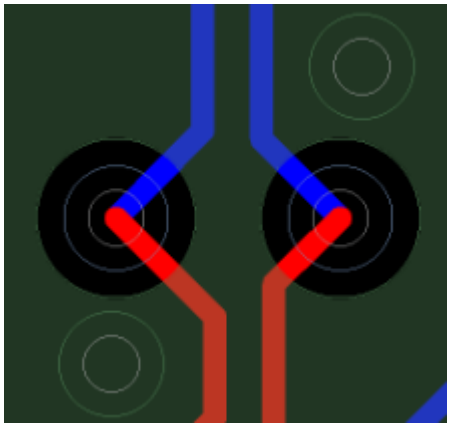
The following is a general set of instruction notes placed on the PCB fabrication drawing. They allow the PCB fabricator to tweak the gerbers to match their process and materials.

1. Characteristic impedance of all signal layers to be 50 Ω ± 10%
2. Differential impedance of 0.127 mm traces with 0.192 mm gap shall be 100Ω ± 10%. Vendor may adjust trace widths, trace spacings and dielectric thickness as required. (this note is for the TMDS

pairs only, extra information may need to be passed on to the fabricator to indicate exactly which traces are part of a HDMI channel set)

How to handle reference plane transitions

Analog Devices HDMI components are designed so routing is a straight shot from the device pin to the connector pin. However sometimes you need to change layers the HDMI routing is done on, often changing the reference ground plane in the process. The transition vias should be symmetrically placed in the path and ground to ground vias to handle the signal integrity of reference plane jumping as illustrated below



This particular example is from an eight layer board, the red trace is on the top layer, the blue trace is on the bottom layer and the dark green layers are the solid ground planes adjacent to the top and bottom layers. Note that the vias are place symmetrically in the path and separated by 1.14mm. Also note the 2 ground vias adjacent to the 2 trace vias.

In this example if the differential pair jumped from layer 1 to layer 3, no ground to ground vias would need to be added since you are not jumping reference ground planes.

It is best to keep the number of differential pair vias to a minimum since each via introduces impedance changes.

It is also a good idea to stitch ground to ground vias along the trace path every 2 cm or so. This aids in general signal integrity control.

How far can you go?

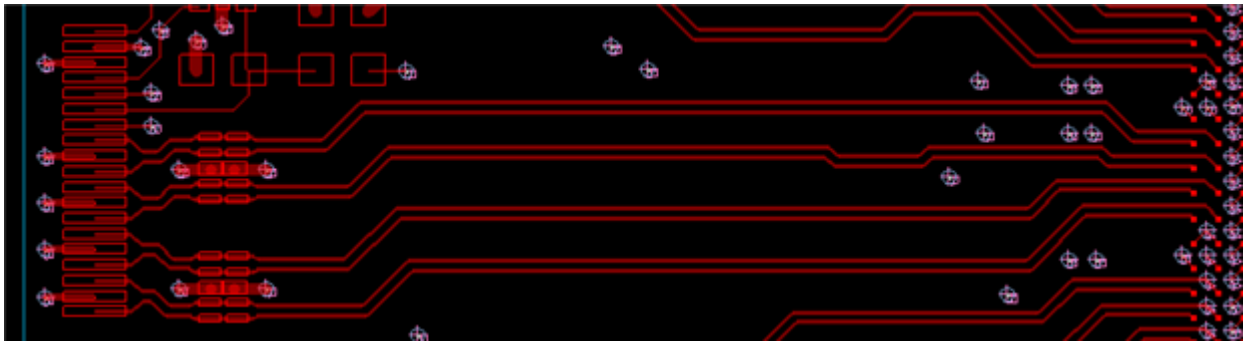
Normally HDMI traces on boards are very short, directly from the connector to the receiver/transmitter. Many times we get the question of how long can I make HDMI traces. The HDMI specification does not define maximum length, only expected impedance. As long as you follow the layout rules above you should be able to run HDMI traces over 20-30cm easily. Longer if you are careful.

ESD Protection

ESD protection devices are often added to increase ESD protection levels. I suggest devices with signal flow through like Semtech RClamp0524. They allow HDMI signals to flow directly under the part while providing low capacitance ESD protection. There are many vendors producing these types of low capacitance TVS arrays.

HDMI Differential Routing Example

Here's an example HDMI routing from a horizontal HDMI connector on the left to an ADV7850 receiver port.



Things to Note:

- Smooth flow through from connector through ESD protection and to the ADV7850
- Jog in TMDS pair used to equalize pair to pair lengths
- Pair to pair separation where feasible
- Pair to non-HDMI channel signal separation

The Big Picture

Designing a HDMI transmitter or receiver board is just part of the of the whole system. You must always keep in mind that you are often connecting through a cable to a source/sink. The connection from the board to the cable and from the cable to the source/sink are transition points. Most HDMI connectors are 100 Ω ± 15% and cables have attenuation proportional to the length. Poor transition points can cause reflections causing poor signal integrity. Long cables will attenuate signals decreasing the swing voltage at the receiver dropping the received signal out of specification. All these problem become more prevalent at higher resolution like 1080p or 4K.

Analog Devices Inc provides many reference board designs from which you can copy layouts from.

I recommend using signal integrity tools to verify HDMI trace layouts meet specifications.

Disclaimers:

- These guidelines are what I use designing HDMI circuit boards. They are not intended to be definitive in any way but are intended to aid other designers understanding what to do and look out for.

References:

- High-Definition Multimedia Interface 1.4b
- DVP PCB Layout Recommendations (??need link??)

Comments

15 comments 0 members are here

ments

GuenterL *over 4 years ago in reply to moisesm3* +1

From CEA861E, 1080p120 => 297Mhz pixel rate =? TMDS rate = 10 * 297MHz = 2.97GMhz (3G).

Yes, 1080p60 deep color only goes to 2.25GHz

Where in the spec do you see the 3.4Ghz limit?

For HDMI2.0...

GuenterL *over 4 years ago in reply to moisesm3* +1

That cable assembly just specs 340MHz for the cable. Receivers and transmitters are designed for 3G ma

When you talk about transmitting a byte (01010101), the transmitter is doing 8b10 encoding.
...

GuenterL *over 4 years ago in reply to moisesm3* +1

FR4 propagation delay at 3Ghz = ~6.67ps/mm. This is not related to Gbps, it's just a pure single ended pro

What's important is the differential arrival time of data signals to the...

Sasa *over 6 years ago*

Thank You

About ESD-protection. I use CM2031-A0TR for Rx and CM2020-00TR for Tx (ON Semiconductor).

mightyohm *over 4 years ago*

This is very useful & helpful, thanks!

One suggestion - please give the stackup details of your PCB. Otherwise your trace/space recommendations are not meaningful, since they are tied to a specific dielectric thickness (5 mils?).

> **GuenterL** *over 4 years ago in reply to mightyohm*
>
> Thanks for the compliment.
>
> Stack up and trace widths are all dependent on your PCB specifications, mostly affected by pre-preg material and thickness. I've created a simple tool to get a 1st order approximation of the stack up. You can find it here.
>
> PCB Trace Impedance Calculator
>
> You really need to work with layout and fabricators to get to the final solution.
>
> My normal boards are designed with 4 mil FR4 pre-preg and 5 mil traces on the outer layers. Gives a 55 Ohm single ended impedance. If you space them 7 mils apart it'll give you ~100 differential.

moisesm3 *over 4 years ago*

Hi Guenter,

This is a pretty good guide, although there is something that confuses me.

HDMI1.4b supports data rates up to 3.4Gbps, this would create a signal with max frequency of 1.7Ghz

HDMI2.0 supports data rates up to 6Gbps, this would create a signal with max frequency of 3Ghz

So, 6.67ps/mm is for a signal of 3GHz(6Gbps HDMI2.0) or 3.4Gbps(1.7Ghz HDMI1.4b)?

Do you have a plot ps/mm vs GHz?

Regards

> **GuenterL** *over 4 years ago in reply to moisesm3*
>
> From CEA861E, 1080p120 => 297Mhz pixel rate =? TMDS rate = 10 * 297MHz = 2.97GMhz (3G).
>
> Yes, 1080p60 deep color only goes to 2.25GHz
>
> Where in the spec do you see the 3.4Ghz limit?
>
> For HDMI2.0 4Kp60 => pixel rate at 594MHz => 10 * 594MHz => 5.94GHz tmds rate but this is for HDMI 2.0
>
> This guide was originally done for 3G designs. I'll have to update it for 6G in the future.
>
> Ideally you'd want intra-pair skew to be less than (7.57 / 2) mm
>
> > **moisesm3** *over 4 years ago in reply to GuenterL*
> >
> > Hi Guenter,

Thanks for your prompt response.

Category 2 cables support TMDS clock frequencies up to 340MHz, supporting 3.4Gbps. Section 4.2.6 or table 4-1

But this is no what confuses me.

a 3.4Gbps signal will need a 3.4GHz clock to recover the data(or 1.7GHz if working in dual data rate), but the signal itself will generate a maximum of 1.7GHz this would be in the case a sequence of ones and zeros is transmitted(1010101)

So, if 6.67ps/mm is for 3GHz signals, this is the delay a 6Gbps signal will have.

If 6.67ps/mm is for a 3Gbps signal, then it is the delay for a 1.5GHz signal.

Gbps = 2*GHz

6.67ps/mm is for 3GHz or 1.5GHz?

GuenterL *over 4 years ago in reply to moisesm3*

That cable assembly just specs 340MHz for the cable. Receivers and transmitters are designed for 3G max.

When you talk about transmitting a byte (01010101), the transmitter is doing 8b10 encoding. This is where the 10x comes from. What's important is the differential delay between different pairs of channels. All 4 tmds pairs could be delayed 100ns without problems. But they all must be delayed together. Differential delay between pairs are limited to 0.15Tbit so the 10 bit symbols can be decoded by the receiver. If one tmds pair gets delayed by 1 bit, the 10bit symbol decoding will be out of sync and broken.

moisesm3 *over 4 years ago*

Hi Guenter,

I understand, the main question remains the same:

6.67ps/mm is for:

3GHz(6Gbps) or 3Gbps(1.5GHz)

Regards

GuenterL *over 4 years ago in reply to moisesm3*

FR4 propagation delay at 3Ghz = ~6.67ps/mm. This is not related to Gbps, it's just a pure single ended propagation delay.

What's important is the differential arrival time of data signals to the sink are less than one bit apart so the sink can synchronize the symbols. For 4Kp30 the clock rate is 297MHz and the data rate is 2.97GHz.

moisesm3 *over 4 years ago in reply to GuenterL*

Of course it is related to Gbps,

If you have a single ended signal say a long sequence of 10101010101010101010101010 at 6Gbps it will create a square waveform of 3GHz every 10 is one cycle. This 3GHz waveform is present on the FR4 trace, to recover the signal a 6GHz clock would be needed.

Then, if 6.67ps/mm is for 3GHz, it will be used as the maximum FR4 attenuation of 6Gbps.

van.yang@analog.com *over 4 years ago*

It's very helpful, but i noticed that in the datasheet, the 0.15Tbit was defined as mininum intrapair skew for TMDS. why is it minimum?

GuenterL *over 4 years ago in reply to van.yang@analog.com*

Which data sheet are you referring to?

van.yang@analog.com *over 4 years ago in reply to GuenterL*

ADV7604, ADV7614

GuenterL *over 4 years ago in reply to van.yang@analog.com*

This looks like a typo in the datasheet. It doesn't make sense to have a minimum skew for a receiver part. Those should have been moved to the Maximum column. Good eye. Newer datasheets don't even list that parameter since the part meet HDMI specifications

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