A

REPORT

ON

DIGITAL ASSIGNMENT

Prepared in partial fulfillment of the Course

Analog and Digital VLSI Design (INSTR\EEE F313)

By:

Nikhil Motiani	**2011A8PS347P**
Naman Maheshwari	**2011A3PS199P**
Nitin Singla	**2011A3PS198P**

BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI

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SPECIFICATION OF THE DESIGN:

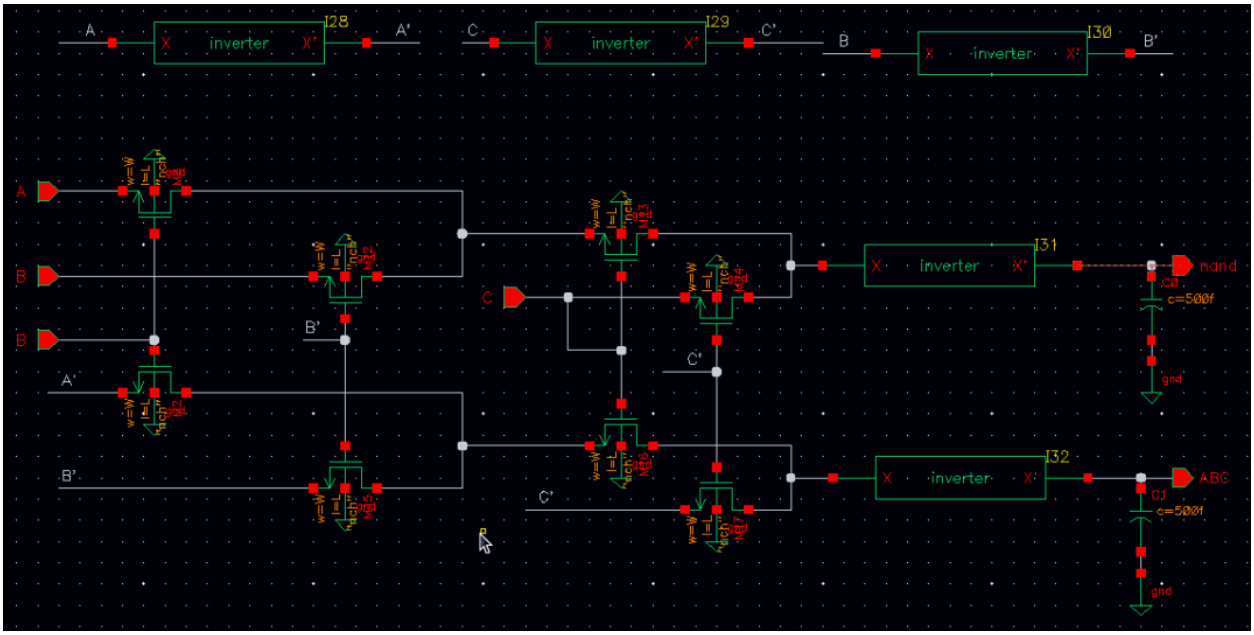
Designing a 3- input NAND/AND logic gate using Complementary Pass Logic style at 500 MHz with Load capacitance of 500fF.

APPROACH FOLLOWED:

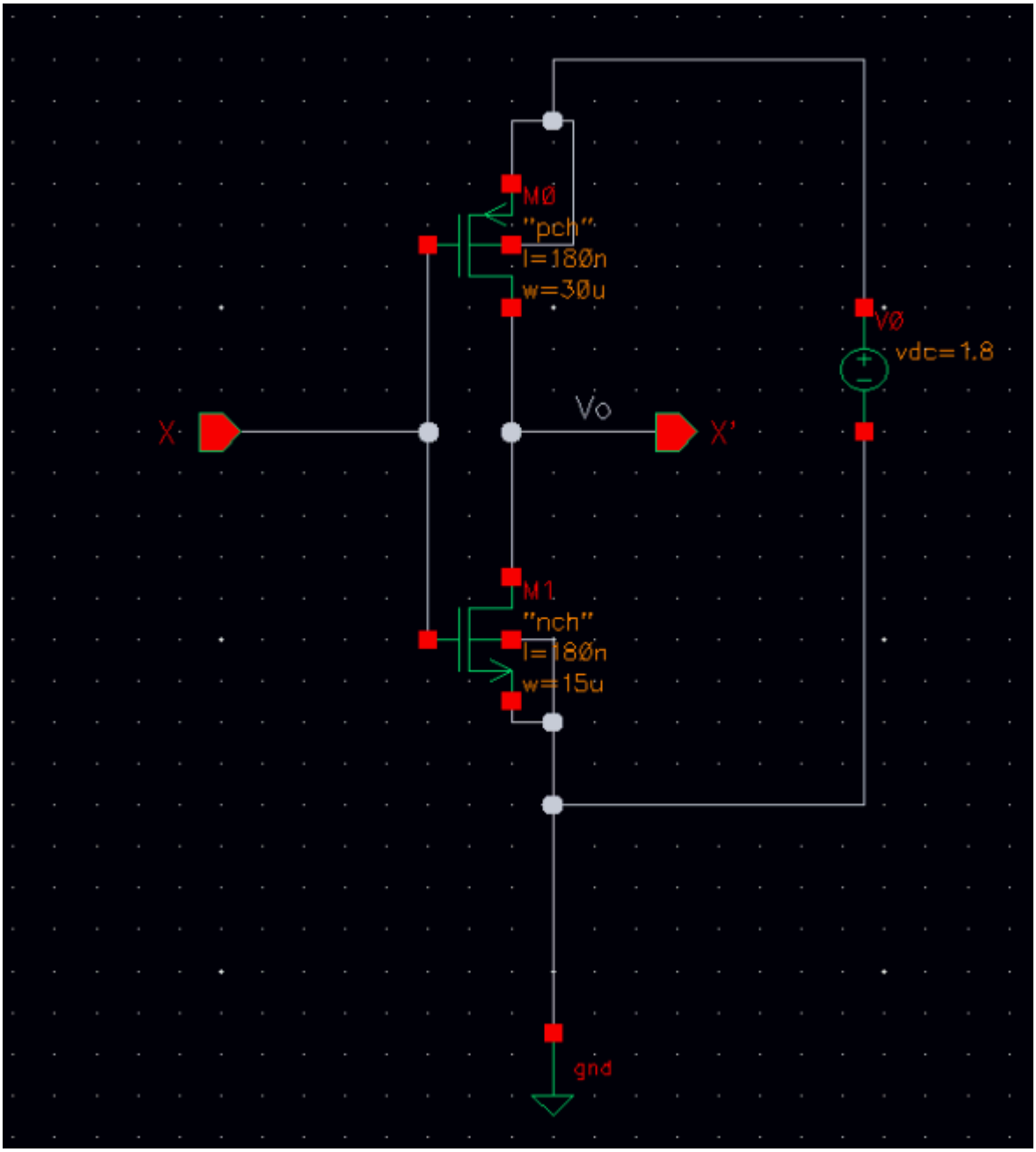
For delay minimization, W/L of p-mos is taken to be twice of the w/l of n-mos. As the frequency at which the circuit had to be operated is 500 MHz and the load capacitance is 500 fF, the W/L needed to be increased so that full logic levels could be reached, ie, the complete charging and discharging of capacitance could take place.

After the inverter was designed, it was used to take complementary inputs. Also, the W/Ls of the other transistors in the circuit were calculated in proportion to that of the inverter. To attain the full logic levels, the inverters were also added at the outputs.

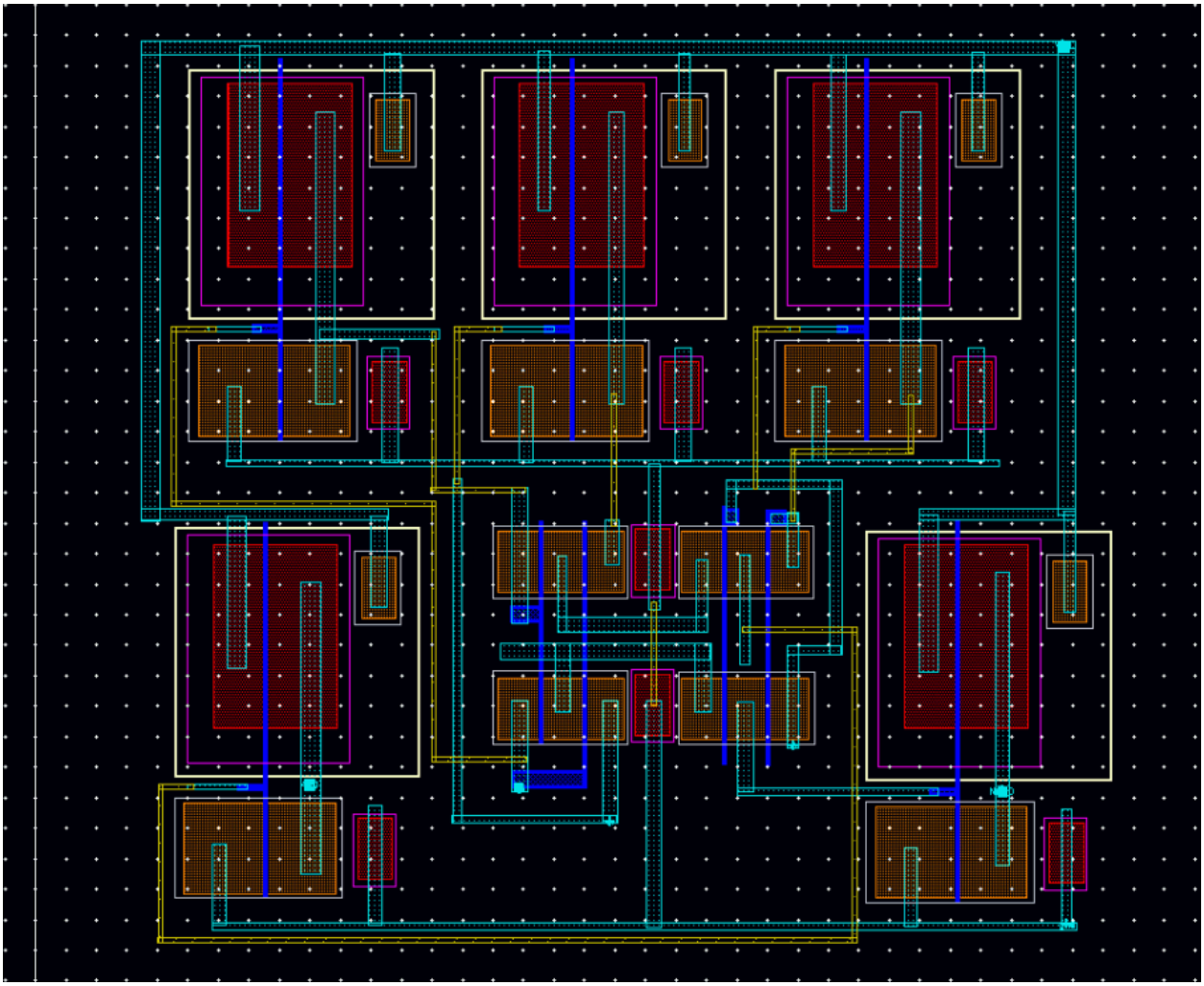
SCHEMATIC:



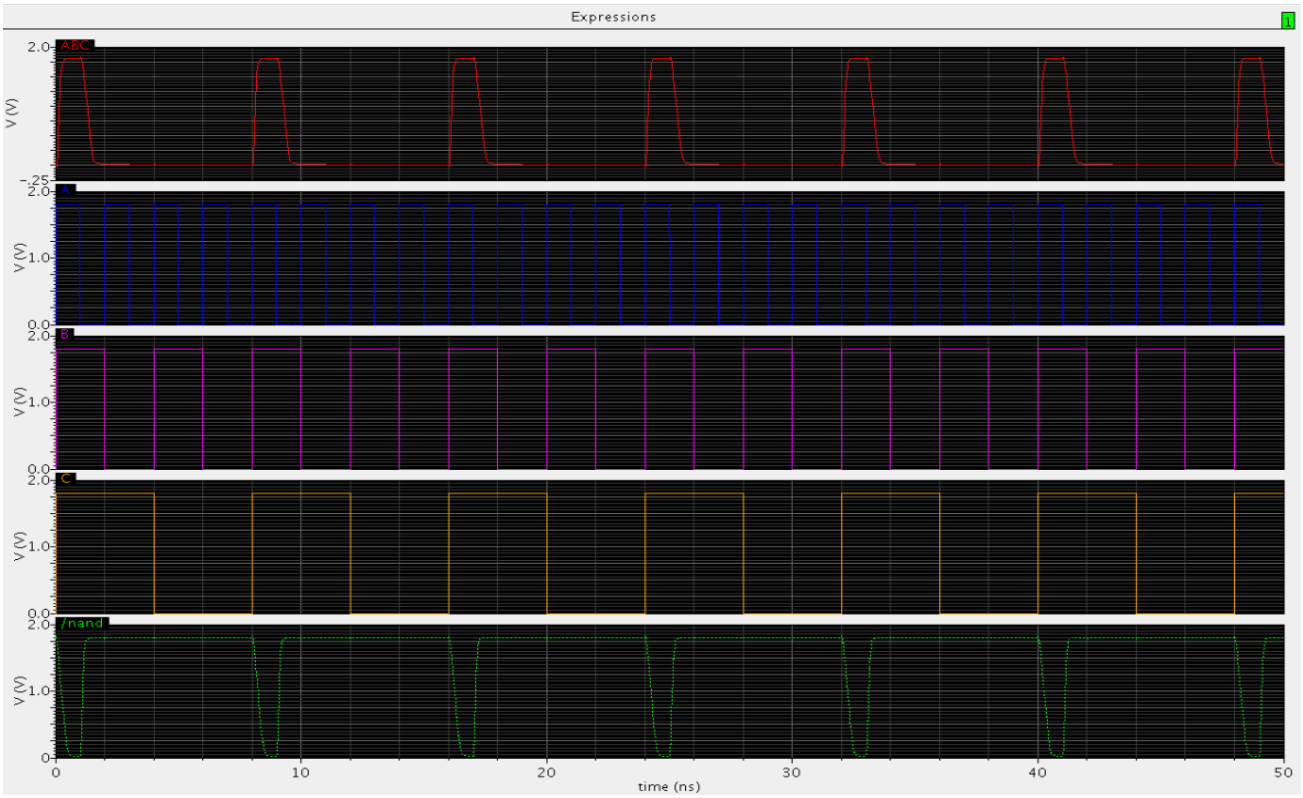
INVERTER SCHEMATIC:



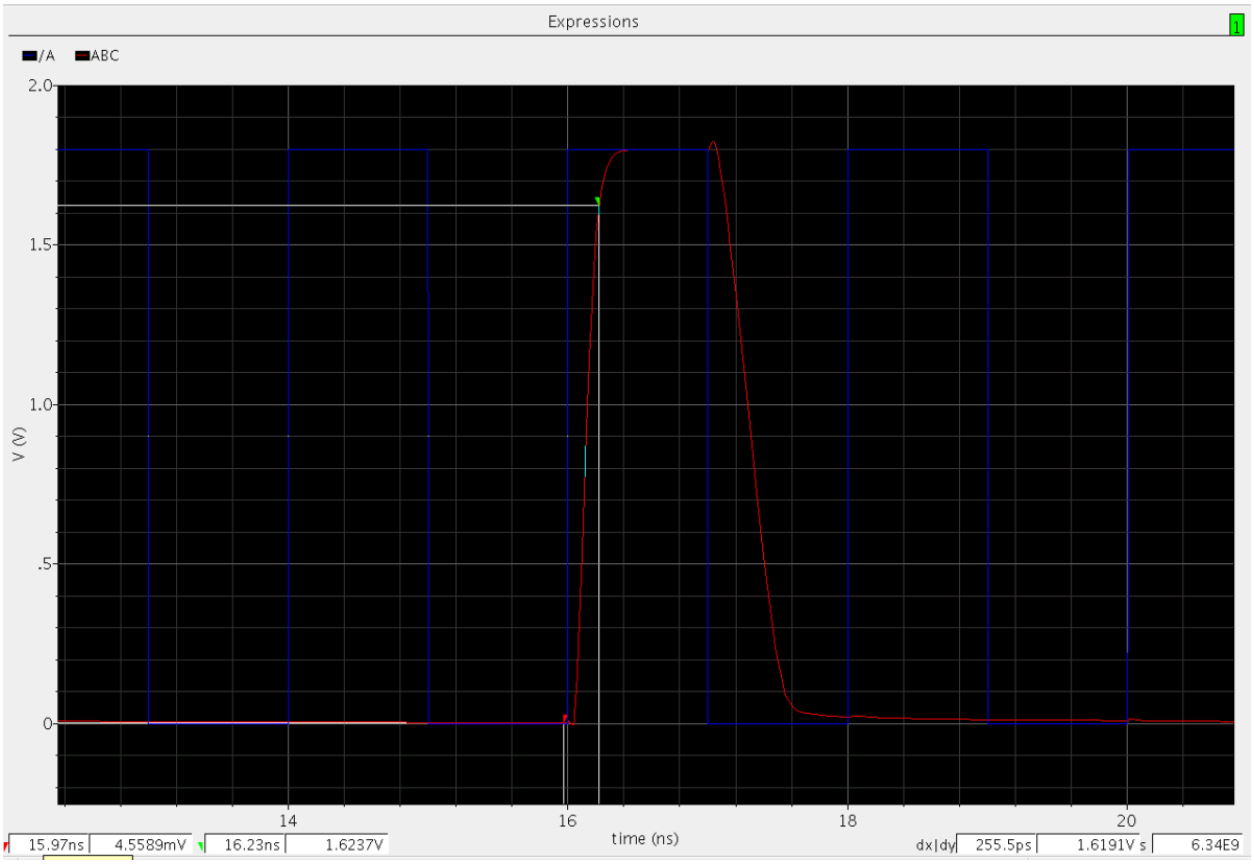
LAYOUT:



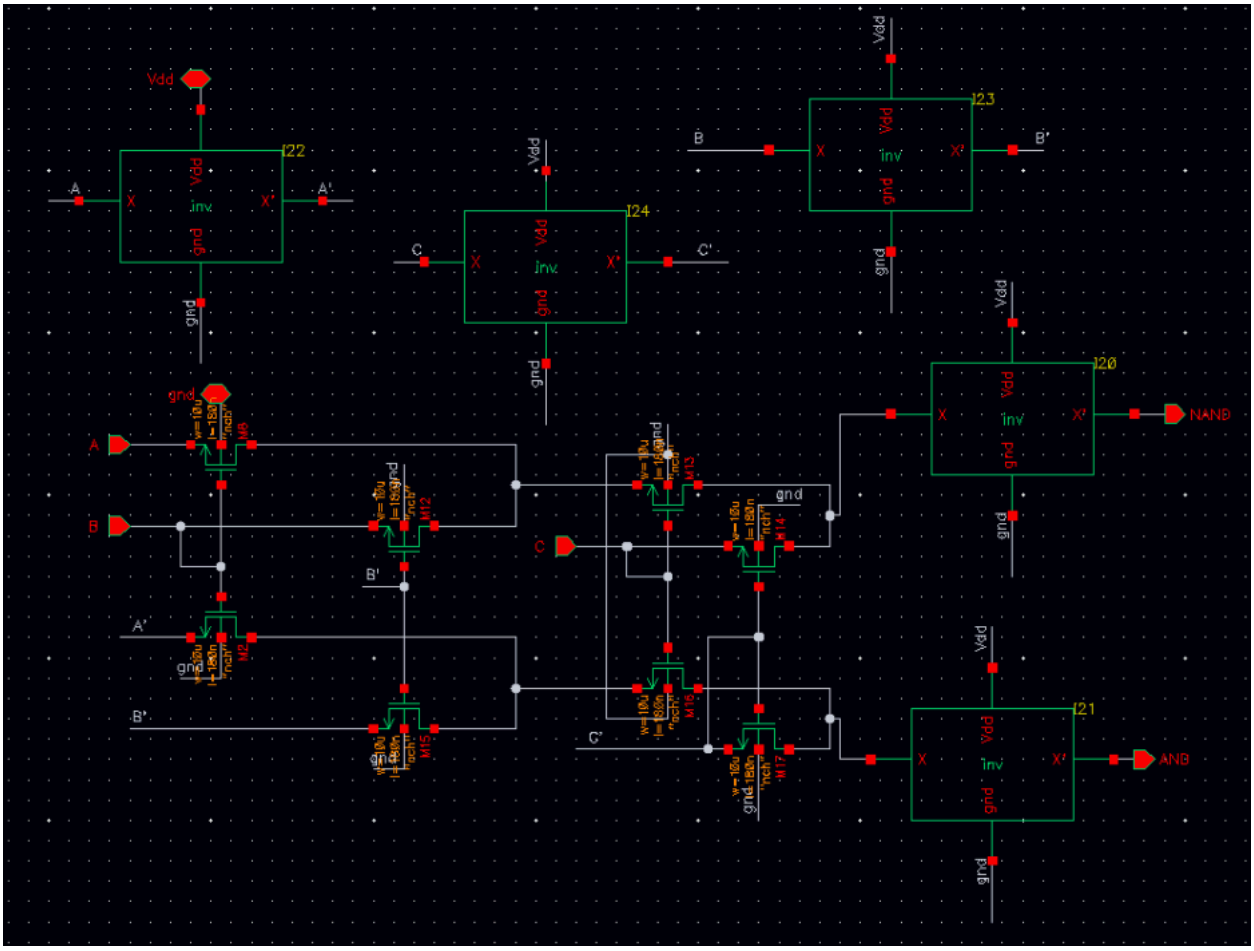
INPUTS AND OUTPUTS:



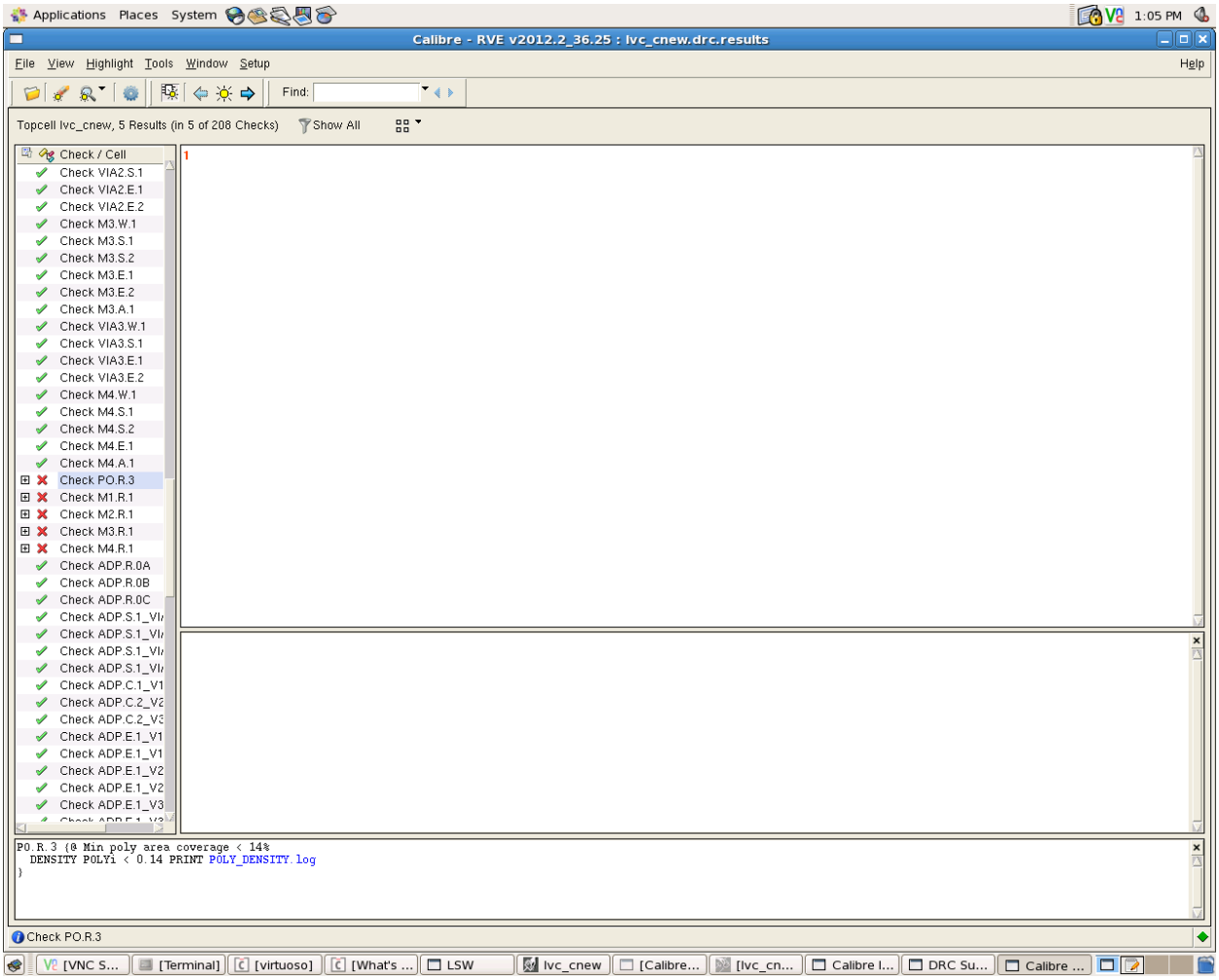
RISE TIME:


Expressions
/A
ABC
2.0
1.5
1.0
.5
0
V (V)
14
16
18
20
time (ns)
15.97ns
4.5589mV
16.23ns
1.6237V
dx|dy
255.5ps
1.6191V s
6.34E9

LVS CIRCUIT:


Vdd
gnd
A
A'
B
B'
C
C'
NANB
ANB
X
X'
inv
pdn
pun
I22
I23
I24
I20
I21
M1
M2
M11
M12
M13
M14
M15
M16
M17

DRC TEST:


Applications Places System
1:05 PM
Calibre - RVE v2012.2_36.25 : lvc_cnew.drc.results
File View Highlight Tools Window Setup
Help
Find:
Topcell lvc_cnew, 5 Results (in 5 of 208 Checks)
Show All
Check / Cell
Check VIA2.S.1
Check VIA2.E.1
Check VIA2.E.2
Check M3.W.1
Check M3.S.1
Check M3.S.2
Check M3.E.1
Check M3.E.2
Check M3.A.1
Check VIA3.W.1
Check VIA3.S.1
Check VIA3.E.1
Check VIA3.E.2
Check M4.W.1
Check M4.S.1
Check M4.S.2
Check M4.E.1
Check M4.A.1
Check PO.R.3
Check M1.R.1
Check M2.R.1
Check M3.R.1
Check M4.R.1
Check ADP.R.0A
Check ADP.R.0B
Check ADP.R.0C
1
PO.R.3 {@ Min poly area coverage < 14%
DENSITY POLYi < 0.14 PRINT POLY_DENSITY.log
}
Check PO.R.3
[VNC S...
[Terminal]
[virtuoso]
[What's ...
LSW
lvc_cnew
[Calibre...
[lvc_cn...
Calibre l...
DRC Su...
Calibre ...

LVS REPORT:

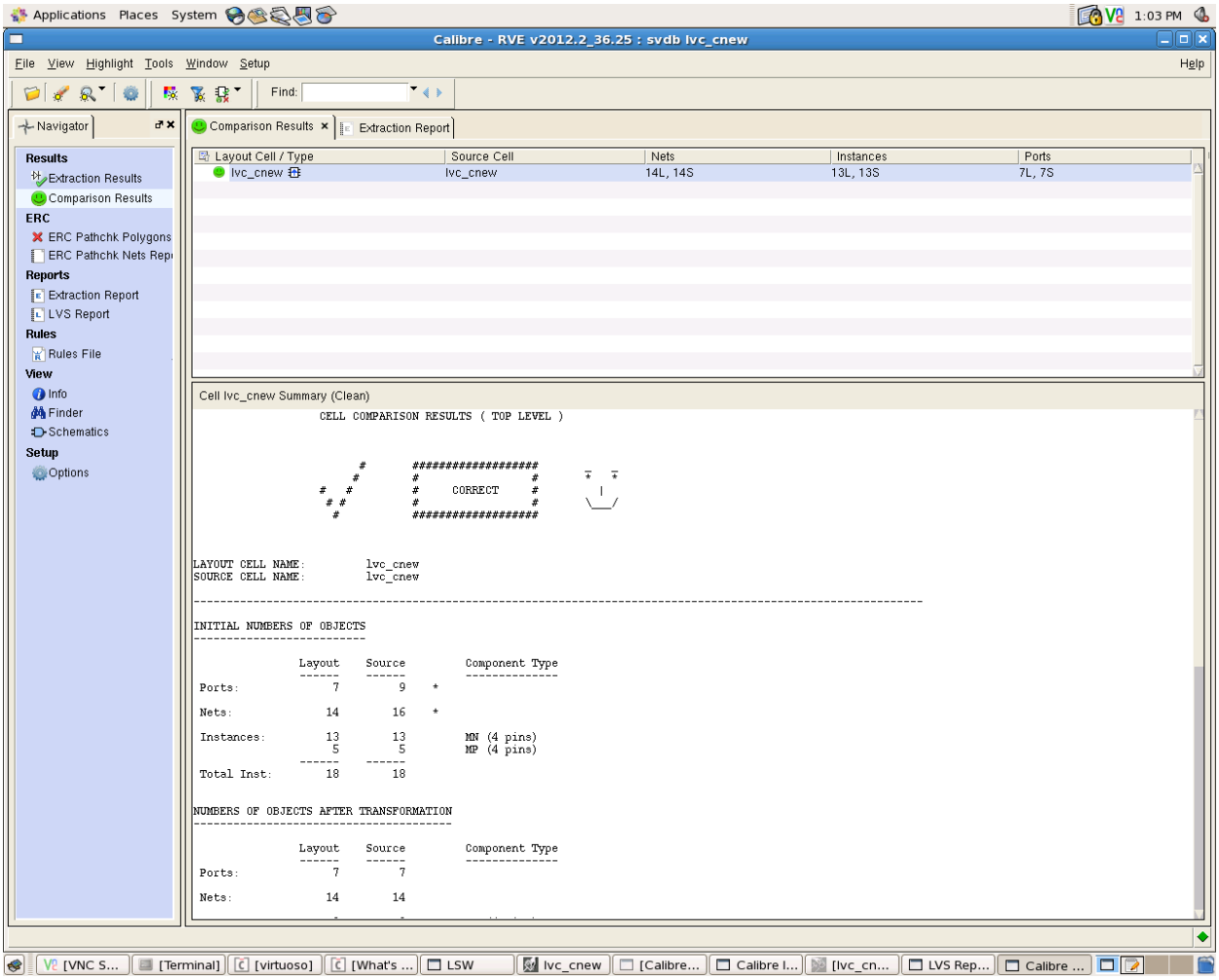

Applications Places System
1:03 PM
Calibre - RVE v2012.2_36.25 : svdb lvc_cnew
File View Highlight Tools Window Setup
Help
Find:
Navigator
Results
Extraction Results
Comparison Results
ERC
ERC Pathchk Polygons
ERC Pathchk Nets Rep
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Extraction Report
Layout Cell / Type
Source Cell
Nets
Instances
Ports
lvc_cnew
lvc_cnew
14L, 14S
13L, 13S
7L, 7S
Cell lvc_cnew Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: lvc_cnew
SOURCE CELL NAME: lvc_cnew
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 7 9 *
Nets: 14 16 *
Instances: 13 13 MN (4 pins)
5 5 MP (4 pins)
Total Inst: 18 18
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 7 7
Nets: 14 14
[VNC S...
[Terminal]
[virtuoso]
[What's ...
LSW
lvc_cnew
[Calibre...
Calibre l...
[lvc_cn...
LVS Rep...
Calibre ...

TABLE OF RESULTS:

Parameter	Pre-Layout Results
T_{pHL}	0.247ns
T_{pLH}	0.133ns
Propagation Delay	0.190ns
Rise Time	0.186ns
Fall Time	0.448ns
Power Consumption	0.299mW
Area	$0.023mm^2$

CONCLUSIONS:

We were able to design the circuit which completely met the required specifications with a very small propagation delay.

REFERENCES:

- Kang. S.M and Leblebici Y., “CMOS Digital Integrated Circuits: Analysis and Design, McGraw Hill.Electronic Design Automation Handbook, Dirk Jansen
- Rabaey Jan M. , Chandrakasan Anantha and Nikolic Borivoje, " Digital Integrated Circuits", Pearson Education.