NAMAN MAHESHWARI

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EDUCATION

Master of Science, Electrical and Computer Engineering (Integrated Circuits and Systems) **Class of 2021**
The University of Texas at Austin
Advisor: Dr. Nur Touba
Relevant Coursework: VLSI-1, Dependable Computing

Bachelor of Engineering (Hons.), Electrical and Electronics Engineering **May 2015**
Birla Institute of Technology and Science (BITS)-Pilani, Pilani Campus, India **CGPA: 9.31/10.00**

SKILL SET

Programming Languages: Verilog, VHDL, C, C++, JAVA, PERL, Assembly Language
Technical Software: Cadence Encounter Test, Cadence Incisive, Cadence Virtuoso, Xilinx Vivado, Synopsys Design Suite, MATLAB & Simulink, LT-Spice, Proteus, Code Composer Studio, Electric VLSI, Scilab

PROFESSIONAL EXPERIENCE

Digital Design Engineer, Design-for-Testability Team, Automotive-Radar chip Jul 2015 – Jul 2017
Texas Instruments, Bangalore, India

- Implemented the Built-In Self-Test (BIST) mechanism for memories for a complex design with 250+ memories
  - Implemented the architecture for memory testing during production as well as field testing
  - Verification of multiple fault-detection algorithms on all the memories in the design across multiple process corners, with high-security considerations and test-time optimization techniques like concurrent testing of memories
- Generated test patterns for advanced fault models like Small Delay Defect (SDD) & Path Delay, and measured the test quality by fault simulating across various fault models, thus improving test quality and optimizing pattern count
- Logic BIST and Automatic Test Pattern Generation (ATPG) for critical IPs in the design which are under the scope of Self-Test for automotive safety and implemented novel techniques like Low-Power Scan for scan-shift power reduction by 43%
- Invented and implemented a novel JTAG-based Hybrid Multiple Input Signature Register (H-MISR) which aids in seamless debug and diagnosis of MISR-based scan compression patterns without the need of exclusive long-chain mode

INTERNSHIPS

Digital Design Intern, Design-for-Testability Team, Automotive-Radar chip Jan 2015 – Jun 2015
Texas Instruments, Bangalore, India

- Designed and implemented Context Save Restore Mechanism to preserve the content of critical functional registers in the design during on-the fly test of IPs through self-test controller
- Built an automated infrastructure to create a ROM image containing patterns and golden MISR signatures for various operational modes for IPs under the scope of self-test, implemented based on On-Product MISR (OPMISR) codec with Low Power Scan Architecture. The flow also provides novel support of per cycle debug/diagnosis which does not exist with ATPG tool natively

Visiting Research Scholar, Department of Electrical and Computer Engineering May 2014 – Jul 2014
University of Alberta, Edmonton, Canada
Guide: Dr. Jie Han, Associate Professor, Dept. of Electrical and Computer Engg, University of Alberta

- Comparative Study of 16X16 approximate multipliers by implementing the designs in VHDL to calculate design metrics (power, delay and area) using Synopsys Design Suite, and in MATLAB to calculate accuracy metrics (error distance and error rate) by running Monte Carlo simulations
- Proposed novel 8X8 multiplier designs based on approximate 4:2 compressors which achieved an improvement of approximately 80% in terms of accuracy and 5% power reduction over the existing approximate compressor based designs

PATENT AND PUBLICATIONS

1. **Naman Maheshwari**, Wilson Pradeep and Prakash Narayanan, **"Novel Method and Apparatus for Per Cycle and Per Pattern MISR Debug and Diagnosis"**, filed at USPTO from Texas Instruments

2. **Naman Maheshwari**, Zhixi Yang, Jie Han and Fabrizio Lombardi, **"A Design Approach for Compressor Based Approximate Multipliers"**, Proceedings of 28th International Conference on VLSI Design, 2015 (**VLSID-2015**) [PDF]
   - Awarded the **Student Fellowship** by the Conference Committee, for excellent record in academics & past work

3. Wilson Pradeep, Prakash Narayanan, Rajesh Mittal, **Naman Maheshwari** and Nikita Naresh, **"Frequency Scaled Segmented (FSS) Scan Architecture for Optimized Scan-Shift Power and Faster Test Application Time"**, *accepted* in 48th IEEE International Test Conference, 2017 (**ITC-2017**)

4. Naman Maheshwari, Wilson Pradeep, Prakash Narayanan and Rajesh Mittal, **"Enhanced MISR Debug and Diagnosis with Per Cycle Scan Data Observation Capability"**, Proceedings of 19th Texas Instruments India Technical Conference, 2016 (**TIITC-2016**) [Acceptance Rate: 24%]

5. Honglan Jiang, Cong Liu, **Naman Maheshwari**, Fabrizio Lombardi and Jie Han, **"A Comparative Evaluation of Approximate Multipliers"**, Proceedings of 12th ACM/IEEE International Symposium on Nanoscale Architectures, 2016 (**NANOARCH-2016**) [PDF]

- Nominated for the **Best Paper Award** in the conference proceedings

6. Wilson Pradeep, Aravinda Acharya and **Naman Maheshwari**, **"Low Cost High-Performance Built-In Self-Test Solution using Cadence LBIST for Safety Critical SoCs"**, Proceedings of Cadence User Conference, 2017 (**CDNLIVE-2017**)

- Won the **Best Paper Award** in the conference proceedings

TEACHING EXPERIENCE

Teaching Assistant, The University of Texas at Austin Aug 2017 - Present

- Working as a T.A. for the course **EE 316 (Digital Logic Design)** and doing the development of the labs based on designing in Verilog and simulation on Basys FPGA board

Guest Talk, Vellore Institute of Technology, Vellore, India Aug 6, 2016

- Invited by Dr. S. Balamurugan to give a guest lecture on "**Design of Approximate Arithmetic Circuits and their real-time applications**" where I presented my work on the design of approximate multipliers and their use in image processing

Professional/Teaching Assistant, BITS-Pilani, India Aug 2013 – Dec 2014

- Worked as a T.A. for various courses like **Microprocessors Programming & Interfacing**, **Analog & Digital VLSI Design**, **Microelectronic Circuits** and **Signals & Systems** and helped students in learning software like Proteus, Cadence Virtuoso, LT-Spice and MATLAB

ACADEMIC PROJECTS

Implementation of 16x16 Compressor Based Approximate Multipliers Aug 2014 – Dec 2014

- Proposed and implemented compressor based 16x16 approximate multipliers using the technique of recursive multiplication in VHDL and MATLAB, which achieve approximately 50% reduction in power and 20% reduction in circuit area over the accurate compressor based design

Building a Virtual Lab Aug 2014 – Dec 2014

- Built a Virtual Lab on open source software like Electric VLSI and Scilab for Work Integrated Learning Program (WILP) students of BITS-Pilani

Operational Amplifier Design Aug 2013 – Dec 2013

- Designed & simulated a two-stage folded cascode op-amp and met challenging specifications of gain, bandwidth and phase margin on Cadence Virtuoso ADE and Spectre Circuit Simulator

3-input AND/NAND Gate Design Aug 2013 – Dec 2013

- Designed a 3-input AND/NAND gate using pass transistor logic to achieve desired functionality and prepared its layout on Cadence Virtuoso Layout Suite, thus gaining an experience on how the circuits are fabricated

ACHIEVEMENTS

MITACS Globalink Scholar
Selected among 470 fellows for MITACS Globalink Fellowship 2014 from 8000+ applicants from the top universities of the world for a summer research-assistantship in Canada

Microsoft Code.Fun.Do.
Developed a Kinect application V-Braille for enabling blind people to type and won the Code.Fun.Do. competition organized by Microsoft in BITS-Pilani

Best Design Prize
Learnt the complete RTL Design to GDSII flow for an SoC and won the Best Design Prize for designing an optimized transceiver in two Digital Design boot-camps held as part of TI's Make-an-Impact program for New College Graduates