

# A Comparison of Approximate Multipliers for Error-Resilient Applications

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## Introduction

- Approximate or Inexact Computing has gained a significant attention for error tolerant applications such as image and signal processing.
- In such applications, perfectly accurate results are not required and hence, accuracy can be traded with power, area and delay.
- A multiplier is a fundamental component in such applications and hence, the choice of the design of the multiplier is an important aspect of approximate computing.
- The study and MATLAB & VHDL implementations of various already proposed designs is carried out to compare the designs on the basis of error metrics (Error Distance and Error Rate) and circuit metrics (power, delay and area) and hence, helping in the choice of the multiplier to be used according to the application.

- i. Literature survey of the approximate multipliers
- ii. MATLAB and VHDL implementations of the designs
- iii. Comparison of design and circuit metrics

Figure 1: Methodology Involved

## Wallace Tree Multiplier

- All the multipliers implemented are 16X16 and comparisons have been made with an accurate multiplier of the same size implemented with a technique called Wallace Tree.
- An accurate Wallace Tree multiplier involves 3 steps as shown in the figure below.

- i. Generation of partial products
- ii. Using full and half adders for partial product reduction
- iii. Adding the 2 lines using a conventional adder

Figure 2: Implementation of a Wallace Tree Multiplier

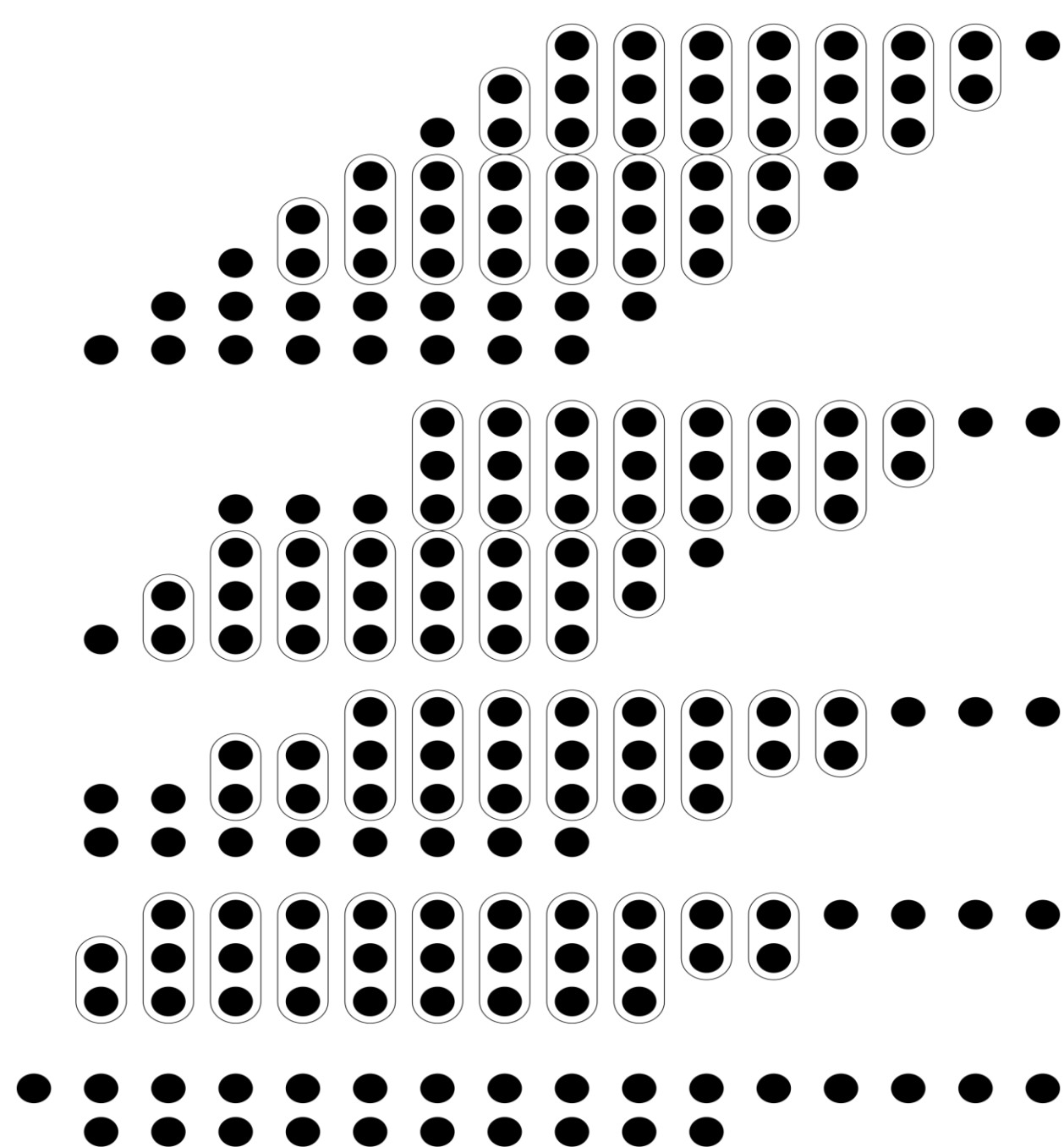


Figure 3: Partial Product Reduction using Wallace Tree

## Multipliers Implemented

- [1] describes an Error Tolerant Multiplier (ETM) which uses accuracy as the design parameter.
- [2] presents a 2X2 Underdesigned Multiplier (UDM) block and uses it to build large power efficient approximate multipliers.
- [3] describes a Broken Array Multiplier (BAM) which involves faster and approximate implementation of the Array Multiplier.
- [4] proposes a Broken Booth Multiplier (BBM) which utilizes BAM approximation method on the conventional Booth Multiplier.
- [5] presents an Imprecise Compressor Multiplier (ICM) which uses an inaccurate 4:2 counter to reduce the partial product stages of the Wallace Tree Multiplier.
- [6] presents an Approximate Wallace Tree Multiplier (AWTM) which uses a carry prediction method to calculate the product faster.
- [7] proposes an approximate adder which is used in partial product reduction and hence, increases the speed of multiplication in Approximate Multiplier (AM).

## Simulation Results

- Monte Carlo Simulations were run for all the multipliers on MATLAB for the calculation of error metrics (Normalized Mean Error Distance, Mean Relative Error Distance and Error Rate) and the results are shown in the table below.

Parameter	NMED (%)	MRED (%)	ER (%)
ETM			
Parameter : No. of LSBs as Inaccurate Part			
7	0.097	1.56	99.99
8	0.194	2.85	100.00
UDM			
Parameter : No Configurable Parameter			
N/A	1.392	3.33	80.99
BAM			
Parameter : Vertical Broken Length			
16	0.006	0.21	99.99
18	0.022	0.63	99.99
20	0.079	1.79	100.00
22	0.268	4.75	100.00
BBM			
Parameter : No. of Truncated Bits			
9	0.000	0.01	98.94
15	0.008	0.6	99.98
ICM			
Parameter : No Configurable Parameter			
N/A	0.029	0.06	5.45
AWTM (Inputs ≠ 0)			
Parameter : Mode No.			
1	0.270	75.00	100.00
2	0.188	39.37	100.00
3	0.012	2.51	99.99
4	0.002	0.33	99.94
AM			
Parameter : No. of MSBs for Error Reduction			
13	0.112	0.69	99.40
15	0.106	0.54	98.89

Table 1: Comparison of Error Metrics of different multipliers

- For computing the circuit metrics, the multipliers were coded on VHDL and then simulated on Synopsys Design Vision based on TSMC 65 nm process to get the Power, Delay and Area. The results are shown in the table below.

Parameter	Delay (ns)	Area (μm <sup>2</sup> )	Power (mW)
ETM			
Parameter : No. of LSBs as Inaccurate Part			
7	1.48	1084	0.49
8	1.51	1126	0.46
UDM			
Parameter : No Configurable Parameter			
N/A	1.97	3099	1.85
BAM			
Parameter : Vertical Broken Length			
16	2.63	1679	0.97
18	2.31	1325	0.70
20	1.92	1023	0.47
22	1.53	780	0.29
BBM			
Parameter : No. of Truncated Bits			
9	3.38	3759	2.39
15	2.90	2821	1.69
ICM			
Parameter : No Configurable Parameter			
N/A	2.06	3462	1.74
AWTM (Inputs ≠ 0)			
Parameter : Mode No.			
1	1.94	2417	1.09
2	1.94	2510	1.13
3	1.94	2603	1.18
4	1.99	2595	1.21
AM			
Parameter : No. of MSBs for Error Reduction			
13	0.88	2812	1.06
15	1.32	2873	1.09

Table 2: Comparison of Circuit Metrics of different multipliers

## Conclusions

- Various approximate multipliers are compared on the basis of accuracy, power, delay and area.
- Among these multipliers, UDM has the highest NMED while BBM has the lowest and hence, BBM can be chosen in the applications requiring high accuracy but only at the cost of more delay, power and area.
- Further, AM has the lowest delay and BAM has the lowest power and area at the cost of less accuracy and these can be used in error-tolerant, low-power and high-speed applications.
- The best application specific multiplier can be chosen according to the requirement of the application by looking at the results.
- Further, multipliers based on Approximate Compressor designs will be included in the comparison which can also prove to be useful in various applications.

## References

[1] Kyaw, K. Y., Goh, W. L., & Yeo, K. S. (2010). Low-power high-speed multiplier for error-tolerant application. In 2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC).  
[2] Kulkarni, P., Gupta, P., & Ercegovic, M. (2011). Trading Accuracy for Power with an Underdesigned Multiplier Architecture. In 2011 24th International Conference on VLSI Design  
[3] Mahdiani, H. R., Ahmadi, A., Fakhraie, S. M., & Lucas, C. (2010). Bio-Inspired Imprecise Computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications. IEEE Transactions on Circuits and Systems  
[4] Farshchi, F., Abrishami, M. S., & Fakhraie, S. M. (2013). New approximate multiplier for low power digital signal processing. In The 17th CSI International Symposium on Computer Architecture & Digital Systems (CADSD 2013)  
[5] Lin, C., & Lin, I. (2013). High accuracy approximate multiplier with error correction. Computer Design (ICCD), 2013 IEEE 31st ..., 33–38.  
[6] Bhardwaj, K., Mane, P. S., & Henkel, J. (2014). Power- and area-efficient Approximate Wallace Tree Multiplier for error-resilient systems. In Fifteenth International Symposium on Quality Electronic Design (pp. 263–269). IEEE.  
[7] Cong Liu, Jie Han and Fabrizio Lombardi, A Low-Power, High-Performance Approximate Multiplier with Configurable Partial Error Recovery. *Design, Automation & Test in Europe Conference (DATE 2014)*, Dresten, Germany, March 24 - 28, 2014.