[FED08]

Low Cost High Performance Built-In Self-Test Solution Using Cadence LBIST for Safety Critical SoCs

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Outline

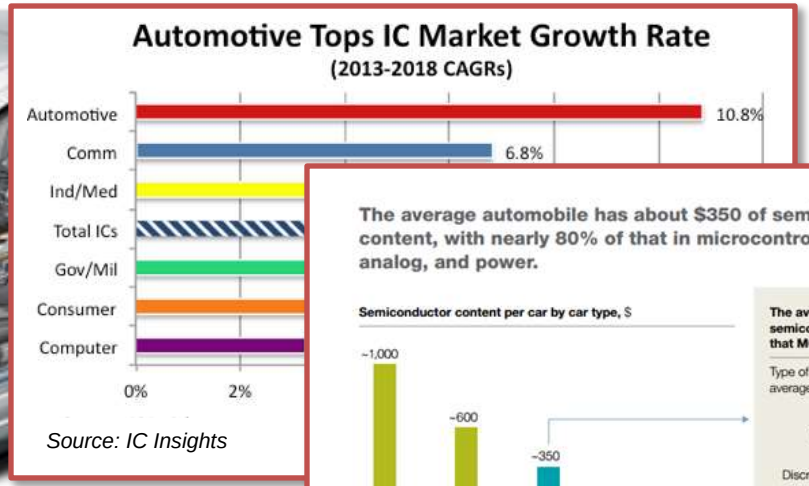
- Test Requirement in Safety Critical Automotive SoCs
- Comparison of Conventional Methods
- Overview of Cadence LBIST Solution
- Proposed Optimizations for LBIST QoR Improvements
- Results
- Conclusion

Automotive Market

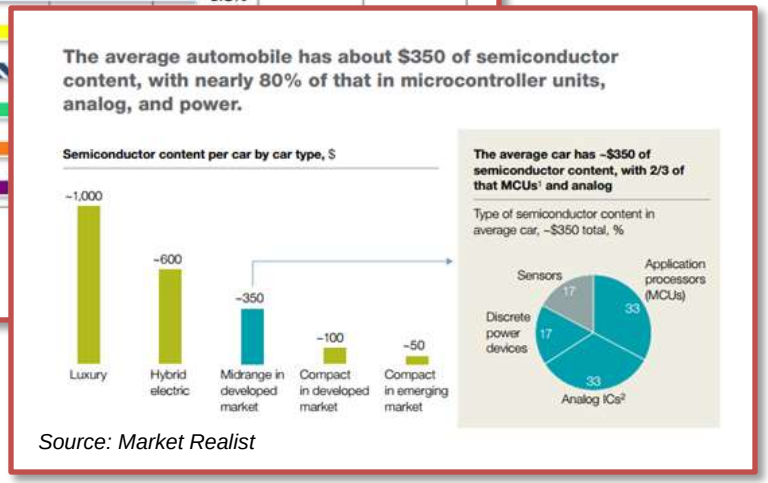
Automotive Market: Sales $21B – 2015 → $29B – 2019.

ADAS fastest growing automotive application. 25% CAGR 14-21. ($1B demand for ADAS proc.)

Source: behance.net

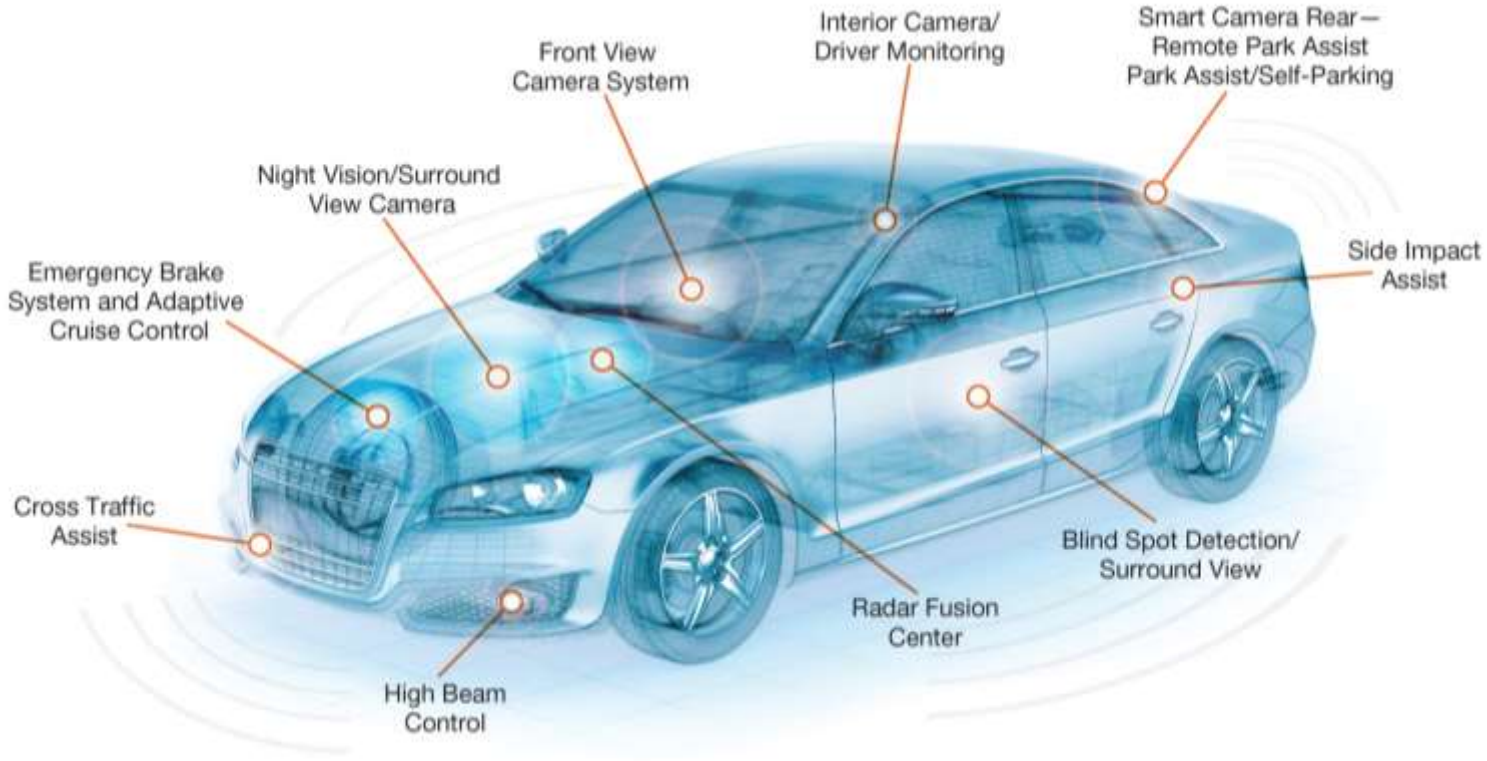


Source: IC Insights



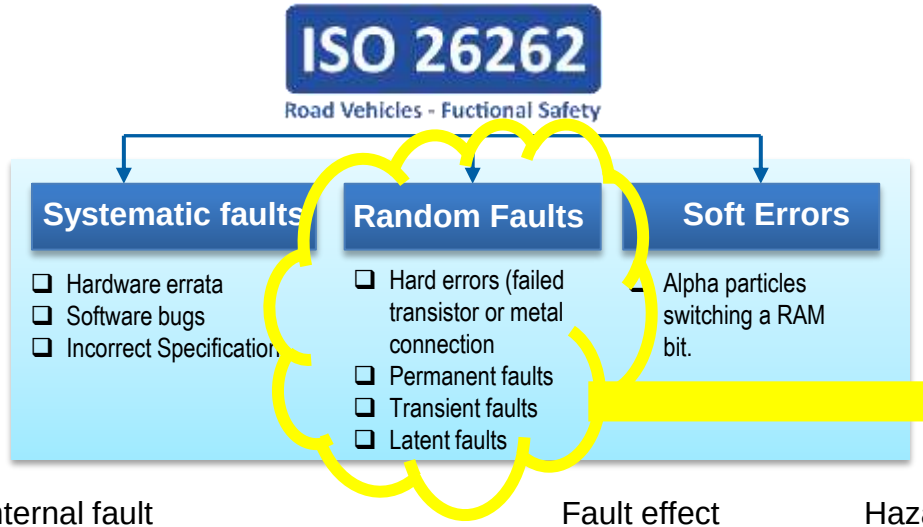
Source: Market Realist

Automotive Electrification



Source: johndayautomotivelectronics.com

Automotive Functional Safety

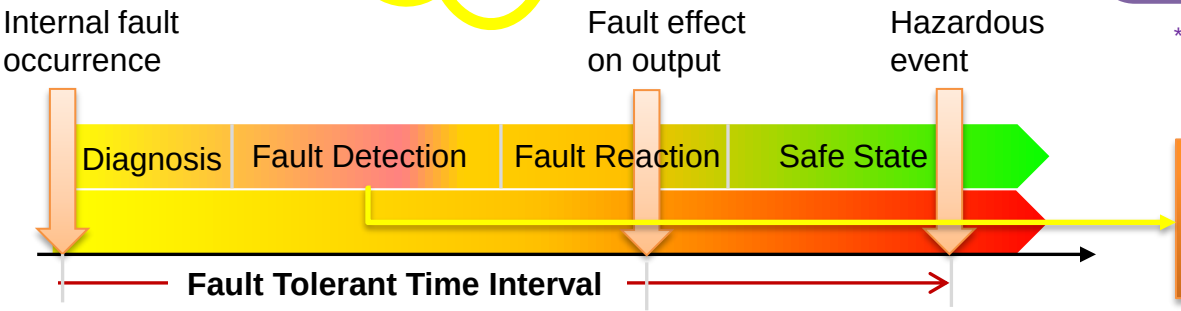


Safety	SPFM	LFM
QM	Design Assurance	
ASIL A	Nominal	
ASIL B	90%	60%
ASIL C	97%	80%
ASIL D	99%	90%

Permanent Faults

Transient Faults*

** Expect to extend to ASIL B post 2018*



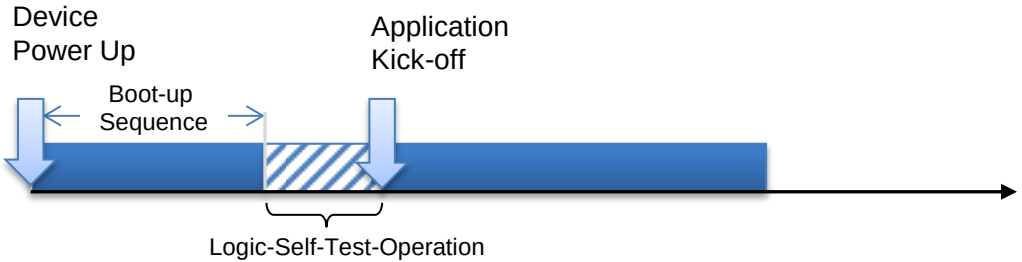
Design Hardware Mechanism

Logic Self-Test | Memory Self-Test

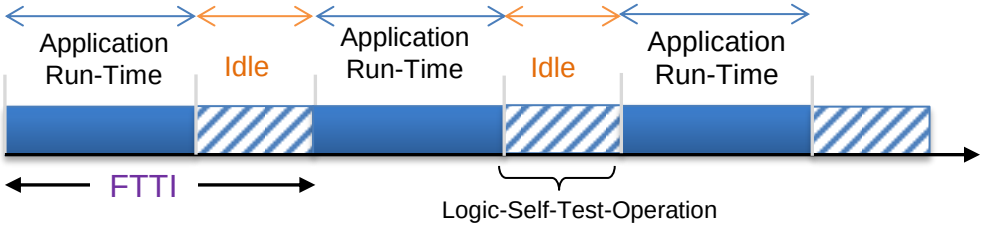
ECC

Logic Self-Test Requirements

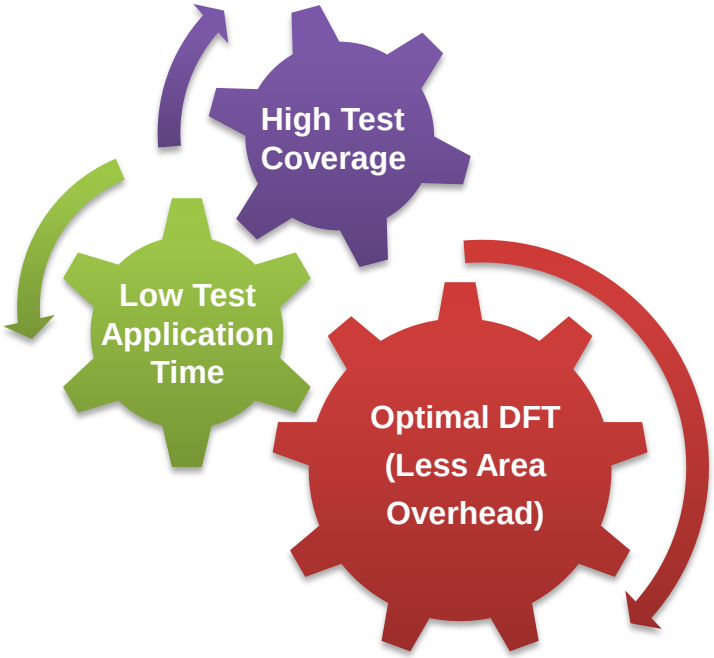
Power-On Self-Test



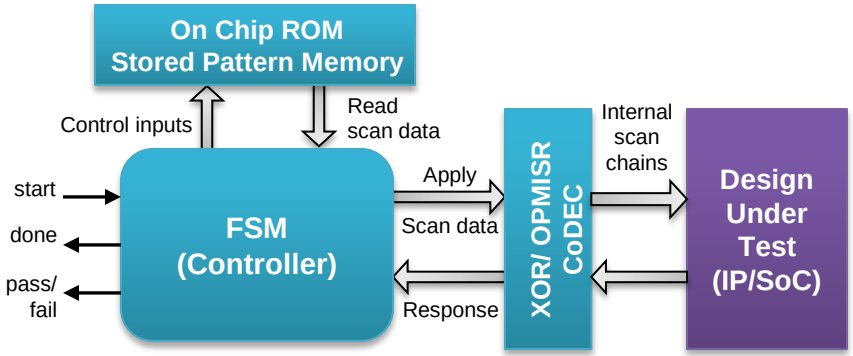
In-Field Self-Test



Test Requirements



Conventional Logic Self-Test Solutions

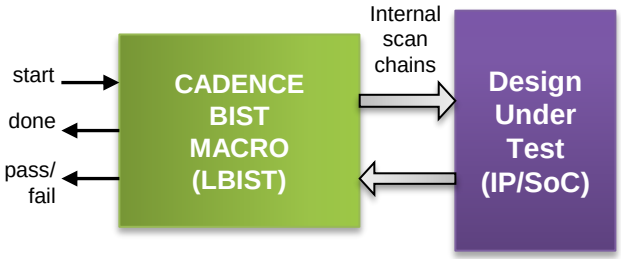


Stored Test Pattern Method

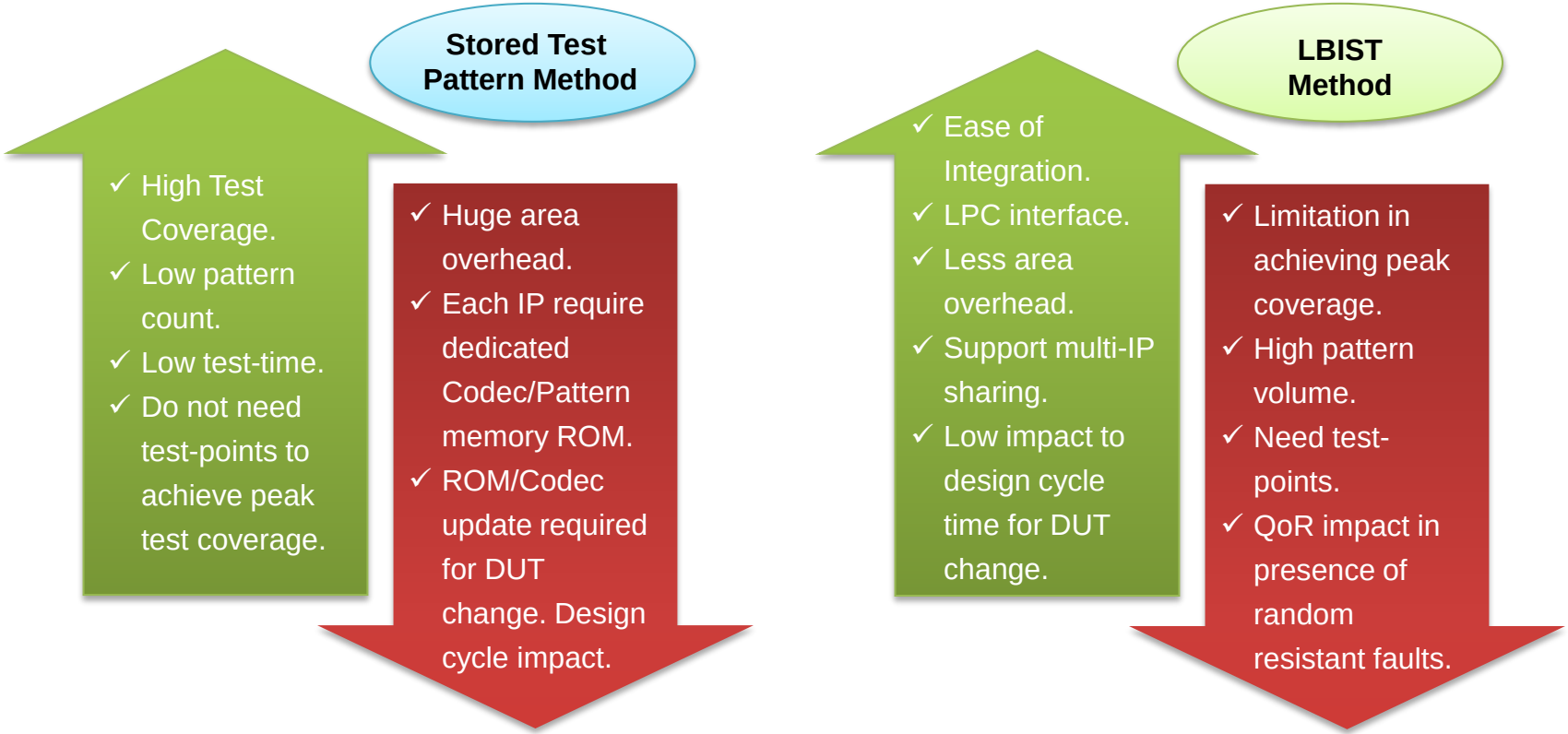
- Deterministic ATPG
- Patterns stored in on-chip memory
- Uses conventional XoR/OPMISR CoDec
- Pattern application & response analysis done using custom controller

LBIST Method

- Random ATPG
- Patterns generated using pseudo random pattern generator (PRPG)
- Final signature compared against expected using BIST macro.

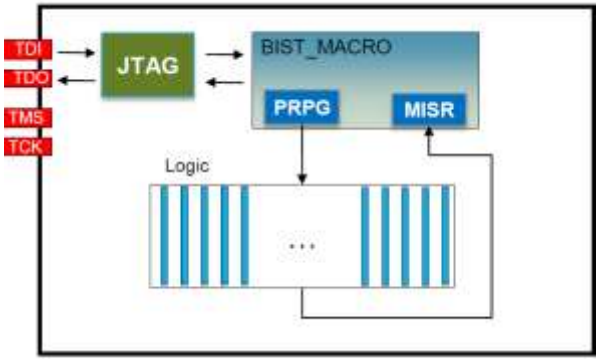


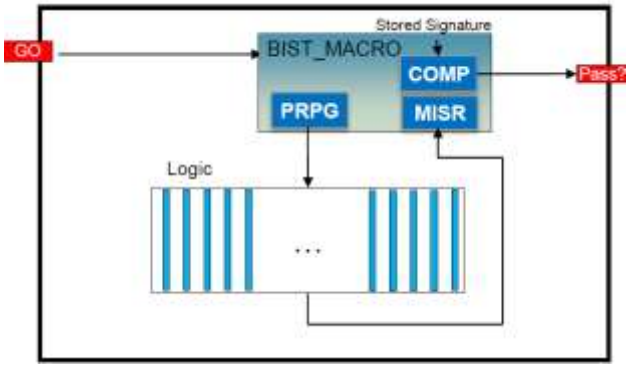
Pros & Cons


Stored Test Pattern Method
✓ High Test Coverage.
✓ Low pattern count.
✓ Low test-time.
✓ Do not need test-points to achieve peak test coverage.
✓ Huge area overhead.
✓ Each IP require dedicated Codec/Pattern memory ROM.
✓ ROM/Codec update required for DUT change. Design cycle impact.
LBIST Method
✓ Ease of Integration.
✓ LPC interface.
✓ Less area overhead.
✓ Support multi-IP sharing.
✓ Low impact to design cycle time for DUT change.
✓ Limitation in achieving peak coverage.
✓ High pattern volume.
✓ Need test-points.
✓ QoR impact in presence of random resistant faults.

Overview of Cadence LBIST

- Cadence mainly supports two type of LBIST configuration
  - ❑ **JTAG LBIST** (Controlled through JTAG, Signatures read & Compared using TDO, Option for PRPG Reseeding, Configurable parameters)
  - ❑ **Direct Access LBIST** (triggered through pin, Signatures are compared with stored internal values, Non-Configurable).
- Additionally it provides following features:
  - ❑ Multiple clock output (to support multi-clock (asynchronous) domain designs
  - ❑ Clock staggering to enable Low-power scan.
  - ❑ Internal clock gen/control logic with ability to generate custom clock waveforms.
  - ❑ Support asynchronous set/rest clocking to gain set/reset line coverage



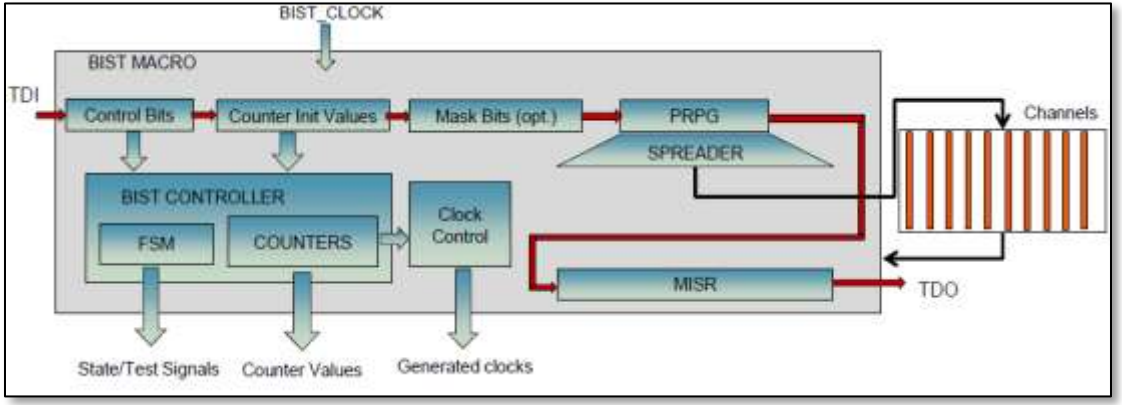


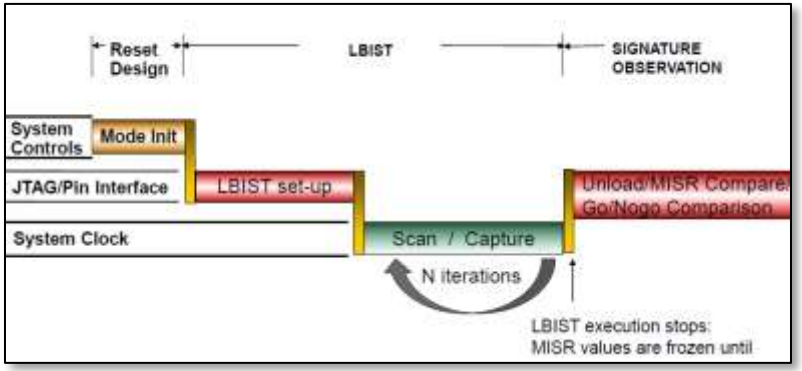
Source: Cadence.com

Overview of Cadence LBIST

BIST MACRO contains :

- State Machine
- PRPG (Pseudo-Random Pattern Generator) and MISR (Multiple-Input Shift Register)
- Spreader logic
- Mask Bits – Used to disable channels during LBIST (Optional hardware)
- Clock Generation logic
- JTAG TDR is shown in red (TDI->TDO). Bits are fixed values for Direct Access LBIST.





Source: Cadence.com

Need for Optimized LBIST Solution

Design: IP-A	
Technology	45nm
Gate Count	>1 M
Flip-Flop Count	~50K
Stump Size	64
Stump Count	804

	Coverage Peak		Coverage =90%		
Mode	**Test Coverage**	**Pattern Count**	**Pattern Count**	**Test Cycles**	**Normalized Area**
STP (XoR + OPMISR)	94.97%	2320	240	15360	9.91
Default LBIST	90.58%	20.2K	6109	390976	1
Delta	**- 4.39 %**	**↑ 8.71X**	**↑ 25.45X**		**- 90%**

Primary Objectives

Improve Test-Coverage

Optimize pattern Volume

- In comparison to STP, LBIST is much simpler solution due to following factors-
  - ❑ Ease of integration and ability to scale with design.
  - ❑ Ability to share single LBIST for multiple cores.
  - ❑ Does not require macro regeneration for any change in DUT (Design Under Test).
  - ❑ Significant area savings (80-90% less compared to STP method).
- Major concern with its adoptability in native form – Low test coverage and Huge pattern volume inflation

Proposed Optimizations

Propose following enhancements to native **Cadence LBIST** to

a) Improve performance and QoR

b) Achieving desired coverage goal target with minimal test-cost impact.

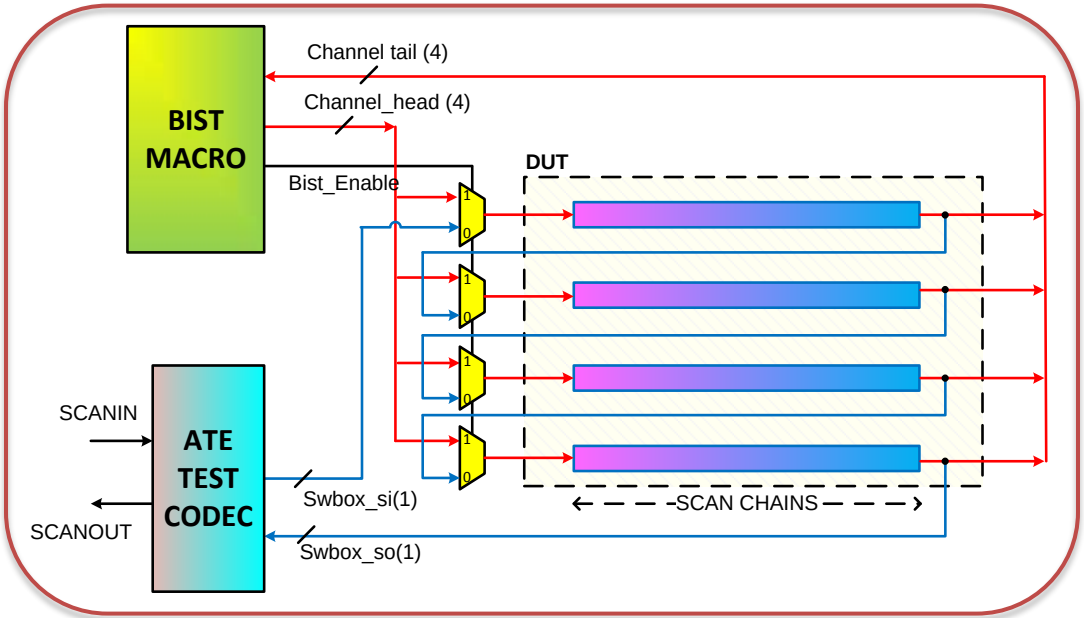
1. Target higher scan compression ratio
2. Optimized test-point insertion
3. Recurring capture mode test
4. Staggered + recurring capture for multi-clock domain design

- Proposed solutions largely make use of the various customizable options available with Cadence LBIST macro (generated using Genus 16.2) - Programmable counters, Multiple clock outputs, Clock staggering, etc.
- **Key benefits :**
  - Does not incur huge area overhead – require only few gates in addition to existing BIST_MACRO.
  - Easily supported by Cadence ET/Modus tool.

Optimization Method #1:

Target Higher Scan Compression Ratio

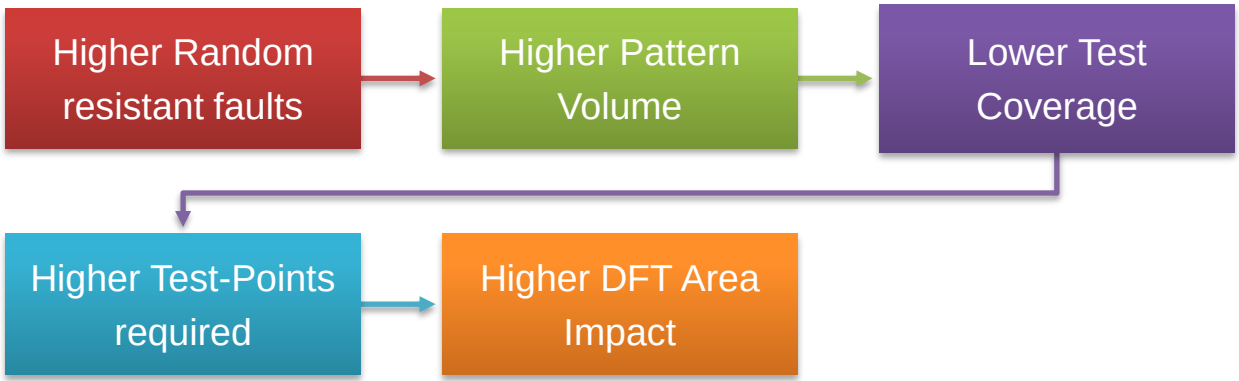
- Higher scan compression ratio → Higher test compaction.
- In Deterministic ATPG - maximum compression ratio is limited due to pattern count inflation as an effect of higher correlation.
- In Random ATPG – Compression ratio has little to no impact on pattern volume.
- Hence making chains shorter (higher compression ratio) for LBIST ; help in achieve faster run-time.



- Scan chains are constructed to operate in dual scan configuration mode
  - Production mode (test via ATE) – 1x compression ratio
  - Logic self-test mode (test via CDN LBIST) – 2x/4x/8x compression ratio.

Optimization Method #2:

Low cost test-point insertion



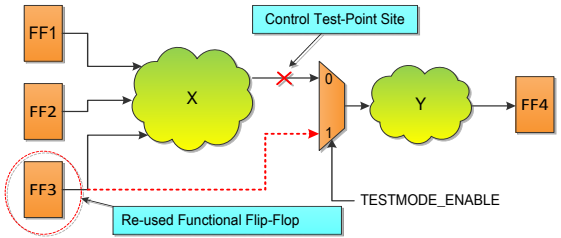
- In most designs, it is almost impossible to achieve peak test-coverage without use of test-points.
- Test-point insertion comes with additional area overhead – Hence need to insert optimal test-points to meet desired coverage & pattern count goals.

Custom Enhancement #2:

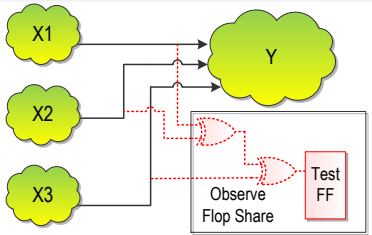
Low Cost Test-Point Insertion

Area Overhead Optimization Methods

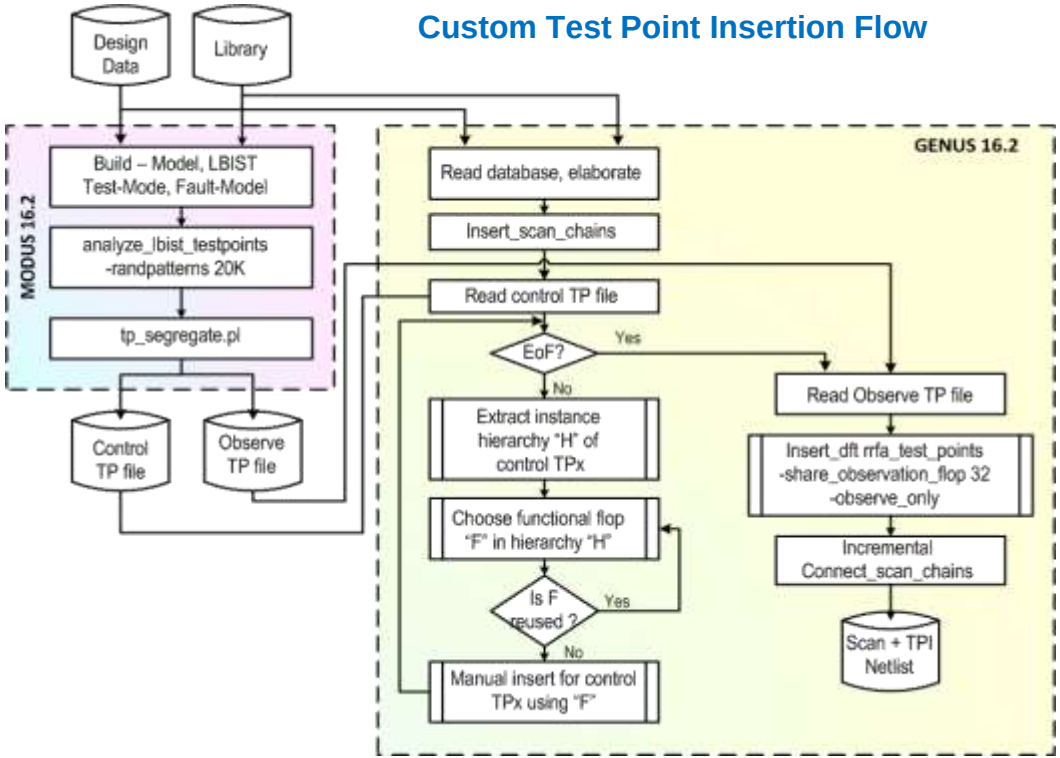
Reuse localized functional flip-flop for control points { Custom Method }



Share single test flip-flop for multiple observe test-points { Through Tool Option }

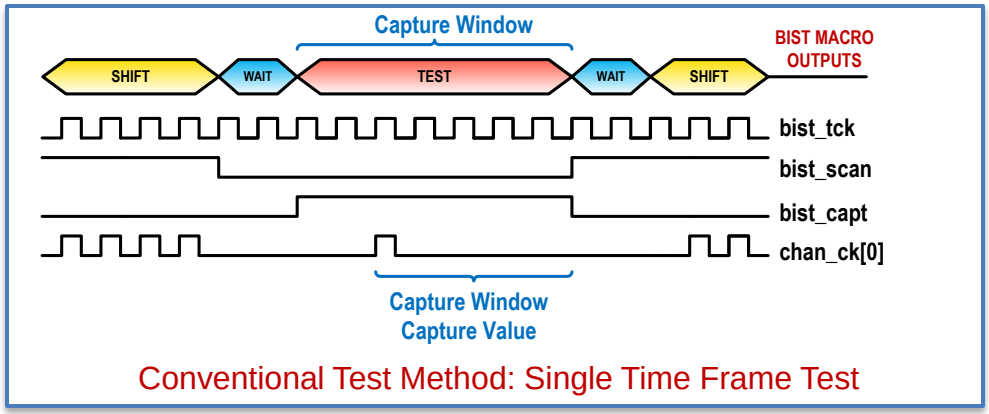


Custom Test Point Insertion Flow

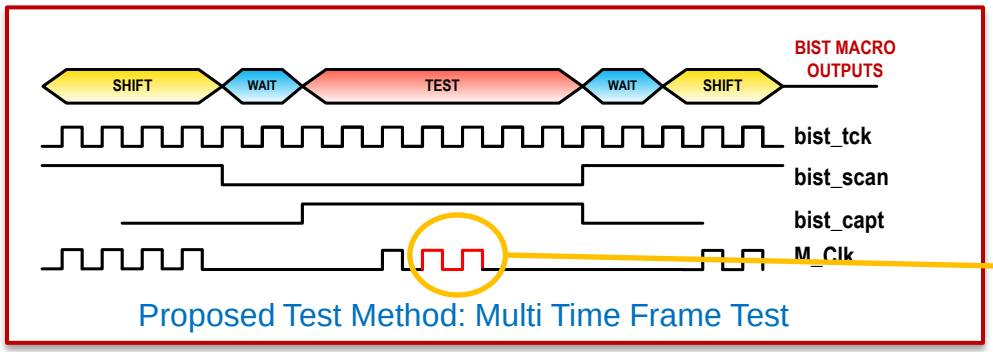


Custom Enhancement #3:

Recurring Capture Mode (RCM) Test



Conventional Test Method: Single Time Frame Test



Proposed Test Method: Multi Time Frame Test

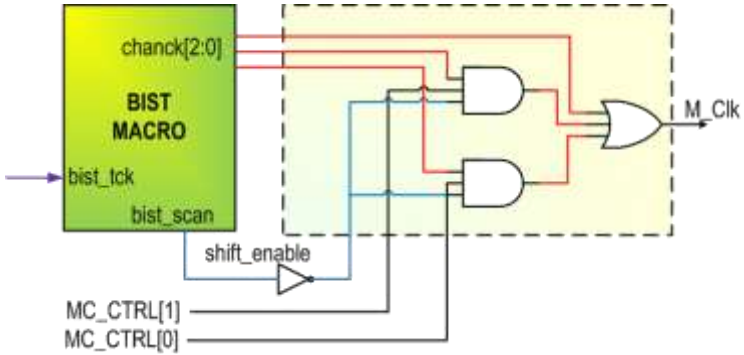
- Limitation of Conventional Method: Complete scan load sequence is required to create per unique random pattern.
- Proposed Method : RCM - Multiple recurring capture pulses (multi-time frame test) are enabled per scan load sequence.
- Advantage: Multiple unique random patterns created per scan load by virtue of multiple capture events.
- Enables significant pattern volume optimization.

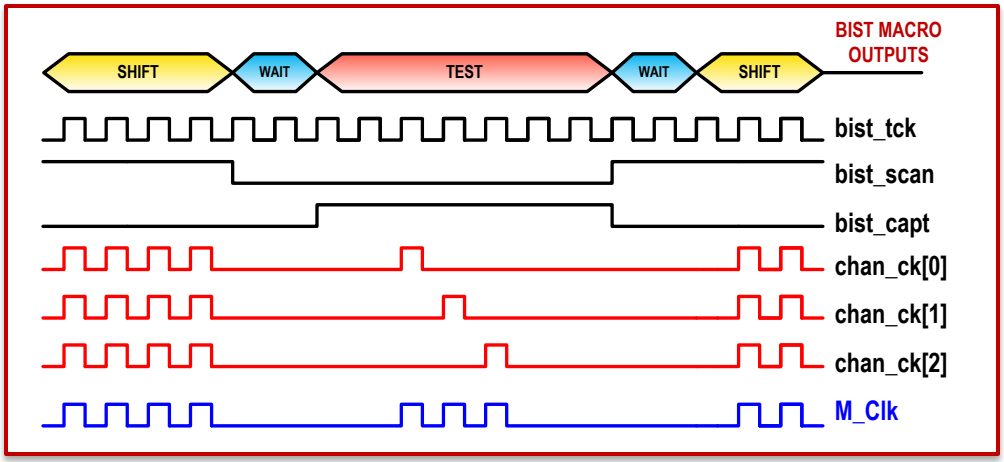
Custom Enhancement #3:

Recurring Capture Mode (RCM) Test

- Uses multi-clock output and clock stagger features of default BIST_MACRO
- Custom clock merge circuit is used to generate merged clock (M_Clk)

```
write_dft_lbist_macro
-clocks 3
-capture_clock_stagger_ratio 1
-scan_clock_stagger_ratio 0
```

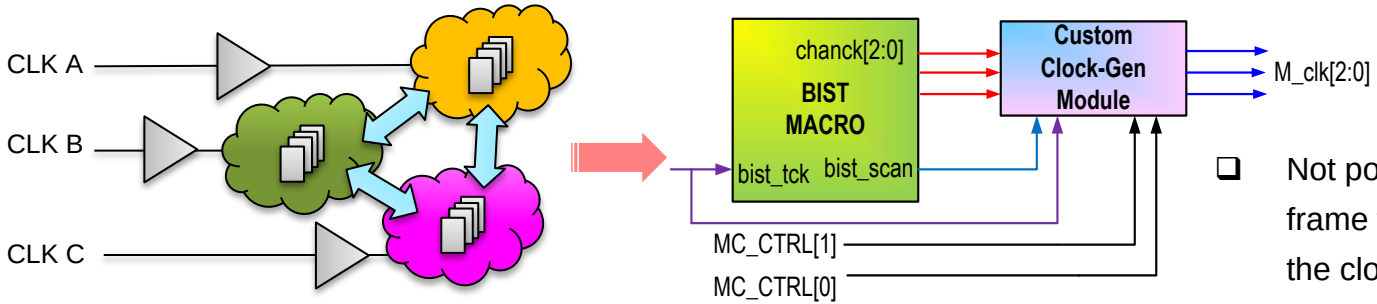


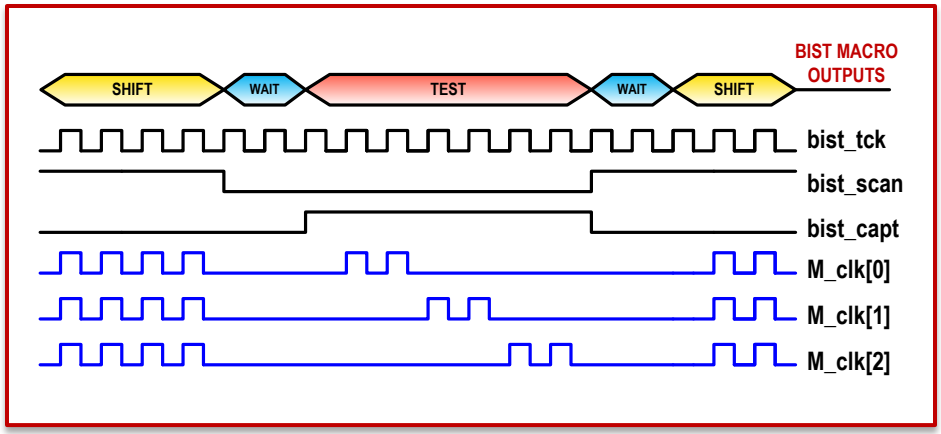


Option	MC_ CTRL[1]	MC_ CTRL[0]	M_Clk
Shift	X	X	Chanck[0]
Single Static Pulse	0	0	Chanck[0]
RCM w/ 2 capture pulse	1	0	Chanck[0] || Chanck[1]
RCM w/ 3 capture pulse	1	1	Chanck[0] || Chanck[1] || Chanck[2]

Custom Enhancement #4:

Staggered + RCM (multi-clock domain design)





- Not possible to perform single time frame test with edge aligned capture as the clocks for different domains are asynchronous.
- To mitigate, reuse clock staggering feature of BIST_MACRO to generate multiple phase shifted capture clocks.
- To further improve test-efficiency RCM test method is overlaid.
- Circuit also provides flexibility to control number of recurring capture clock pulses per clock domain.

Results

- Experiments were performed on the below two designs.

Design: IP-A	
Technology	45nm
Gate Count	>1 M
Flip-Flop Count	~50K
Stump Size	64
Stump Count	804

Design: SoC-A	
Technology	45nm
Gate Count	>50 M
Flip-Flop Count	~750K
Stump Size	256
Stump Count	1880

For comparison, following experiments were performed on each design

- **Stored test-pattern method** using regular OPMISR based codec.
- **Default LBIST** –Cadence LBIST in its native form by re-using existing scan-chains.
- **Optimized LBIST** – Cadence LBIST with custom enhancements.

- Coverage Target: > 90%
- LBIST used: Direct Access Mode
- Tools used:
  - Cadence Genus (v16.2) - Generation and insertion of BIST_MACRO, scan-insertion, test-point insertion and addition of custom clock generation logic.
  - Cadence Modus (v16.2) – RRFA test-point analysis and ATPG.

Results [IP- A]

Optimized LBIST vs Default LBIST: ~260X test-time reduction for 90% target coverage

Optimized LBIST vs STP: ~3X test-time reduction for 90% target coverage

Stored Test Pattern Method

Mode	Stump Size	Compression Ratio	Test-points	Test Coverage	Pattern Count (Cov=90%)	Test Cycles
Default	64	1X	NA	94.97	240	15360
TPI	64	1X	750	95.08	144	9216
TPI + 4X CR	16	4X	750	95.08	286	4576

LBIST Method

Mode	Stump Size	Compression Ratio	Test-points	Test Coverage	Pattern Count (Cov=90%)	Test Cycles	Comparison w/ Default LBIST	Comparison w/ Eq. XOR Config
Default	64	1X	NA	90.58%	6109	390976	-	25.45 X ↑
Low Cost TPI	64	1X	750	94.95%	324	20736	18.85 X ↓	2.25 X ↑
TPI + 4X CR	16	4X	750	94.88%	349	5584	70.02 X ↓	1.22 X ↑
TPI + 4X CR + RCM=3 (Optimized LBIST)	**16**	**4X**	**750**	**95.05%**	**94**	**1504**	259.96 X ↓	3.04 X ↓

Results [SoC- A]

LBIST Method

Mode	Stump Size	Compression Ratio	Test-points	Pattern Count (Cov=80%)	Test Cycles	Comparison w/ Default LBIST
Default	248	1X	NA	10048	2411520	-
Low Cost TPI	248	1X	4K	5696	1367040	**1.76 X ↓**
TPI + 2X CR	128	2X	4K	5632	720896	**3.35 X ↓**
TPI + 2X CR + RCM=3 (Optimized LBIST)	128	2X	4K	576	73728	**32.71 X ↓**

Optimized LBIST vs Default LBIST: ~32X test-time reduction for 80% target coverage

Conclusion

- LBIST is one of the most commonly method used to perform Logic self-test operation on safety critical automotive devices.
- Although it provides significant area savings compared to stored test-pattern method (80-90%), it's usage in default form suffers significantly with poor test-coverage and high pattern volume inflation.
- Four custom enhancement to native Cadence LBIST with minimal DFT area overhead is proposed.
- Proposed solutions largely make use of the various customizable options available with Cadence LBIST.
- Results from a 50K flip-flop IP indicate, customized LBIST solution ~260x test-time reduction compared to native LBIST for 90% target coverage.
- In comparison to equivalent configuration of stored test-pattern method, it is observed to give ~3x test-time reduction.

Thank You.