NAMAN MAHESHWARI

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RESEARCH INTERESTS

Digital VLSI Design & Test, Low-Power Computing and Emerging Computing Models, System-on-Chip Design

EDUCATION

Bachelor of Engineering (Hons.) 2011-2015
Electrical and Electronics Engineering **CGPA: 9.31/10.00**
Birla Institute of Technology and Science (BITS)-Pilani, Pilani Campus, India

- Among the top 10 students in Electrical, Electronics & Instrumentation Departments in a batch of 150 students
- Overall amongst top 5% students in BITS-Pilani

PROFESSIONAL EXPERIENCE

Texas Instruments, Bangalore, India Jul 2015 – Present
Digital Design Engineer, Design-for-Testability Team, Automotive-Radar CMOS chip
Guide: Mr. Prakash Narayanan, DFT Lead, Automotive-Radar, Texas Instruments, India

- Implemented the Built-In Self-Test (BIST) mechanism for memories for a complex design with 250+ memories
  - Implemented the architecture for memory testing during production as well as field testing
  - Verification of multiple fault-detection algorithms on all the memories in the design across multiple process corners, with high-security considerations and test-time optimization techniques like concurrent testing of memories
- Generated test patterns for advanced fault models like Small Delay Defect (SDD) & Path Delay, and measured the test quality by fault simulating across various fault models, thus improving test quality and optimizing pattern count
- Automatic Test Pattern Generation (ATPG) for critical IPs in the design which are under the scope of Self-Test for automotive safety and implemented novel techniques like Low-Power Scan for scan-shift power reduction by 43%
- Invented and implemented a novel JTAG-based Hybrid Multiple Input Signature Register (H-MISR) which aids in seamless debug and diagnosis of MISR-based scan compression patterns without the need of exclusive long-chain mode

INTERNSHIPS

Texas Instruments, Bangalore, India Jan 2015 – Jun 2015
Digital Design Intern, Design-for-Testability Team, Automotive-Radar CMOS chip
Guide: Mr. Rajesh Mittal, DFT Lead, Wireless Connectivity Solutions, Texas Instruments, India

- Designed and implemented Context Save Restore Mechanism to preserve the content of critical functional registers in the design during on-the fly test of IPs through self-test controller
- Built an automated infrastructure to create a ROM image containing patterns and golden MISR signatures for various operational modes for IPs under the scope of self-test, implemented based on On-Product MISR (OPMISR) codec with Low Power Scan Architecture. The flow also provides novel support of per cycle debug/diagnosis capability which does not exist with ATPG tool natively

University of Alberta, Edmonton, Canada May 2014 – Jul 2014
Visiting Research Scholar, Department of Electrical and Computer Engineering
Guide: Dr. Jie Han, Associate Professor, Dept. of Electrical and Computer Engg, University of Alberta

- Comparative Study of 16X16 approximate multipliers by implementing the designs in VHDL to calculate design metrics (power, delay and area) using Synopsys Design Suite, and in MATLAB to calculate accuracy metrics (error distance and error rate) by running Monte Carlo simulations
- Proposed novel 8X8 multiplier designs based on approximate 4:2 compressors which achieved an improvement of approximately 80% in terms of accuracy and 5% power reduction over the existing approximate compressor based designs

PATENT

Naman Maheshwari, Wilson Pradeep and Prakash Narayanan, **"Novel Method and Apparatus for Per Cycle and Per Pattern MISR Debug and Diagnosis"**, approved for filing at USPTO from Texas Instruments

- Invented a JTAG-based Hybrid MISR Implementation to solve the problem of debug in case of failing MISR-based scan compression patterns
- Various key features of the invention are –
  - Enables per pattern and per cycle signature observation without test-time and test-volume impact
  - Existing Test Data Out (TDO) pin is used for MISR-Observe, avoiding the need for exclusive test-pin
  - Does not require additional long-chain diagnostic test-mode and enables continue-on-fail in the event of failures

PUBLICATIONS

1. Naman Maheshwari, Zhixi Yang, Jie Han and Fabrizio Lombardi, **"A Design Approach for Compressor Based Approximate Multipliers"**, Proceedings of 28th International Conference on VLSI Design, 2015 (**VLSID-2015**) [PDF]

- Awarded the **Student Fellowship** by the Conference Committee, for excellent record in academics & past work

2. Naman Maheshwari, Wilson Pradeep, Prakash Narayanan and Rajesh Mittal, **"Enhanced MISR Debug and Diagnosis with Per Cycle Scan Data Observation Capability"**, Proceedings of 19th Texas Instruments India Technical Conference, 2016 (**TIITC-2016**) [Acceptance Rate: 24%]

3. Honglan Jiang, Cong Liu, **Naman Maheshwari**, Fabrizio Lombardi and Jie Han, **"A Comparative Evaluation of Approximate Multipliers"**, Proceedings of 12th ACM/IEEE International Symposium on Nanoscale Architectures, 2016 (**NANOARCH-2016**) [PDF]

- Nominated for the **Best Paper Award** in the conference proceedings

4. Naman Maheshwari, Wilson Pradeep and Prakash Narayanan, **"Novel Debug and Diagnosis Method for MISR based Scan Compression Architecture"**, *submitted* to 35th IEEE VLSI Test Symposium, 2017 (**VTS-2017**)

5. Naman Maheshwari, Cong Liu, Honglan Jiang and Jie Han, **"A Comparison of Approximate Multipliers for Error Resilient Applications"**, presented this poster in a Consortium held for the internship students from around the world at the University of Alberta, Edmonton on July 10, 2014

TEACHING EXPERIENCE

Guest Talk, Vellore Institute of Technology, Vellore, India Aug 6, 2016

- Invited by Dr. S. Balamurugan to give a guest lecture on "**Design of Approximate Arithmetic Circuits and their real-time applications**"
- Addressed the audience consisting of graduate students and research scholars and presented my work on the design of approximate multipliers and their use in image processing

Professional/Teaching Assistant, BITS-Pilani, India Aug 2013 – Dec 2014

- Worked as a T.A. for various courses like **Microprocessors Programming & Interfacing, Analog & Digital VLSI Design**, **Microelectronic Circuits** and **Signals & Systems** and helped students in learning software like Proteus, Cadence Virtuoso, LT-Spice and MATLAB
- Conducted demo lab sessions and tests and assisted students with the design assignments

ACADEMIC PROJECTS

Implementation of 16x16 Compressor Based Approximate Multipliers Aug 2014 – Dec 2014

Guide: Dr. S. Gurunarayanan, Professor, Dept. of Electrical & Electronics Engg and Dean, Admissions and Work Integrated Learning Programmes (WILP), BITS-Pilani

- Proposed and implemented compressor based 16x16 approximate multipliers using the technique of recursive multiplication in VHDL and MATLAB and compared them on the basis of accuracy and circuit metrics (power, area and delay)
- Proposed designs achieve approximately 50% reduction in power and 20% reduction in circuit area over the accurate compressor based design

Building a Virtual Lab Aug 2014 – Dec 2014

Guide: Dr. S. Gurunarayanan, Professor, Dept. of Electrical & Electronics Engg and Dean, Admissions and Work Integrated Learning Programmes (WILP), BITS-Pilani

- Built a Virtual Lab on open source software like Electric VLSI and Scilab for WILP students of BITS-Pilani

Operational Amplifier Design Aug 2013 – Dec 2013

Guide: Dr. Anu Gupta, Associate Professor, Head of Dept. of Electrical & Electronics Engg, BITS-Pilani

- Designed & simulated a two stage folded cascode op-amp and met challenging specifications of gain, bandwidth and phase margin on Cadence Virtuoso ADE and Spectre Circuit Simulator

3-input AND/NAND Gate Design Aug 2013 – Dec 2013

Guide: Dr. Anu Gupta, Associate Professor, Head of Dept. of Electrical & Electronics Engg, BITS-Pilani

- Designed a 3-input AND/NAND gate using pass transistor logic to achieve desired functionality
- Prepared its layout on Cadence Virtuoso Layout Suite, thus gaining an experience on how the circuits are fabricated

Signal Processing Techniques for Structural Health Monitoring (SHM) Aug 2013 – Dec 2013

Guide: Dr. Kota Solomon Raju, Scientist, Digital Systems Group, Central Electronics Engineering Research Institute (CEERI)-Pilani

- Studied various stages of SHM and different signal processing techniques used at every stage
- Implemented Discrete Wavelet Transform used for SHM in MATLAB and VHDL

Biometric Analysis using Iris Recognition Jan 2013 – May 2013

Guide: Dr. Abhijit R Asati, Assistant Professor, Dept. of Electrical & Electronics Engg, BITS-Pilani

- Implemented an Iris Recognition algorithm, employing pattern recognition algorithms using image processing toolbox in MATLAB and built an automated code for reading images from the MMU database for image matching

ACHIEVEMENTS

MITACS Globalink Scholar
Selected among 470 fellows for MITACS Globalink Fellowship 2014 from 8000+ applicants from the top universities of the world for a summer research-assistantship in Canada

Microsoft Code.Fun.Do.
Developed a Kinect application V-Braille for enabling blind people to type and won the Code.Fun.Do. competition organized by Microsoft in BITS-Pilani

Course Topper in Various Subjects
Stood as course topper in Microprocessors Programming and Interfacing, Signals & Systems and Microelectronic Circuits in a batch of 150 students of Electrical department. Also, topped the course Principles of Economics amongst 600 students

Best Design Prize
Learnt the complete RTL Design to GDSII flow for an SoC and won the Best Design Prize for designing an optimized transceiver in two Digital Design boot-camps held as part of TI's Make-an-Impact program for New College Graduates

SKILL SET

Hardware Implementation Languages:	Verilog, VHDL
Programming Languages:	C, C++, JAVA, PERL, Assembly Language
Technical Software:	Cadence Encounter Test, Cadence Incisive, Cadence Virtuoso, Xilinx ISE, Synopsys Design Suite, MATLAB & Simulink, LT-Spice, Proteus, Code Composer Studio, Electric VLSI, Scilab