A

REPORT

ON

ANALOG ASSIGNMENT

Prepared in partial fulfillment of the Course

Analog and Digital VLSI Design (INSTR\EEE F313)

By:

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1) Introduction:

1.1) Design and Operation of Op Amp:

Given specifications for our design are:

i) DC Gain ≥ 80 dB
ii) UGB ≥ 600 MHz
iii) Phase margin ≈ 55^0
iv) CMRR ≥120dB
v) PSRR ≥ 100dB

The configuration given was a single ended folded cascode op-amp. Since the gain requirements were extremely high hence we chose to use NMOS input differential pair for higher trans-conductance. And all similarly all NMOS input devices have been incorporated in the cascode stage as such a circuitry potentially provides a higher gain of op-amp because of greater mobility of the NMOS devices. For the second stage we chose to use a non-diode connected load again to increase the gain of the op-amp.

The op-amp functions as an unity gain buffer. To check its operation as an unity gain buffer. We gave a dc input and output was found to be equal to input DC voltage.

1.2) Design and Operation of Current Reference:

Most of the transistors in a folded cascade circuit require active biasing; therefore a dedicated biasing circuit is usually designed. The design used requires three different biasing points. The biasing circuit has been designed to provide these. Two biasing points are for PMOS bias and one for NMOS bias. The upper PMOS biases the current source and the lower PMOS biases the cascode stage. The NMOS in cascode are diode connected. NMOS of tail current source is biased from the biasing circuit.

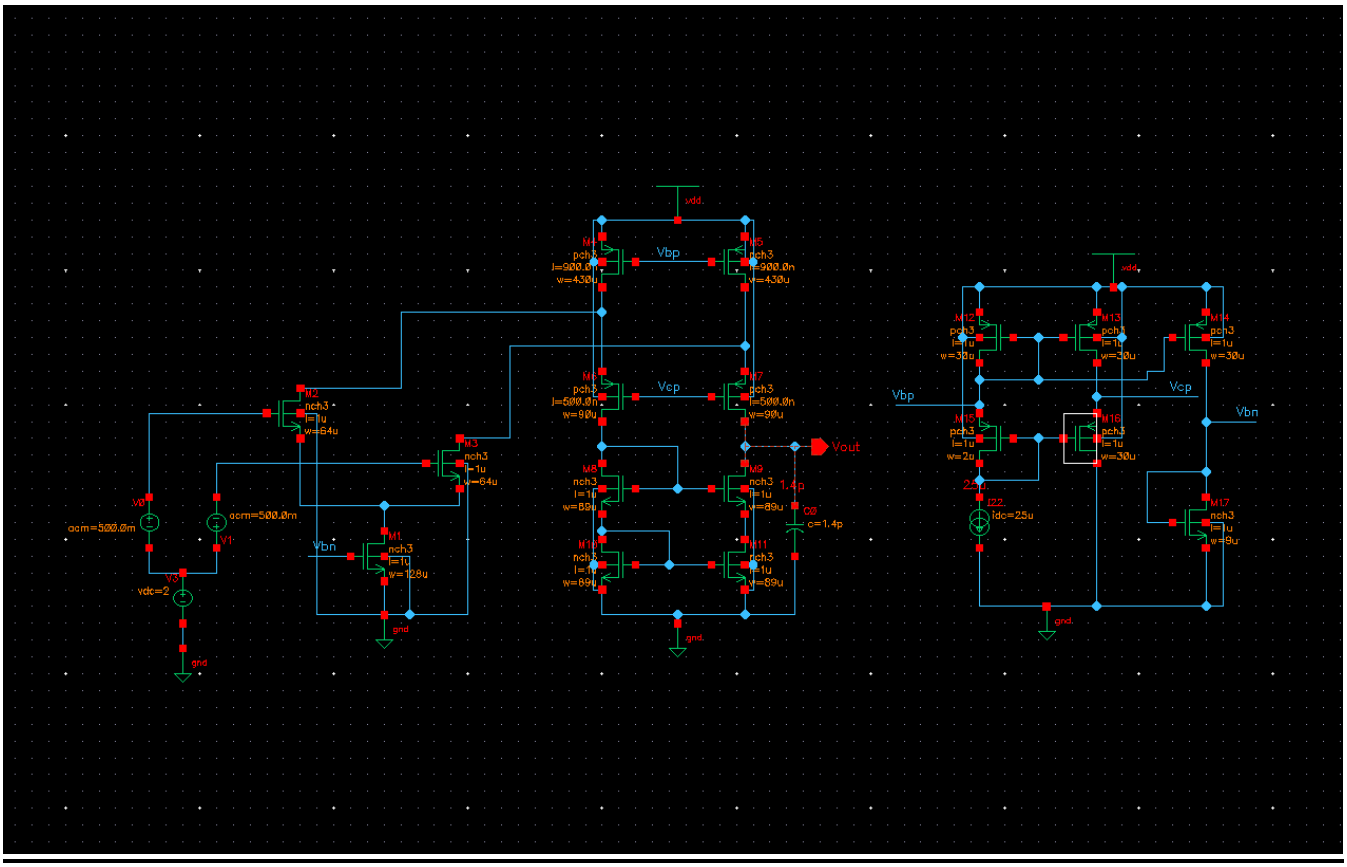
The PMOS requires biasing since a diode connection would reduce the Rout of the final stage, and hence the gain would reduce. An external biasing point helps in getting a higher gain from the second stage.

In the biasing circuit, we first calculated the gate voltages that were required for biasing. The reference current in the ideal current source is taken to be 25uA. Using this reference current and the Vgs-Vt values for the biasing MOSFETs, we calculated the W/L values. The biasing circuit used is made using λ mismatch. The PMOS bias resulted in saturation of the cascode

stage PMOSs. But the W/L of the PMOS had to be adjusted in order to bring both MOSFETs of cascode stage to saturation.

2) Operational Amplifier

2.1) Circuit Diagram:



2.2) Details of Circuit Realisation:

Given parameters: Power consumption <= 3mW, Vdd=3.3V

The circuit comprises of 3 biasing branches and 4 branches of the main op-amp circuitry (as shown in the figure below).

Since the current requirement of the biasing circuit is too less in comparison to the main circuitry, we start the calculation by assuming the current to be negligible in the biasing circuitry. Hence, the current in each main branch is given by the power requirement as shown below:

Vdd*5I=Power consumed (where I = current in each main branch)

⇨ $3.3V*I_{total}=3mW$

⇨ $I_{total}=0.1818$ mA

Hence total current = 0.909mA

We take 9% of this total current to be the biasing current, hence

Biasing current =0.075mA

Main circuit current=0.834 mA

Hence current in each main branch=0.834mA/2=0.417mA

Hence current in each biasing branch=0.025mA

CALCULATIONS OF W/L OF ALL MOSFETs

Using the gm/Id method

For NMOS, $g_m/I_d=11$

For W/L=1, Id= 2.43uA,

For PMOS, $g_m/I_d=8$

For W/l=1, I_d=0.94uA

Now, in order to bias the PMOSs we set using

Calculations:

Using the current equation for MOS in saturation region:

I_d distribution – We distribute 417 uA as as 200uA (in differential branch) 215 uA (in cascode branch)

$(W/L)_4 = (W/L)_5 =$ 417u/0.94u → 482

Similarly for the middle set of PMOS pair

$(W/L)_6 = (W/L)_7$ = 215u/0.94u → 180

Similarly for lower 2 pairs of NMOSs,

$(W/L)_8 = (W/L)_9 = (W/L)_{10} = (W/L)_{11}$ =215u/2.45u → 90

Now, for differential branch, the input NMOSs

$(W/L)_2 = (W/L)_3$ = 180u/2.45u → 64 (Lower than maximum power)

Now for tail current NMOS

$(W/L)_1$ = 360u/2.45u → 128

CALCULATIONS FOR BIAS

FOR NMOS

$(W/L)_{17}$ = 22u/2.45u → 9

FOR PMOS

$(W/L)_{12} = (W/L)_{13} = (W/L)_{14} = (W/L)_{16}$ =25u/0.94u → 30

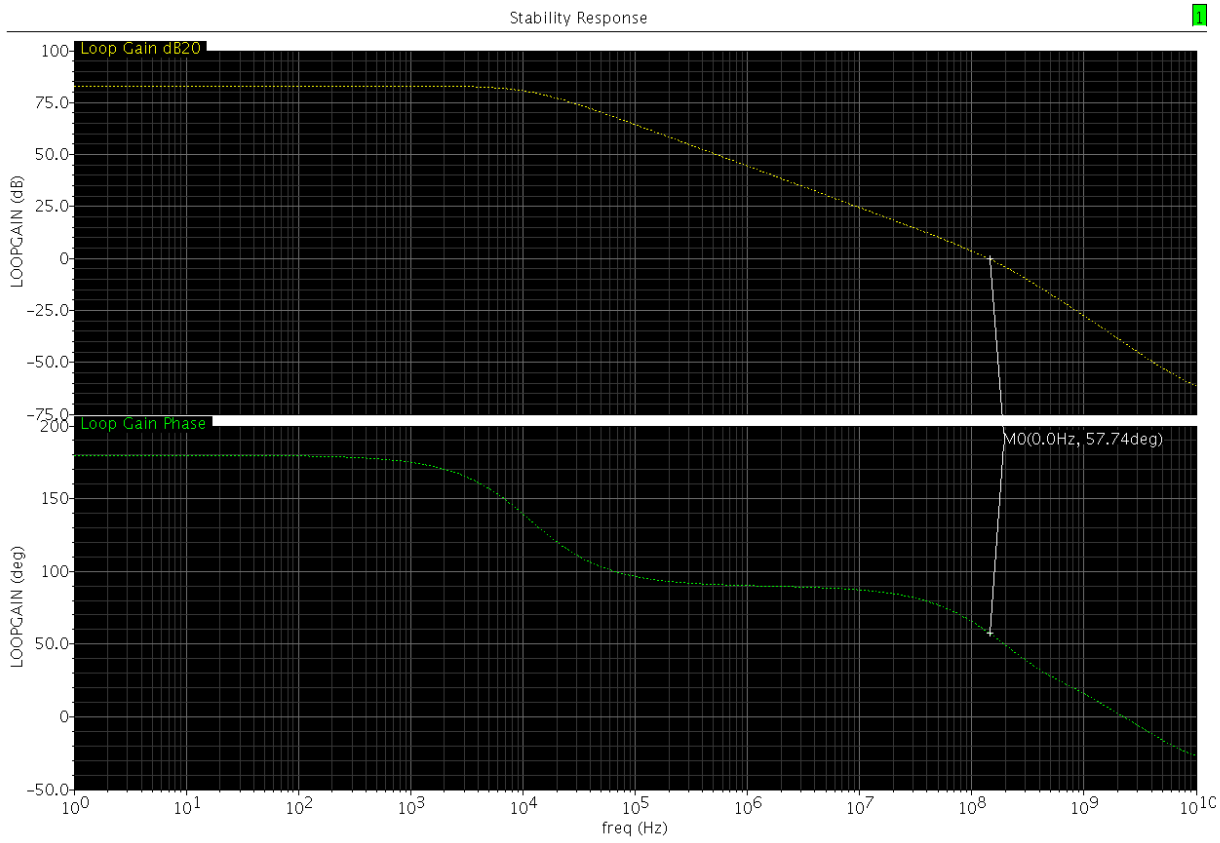
For using λ mismatch

We use **$(W/L)_{15}$ = 2u/1u → 2 (mismatched)**

2.3) Analysis and Results:

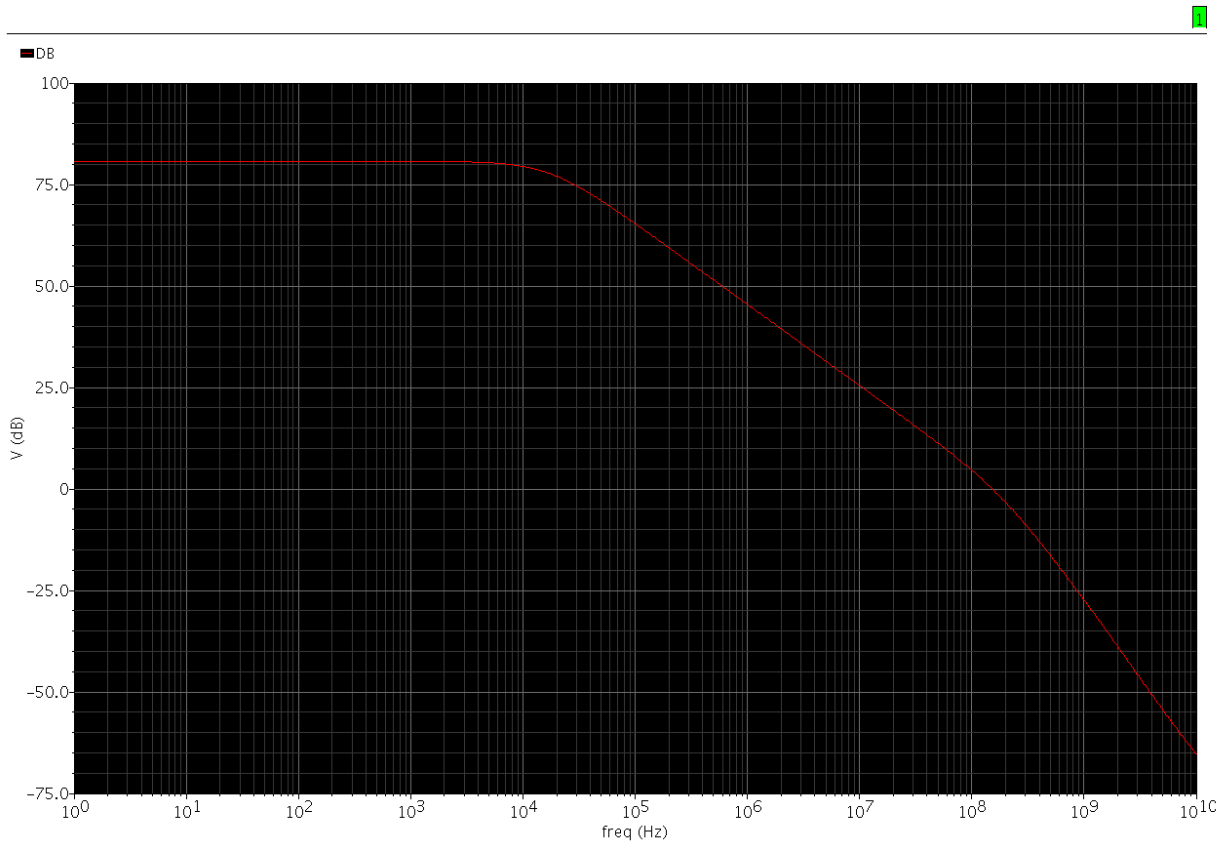
1) STB analysis:

Resulting plots:



2) Bode Plots:

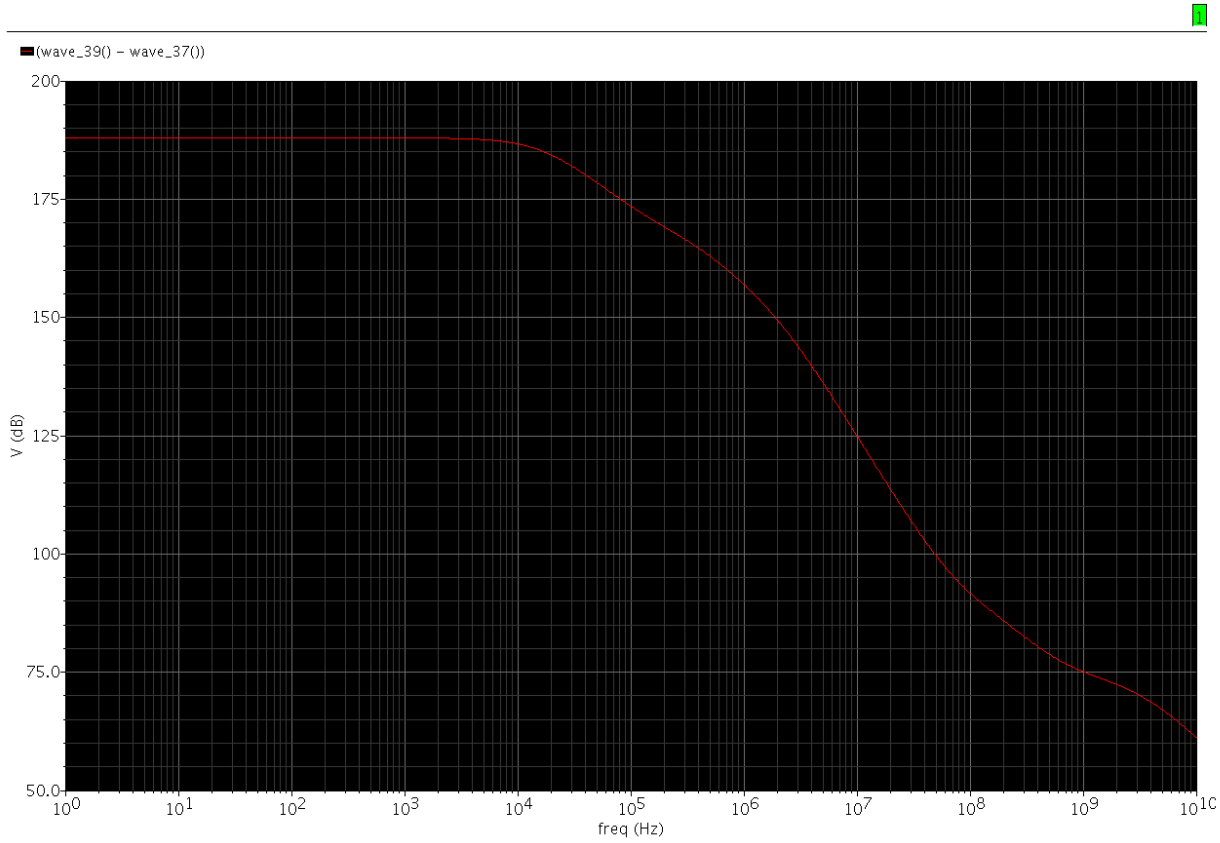
For AC Gain:



DC gain (from graph) (A_d) = 80.7 dB

3) CMRR:

Plot:


1
(wave_39() – wave_37())
200
175
150
125
100
75.0
50.0
V (dB)
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^{10}
freq (Hz)

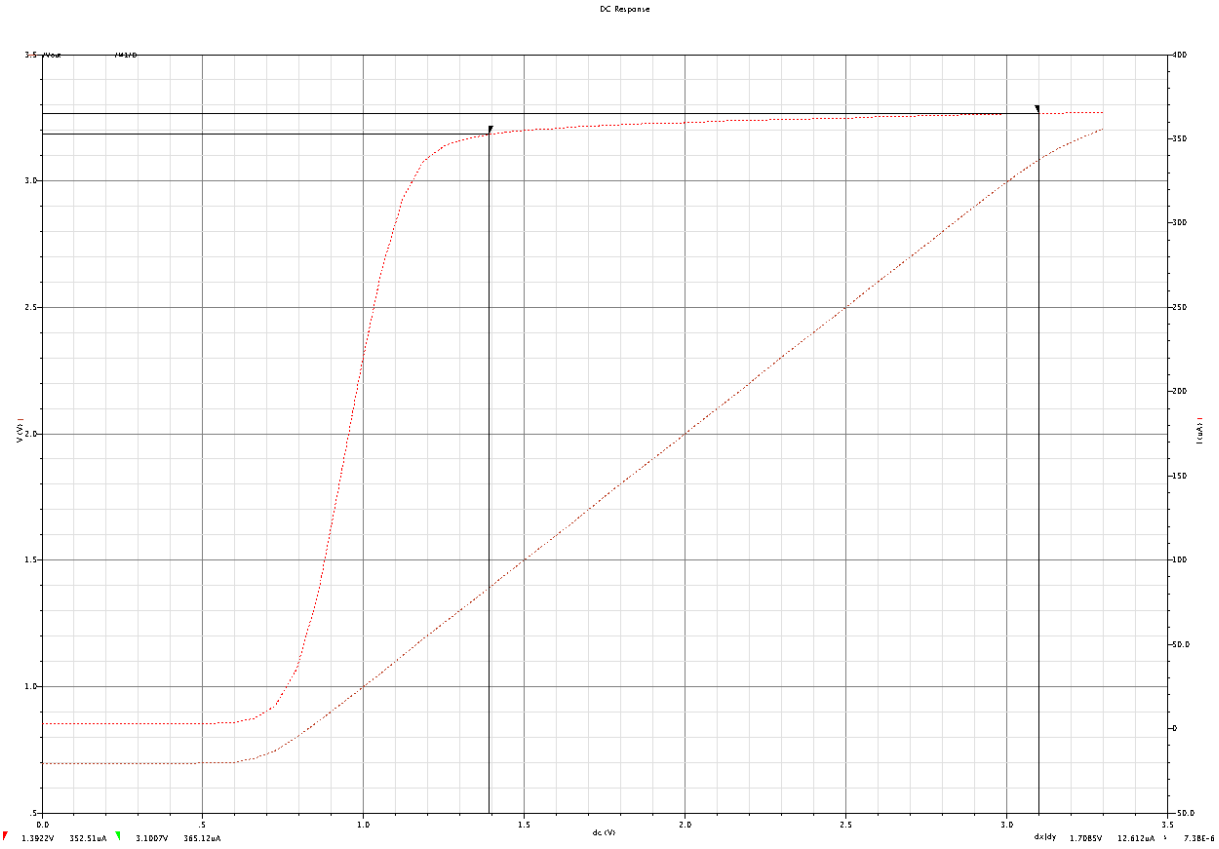
4) ICMR:

By observing the region of the graph where V_{in} and V_{out} are equal, we obtain:

Lower limit= 1.3922 V

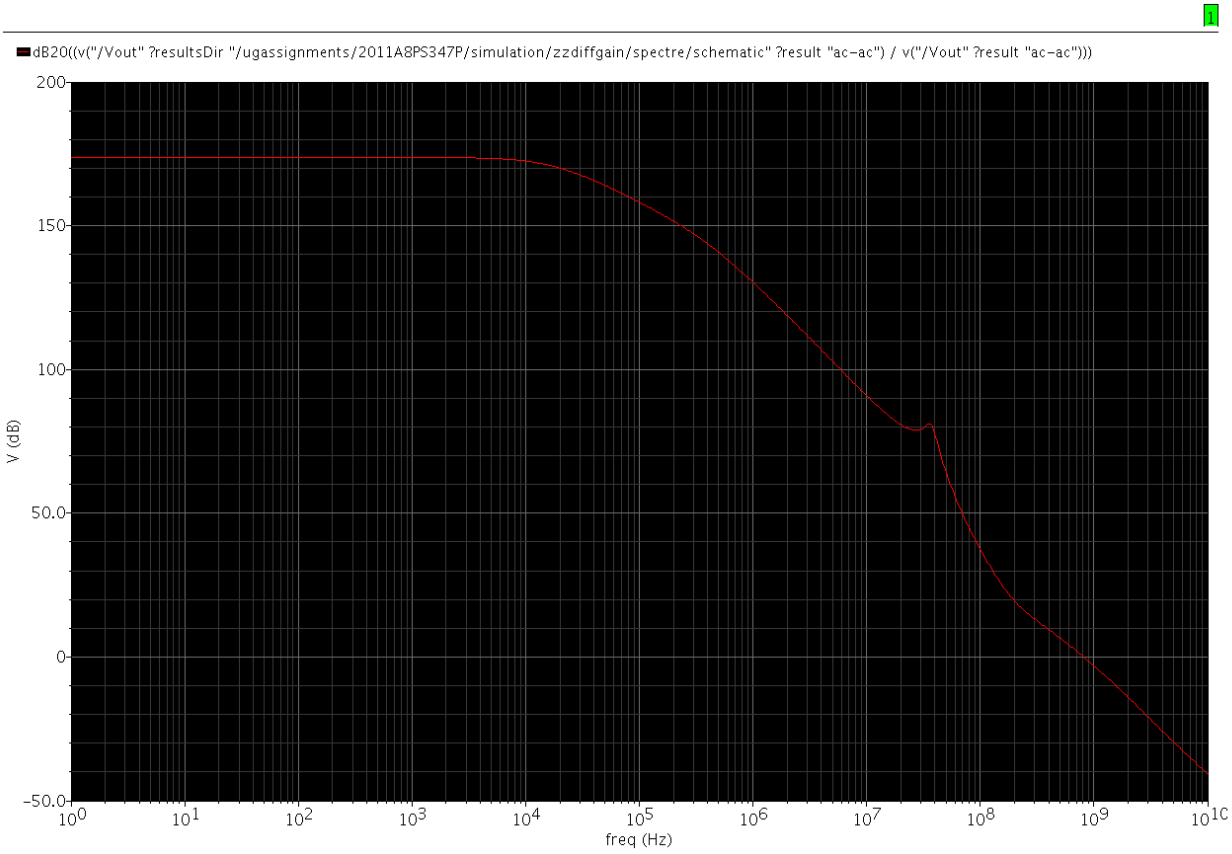
Upper limit= 3.007V

ICMR= Upper limit- Lower limit= 3.007-1.3922 V= 2.6V



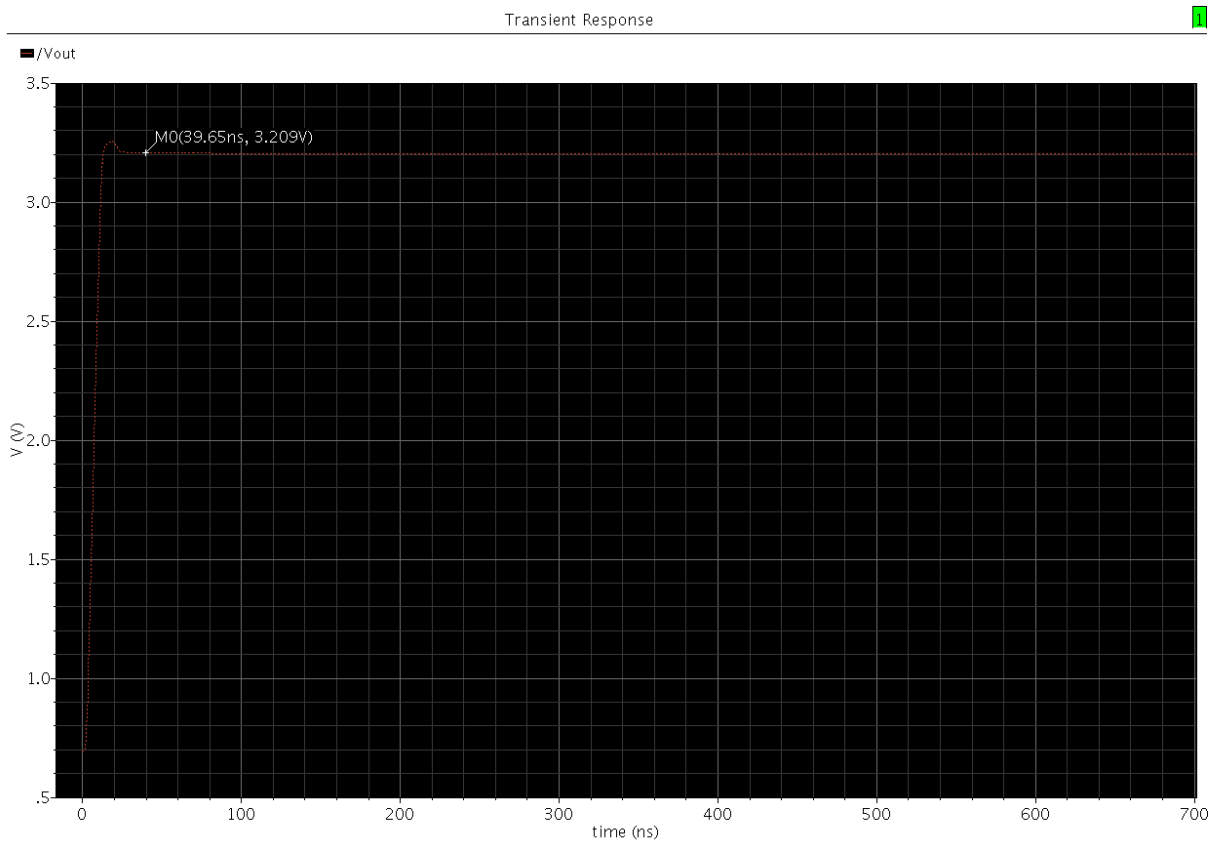
5) PSRR:

Plot


1
dB20((v("/Vout" ?resultsDir "/ugassignments/2011A8PS347P/simulation/zzdiffgain/spectre/schematic" ?result "ac-ac") / v("/Vout" ?result "ac-ac")))
200
150
100
50.0
0
-50.0
V (dB)
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^10
freq (Hz)

6) Slew Rate:

Plot



Slew rate= 240 V/μs

Settling time= 39ns

7) Output voltage swing:

Output voltage swing= Upper limit - Lower limit = 2.6 V

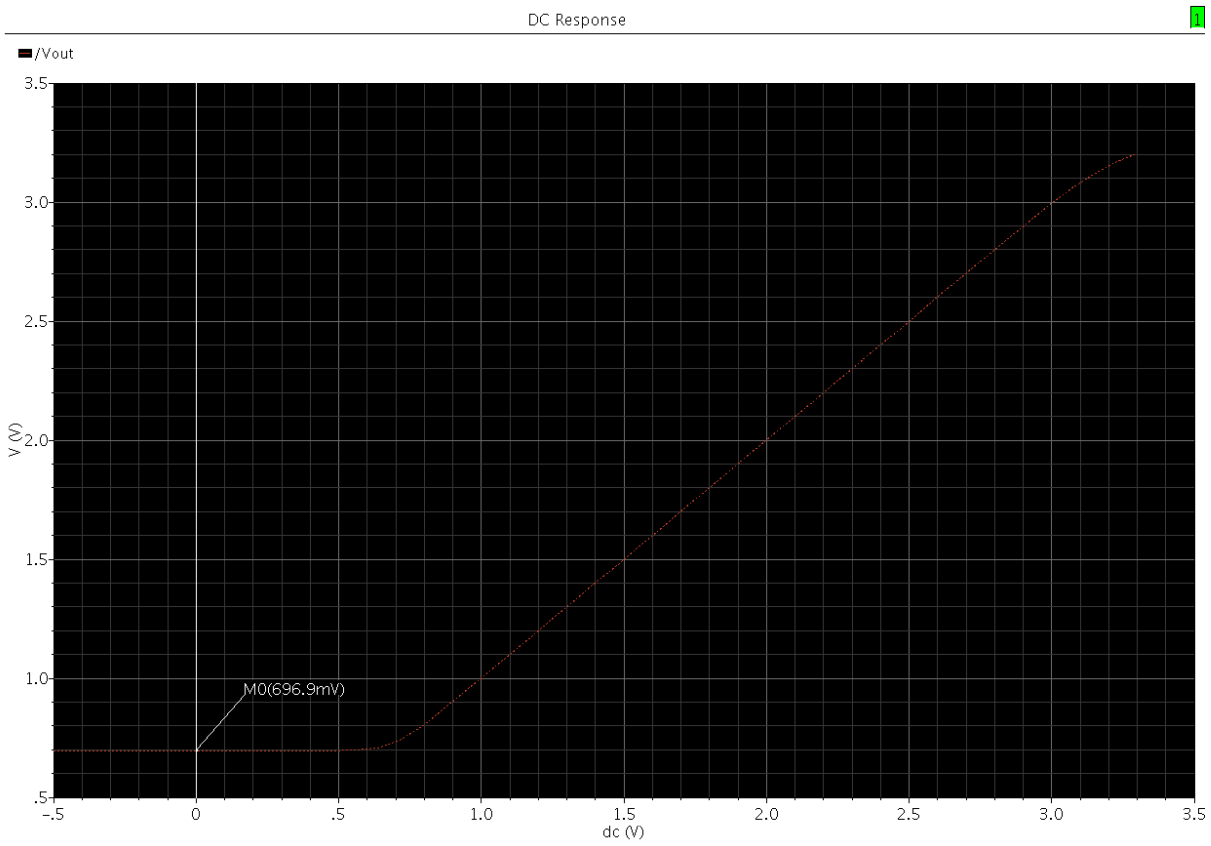
8) Power consumption:

By running analysis for the dc operating point we obtained the following power consumption for the circuit:

Power consumption= 2.85mW

9) Offset voltage:

From the graph, Output offset voltage= 696.9 mV

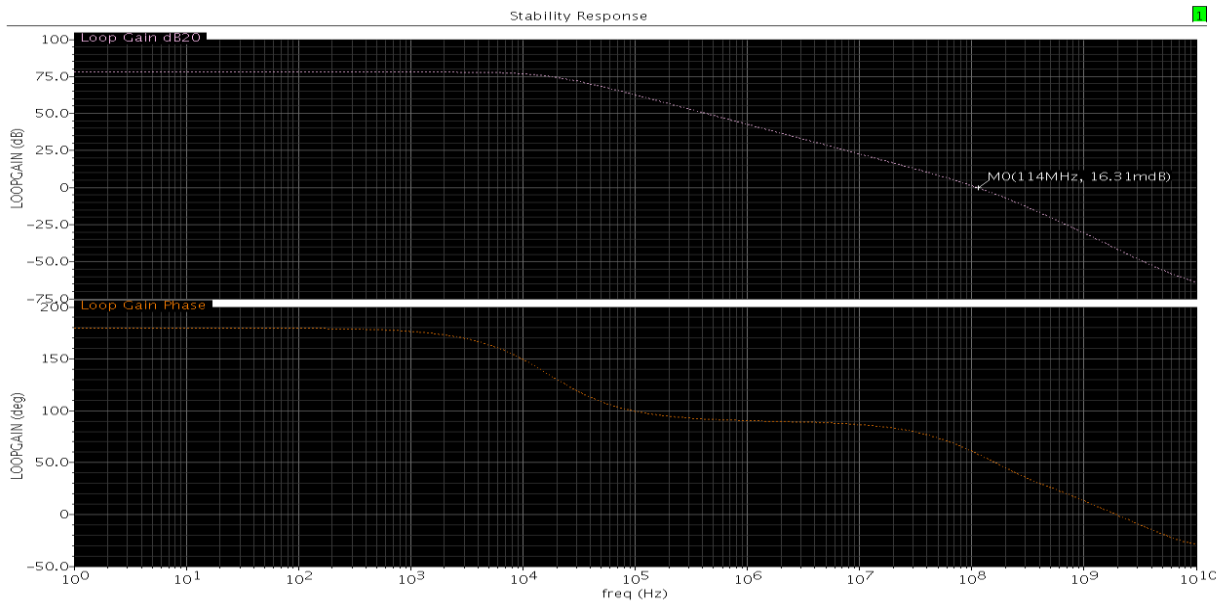


11) Process Corners:

Using STB analysis, we have verified our design for the process corners specified, with respect to gain and phase margin constraints. The design has also been checked for voltage swing.

11.1) For FF, +10% V_{dd}, 0^{o}C:

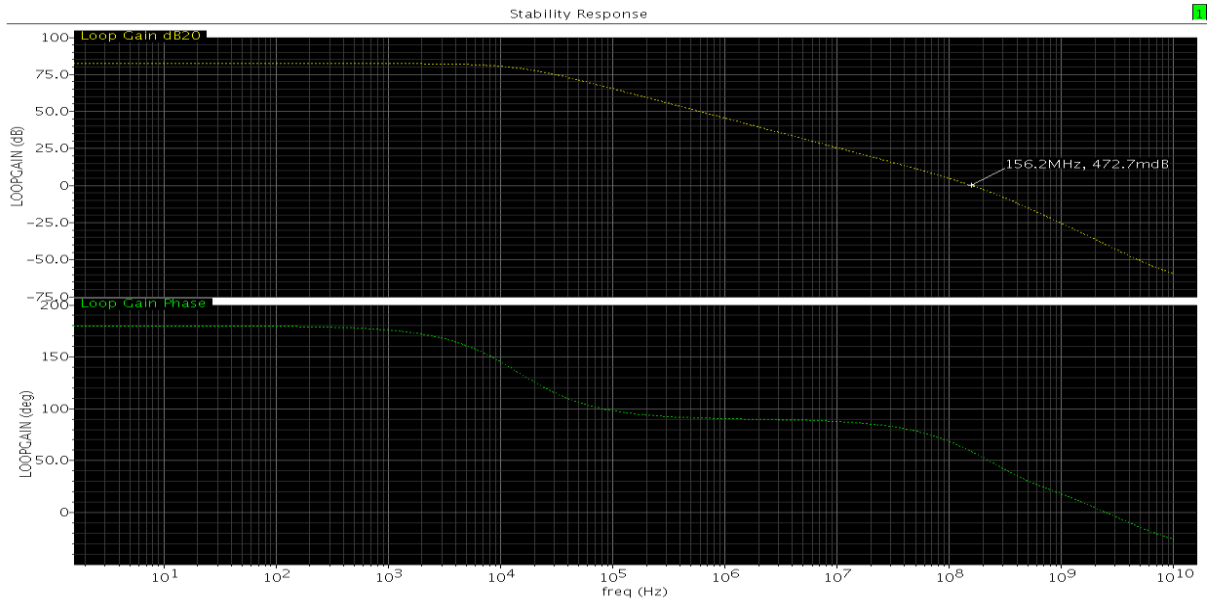
Resulting plots:



Gain= 82.011dB (Approx.) Phase margin= 58.5°

11.2) For SS, -10%V_{dd}, 100°C:

Resulting plots:



Gain= 74.32dB (Approx.) Phase margin= 58.48°

2.4) Table of Results:

For TT:

Sl. No.	Quantity	Value	Required Specifications
1	DC Gain	80.7 dB	80dB
2	Phase Margin	54.99^o	55^o
3	Output Swing	2.6 V	
4	Output DC Offset	696.9 mV	
5	Input DC Offset	0.064 mV	
6	Slew Rate	240 V/µs	
7	Settling Time	39 ns	
9	CMRR	185 dB	120 dB
11	PSRR	173 dB	100 dB
12	ICMR	1.3922 V - 3.007 V	
13	Power Dissipation	2.86 mW	3mW
14	Unity Gain Bandwidth	153 MHz	600 MHz
15	3dB frequency	15.17 kHz	

For FF:

Sl. No.	Quantity	Value	Required Specifications
1	DC Gain	82.011dB	80dB
2	Phase Margin	55.32^o	55^o
3	Unity Gain Bandwidth	172 MHz	600 MHz

For SS:

Sl. No.	Quantity	Value	Required Specifications
1	DC Gain	74dB	80dB
2	Phase Margin	56.04^o	55^o
3	Unity Gain Bandwidth	119.68 MHz	600 MHz

4) Trade-OFFs

We can see that in the circuit made, there is a tradeoff between Phase Margin, UGB and Gain. Only 2 out of three can be achieved while considering all the given requirement and specifications.

In the final circuit, if we want to attain more UGB, we need to increase current, which in turn reduces R_{out} of the circuit and hence reduces the gain.

If we use smaller W/L_s for all transistors, we can achieve better UGB and gain but with bad Phase margin and stability with the given load capacitance.

Hence, tradeoff was observed and a final circuit was made, by changing Ls of different transistors, in order to shift the poles and obtain the best possible specifications for the circuit, closest to the requirements, handling tradeoff.

5) Conclusions:

We therefore conclude that the design we have implemented has met all the required specifications while giving minimal power consumption. The circuit has been successfully verified at the process corners FF, +10%V_{dd}, 0^{o}C, and SS,-10%V_{dd}, 100^{o}C. The design also gives high PSRR, CMRR, ICMR and slew rate with a short settling time.

5) References:

- NDesign of Analog CMOS Integrated Circuits, BehzadRazavi
- Electronic Design Automation Handbook, Dirk Jansen
- NordianaMukahar, ShamianZainal, “Design and Analysis of Operational Amplifier using VLSI software”, International Journal of Undergraduate Studies, 2012
- Satoshi Sakurai, Seyed R. Zarabadi, Mohammed Ismad, “Folded-Cascode CMOS OperationalAmplifier with Slew Rate Enhancement Circuit”, The Ohio State University