

# 1. Description

## 1.1. Project

Project Name	LTDC_800x480
Board Name	custom
Generated with:	STM32CubeMX 6.14.0
Date	03/25/2025

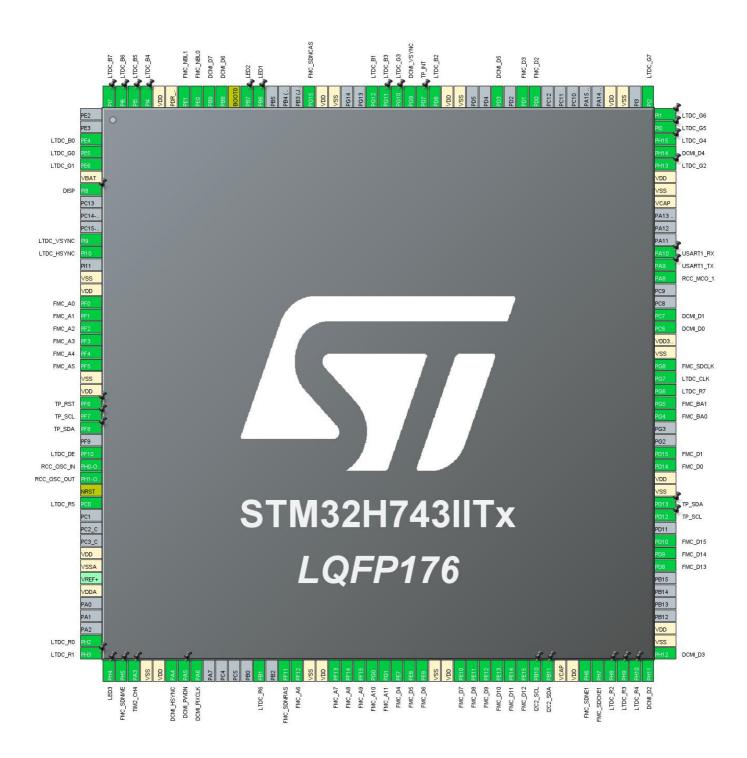
## 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743IITx
MCU Package	LQFP176
MCU Pin number	176

## 1.3. Core(s) information

Core(s)	ARM Cortex-M7

## 2. Pinout Configuration



# 3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP176	(function after		Function(s)	
	reset)			
3	PE4	I/O	LTDC_B0	
4	PE5	I/O	LTDC_G0	
5	PE6	I/O	LTDC_G1	
6	VBAT	Power		
7	PI8 *	I/O	GPIO_Output	DISP
11	PI9	I/O	LTDC_VSYNC	
12	PI10	I/O	LTDC_HSYNC	
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	FMC_A0	
17	PF1	I/O	FMC_A1	
18	PF2	I/O	FMC_A2	
19	PF3	I/O	FMC_A3	
20	PF4	I/O	FMC_A4	
21	PF5	I/O	FMC_A5	
22	VSS	Power		
23	VDD	Power		
24	PF6 *	I/O	GPIO_Output	TP_RST
25	PF7 *	I/O	GPIO_Input	TP_SCL
26	PF8 *	I/O	GPIO_Input	TP_SDA
28	PF10	I/O	LTDC_DE	
29	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
30	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
31	NRST	Reset		
32	PC0	I/O	LTDC_R5	
36	VDD	Power		
37	VSSA	Power		
39	VDDA	Power		
43	PH2	I/O	LTDC_R0	
44	PH3	I/O	LTDC_R1	
45	PH4 *	I/O	GPIO_Output	LED3
46	PH5	I/O	FMC_SDNWE	
47	PA3	I/O	TIM2_CH4	
48	VSS	Power		
49	VDD	Power		
50	PA4	I/O	DCMI_HSYNC	

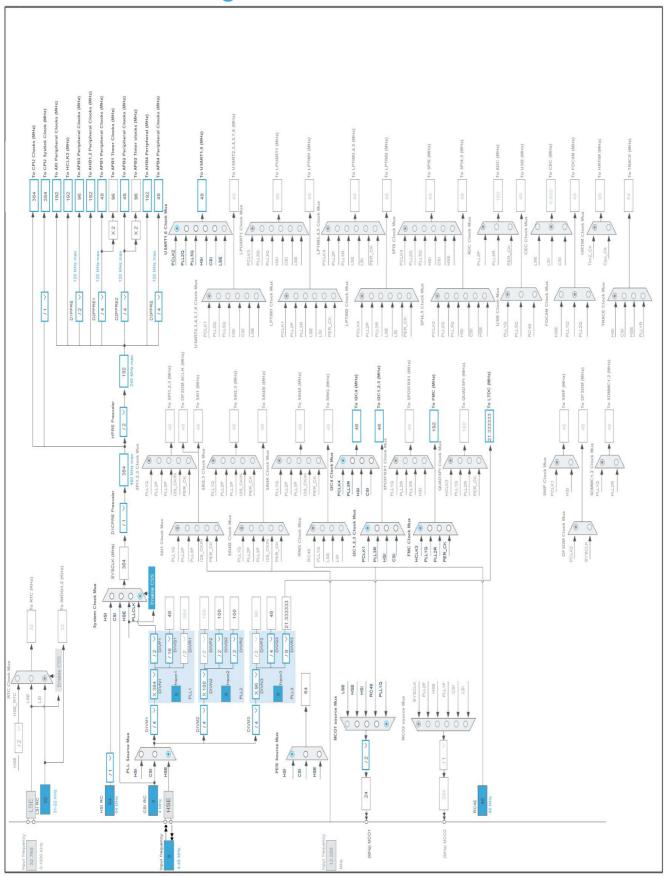
Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
51	PA5 *	I/O	GPIO_Output	DCMI_PWDN
52	PA6	I/O	DCMI_PIXCLK	
57	PB1	I/O	LTDC_R6	
59	PF11	I/O	FMC_SDNRAS	
60	PF12	I/O	FMC_A6	
61	VSS	Power		
62	VDD	Power		
63	PF13	I/O	FMC_A7	
64	PF14	I/O	FMC_A8	
65	PF15	I/O	FMC_A9	
66	PG0	I/O	FMC_A10	
67	PG1	I/O	FMC_A11	
68	PE7	I/O	FMC_D4	
69	PE8	I/O	FMC_D5	
70	PE9	I/O	FMC_D6	
71	VSS	Power		
72	VDD	Power		
73	PE10	I/O	FMC_D7	
74	PE11	I/O	FMC_D8	
75	PE12	I/O	FMC_D9	
76	PE13	I/O	FMC_D10	
77	PE14	I/O	FMC_D11	
78	PE15	I/O	FMC_D12	
79	PB10	I/O	I2C2_SCL	
80	PB11	I/O	I2C2_SDA	
81	VCAP	Power		
82	VDD	Power		
83	PH6	I/O	FMC_SDNE1	
84	PH7	I/O	FMC_SDCKE1	
85	PH8	I/O	LTDC_R2	
86	PH9	I/O	LTDC_R3	
87	PH10	I/O	LTDC_R4	
88	PH11	I/O	DCMI_D2	
89	PH12	I/O	DCMI_D3	
90	VSS	Power		
91	VDD	Power		
96	PD8	I/O	FMC_D13	
97	PD9	I/O	FMC_D14	
98	PD10	I/O	FMC_D15	
	<u> </u>		<u> </u>	

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP176	(function after		Function(s)	
	reset)			
100	PD12	I/O	I2C4_SCL	TP_SCL
101	PD13	I/O	12C4_SDA	TP_SDA
102	VSS	Power	.2005/.	05/
103	VDD	Power		
104	PD14	I/O	FMC_D0	
105	PD15	I/O	FMC_D1	
108	PG4	I/O	FMC_BA0	
109	PG5	I/O	FMC_BA1	
110	PG6	I/O	LTDC_R7	
111	PG7	I/O	LTDC_CLK	
112	PG8	I/O	FMC_SDCLK	
113	VSS	Power		
114	VDD33_USB	Power		
115	PC6	I/O	DCMI_D0	
116	PC7	I/O	DCMI_D1	
119	PA8	I/O	RCC_MCO_1	
120	PA9	I/O	USART1_TX	
121	PA10	I/O	USART1_RX	
125	VCAP	Power		
126	VSS	Power		
127	VDD	Power		
128	PH13	I/O	LTDC_G2	
129	PH14	I/O	DCMI_D4	
130	PH15	I/O	LTDC_G4	
131	PI0	I/O	LTDC_G5	
132	PI1	I/O	LTDC_G6	
133	PI2	I/O	LTDC_G7	
135	VSS	Power		
136	VDD	Power		
142	PD0	I/O	FMC_D2	
143	PD1	I/O	FMC_D3	
145	PD3	I/O	DCMI_D5	
148	VSS	Power		
149	VDD	Power		
150	PD6	I/O	LTDC_B2	
151	PD7	I/O	GPIO_EXTI7	TP_INT
152	PG9	I/O	DCMI_VSYNC	
153	PG10	I/O	LTDC_G3	
154	PG11	I/O	LTDC_B3	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
155	PG12	I/O	LTDC_B1	
158	VSS	Power		
159	VDD	Power		
160	PG15	I/O	FMC_SDNCAS	
164	PB6 *	I/O	GPIO_Output	LED1
165	PB7 *	I/O	GPIO_Output	LED2
166	воото	Boot		
167	PB8	I/O	DCMI_D6	
168	PB9	I/O	DCMI_D7	
169	PE0	I/O	FMC_NBL0	
170	PE1	I/O	FMC_NBL1	
171	PDR_ON	Power		
172	VDD	Power		
173	PI4	I/O	LTDC_B4	
174	PI5	I/O	LTDC_B5	
175	PI6	I/O	LTDC_B6	
176	PI7	I/O	LTDC_B7	

<sup>\*</sup> The pin is affected with an I/O function

## 4. Clock Tree Configuration



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## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
мси	STM32H743IITx
Datasheet	DS12110_Rev8

## 1.2. Parameter Selection

Temperature	25
Vdd	3.0

## 1.3. Battery Selection

Battery	Alkaline(9V)	
Capacity	625.0 mAh	
Self Discharge	0.3 %/month	
Nominal Voltage	9.0 V	
Max Cont Current	200.0 mA	
Max Pulse Current	0.0 mA	
Cells in series	1	
Cells in parallel	1	

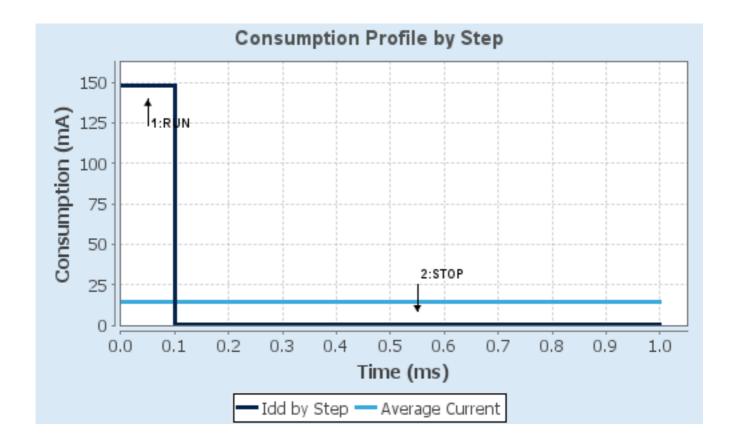
## 1.4. Sequence

		1
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.91	124.98
Category	In DS Table	In DS Table

## 1.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001
			DMIPS

### 1.6. Chart



# 2. Software Project

## 2.1. Project Settings

Name	Value	
Project Name	LTDC_800x480	
Project Folder	C:\Users\Butch\STM32CubeIDE\Waveshare\LTDC_800x480	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

## 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

## 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_DMA_Init	DMA
4	MX_FMC_Init	FMC
5	MX_USART1_UART_Init	USART1
6	MX_LTDC_Init	LTDC
7	MX_DMA2D_Init	DMA2D
8	MX_TIM2_Init	TIM2
9	MX_CRC_Init	CRC
10	MX_I2C4_Init	I2C4
11	MX_DCMI_Init	DCMI

Rank	Function Name	Peripheral Instance Name
12	MX I2C2 Init	I2C2

## 3. Peripherals and Middlewares Configuration

#### 3.1. CRC

mode: Activated

3.1.1. Parameter Settings:

#### **Basic Parameters:**

Default Polynomial State Enable

Default Init Value State Enable

**Advanced Parameters:** 

Input Data Inversion Mode None
Output Data Inversion Mode Disable
Input Data Format Bytes

#### 3.2. DCMI

**DCMI: Slave 8 bits External Synchro** 

### 3.2.1. Parameter Settings:

#### **Mode Config:**

Pixel clock polarity Active on Falling edge

Vertical synchronization polarity Active Low Horizontal synchronization polarity Active Low

Frequency of frame capture All frames are captured

JPEG mode Disabled

**Interface Capture Config:** 

Byte Select Mode Interface captures all received bytes
Line Select Mode Interface captures all received lines

#### 3.3. DMA2D

mode: Activated

#### 3.3.1. Parameter Settings:

#### **Basic Parameters:**

Transfer Mode Memory to Memory

Color Mode RGB565 \*

Output Offset 0

#### Foreground layer Configuration:

DMA2D Input Color Mode RGB565

DMA2D ALPHA MODE

No modification of the alpha channel value

Input Alpha 0
Input Offset 0

DMA2D ALPHA Inversion Regular Alpha

DMA2D Red and Blue swap

Regular mode (RGB or ARGB)

DMA2D Chroma Sub-Sampling Mode

No chroma sub-sampling 4:4:4

#### 3.4. FMC

#### SDRAM 1

Clock and chip enable: SDCKE1+SDNE1

Internal bank number: 4 banks

Address: 12 bits Data: 16 bits

Byte enable: 16-bit byte enable

3.4.1. SDRAM 1:

#### **SDRAM** control:

Bank SDRAM bank 2

Number of column address bits 8 bits
Number of row address bits 12 bits

CAS latency 3 memory clock cycles \*

Write protection Disabled

SDRAM common clock 2 HCLK clock cycles \*

SDRAM common burst read Disabled

SDRAM common read pipe delay 1 HCLK clock cycle \*

#### SDRAM timing in memory clock cycles:

Load mode register to active delay 2 \*

Exit self-refresh delay 7 \*

Self-refresh time 4 \*

SDRAM common row cycle delay 6 \*

Write recovery time 2 \*

SDRAM common row precharge delay 2 \*

#### 3.4.2. Bank Mapping:

Row to column delay

2 \*

#### **Mapping parameters:**

FMC bank mapping Default mapping

3.5. I2C2

12C: 12C

#### 3.5.1. Parameter Settings:

#### Timing configuration:

Custom Timing Disabled

I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz)100Rise Time (ns)0Fall Time (ns)0Coefficient of Digital Filter0

Analog Filter Enabled

Timing 0x20303E5D \*

#### **Slave Features:**

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

3.6. I2C4 I2C: I2C

### 3.6.1. Parameter Settings:

#### Timing configuration:

Custom Timing Disabled

I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz)100Rise Time (ns)0Fall Time (ns)0Coefficient of Digital Filter0

Analog Filter Enabled

Timing **0x20303E5D** \*

#### **Slave Features:**

Clock No Stretch Mode Enabled \*
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

#### 3.7. LTDC

## Display Type: RGB888 (24 bits)

### 3.7.1. Parameter Settings:

### **Synchronization for Width:**

Horizontal Synchronization Width	30 *
Horizontal Back Porch	46 *
Active Width	800 *
Horizontal Front Porch	6
HSync Width	29
Accumulated Horizontal Back Porch Width	75
Accumulated Active Width	875
Total Width	881

#### Synchronization for Height:

Vertical Synchronization Height	10 *
Vertical Back Porch	23 *
Active Height	480
Vertical Front Porch	22 *
VSync Height	9
Accumulated Vertical Back Porch Height	32
Accumulated Active Height	512
Total Height	534

#### **Signal Polarity:**

Horizontal Synchronization Polarity

Vertical Synchronization Polarity

Data Enable Polarity

Pixel Clock Polarity

Active Low

Normal Input

#### **Layer Default Color:**

Red	0
Green	0
Blue	0

### 3.7.2. Layer Settings:

**Layer Default Color:** 

 Layer 0 - Alpha
 0

 Layer 0 - Blue
 0

 Layer 0 - Green
 0

 Layer 0 - Red
 0

**Number of Layers:** 

Number of Layers 1 layer \*

**Windows Position:** 

Layer 0 - Window Horizontal Start 0

Layer 0 - Window Horizontal Stop 800 \*

Layer 0 - Window Vertical Start 0

Layer 0 - Window Vertical Stop 480 \*

**Pixel Parameters:** 

Layer 0 - Pixel Format RGB565 \*

Blending:

Layer 0 - Alpha constant for blending **0xff** \*

Layer 0 - Blending Factor1 Alpha constant
Layer 0 - Blending Factor2 Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress 0xD0000000 \*

Layer 0 - Color Frame Buffer Line Length (Image **800** \*

Width)

Layer 0 - Color Frame Buffer Number of Lines (Image 480 \*

Height)

#### 3.8. MEMORYMAP

mode: Activated

### 3.9. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

mode: Master Clock Output 1

3.9.1. Parameter Settings:

#### **Power Parameters:**

SupplySource PWR\_LDO\_SUPPLY

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

**RCC Parameters:** 

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000
CSI Calibration Value 32
HSI Calibration Value 64

**System Parameters:** 

VDD voltage (V) 3.3

Flash Latency(WS) 2 WS (3 CPU cycle)

Product revision rev.V

**PLL range Parameters:** 

PLL1 clock Input range

PLL3 input frequency range

Between 2 and 4 MHz

Between 2 and 4 MHz

PLL1 clock Output range

Wide VCO range

Wide VCO range

3.10. SYS

**Timebase Source: SysTick** 

3.11. TIM2

Channel4: PWM Generation CH4

3.11.1. Parameter Settings:

**Counter Settings:** 

Prescaler (PSC - 16 bits value) 100-1 \*

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value ) 1000-1 \*

Internal Clock Division (CKD) No Division auto-reload preload Enable \*

**Trigger Output (TRGO) Parameters:** 

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx\_EGR)

Clear Input:

Clear Input Source Disable

**PWM Generation Channel 4:** 

Mode PWM mode 1

Pulse (32 bits value) 500 \*

Output compare preload Enable
Fast Mode Disable
CH Polarity High

#### 3.12. USART1

### **Mode: Asynchronous**

### 3.12.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

#### **Advanced Parameters:**

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration Rxfifo Threshold 1 eighth full configuration

#### **Advanced Features:**

Auto Baudrate Disable Disable TX Pin Active Level Inversion **RX Pin Active Level Inversion** Disable Data Inversion Disable TX and RX Pins Swapping Disable Overrun Enable DMA on RX Error Enable MSB First Disable

#### \* User modified value

# 4. System Configuration

## 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
DCMI	PA4	DCMI_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	DCMI_PIXCLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH11	DCMI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH12	DCMI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	DCMI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	DCMI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH14	DCMI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	DCMI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG9	DCMI_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	DCMI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	DCMI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH7	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	1111	- WO_ODONET	Automato i unotioni i usii Fuli	110 pair up and 110 pair-aowii	very riigir	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up *	High *	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up *	High *	
I2C4	PD12	I2C4_SCL	Alternate Function Open Drain	Pull-up *	High *	TP_SCL
	PD13	I2C4_SDA	Alternate Function Open Drain	Pull-up *	High *	TP_SDA
LTDC	PE4	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC0	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH2	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH3	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH8	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH9	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH10	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH13	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH15	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI4	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI5	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI6	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI7	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PA8	RCC_MCO_1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PI8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISP
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TP_RST
	PF7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TP_SCL
	PF8	GPIO_Input	Input mode	Pull-up *	n/a	TP_SDA
	PH4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DCMI_PWDN
	PD7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	TP_INT
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2

## 4.2. DMA configuration

DMA request	Stream	Direction	Priority
DCMI	DMA2_Stream0	Peripheral To Memory	Low
USART1_TX	DMA1_Stream1	Memory To Peripheral	Low

### DCMI: DMA2\_Stream0 DMA request Settings:

Mode: Normal Use fifo: Enable \* FIFO Threshold: Full Peripheral Increment: Disable Memory Increment: Enable \* Peripheral Data Width: Word \* Word Memory Data Width: Peripheral Burst Size: Single Memory Burst Size: Single

### USART1\_TX: DMA1\_Stream1 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Byte
Memory Data Width: Byte

### 4.3. BDMA configuration

nothing configured in DMA service

### 4.4. MDMA configuration

nothing configured in DMA service

## 4.5. NVIC configuration

## 4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
		0	0		
System tick timer	true				
DMA1 stream1 global interrupt	true	0	0		
EXTI line[9:5] interrupts	true	0	0		
USART1 global interrupt	true	0	0		
DMA2 stream0 global interrupt	true	0	0		
DCMI global interrupt	true	0	0		
LTDC global interrupt	true	0	0		
DMA2D global interrupt	true	0	0		
PVD and AVD interrupts through EXTI line 16		unused			
Flash global interrupt		unused			
RCC global interrupt		unused			
TIM2 global interrupt		unused			
I2C2 event interrupt		unused			
I2C2 error interrupt		unused			
FMC global interrupt		unused			
FPU global interrupt		unused			
LTDC global error interrupt		unused			
I2C4 event interrupt	unused				
I2C4 error interrupt		unused			
HSEM1 global interrupt		unused			

## 4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false

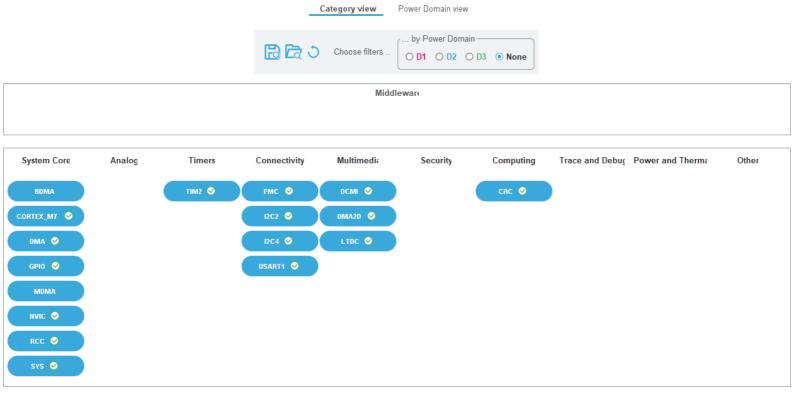
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream1 global interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true
USART1 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DCMI global interrupt	false	true	true
LTDC global interrupt	false	true	true
DMA2D global interrupt	false	true	true

<sup>\*</sup> User modified value

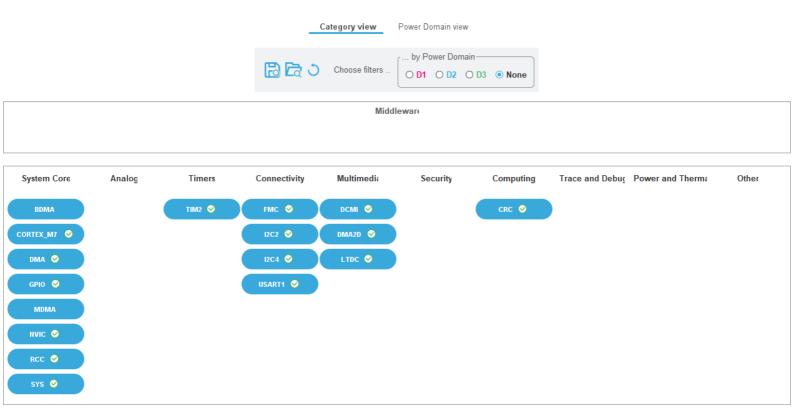
## 5. System Views

5.1. Category view

5.1.1. Current



## 5.1.2. Without filters



## 5.2. Power Domain view

D2 D3

DCMI ♥ BDMA

DMA ♥ CRC ♥

TIM2 🔗

USART1 ⊗

Power Domain view

Category view

D1

DMA2D 🤡

MDMA

## 6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl\_model/stm32h7\_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis\_model/stm32h7\_ibis.zip

System View https://www.st.com/resource/en/svd/stm32h7-svd.zip

Description

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m32h7\_series\_product\_overview.pdf

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stm8\_embedded\_software\_solutions.pdf

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